NASA Cooperative Agreement NCC 2-303

INVESTIGATION OF ADVANCED FAULT INSERTION AND SIMULATOR METHODS

FINAL TECHNICAL REPORT

covering the period
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Report Summary

The cooperative agreement partly supported research leading to the open-literature publication cited below.

Additional efforts under the agreement included research into fault modelling of semiconductor devices. Results of this research are presented in this report which is summarized in the following paragraphs.

As a result of the cited research, it appears that semiconductor failure mechanism data is abundant but of little use in developing pin-level device models. Failure mode data on the other hand does exist but is too sparse to be of any (statistical) use in developing fault models. What is significant in the failure mode data is that, unlike classical logic, MSI and LSI devices do exhibit more than "stuck-at" and open/short failure modes. Specifically they are dominated by parametric failures and functional anomalies that can include intermittent faults and multiple-pin failures.

The report discusses methods of developing composite pinlevel models based on extrapolation of semiconductor device failure mechanisms, failure modes, results of (temperature) stress testing and functional modelling. Limitations of this model particularly with regard to determination of fault detection coverage and latency time measurement are discussed.

Indicated research directions are presented.

Reference

Dunn, W.R., "Software Reliability: Measures and Effects in Flight Critical Digital Avionics Systems", 7th Digital Avionics Systems Conference, Fort Worth, Texas, October 13-16, 1986.

Notation

DTL = Diode-Transistor Logic

FMEA = Failure Modes & Effects Analysis

FMET = Failure Modes & Effects Tests

LSTTL = Low Power Schottky Transistor-Transistor Logic

RAC = Reliability Analysis Center

SSI = Small Scale Integration

VLSI = Very Large Scale Integration

INVESTIGATION OF ADVANCED FAULT INSERTION AND SIMULATOR METHODS

1.0 Introduction

In the design and development of a flight-critical digital system, it is necessary to prove that the system can tolerate single- and multiple-component faults. Two widely-used methods supporting such proof are Failure Modes and Effects Analysis (FMEA) and Failure Modes and Effects Testing (FMET). FMEA is usually performed very early in the design process either by hand or, in more complex systems, through fault simulation. FMET is performed toward the end of development and prior to initial flight test. In Failure Modes and Effects Testing, actual or simulated faults are inserted in the actual digital system (generally configured in ground-based, "iron bird" environment) in order to validate system fault tolerance. Both FMEA and FMET activities require knowledge of probable component failure modes.

This report addresses the subject of digital integrated circuit semiconductor failure modes. The study leading to the report was motivated by the suspicion that the permanent, "stuck- at" type failure modes characteristic of relay, transistor and small-scale integrated circuit logic might not fully embrace possible failure modes in many of the Medium Scale Integration (MSI) and Very Large Scale Integration (VLSI) components employed in modern, flight-critical digital system designs. The study was therefore undertaken with the (admittedly ambitious) objective of developing an approach for deriving practical fault models for MSI digital integrated circuits. The work was subject to two important, practical constraints:

1) Owing to limited resources, detailed study would be confined to a limited number of Low Power Schottky Transistor-Transistor Logic (LSTTL) devices. (These devices are extensively employed in modern flight systems.)

2) The study would employ only that semiconductor reliability data available to the general public. (Superior data lies within the semiconductor houses but is, in general, not available to the avionics designer.)

As the informed reader might suspect, it was quickly determined that the latter reliability data was of very limited usefulness in terms of fault model development.*

*At the time, workers at Hughes aircraft independently reached the same conclusion. See Reference 1.

For this reason, the originally-planned research activities were supplemented with laboratory stress testing of select LSTTL devices.

The remainder of this report is organized as discussed in the following.

Section 2.0 explains in detail what is meant by "fault model" and discusses past approaches to realizing fault models. Limitations of these models are discussed.

Section 3.0 presents definitions of semiconductor failure mechanisms and failure modes. Results of a USC survey and analysis of available failure mechanism and mode data bases are presented.

Section 4.0 describes several approaches to fault model development including use of semiconductor failure mode data and extrapolation of failure mechanism data. The section also contains a description of the test methodology and results of USC semiconductor stress testing.

Section 5.0 presents conclusions and indicated research directions.

2.0 Pin-Level Fault Modelling in Failure Modes and Effects Analysis and Testing

2.1 Pin Level Fault Model

Figure 2-1 shows the package outline of a general LSTTL device. In every device, two pins are dedicated to power supply source and return. The remaining pins are inputs and outputs. Under unfaulted conditions the device will output a predictable set of logic states (and/or state transitions) given a set of input states (and/or transitions) and (for sequential logic devices) a set of internal states. If there are failures internal to the device, output may be incorrect. To effect a pin-level fault model for the device, electrical characteristics at one or more pins are altered in such a manner that the resulting "new" device behaves exactly the same as the corresponding device with the internal failure.

In a FMEA these characteristics are introduced analytically. In a FMET, special circuitry is interposed between the good device and the system circuitry as shown in Figure 2-2 and altered characteristics are electrically introduced at the device pins. (Reference 2 & 3.)

This report focuses on approaches (and limitations) for determining these pin-level characteristics for failures that can occur within the device. (The term "fault modelling" is used in this report to describe this process.)

2.2 Gate-Level Fault Models

Prior to the introduction of integrated circuit logic (almost 30 years ago) it was relatively simple to correllate physical failures with the altered behavior of logic components. For example, the relay of Figure 2-3a could be associated with four fault characteristics: contact stuck-open, contact stuck-closed, coil short-circuited and coil open-circuited. Discrete component logic could be handled in a similar manner. For example, in the discrete component, diode-transistor-logic (DTL) gate of Figure 2-3b, one could directly associate known physical failures (open and shorted resistors, open diodes, collector-base opens, open solder joints, etc.) with behavior at the input/output terminals of the circuit.

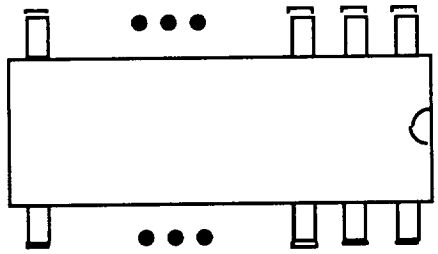


FIGURE 2-1 PACKAGE OUTLINE - LSTTL DEVICE

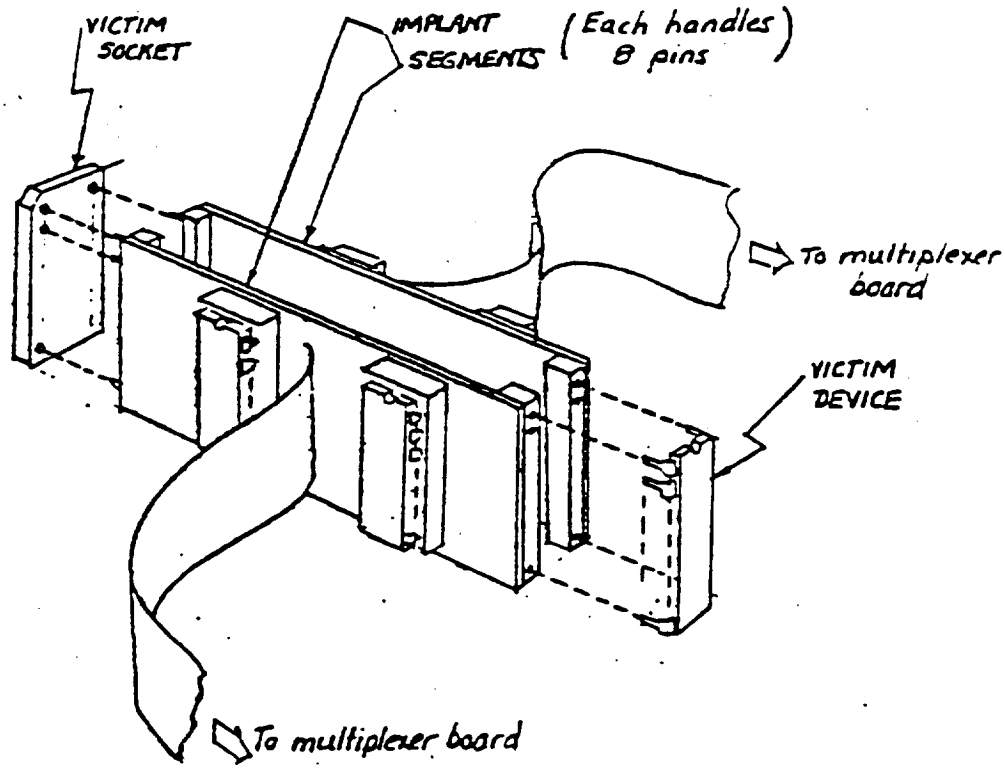
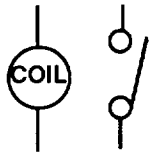
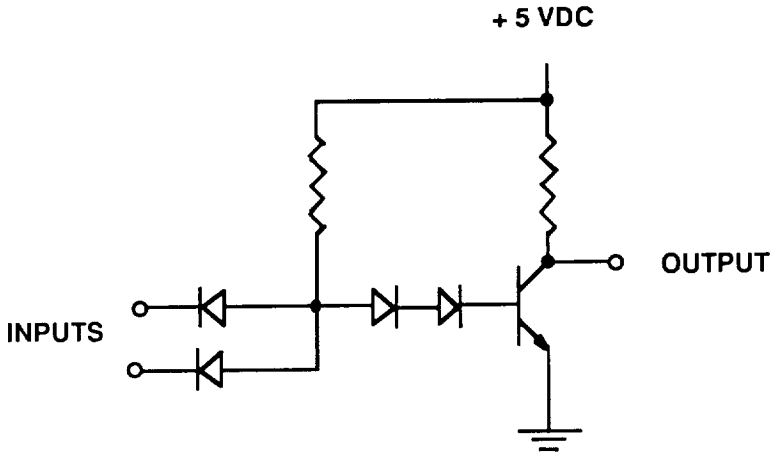


FIGURE 2-2 FAULT INSERTION CIRCUITRY



(a) Relay



(b) Discrete Diode-Transistor Logic

FIGURE 2-3 EARLY LOGIC DEVICES

The first digital integrated circuits consisted of single gates (such as the DTL gate of Figure 2-3b) implemented on a single chip. For reasons to be explained shortly (Section 3.3), on-chip physical failure mechanisms could not be translated to behavior at the output terminals. Instead, physical failures were considered in terms of altered behavior at the gate inputs and outputs which could be stuck-at-1, stuck-at-0, open-circuited or short-circuited. Realistic FMEAs and FMETs could be performed for early systems employing these small scale, integrated gates by successively applying each of these failure characteristics to each pin in the logic circuit.

2.3 Limitations of Gate-Level Fault Models

This report is concerned with fault modelling of commercial, non-custom MSI, LSI and VLSI digital semiconductor devices. (As noted, USC detailed studies were confined to LSTTL SSI and MSI devices. Findings with these specific devices appear however to apply to higher levels of integration and to other semiconductor technologies.) In attempting to apply classical, gate-level fault modelling to this class of devices, one encounters several practical roadblocks:

1) With a few exceptions, semiconductor manufacturers do not provide gate-level circuit schematics of their integrated devices. Consequently, one cannot perform a gate-level FMEA.

2) With early gate-level circuitry, it was possible to perform fault insertions (as a part of FMET) by opening and/or shorting gate inputs and outputs. In MSI and LSI, gates are integrated on the chip with the result that internal gate imputs and outputs cannot be physically accessed.

3) As will be seen in the next section, failure mechanisms within the device can lead to failure modes other than open-circuit, short-circuit and stuck-at behavior at the device pins.

3.0 Semiconductor Failure Mechanisms and Modes

3.1 Definitions

In what follows, the term <u>failure mechanism</u> refers to a physical anomaly within the device. <u>Failure mode</u> refers to altered electrical characteristics and/or behavior as a result of occurrence of the failure mechanism.

For example, a broken wire bond is a failure mechanism. It produces an open circuit failure mode at the pin to which it is connected.

3.2 Survey of Available Failure Mode and Failure Mechanism Data Bases

USC conducted a survey among some ten semiconductor manufacturers and three avionics firms in an effort to obtain failure mechanism and failure mode data to support pin-level fault modelling of select LSTTL devices. In the course of this survey, it was determined that these data are also collected by the DOD-sponsored Reliability Analysis Center (RAC) located at Griffiss AFB in New York.

Between the semiconductor manufacturers and the RAC, there is a copious amount of available data on digital semiconductor failure mechanisms. Failure mode data on the other hand is another matter. It is available only (with a few exceptions) from RAC which periodically publishes failure mechanism and failure mode data by semiconductor technology.

Tables 3-1 and 3-2 respectively summarize LSTTL failure mechanism and failure mode data taken from two RAC reports as referenced. Note that, in terms of the objectives of the study (to obtain pin level models of digital devices), these data represent the best* information gathered in the study.

3.3 Analysis of Failure Mechanism Data

With the exception of wirebond failures, it is virtually impossible to directly correlate semiconductor failure mechanisms with behavior at the device terminals. (Again, it is assumed that details of the chip circuitry and layout are not known.) The reason for this is that die defects (or package defects that lead to die contamination) can be very local (e.g. bad metal contact on a single emitter) or regional (e.g. an oxide contamination effecting several transistors). With each defect, the digital circuit structure can be altered. Given the range of possible combinations of defects one is inclined to speculate that a device could exhibit every possible combination of outputs for any given input (and input history in the case of a sequential circuit).

*We had originally hoped to find failure mode data for each chip type. Unfortunately, (RAC) published data on each device type is too fragmentary to attach any statistical significance to the distribution of failure modes of any given device.

TABLE 3-1 - LSTTL Failure Mechanisms

(SSI and MSI Devices)

Failure Mechanism (By Component)	1984 RAC Report (Ref. 4) No. of Devices	Percentage
Die:	68	25.1
Bulk Aspects	15	
Metallization	38	
Oxide/Dielectric	10	
Surface	5	
Interconnects:	24	8.8
Wire	9	
Wirebond	15	
Package:	179	66.1
Seal	116	
Lid	54	
Die Attach Bond	9	

TABLE 3-2 - LSTTL Device Failure Modes (Ref. 4)
(SSI and MSI Devices)

Failure Mode	Percent of Total	Adjusted**
OPEN	3.4	3.4
SHORT	4.1	4.1
DEGRADED	22.4	22.4
Unknown*	3.4	0.0
Leakage	6.1	7.2
Parameter Out-of-Tolerance	12.9	15.2
FUNCTIONAL ANOMALY	70.1	70.1
Unknown	57.2	0.0
Non-Functional	2.7	14.8
Improper Output	9.5	51.6
Stuck-at-1	0.0	0.0
Stuck-at-0	0.7	3.7

*"Unknown" means failure mode was in major category (DEGRADED or FUNCTIONAL ANOMALY) but sub-category (leakage, improper output, etc.) is not known.

**Unknowns allocated to known categories in proportion to known percentages of total.

3.4 Analysis of Failure Mode Data

Unlike failure mechanism data, failure mode data (Table 3-2) describe faulted behavior at the device pins. What stands out most in the table is that the majority of failure modes in LSTTL are not the classical open, short and stuck- at modes but functional, parametric and leakage failures. (Table 3-3, prepared from the same RAC report, shows expectedly, that failure modes for the obsolescent DTL technology fall principally in the former category.)

Excess leakage and parameter out-of-tolerance failure modes could have three effects in an operational digital flight system:

1) If sufficiently severe, they could produce a hard or permanent device failure.

2) If borderline, they could produce a soft or intermittent device failure. (In working with LSTTL devices, one occasionally encounters what's called a "flaky chip": a device that works correctly most of the time but not always.)

3) If below fault-activating thresholds, the device could be expected to function properly but with reduced life.

It is observed that in both DTL and LSTTL implementations, leakage and parametic failures can constitute a significant portion of latent faults. Unlike the "stuck-bit" latent fault, leakage and parametric failure modes could conceivably be missed in preflight built-in-test yet become activated in the harsher environment of flight.

LSTTL failure mode data of Table 3-4 for both life test and field application would seem to indicate the presence of such latent faults in fielded equipment. It is important to qualify this latter statement as well as all of the RAC data related to LSTTL failure modes. Specifically the failure mode distributions of Table 3-2 correspond to a limited number of devices that does not span the full range of device types. Table 3-5 shows significantly different failure mode distributions for two separate LSTTL samples, one taken in 1984 (the data of Table 3-2) and another taken in 1980 (Reference 5). (As suggested by Table 3-6, this difference in distributions does not appear to apply to DTL.)

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TABLE 3-3 - DTL Failure Modes (Ref. 4)

Failure Mode	Percent of Total	Percent Adjusted**
OPEN	0.0	0.0
SHORT	6.2	6.2
DEGRADED	18.8	18.8
Unknown*	15.6	0.0
Leakage	1.6	9.4
Parameter Out-of-Tolerance	1.6	9.4
FUNCTIONAL ANOMALY	75.0	75.0
Unknown	46.9	0.0
Non-Functional	1.6	4.2
Improper Output	1.6	4.2
Stuck-at-1	10.8	29.1
Stuck-at-0	14.1	37.5

*"Unknown" means failure mode was in major category (DEGRADED or FUNCTIONAL ANOMALY) but sub-category (leakage, improper output, etc.) is not known.

**Unknowns allocated to known categories in proportion to known percentages of total.

TABLE 3-4 - LSTTL Device Failure Modes
Life Test vs. Field

Failure Mode	Life Test Percent of Total	Field Percent of Total
OPEN	3.5	4.5
SHORT	2.8	4.5
DEGRADED	22.4	10.7
FUNCTIONAL ANOMALY	71.3	80.3

TABLE 3-5 - LSTTL Device Failure Modes
(SSI and MSI Devices)

Comparison of 1984 and 1980 Data

Failure Mode	Percent of Total 1984 Data (147 Devices)	Percent of Total 1980 Data (450 Devices)
OPEN	3.4	0.0
SHORT	4.1	0.4
DEGRADED	22.4	84.7
FUNCTIONAL ANOMALY	70.1	14.9

TABLE 3-6 - DTL Device Failure Modes

Comparison of 1984 and 1980 Data

Failure Mode	Percent of Total 1984 Data (64 Devices)	Percent of Total 1980 Data (59 Devices)
OPEN	0.0	0.0
SHORT	6.2	0.0
DEGRADED	18.8	20.3
FUNCTIONAL ANOMALY	75.0	77.7

4.0 Developing Pin-Level Device Models

4.1 Overview

Given the severe constraint that one does not "know" what's inside the semiconductor package, fault modelling becomes more art than science. This section, therefore, describes various approaches (employed by USC and others) which can be invoked collectively to develop a pin-level fault model. The approaches consist of device modelling based on,

(1) failure mechanisms

(2) failure mode data

(3) device stress testing

(4) functional modelling

4.2 Model Elements Based on Failure Mechanisms

4.2.1 Interconnects

Interconnect failure mechanisms consist of broken wire and detachment of die-pad and/or lead-frame wire bonds. These mechanisms can be modelled by:

1) introducing single (i.e. one-at-a-time) open-circuits at each pin.

2) introducing single short circuits across adjacent pins.

(These two failure modes are also discussed in Section 4.3)

4.2.2 Die Defects/Package Failures

As discussed in Section 3.3, die defects and package failures can lead to a virtually infinite combination of incorrect signal outputs.

With SSI devices and (to a limited extent) MSI devices, all combinations could be considered (in FMEA) and inserted (in FMET) provided that circuit complexity is low. In complex circuits employing both MSI and LSI devices, such exhaustive testing is impractical. As a result one must consider altering outputs by randomly selecting a subset of total combinations or employing a set of "worst case" combinations based upon the specific circuit design.

4.3 Model Elements Based on Failure Mode Data

4.3.1 Open Circuits

Based on the 1984 RAC data, open circuits (pin- to-pad) constitute some 3% of total failure modes (Table 3-2). (Wire bond data in Table 3-1 tends to collaborate this fraction.) Note that open-circuit failure modes are single failures.

4.3.2 Short Circuits

Short circuits would include single shorts of adjacent pins.

4.3.3 Excess Leakage and Out-of-Tolerance Parameters

Note that failure mode data applies to leakages and parameters at the pins. We are of the belief that equivalent (for FMEA) or actual (for FMET) analog interface circuitry could be interposed between device pins and socket host to effect excess leakages and out- of-tolerance voltage levels, switching characteristics and delays. (This "parasitic circuit" model has, to date, not been pursued in the study.) Failure modes here would be single and multiple. With the same considerations discussed in Section 4.2.2, fault insertion testing involving all possible combinations of leakage currents and parameter values is not practical for complex circuitry. One would accordingly have to randomly select combinations or, where possible, select "worst case" combinations based on the design at hand.

4.3.4 Functional Anomalies

The non-functional chip, improper output and latched-output failure modes can be modelled using the classical "stuck-at" approaches. Again, one faces a virtually infinite number of fault combinations for MSI and LSI devices employed in complex circuitry.

4.4 Semiconductor Device Stress Testing

4.4.1 Rationale Behind Semiconductor Stress Testing

The failure modes termed "degraded" in Table 3-2 are the result of altered transistor gains, switching thresholds, changed (diffused) resistance values and excess leakage

current. (Responsible failure mechanisms would include marginal semiconductor doping concentrations and/or die bulk and surface contamination.) As seen in Table 4-1, these circuit parameters are all temperature dependent. Consequently by operating an LSTTL device outside of its specified operating temperature limits* it is possible to induce failure of the device.

4.4.2 Experimental Setup

USC students set up a high-temperature burn-in rig with which digital integrated circuits could be operated and monitored from room temperature up to 200 degrees Celsius.

Three LSTTL device types and one TTL device type were selected** for high temperature testing:

74LS138	1-of-8-DECODER/DEMULTIPLEXER
74174	HEX D-TYPE FLIP FLOPS
74LS257	QUAD 2-TO-1 MULTIPLEXER
74LS194	4-BIT SHIFT REGISTER

Burn-in circuits for these devices are shown in Figure 4-1.

4.4.3 Stress Testing Results

All devices tested were commercial components having a maximum operating temperature*** of 70 degrees Celsius.

The following describes results of operating the devices at elevated temperatures. (Device data sheets are presented in Appendix A.)

---

*These limits define the temperature range over which the device manufacturer guarantees minimum and maximum parameter values.

**These device types were concurrently being employed in fault insertion experiments at NASA Ames Research Center.

***As noted earlier, this is the temperature beyond which the manufacturer will not guarantee minimum and maximum parameter values.

TABLE 4-1

Transistor Parameters vs. Temperature

Parameter	Units	Typical Values -55 C	25 C	70 C
Resistance (Diffused Resistor)	Ohms	320	360	450
(DC) Current Gain	dim.	65	100	200
LeakageCurrent	nA	10	70	300
Input Voltage Threshold	Volts	0.95	0.82	0.70

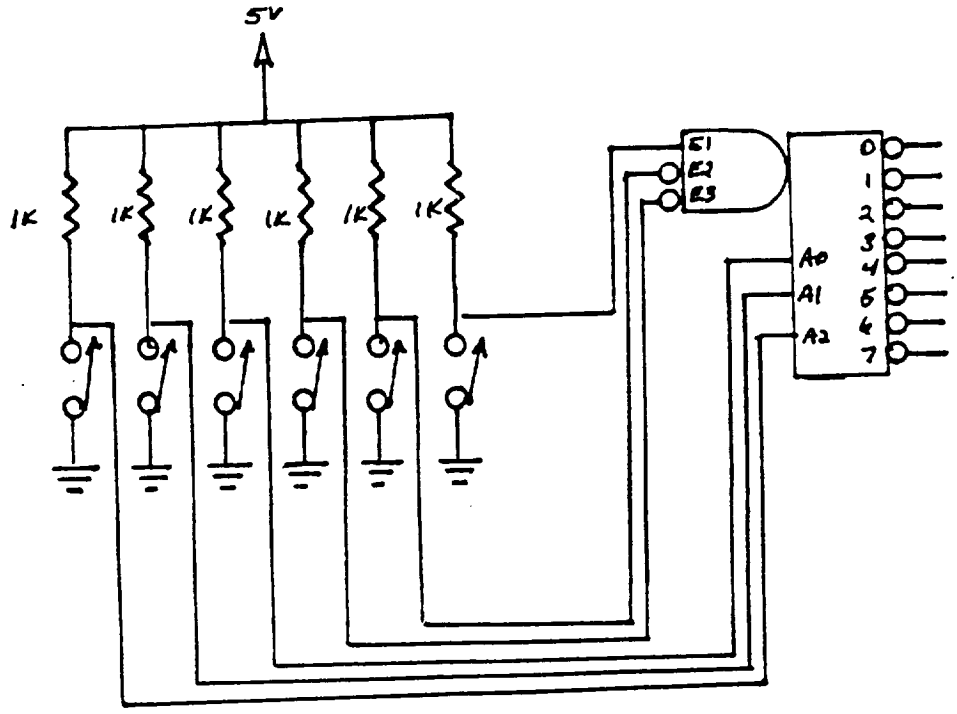

FIGURE 4-1a BURN-IN CIRCUIT FOR THE 74LS138

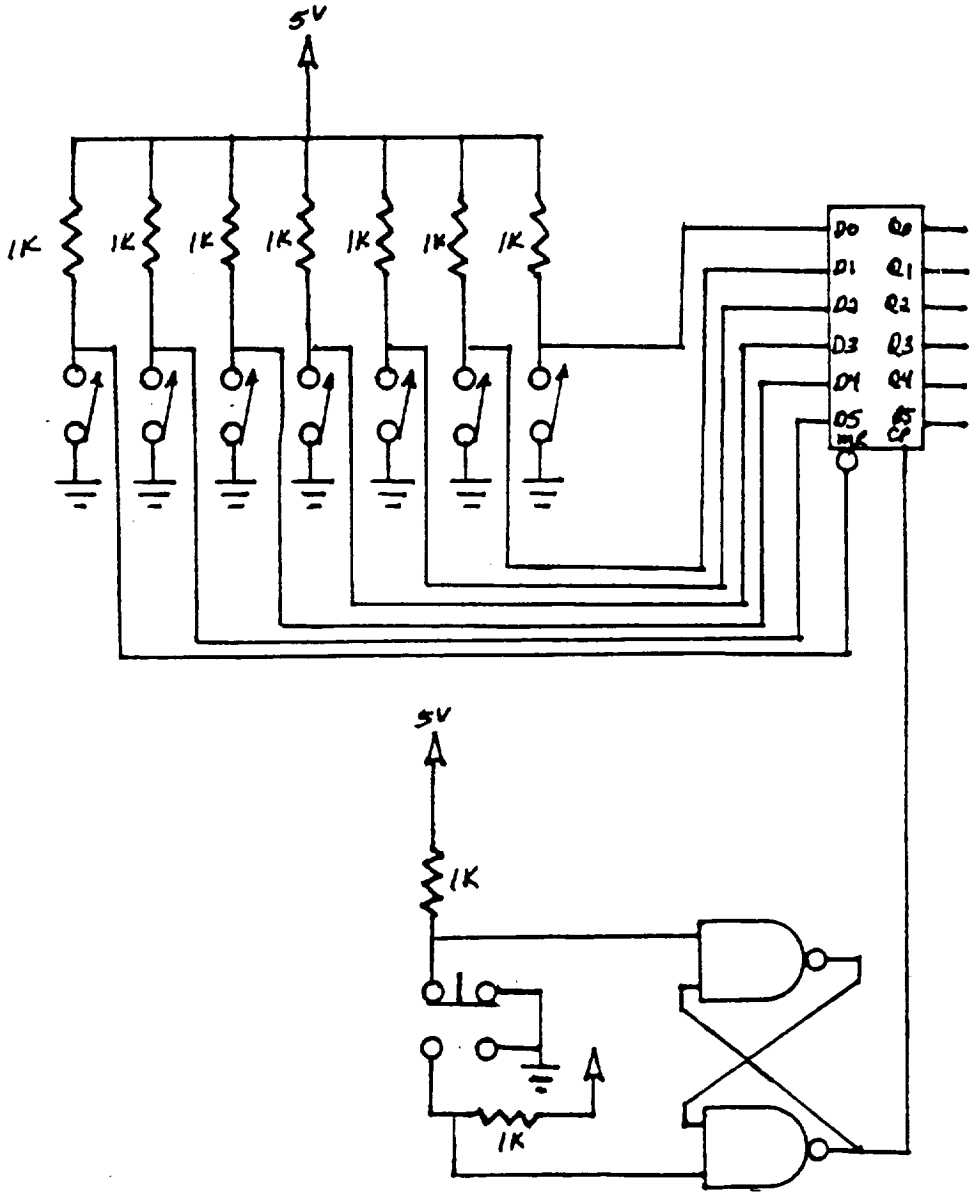

FIGURE 4-1b BURN-IN CIRCUIT FOR THE 74174

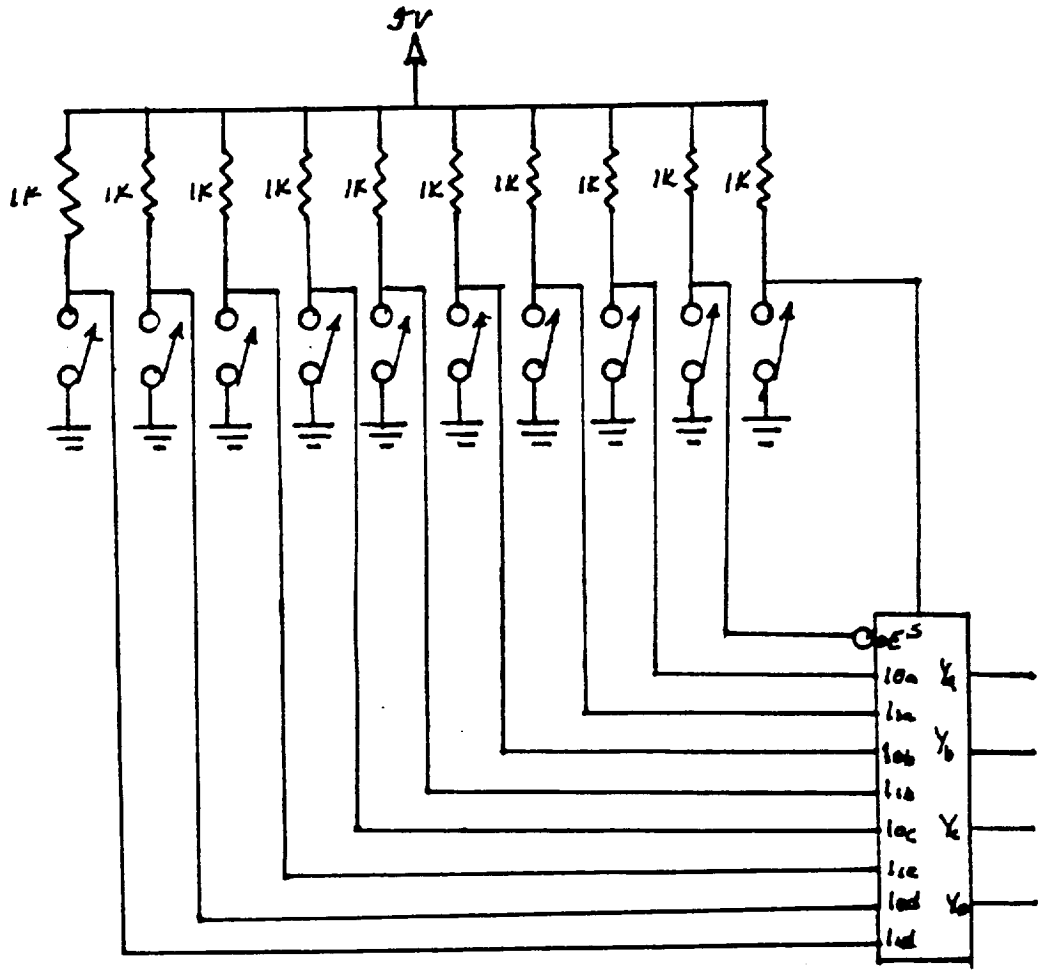

FIGURE 4-1c BURN-IN CIRCUIT FOR THE 74LS257

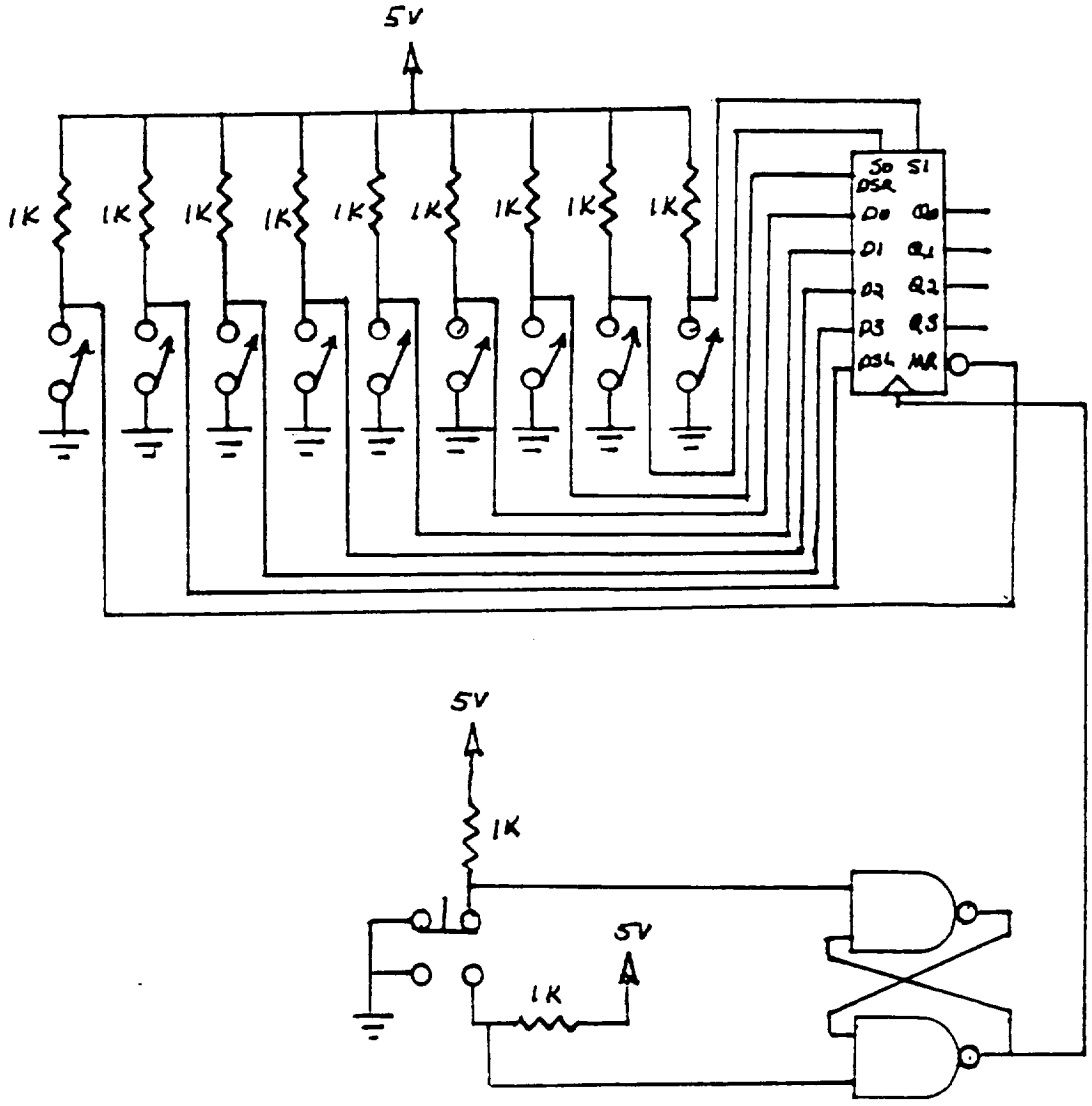

FIGURE 4-1d BURN-IN CIRCUIT FOR THE 74LS194

When testing the 74LS138, five different devices were tested under high temperature tests and the following results were obtained: In the first test, all of the outputs stuck high from 170 to 200 degrees Celsius. In the second test, all of the outputs stuck high from 170 to 200 degrees Celsius. For the other three tests, the circuits performed exactly as they were supposed to for temperatures from 20 to 200 degrees Celsius.

When testing the 74174, five different devices were tested and the following results were obtained: In the first test, output Q3 stuck low from 180 to 200 degrees Celsius. In the second test, the clock and output Q5 shorted together from 180 to 200 degrees Celsius. In the third test, output Q4 stuck high from 160 to 200 degrees Celsius. In the fourth test, all outputs stuck low from 100 to 200 degrees Celsius. In the fifth test, all outputs stuck low from 120 to 200 degrees Celsius.

When testing the 74LS257, five different devices were tested under high temperature tests and no change in the outputs was found from 20 to 200 degrees Celsius.

When testing the 74LS194, five different devices were tested under high temperature conditions and the following results were obtained: In the first test, outputs Q0, Q1, and Q2 were stuck high in the hold mode at 190 degrees Celsius. In the second test, all of the outputs stuck high at 200 degrees Celsius. In the third test, all of the outputs stuck high at 80 degrees Celsius. In the fourth test, all outputs were stuck high in the shift left mode at 200 degrees Celsius. In the fifth test, outputs Q1 and Q3 were stuck high in the parallel load mode from 80 to 200 degrees Celsius.

The foregoing test results are summarized in Table 4-2.

Appendix B shows the truth tables for each of the failed devices made at the time the device was failed. Note that all of the faults induced were permanent faults. (No attempt was made in the experiments to induce intermittent faults.)

TABLE 4-2

Semiconductor Device Stress Testing Results

DEVICE TYPE	DEVICE NO.	RESULTS
74LS138	1, 2	ALL OUTPUTS STUCKHIGH
	3, 4, 5	NO FAILURES
74174	1	Q3 STUCK LOW
	2	CLOCK AND Q5 SHORTED
	3	Q4 STUCK HIGH
	4, 5	ALL OUTPUTS STUCK LOW
74LS257	1, 2, 3, 4, 5	NO FAILURES
74LS194	1	Q0, Q1, Q2 STUCK HIGH
	2	ALL OUTPUTS STUCK HIGH
	3	ALL OUTPUTS STUCK HIGH
	4	ALL OUTPUTS STUCK HIGH (IN LEFT SHIFT MODE)
	5	Q1 AND Q3 STUCK HIGH (IN PARALLEL LOAD MODE)

4.5 Functional Fault Modelling

Given that gates in an LSI device are inaccessable (i.e. analytically in FMEA; physically in FMET), many workers have opted to employ functional models in performing fault free and fault insertion simulations (e.g. see References 6, 7 & 8). Functional fault modelling, quite simply, consists of altering pin states (in simulation during FMEA; or in real time during FMET) such that the function of the (individual or sets of) pins is defeated. Table 4-3 shows functional faults for a select number* of LSTTL devices along with the corresponding alteration of pin states. Note that some of the fault insertions in the table require that pin states be changed instantaneously. (For example, the insertion "invert state" in Table 4-3a requires that the corresponding pin state must be monitored and changed.) While "instantaneous" changes are feasible in simulation, they may be impossible to achieve in physical fault insertion
particularly where victim circuit speeds equal or exceed that of the insertion circuitry. Finally, it is noted that the fault insertions of Table 4-3 can occur as single or multiple faults and as well as being permanent or intermittent in duration.

4.6 Summary

As noted in the introduction to this section, a fault model for an LSTTL device would incorporate all of the approaches described above. These are summarized in Table 4-4 which also shows corresponding failure modes.

5.0 Conclusions and Indicated Research Directions

As a result of our investigations, we find that semiconductor failure mechanism data is abundant but of little use in developing pin level device models. Failure mode data on the other hand does exist but is too sparse to be of any (statistical) use in developing fault models.

What is significant in the failure mode data is that, unlike classical logic, MSI and LSI devices do exhibit more than "stuckat" and open/short failure modes. Specifically they are dominated by parametric failures and functional anomalies that can include intermittent faults and multiple pin failures.

*These device types were concurrently being employed in fault insertion experiments at NASA Ames Research Center.

TABLE 4-3a FUNCTIONAL FAULT MODELLING

2901 MICROPROCESSOR SLICE

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Register select failure (A port)	4 (A0)	invert state
"	3 (A1)	"
"	2 (A2)	"
"	1 (A3)	"
Register select failure (B port)	17 (B0)	"
"	18 (B1)	"
"	19 (B2)	"
"	20 (B3)	"
Microinstruction decode fail	12 (I0)	"
"	13 (I1)	"
"	14 (I2)	"
"	26 (I3)	"
"	28 (I4)	"
"	27 (I5)	"
"	5 (I6)	"
"	7 (I7)	"
"	6 (I8)	"
Correct data shift fail (Q req.)	8	open
"	9	"

TABLE 4-3a FUNCTIONAL FAULT MODELLING

2901 MICROPROCESSOR SLICE

(CONTINUED)

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Correct (Y) output fail state	36	invert
"	37	"
"	38	"
"	39	"
Output disable*	40	S-a-1
Carry generate/prop fail state	32	invert
"	35	"
Overflow (false) fail	34	S-a-1
ALU zero (false) fail	11	S-a-1
ALU MSB out fail state	31	invert
Carry-in fail	29	S-a-1
Clock fail	15	S-a-1
"	15	S-a-0

*Tied low on all 2901 chips.

TABLE 4-3b Functional Fault Modelling

2911 Microprogram Sequencer

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Address source select fail state	10	invert
"	11	"
Push/pop stock oper. fail	19	"
"	20	"
Internal reg. select fail	3	S-a-1
Zero enable fail	9 (zero)	S-a-1
Zero disable fail	9	S-a-0
Y-enable fail	16	S-a-1
Y-disable fail	16	S-a-0
Incrementer carry-in fail	17	S-a-0
"	6	invert state

TABLE 4-3c Functional Fault Modelling

2918 Quad D Register

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Y enable fail	7 (OE)	S-a-1
Y disable fail	7 (OE)	S-a-0
Clock fail	9 (CP)	S-a-0
Correct Q output fail	2 (Q0)	invert state
"	5 (Q1)	"
"	11 (Q2)	"
"	14 (Q3)	"
CorrectY output fail	3 (Y0)	invert state (when pin 7 = 0)
"	6 (Y1)	"
"	10 (Y2)	"
"	13 (Y3)	"

TABLE 4-3d Functional Fault Modelling

54LS253 Dual 4-Input Multiplexer

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Chip enable fail	1 (Mux 1 enable)	S-a-1
"	15 (Mux 2 enable)	"
Chip disable fail	1	S-a-0
"	15	"
Channel select fail state	14 (select 0)	invert
"	2 (select 1)	"
Correctoutput fail	7 (Mux 1 out)	invert when pin 1 = 0
"	9 (Mux 2 out)	invert when pin 15 = 0

TABLE 4-3e Functional Fault Modelling

54LS02 - Quad NOR

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Fails to perform NOR state	1 (A output)	Invert
"	4 (B output)	"
"	10 (C output)	"
"	13 (D output)	"

TABLE 4-3f Functional Fault Modelling

54LS00 - Quad NAND

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Fails to perform NAND state	3 (A output)	Invert
"	6 (B output)	"
"	8 (C output)	"
"	11 (D output)	"

TABLE 4-3g Functional Fault Modelling

5404 Hex Inverter

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Fails to invert state	1 (A input)	Invert
"	3 (B input)	"
"	5 (C input)	"
"	9 (D input)	"
"	11 (E input)	"
"	13 (F input)	"

TABLE 4-3e Functional Fault Modelling

54LS02 - Quad NOR

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Fails to perform NOR state	1 (A output)	Invert
"	4 (B output)	"
"	10 (C output)	"
"	13 (D output)	"

TABLE 4-3f Functional Fault Modelling

54LS00 - Quad NAND

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Fails to perform NAND state	3 (A output)	Invert
"	6 (B output)	"
"	8 (C output)	"
"	11 (D output)	"

TABLE 4-3g Functional Fault Modelling

5404 Hex Inverter

FUNCTIONAL FAULT INSERTION	PIN	FAULT
Fails to invert state	1 (A input)	Invert
"	3 (B input)	"
"	5 (C input)	"
"	9 (D input)	"
"	11 (E input)	"
"	13 (F input)	"

TABLE 4-4 - LSTTL Failure Modes and Fault Models

Failure Mode	Fault Model
Functional Anomaly	Functional Fault Model (FMEA); Model Generated Fault Patterns (FMET)
Degraded (At Pins)	Parasitic Circuit
Degraded (On Chip)	Device Stress Tests to Corroborate Functional Fault Model
Opens	Open-Circuit Pin
Shorts	Short-Circuit Adjacent Pins

It is certainly possible, and this report discusses the methods, to develop pin-level models based on extrapolation of semiconductor device failure mechanisms, failure modes, results of (temperature) stress testing and functional modelling. Such a composite model would include credible faults that could be experienced by the device. Unfortunately, the number of such faults would be insignificant when compared to the (virtually infinite) number of possible fault patterns. At issue here is the fact that one could insert all the faults in a composite model and yet gain no accurate measure of fault detection coverage and/or fault latency times. I.e. one could demonstrate fault tolerance yet come away with no measures of the degree of fault tolerance.

The foregoing prompt several research questions:

1) Although single-pin "stuck-at" or open/short permanent fault insertions do not characterize the modern MSI and LSI device, can they be legitimately* employed to cover actual failure modes that might be experienced?

2) Is it possible to obtain a definition of coverage and coverage measures with a device which can exhibit permanent or intermittent failures at one or more device pins?

3) Is one better off considering failure patterns at electrical connection boundaries other than integrated circuit pins (e.g. data busses, I/O lines, etc.)?

*The approach is extensively used today with FMEA.

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Acknowledgements

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APPENDIX A

DEVICE DATA SHEETS

MOTOROLA

SN54LS138
SN74LS138

1-OF-8-DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL MSI SN54LS 74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

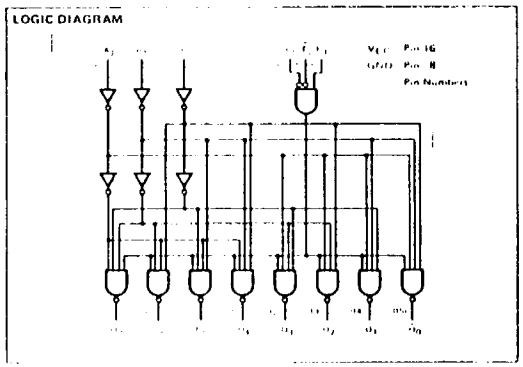
- DEMULTIPLEXING CAPABILITY
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION
- TYPICAL POWER DISSIPATION OF 32 mW
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES

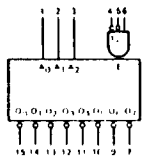
		LOADING (Note a) HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1, \overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH, 1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

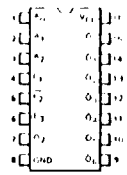


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

NOTE
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

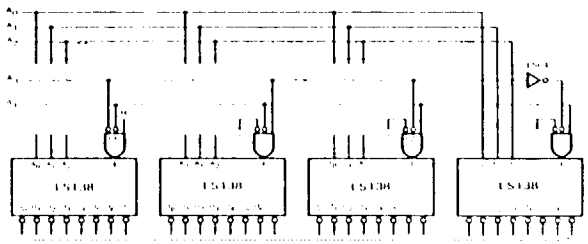


Fig. a

54LS138 1-of-8 Decoder

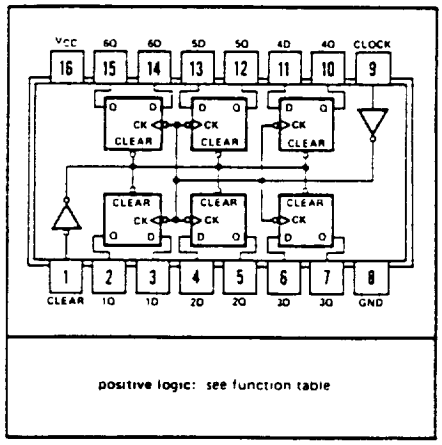
TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

BULLETIN NO. DL-S 7511803, DECEMBER 1972—REVISED OCTOBER 1976

'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

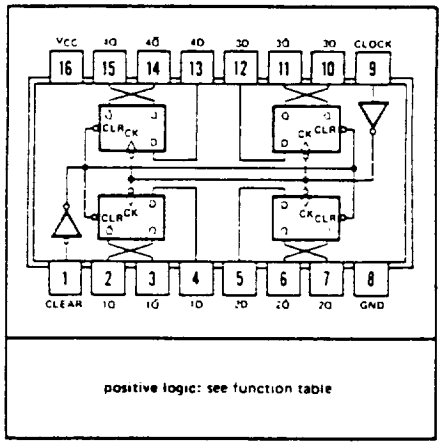
- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174, SN74LS174, SN74S174 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175, SN74LS175, SN74S175 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flops.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

54LS174 Hex D-Type Flip Flops

MOTOROLA

SN54LS/74LS257A
SN54LS/74LS258A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

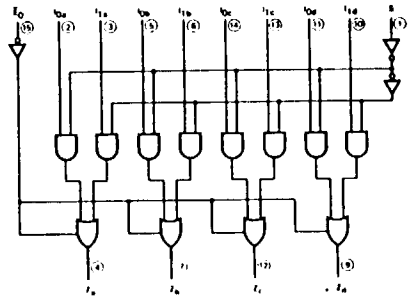
LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS257A and the SN54LS/74LS258A are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

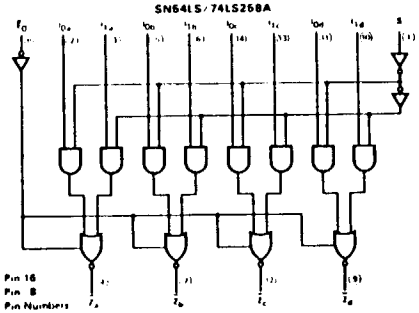
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

LOGIC DIAGRAMS

SN54LS/74LS257A



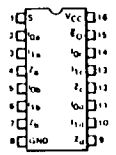
SN54LS/74LS258A



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

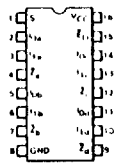
CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS257A



V_{CC} = Pin 16
GND = Pin 8

SN54LS/74LS258A



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

NOTE
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS257A and LS258A are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257A and in the inverted form for the LS258A.

The LS257A and LS258A are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

LS257A
$$Z_a = \overline{E}_O \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = \overline{E}_O \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E}_O \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = \overline{E}_O \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

LS258A
$$\overline{Z}_a = \overline{E}_O \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad \overline{Z}_b = \overline{E}_O \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{E}_O \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad \overline{Z}_d = \overline{E}_O \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257A	OUTPUTS LS258A
$\overline{E}_O$	S	I_0	I_1	Z	$\overline{Z}$
H	X	X	X	(Z)	(Z)
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (off)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54			-1.0	mA
		74			-2.6	
I_{OL}	Output Current — Low	54			12	mA
		74			24	

54LS257 Quad 2-Input Multiplexer

MOTOROLA

SN54LS194A
SN74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS194A is a High Speed 4 Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL families.

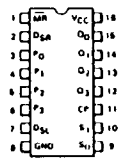
- TYPICAL SHIFT FREQUENCY OF 36 MHz
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0, S_1	Mode Control Inputs	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
D_{SR}	Serial (Shift Right) Data Input	0.5 U.L.	0.25 U.L.
D_{SL}	Serial (Shift Left) Data Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

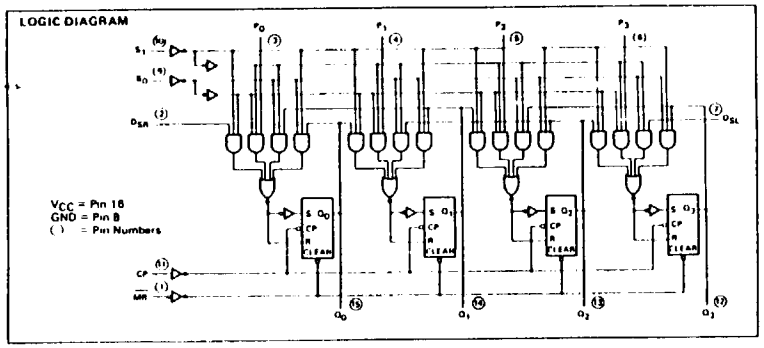
NOTES
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4 Bit Bidirectional Shift Register. The LS194A is similar in operation to the Motorola LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

1. All data and mode control inputs are edge triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set up time prior to the positive transition of the clock pulse.
2. The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.
3. The four parallel data inputs (P_0, P_1, P_2, P_3) are D type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2, and P_3 inputs is transferred to the Q_0, Q_1, Q_2, and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.
4. The asynchronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

1. Two mode control inputs (S_0, S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.
2. D type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS $\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	OUTPUTS Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set up time prior to the LOW to HIGH clock transition.

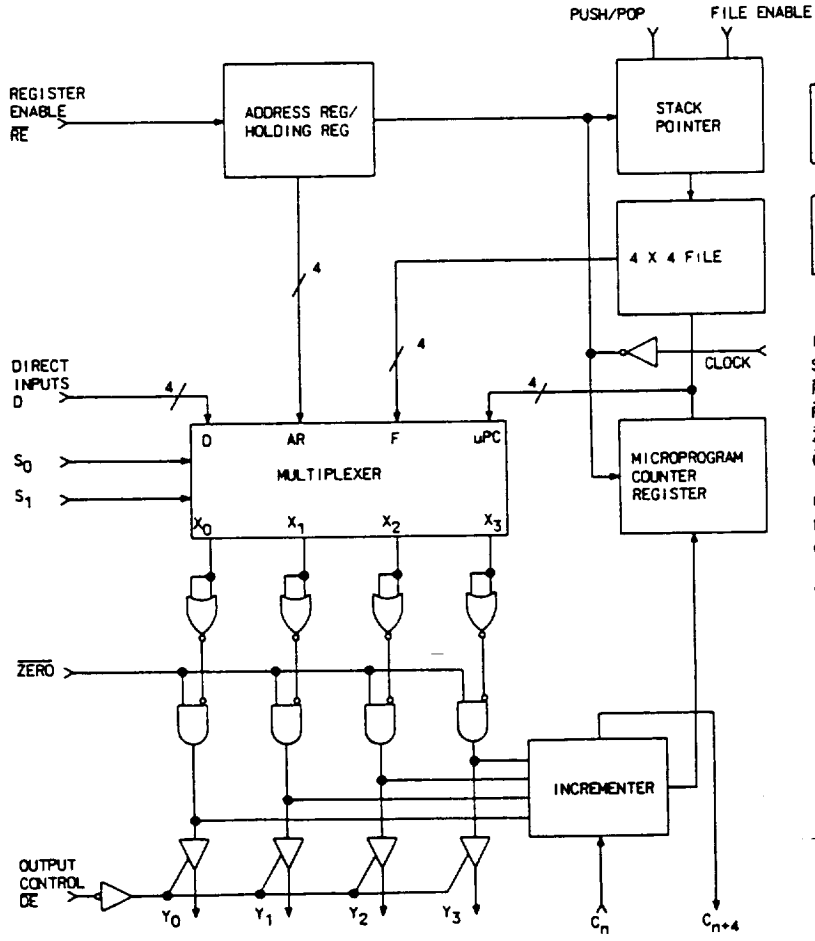
54LS194 4-Bit Bidirectional Universal Shift Register

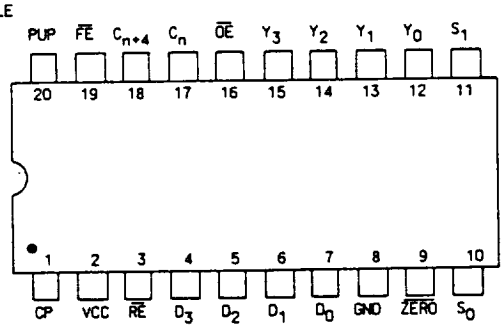
GENERAL DESCRIPTION

THE 2911 IS A FOUT-BIT WIDE ADDRESS CONTROLLER INTENDED FOR SEQUENCING THROUGH A SERIES OF MICROINSTRUCTIONS CONTAINED IN A ROM OR PROM. TWO 2911'S MAY BE INTERCONNECTED TO GENERATE AN EIGHT-BIT ADDRESS (256 WORDS), AND THREE MAY BE USED TO GENERATE A TWELVE-BIT ADDRESS (4K WORDS).

THE 2911 CAN SELECT AN ADDRESS FROM ANY OF THREE SOURCES. THEY ARE: 1) A SET OF EXTERNAL DIRECT INPUTS (D); 2) A FOUR-WORD DEEP PUSH/POP STACK; OR 3) A PROGRAM COUNTER REGISTER (WHICH USUALLY CONTAINS THE LAST ADDRESS PLUS ONE). THE PUSH/POP STACK INCLUDES CERTAIN CONTROL LINES SO THAT IT CAN EFFICIENTLY EXECUTE NESTED SUBROUTINE LINKAGES. A SEPARATE LINE FORCES THE OUTPUTS TO ALL ZEROES. THE OUTPUTS ARE THREE-STATE.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM





INPUTS TO 2911

S_1, S_0	CONTROL LINES FOR ADDRESS SOURCE SELECTION
$\overline{FE}$, PUP	CONTROL LINES FOR PUSH/POP STACK
$\overline{RE}$	ENABLE LINE FOR INTERNAL ADDRESS REGISTER
$\overline{ZERO}$	LOGIC AND INPUT ON THE OUTPUT LINES
$\overline{OE}$	OUTPUT ENABLE. WHEN $\overline{OE}$ IS HIGH, THE Y OUTPUTS ARE OFF (HIGH IMPEDANCE)
C_n	CARRY-IN TO THE INCREMENTER
D_i	DIRECT INPUTS TO THE MULTIPLEXER
CP	CLOCK INPUT TO THE AR AND uPC REGISTER AND PUSH-POP STACK.

OUTPUTS FROM THE 2911

Y_i	ADDRESS OUTPUTS FROM 2911. (ADDRESS INPUTS TO CONTROL MEMORY.)
C_{n+4}	CARRY OUT FROM THE INCREMENTER

EXTERNAL TO THE 2911

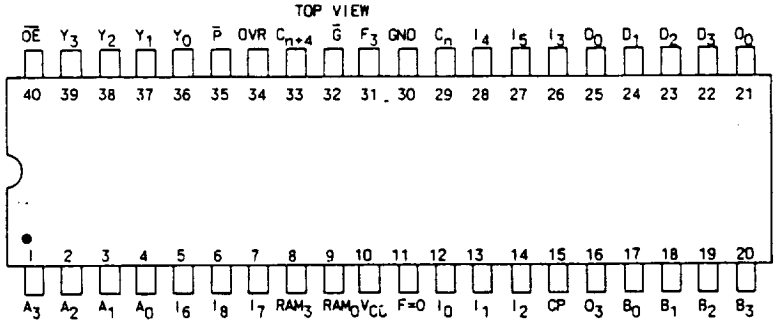
A	ADDRESS TO THE CONTROL MEMORY
I(A)	INSTRUCTION IN CONTROL MEMORY AT ADDRESS A
uWR	CONTENTS OF A MICROWORD REGISTER (AT OUTPUT OF CONTROL MEMORY). THE MICROWORD REGISTER CONTAINS THE INSTRUCTION CURRENTLY BEING EXECUTED.
T_n	TIME PERIOD (CYCLE) n

TP6-5385-014

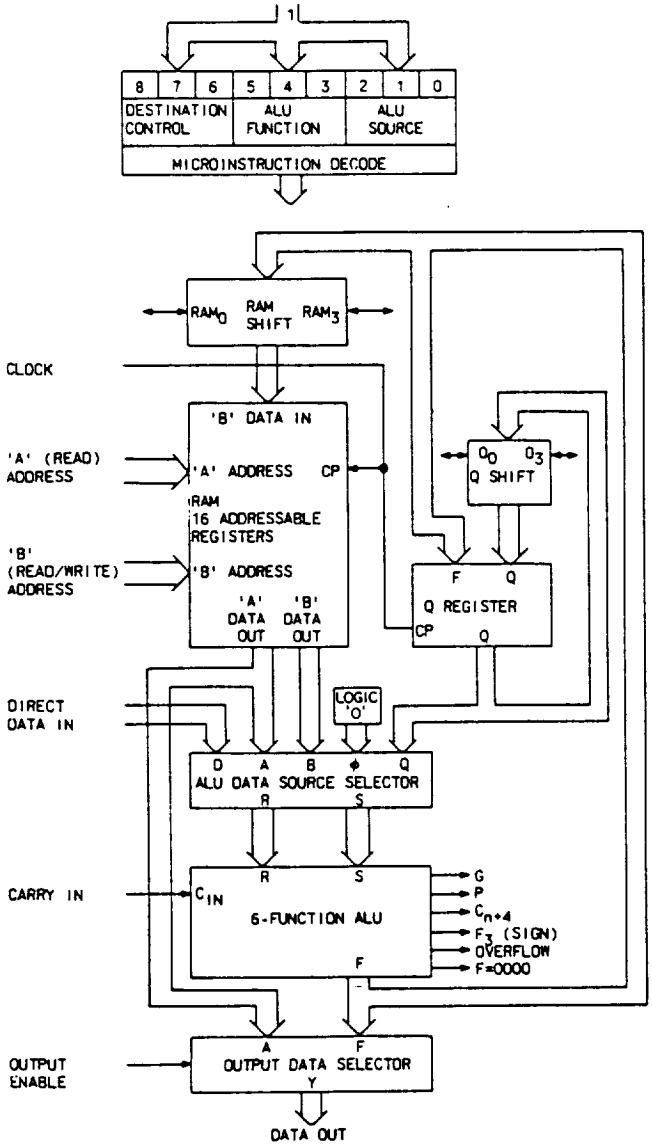
GENERAL DESCRIPTION

THE FOUR-BIT BIPOLAR MICROPROCESSOR SLICE IS DESIGNED AS A HIGH SPEED CASCADABLE ELEMENT INTENDED FOR USE IN CPU'S, PERIPHERAL CONTROLLERS, PROGRAMMABLE MICROPROCESSORS AND NUMEROUS OTHER APPLICATIONS. THE MICROINSTRUCTION FLEXIBILITY OF THE 2901A WILL ALLOW EFFICIENT EMULATION OF ALMOST ANY DIGITAL COMPUTING MACHINE. THE DEVICE, AS SHOWN IN THE BLOCK DIAGRAM BELOW, CONSISTS OF A16-WORD BY 4-BIT TWO-PORT RAM, A HIGH-SPEED ALU, AND THE ASSOCIATED SHIFTING, DECODING AND MULTIPLEXING CIRCUITRY. THE NINE-BIT MICROINSTRUCTION WORD IS ORGANIZED INTO THREE GROUPS OF THREE BITS EACH AND SELECTS THE ALU SOURCE OPERANDS, THE ALU FUNCTION, AND THE ALU DESTINATION REGISTER. THE MICROPROCESSOR IS CASCADABLE WITH FULL LOOK-AHEAD OR WITH RIPPLE CARRY, HAS THREE-STATE OUTPUTS, AND PROVIDES VARIOUS STATUS FLAG OUTPUTS FROM THE ALU

CONNECTION DIAGRAM
TOP VIEW



MICROPROCESSOR SLICE BLOCK DIAGRAM



PIN DEFINITIONS

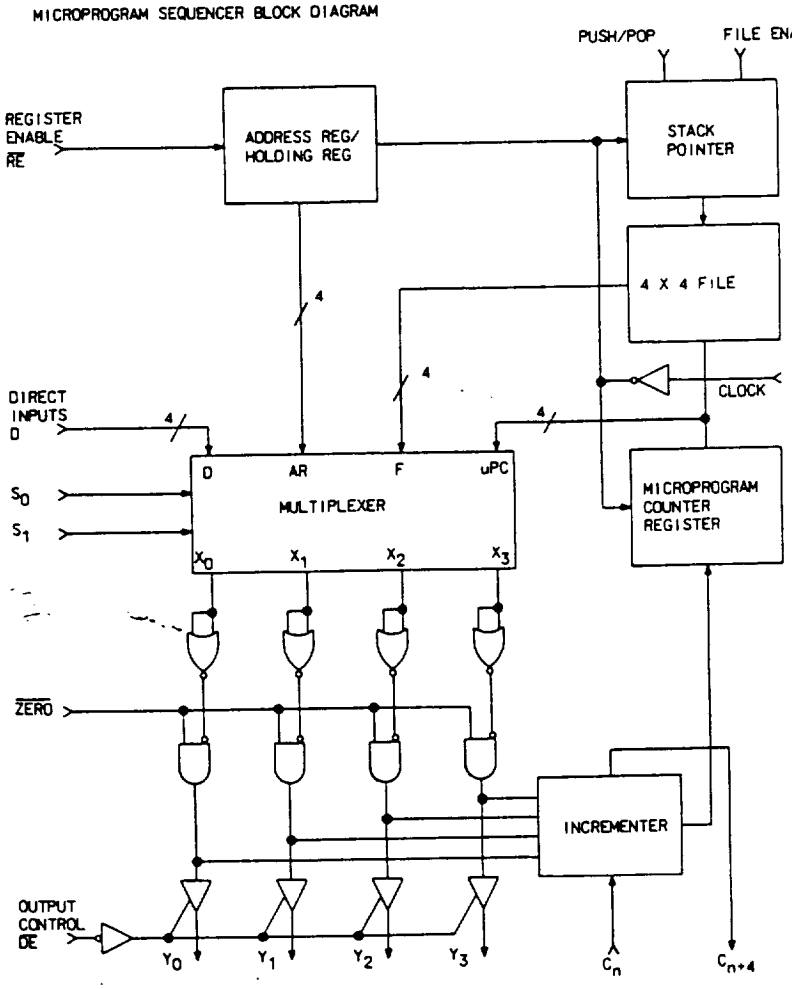
A_{0-3}	THE FOUR ADDRESS INPUTS TO THE REGISTER STACK USED TO SELECT ONE REGISTER WHOSE CONTENTS ARE DISPLAYED THROUGH THE A-PORT.
B_{0-3}	THE FOUR ADDRESS INPUTS TO THE REGISTER STACK USED TO SELECT ONE REGISTER WHOSE CONTENTS ARE DISPLAYED THROUGH THE B-PORT AND INTO WHICH NEW DATA CAN BE WRITTEN WHEN THE CLOCK GOES LOW.
I_{0-8}	THE NINE INSTRUCTION CONTROL LINES TO THE 2901A. USED TO DETERMINE WHAT DATA SOURCES WILL BE APPLIED TO THE ALU (I_{012}), WHAT FUNCTION THE ALU WILL PERFORM (I_{345}), AND WHAT DATA IS TO BE DEPOSITED IN THE Q-REGISTER OR THE REGISTER STACK (I_{678})
Q_3 RAM_3	A SHIFT LINE AT THE MSB OF THE Q REGISTER (Q_3) AND THE REGISTER STACK (RAM_3). ELECTRICALLY THESE LINES ARE THREE-STATE OUTPUTS CONNECTED TO TTL INPUTS INTERNAL TO THE 2901A. WHEN THE DESTINATION CODE ON I_{678} INDICATES AN UP SHIFT (OCTAL 6 OR 7) THE THREE-STATE OUTPUTS ARE ENABLED AND THE MSB OF THE Q REGISTER IS AVAILABLE ON THE Q_3 PIN AND THE MSB OF THE ALU OUTPUT IS AVAILABLE ON THE RAM_3 PIN. OTHERWISE, THE THREE-STATE OUTPUTS ARE OFF (HIGH-IMPEDANCE) AND THE PINS ARE ELECTRICALLY LS-TTL INPUTS. WHEN THE DESTINATION CODE CALLS FOR A DOWN SHIFT THE PINS ARE USED AS THE DATA INPUTS TO THE MSB OF THE Q REGISTER (OCTAL 4) AND RAM (OCTAL 4 OR 5).
Q_0 RAM_0	SHIFT LINES LIKE Q_3 AND RAM_3, BUT AT THE LSB OF THE Q-REGISTER AND RAM. THESE PINS ARE TIED TO THE Q_3 AND RAM_3 PINS OF THE ADJACENT DEVICE TO TRANSFER DATA BETWEEN DEVICES FOR UP AND DOWN SHIFTS OF THE Q REGISTER AND ALU DATA.
D_{0-3}	DIRECT DATA INPUTS. A FOUR-BIT FIELD WHICH MAY BE SELECTED AS ONE OF THE ALU DATA SOURCES FOR ENTERING DATA INTO THE 2901A. D_0 IS THE LSB.
Y_{0-3}	THE FOUR DATA OUTPUTS OF THE 2901A. THESE ARE THREE-STATE OUTPUT LINES. WHEN ENABLED, THEY DISPLAY EITHER THE FOUR OUTPUTS OF THE ALU OR THE DATA ON THE A-PORT OF THE REGISTER STACK, AS DETERMINED BY THE DESTINATION CODE I_{678}.
$\overline{OE}$	OUTPUT ENABLE. WHEN $\overline{OE}$ IS HIGH, THE Y OUTPUTS ARE OFF; WHEN $\overline{OE}$ IS LOW, THE Y OUTPUTS ARE ACTIVE (HIGH OR LOW).
$\overline{P}, \overline{G}$	THE CARRY GENERATE AND PROPAGATE OUTPUTS OF THE 2901A'S ALU. THESE SIGNALS ARE USED WITH THE 2902 FOR CARRY-LOOKAHEAD.
OVR	OVERFLOW. THIS PIN IS LOGICALLY THE EXCLUSIVE-OR OF THE CARRY-IN AND CARRY-OUT OF THE MSB OF THE ALU. AT THE MOST SIGNIFICANT END OF THE WORD, THIS PIN INDICATES THAT THE RESULT OF AN ARITHMETIC TWO'S COMPLEMENT OPERATION HAS OVERFLOWED INTO THE SIGN-BIT.
F=0	THIS IS AN OPEN COLLECTOR OUTPUT WHICH GOES HIGH (OFF) IF THE DATA ON THE FOUR ALU OUTPUTS F_{0-3} ARE ALL LOW. IN POSITIVE LOGIC, IT INDICATES THE RESULT OF AN ALU OPERATION IS ZERO.
F_3	THE MOST SIGNIFICANT ALU OUTPUT BIT.
C_n	THE CARRY-IN TO THE 2901A'S ALU.
C_{n+4}	THE CARRY-OUT OF THE 2901A'S ALU
CP	THE CLOCK TO THE 2901A. THE Q REGISTER AND REGISTER STACK OUTPUTS CHANGE ON THE CLOCK LOW-TO-HIGH TRANSITION. THE CLOCK LOW TIME IS INTERNALLY THE WRITE ENABLE TO THE 16 x 4 RAM WHICH COMPROMISES THE "MASTER" LATCHES OF THE REGISTER STACK. WHILE THE CLOCK IS LOW, THE "SLAVE" LATCHES ON THE RAM OUTPUTS ARE CLOSED, STORING THE DATA PREVIOUSLY ON THE RAM OUTPUTS. THIS ALLOWS SYNCHRONOUS MASTER-SLAVE OPERATION OF THE REGISTER STACK.

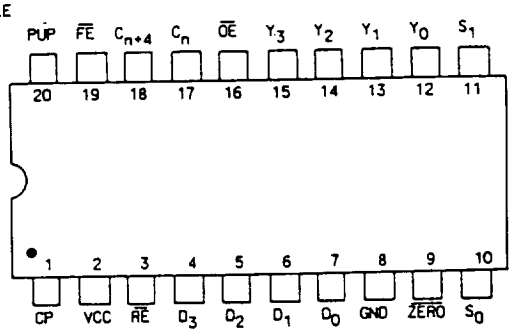
GENERAL DESCRIPTION

THE 2911 IS A FOUT-BIT WIDE ADDRESS CONTROLLER INTENDED FOR SEQUENCING THROUGH A SERIES OF MICROINSTRUCTIONS CONTAINED IN A ROM OR PROM. TWO 2911'S MAY BE INTERCONNECTED TO GENERATE AN EIGHT-BIT ADDRESS (256 WORDS), AND THREE MAY BE USED TO GENERATE A TWELVE-BIT ADDRESS (4K WORDS).

THE 2911 CAN SELECT AN ADDRESS FROM ANY OF THREE SOURCES. THEY ARE: 1) A SET OF EXTERNAL DIRECT INPUTS (D); 2) A FOUR-WORD DEEP PUSH/POP STACK; OR 3) A PROGRAM COUNTER REGISTER (WHICH USUALLY CONTAINS THE LAST ADDRESS PLUS ONE). THE PUSH/POP STACK INCLUDES CERTAIN CONTROL LINES SO THAT IT CAN EFFICIENTLY EXECUTE NESTED SUBROUTINE LINKAGES. A SEPARATE LINE FORCES THE OUTPUTS TO ALL ZEROES. THE OUTPUTS ARE THREE-STATE.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM





INPUTS TO 2911

S_1, S_0	CONTROL LINES FOR ADDRESS SOURCE SELECTION
$\overline{FE}$, PUP	CONTROL LINES FOR PUSH/POP STACK
$\overline{RE}$	ENABLE LINE FOR INTERNAL ADDRESS REGISTER
$\overline{ZERO}$	LOGIC AND INPUT ON THE OUTPUT LINES
$\overline{OE}$	OUTPUT ENABLE. WHEN $\overline{OE}$ IS HIGH, THE Y OUTPUTS ARE OFF (HIGH IMPEDANCE)
C_n	CARRY-IN TO THE INCREMENTER
D_i	DIRECT INPUTS TO THE MULTIPLEXER
CP	CLOCK INPUT TO THE AR AND uPC REGISTER AND PUSH-POP STACK.

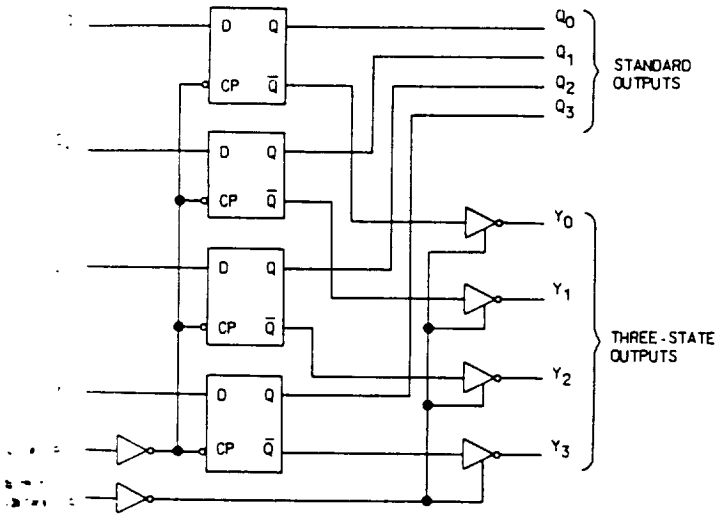
OUTPUTS FROM THE 2911

Y_i	ADDRESS OUTPUTS FROM 2911. (ADDRESS INPUTS TO CONTROL MEMORY.)
C_{n+4}	CARRY OUT FROM THE INCREMENTER

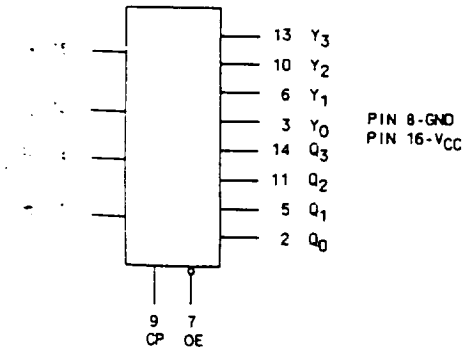
EXTERNAL TO THE 2911

A	ADDRESS TO THE CONTROL MEMORY
I(A)	INSTRUCTION IN CONTROL MEMORY AT ADDRESS A
uWR	CONTENTS OF A MICROWORD REGISTER (AT OUTPUT OF CONTROL MEMORY). THE MICROWORD REGISTER CONTAINS THE INSTRUCTION CURRENTLY BEING EXECUTED.
T_n	TIME PERIOD (CYCLE) n

LOGIC DIAGRAM



LOGIC SYMBOL



PIN 8-GND
PIN 16-V_{CC}

DESCRIPTION

THE 2918 CONSISTS OF FOUR D-TYPE FLIP-FLOPS WITH A BUFFERED COMMON CLOCK. INFORMATION MEETING THE SET-UP AND HOLD REQUIREMENTS ON THE D INPUTS IS TRANSFERRED TO THE Q OUTPUTS ON THE LOW-TO-HIGH TRANSITION OF THE CLOCK.

THE SAME DATA AS ON THE Q OUTPUTS IS ENABLED AT THE THREE-STATE Y OUTPUTS WHEN THE "OUTPUT CONTROL" (OE) INPUT IS LOW. WHEN THE OE INPUT IS HIGH, THE Y OUTPUTS ARE IN THE HIGH-IMPEDANCE STATE.

THE 2918 IS A 4-BIT, HIGH-SPEED REGISTER INTENDED FOR USE IN REAL-TIME SIGNAL PROCESSING SYSTEMS WHERE THE STANDARD OUTPUTS ARE USED IN A RECURSIVE ALGORITHM AND THE THREE-STATE OUTPUTS PROVIDE ACCESS TO A DATA BUS TO DUMP THE RESULTS AFTER A NUMBER OF ITERATIONS.

THE DEVICE CAN ALSO BE USED AS AN ADDRESS REGISTER OR STATUS REGISTER IN COMPUTERS OR COMPUTER PERIPHERALS.

THE 2918 IS ALSO USEFUL IN CERTAIN DISPLAY APPLICATIONS WHERE THE STANDARD OUTPUTS CAN BE DECODED TO DRIVE LED'S (OR EQUIVALENT) AND THE THREE-STATE OUTPUTS ARE BUS ORGANIZED FOR OCCASIONAL INTERROGATION OF THE DATA AS DISPLAYED.

DEFINITION OF FUNCTIONAL TERMS

D_i THE FOUR DATA INPUTS TO THE REGISTER.

Q_i THE FOUR DATA OUTPUTS OF THE REGISTER WITH STANDARD TOTEM-POLE ACTIVE PULL-UP OUTPUTS. DATA IS PASSED NON-INVERTED.

Y_i THE FOUR THREE-STATE DATA OUTPUTS OF THE REGISTER. WHEN THE THREE-STATE OUTPUTS ARE ENABLED, DATA IS PASSED NON-INVERTED. A HIGH ON THE "OUTPUT CONTROL" INPUT FORCES THE Y_i OUTPUTS TO THE HIGH-IMPEDANCE STATE.

CP CLOCK. THE BUFFERED COMMON CLOCK FOR THE REGISTER ENTERS DATA ON THE LOW-TO-HIGH TRANSITION.

$\overline{OE}$ OUTPUT CONTROL. WHEN THE OE INPUT IS HIGH, THE Y_i OUTPUTS ARE IN THE HIGH-IMPEDANCE STATE. WHEN THE OE INPUT IS LOW, THE TRUE REGISTER DATA IS PRESENT AT THE Y_i OUTPUTS.

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	-
H	H	X	NC	Z	-
H	↑	L	L	Z	-
H	↑	H	H	Z	-
L	↑	L	L	L	-
L	↑	H	H	H	-
L	~	-	L	L	1
L	-	-	H	H	1

L = LOW
H = HIGH
X = DON'T CARE
NC = NO CHANGE
↑ = LOW TO HIGH TRANSITION
Z = HIGH IMPEDANCE

NOTE:

1. WHEN $\overline{OE}$ IS LOW, THE Y OUTPUT WILL BE IN THE SAME LOGIC STATE AS THE Q OUTPUT.

2918 Quad-D Register

MOTOROLA

SN54LS253
SN74LS253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

DESCRIPTION — The LSTTL/MSI SN54LS/74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{E}_0$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

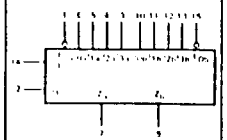
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0 S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output (Note b)	65 (25) U.L.	15 (7.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Multiplexer Output (Note b)	65 (25) U.L.	15 (7.5) U.L.

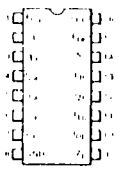
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH, 1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 2.5 U.L. for Military (54) and 6.5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

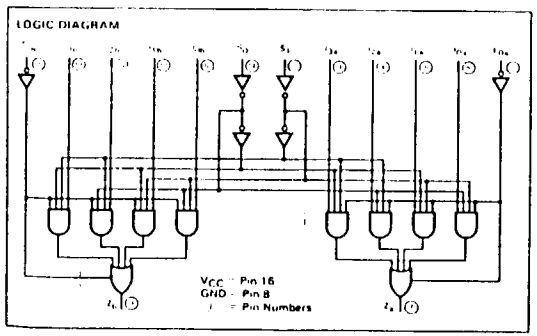
CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

NOTE:
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high-Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

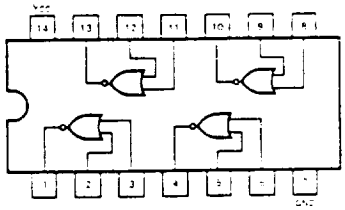
H = HIGH Level
L = LOW Level
X = Irrelevant
(Z) = High Impedance (Off) State

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage				
T_A	Operating Ambient Temperature Range				
I_{OH}	HIGH-Level Output Current				
I_{OL}	LOW-Level Output Current				

MOTOROLA

SN54LS02
SN74LS02



J Suffix — Case 632-07 (Ceramic)
N Suffix — Case 646-05 (Plastic)

QUAD 2-INPUT NOR GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

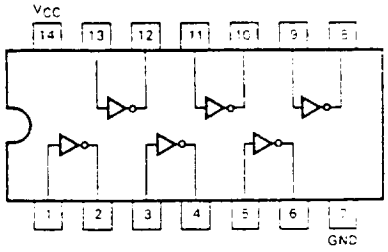
SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54 74	2.5 2.7	3.5 3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74 54 74		0.25 0.35	0.4 0.5	V	I_{OL} = 4.0 mA, V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20 0.1	μA mA	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				1.6 3.2	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	

MOTOROLA

SN54LS04
SN74LS04



J Suffix — Case 632-07 (Ceramic)
N Suffix — Case 646-05 (Plastic)

HEX INVERTER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54 74	2.5 2.7	3.5 3.5		V V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74 74		0.25 0.35	0.4 0.5	V V	I_{OL} = 4.0 mA I_{OL} = 8.0 mA V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20 0.1	μA mA	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				0.8 2.7	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

5404 Hex Inverter

APPENDIX B

TEMPERATURE STRESS TEST RESULTS

74LS138 @ 25 C (No Failure)

A0	A1	A2	E1	E2	E3	0	1	2	3	4	5	6	7
X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L

X = DON'T CARE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS138 (Device No. 1) @ 170 C

A0	A1	A2	E1	E2	E3	0	1	2	3	4	5	6	7
X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	H	H	H	H	H
H	H												
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	H	H	H	H
H	H	H	L	L	H	H	H	H	H	H	H	H	H

X = DON'T CARE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS138 (Device No. 2) @ 170 C

A0	A1	A2	E1	E2	E3	0	1	2	3	4	5	6	7
X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	H	H	H	H
H	H	H	L	L	H	H	H	H	H	H	H	H	H

X = DON'T CARE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74174 @ 25 C (No Failure)

CP	MR	D0	D1	D2	D3	D4	D5	Q0	Q1	Q2	Q3	Q4	Q5
X	L	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	L	L	L	L	L	L	L	L	L	L	L	L
↑	H	H	H	H	H	H	H	H	H	H	H	H	H

74174 @ 180 C

CP	MR	D0	D1	D2	D3	D4	D5	Q0	Q1	Q2	Q3	Q4	Q5
X	L	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	L	L	L	L	L	L	L	L	L	L	L	L
↑	H	H	H	H	H	H	H	H	H	H	L	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74174 (Device No. 2) @ 180 C

CP	MR	D0	D1	D2	D3	D4	D5	Q0	Q1	Q2	Q3	Q4	Q5
X	L	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	L	L	L	L	L	L	L	L	L	L	L	L
↑	H	H	H	H	H	H	H	H	H	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74174 (Device No. 3) @ 160 C

CP	MR	D0	D1	D2	D3	D4	D5	Q0	Q1	Q2	Q3	Q4	Q5
X	L	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	L	L	L	L	L	L	L	L	L	L	H	L
↑	H	H	H	H	H	H	H	H	H	H	H	H	H

74174 (Device No. 4) @ 120 C

CP	MR	D0	D1	D2	D3	D4	D5	Q0	Q1	Q2	Q3	Q4	Q5
X	L	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	L	L	L	L	L	L	L	L	L	L	L	L
↑	H	H	H	H	H	H	H	L	L	L	L	L	L

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74174 (Device No. 5) @ 100 C

CP	MR	D0	D1	D2	D3	D4	D5	Q0	Q1	Q2	Q3	Q4	Q5
X	L	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	L	L	L	L	L	L	L	L	L	L	L	L
↑	H	H	H	H	H	H	H	L	L	L	L	L	L

74LS257 @ 25 C (No Failure)

OE	S	IOA	IOB	IOC	IOD	I1A	I1B	I1C	I1D	YA	YB	YC	YD
H	X	X	X	X	X	X	X	X	X	L	L	L	L
L	H	X	X	X	X	L	L	L	L	L	L	L	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	L	X	X	X	X	L	L	L	L
L	L	H	H	H	H	X	X	X	X	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS194 @ 25 C (No Failure)

CP	MR	DSR	DO	D1	D2	D3	DSL	S0	S1	Q0	Q1	Q2	Q3
X	L	X	X	X	X	X	X	X	X	L	L	L	L
↑	H	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	X	X	X	X	X	H	L	H	L	L	L	H
↑	H	X	X	X	X	X	L	L	H	L	L	H	L
↑	H	H	X	X	X	X	X	H	L	H	L	L	H
↑	H	L	X	X	X	X	X	H	L	L	H	L	L
↑	H	X	L	L	L	L	X	H	H	L	L	L	L
↑	H	X	H	H	H	H	X	H	H	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS194 (Device No. 1) @ 190 C

CP	MR	DSR	DO	D1	D2	D3	DSL	S0	S1	Q0	Q1	Q2	Q3
X	L	X	X	X	X	X	X	X	X	L	L	L	L
↑	H	X	X	X	X	X	X	L	L	H	H	H	L
↑	H	X	X	X	X	X	H	L	H	H	H	L	H
↑	H	X	X	X	X	X	L	L	H	H	H	H	L
↑	H	H	X	X	X	X	X	H	L	H	H	H	H
↑	H	L	X	X	X	X	X	H	L	L	L	L	L
↑	H	X	L	L	L	L	X	H	H	L	L	L	L
↑	H	X	H	H	H	H	X	H	H	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS194 (Device No. 2) @ 200 C

CP	MR	DSR	DO	D1	D2	D3	DSL	S0	S1	Q0	Q1	Q2	Q3
X	L	X	X	X	X	X	X	X	X	L	L	L	L
↑	H	X	X	X	X	X	X	L	L	H	H	H	H
↑	H	X	X	X	X	X	H	L	H	H	H	H	H
↑	H	X	X	X	X	X	L	L	H	H	H	H	H
↑	H	H	X	X	X	X	X	H	L	H	H	H	H
↑	H	L	X	X	X	X	X	H	L	H	H	H	H
↑	H	X	L	L	L	L	X	H	H	H	H	H	H
↑	H	X	H	H	H	H	X	H	H	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS194 (Device No. 3) @ 80 C

CP	MR	DSR	DO	D1	D2	D3	DSL	S0	S1	Q0	Q1	Q2	Q3
X	L	X	X	X	X	X	X	X	X	L	L	L	L
↑	H	X	X	X	X	X	X	L	L	H	H	H	H
↑	H	X	X	X	X	X	H	L	H	H	H	H	H
↑	H	X	X	X	X	X	L	L	H	H	H	H	H
↑	H	H	X	X	X	X	X	H	L	H	H	H	H
↑	H	L	X	X	X	X	X	H	L	H	H	H	H
↑	H	X	L	L	L	L	X	H	H	H	H	H	H
↑	H	X	H	H	H	H	X	H	H	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS194 (Device No. 4) @ 60 C

CP	MR	DSR	DO	D1	D2	D3	DSL	S0	S1	Q0	Q1	Q2	Q3
X	L	X	X	X	X	X	X	X	X	L	L	L	L
↑	H	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	X	X	X	X	X	H	L	H	H	H	H	H
↑	H	X	X	X	X	X	L	L	H	H	H	H	H
↑	H	H	X	X	X	X	X	H	L	H	H	H	H
↑	H	L	X	X	X	X	X	H	L	L	H	H	H
↑	H	X	L	L	L	L	X	H	H	L	L	L	L
↑	H	X	H	H	H	H	X	H	H	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

74LS194 (Device No. 5) @ 80 C

CP	MR	DSR	DO	D1	D2	D3	DSL	S0	S1	Q0	Q1	Q2	Q3
X	L	X	X	X	X	X	X	X	X	L	L	L	L
↑	H	X	X	X	X	X	X	L	L	L	L	L	L
↑	H	X	X	X	X	X	H	L	H	L	L	L	H
↑	H	X	X	X	X	X	L	L	H	L	L	H	L
↑	H	H	X	X	X	X	X	H	L	H	L	L	H
↑	H	L	X	X	X	X	X	H	L	L	H	L	L
↑	H	X	L	L	L	L	X	H	H	L	H	L	H
↑	H	X	H	H	H	H	X	H	H	H	H	H	H

X = DON'T CARE

↑ = POSTIVE GOING CLOCK PULSE

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL