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Thomas Noll

Thomas Noll has a BS in Chemical Engineering from the University of Wisconsin, and over twenty years experience developing advanced materials and processes for PWBs and MCMs. He is currently a Senior Engineer at Foster-Miller, Inc., developing electronic packaging technology. Prior to this, he performed similar work at Teradyne Connection Systems, Digital Equipment and Rockwell-Collins. He is a member of IEEE and has published a number of papers in advanced substrate technology.

Abstract

Dielectric materials based on innovative Liquid Crystal Polymers (LCPs) have been used to fabricate surface mount PWBs with a coefficient of thermal expansion matched to leadless ceramic chip carriers. Proprietary and patented polymer processing technology has resulted in self-reinforcing material with balanced in-plane mechanical properties. In addition, LCPs possess excellent electrical properties, including a low dielectric constant (<2.9) and very low moisture absorption (<.02 %). LCP-based multilayer boards processed with conventional drilling and plating processes show improved performance over other materials because they eliminate the surface flatness problems of glass or aramid reinforcements. Laser drilling of blind vias in the LCP dielectric provides a very high density for use in direct chip attach and area array packages. The material is ideally suited for MCM-L and PCMCIA applications fabricated with very thin dielectric layers of the liquid crystal polymer.

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CONTROLLED THERMAL EXPANSION PRINTED WIRING BOARDS BASED ON LIQUID CRYSTAL POLYMER DIELECTRICS

Thomas E. Noll, Kent Blizzard, K. Jayaraj, Leslie S. Rubin
Foster-Miller, Inc.
Waltham, MA 02154

INTRODUCTION

Electronic packaging in the 1990s must meet the dual challenges of providing the performance requirements driven by semiconductor packaging, and the cost requirements driven by the emerging markets of telecommunications and data transfer referred to recently as the data superhighway. The transformation of chip packaging into surface mounted high I/O leadless ceramic carriers, and from there into direct chip attach approaches, continues to make a significant impact on the direction of printed wiring board technology development. Semiconductors first started appearing in leadless ceramic packages because of improved electrical characteristics due to elimination of the inductive wire leads. Failures of the solder joints connecting the packages to the PWBs immediately started occurring because the in-plane thermal expansion of the PWB (14-16 ppm/°C) relative to the ceramic (6-8 ppm/°C) created strains that cracked the solder fillets.

Extensive development efforts resulted in a family of solutions to prevent these failures. These efforts included restraining metal cores made out of copper-invar-copper, copper molybdenum, or other low expansion metals. Later, aramid-reinforced epoxy and polyimide laminate materials, negative thermal expansion of the fibers, were introduced as a solution (1,2). These packaging approaches are costly compared to conventional FR-4 or glass-reinforced polyimide multilayer boards. They also add significant weight and thickness to the module, severe drawbacks for avionics packaging or for portable electronics. Coupled with process improvements such as thick solder plating and improved package designs that minimize thermal stresses, these approaches have barely met packaging requirements. As semiconductors have increased in I/O with the advent of powerful microprocessors such as Digital's Alpha™, these approaches cannot meet the future requirements in an increasingly cost-sensitive marketplace. The drive to low cost, low weight, high performance personal communication devices will certainly bypass the thicker, heavier packaging methods.

To meet these future requirements, Foster-Miller, supported by Navy electronics packaging and NASA materials technology, began developing thermotropic Liquid Crystal Polymer (LCP) processing technologies to provide a dielectric material with significant advantages over other approaches (3). These melt processable LCPs are long-chain aromatic copolyester polymers that maintain a crystalline structure above their melting point. Because of the orientation of these "rigid rod" molecules during processing, LCPs are often termed self-reinforcing. LCPs offer improvements in a number of properties critical for surface mounted PWBs and advanced packaging substrates as shown in Table 1. One unique property is the low coefficient of thermal expansion (CTE) that can be achieved with these polymers. The in-plane CTE of LCPs is similar to aramid, with the added ad-

vantage that biaxial LCP films are strong enough to be used alone. Aramid, on the other hand, requires an impregnated resin, usually an epoxy or high temperature thermoset resin such as polyimide. The dielectric properties of LCPs are also consistently better than conventional materials, with a lower dielectric constant (Table 1 and Figure 1), very low moisture absorption, and a low dissipation factor, making LCPs a potential microwave substrate as well. Foster-Miller technology permits thermotropic LCPs to be extruded into balanced films of virtually any thickness so that mechanical and electrical design requirements are not limited by available constructions. These films are readily bonded to copper foil without requiring special adhesives and without the thickness limitation that reinforcements always impose.

LCP EXTRUSION PROCESS AND RAW MATERIAL FABRICATION

The Foster-Miller extrusion process is based on our proprietary and patented counter-rotating die technology, as shown in Figure 2 and described in more detail in other papers (3,4,5). The process differs from conventional extruding processes (6) in that it biaxially orients the polymer chains as they are being extruded, imparting balanced mechanical properties. Figure 3 shows typical modulus data for a 2 mil balanced film as a function of test direction. The graph is nearly symmetrical, showing that there is little variation in modulus, unlike typical slot extrusion processes where properties in the machine direction differ greatly from those in the transverse direction. Other properties, such as in-plane CTE, are also symmetrical as a result of this extrusion process. As shown in Figure 4, the liquid crystals are oriented at + Θ to - Θ as the film is produced. When this angle is 45 deg, the film is isotropic. By changing the extrusion conditions (flow rate, die rotation, take-up speed), highly uniaxial isotropic films can be produced. In contrast, conventional processing of LCP films results in unbalanced in-plane properties.

Table 1. Properties of Laminate Materials
for Controlled CTE PWBs

Material	LCP	FR-4	Epoxy/Aramid
CTE x, y ppm/°C	0 - 4	12 - 16	9 - 12
Dielectric Constant	2.6 - 2.9	4 - 4.4	3.5 - 3.8
Dissipation Factor	0.01 - 0.004	0.02 - 0.04	0.003 - 0.006
Moisture Content	<0.02%	0.1 - 0.3%	0.05 - 0.3

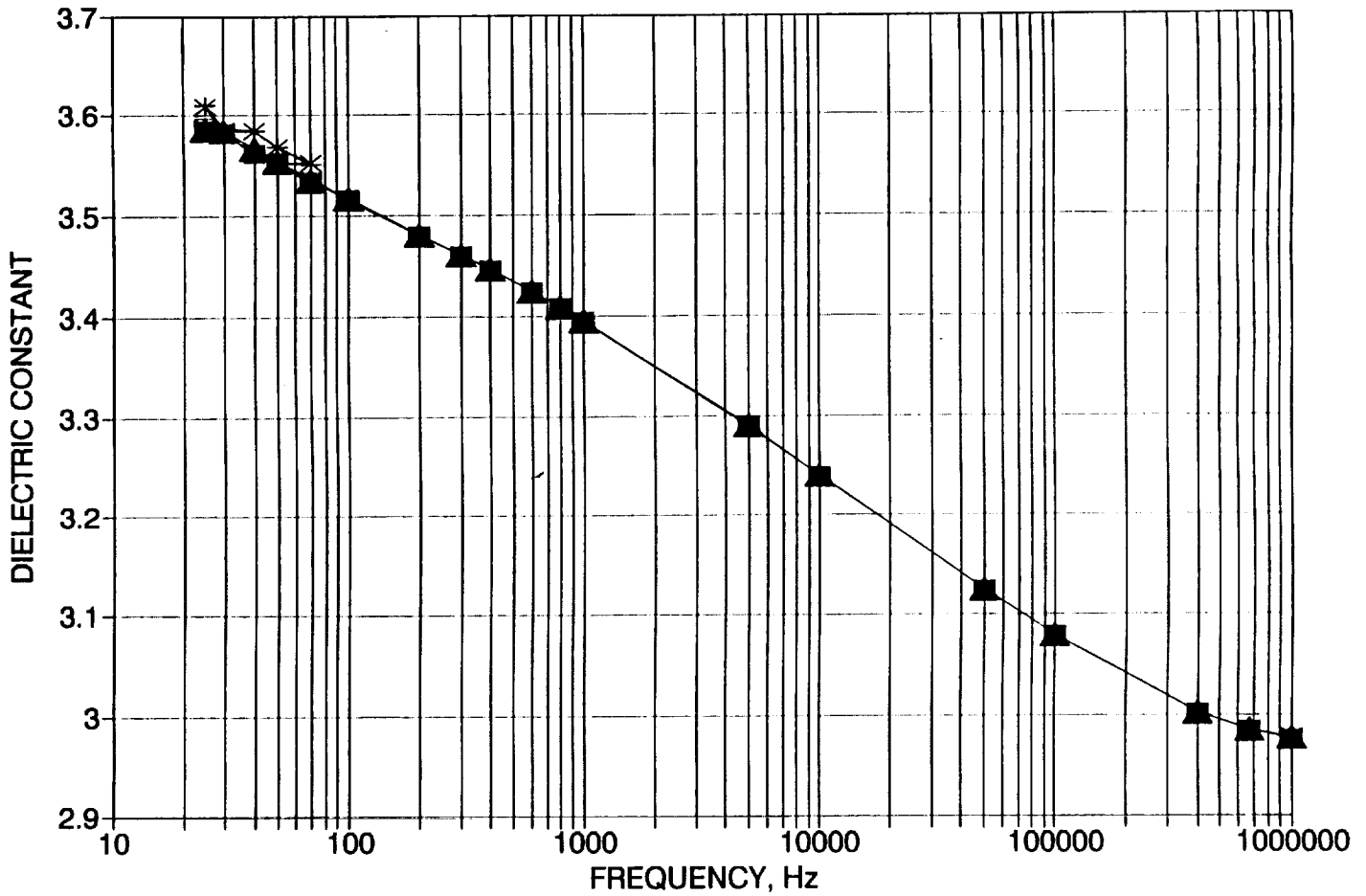
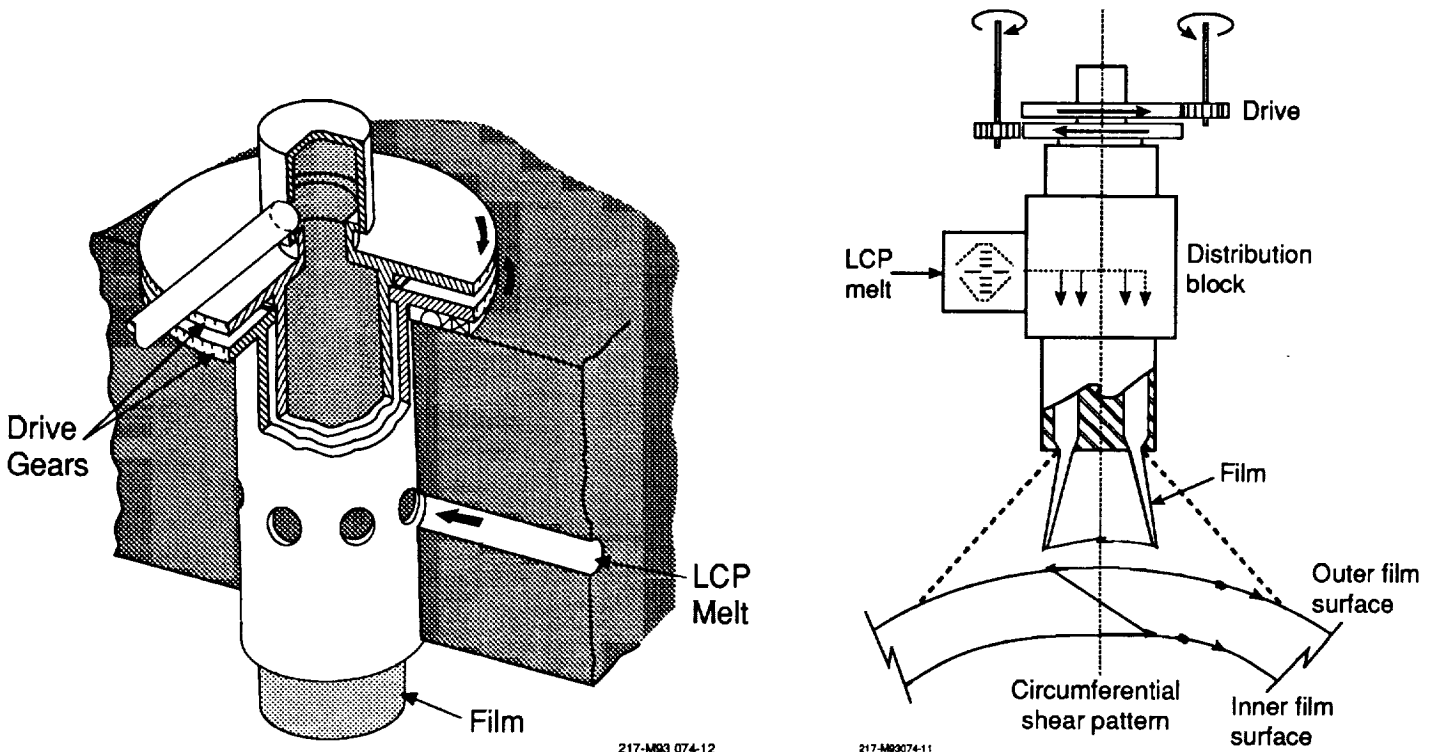


Figure 1. Dielectric Constant of LCP



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Figure 2. Counter-rotating Die

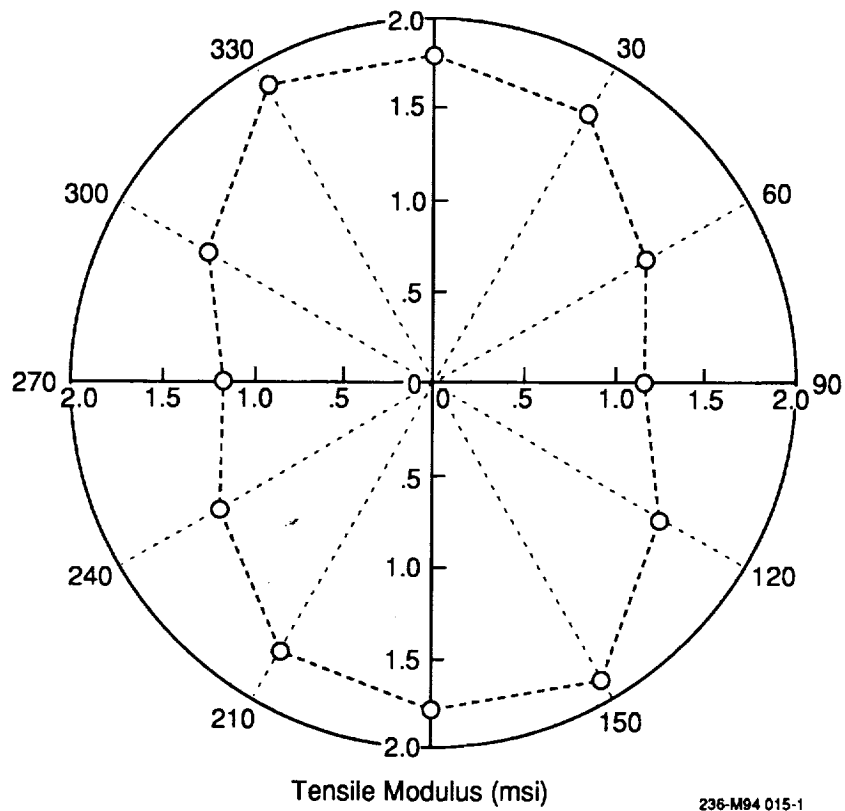


Figure 3. Balanced Modulus of Biaxially-oriented LCP Film

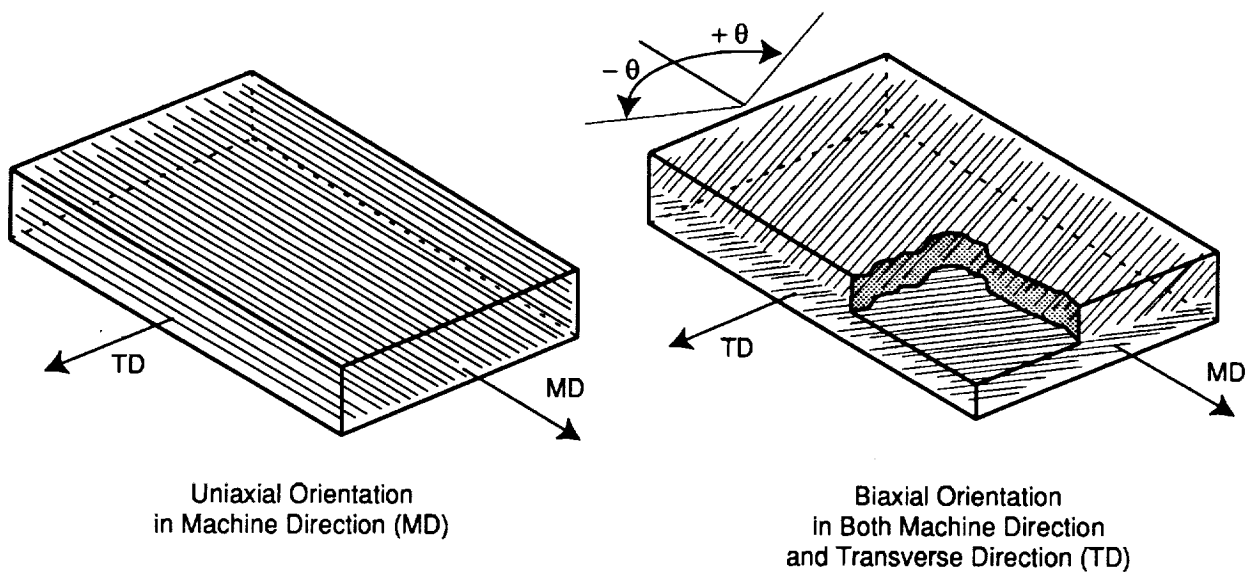


Figure 4. Uniaxial and Biaxial Orientation of LCP's

The in-plane CTE of LCP dielectric materials fabricated for this program with the counter-rotating die was 4 ppm/°C in both x and y directions. We modeled the expected CTE of a printed wiring board using the rule of mixtures to predict values for a completed board, as shown in Figure 5. Laminate material for printed wiring boards is clad with copper foil which has a CTE of 17 ppm/°C and a modulus approximately 10 times LCP. This analysis predicted that, with the construction used in our program and using an LCP with a low CTE, we would achieve a CTE that would very closely match the ceramic chip carriers used on surface mount product. The model also predicts CTE values for other combinations of copper and polymer. Figure 6 describes the CTEs of materials used in electronic packaging, showing that LCPs are an excellent choice for meeting thermal expansion requirements for surface mounted boards as well as

for future direct chip attached modules using LCPs with CTEs matched to silicon.

During the prototype fabrication of the copper clad material for this program, we continually evaluated the quality of our material in order to be sure that the program would result in a product that could be transferred to volume manufacturing. Results of two tests in particular demonstrate the suitability of the LCP laminates. The first, peel testing, was performed per MIL-P-13949, to ensure that the material has sufficient adhesion to copper, especially since we employ an adhesiveless process. Figure 7 shows the results of testing one ounce copper foil clad laminates. Since the LCP has a melt point above typical soldering and thermal cycling temperatures, these values, while not as high as values for FR-4 laminates, will not degrade at assembly tem-

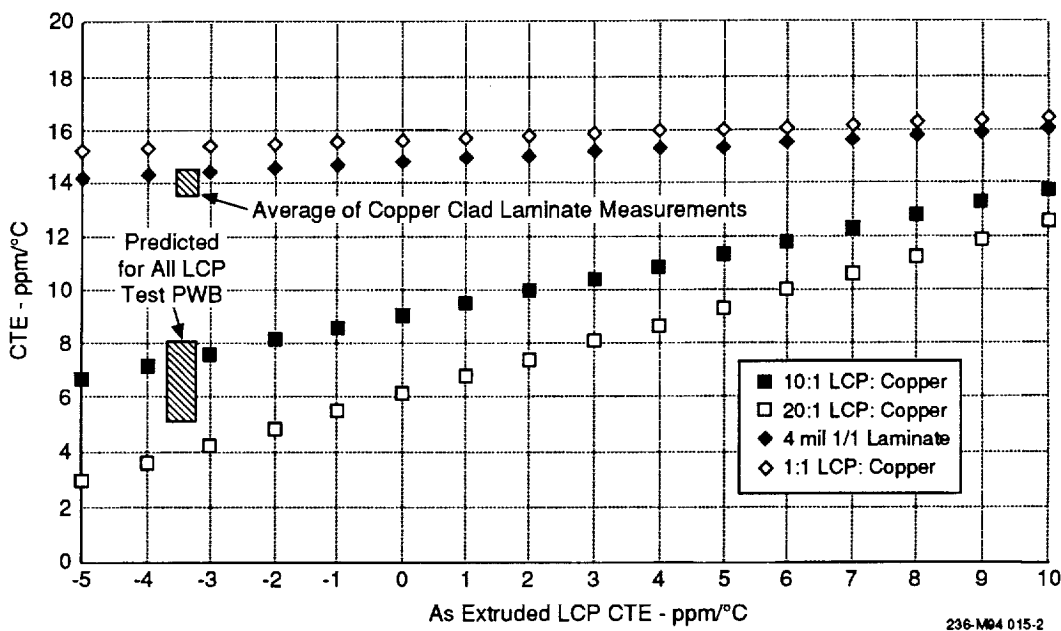


Figure 5. Construction Impact on CTE of NASA PWB

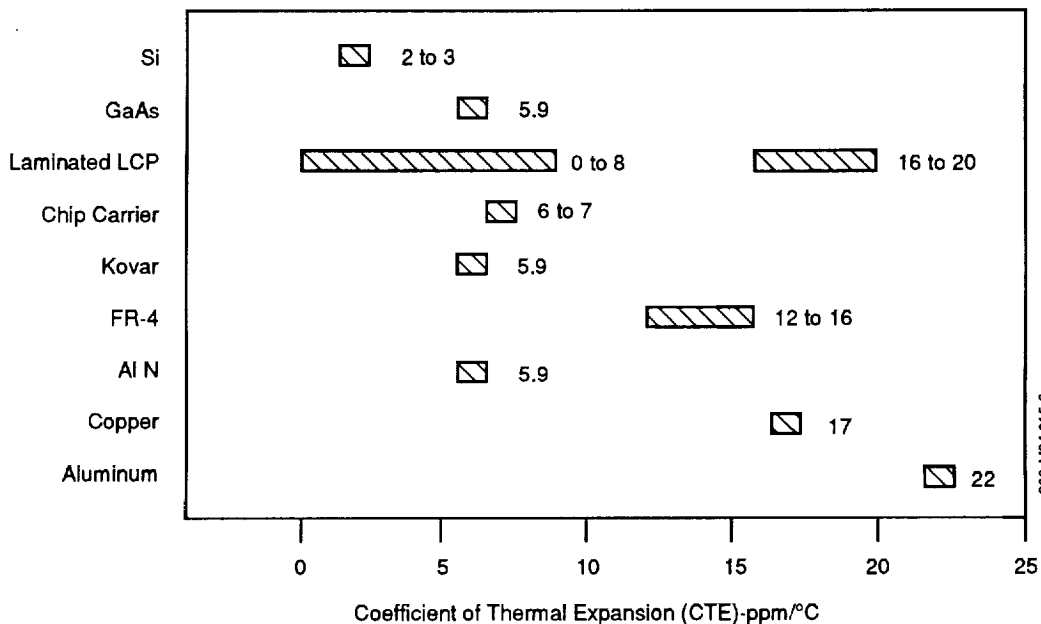


Figure 6. Controlled Low CTE

peratures, and the PWBs will maintain high reliability through assembly and during the product lifetime.

The second quality testing we measured routinely was thickness of the dielectric, as shown in Figure 8. Even though this material was made in lab prototype conditions, we were able to achieve a very tight distribution of dielectric thickness. With even better controls in a volume manufacturing facility, this material can easily exceed the tightest commercial or military specifications for laminate materials. This again is a benefit of using a self-reinforcing material where allowances do not have to be made for resin content or reinforcement thicknesses. This tight dielectric control is independent of material thickness, so for characteristic impedance requirements or overall board thickness any nominal value can be chosen for an application.

CONTROLLED CTE SURFACE MOUNT PWB TEST PLAN

The goal of our current program is to build, assemble and test multilayer, double-sided, surface mounted PWBs built with liquid crystal polymer dielectrics. The test board we chose for the test plan is shown in Figures 9 and 10. It contains the following features:

- 16 footprints for leadless ceramic chip carriers, daisy chained and routed to an edge connector for measurement of resistance with an automated system
- plated through hole via chains, daisy chained to allow measurement of resistance changes
- pads for attaching resistor and capacitors
- MIL-STD-275

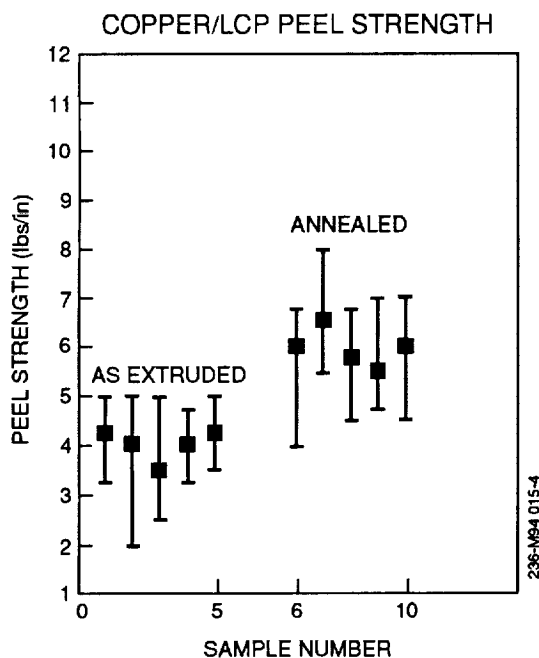


Figure 7. Adhesion Data for LCP Laminate

The board contains 10 layers, as shown in Figure 10—two internal plane layers, six signal layers and two external bonding layers. The copper is one ounce throughout, with dielectric thicknesses in the 0.0035 in. to 0.004 in. range. This board is used for qualifying to NASA specifications, where light weight and minimum thickness are highly desirable. For the bonding layer, we chose to build the PWBs with two approaches. The first boards were fabricated with random aramid-reinforced epoxy resin, using lamination cycles developed for all aramid products. Since the aramid materials are only slightly higher in CTE than the LCP dielectrics we are using, the overall board in-plane CTE will still be close to desired values. The second set of boards will be fabricated with an LCP bonding layer that melts at a lower temperature than the copper clad LCP. This difference in melt temperatures is necessary to prevent the copper clad cores from softening and distorting during the lamination cycle. This differential can be achieved either by selecting a different polymer with similar mechanical properties but a lower melt point, or by treating the copper clad LCP to raise the melt temperature above the as-extruded value. We are presently evaluating both approaches.

RESULTS OF THE PWB FABRICATION

Figure 11 shows one of the completed PWBs after surface mount assembly. The board has been coated with a conventional solder mask with good bonding of the mask to the LCP surface. A matrix of testing was performed to develop drilling parameters suitable for the material, followed by plasma and chemical hole cleaning experiments. Figure 12 shows a cross section of one of the

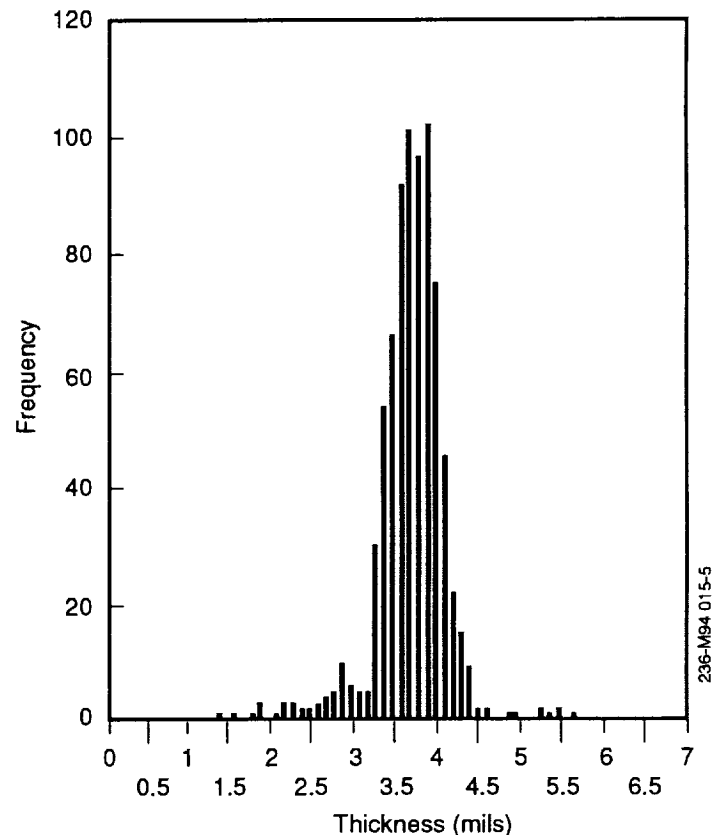
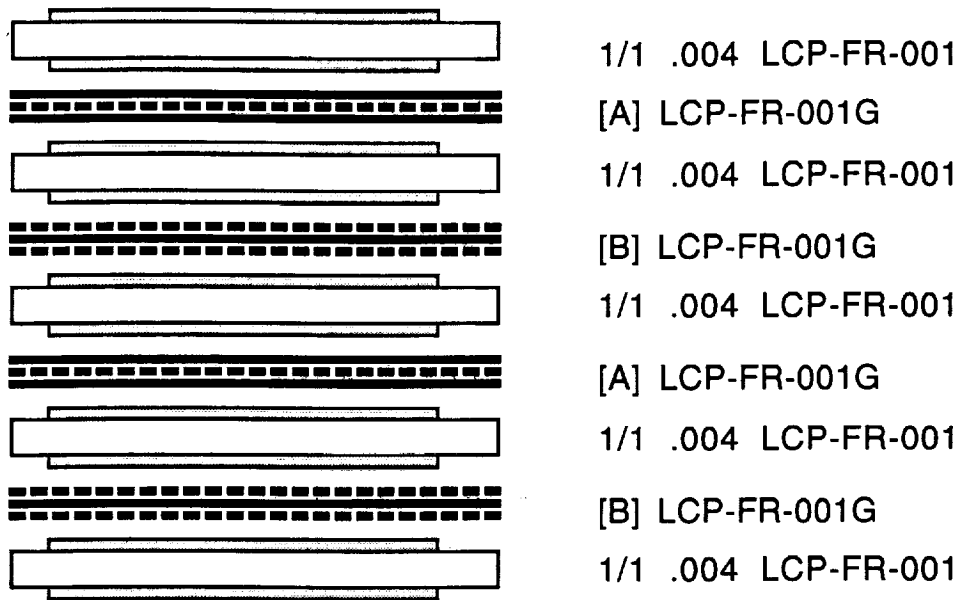
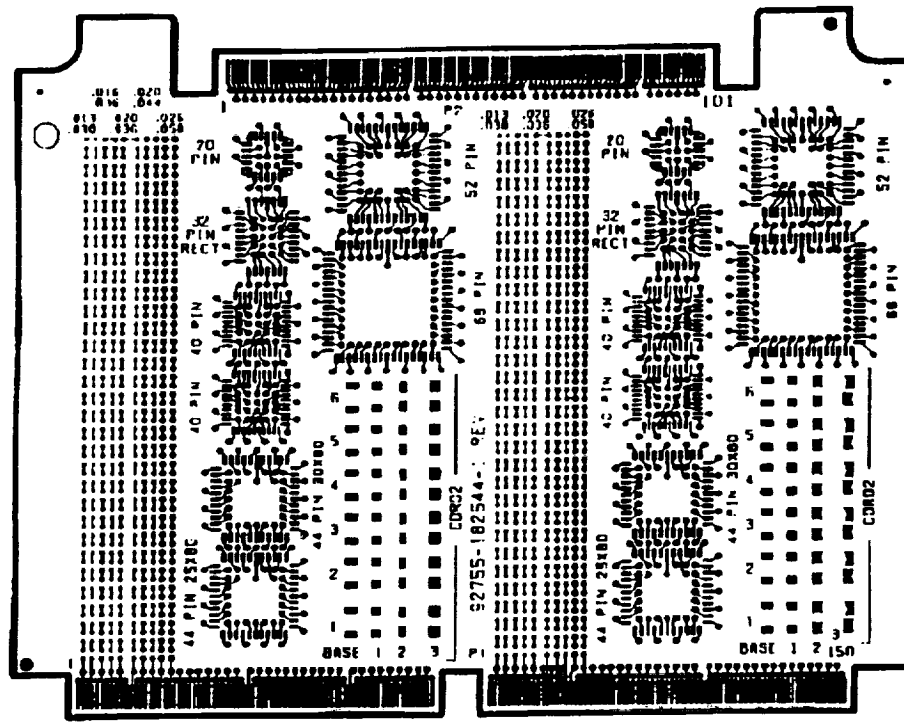


Figure 8. Thickness Control of March 1993 Lot of LCP Film



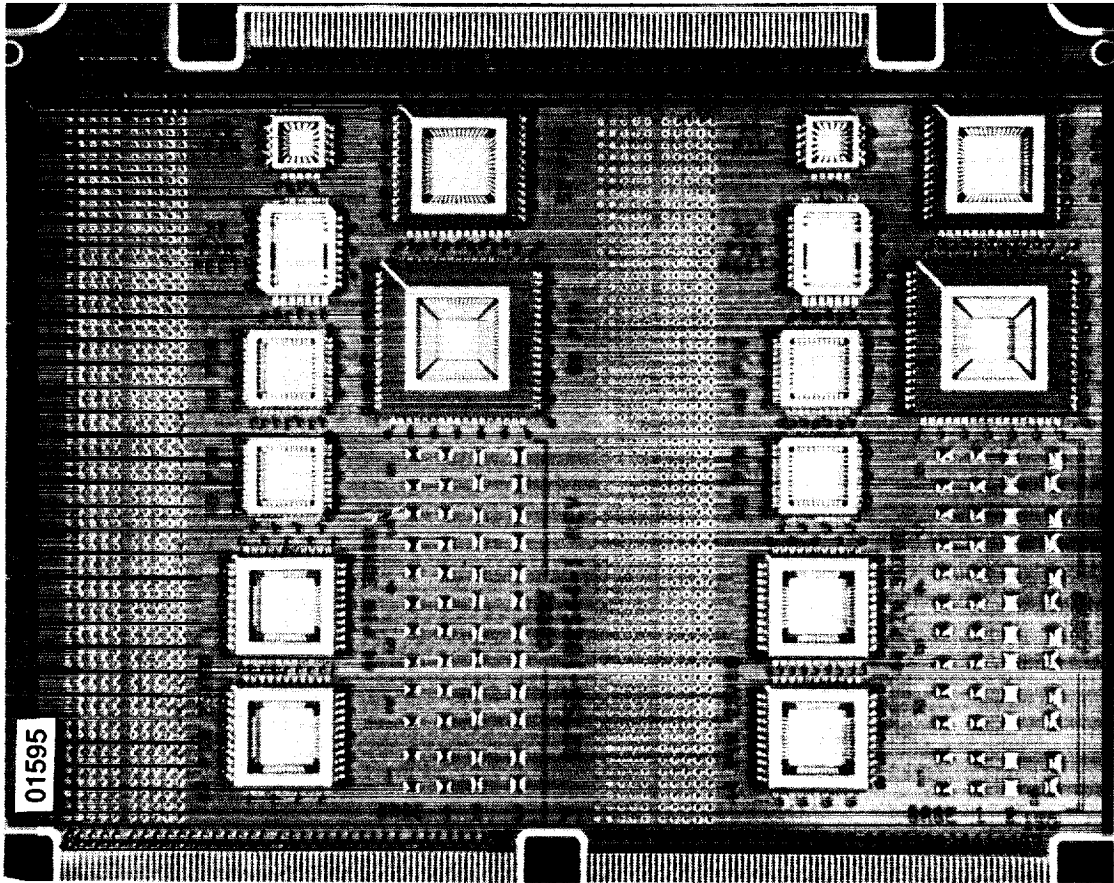


Figure 11. Photo of CTE Controlled Surface Mount PWB

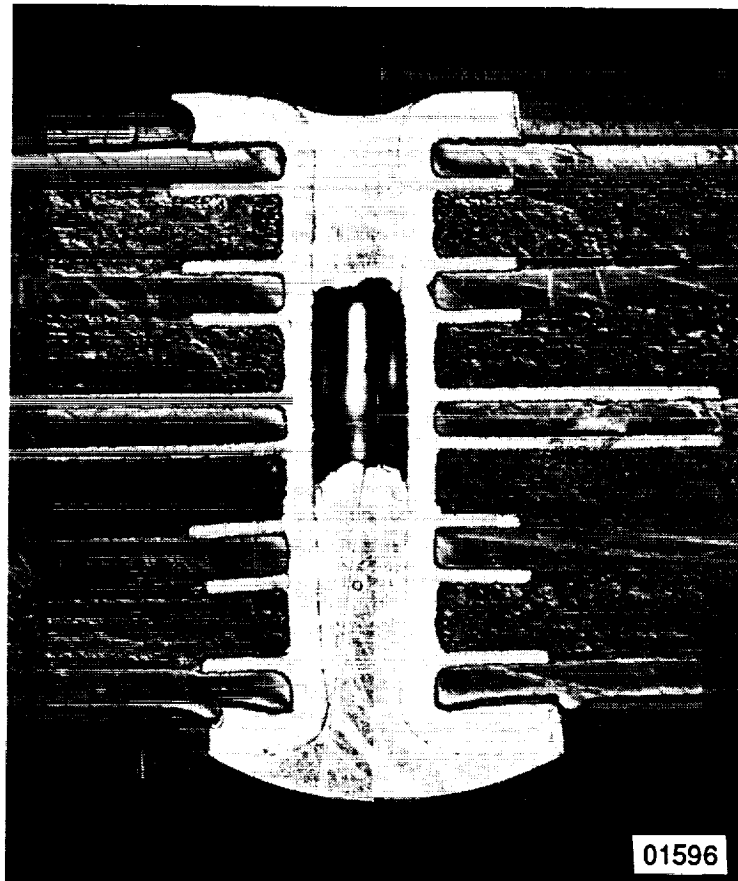


Figure 12. Cross Section after Thermal Stress (288°C Solder Float)

0.013 in. diameter holes after solder floating. The drilling and plating processes were optimized to provide good quality of the plated through hole with no evidence of cracks, pad lifting, or separation of plated wall. This has been of concern with unreinforced materials since their z-axis expansion is higher than some glass-reinforced materials. However, because the LCP material does not go through a significant glass transition temperature, the overall expansion from room temperature to solder temperatures is still significantly lower than a typical FR-4 PWB. This type of board will also be thinner than typical reinforced resin-based boards, which also minimizes the stress effects on the plated hole barrel.

As shown in this figure also, the layers line up with virtually no misregistration. Because of the low CTE of the LCP, the lack of shrinkage due to moisture desorption, and their high modulus compared to the bonding material used, we expected the layers to perform very well during process and this expectation was met in these test boards. X-ray analysis of the entire board shows that the pads line up on all parts of the panel. This is a key advantage of this material system for substrates that require much higher density, such as MCM-Ls, where board real estate cannot be dedicated to large pads to accommodate inner layer registration. Combining thinner dielectrics, very small holes, and the fine lines possible with a flat, unreinforced substrate, these materials will support the emerging thin board requirements.

Since the primary focus of this program was high reliability surface mounted PWBs with matched CTE, measuring that parameter was a critical part of demonstrating that this is a successful approach. Figure 13 summarizes CTE measurements from sections taken from the LCP aramid board, an all LCP board and a polyimide glass/LCP board also fabricated during the program. A thermomechanical analyzer was used to measure CTE in-plane (x and y) as well as z-axis. As expected, the all LCP PWB provided the lowest in-plane CTE, closely matching the goal of 6-8 ppm/°C. The LCP laminate/aramid bond sheet board showed slightly higher values since the high resin aramid bond materials show slightly higher CTE. The z-axis values were also within expected ranges for these materials. The numbers we obtained from the actual boards closely match the predicted values. We are using the data from these tests along with physical data on

the LCP materials such as modulus to generate reliability models for LCP PWBs. This work is being performed at the CALCE center of the University of Maryland where they have developed extensive models for surface mount reliability and will be reported in a later paper.

SUMMARY

Based on the results we have reported here, as well as in our other packaging programs, we will continue to develop thermotropic liquid crystal polymers as dielectric materials for electronic packaging applications. We have demonstrated that LCP-based surface mounted printed wiring boards can be successfully fabricated to military specifications. The potential applications that these materials are suitable for include laminate-based multichip modules (MCM-L), thin memory cards (PCMCIA) and smart cards, as well as other semiconductor packaging, such as ball grid arrays that currently use glass-reinforced PWB materials. Unlike many new materials that have shown performance advantages in electronic packaging, the LCP materials will also provide cost competitiveness. Table 2 compares material costs for a number of laminate materials, clearly showing that LCPs, because they are self-reinforcing, are significantly lower than other polymer-based CTE controlled materials. In addition, the lower processing costs which are possible because the material can be fabricated in conventional PWB facilities, coupled with the improved functionality that can be achieved, make LCP materials strong candidates for meeting the needs of emerging electronic products.

Table 2. Cost of LCP-Based PWB Materials

FR-4	1
BT/Glass	1.3 - 1.4
Cyanate Ester/Glass	1.9 - 2.1
Polyimid/Glass	2
Epoxy Aramid	3 - 5
LCP	0.8 - 1.2

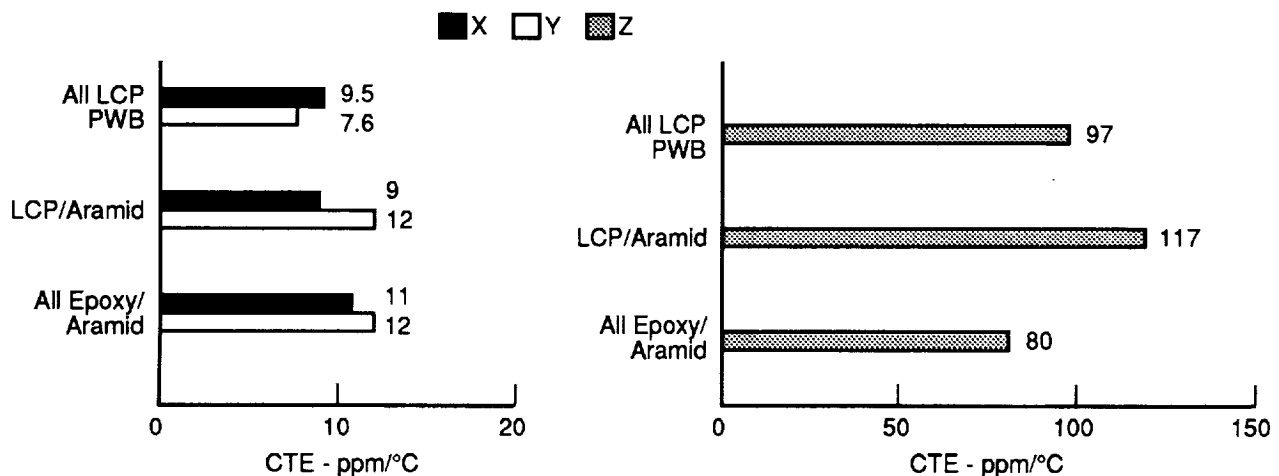


Figure 13. Results of CTE Testing

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