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Design and Implementation of a Hybrid Digital Phase-Locked Loop With a TMS320C25—An Application to a Transponder Receiver Breadboard

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Design, modeling, analysis, and simulation of a phase-locked loop (PLL) with a digital loop filter are presented in this article. A TMS320C25 digital signal processor (DSP) is used to implement this digital loop filter. In order to keep the compatibility, the main design goal was to replace the analog PLL (APLL) of the Deep-Space Transponder (DST) receiver breadboard's loop filter with a digital loop filter without changing anything else. This replacement results in a hybrid digital PLL (HDPLL). Both the original APLL and the designed HDPLL are Type I second-order systems. The real-time performance of the HDPLL and the receiver is provided and evaluated.

I. Introduction

Future NASA missions will require low-cost, small-sized, low-power-consumption spacecraft telecommunication equipment. To achieve the best design within mission resources, one must incorporate emerging technologies in the flight hardware. These requirements motivate the study of replacing a baseband analog loop filter with a digital filter in the phase-locked loop (PLL) of the existing X-band (7.145–7.19 MHz) transponder receiver breadboard.

Conventional spacecraft transponders employ analog circuits from the front-end antenna to the baseband carrier phase-tracking loop. With new digital technology, it is possible to build a very reliable all-digital IF and baseband circuit by using digital signal-processing techniques. However, before building a space-qualified all-digital transponder, it is preferable to experiment on a hybrid digital PLL (HDPLL) by using an existing X-band Deep-Space Transponder (DST) receiver breadboard as a first step in order to build confidence and obtain design experience. Furthermore, in order to keep the compatibility, the main design goal is limited to replacing an analog PLL (APLL) with an equivalent HDPLL without changing anything else. This implies a restricted design approach to the HDPLL. Modeling and computer simulation of the HDPLL are required to validate the algorithm and basic approach. This article describes the design, analysis, modeling, simulation, and real-time performance of a HDPLL of the X-band DST receiver breadboard.

The design specifications and functional description of the carrier tracking loop are summarized in Section II.

The conventional analog filter and APLL for various input signal levels are given in Section III. Section IV describes digital filter design, the HDPLL, and the analysis. Digital filter implementation and breadboard performance of the HDPLL are given in Section V. Finally, conclusions and recommendations are given in Section VI.

II. Design Requirements

The DST receiver specifications are listed as follows: The carrier signal tracking threshold is -157.3 dBm. The dynamic range is 88 dB (carrier threshold to -70 dBm). The noise figure at the DST receiver input is 1.4 dB nominal. The tracking range is ± 250 kHz minimum at the assigned channel frequency. The steady-state tracking error at a carrier signal level greater than -110 dBm shall be less than 1 percent per 40 KHz. The capture range is ± 1.3 KHz at a carrier signal level greater than -120 dBm. The acquisition and tracking rate is at least 550 Hz/sec at a carrier signal level greater than -110 dBm.

A DST receiver breadboard was built that met specifications [1], using all analog components in the APLL. The carrier phase-tracking APLL is a Type I second-order system with built-in characteristics, as follows:

(1) The two-sided noise bandwidth ($2B_L$) of the carrier tracking loop at threshold is 18 Hz.

(2) The signal-to-noise ratio (SNR) in the carrier tracking channel at the phase detector input is -25 dB.

(3) The damping factor at threshold (-157.3 dBm) ranges from 0.4 to 0.6.

(4) The loop predetection filter bandwidth is equal to 5000 Hz.

III. Analog Phase-Locked Loop

The basic block diagram of the receiver breadboard of the DST is given in Fig. 1(a). The simplified APLL which tracks carrier phase is given in Fig. 1(b). The equivalent HDPLL is obtained by replacing the analog loop filter with a digital filter, as shown in Fig. 1(b) and as will be discussed in the next section. A bandpass limiter is used in the APLL and HDPLL receivers to maintain a constant total power at the input to the loop [2,3]. This minimizes the total mean-square error of the loop over a wide range of input SNR's. It is also used to protect various loop components, the phase detector in particular, where signal and noise levels could otherwise vary over several orders of magnitude and exceed the dynamic range of these components.

By measuring the analog loop filter of the DST receiver breadboard, the loop filter parameters τ_1 and τ_2 are obtained and its transfer function is given as follows:

$$F(s) = \frac{A_0\,(1+\tau_2 s)}{1+\tau_1 s} \tag{1}$$

where $\tau_2 = 0.0464$ sec, $\tau_1 = 3655$ sec, and $A_0 = 43.4$ dB.

Because the bandwidth of the loop predetection bandpass filter is 5 kHz, the threshold level at the transponder input is -157.3 dBm. Consequently, the suppression factor $\acute{\alpha}$ is 0.0531 at threshold and 1 at strong signal (50 dB above threshold) [2]. A detailed discussion on the suppression factor $\acute{\alpha}$ is provided in Appendix A. The closed-loop transfer function of the linearized APLL is given in [3] with an open-loop dc gain parameter $k = 2.2(10^7)$. The parameter A_0 is included in parameter k [1].

$$H(s) = \frac{1+\tau_2 s}{1+\left[\tau_2 + \frac{1}{\acute{\alpha}k}\right] s + \frac{\tau_1}{\acute{\alpha}k} s^2} \tag{2}$$

For simulation purposes, the linearized APLL transfer function is computed for the input at threshold and strong signal. Computer simulations are conducted for both cases. The magnitude and phase responses of the APLL are shown in Figs. 2(a) and 2(b) at threshold and Figs. 3(a) and 3(b) at strong signal, respectively. The damping factor is 0.5 for threshold and 2.18 for strong signal. The two-sided equivalent loop noise bandwidth ($2B_L$) is 18 Hz at threshold and 160 Hz ($2B_L$) at strong input signal. Time domain responses of impulse, step, ramp error at both threshold and strong input signal cases are shown in Figs. 4(a–c) and 5(a–c), respectively.

The phase margins of the APLL are 44.5 deg and 85.6 deg at threshold and strong signal cases, respectively. Since phase is always greater than 180 deg, the gain margin is then not used. This APLL is a Type I second-order system with $\tau_1 >> \tau_2$ and $\tau_1 >> 1$. Therefore, $F(s)$ can be modelled as a perfect integrator, as follows:

$$F(s) \approx \frac{A_0\,(1+\tau_2 s)}{\tau_1 s} \tag{3}$$

This mathematical model of $F(s)$ will be used to develop the equivalent digital filter in the next section for easy DSP implementation.

IV. Digital Filter Design, the HDPLL, and Analysis

The analog filter $F(s)$ of the APLL is replaced by an equivalent digital filter and employed together with an analog-to-digital converter (ADC) and digital-to-analog converter (DAC) in the HDPLL as shown in Fig. 1(b). A sampling rate must be selected first for the HDPLL. Since the 3-dB bandwidth of the bandpass limiter is 5 kHz and the DSP board employed provides the best performance at a sampling rate of 50 kHz, the sampling rate selected is 50 kHz. The higher the sampling rate (50 >> 5 kHz), the more the HDPLL performs like the analog loop.

A. Digital Filter Design

Two design steps are required to obtain digital filters. In step one, a digital filter algorithm must be developed. In step two, the digital filter coefficients must be quantized and scaled properly for fixed-point arithmetic implementation of the HDPLL.

1. Digital Filter Algorithm. Based on the analog carrier loop filter transfer function, three digital filter design methods [4,5] are considered. These are bilinear transformation, hold equivalence (also known as step-invariant), and impulse-invariant methods. Since the sampling frequency is much higher than the APLL noise equivalent bandwidth, the bilinear transformation method can be applied directly without prewarping the analog frequency.

The bilinear transformation is

$$F_1(z) = F(s)\Big|_{s=\frac{2(z-1)}{T(z+1)}} = \frac{bz+c}{z-1} \tag{4}$$

where

$$b = \frac{A_0\,(T+2\tau_2)}{2\tau_1}$$
$$c = \frac{A_0\,(T-2\tau_2)}{2\tau_1} \tag{5}$$

The hold equivalence is

$$F_2(z) = (1-z^{-1})\left(Z\left[\frac{F(s)}{s}\right]\right) = \frac{bz+c}{z-1} \tag{6}$$

where Z[.] represents a Z-transform of [.],

$$b = \frac{A_0\tau_2}{\tau_1}$$
$$c = \frac{A_0(T-\tau_2)}{\tau_1} \tag{7}$$

The impulse invariance is

$$F_3(z) = T\,(Z\,[F(s)]) = \frac{bz+c}{z-1} \tag{8}$$

where

$$b = \frac{A_0\,(T+\tau_2)}{\tau_1}$$
$$c = \frac{-A_0\tau_2}{\tau_1} \tag{9}$$

The parameters b, c, and associate zeros of the digital filters are obtained and given in Table 1.

Among these three digital filters, parameters b, c, and zero location are very close to each other. This is because the sampling frequency selected is much higher than the analog loop filter 3-dB bandwidth. Consequently, all three digital filters have nearly the same characteristics. However, the bilinear transformation is better than the other two transformations in preserving the phase response [10]. Hence $F_1(z)$ is chosen as the digital filter algorithm and will be quantized for fixed-point DSP implementation.

2. Quantization and Scaling [5]. Several simulations are conducted with fixed-point arithmetic in order to determine the number of bits of filter coefficients, digital gain, and scaling factor for implementation. It is found that the quantization causes a larger effect than which transformation is used. This is because the analog loop filter has an extremely narrow bandwidth in comparison to the sampling frequency. The pole and zero of the corresponding digital filter may cancel out each other if improper scaling and quantization are applied. Finally, 16-bit coefficients and a high digital gain ($g_d = 148$) are selected for the following reasons:

(1) Easy and fast acquisition.

(2) Accurate digital representation for parameters b and c and to avoid pole-zero cancellation due to quantization.

(3) Easy implementation by a TMS320C25.

(4) To preserve the noise equivalent bandwidth by choosing $g_d = 148$ for both strong signal and threshold. (More discussion on the g_d is provided in the analysis section.)

The 16-bit digital filter is obtained by

$$F_q(z) = \frac{[b_q z + c_q]\, 2^{-8}}{z - 1} \tag{10}$$

where

$$b_q = \frac{\text{Int}\left[(g_d b/A_0)\left(2^8(2^{15}) - 1\right) + 0.5\right]}{2^{15} - 1} = 15764/32767$$

$$c_q = \frac{\text{Int}\left[(g_d c/A_0)\left(2^8(2^{15}) - 1\right) + 0.5\right]}{2^{15} - 1} = 15758/32767$$

$$g_d = \text{digital gain} = 148$$

Int [.] represents the integer portion of [.].

This digital filter exhibits similar performance to the analog carrier loop filter. However, an extra 8-bit gain (2^8) is applied to form b_q and c_q in Eq. (10) for maximizing numerical accuracy and results in 16-bit fixed-point coefficients for DSP implementation. This 8-bit gain is then compensated by 2^{-8} at the output of the digital filter. Hence the total filter gain remains the same as that of the analog filter. Notice that distortion due to quantization is very small and can be ignored.

B. The Hybrid Digital Phase-Locked Loop

The simplified block diagram of a HDPLL is shown in Fig. 1(b). By comparing Figs. 1(a) and 1(b), one notes that the analog filter of Fig. 1(a) is replaced by an equivalent digital filter with the 16-bit ADC and DAC in Fig. 1(b). We model the ADC plus digital filter plus DAC as an impulse modulator, a fixed-point digital filter algorithm, and a zero-order hold. By using the block diagram analysis of sampled data systems [4], the sampled (discrete-equivalent) transfer function, $H(z)$, of the linearized HDPLL is obtained. A detailed derivation is given in Appendix B. Again, computer simulations are conducted at both threshold and strong signal cases. The magnitude and phase responses of the HDPLL are shown in Figs. 2(a) and 2(b) at threshold, and Figs. 3(a) and 3(b) at strong signal, respectively. Notice that frequency responses of the APLL and HDPLL are approximately the same except for the phase response at frequencies above 1 kHz. This shows that the HDPLL preserves both magnitude and phase characteristics very well at frequencies less than 1 kHz. Consequently, the noise equivalent loop bandwidth of the HDPLL is the same as that of the APLL at both strong signal and threshold cases. Therefore, the phase jitter of the HDPLL is the same as that of the APLL.

The impulse, step responses, and ramp-error response of the HDPLL at both threshold and strong signal cases are shown in Figs. 6(a–c) and 7(a–c), respectively. The ramp-error response shows the dynamic phase error (DPE) in the acquisition. The digital gain is 148 at threshold in Figs. 6(a–c). Two different digital gains are used in Figs. 7(a–c). Notice that these time domain responses of the HDPLL are significantly different from counterparts of the APLL. Specifically, the impulse response of the HDPLL has a much smaller dynamic range than that of the APLL. On the other hand, the DPE of the HDPLL has a much larger dynamic range than that of the APLL. However, the impulse response of the HDPLL becomes larger with a larger digital gain, as shown in Fig. 7(a). The DPE becomes smaller with a larger digital gain, as shown in Fig. 7(c). It shows that digital gain significantly controls the dynamic range of the time domain response. These features indicate that the dynamic range of the accumulator of the processor must be large enough to accommodate the DPE during the acquisition process. We select $g_d = 148$ for having a B_L which meets the specification. It is observed that step responses of the HDPLL show that the damping factor is about 0.5 at threshold and larger than 1 at strong signal. Notice that there is a smoothing analog filter used after digital-to-analog (D/A) conversion in the HDPLL. Consequently, this HDPLL is a Type I, second-order closed-loop system.

C. Analysis

1. Digital Gain Versus Stability. It is well known that second-order, Type I APLLs are unconditionally stable. However, Type I HDPLLs are only conditionally stable and Type I second-order HDPLLs are unstable at high loop gains. The root locus plot of the HDPLL is shown in Fig. 8. Both poles are forced to remain on or near the real axis for the maximum possible range of loop gain, as shown in Fig. 8. The pole of the HDPLL moves outside the unit circle and becomes unstable when digital gain is larger than 50,465. By using $g_d = 148$, the phase margin and gain margin of the HDPLL are computed at both threshold and strong signal cases. Table 2 compares the phase margin between the APLL and the HDPLL. The phase margin of the HDPLL is about the same as that of the APLL. Consequently, the HDPLL is very stable at both threshold and strong signal cases.

2. Digital Gain Versus Noise Equivalent Bandwidth. In general, it does not matter whether the gain is in the digital or analog portion of the loop. However, since

all analog parts of the HDPLL are fixed components in the receiver breadboard, only the digital filter gain can be easily adjusted as a flexible parameter. Consequently, the relationship between the digital gain and the noise equivalent bandwidth becomes important. The one-sided noise equivalent digital bandwidth B_{Ld} (Hz) of the HDPLL is given by

$$B_{Ld} = \frac{1}{2T\,(H^2(1))\,2\pi j} \oint_{|z|=1} H(z)H(z^{-1})\frac{dz}{z} \qquad (11)$$

where T is the update time in seconds and $H(z)$ is the transfer function of the HDPLL with $H(1) = 1$. The B_{Ld} can be calculated by using either numerical integration or Table III in [6]. At $g_d = 148$, the $2B_{Ld}$ is obtained as 156 Hz and 17 Hz at both strong signal and threshold, respectively. The noise equivalent bandwidth of the HDPLL is nearly the same as that of the APLL. Furthermore, the relationship between the g_d and the B_{Ld} is depicted in Fig. 9 at strong signal case. It is observed from Fig. 9 that the noise equivalent loop bandwidth increases when digital gain increases. However, the B_{Ld} will be greater than 25 kHz if the digital gain is greater than 26,400. Consequently, the g_d should be less than 26,400 to avoid aliasing errors.

3. Steady-State Phase Error. Under the assumption of linearity, the phase error (no noise) in the z-domain is given by the following expression:

$$\Theta(z) = \{1 - H(z)\}\,\theta_i(z) \qquad (12)$$

where $H(z)$ is the closed-loop transfer function of the HDPLL and $\theta_i(z)$ is the z-transform of the phase input. Furthermore, an instantaneous Doppler, denoted as $d(t)$, is assumed as follows:

$$d(t) = \frac{\omega_i(\Omega_o + \Lambda_o t)}{c} \qquad (13)$$

where

ω_i = carrier frequency (rad/sec)

Ω_o = spacecraft speed (m/sec)

Λ_o = spacecraft acceleration (m/sec^2)

c = speed of light (m/sec)

The input phase $\theta_i(t)$ of the HDPLL is the integration of the $d(t)$ with respect to time and is obtained by

$$\theta_i(t) = \frac{\omega_i(\Omega_o t + 0.5\Lambda_o t^2)}{c}$$

By applying the final value theorem to the phase-error equation, we get

$$\begin{aligned}\phi_{ss} &= \lim_{z\to 1}(z-1)(1-H(z))\theta_i(z) \\ &= \lim_{z\to 1}(1-H(z))\left(\frac{\omega_i}{c}\right) \\ &\quad \times \left[\frac{\Omega_o T z}{(z-1)^2} + 0.5\Lambda_o T^2 z\left(\frac{z+1}{(z-1)^3}\right)\right] \\ &= \frac{(\omega_i/c)\Lambda_o T}{(k/A_0)(b_q + c_q)2^{-8}} \qquad (14)\end{aligned}$$

For the Voyager mission at an 8.4-GHz carrier frequency, we assume acceleration values of $\Lambda_o = 0.32$ m/sec^2 for Uranus [7]. The steady-state phase error at the strong signal case is obtained as 0.607 deg at encounter. Clearly, this HDPLL meets the specification that requires a steady-state error of 1 deg, as mentioned in Section II.

4. The Phase-Error Variance of the PLL. The phase-error variance of the linearized APLL after the bandpass limiter is calculated as

$$\sigma_e^2 = \left(\frac{N_0 B_L}{P_c}\right)\Gamma$$

where

N_0 = the one-sided noise power spectral density

P_c = the carrier power

Γ = limiter performance factor = $(1+\rho_i)/(0.862+\rho_i)$

ρ_i = $P_c/N_0 W_i$ = the SNR input to the limiter

W_i = the bandwidth of the bandpass filter = 5000 Hz

The limiter performance factor equation is obtained experimentally [8]. From the breadboard DST second IF gain distribution measurements,[1] parameters of both

[1] J. Perret, "Breadboard Uplink Command Channel Performance Analysis Calibration and Testing Accomplished in 1991," Interoffice Memorandum 3367-93-171 (internal document), Jet Propulsion Laboratory, Pasadena, California, May 1993.

threshold and strong signal cases are obtained with the automatic gain control (AGC) on (threshold) and off (strong signal), respectively. (See Table 3.)

Based on the parameters provided in Table 3, the SNR of both the APLL and HDPLL can be computed as follows:

$$\text{SNR of the APLL} = 10 \log \frac{1}{\sigma_e^2} \text{ dB}$$

$$= 10 \log \left[\left(\frac{P_c}{N_0 W_i} \right) - \log (\Gamma) \text{ dB} + \log \left(\frac{5000}{B_L} \right) \right] \text{ dB}$$

$$\text{SNR of the HDPLL} = 10 \log \left[\frac{1}{\left(\frac{N_0 B_{Ld}}{P_c} \right) \Gamma} \right] \text{ dB}$$

The SNR of both APLL and HDPLL at both threshold and strong signal is provided in Table 4.

V. Digital Filter Implementation and Breadboard Performance

A PC board of the Ariel DSP-16 Plus is employed together with an X-band DST breadboard for real-time digital loop filter implementation. The bandwidth of both antialiasing (input) and smoothing (output) filters is 20 kHz. Both ADC and DAC are 16-bit with a selected sampling rate of 50 kHz for best board performance. A TMS320C25 digital signal processor is employed to implement this 16-bit digital loop filter. This DSP has a 32-bit-wide accumulator. However, a 40-bit equivalent accumulator is employed to accommodate the large dynamic range required during the acquisition process.

Transponder receiver experiment results are obtained in real-time operation. Evaluation experiments include receiver tracking threshold sensitivity and static phase errors for X-band uplink frequency offset. All measurements were made at room temperature (25 deg C). The theoretical equation used for the calculation of the carrier tracking threshold is given in Appendix A. The measured tracking threshold sensitivity at the receiver best lock frequency (7162.3125 MHz) is -155.3 dBm, which is higher than the design threshold value of -157.3 dBm. This is due to the dc bias at the analog-to-digital (A/D) converter of the DSP board. However, the measured hybrid digital receiver threshold characteristics show good correlation with the actual analog receiver performance and agree with theoretical performance over the tracking range, as shown in Fig. 10. Figure 11 shows a linear relationship between measured static phase error (SPE) voltage versus uplink frequency offset over the receiver tracking range. The measured SPE shows a good correlation with expected performance (Appendix C). The measured tracking ranges of APLL and HDPLL are ± 270 and ± 280 kHz, respectively, which is greater than the required tracking range value of ± 250 kHz.

VI. Conclusion

This article presents the design, implementation, analysis, and performance testing of a HDPLL of the DST receiver breadboard. The baseband carrier loop filter has been successfully replaced by a 16-bit digital filter (digital integrator). A TMS320C25 DSP is employed to implement this filter in real time. All simulations show that the designed fixed-point digital filter works very well in the HDPLL. The simulated performance in the frequency domain of the HDPLL is nearly the same as the original APLL at both threshold and strong signal cases. However, time-domain responses of the HDPLL are controlled by the digital gain. To meet the B_L requirement, the g_d is chosen as 148. Hence, the HDPLL's dynamic range of time-domain responses is different than that of the APLL.

Testing results are in good agreement with predicted characteristics, with the exception of tracking threshold (about a 2-dB loss due to the dc bias of the A/D). This loss can be reduced if the digitization occurs at the IF signal, instead of the digitizing baseband signal. In conclusion, it has been demonstrated that the baseband carrier loop filter of the DST receiver can be replaced by a digital filter. By using this HDPLL as a basic model, an advanced digital receiver employing digital IF techniques is recommended for future deep-space transponders [9,10]. An adaptive scheme is also recommended to solve the high transient DPE problem as follows. First, to reduce the transient DPE in the acquisition mode, the digital gain of the digital filter should be increased. Consequently, the loop bandwidth is opened up. This operation will ensure a larger acquisition sweep rate. Secondly, after the phase is locked, the digital gain should be reduced. Hence, the loop bandwidth is reduced in the tracking mode. This operation will reduce phase noise and ensure a limited steady-state tracking error.

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Table 1. Parameters and zeros of digital filters.

Design method	Parameter b $(\times 10^{-3})$	Parameter c $(\times 10^{-3})$	Zero
Bilinear transformation	1.879256	−1.878446	0.999569
Hold equivalence	1.878851	−1.878041	0.999569
Impulse invariance	1.879661	−1.878851	0.999569

Table 2. A comparison of phase margin and gain margin between the APLL and HDPLL.

	Phase margin		Gain margin	
	APLL, deg	HDPLL, deg	APLL	HDPLL, dB
Threshold	44.5	47	N/A[a]	−77
Strong signal	85.6	86	N/A[a]	−51

[a] Gain margin is not used because the phase of the APLL is always greater than 180 deg.

Table 3. Measured signal and noise power input to the limiter and associated parameters ρ_i and Γ at threshold and strong signal.

	P_c, dBm	N_0W_i, dBm	ρ_i	Γ
Threshold	−26.5	−1.5	0.003	1.16
Strong signal	−26.5	−87.5	1.2×10^6	1.0

Table 4. The SNR of both the APLL and HDPLL at both threshold[a] and strong signal.

SNR	APLL, dB	HDPLL, dB
Threshold	1.80	2.05
Strong signal	78.96	79.07

[a] Threshold is defined as the point where probability is 50-percent lock and 50-percent unlock.

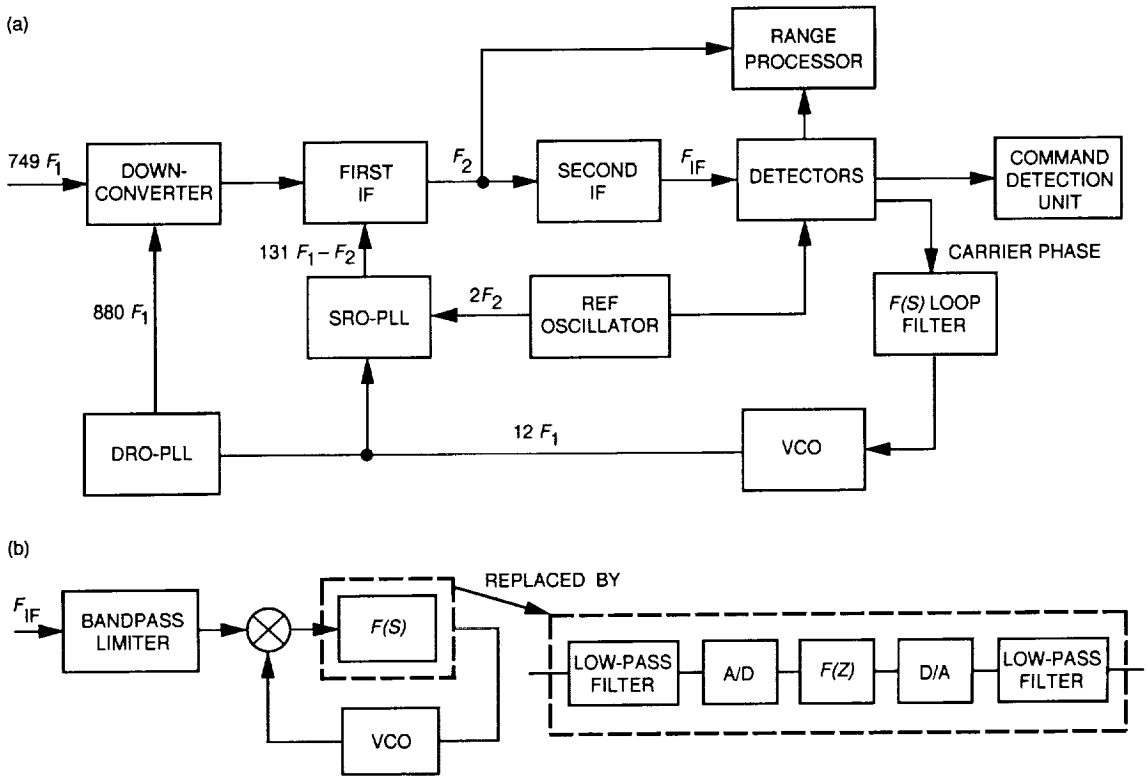

Fig. 1. Functional block diagrams of (a) the receiver of the DST breadboard and (b) the simplified carrier phase tracking loop with the analog loop filter replaced by a digital filter.

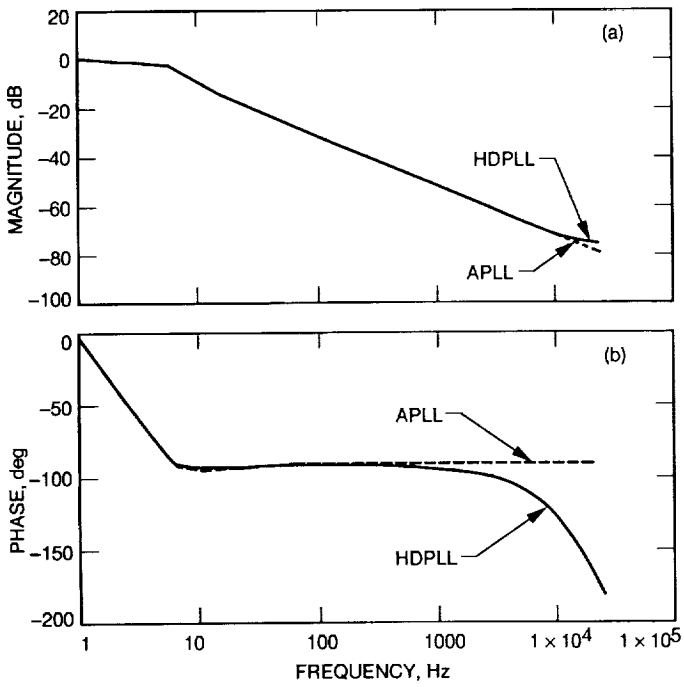

Fig. 2. Simulated responses of the APLL and HDPLL at the threshold: (a) magnitude and (b) phase.

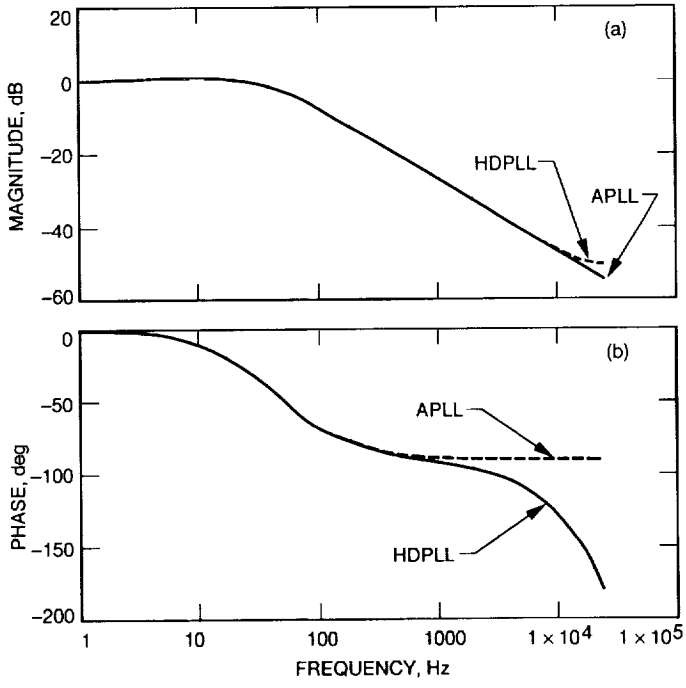

Fig. 3. Simulated responses of the APLL and HDPLL at the strong signal input: (a) magnitude and (b) phase.

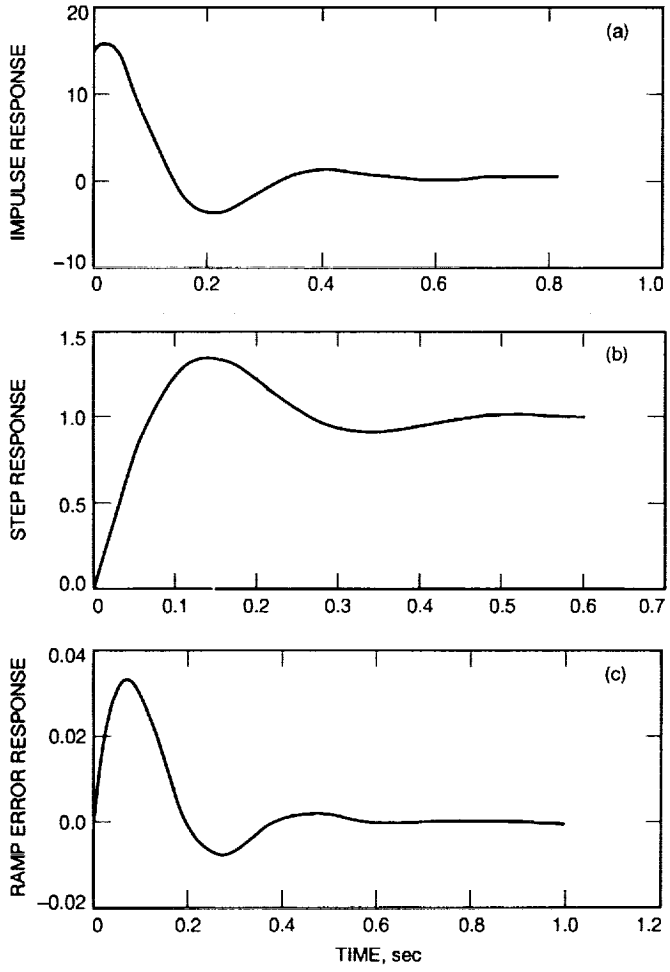

Fig. 4. Time-domain responses of the APLL at threshold: (a) impulse, (b) step, and (c) ramp error.

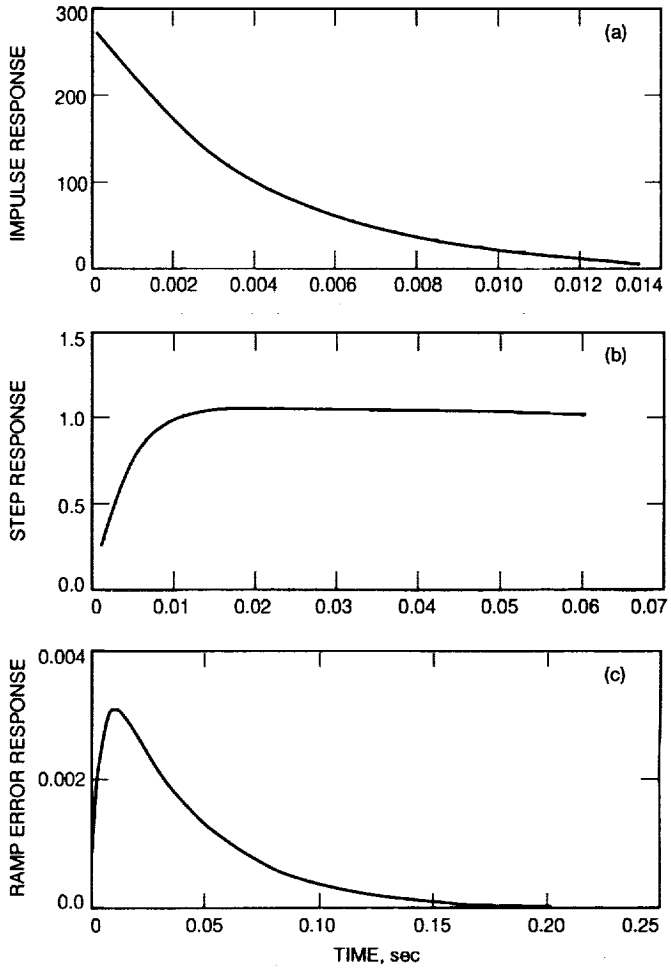

Fig. 5. Time-domain responses of the APLL at strong signal: (a) impulse, (b) step, and (c) ramp error.

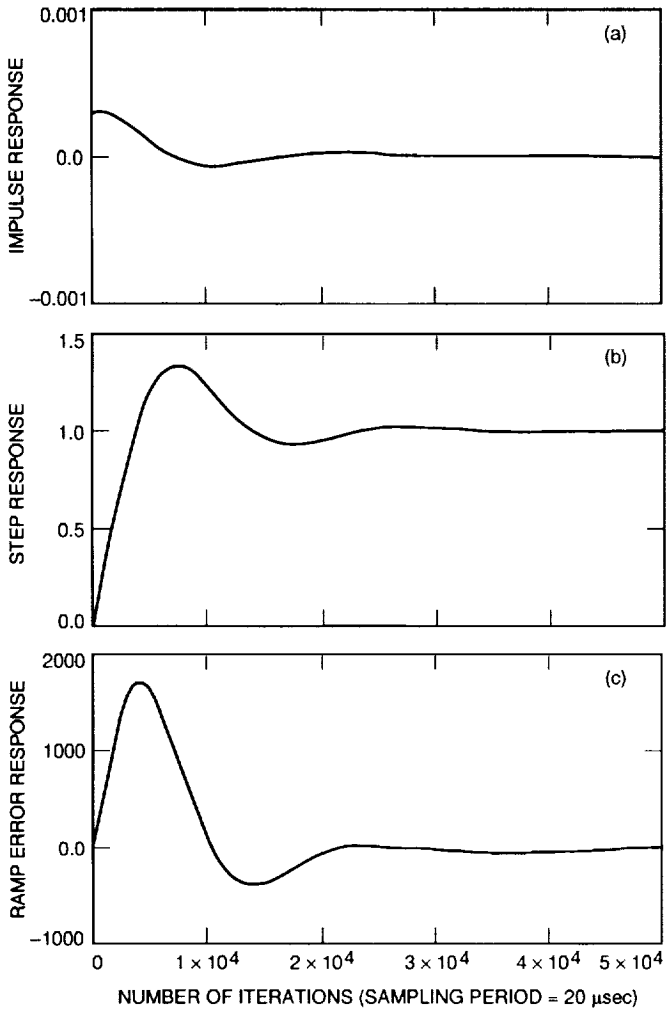

Fig. 6. Responses of the HDPLL at threshold: (a) impulse, (b) step, and (c) ramp error.

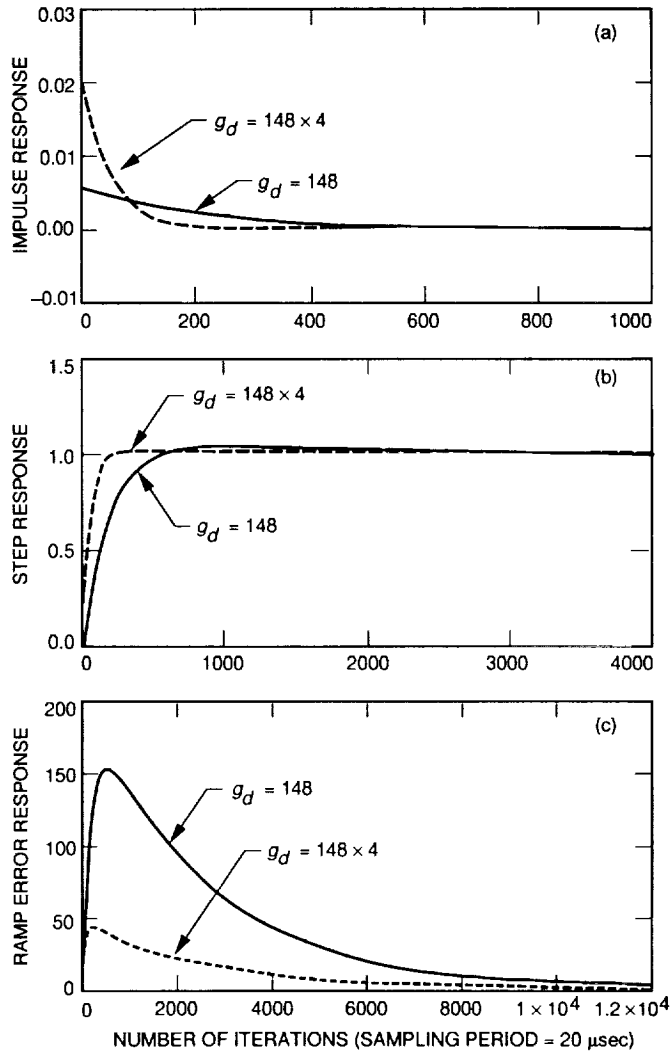

Fig. 7. Responses of the HDPLL at strong signal with two different digital gains: (a) impulse, (b) step, and (c) ramp error.

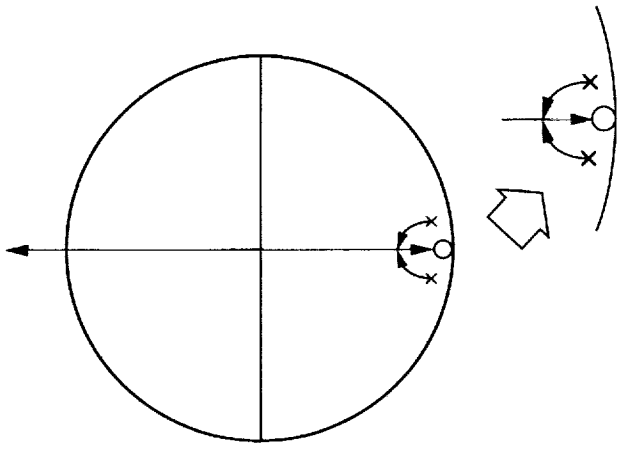

Fig. 8. The root locus plot of the HDPLL.

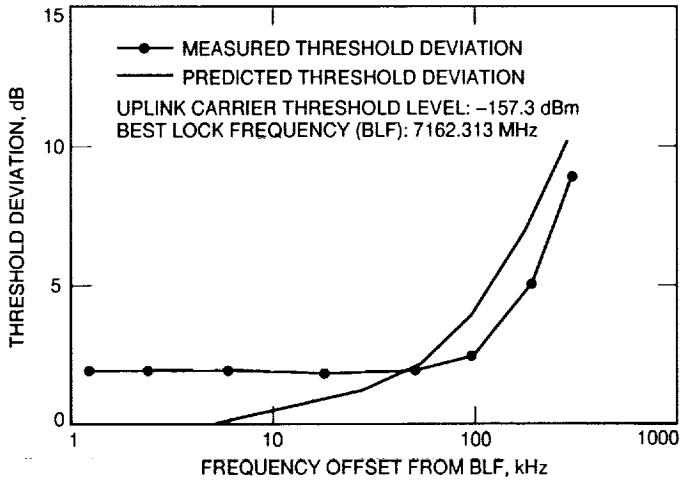

Fig. 10. The measured receiver carrier tracking threshold versus the offset frequency.

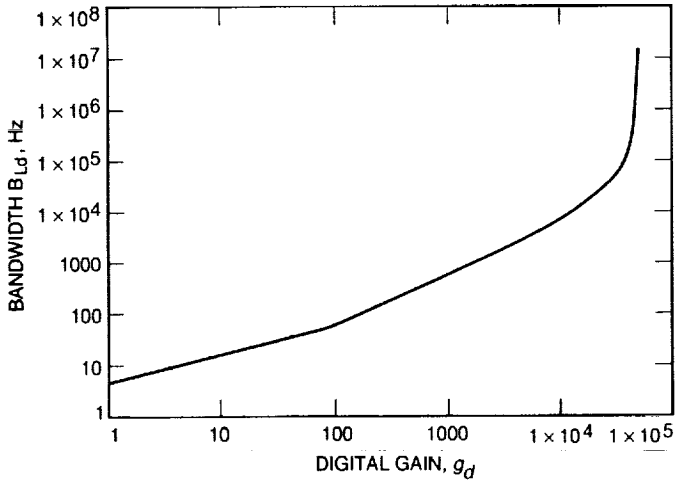

Fig. 9. Digital gain g_d versus one-sided noise equivalent bandwidth B_{Ld} at strong signal.

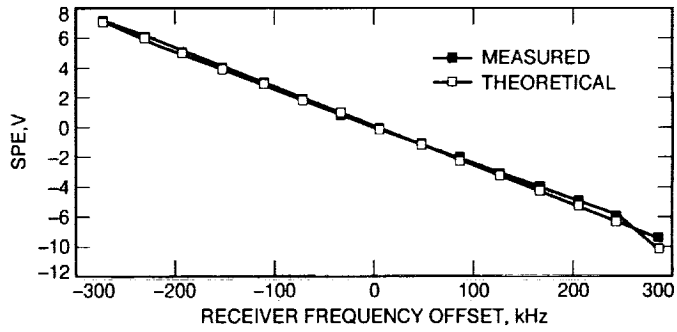

Fig. 11. The measured static phase error voltage of the HDPLL versus uplink frequency offset over the receiver tracking range.

Appendix A

A Mathematical Model of the Suppression Factor and Tracking Threshold Calculation

The mathematic model of the suppression factor α and calculation of the carrier tracking threshold of a PLL receiver are provided here.

The carrier tracking threshold of a PLL receiver is defined as the minimum uplink signal required to maintain a 50 percent probability of lock at any given offset from best lock frequency (BLF). The worst-case carrier tracking threshold signal level S_o at the transponder input port and at the BLF is determined from the following equations:

$$S_o = kT_oF(2B_L)L \tag{A-1}$$

where

S_o = the received input signal level for tracking threshold at receiver BLF

k = Boltzmann's constant

T_o = the reference system temperature

F = receiver noise figure at the transponder input

L = the receiver carrier channel loss

The S_o is calculated and is equal to -157.5 dBm (the receiver carrier tracking threshold) for a $2B_L$ of 18 Hz, channel loss of 1 dB, and noise figure of 2.9 dB at 290 K.

The PLL receiver limiter suppression factor α is given by [3]

$$\alpha = 1/\sqrt{1 + \frac{2B_{LI}S_o}{\pi B_L S}} \tag{A-2}$$

where

S = the receiver input signal power level

B_{LI} = the noise equivalent predetection bandwidth

In the region near tracking threshold, the phase offset θ_e at the PLL phase detector can be estimated from an empirical equation

$$\begin{aligned} \theta_e &= 1 - \frac{\alpha_0}{\alpha} \\ \alpha_o &= \left(\frac{\pi B_L}{2B_{LI}}\right)^{0.5} \end{aligned} \tag{A-3}$$

Notice that α_0 is the limiter suppression factor at carrier threshold.

The phase-detector output voltage is given by an empirical equation

$$V_c = \alpha \sin(\theta_e)\cos(\theta_e) \tag{A-4}$$

The frequency offset at X-band is then obtained as

$$\Delta f = V_c k \tag{A-5}$$

where k = open loop dc gain of the PLL.

Appendix B

Derivation of the HDPLL Closed-Loop Transfer Function

The HDPLL closed-loop transfer function derivation is provided here [4].

From Fig. 1(b), the DAC is modeled as $(1 - e^{-sT})/s$, and the voltage-controlled oscillator (VCO) is modeled as k/s. Then the output of the sampled-data system is obtained as

$$\theta_o^* = \frac{G^*}{1 + G^*}\,\theta_i^* \qquad \text{(B-1)}$$

where

θ_o^* = the sampled output of the HDPLL

θ_i^* = the sampled input of the HDPLL

$$G^* = \alpha\left(1 - e^{-sT}\right) F_q^*\left(\frac{k/g}{s^2}\right)^*$$

$$= \alpha\left(1 - e^{-sT}\right) F_q\left[\frac{T(k/g)e^{sT}}{\left(e^{sT} - 1\right)^2}\right]$$

$$= \frac{AF_q(z)}{z - 1}$$

$$= \frac{A(b_q z + c_q)}{(z - 1)^2}$$

and

$$A = \frac{\alpha k T 2^{-8}}{g}$$

$$z = e^{sT}$$

b_q and c_q are 16-bit digital filter coefficients.

The closed-loop transfer function is then

$$H(z) = \frac{\theta_o^*}{\theta_i} = \frac{A(b_q z + c_q)}{z^2 + (Ab_q - 2)z + Ac_q + 1} \qquad \text{(B-2)}$$

Appendix C

Relationship Between SPE and Uplink Frequency Offset

The relationship between the static phase error (SPE) and the uplink frequency offset over the receiver tracking range is found as follows.

The VCO receives SPE as input and provides output frequency at $12F_1$ with a gain of 628 Hz/V (measured). The frequency of the received uplink signal is $749F_1$, as shown in Fig. 1(a). Consequently, the uplink frequency offset from the best lock frequency is obtained as

$$\Delta f = -\text{SPE}(628)\left(\frac{749}{12}\right) \tag{C-1}$$

The minus sign is used for the negative feedback PLL.