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Micro-Opto-Mechanical Devices and Systems Using Epitaxial Lift Off

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Introduction

The integration of high quality, single crystal thin film gallium arsenide (GaAs) and indium phosphide (InP) based photonic and electronic materials and devices with host microstructures fabricated from materials such as silicon (Si), glass, and polymers will enable the fabrication of the next generation of micro-opto-mechanical systems (MOMS) and optoelectronic integrated circuits. Thin film semiconductor devices deposited onto arbitrary host substrates and structures create hybrid (more than one material) near-monolithic integrated systems which can be interconnected electrically using standard inexpensive microfabrication techniques such as vacuum metallization and photolithography. These integrated systems take advantage of the optical and electronic properties of compound semiconductor devices while still using host substrate materials such as silicon, polysilicon, glass and polymers in the microstructures. This type of materials optimization for specific tasks creates higher performance systems than those systems which must use trade-offs in device performance to integrate all of the function in a single material system. The low weight of these thin film devices also makes them attractive for integration with micromechanical devices which may have difficulty supporting and translating the full weight of a standard device. These thin film devices and integrated systems will be attractive for applications, however, only when the development of low cost, high yield fabrication and integration techniques makes their use economically feasible. In this paper, we discuss methods for the alignment, selective deposition, and interconnection of thin film epitaxial GaAs and InP based devices onto host substrates and host microstructures.

In integrated systems, it is often advantageous to utilize a variety of materials, each suited to a particular purpose. Compound semiconductors are useful for optical and optoelectronic devices, and silicon, polysilicon, glass, metals and polymers have been widely investigated for microstructure and microelectronic systems. High quality compound semiconductor devices, particularly those suited for optoelectronic applications, are generally grown lattice matched or near lattice matched. For the integration of GaAs onto single crystal Si, heteroepitaxial growth has been intensively investigated [1]. However, the crystal quality of this material is often insufficient for many optical applications. To integrate compound semiconductor devices with host materials which have no periodicity, however, such as polysilicon, glass, metals and polymers, the compound semiconductor cannot be grown directly upon such a host. In many cases, the substrate which is used as a nucleation seed for lattice matched growth is not essential to the performance of the epitaxial device. In fact, some device structures can be significantly improved upon if the growth substrate is removed from the lattice matched epitaxial device layers. These thin film epitaxial devices are light weight and the device designer has access to both sides of the epilayer, uninhibited by the substrate.

Bellcore first reported the separation of epitaxial layers from the lattice matched growth subsytrate using selective etches, and named the process epitaxial liftoff (ELO) [2]. A thin aluminum arsenide (AlAs) sacrificial layer is grown lattice matched onto a GaAs substrate, and GaAs device epilayers of interest are grown on top of this AlAs layer. The GaAs lattice matched epilayers are separated from the growth substrate by selectively etching the AlAs sacrificial layer. These epilayers are then mounted onto a variety of smooth substrates and this sheet of material is subsequently etched to define individual devices. This ELO material is very high quality [2]; devices tested before and after ELO show no degradetion in device performance. These materials are currently being used for the integration of GaAs materials onto host substrates such as Si, glass, lithium niobate, and polymers [2-5].

Although the Bellcore technique yields high quality material, it has several problems, including the inability to align and selectively deposit the thin film devices, smoothness constraints on the host substrate, and difficulties in contacting both sides of the patterned device. In this paper, we report two modified ELO techniques which enable the alignment and selective deposition of a device or array of devices onto a host structure, and also allows the devices to be processed on both the top and bottom of the epitaxial sample while under support. The smoothness constraints on the host substrate are also relaxed since the devices are deposited individually or as an array and not, in contrast to the Bellcore process, as a continuous sheet of material. This alignment and selective deposition also places the relatively expensive compound semiconductor GaAs and InP based devices only where needed, thereby producing an inexpensive integrated system. The thin film epitaxial devices and the host strucutures can be independently optimized and tested, leading to high performance and high yield. This technique also enables the formation of large scale, repairable arrays of devices as well as the integration of thin film compound semiconductor devices with microstructures.

Integration Process Technology

In the first of the two Georgia Tech ELO techniques, the GaAs and InP based device layers (Figure 1a) are defined on the growth substrate using mesa etch processing (Figure 1b). Processing steps such as contact definition can also occur on these mesa defined devices either before or after the mesa etch (Figure 1c). These devices are then coated with Apiezon W (Figure 1d) and, for the GaAs based devices, are exposed to a standard $HF:H_2O$ (1:10) etch solution to separate the epitaxial devices from the growth substrate (Figure 1e). High Al composition layers can be included in the ELO devices, since these layers are protected from the ELO etch solution. The array of mesa defined epitaxial devices is embedded in the surface of the Apiezon W carrier, which is approximately 100 μm thick and can be easily handled. At this point it is not possible to align these ELO devices with respect to features on a host substrate since the Apiezon W is opaque.

To overcome this difficulty, the ELO devices are VDW bonded to a transparent polyimide diaphragm which serves as an alignment and selective deposition transport for the ELO devices (Figure 1f). The polyimide diaphragm is fabricated using standard micromachining techniques. Silicon wafers are coated with approximately 4 μm of polyimide, which is spin-cast from a commercially available polyamic acid solution (DuPont PI-2611), baked at 150 °C in air for 30 minutes, and cured at 400 °C in nitrogen for one hour. The central portion of the wafer is then etched from the backside using a single sided etching technique [9] and 6:1:1 $HF:HNO_3:H_2O$ as the etchant to form a polyimide diaphragm

approximately 4 μm thick and ranging from 3 mm to 25 mm in diameter, supported by a silicon 'ring' at its perimeter. The diaphragm fabricated in this manner is transparent, taut, and mechanically tough, and is ideal as a carrier for the liftoff layers. Mylar transparent diaphragms have also been used at Georgia Tech for this process. The ELO devices on the Apiezon W carrier are then brought into contact with the polyimide, and through VDW bonding, the ELO devices are attached to the polyimide (Figure 1f). The Apiezon W is dissolved with trichloroethylene, leaving the ELO devices bonded to the top of the polyimide. Note that the pre-liftoff processing (for example, contacts) applied to these devices now lies on the top of the ELO devices supported by the polyimide diaphragm. The devices can now be aligned through the transparent diaphragm and selectively deposited to the host structure as shown in Figure 1g.

The second Georgia Tech ELO process utilizes a spun on film of transparent polyimide (DuPont PI-2611) as the handling layer instead of the opaque Apiezon W. The epitaxial devices are mesa etched, the polyimide is spun on, a support ring is placed upon the polyimide before curing, and the polyimide is cured to form the protective handling layer. This assembly is then placed in the HF etch solution to release the epitaxial device. The devices can now be aligned and selectively deposited onto the host structure.

An etch as highly selective etch as that which enables the ELO process in GaAs-based compounds has not yet been identified for InP based compounds. We have demonstrated the formation of thin film epitaxial devices in InP based compounds, namely, InP, InGaAs and InGaAsP, using a slightly different etching sequence. This technique uses a single or a pair of selective etches and etch stop layers to dissolve the substrate, leaving behind the epitaxial layers of interest. An InGaAsP (bandgap of 0.95 eV) etch stop layer is grown lattice matched onto the InP substrate. The epitaxial devices are mesa etched, the handling layer is applied, and the assembly is placed into the HCl etch solution, which selectively etches the InP. The stop etch InGaAsP is subsequently removed with H_2SO_4:H_2O_2:H_2O (1:1:1) if this layer is not part of the functional epitaxial device. The alignment and deposition of these InP based devices then proceeds identically to the GaAs based devices.

Results

Figure 2 is a photomicrograph of InP/InGaAsP/InP pin double heterostructure detectors mounted on a polyimide transfer diaphragm in a top view with illumination through the transparent diaphragm. The dark squares are the thin film devices on the diaphragm. This transparent diaphragm enables the user to align the ELO devices with respect to the host substrate prior to deposition. Current alignment and deposition capability is to within 1 μm. After deposition, the uncontacted side of the ELO devices faces up, and conventional photolithographic and processing techniques can be used to apply contacts to this side of the devices. This process sequence is important, as we have noted some difficulty with processing steps such as contact deposition if these thin ELO samples are not supported by a substrate during deposition.

Since the ELO devices are on the order of 2-3 microns thick, the surface profile of the devices on the host substrate is nearly monolithic, and conventional processing techniques can be used to electrically connect the devices to the host substrate. Figure 3 shows a photomicrograph of a GaAs/GaAlAs light emitting diode (LED) structure which has been mesa etched, preprocessed, lifted off, transferred, deposited onto Si and post processed using

the Georgia Tech ELO technique. This LED structure was patterned into mesas and ohmic contact was deposited while the ELO sample was still on the growth substrate. After lift off and adhesion to the polyimide diaphragm, the devices were adhered to a Si host substrate which had previously been coated with Au. The n-type material, now available on the top of the device, then had an ohmic contact deposited onto it, and a window was opened in the contact using photolithography. The contact was rapid thermal annealed, which also bonded the bottom contact to the Au on the Si host substrate for enhanced adhesion of the ELO device to the host substrate. Figure 3 shows this device emitting infrared light under forward bias, illustrating the successful liftoff, transfer, and electrical contacting of this device.

The alignment and deposition of single thin film devices or arrays of devices can be performed using the Georgia Tech ELO process. To form large (wafer scale) arrays of devices, subarrays of devices can be aligned and deposited to form larger arrays. This eliminates the need for wafer-scale growth uniformity of devices for wafer-scale integration. Figure 4 shows a 4 X 4 array of InP/InGaAsP/InP pin detectors which have been deposited onto gold pads which lie on Si.

For high yield in integrated systems, the ability to repair devices is of paramount importance. The lower right hand element shown in the array in Figure 4 was slightly offset due to a particule which was included during deposition. This defective device was removed, and a new device was aligned and selectively deposited onto that bare pad, as shown in Figure 5. Thus the demonstrated integration technology allows the replacement of defective devices.

Micro-Opto-Mechanical Systems

For applications from sensors to packaging, the combination of optoelectronic devices and microstructures is extremely attractive. The integration tools described herein will prove to be particularly usefuly for the integration of micromechanical structures with thin film GaAs and InP based devices to form micro-opto-mechanical systems (MOMS). The integration of high quality single crystal semiconductor optical devices such as emitters, detectors and modulators directly on top of or into moving microsensors and microactuators is currently limited by the heavy weight and/or large thicknesses of the optical devices. The elimination of the substrate material decreases the weight and thickness of the optical device, thus making them ideal for integration with micromachines. The deposition of these thin film devices results in the monolithic integration of these devices, so standard microfabrication processes are used to connect the devices to the micromechanical device and to adjacent control circuitry. This use of standard processing for interconnect produces high reliability, low cost, manufacturable integrated MOMS.

To demonstrate the utility and manufacturability of MOMS, we are developing the MOMS technology through a variety of test vehicles, including an accelerometer and a fiber optic automated alignment package. Both of these designs are based upon micromachined movable platforms coupled with thin film semiconductor optoelectronic devices. The accelerometer is a self-contained optical Fabry-Perot interferometric acceleration sensor. The thin film optical emitter is integrated directly onto an optically transparent movable platform which responds to acceleration by changing its Fabry-Perot cavity spacing. The highly sensitive interferometric output of this device is detected by an optical sensor integrated in the surface of the silicon underneath the movable platform. Due to the ability to sense small deflections interferometrically, the platform structure can be made very stiff, potentially allowing sensing

bandwidth on the order of 1 MHz. The dynamic range is tuned through the initial position of the platform, which determines the tuning point on the Fabry-Perot curve, thereby setting the platform movement necessary to produce an output.

The fiber optic positioner utilizes a micromachined movable platform to position an emitter or detector with respect to an optical fiber. One such micromachined platform fabricated at Georgia Tech, shown in Figure 6, has the capability to move in three dimensions, thereby aligning the emitter, detector or modulator with respect to the fiber. We have begun our MOMS integration by aligning and depositing a GaAs/GaAlAs double heterostructure detector onto a micromachined platform, shown in Figure 7. An added advantage of this system is the fact that the feedback signal from the fiber to the platform can be processed using circuitry integrated into the silicon substrate upon which the platform in fabricated. This type of inexpensive, automated alignment of optical components with fibers may significantly reduce the packaging cost of optoelectronic components which are fiber coupled.

Conclusions

The integration of high quality thin film GaAs and InP based optoelectronic devices with micromechanical structures expands the functional operation of micromechanical integrated systems into the realm of optical applications, which includes sensors and packaging for photonic interconnect such as optical fibers. Epitaxial lift off processes which utilize a transparent polyimide diaphragm have been developed to realize the alignable, selective deposition of epitaxial GaAs and InP based lift off material onto host structures comprised of materials such as Si, glass, and polymers. This transparent diaphragm can be used to align and selectively deposit the thin film GaAs and InP based devices as individual devices from the array or as an entire array onto the host substrate. The use of the polyimide transfer diaphragm also allows both the bottom and the top of the device to be processed while under substrate support. These thin film devices can be removed if they are defective, and replaced with aligned and deposited replacement devices. This low cost integration technology, which produces thin, light weight devices, is being coupled with micromechanical structures. These micro-opto-mechanical systems will introduce optical functions into microstructures, thereby addressing applications needs from sensors to low cost packaging.

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Figure Captions

Figure 1. Georgia Tech epitaxial lift off process. (a) Starting substrate with grown layers; (b) after mesa etching; (c) after contacting; (d) after Apiezon W application; (e) after selective etch; (f) after adhesion to silicon supported polyimide diaphragm and removal of Apiezon W; (g) after selective deposition onto host substrate. Individual devices or the entire array can be aligned and deposited onto host substrates.

Fig 2: Photograph of an array of 250 um x 250 um x 4 um thick InP/InGaAsP/InP double heterostructure lifted-off devices on a 6 um thick mylar diaphragm. a) top illumination, b) bottom illumination (through the transparent diaphragm).

Figure 3. An epitaxial liftoff LED, emitting radiation, which has been selectively deposited from the polyimide diaphragm onto a Si host substrate.

Figure 4. Four by four array of InP/InGaAsP/InP pin detectors on Si.

Figure 5. Defective device from Figure 4 was removed and replaced with new device aligned and deposited.

Figure 6. Micromachined movable platform onto which a thin film optoelectronic device will be integrated.

Figure 7. GaAs/GaAlAs detector integrated onto a micromachined platform.

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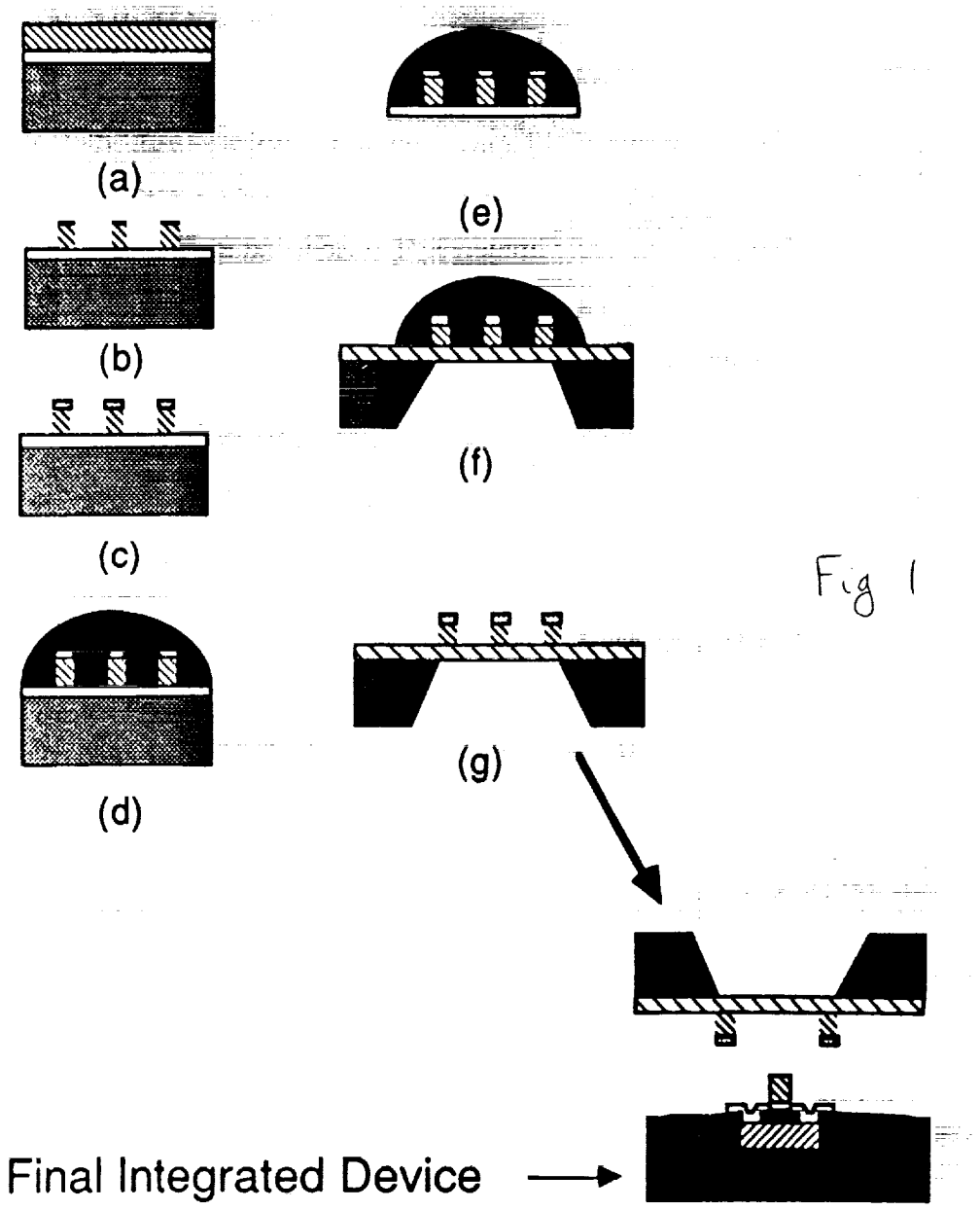

Fig 1

Fig. 1

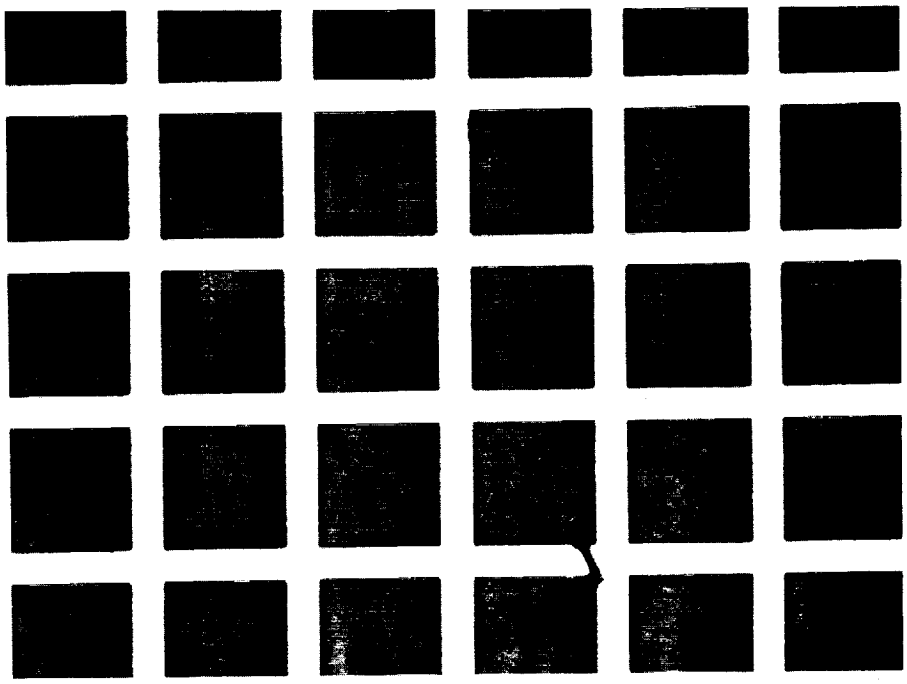

Fig. 2

Fig. 3

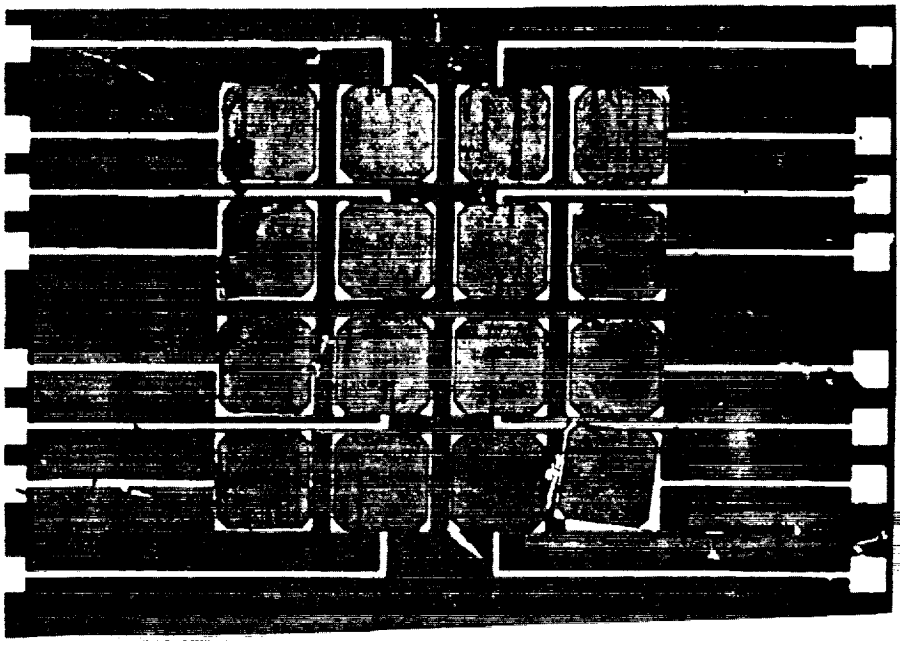

Fig 4

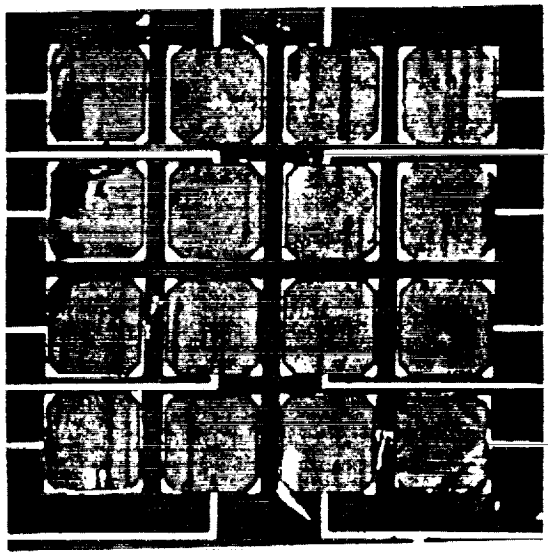

Fig 5.

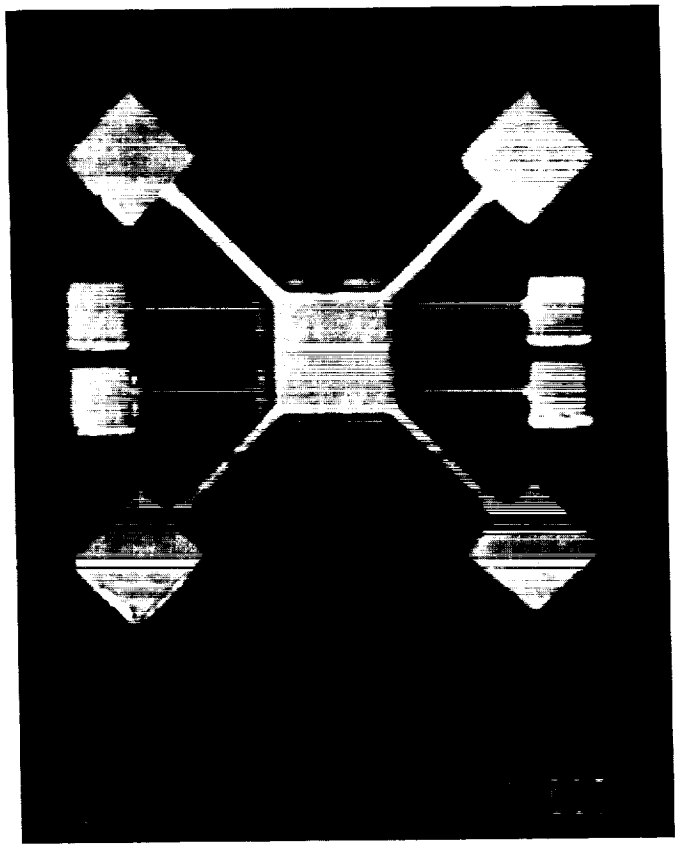

Fig. 6

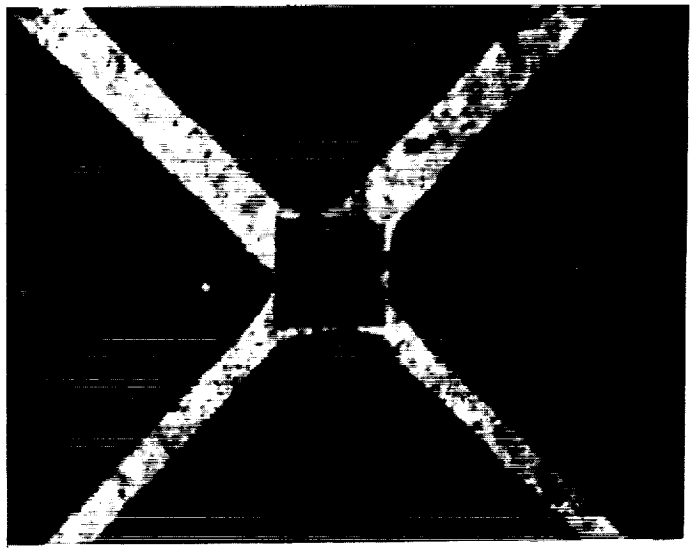

Fig. 7