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Characteristics of III-V Semiconductor Devices at High Temperature

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CHARACTERISTICS OF III-V SEMICONDUCTOR DEVICES AT HIGH TEMPERATURE

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ABSTRACT

This paper presents the development of III-V based pseudomorphic high electron mobility transistors (PHEMTs) designed to operate over the temperature range 77 to 473 K (−196 to 200 °C). These devices have a pseudomorphic undoped InGaAs channel that is sandwiched between an AlGaAs spacer and a buffer layer, gate widths of 200, 400, 1600 and 3200 μm, and a gate length of 2 μm. Measurements were performed at both room temperature and 473 K (200 °C) and show that the drain current decreases by 30 percent, and the gate current increases to about 9 μA (at a reverse bias of −1.5 V) at the higher temperature. These devices have a maximum DC power dissipation of about 4.5 W and a breakdown voltage of about 16 V.

INTRODUCTION

In space borne electronics systems, such as converters, power semiconductor devices are subjected to a wide range of temperatures. The ambient temperature in space, and the large amount of self heating of the devices can produce temperatures as low as 77 K (−196 °C) and as high as 473 K (200 °C) respectively. Since power devices must operate in extreme temperature environments, the material used to fabricate them is critical. Although silicon is a very good material for fabricating power devices, in general, devices fabricated in it suffer from high leakage currents at high temperatures. Also, carrier freeze-out occurs in silicon at temperatures just below that of liquid nitrogen. Silicon carbide (SiC), on the other hand, is an excellent high temperature material. Due particularly to its very wide band gap. Devices fabricated with it have the potential to operate at temperatures as high as 873 K (600 °C). Unfortunately, SiC technology is still very immature. Therefore, working, reliable power devices are not forthcoming. In addition, both 6H and 4H polytype SiC reach carrier freeze-out at temperatures higher than that of silicon. Materials that are well suited for both low and high temperature applications belong to the III-V group. This includes such materials as: gallium arsenide (GaAs), gallium aluminum arsenide (GaAlAs) and indium phosphide (InP). They all have wide band gaps and low carrier freeze-out temperatures. In addition, these materials are part of established technologies, particularly in the case of GaAs.

Recently, the suitability of GaAs device technology for wide temperature range applications has been demonstrated in several studies. One study showed that GaAs MESFET's that have WSi_2 diffusion barriers in the ohmic contacts and Si_3N_4 passivation can withstand temperatures of 573 K (300 °C) for 1000 hr with excellent device characteristic stability (Fricke et al., 1989). Another showed that ion-implanted GaAs MESFET's showed no degradation of the ohmic contacts and the gate metalization, when subjected to an ambient temperature of 398 K (125 °C) for 10 000 hr (Esfandiari et al., 1990). There have also been studies that

have shown how the III-V device characteristics change with temperature. For instance, the study by Shoucair et at (Shoucair et al., 1992) show that when GaAs MESFET's are subjected to temperatures of 673 K (400 °C) they show an increased gate leakage current, a lowered Schottky-barrier height, a lowered sensitivity to sidegating and backgating, a lowered input resistance and an increased drain resistance. Also, thermal models based on experimental results have been developed to predict the DC characteristics (Anholt, 1992; Selmi et al., 1993) and the RF equivalent circuit of GaAs MESFET's (Tellez et al., 1993).

III-V based HEMT structures have also been characterized at high temperatures. GaAs/AlGaAs HEMT's (Fricke, 1992) and AlInP/InGaAs HEMT's (Kuo, et al., 1993) have been shown to operate satisfactorily up to 473 K (200 °C). AlGaAs/InGaAs pseudomorphic HEMT's (PHEMT's) have shown an increase in f_T when cooled from room temperature to 77 K (−196 °C) and a decrease in f_T when heated from room temperature to 463 K (190 °C) (Mizutani et al., 1992). This paper presents the I-V characteristics, gate leakage current and breakdown voltage of an AlGaAs/InGaAs pseudomorphic HEMT with a delta doped donor layer at 473 K (200 °C).

DEVICE STRUCTURE AND FABRICATION

PHEMT devices were fabricated on a structure grown epitaxially by MBE on a semi-insulating GaAs wafer (Quantum Epitaxial Designs, Inc.). The structure included: a highly doped top layer of GaAs (350 Å) for fabricating ohmic contact, an undoped $Al_{0.23}Ga_{0.77}As$ layer (325 Å), a silicon delta doping spike (3.5×10^{12} cm^{-2}), an undoped $Al_{0.23}Ga_{0.77}As$ spacer layer (50 Å), a pseudomorphic undoped $In_{0.20}Ga_{0.80}As$ channel (150 Å) all on top of undoped GaAs and $Al_{0.23}$ $Ga_{0.77}As$/GaAs superlattice buffer (0.8 μm). Because GaAs has very poor thermal conductivity, a thin AlAs (500 Å) peel-off layer was added just below the buffer. This will enable the removal of the active structure so that it can be mounted on a suitable heat sink material such as diamond. This procedure will be performed at a future date. Figure 1 shows the pseudomorphic HEMT structure. Four different devices were fabricated on this structure, containing gate widths of 200, 400, 1600 and 3200 μm. The gate length of all the devices was 2 μm and the gate metalization used a platinum barrier to inhibit gold migration into the channel (Ti/Pt/Au: 500 Å/300 Å/2000 Å). The source and drain contacts were made of nickel/germanium/nickel/indium/nickel/tungsten (50 Å/50 Å/50 Å/50 Å/50 Å/500 Å) to eliminate the formation of the gold/arsenic compounds which tend to decrease contact resistivity at high temperatures. The gate-to-source separation was made small (2 μm) to reduce the source series resistance and improve the DC switching capability. The gate-to-drain separation was made large (10 μm) to increase the breakdown voltage and therefore, the output power of the devices.

EXPERIMENTAL RESULTS

The four devices were tested at room temperature, 373 K (100 °C) and 473 K (200 °C). There was no degradation in either the Schottky or the ohmic metalizations. The ohmic contacts had a high contact resistivity of about 10^{-5} Ω-cm^2. The maximum DC power dissipated in the devices was about 4.5 W. The average break-down voltage of the devices was found to be approximately 16 V. Figure 2 shows the gate leakage current with temperature as a parameter measured using a Sony/Tektronix Model 370A Programmable curve tracer. The gate leakage current at 473 K (200 °C) and at a reverse bias of −1.5 V is about 9 μA. Figure 3 shows the measured DC drain current as a function of the drain-to-source voltage of the PHEMT for several gate widths at 473 K (200 °C). The drain current decreases by about 30 percent at 473 K (200 °C) when compared to room temperature measurements.

The pinch-off voltage (V_p) generally increases with temperature. The V_p for the device with a gate width of 400 μm was −2.01 V at room temperature. At 473 K (200 °C) V_p was about −2.768 V.

CONCLUSIONS

The I-V characteristics of an AlGaAs/InGaAs pseudomorphic HEMT with a delta doped donor layer were measured at 473 K (200 °C). There was no degradation in either the Schottky or the ohmic metalizations at 473 K (200 °C). However, for lower contact resistance, an optimization of the refractory based contacts should be done. We expect these devices to operate at temperature higher than 473 K (200 °C). However, these devices have to be recharacterized for their new I-V characteristics before circuits can be built around them.

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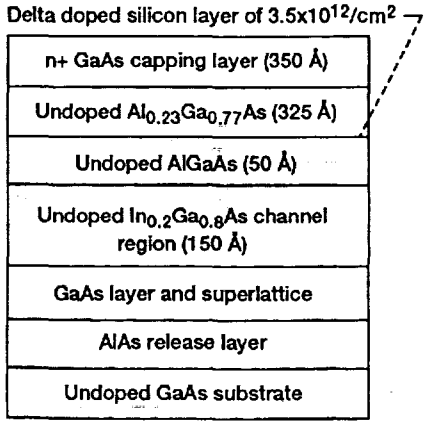

Figure 1.—Pseudomorphic HEMT structure with $In_{0.2}$ $Ga_{0.8}As$ channel and delta-doped $Al_{0.23}Ga_{0.77}As$ barrier.

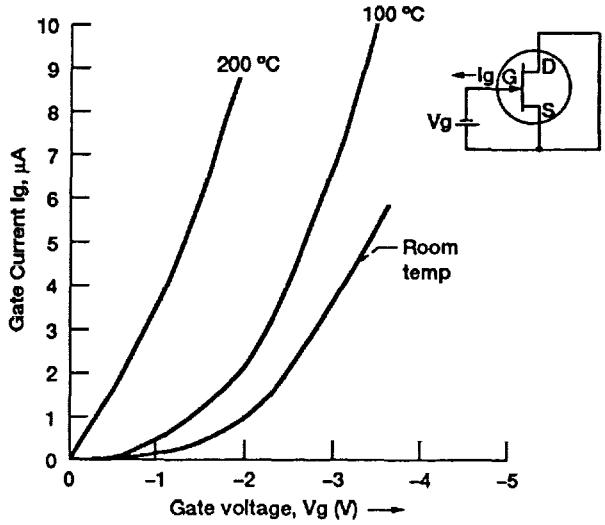

Figure 2.—Gate leakage current with temperature as a parameter.

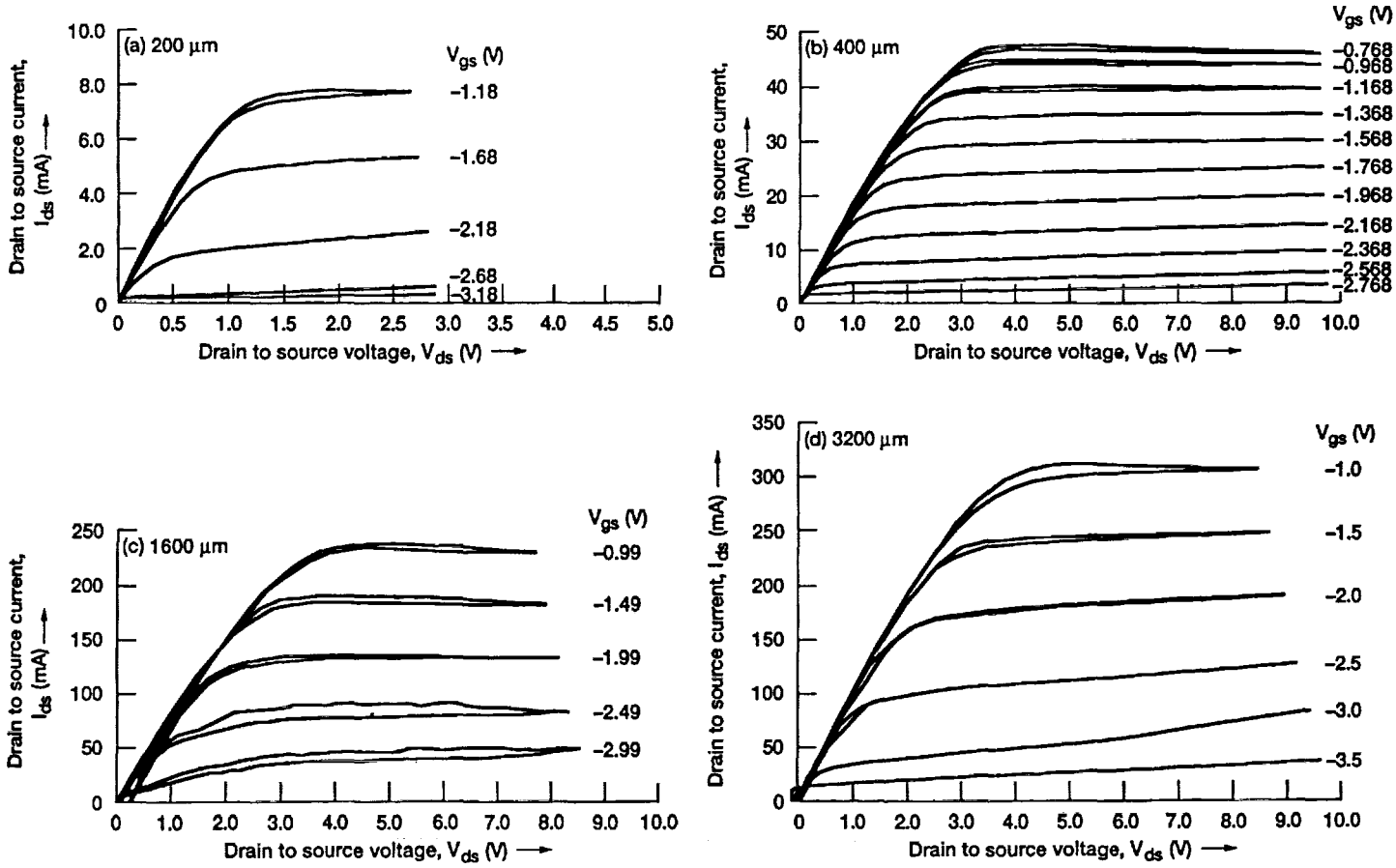

Figure 3.—Drain characteristics of the PHEMT at 200 °C for several gate widths.

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13. ABSTRACT (*Maximum 200 words*)

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