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Ku-BAND HIGH EFFICIENCY GaAs MMIC POWER AMPLIFIERS

H. Q. Tserng,

Texas Instruments Incorporated
Central Research Laboratories
P. O. Box 655936
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Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

NASA/Lewis Research Center
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Ku-BAND HIGH EFFICIENCY GaAs MMIC POWER AMPLIFIERS

I. SUMMARY

This interim report covers the first 12 months of a 30-month contract for the development of Ku-band high efficiency GaAs MMIC power amplifiers. The objective of this program is to develop high efficiency, high power, high gain, wide bandwidth monolithic GaAs amplifiers for future NASA space communications applications. Specifically, three amplifier modules operating over the 13 to 15 GHz frequency range are to be developed. The first MMIC is a 1 W variable power amplifier (VPA) with high efficiency over a wide range of output power levels. On-chip digital gain control is to be provided. The second MMIC is a medium power amplifier (MPA) with an output power goal of 1 W (at saturation) and 40% power-added efficiency. The third MMIC is a high power amlifier (HPA) with 4 W output power goal (at saturation) and 40% power-added efficiency. The gains are to be equal to or greater than 15 dB over the design bandwidth. In addition to the baseline GaAs MESFET amplifiers, amplifiers using advanced heterostructure devices such as AlGaAs/GaAs heterojunction MESFETs and AlGaAs/GaAs heterojunction MISFETs are also to be fabricated and tested.

Discrete single-gate MESFETs were fabricated on MOCVD, MBE, and ion-implanted wafers for Ku-band optimization. An output power of 0.7 W/mm with 40% efficiency, 0.5 W/mm with 39% efficiency, and 0.36 W/mm with 49% efficiency has been obtained on MOCVD, MBE, and ion implanted material. Low value I_{dss} (low pinchoff) devices have demonstrated best efficiencies with little sacrifice in output power.

A mask set containing one-stage, two-stage, and three-stage amplifiers (MPA and HPA) was designed and fabricated. The measured small signal performance of these amplifiers is extremely close to predicted values. A single-stage 600 μm amplifier with an efficiency of 40% and 0.4 W/mm output power was obtained.

A four-stage dual-gate variable power amplifier was modified to operate at Ku-band frequencies. An output power of 500 mW with 20 dB gain was

measured at 17 GHz. A dual gate FET scribed from the amplifier was capable of an output power of 0.42 W/mm with 27% efficiency.

A four-bit digital-to-analog converter was designed and fabricated. Sixteen states with a -3 V to +1 V swing were obtained.

II. INTRODUCTION

This interim report covers the first 12 months of a 30-month contract for the development of Ku-band high efficiency GaAs MMIC power amplifiers. The objective of this program is to develop high efficiency, high power, high gain, wide bandwidth monolithic GaAs amplifiers for future NASA space communications applications. Specifically, three amplifier modules operating over the 13 to 15 GHz frequency range are to be developed. The first MMIC is a 1 W variable power amplifier (VPA) with high efficiency over a wide range of output power levels. On-chip digital gain control is to be provided. The second MMIC is a medium power amplifier (MPA) with an output power goal of 1 W (at saturation) and 40% power-added efficiency. The third MMIC is a high power amplifier (HPA) with 4 W output power goal (at saturation) and 40% power-added efficiency. The gains are to be equal to or greater than 15 dB over the design bandwidth. In addition to the baseline GaAs MESFET amplifiers, amplifiers using advanced heterostructure devices such as AlGaAs/GaAs heterojunction MESFETs and AlGaAs/GaAs heterojunction MISFETs are also to be fabricated and tested.

The optimization of channel structures of single- and dual-gate FETs is discussed in Section III. At 15 GHz a power-added efficiency as high as 56% was demonstrated using FETs with gate lengths of 0.25 μm. A 1200 μm gate width FET has achieved a power density of 0.7 W/mm with 40% efficiency at 15 GHz. The amplifier module development is described in Section IV. A mask set containing various multistage MMIC amplifiers for the MPA and HPA was designed and fabricated. Single-stage amplifiers with power-added efficiencies of up to 40% were demonstrated. Technical achievements during this report period are summarized in Section V. Plans for the remaining contract period are given in Section VI.

III. DEVICE OPTIMIZATION

A. Single-Gate FET

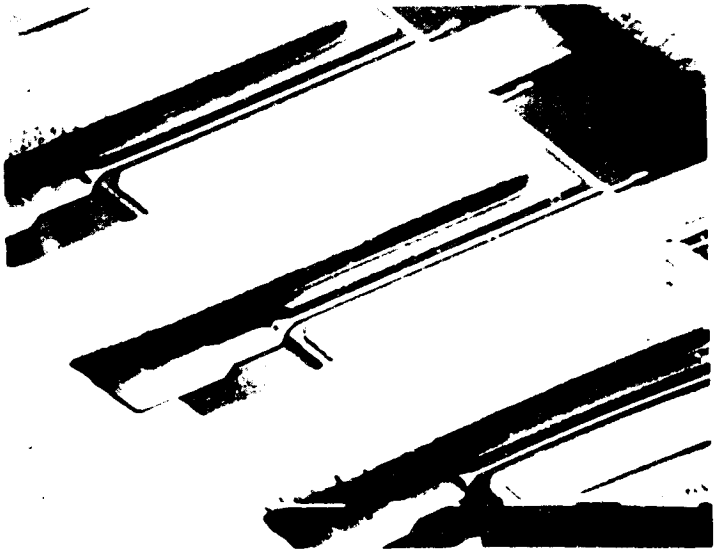
Discrete 1200 μm FETs with the source-overlay structure were chosen for Ku-band FET optimization. These FETs have the source fingers air-bridged over the gates to via grounding pads. Figure 1 is a photograph of a 1200 μm FET. A unit finger width of 60 μm and a source/drain spacing of 3 μm were used. This is the same type of FET used at higher frequencies (20 GHz).

Material and gate channel structure were the two variables chosen for optimization to achieve maximum FET performance at Ku-band. A goal of 0.7 W/mm with 50% efficiency from a discrete FET was set to meet the high power amplifier specifications, and a goal of 0.5 W/mm with 50% efficiency was set to meet the medium power amplifier specifications. Material optimization included investigating MOCVD, MBE, and ion implant material with varying doping densities. Channel structure optimization included varying the wide and narrow recesses of the FET channels.

Initially, we had difficulties fabricating the double recess structure shown in Figure 2. The etch undercut the resist for the wide recess, leaving the recess excessively large. Experiments showed that too large a wide recess degrades rf performance, and these FETs would generate little power (< 0.2 W/mm).

Two devices, one with high power density (167-24) and one with low power density (167-23) were characterized by S-parameter measurements over the frequency range from 1 to 26 GHz. The S-parameters were deembedded using the through-short-delay (TSD) method. The element values of the equivalent circuit shown in Figure 3 were then fitted to the measured data using the SUPER-COMPACT program. Table 1 shows the values obtained for the equivalent circuits of the two devices. In general, the fit was excellent over the frequency range from 1 to 26 GHz.

(a)



(b)

Figure 1. SEM photographs of 1200 μm gate width FET with source overlay grounding.

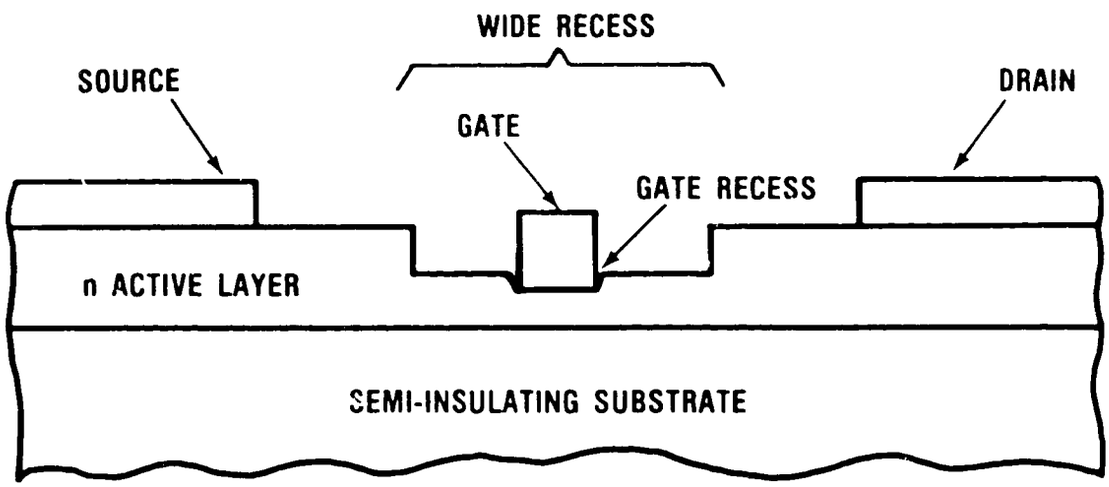


Figure 2. FET channel structure.

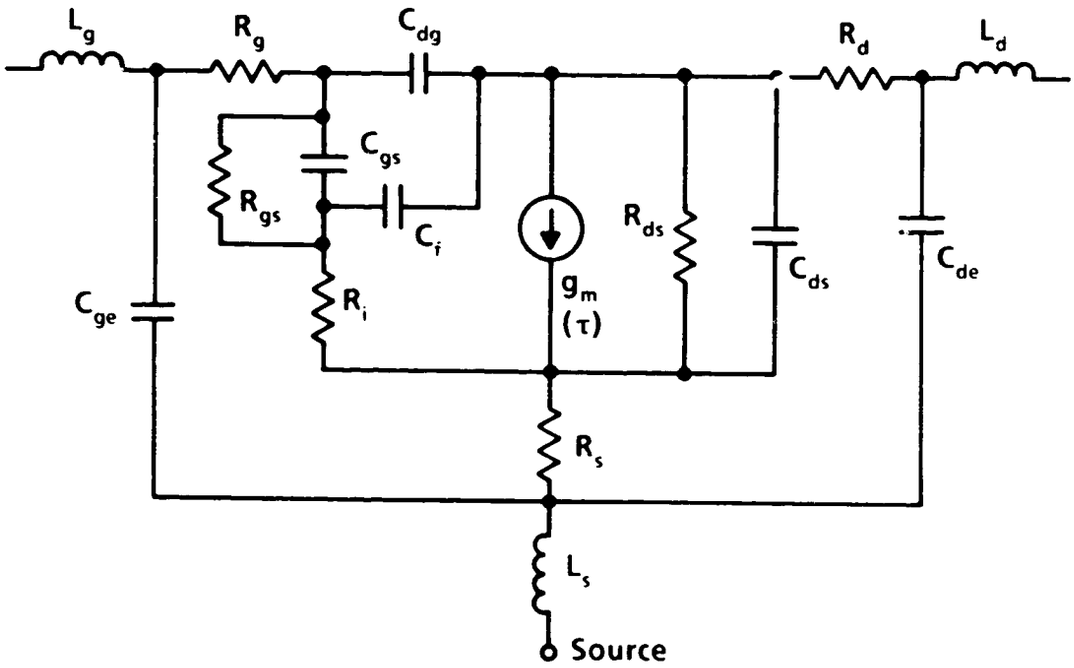


Figure 3. FET equivalent circuit model.

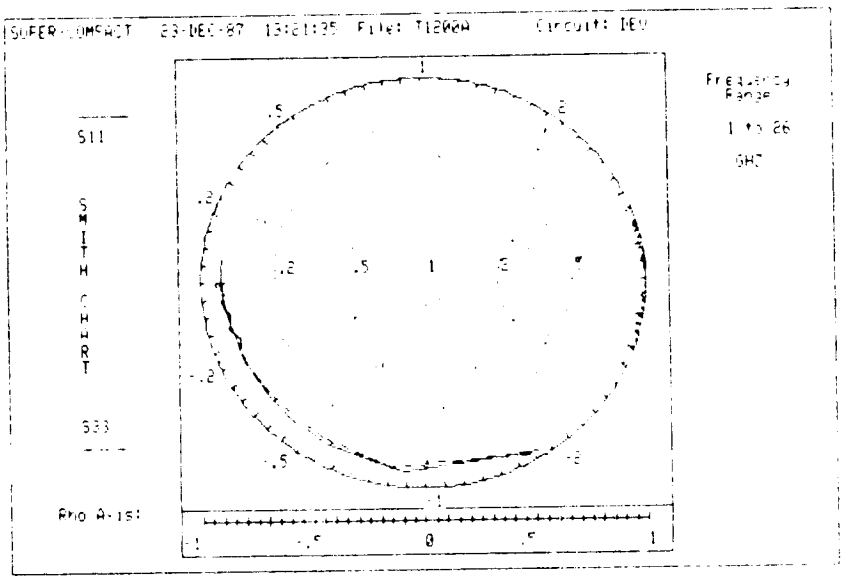
Table 1. Modeled Element Values of 1200 μm FETs

Parameter	Device 167-23	Device 167-24
R_g (ohms)	0.67	0.65
R_i (ohms)	0.91	0.93
C_{gs} (pF)	1.59	2.03
C_{dg} (pF)	0.060	0.077
C_f (pF)	0.020	0.022
g_m (mS)	98	168
T_d (ps)	7.3	4.4
R_s (ohms)	1.00	0.96
R_{ds} (ohms)	272	136
C_{ds} (pF)	0.17	0.30
R_d (ohms)	-3	0.98
L_s (nH)	0.015	0.012
L_g (nH)	0.029	0.059
L_d (nH)	0.036	0.075
C_{ge} (pF)	0.031	0.031
C_{de} (pF)	0.033	0.032
f_t (GHz)	9.8	13.4

Figures 4(a)-(c) and 5(a)-(c) compare the measured and modeled S-parameters of thc two FETs. To plot the modeled and measured S-parameters on the same graph, the two sets of S-parameters were constructed as unconnected four-port in the SUPER-COMPACT input file. The port 3 (input) and port 4 (output) are identified as the two-port with the measured S-parameters. These results indicate that the fixture design and the deembedding scheme work well in the measured frequency range. Table 1 shows that the two devices differ in transconductance (g_m), delay time (T_d), drain-source capacitance (C_{ds}), and drain resistance (R_d). It should be noted that device 167-23 needs a negative drain resistance of 3 ohms for the S_{22} to fit well at high frequencies. Examination of the stability factors shows that the device with poor large-signal performance (167-23) has a very strong tendency to oscillate (with stability factor less than 1). The poor power performance is attributed to a nonoptimum wide recess with a gradual slope. We know from past experience that the gate recess shape is critical to obtaining good output power. From this modeling effort we have been able to determine the effects of process variations on equivalent circuit element values. A nonoptimum recess coupled with the particular channel doping level and the active layer thickness under the gate can result in Gunn-type instability, which will degrade the FET power performance.

The e-beam exposure was adjusted so that no undercutting of the resist was visible. Figure 6 is SEM photograph of a properly exposed double-recess channel structure.

Table 2 lists the best performance of 1200 μm FETs fabricated on MBE, MOCVD, and ion implant wafers. The dopings were approximately 2×10^{17} cm^{-3}, and the gate length was 0.4 μm. The best performance was obtained from an MOCVD wafer with AlGaAs buffer. An output power of 0.8 W/mm with 35% efficiency and 3.8 dB gain was achieved. When this device was tuned for maximum efficiency, it achieved an efficiency of 40% with 5.2 dB gain and 0.72 W/mm power. The MBE and ion implanted wafers had similar efficiencies, but lower output powers. MOCVD wafers with standard GaAs buffers performed poorly. Figures 7 through 9 show saturation responses of the MBE and MOCVD devices.



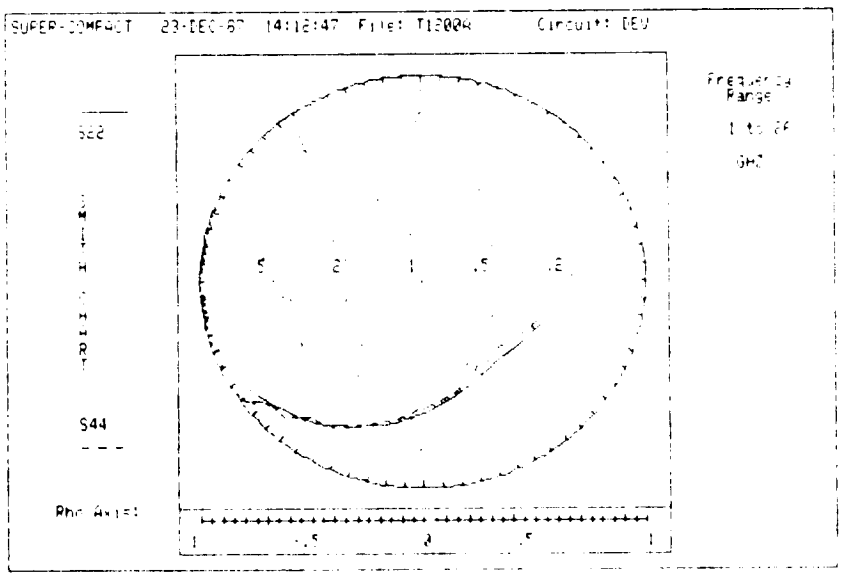


Figure 4(a). S_{11} and S_{22} of Device 167-23.

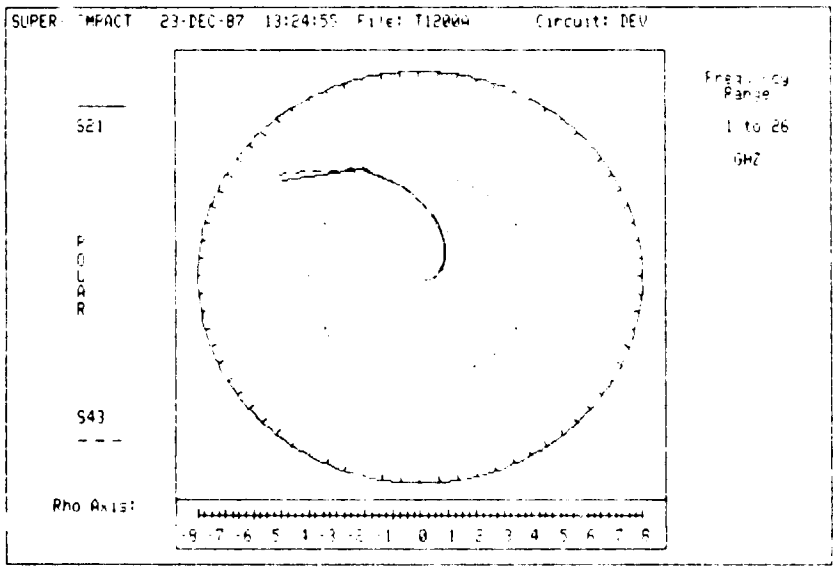
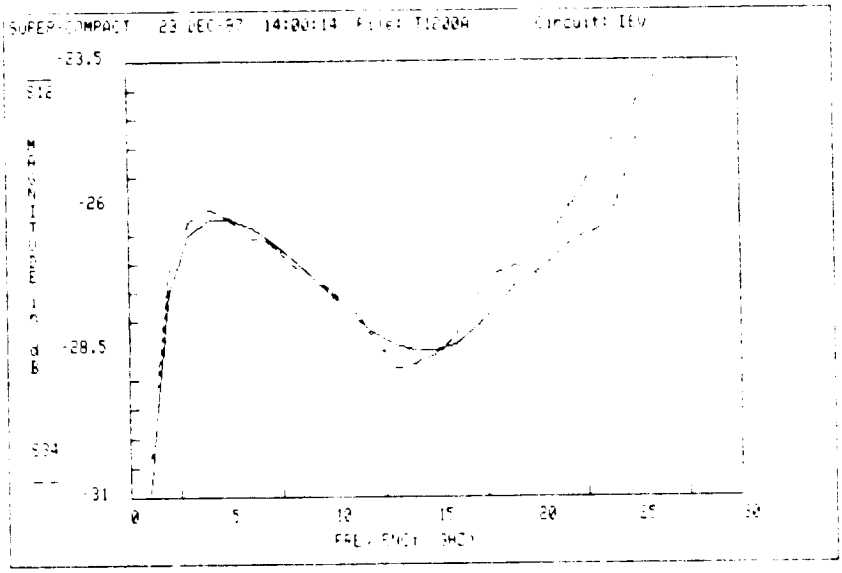


Figure 4(b). S_{21} of Device 167-23.



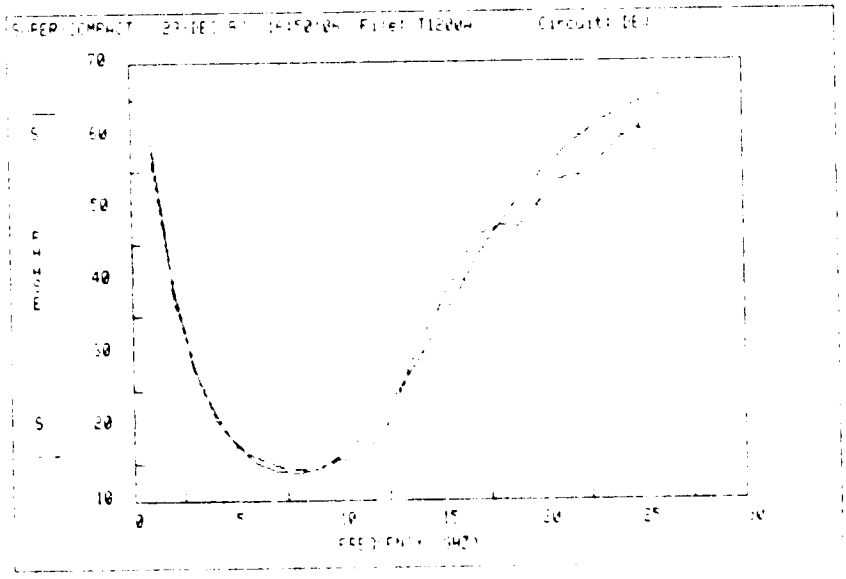
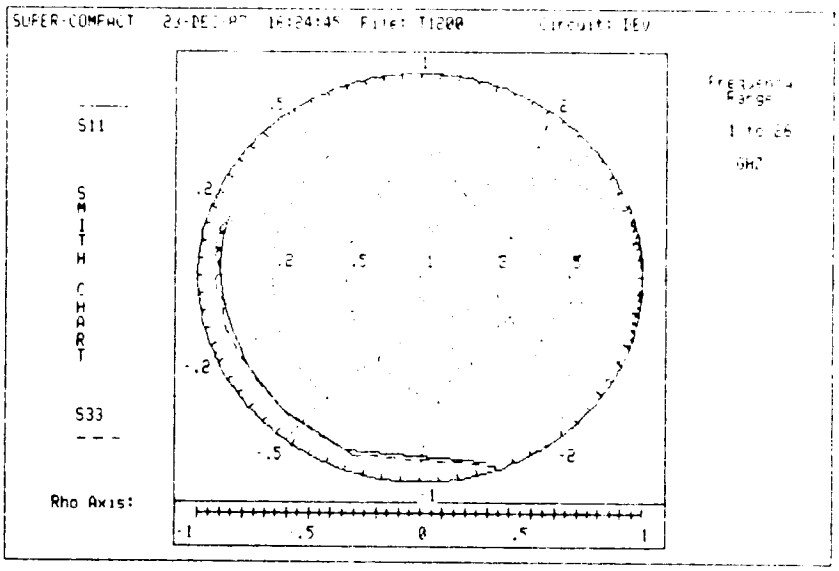


Figure 4(c). S_{12} of Device 167-23.



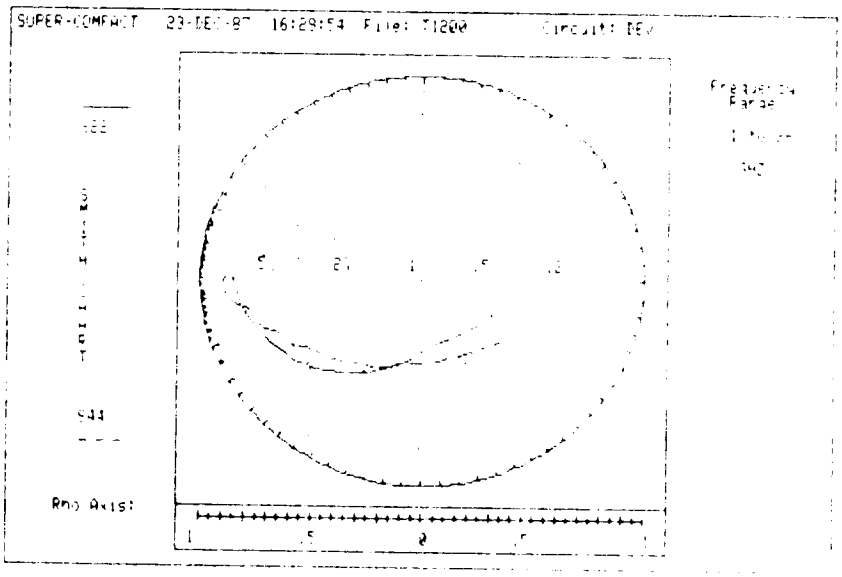


Figure 5(a). S_{11} and S_{22} of Device 167-24.

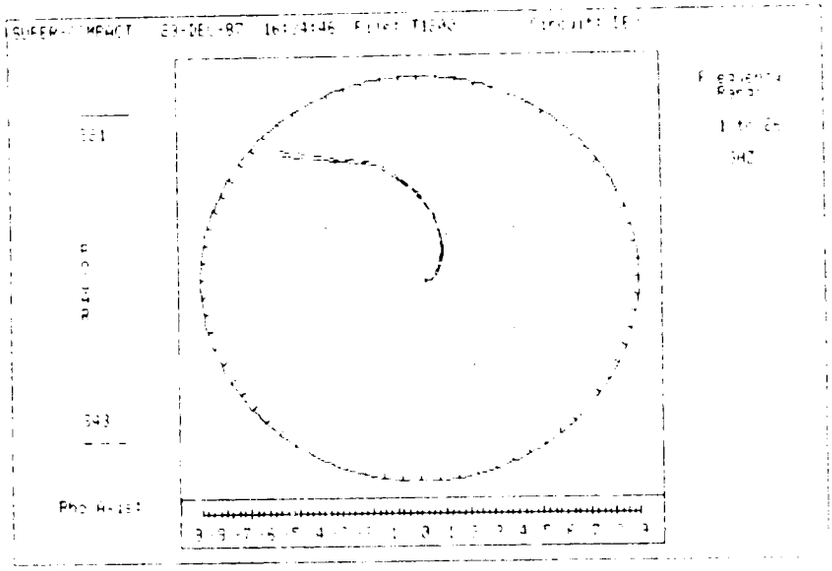
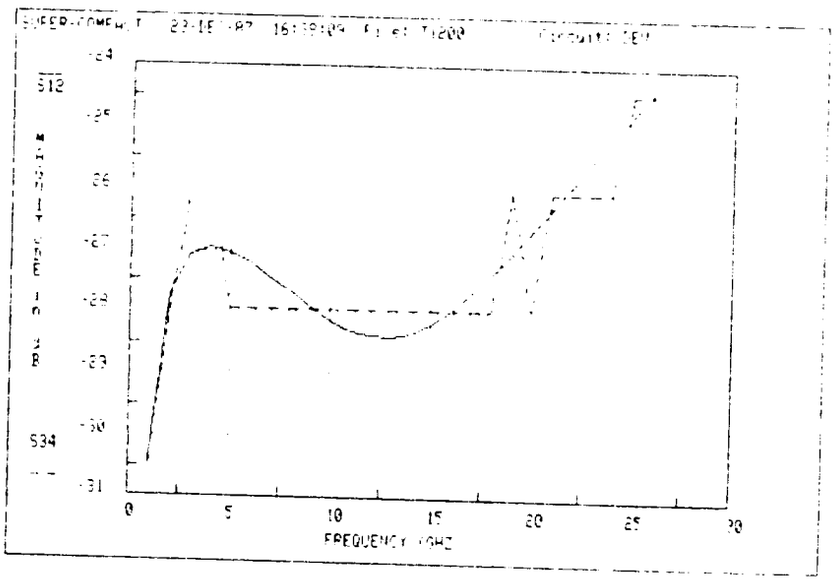


Figure 5(b). S_{21} of Device 167-24.



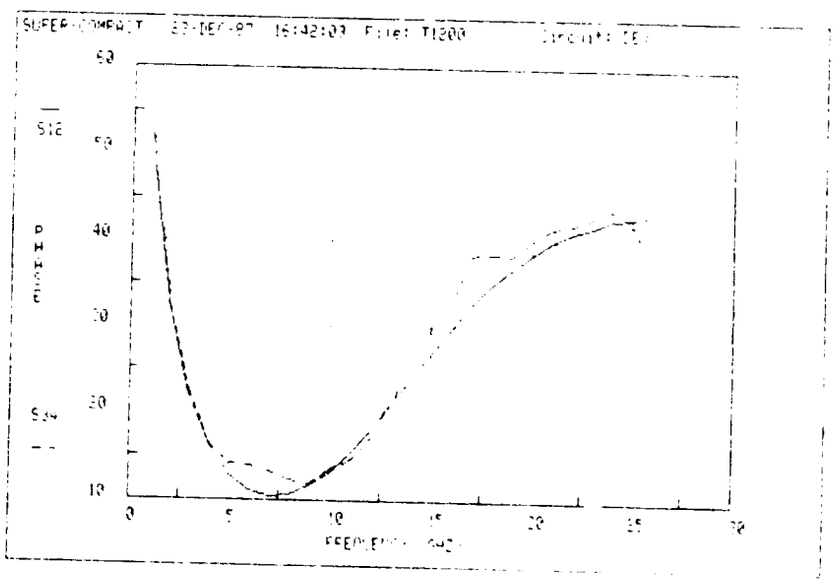


Figure 5(c). S_{12} of Device 167-24.

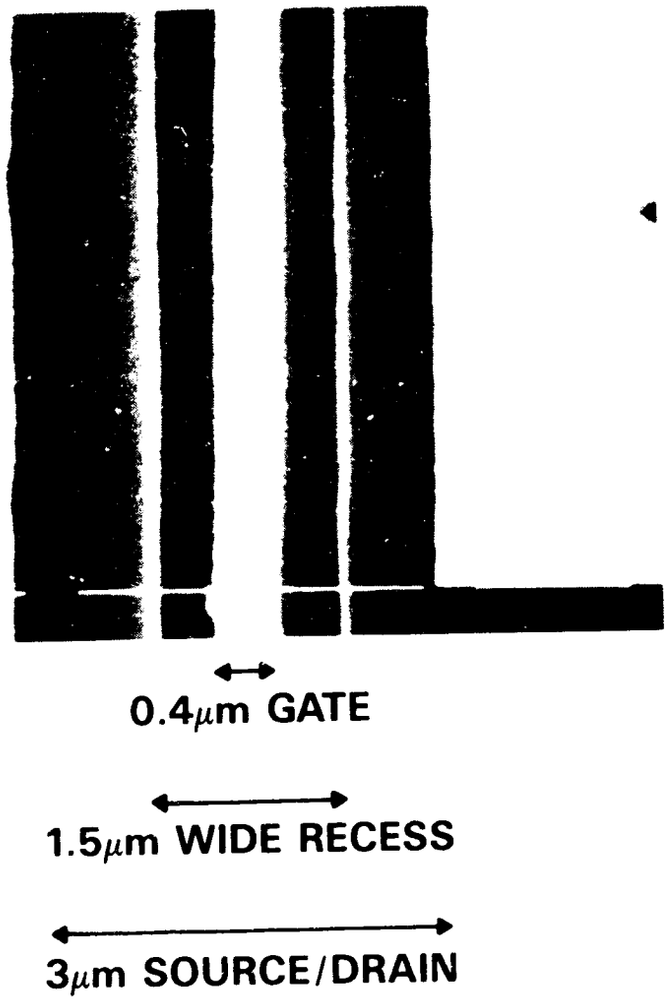


Figure 6. Single-gate channel structure.

Table 2. 1200 μm FET Performance

	MBE	MOCVD (AlGaAs)	MOCVD	Implant
Doping	2.5×10^{17}	2.0×10^{17}	2.0×10^{17}	2.0×10^{17}
Small Signal Gain	7.3 dB	8 dB	8 dB	10.3 dB
Maximum Power Efficiency Gain	0.6 W/mm 29% 3.5 dB	0.8 W/mm 35% 3.8 dB	0.37 W/mm 15% 3.3 dB	0.42 W/mm 34% 6.9 dB
Power Maximum Efficiency Gain	0.5 W/mm 39% 5 dB	0.72 W/mm 40% 5.2 dB	-- -- --	0.36 W/mm 49% 6.3 dB

Table 3. 800 μm x 0.25 μm MESFET

Doping	3.5×10^{17}
Small Signal Gain	7.6 dB
Maximum Power Efficiency Gain	0.38 W/mm 56% 6.9 dB

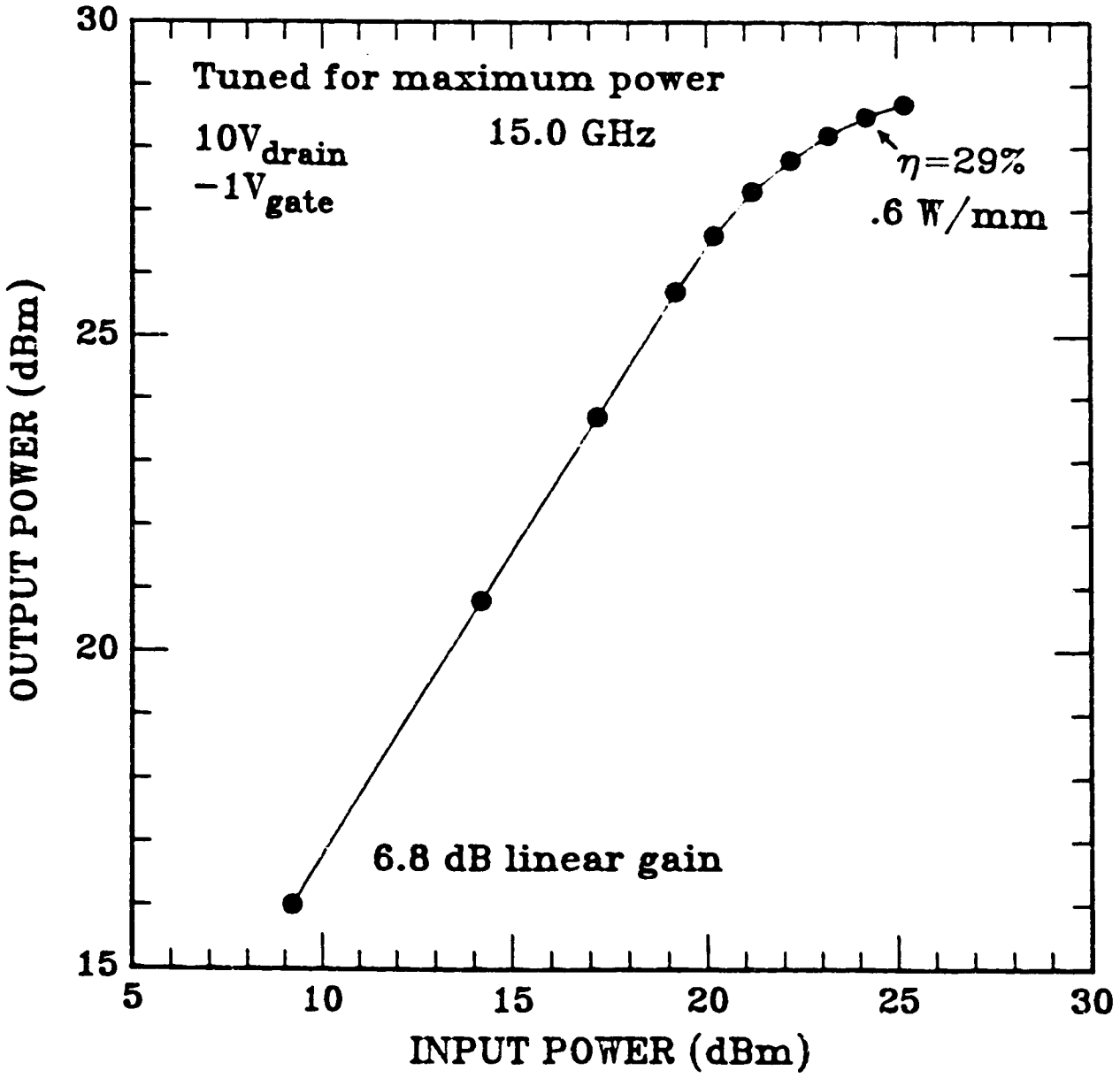


Figure 7. 1200 μm MBE FET tuned for maximum power.

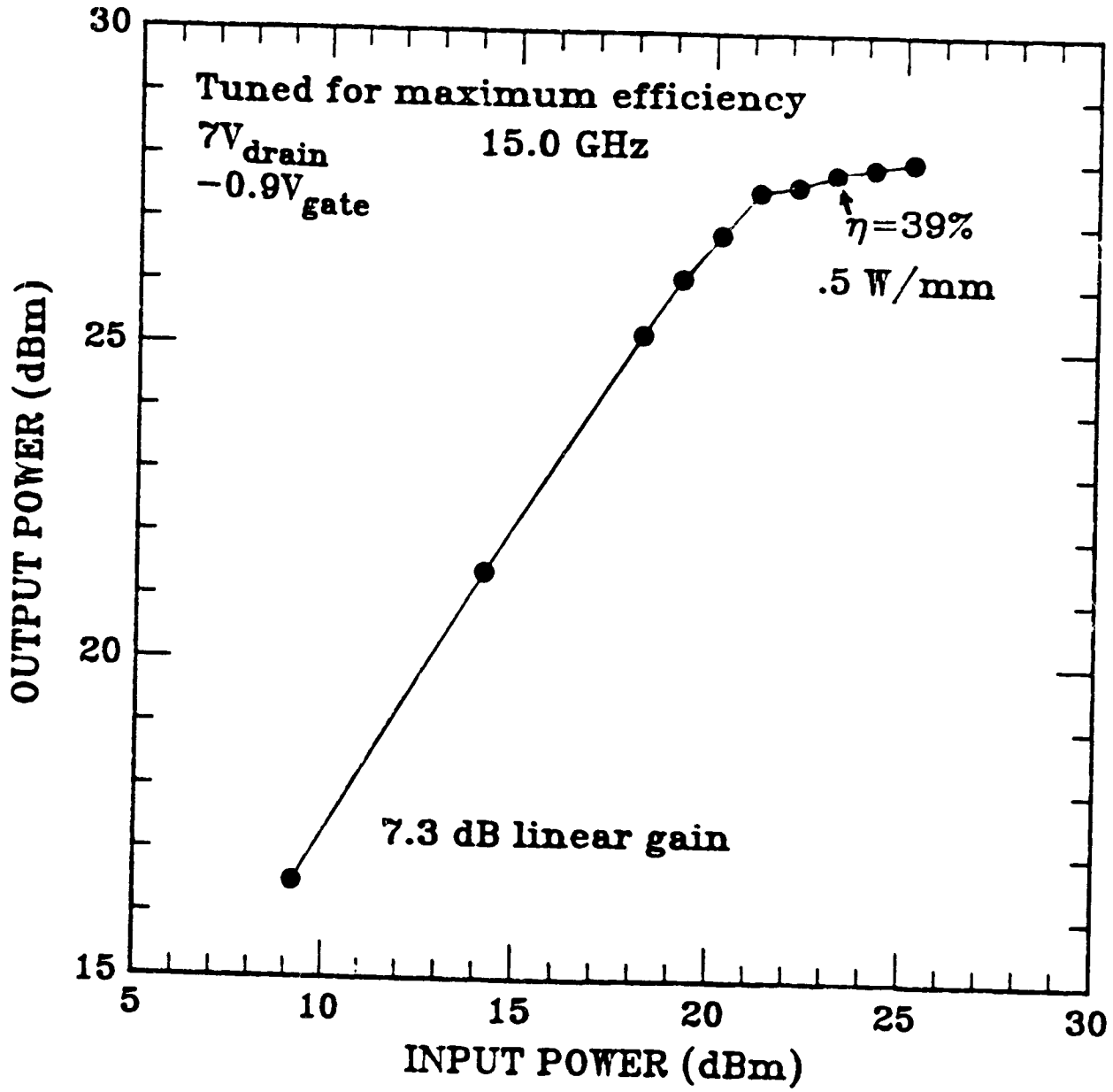


Figure 8. 1200 μm MBE FET tuned for maximum efficiency.

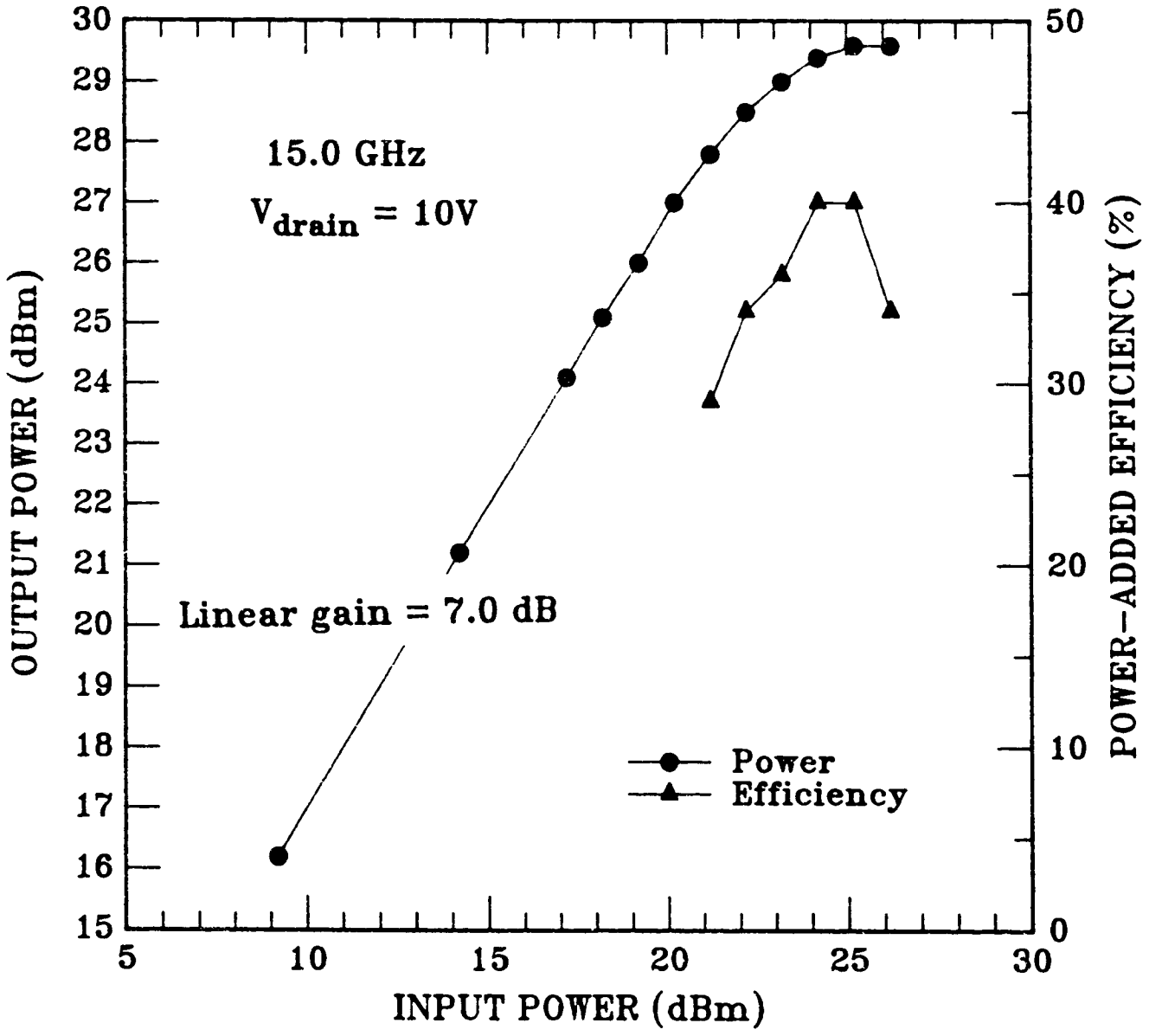


Figure 9. 1200 μm MOCVD with AlGaAs FET.

On another program a 0.25 μm FET with higher doping was tested at Ku-band. The results are shown in Table 3. An efficiency of 56% was obtained with 0.38 W/mm. The saturation response is plotted in Figure 10.

The I_{dss} varied considerably across an ion implanted wafer. This enabled us to correlate rf performance with I_{dss}. The low I_{dss} devices had pinch-off voltages near 2 V, and the high I_{dss} devices had pinch-off voltages near 5 V. Table 4 summarizes the performance of discrete 600 μm and 1200 μm FETs tuned for maximum power and for maximum efficiency. Maximum power-added efficiencies have a direct correlation on I_{dss}: the lower the current, the higher the efficiency. The increase in efficiency is at only a small expense of lower output power. An efficiency of 49% with an output power of 0.36 W/mm was obtained from a 1200 μm FET, and an efficiency of 40% with an output power of 0.41 W/mm was obtained from a 600 μm FET at low I_{dss}. Efficiencies decreased to 30% at high I_{dss}.

MOCVD wafers occasionally had leaky buffers, and the results with AlGaAs buffers were not reproducible. Since etching vias in wafers with thick AlGaAs buffers also presented problems, we discontinued work on MOCVD material. Work is continuing on MBE and ion implant material optimization, particularly at higher dopings.

B. Dual-Gate FETs

The dual-gate FETs used for this program were initially identical to those used on the NASA 20 GHz variable power amplifier program (Contract No. NAS3-22886). These FETs have an integrated second-gate capacitive termination. However, 300 μm gate width devices showed a resonance behavior that caused reduced gain at lower Ku-band frequencies.

The dual gate FETs used for the Ku-band four-stage variable power amplifier were subsequently modified from the NASA 20 GHz variable power amplifier design. The source/drain spacing was reduced from 7.5 μm to 5 μm, and the active area under the gate feed was removed. Figure 11 is a SEM of the dual gate FET with the two changes. Figure 12 is an enlarged view of the gate area. The gates are 0.3 μm long.

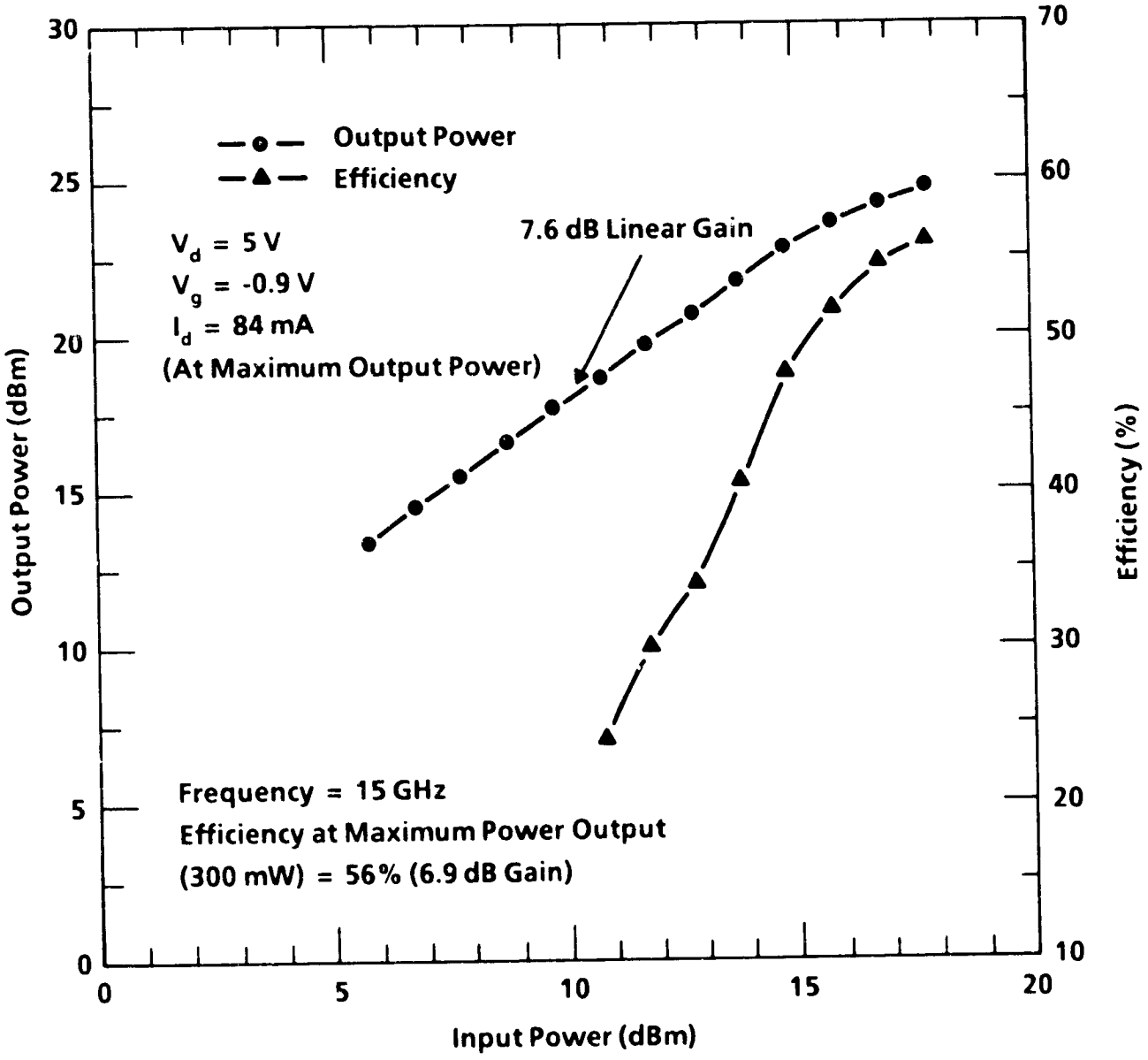


Figure 10. Performance of 800 μm x 0.25 μm GaAs MESFET.

Table 4. Performance of 600 μm and 1200 μm FETs with Varying I_{dss}

I_{dss}/ Device Size	Small Signal Gain (dB)	Maximum Power (W/mm)	Associated Gain (dB)	Associated Efficiency (%)	Maximum Efficiency (%)	Associated Gain (dB)	Associated Power (W/mm)
110 mA/600 μm	10.1	0.43	7.0	33	40	6.8	0.41
180 mA/600 μm	10.7	0.49	6.5	24	33	6.0	0.43
190 mA/600 μm	12.0	0.51	7.8	21	28	6.0	0.42
220 mA/600 μm	11.0	0.62	8.6	24	30	6.0	0.43
200 mA/1200 μm	10.3	0.42	6.9	34	49	6.3	0.36
250 mA/1200 μm	10.9	0.37	7.4	39	39	7.4	0.37
280 mA/1200 μm	9.2	0.35	6.2	29	37	5.6	0.31
310 mA/1200 μm	10.0	0.44	7.1	25	28	6.4	0.37

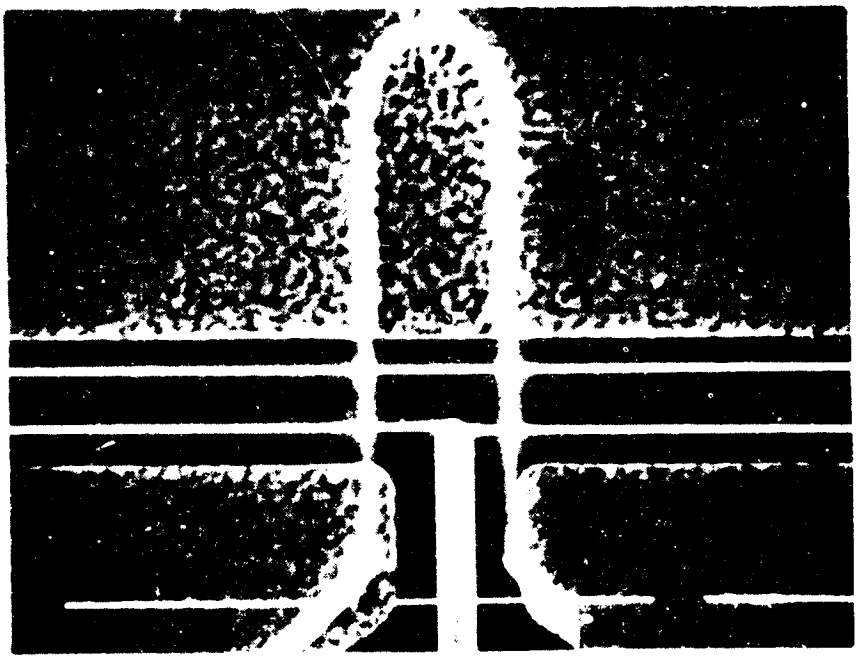


Figure 11. New mesa and source/drain levels for VPA.

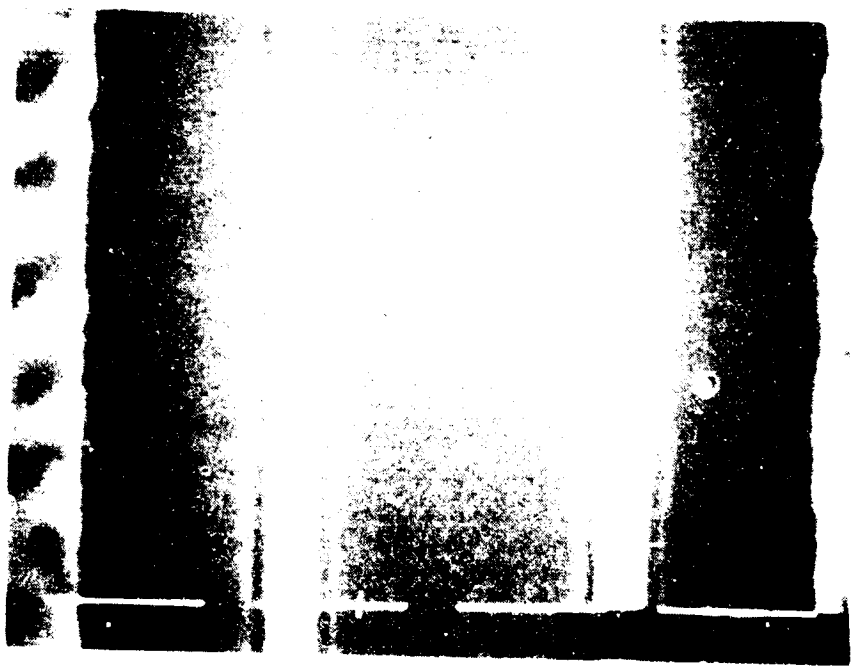


Figure 12. 0.3 μm dual gates in a 5 μm source-drain spacing.

The f_T of the dual gate FETs improved from 10 GHz to 18 GHz with these modifications. Figure 13 is a power saturation curve of a discrete 300 μm dual gate FET. An output power of 0.42 W/mm with an efficiency of 27% was obtained.

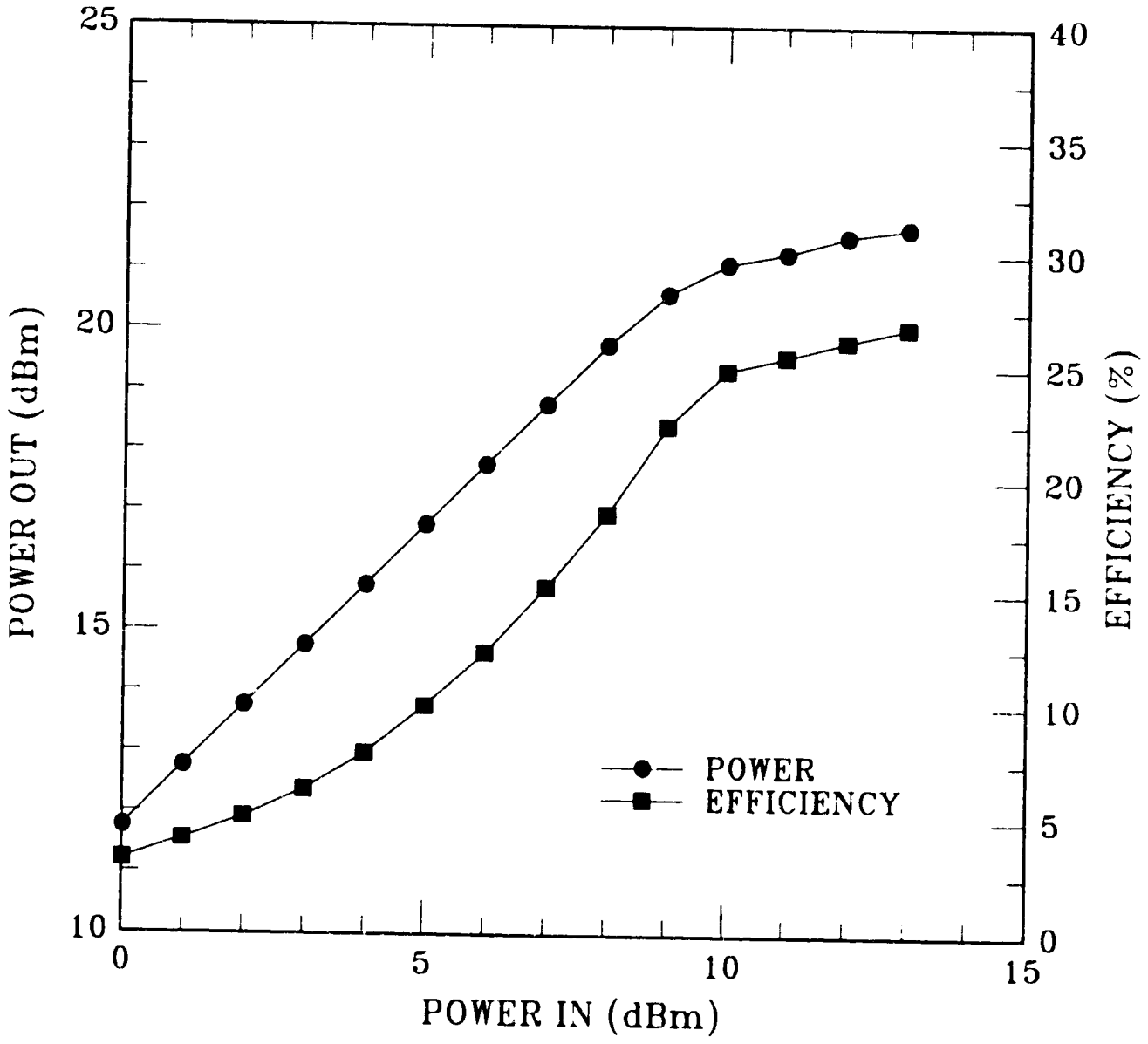


Figure 13. Power saturation curve of a 300 μm dual-gate FET.

IV. AMPLIFIER MODULE DEVELOPMENT

A. Single-Gate FET Amplifiers (MPA, HPA)

The medium-power amplifier (MPA) and the high-power amplifier (HPA) are of a low-pass circuit topology similar to that used in the design of the 2.5 W module (developed under Contract No. NAS3-23781) shifted to the 13 to 15 GHz frequency range. For the 1 W MPA, FETs with gate widths of 0.6 mm, 1.2 mm, and 2.4 mm were cascaded; for the HPA, FETs with 1.2 mm, 2.4 mm, and 6.0 mm gate widths were cascaded. To further aid in the development of the amplifiers, single-stage amplifier circuits were designed around the 0.6 mm and 1.2 mm FETs, and a two-stage 1.2 mm to 2.4 mm FET amplifier was included The designs were created utilizing a device model based on measurements of FETs of similar size produced in the past, and the circuit topology realized in microstrip on GaAs was modeled using SUPER-COMPACT. Figure 14 shows the circuit topology of the amplifiers, and Figure 15 shows their predicted microwave performance.

The three-stage, two-stage, and single-stage amplifiers for the MPA and HPA have been designed and completed. Figure 16 is a CALMA plot of the mask layout. The circuits are, starting from the upper left corner in the figure and proceeding clockwise, the three-stage MPA (0.6 mm - 1.2 mm - 2.4 mm); the single-stage 1.2 mm circuit; the single-stage 0.6 mm circuit; discrete 2.4 mm, 1.2 mm, and 0.6 mm FETs with both 3.5 μm and 5.0 μm source/drain spacings; the process test bar; the two-stage 1.2 mm - 2.4 mm circuit; and the three-stage HPA (1.2 mm - 2.4 mm - 6.0 mm). The bar size is 370 mils by 370 mils. Nine photomask levels are used for this design (mesa, source/drain, bond pad/inductor, capacitors, nitride etch, air bridge post, air bridge plate, via, and scribe). The gates are exposed by direct-write e-beam lithography. Figure 17 shows a photomicrograph of the HPA/MPA circuits on GaAs.

The first slice of MPAs and HPAs had poor power performance, although small-signal performance was close to that predicted for the one-, two-, and three-stage amplifiers measured (Figures 18 through 21). When the gates were

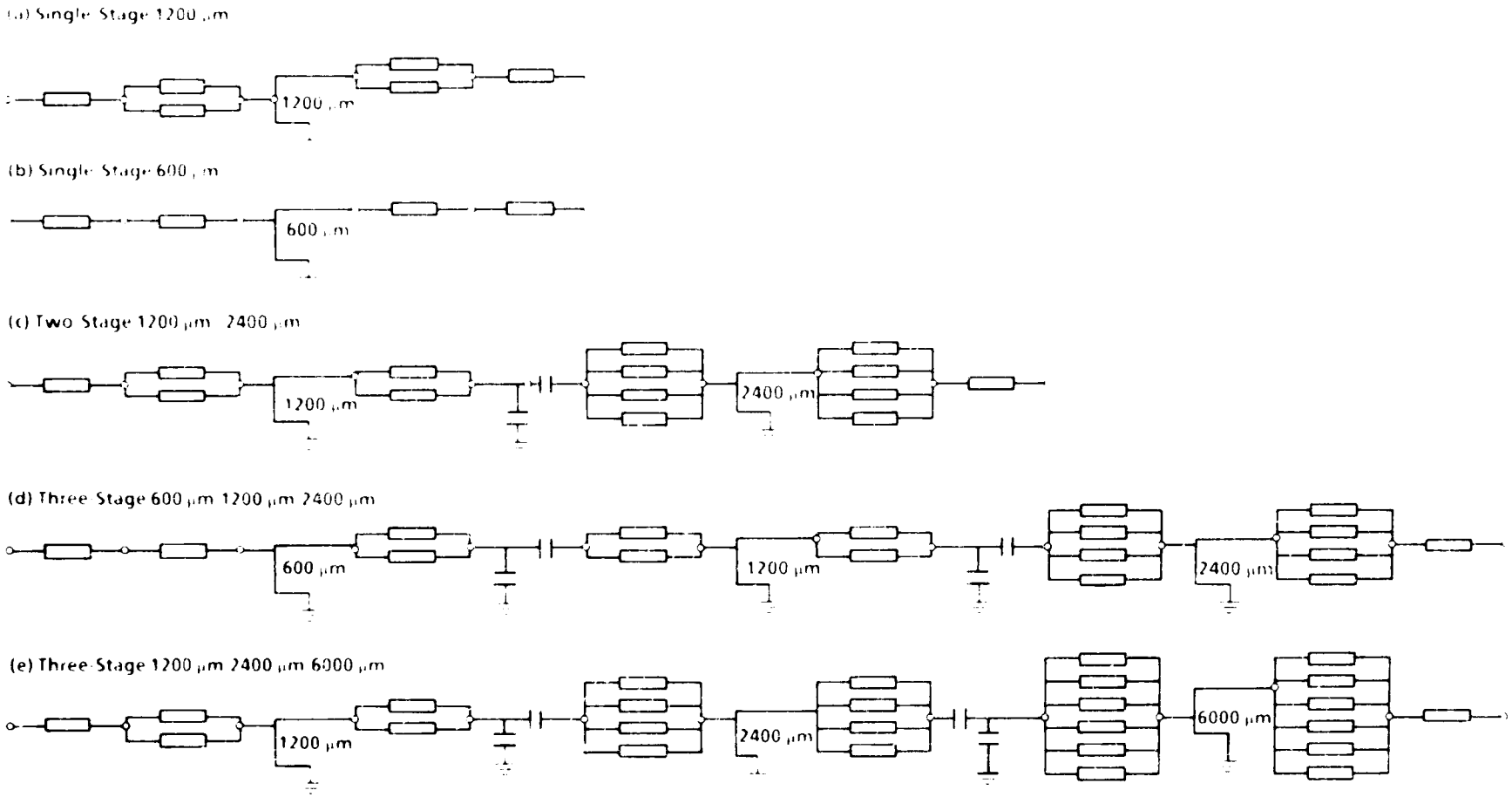


Figure 14. Circuit topologies of Ku-band MMIC amplifiers.

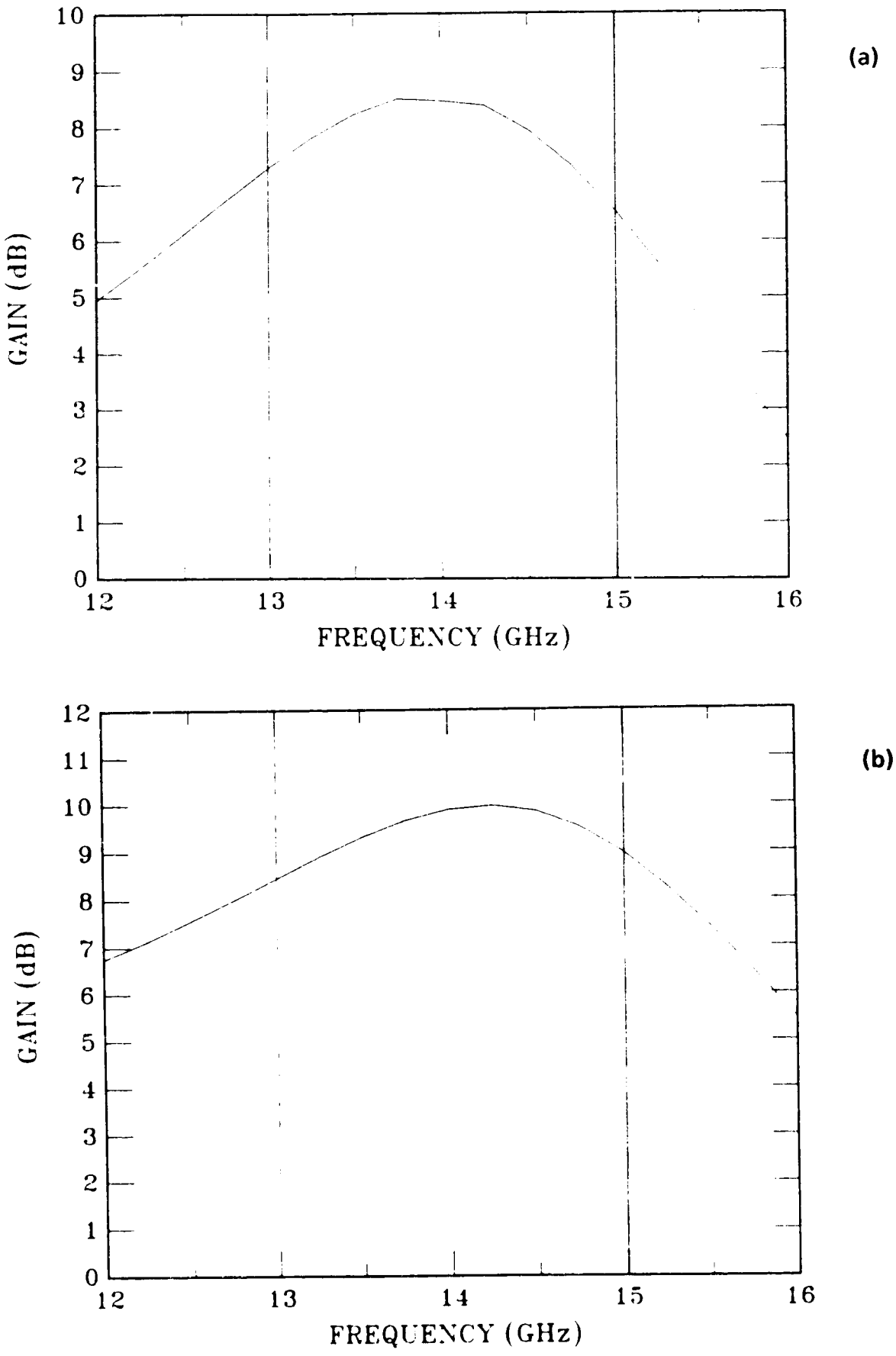
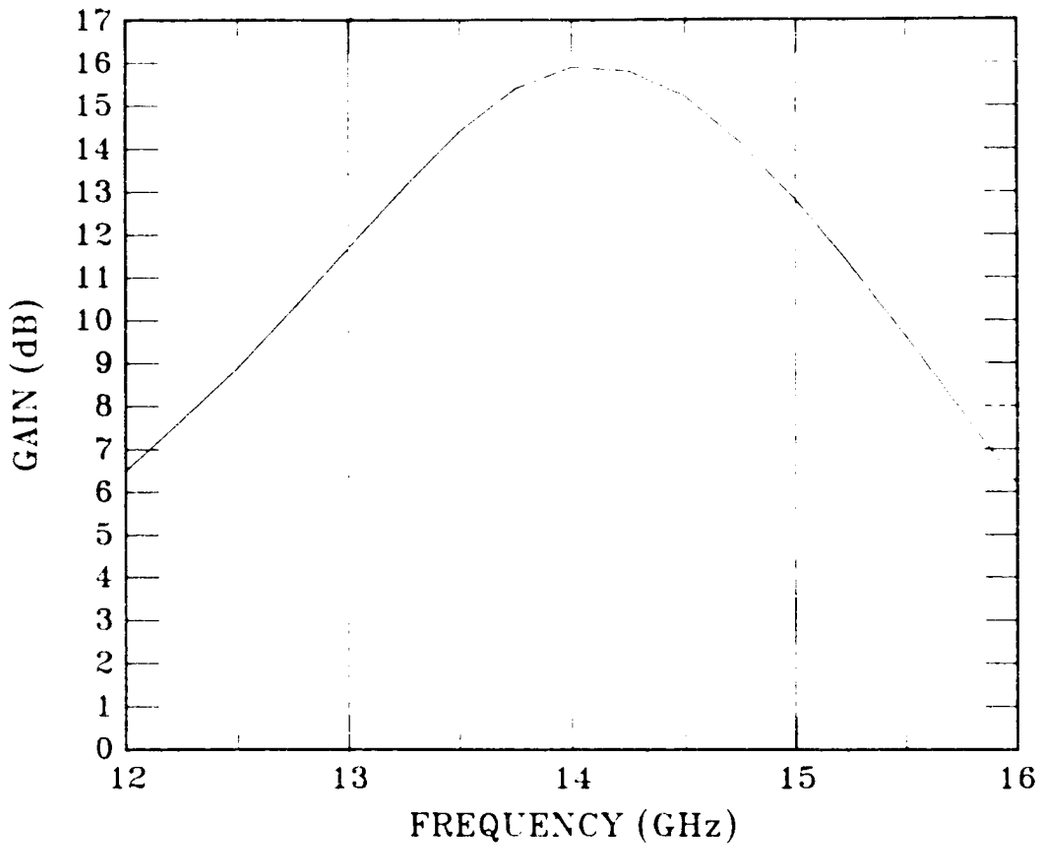


Figure 15. Predicted gain-frequency responses. (a) Single-stage 1200 μm and (b) single-stage 600 μm.



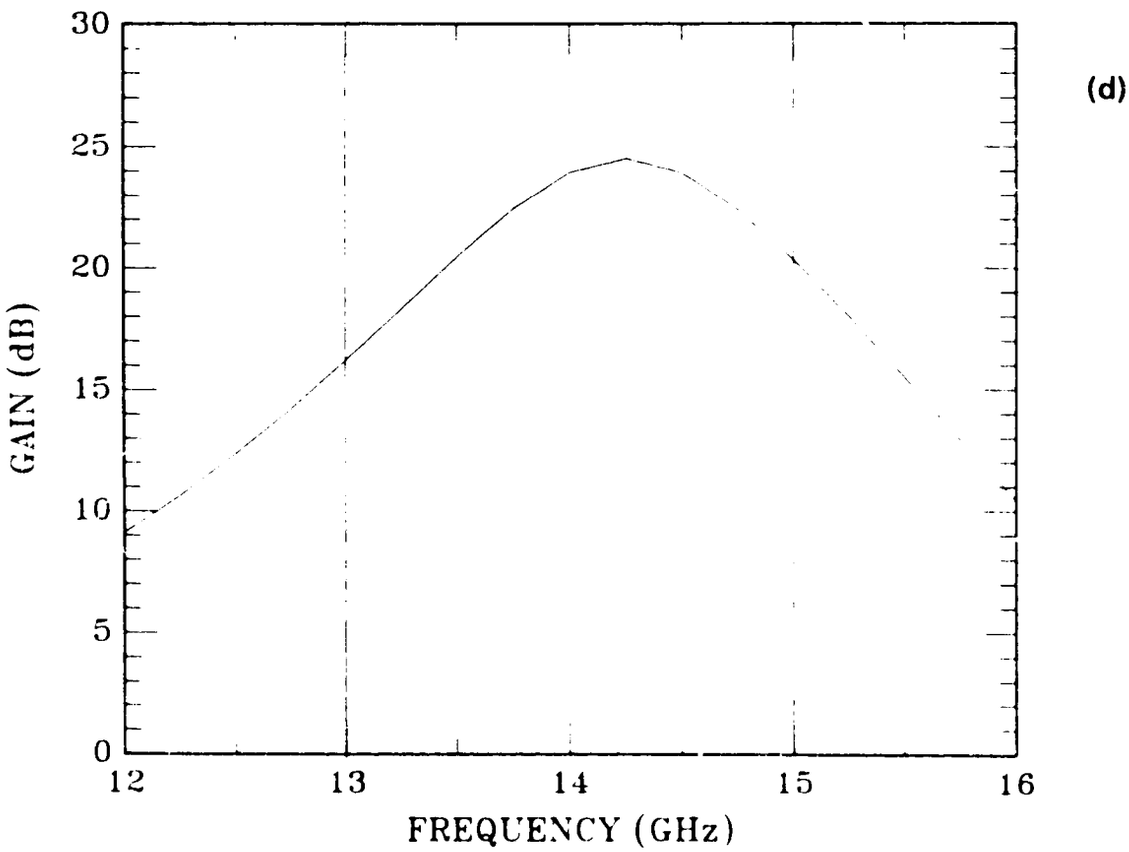


Figure 15. (c) Two-stage 1200 μm - 2400 μm and (d) three-stage 600 μm - 1200 μm - 2400 μm.

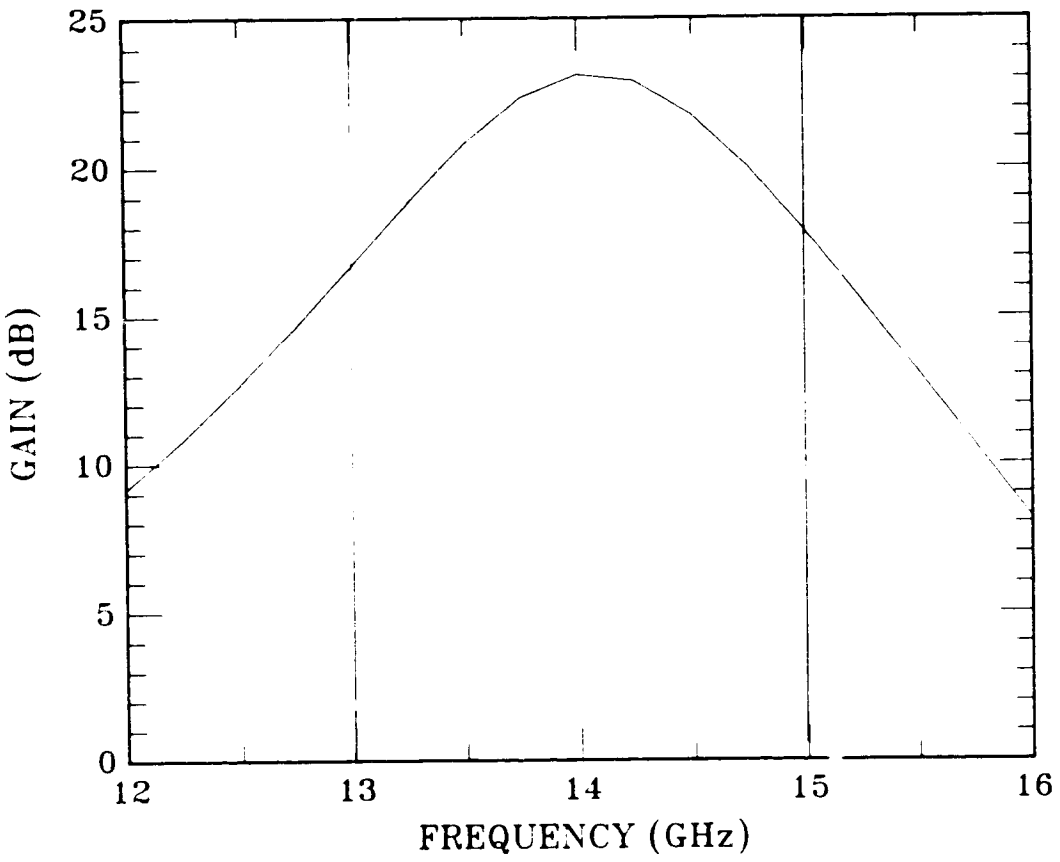


Figure 15(e). Three-stage 1200 μm - 2400 μm - 6000 μm.

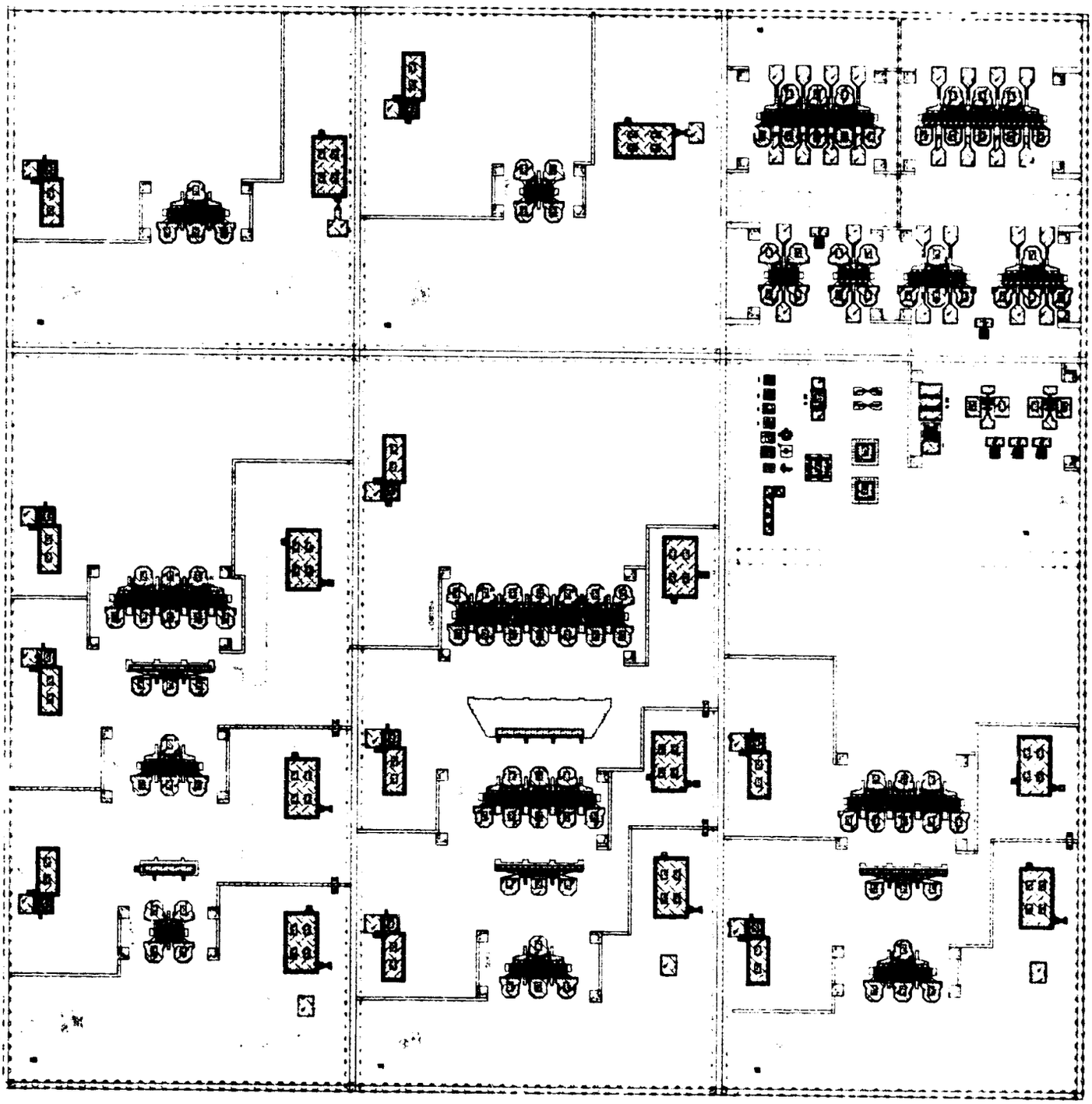


Figure 16. CALMA plot of HPA and MPA circuits. Bar size is 370 x 370 mils^2.

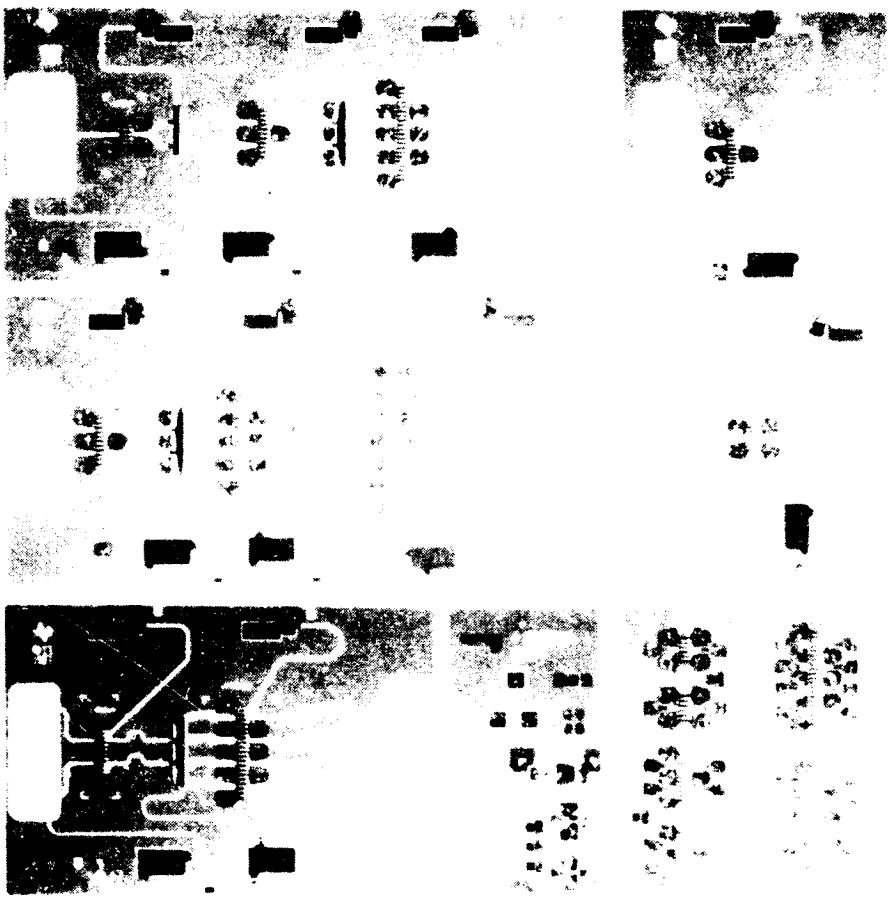


Figure 17. Photomicrograph of HPA/MPA circuits. Bar size is 370 mils x 370 mils.

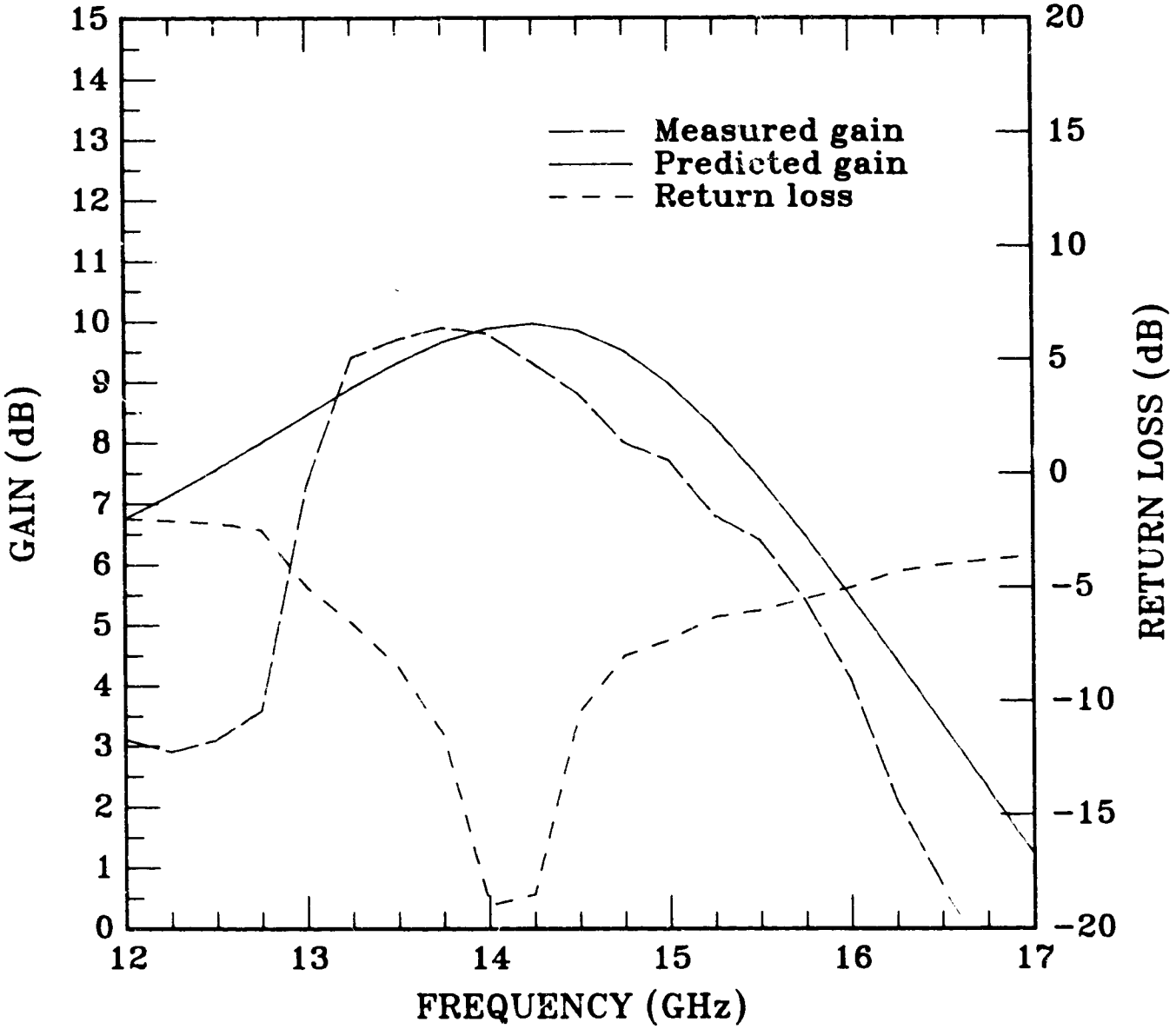


Figure 18. Performance of single-stage 600 μm FET amplifier.

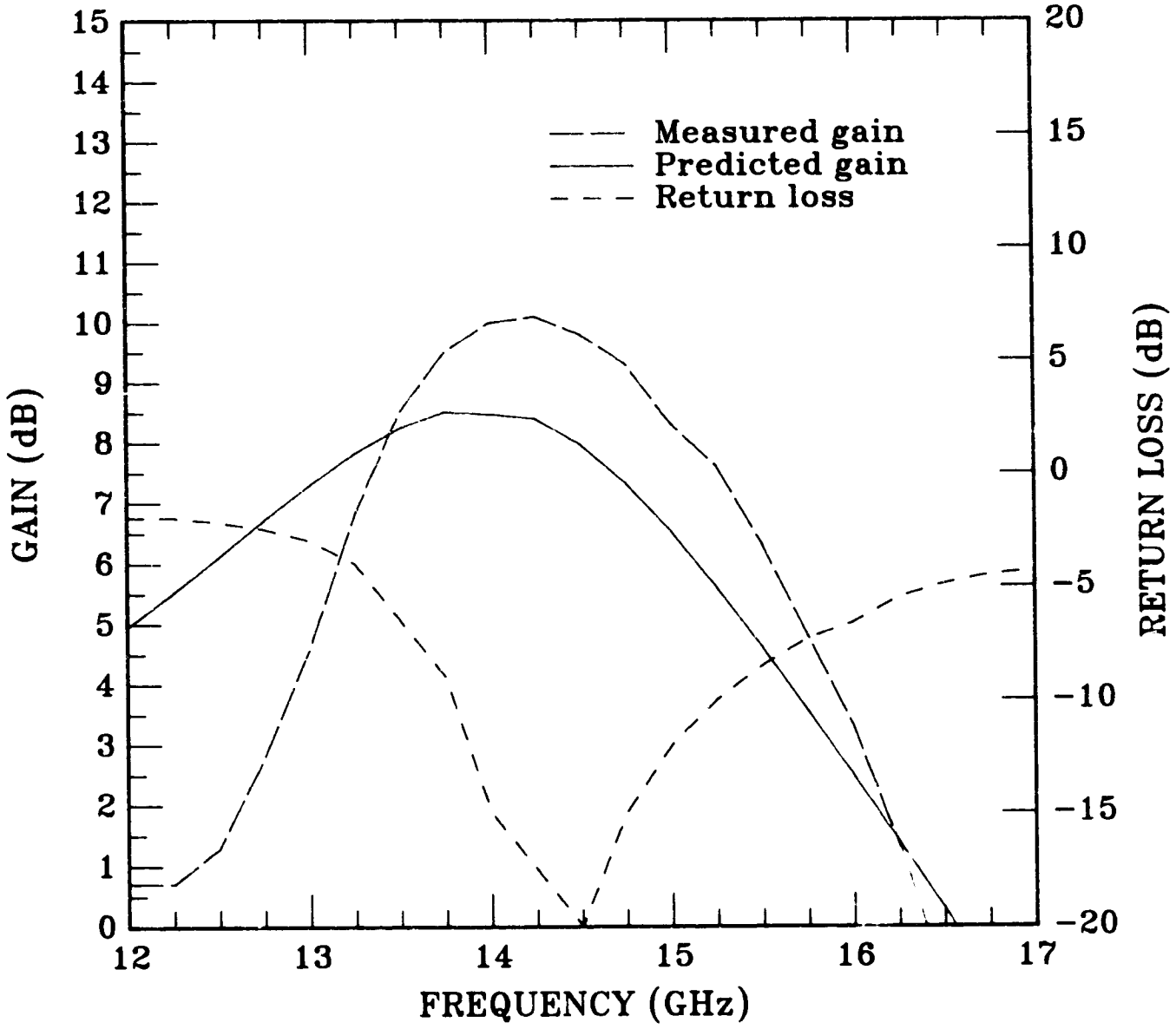


Figure 19. Performance of single-stage 1200 μm FET amplifier.

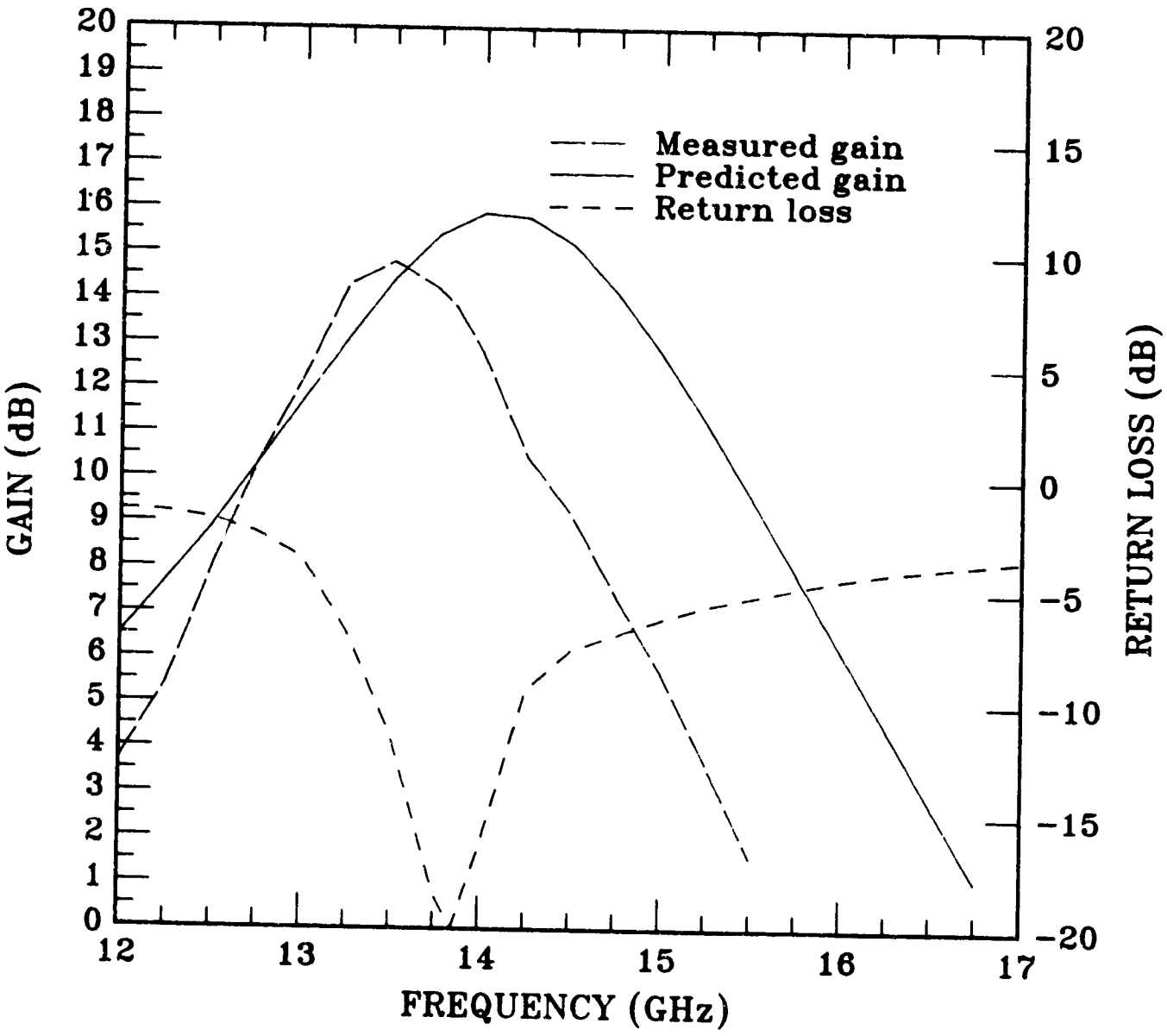


Figure 20. Performance of two-stage 1200-2400 μm FET amplifier.

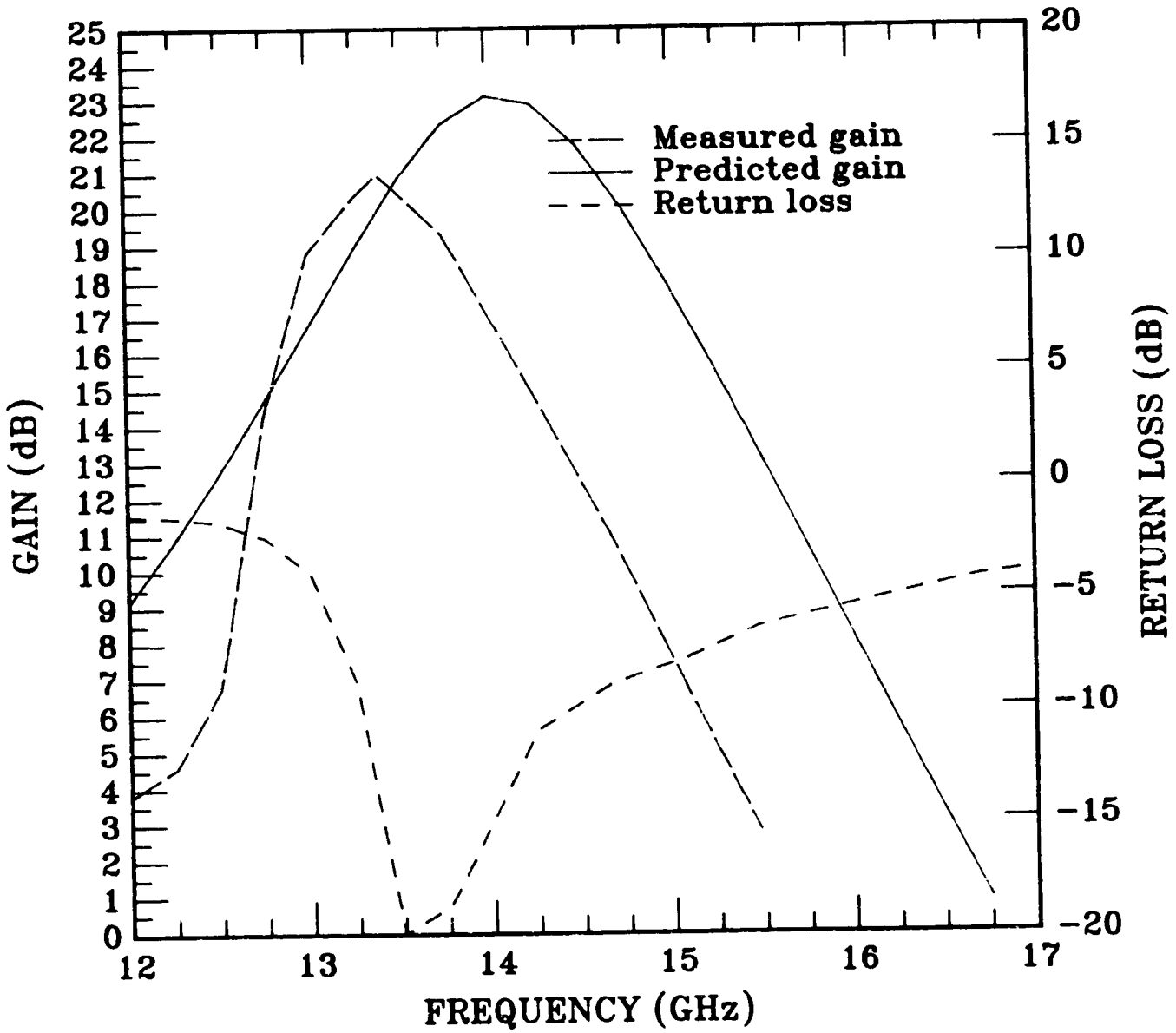


Figure 21. Performance of three-stage 1200-2400-6000 μm FET amplifier.

examined under the microscope, the wide recess was found to be excessive. It had been noted earlier, in device optimization of discrete FETs, that a poor gate recess can severely limit output power.

The second slice showed a marked improvement over the first slice in output power and efficiency. This slice had the proper width for the wide recess. The single-stage 600 μm amplifier had an output power density of 0.4 W/mm and 40% efficiency. The saturation characteristics of this amplifier are shown in Figure 22. An efficiency of 49% with an output power of 0.36 W/mm was obtained from the single-stage 1200 μm amplifier. The small signal performance data for the amplifiers were nearly identical to the data for the first slice (Figure 18 through 21)

Two MBE slices were then processed. The first of these was comparable to the second slice in gain-frequency response (Figure 23) and power performance (Figure 24); the second was low in gain and mismatched at small-signal levels, although power performance was good when the device was retuned (Figure 25).

The latest two slices processed were ion implanted. Initial indications are that they are also comparable to the second slice in performance although they are lower in efficiency. This is possibly due to current levels on the high end of the range of I_{dss} values for that slice.

B. Dual-Gate FET Amplifiers (VPA)

1. Amplifier Design

Dual-gate FET models obtained from a previous NASA contract (NAS3-22886) were used for the initial amplifier design. The modeling effort was continued throughout this report period to aid in device optimization and amplifier design.

Using a 300 μm dual-gate FET on a VPA amplifier with ion-implanted material, an equivalent circuit model was derived from the measured S-parameters using SUPER-COMPACT. Figure 26 shows the equivalent circuit, and

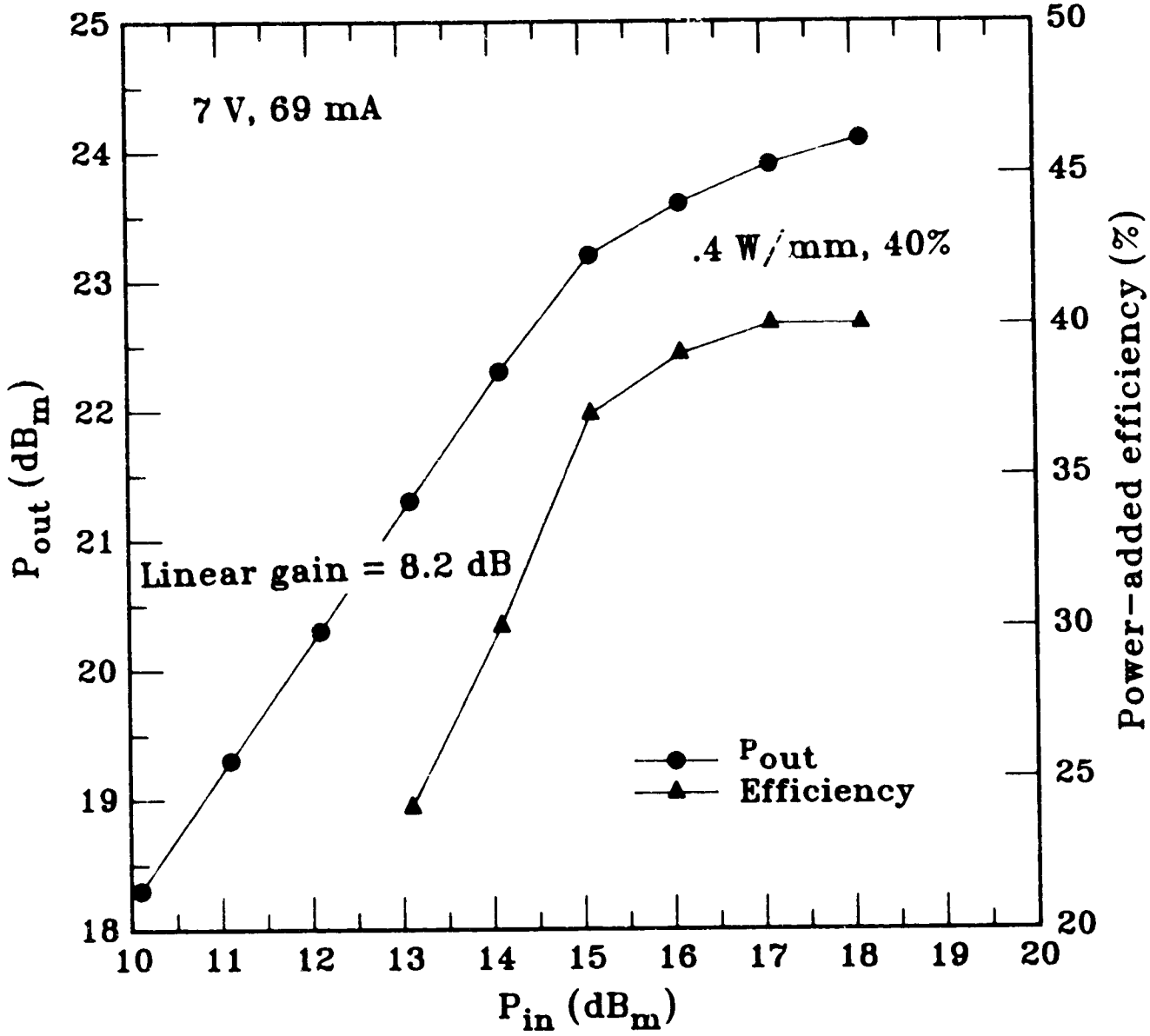


Figure 22. Power performance of a 600 μm single-stage amplifier.

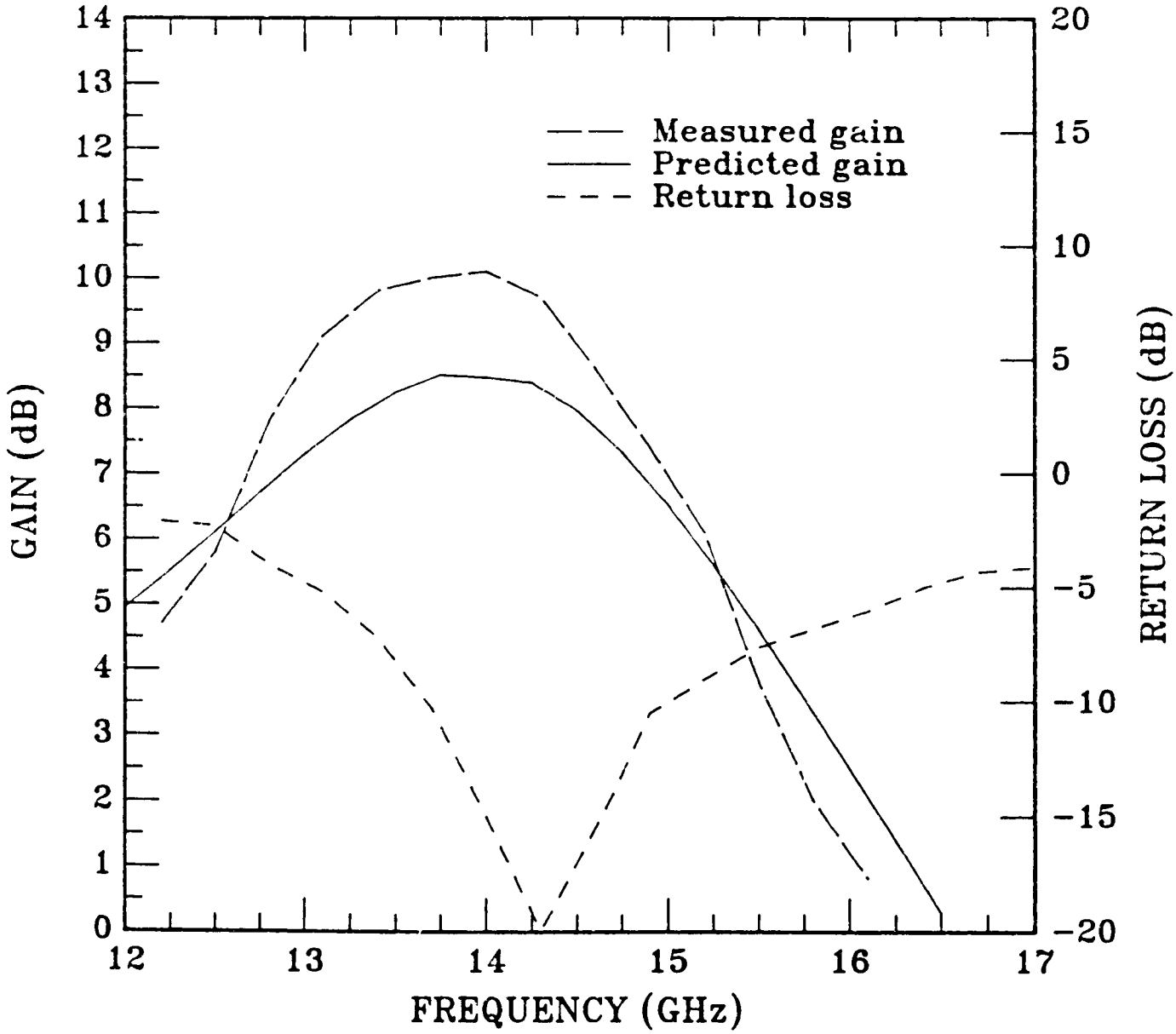


Figure 23. Gain-frequency response of a single-stage 1200 μm FET amplifier.

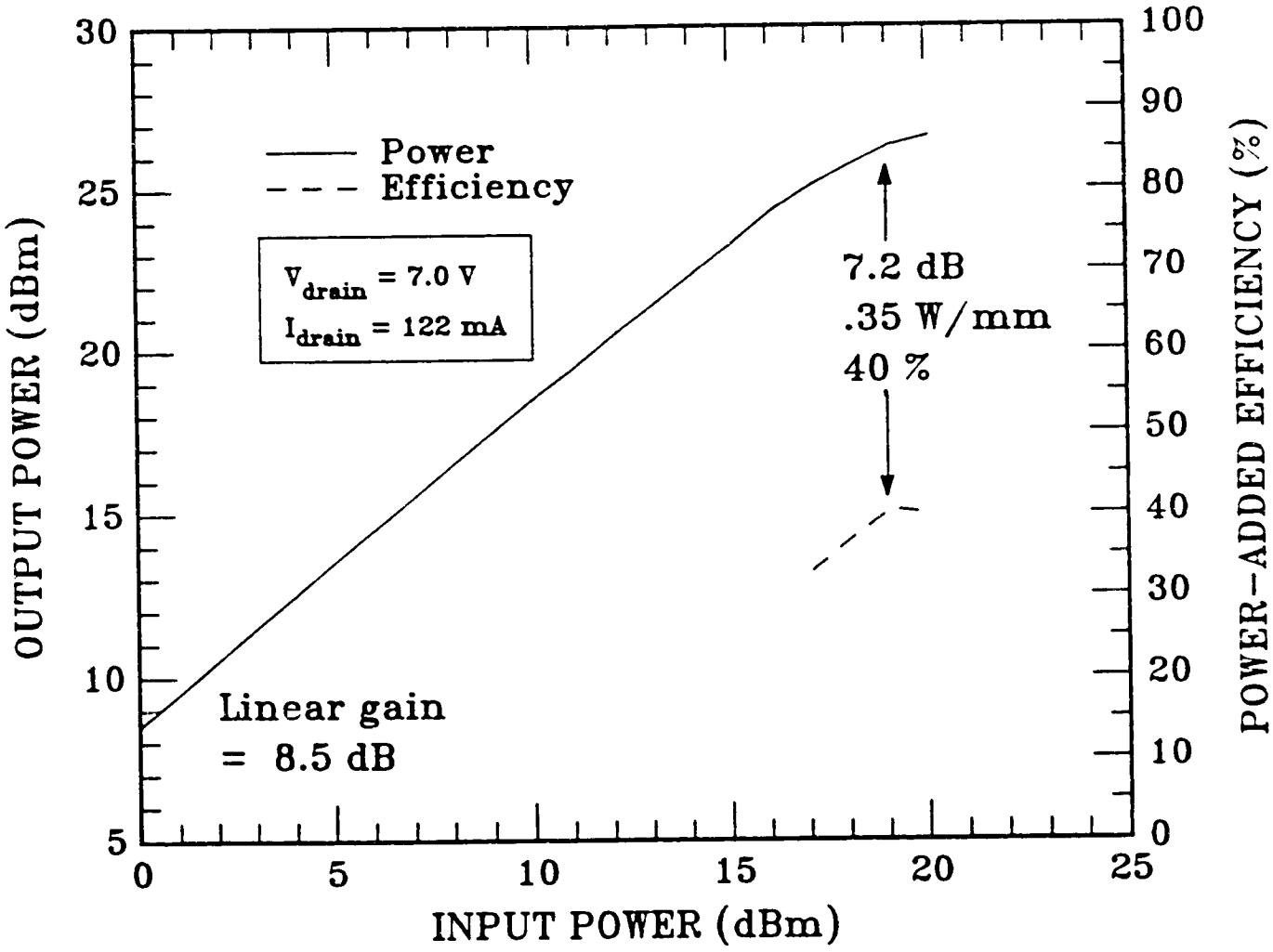


Figure 24. Gain compression at 14 GHz for 1200 μm single-stage amplifier biased and tuned for maximum efficiency.

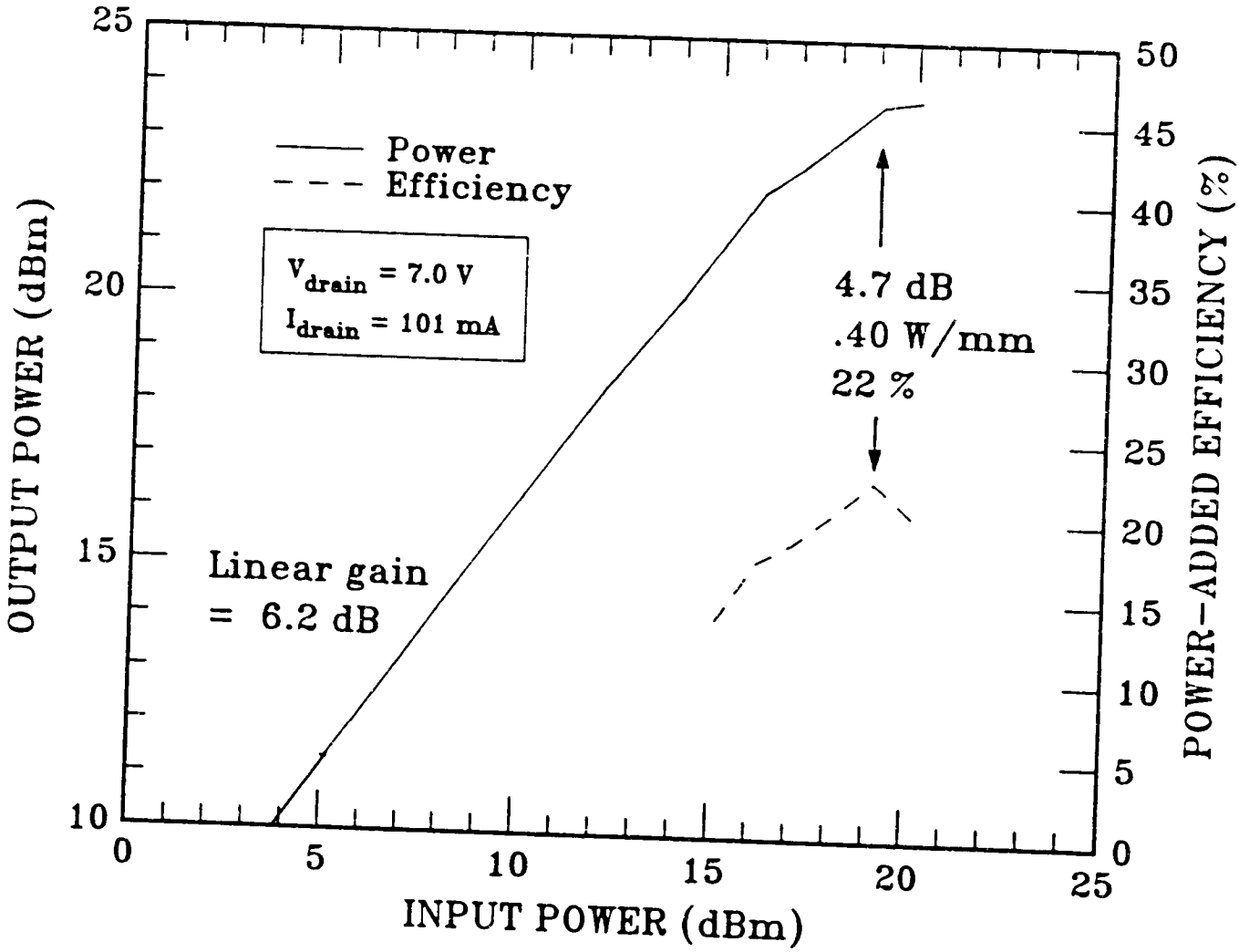


Figure 25. Gain compression at 14 GHz for 600 μm single-stage amplifier biased and tuned for maximum efficiency.

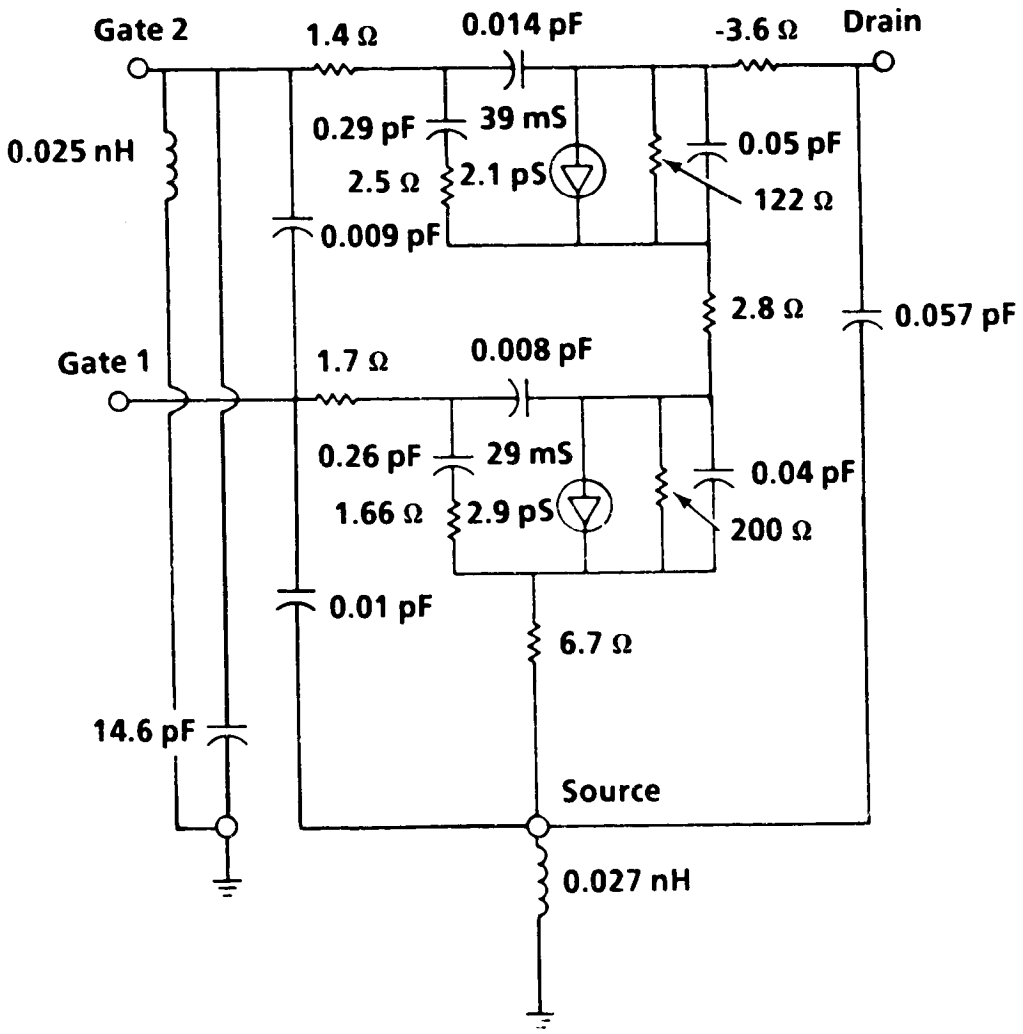


Figure 26. Cascode dual-gate FET model.

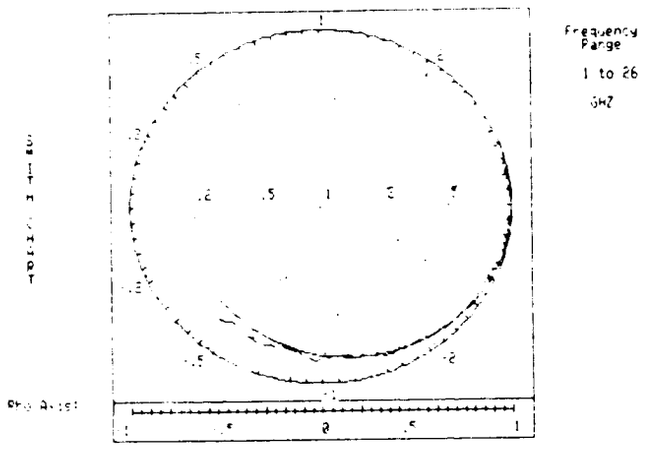
Figure 27 shows the measured and modeled S-parameters. Over the frequency range from 1 to 26 GHz, excellent agreement was obtained between the measured and modeled values. In the model in Figure 26 the second gate was terminated by a parallel combination of inductance and capacitance. It was found that the parallel resonant frequency of this termination causes a drastic output impedance change and a drop in available gain and current gain of the device. Simulations of different resonant frequencies (by changing the terminating capacitance value) verified this theory. For Ku-band operation it is only necessary to increase the capacitance values (by decreasing the nitride thickness) to move the resonant frequency below 10 GHz. This modeling capability of dual-gate FETs will allow us to optimize the device structure and perform rapid design iterations of MMIC amplifiers.

2. Amplifier Fabrication and Evaluation

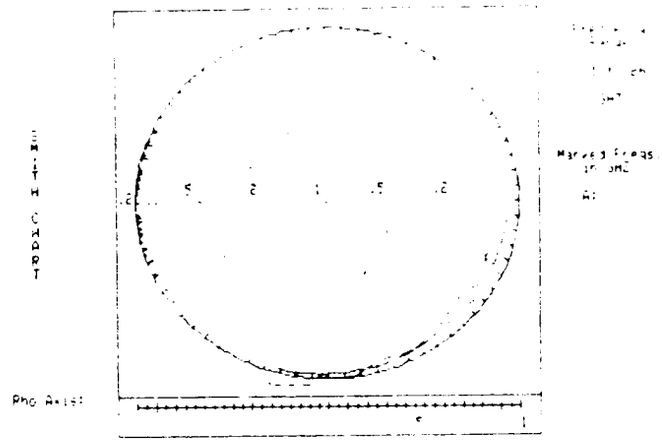
Modifications were made with bond wires to a 20 GHz, four-stage variable power amplifier developed under Contract No. NAS3-22886. Figure 28 shows the gain control characteristics of this amplifier as the second-gate voltages are varied. A gain of 23 dB was obtained with 0 dBm input. When the amplifier was tuned for a higher output power, 450 mW with 26 dB gain was obtained.

The inductor mask level of the four-stage 20 GHz variable power amplifier was modified to shift the operating frequency band down to 13 to 15 GHz. Figure 29 is a CALMA plot of the four-stage amplifier with the modified inductors. The four stages consist of 300 μm, 300 μm, 600 μm, and 1500 μm dual gate FETs.

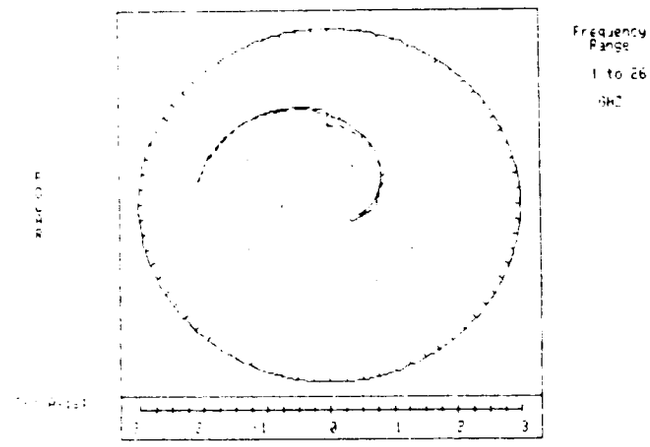
Figure 30 is a photograph of the Ku-band variable power amplifier. Its dimensions are 254 mils x 83 mils. Due to the resonance of the dual-gate FETs at lower Ku-band frequencies (see the section on discrete dual-gate FETs), the four-stage amplifier had lower gain than expected. To improve amplifier performance, the source/drain spacing of the FET was reduced and the mesa level modified. To date, one wafer has been processed with these modifications. Figure 31 shows the gain plot of the four-stage VPA. The amplifier generated 500 mW of power with 20 dB of gain. However, the



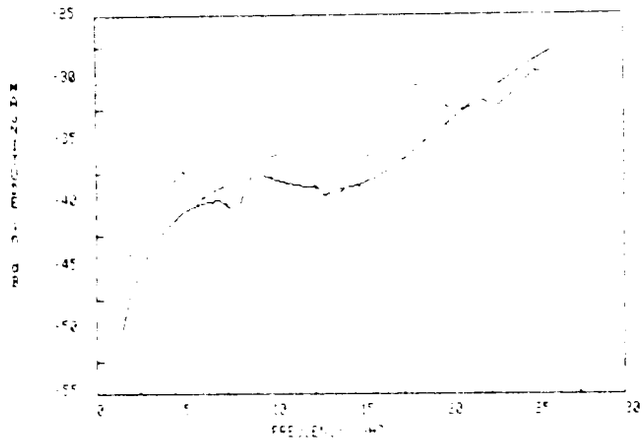
(a) S_{11}



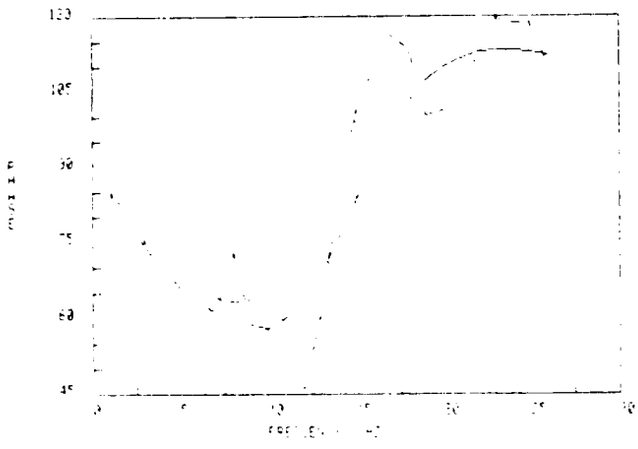
(b) S_{22}



(c) S_{21}



(d) S_{12} Magnitude



(e) S_{12} Phase

Figure 27. Measured and modeled S-parameters of a 0.25 μm x 300 μm dual-gate GaAs FET.

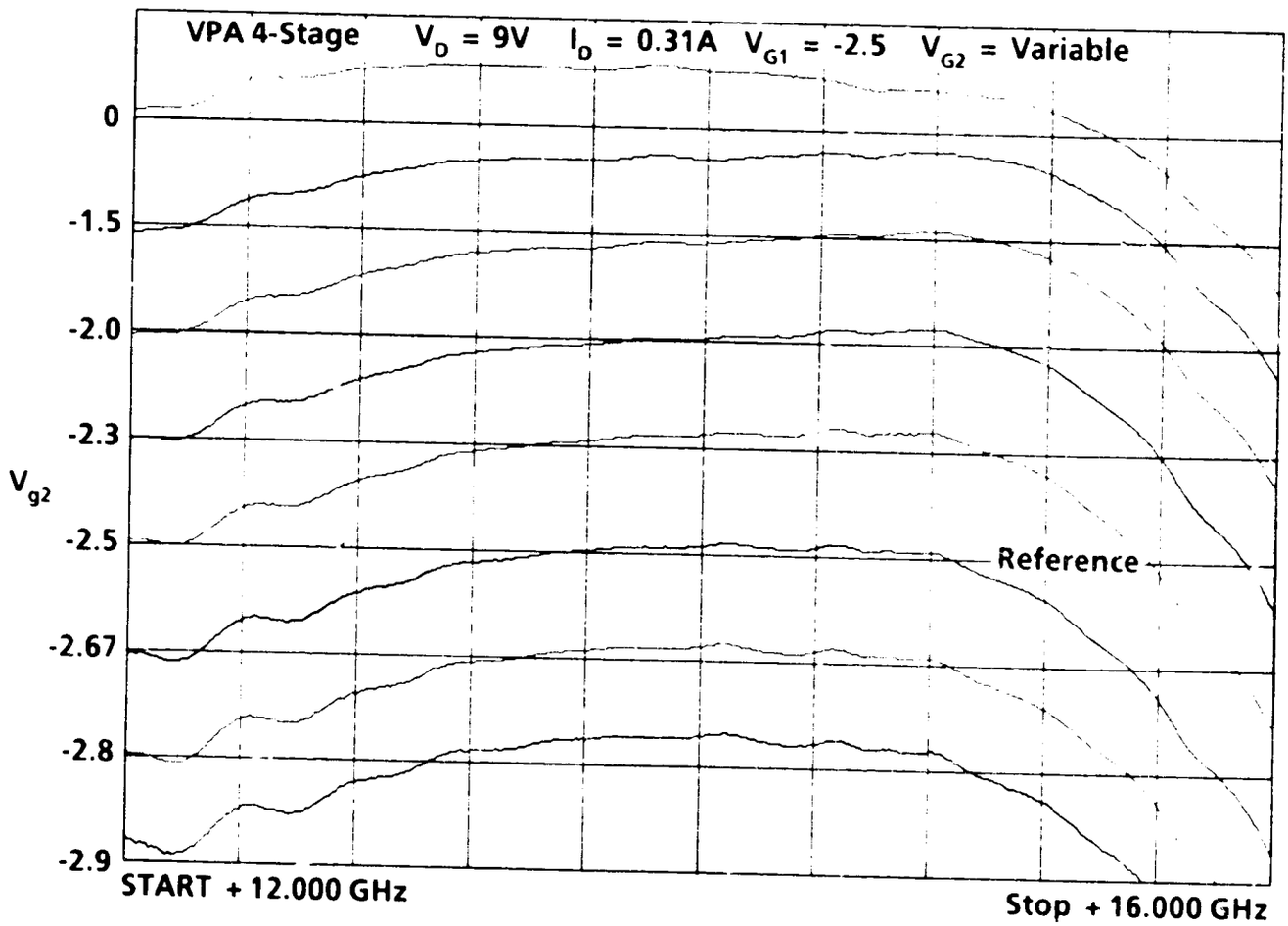


Figure 28. Modified VPA for 13 to 15 GHz operation (vertical scale: 5 dB/division).

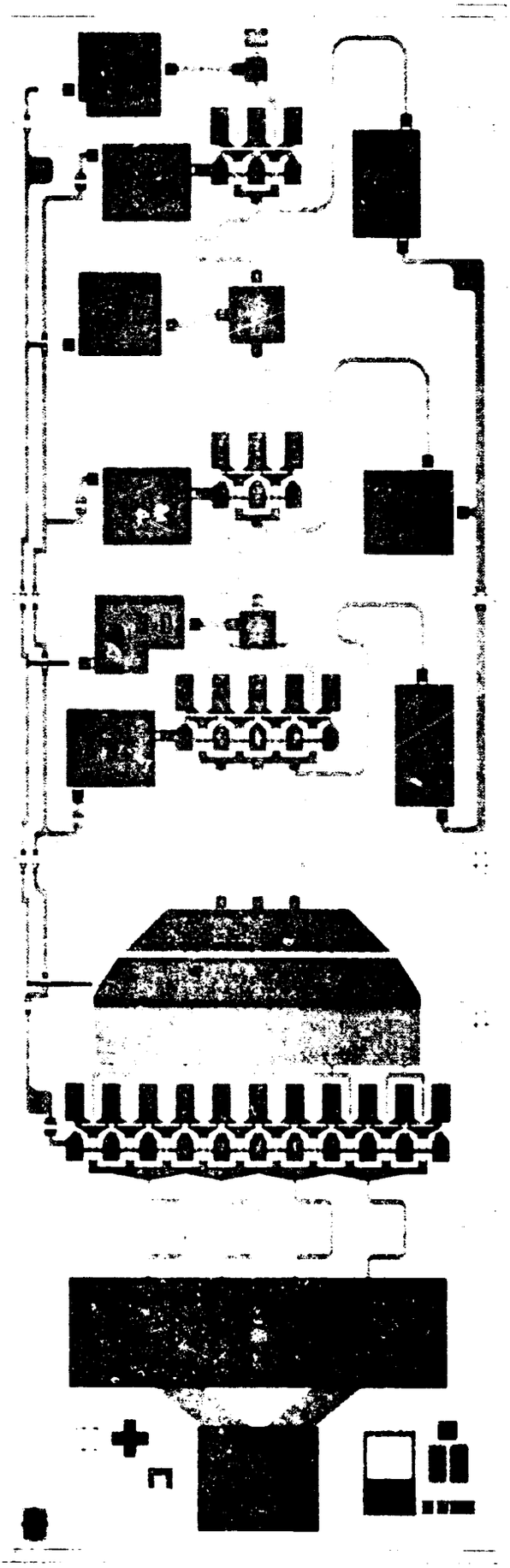


Figure 29. Modified four-stage amplifier for Ku-band operation.

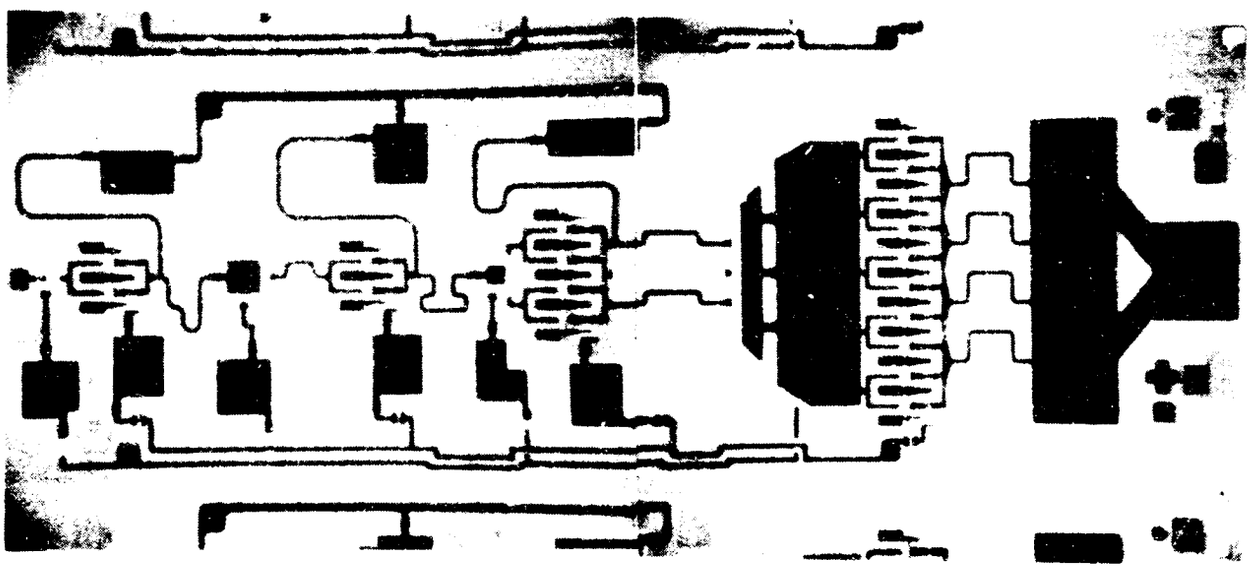


Figure 30. Dual-gate variable power amplifier (VPA).

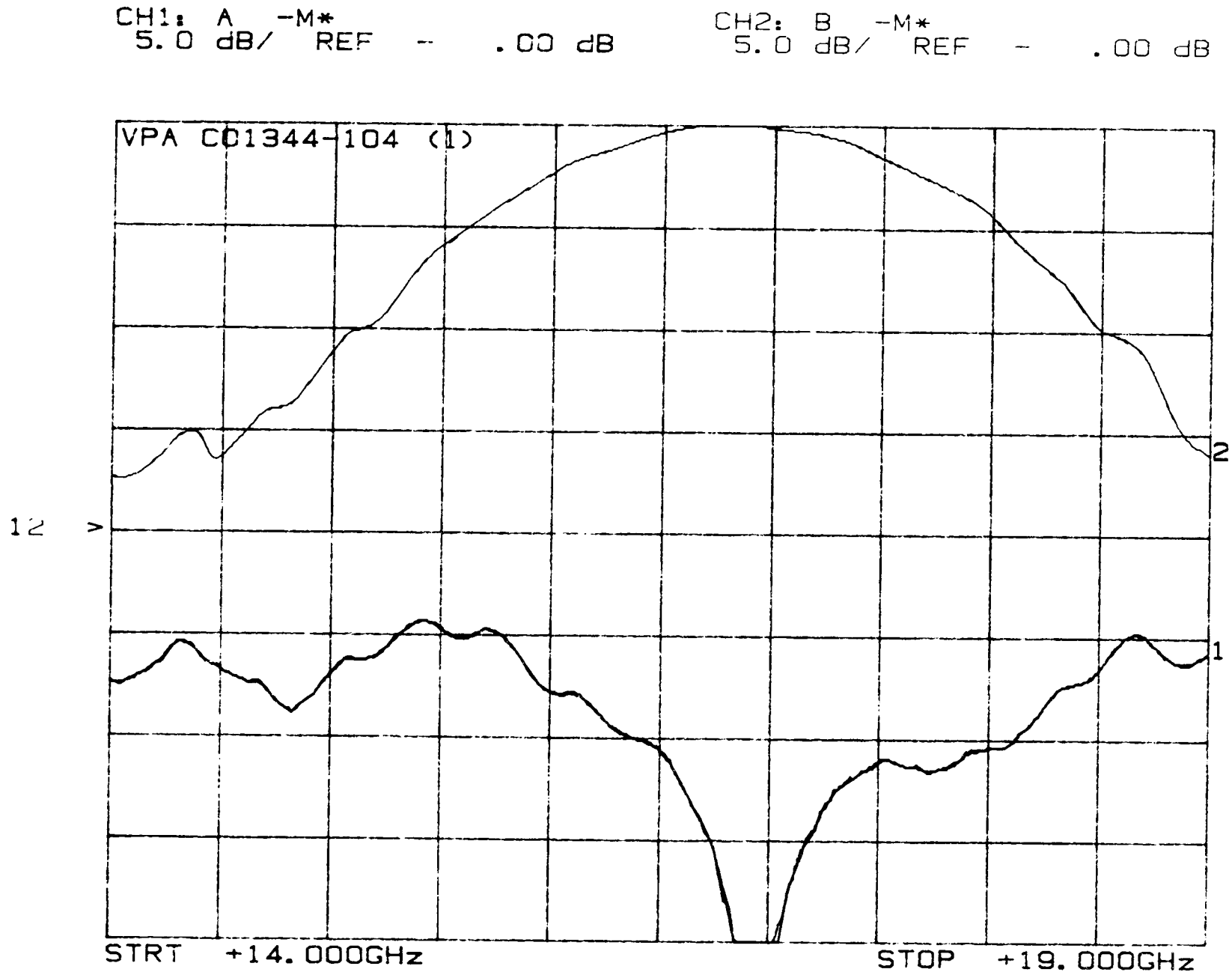


Figure 31. Performance of four-stage variable power amplifier.

frequency is high at 17 GHz. The interstage matching networks need to be modified.

C. D/A Converter

The D/A converter design shown in Figure 32 was proposed initially. The voltage drop at node 1 is I/8 x R, I/4 x R, I/2 x R, and I x R when Q_1, Q_2, Q_3, and Q_4, respectively, are turned ON by a high TTL input. Figure 33 shows the design we used under Contract NAS3-22886. The digital inputs are connected to the gates of transistors Q_1 to Q_4. The sources of these FETs are as biased at 3 V. Thus, a TTL logical 0 pinches them off, and a logical 1 drives them into a forward-biased maximum current mode. The gate widths of Q_1 to Q_4 are scaled by a power of two. The current develops a voltage across resistor R_1 so the digital-to-analog conversion can be performed.

Both designs are sensitive to the value of resistors R and R_1, respectively, and to the saturation current of the FET. The first design has an advantage when a large number of bits are needed, since the switching FETs have the same gate width. Above 4 bits, the gate width of the switching FETs in the second design becomes prohibitive.

Because of its simplicity, we chose the design of Figure 33. The initial parameters are the resistance R_1 and the saturation current of Q_1 to Q_4. In this design we will trim R_1 if necessary. An extra mask level will be used. To have a reproducible saturation current, selective ion implant will be used for Q_1 to Q_7. Gate recess will be used only to fine-adjust the current.

The digital-to-analog converters fabricated are shown in Figure 34. Figure 35 shows the output voltage when the input word counts from 1111 to 0000. The 16 states allow a voltage between -3 V and +1 V to be chosen. (A larger voltage swing can be obtained by increasing the resistor in the circuit.) Several circuits were tested from the two wafers fabricated, with little to no variation. The two wafers were ion-implanted with a peak doping concentration of $\sim 2 \times 10^{17}$ cm^{-3}.

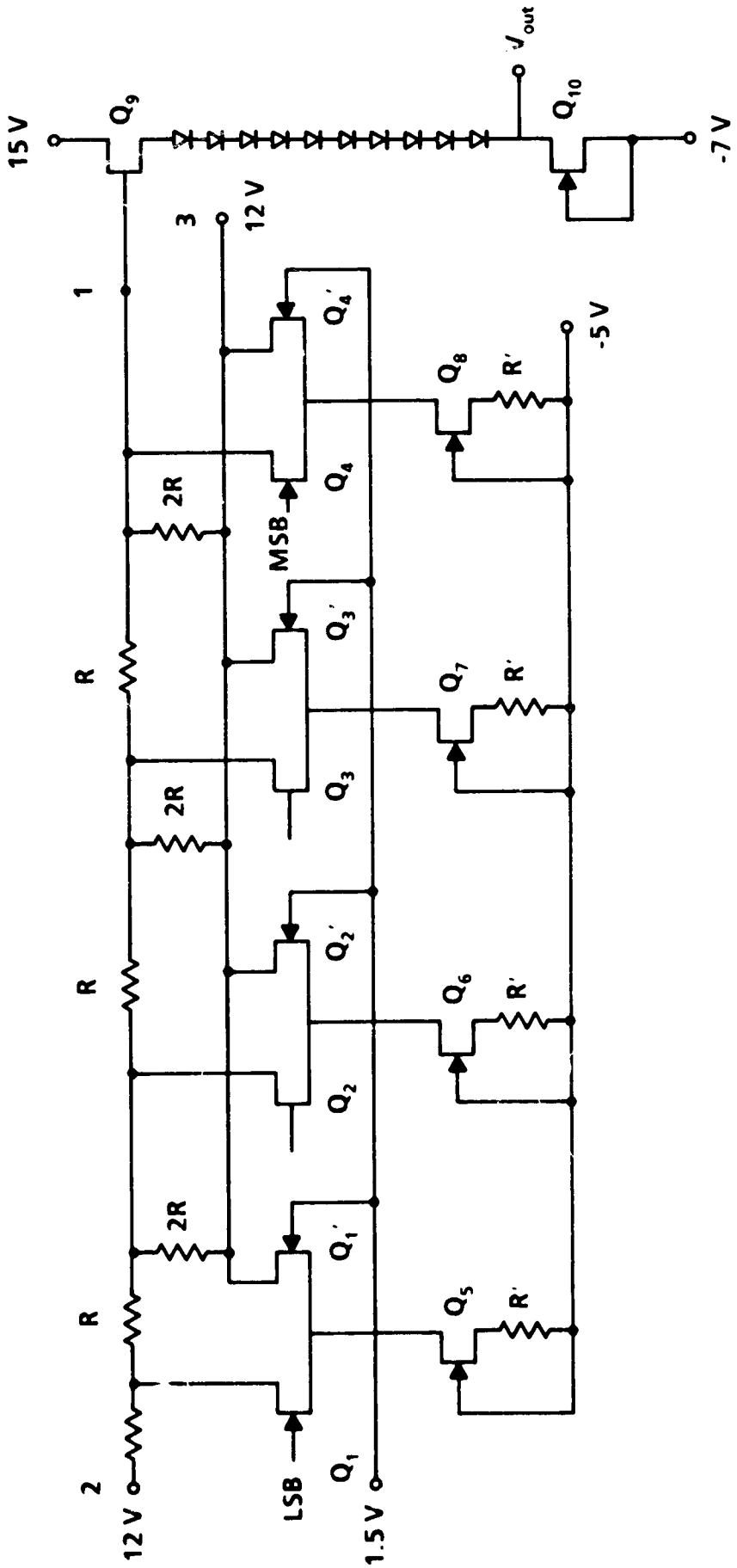


Figure 32. Proposed D/A Converter.

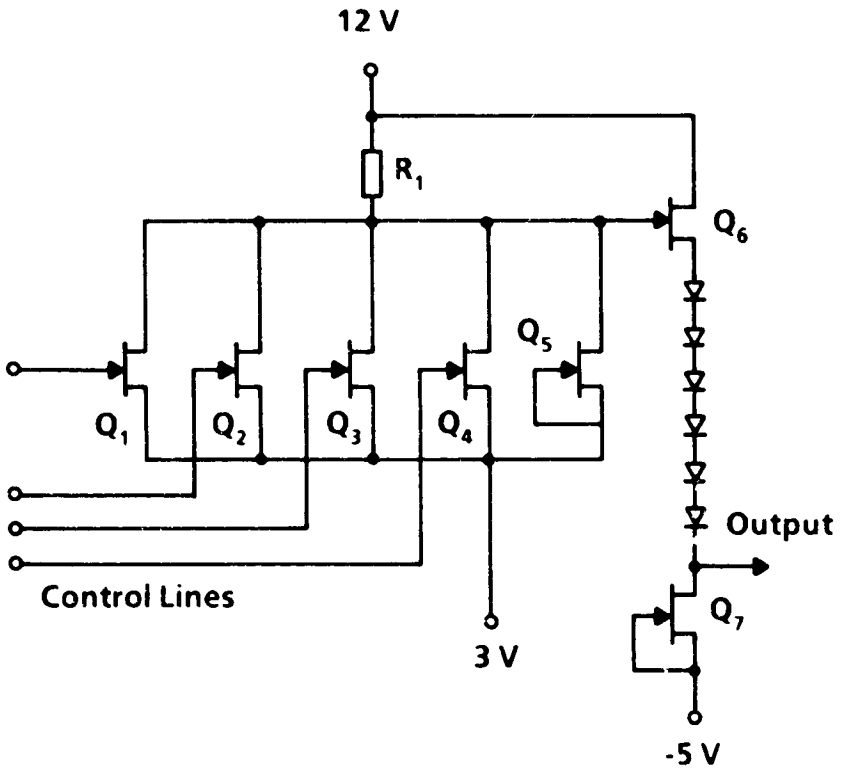


Figure 33. Four-bit D/A converter circuit diagram.

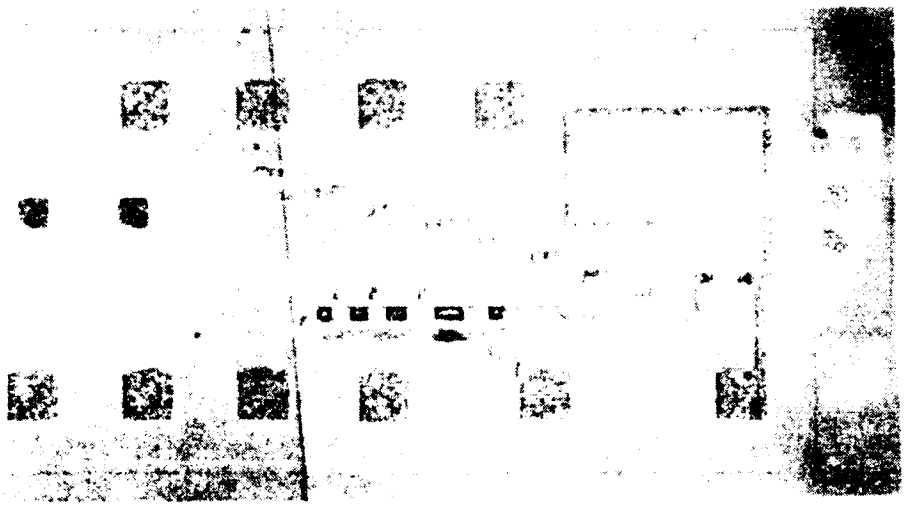


Figure 34. Digital-to-analog converter.

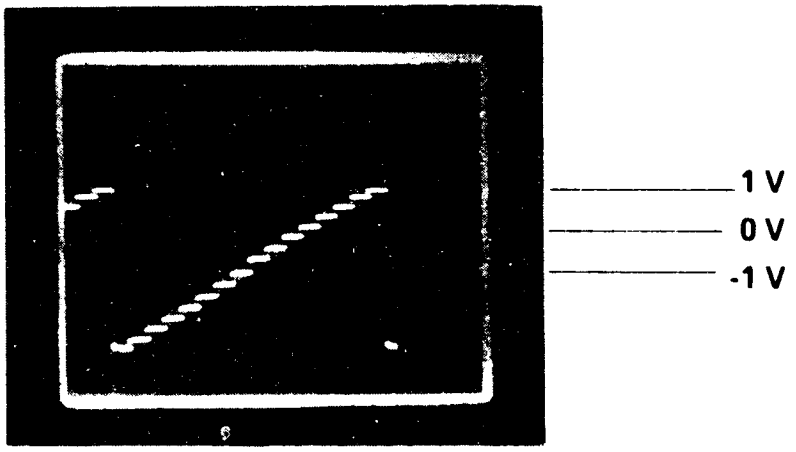


Figure 35. Four-bit digital-to-analog converter output voltage.

V. SUMMARY

Achievements in this program for the first 12-month period are summarized below.

- Single Gate FETs
  - 0.7 W/mm output power with 40% efficiency for MOCVD with AlGaAs buffer.
  - 0.5 W/mm output power with 39% efficiency for MBE.
  - 0.36 W/mm output power with 49% efficiency for implant.

- Dual Gate FETs
  - 0.42 W/mm output power with 27% efficiency for implant.

- D/A converter
  - Fully functional with -3 V to +1 V swing.

- VPA
  - 500 mW output power with 20 dB gain at 17 GHz.

- MPA/HPA
  - Single stage, 600 μm amplifier with 0.4 W/mm output power and 40% efficiency.
  - One-, two-, and three-stage amplifiers with small signal gain and frequency as predicted.

VI. PLANS

Plans for the remaining contract period are summarized below.

- D/A converter
  - Increase resistor value to increase output voltage swing.

- VPA
  - Reduce frequency of amplifier with interstage modifications.
  - Optimize power and efficiency of dual-gate FET.

- MPA/HPA
  - Evaluate higher doped material
  - Determine optimum large signal match of amplifiers for maximum efficiency and power.

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16. Abstract

This report covers the first 12 months of a 30-month contract for the development of Ku-band high efficiency GaAs MMIC power amplifiers. Three amplifier modules operating over the 13 to 15 GHz frequency range are to be developed. The first MMIC is a 1 W variable power amplifier (VPA) with 35% efficiency. On-chip digital gain control is to be provided. The second MMIC is a medium power amplifier (MPA) with an output power goal of 1 W and 40% power-added efficiency. The third MMIC is a high power amplifier (HPA) with 4 W output power goal and 40% power-added efficiency.

An output power of 0.36 W/mm with 49% efficiency has been obtained on an ion implanted single gate MESFET at 15 GHz. On a dual-gate MESFET, an output power of 0.42 W/mm with 27% efficiency has been obtained. A mask set has been designed that includes single-stage, two-stage, and three-stage single gate amplifiers. A single-stage 600 μm amplifier has produced 0.4 W/mm output power with 40% efficiency at 14 GHz. A four-stage dual-gate amplifier has generated 500 mW of output power with 20 dB gain at 17 GHz. A four-bit digital-to-analog converter has been designed and fabricated which has an output swing of -3 V to +1 V.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
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