FINAL REPORT

for

DESIGN OF POWER ELECTRONICS FOR TVC & EMA SYSTEMS

CONTRACT NO. NASA-NAS8-39131

DELIVERY ORDER NO. 24

Submitted by:

R. Mark Nelms, J. Brett Bell, and Michael T. Shepherd
Department of Electrical Engineering
Auburn University

November 7, 1994

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INTRODUCTION

The Component Development Division of the Propulsion Laboratory at Marshall Space Flight Center (MSFC) is currently developing a class of electromechanical actuators (EMAs) for use in space transportation applications such as thrust vector control (TVC) and propellant control valves (PCV). These high power servomechanisms will require rugged, reliable, and compact power electronic modules capable of modulating several hundred amperes of current at up to 270 volts. MSFC has selected the brushless dc motor for implementation in EMAs.

A previous project performed by Auburn University examined the use of the resonant dc link (RDCL) inverter, pulse density modulation (PDM), and mos-controlled thyristors (MCTs) for speed control of a brushless dc motor [1]. The speed of the brushless dc motor is proportional to the applied stator voltage. In a PDM system, the control system determines the number of resonant voltage pulses which must be applied to the stator to achieve a desired speed. The addition of a waveshaping circuit to the front end of a standard three-phase inverter yields a RDCL inverter; the resonant voltage pulses are produced through the action of this waveshaping circuit and the inverter.

The RDCL inverter permits soft-switching of all semiconductor switches in the waveshaping section and the inverter section. In contrast to hard-switching, semiconductors in a soft-switching scheme are turned on or off at conditions of zero voltage and/or zero current. As a result, the inverter switching frequency may be increased, since the switching losses and switching stresses are reduced to low levels. Hard-switching in high power systems such as the EMAs for MSFC can result in considerable electromagnetic interference (EMI). Soft-switching also has the advantage of reduced EMI.

Soft-switching is not achieved without a penalty. In the RDCL, the amplitude of the resonant voltage pulses necessary to produce zero-voltage switching can easily exceed twice the bus voltage [2-3], depending on the circuit operating conditions. For example, on the 270 Vdc system considered for EMAs, the amplitude of the resonant pulses may exceed 540 volts. This is of particular importance for space vehicles which operate in environments where the breakdown voltage is greatly reduced compared to terrestrial levels. Another concern with a PDM system is that the inverter switches may only be changed during the instances of time when the input voltage to the inverter is clamped at zero. Therefore, the number of potential switching instances is reduced in comparison to a pulse-width modulated (PWM) system which has in essence an infinite number of potential switching instances. The disadvantage of a reduced number of potential switching instances is somewhat offset by the higher switching frequencies possible with an RDCL inverter.

Because of concerns with the high peak voltages possible for the RDCL inverter, this project has focused on the implementation of a system which permits zero-voltage switching with the bus voltage clamped at the input voltage level. In the same manner as the RDCL inverter, the inverter selected for this implementation is a combination of a waveshaping circuit and a standard three-phase inverter. In addition, this inverter allows a PWM-like control scheme instead of a PDM scheme. The next chapter of this report will present the inverter implemented for this project. The operation of the waveshaping circuit will be described through analysis and waveforms. Design relationships will also be presented. Chapter 3 contains the design and implementation of a system for the MSFC electromechanical actuation testbed. Experimental results are presented in Chapter 4. Project conclusions are contained in Chapter 5.

Chapter 2

OPERATION, ANALYSIS AND DESIGN OF THE ZVS INVERTER

The EMA testbed at MSFC utilizes a brushless dc motor to control the position of a linear actuator. The rotary motion of the motor is converted to linear motion through the use of a device such as a ball screw. The position of the linear actuator in this system is measured and compared to a position reference signal. The resulting error signal is employed to derive the current command for the brushless dc motor. A three-phase inverter is employed to supply the commanded current to the motor. In high power systems such as the EMA testbed, switching of the large inductive motor currents can result in considerable switching losses and switching stresses in the semiconductors and in EMI. This is particularly true when the devices are hard-switched, i.e. the simultaneous presence of voltage across and current through the semiconductor during the switching transition. Soft-switching occurs when the semiconductors are switched at zero voltage and/or zero current and results in reduced switching stresses, switching losses, and EMI.

This chapter will present the zero-voltage-switched (ZVS) inverter designed, constructed, and tested for the MSFC EMA testbed. The operation of this inverter will be presented first. Inverter operation can be subdivided into six different modes. An equivalent circuit will be given and analyzed for each of the modes. Design equations will be developed based on the analysis.

ZVS Inverter Topology

The zero-voltage-switching characteristics of the inverter are obtained by the addition of a waveshaping circuit to the standard three-phase inverter. An example of this is the RDCL inverter shown in Figure 2.1, which has been examined previously for operation in an EMA system [1-4]. The waveshaping circuit consists of inductor L,

capacitor C, and shunt switch S, which is composed of a semiconductor switch and an anti-parallel diode. The bus is shorted by switch S for a short interval of time. The inductor stores energy during this time interval. Once the switch S is turned off, the capacitor voltage increases sinusoidally from zero to some peak value, determined by the length of the bus shorting interval and the load current, and then returns to zero where it is clamped again at zero. During this period of zero voltage at the inverter input, all switchings of the inverter switches S_1-S_6 are performed at zero voltage.

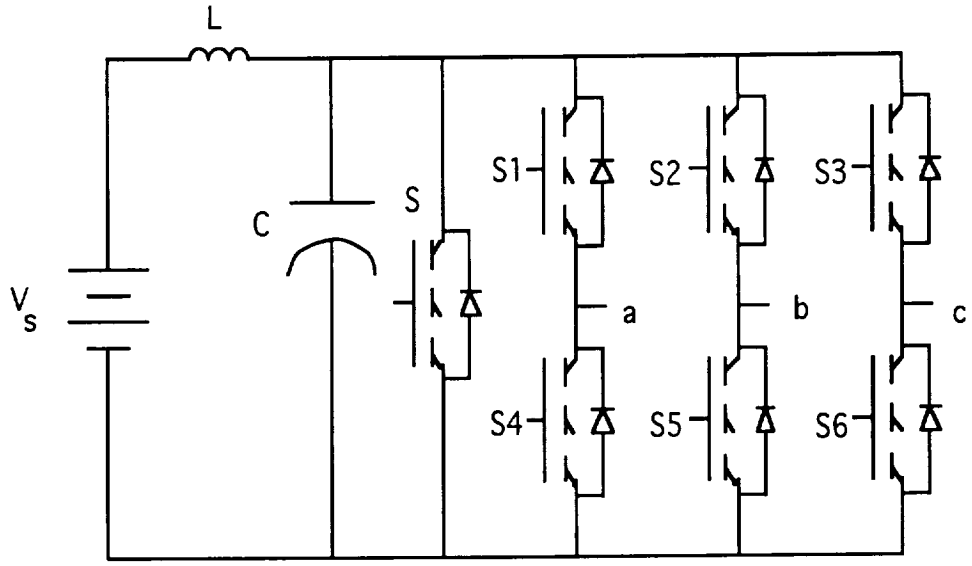

Figure 2.1. Resonant DC Link Inverter [2-3].

Two of the concerns with the circuit of Figure 2.1 is that the voltage across C, which is the input voltage to the three-phase inverter, may reach levels higher than twice the input voltage V_S. For a 270 Vdc system on a space vehicle, these voltage peaks may easily exceed the breakdown voltage in the space environment with the potential of causing system malfunction. The second concern is related to the inductor. Examination of Figure 2.1 shows that all of the power that flows into the load must flow through the inductor. As a result, this inductor must be constructed to be very low loss and also to be capable of carrying a substantial dc current component.

These concerns can be addressed by utilizing a different waveshaping circuit than that of the RDCL inverter. Figure 2.2 shows one possible waveshaping circuit and a three-phase inverter [5-7]. This inverter configuration is selected for implementation in the position controller for the EMA testbed and is referred to as a ZVS inverter because it is capable of both zero-voltage switching and PWM-like operation. The waveshaping circuit is referred to as a parallel-resonant dc link (PRDCL) circuit. Note that it is more complicated than the waveshaping circuit for the RDCL inverter. The PRDCL circuit contains 3 more switches and one more capacitor. The function of switch S_r may be performed by the inverter switches in the same manner as switch S in the RDCL inverter.

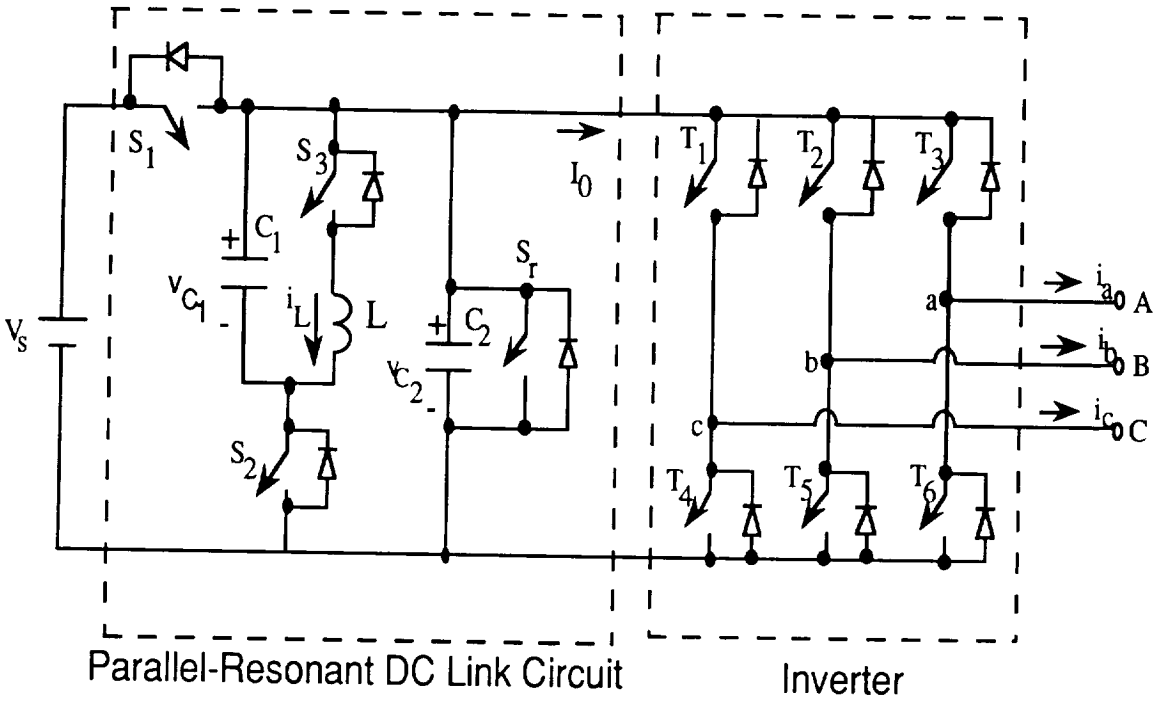

Figure 2.2. ZVS Inverter [5-7].

The operation of the ZVS inverter will be explained with the aid of Figures 2.3 and 2.4 [5-7]. All circuit components are considered to be ideal in the circuit of Figure 2.3. The current I_0 may be modeled as a constant current under the assumptions that the inductance of the inverter load is much larger than L and that the time scale of changes for

the PRDCL circuit variables is much faster than that for the inverter load. The magnitude and sign of the current I_0 depend on the status of the inverter switches T_1-T_6 and the value of the individual phase currents i_a, i_b, and i_c. As will be discussed later, the current control scheme implemented in this brushless dc motor controller results in I_0 being either positive or zero.

Discussion of circuit operation will begin by assuming that the inverter is in steady state and switches S_1 and S_2 are conducting while S_3 and S_r are off. The voltage source V_s is supplying energy to the inverter through S_1. The voltage across both capacitors at this point in time is V_s.

Mode I $[t_0, t_1]$

Switch S_3 is turned on at time t_0. Figure 2.5 shows the equivalent circuit for this circuit condition. The initial conditions for this interval are $v_{c1}(t_0=0) = v_{c2}(t_0=0) = V_s$ and $i_L(t_0=0) = 0$. Note that S_3 is turned on at zero current. The capacitor voltages and inductor current for this mode are described by the following equations:

$$v_{c1}(t-t_0) = v_{c2}(t-t_0) = V_S \tag{2.1}$$

$$i_L(t-t_0) = \frac{V_S}{L}(t-t_0) \tag{2.2}$$

The circuit operates in this mode until time t_1 when sufficient energy has been stored in the inductor to allow v_{C1} and v_{C2} to return to V_s. The value of inductor current at this point in time is given by equation (2.3)

$$I_p = i_L(t_1 - t_0). \tag{2.3}$$

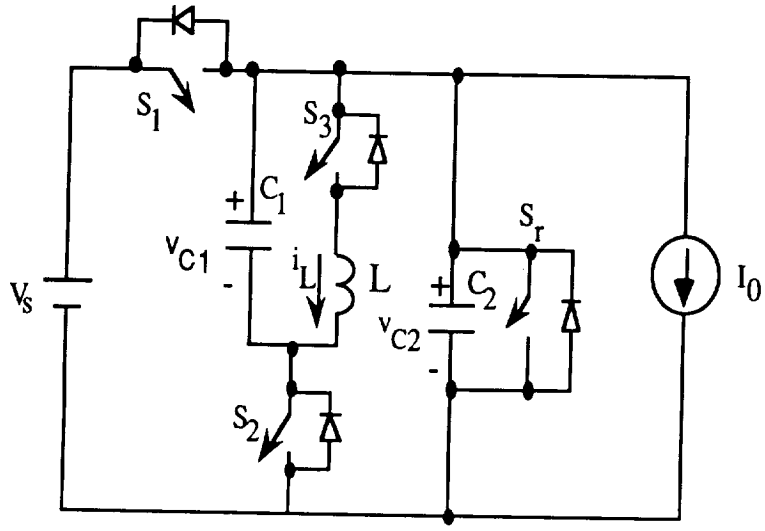

Figure 2.3. PRDCL Circuit with Load Modeled as a Constant Current Source.

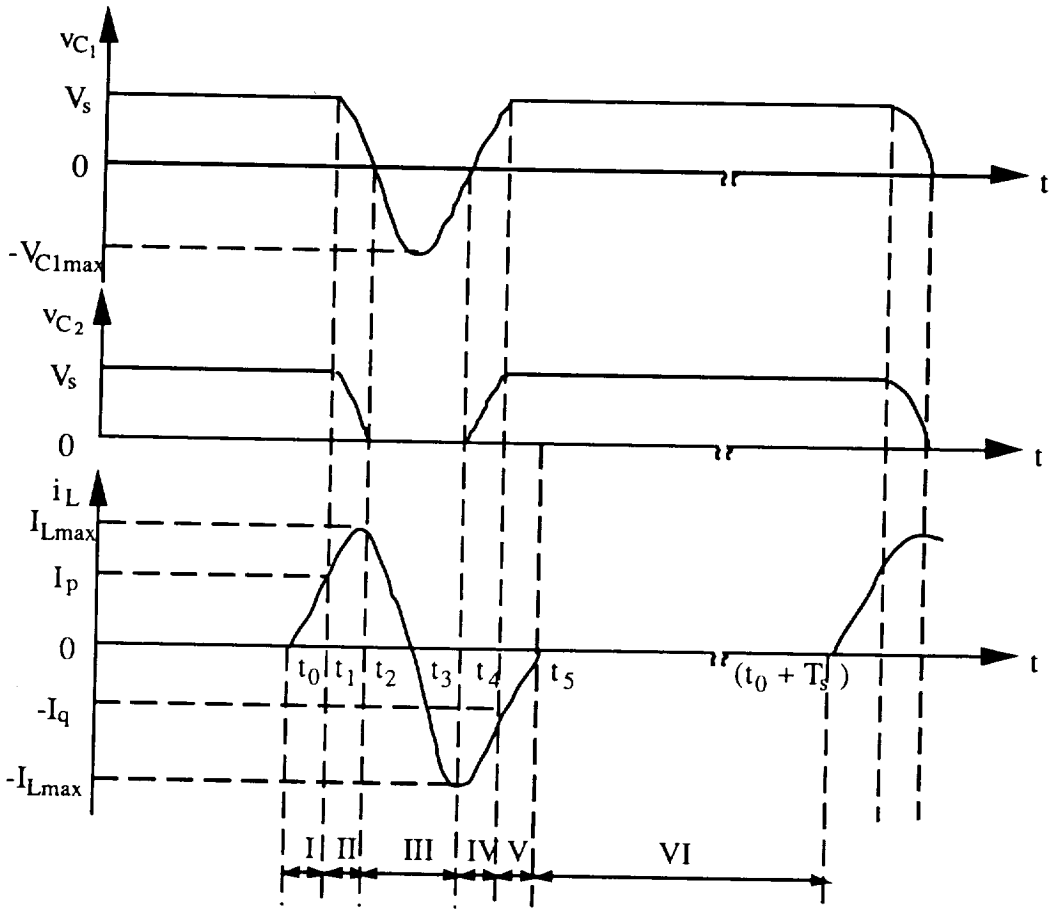

Figure 2.4. Waveforms for the PRDCL Circuit [5-7].

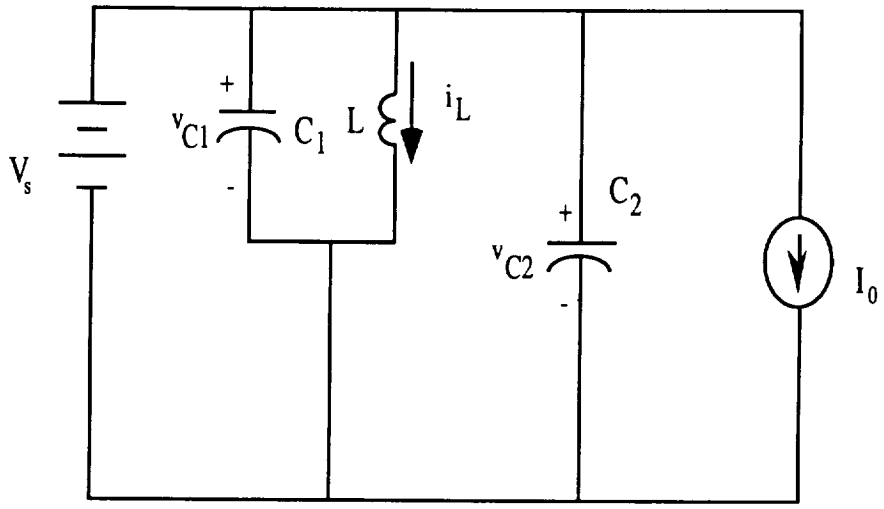

Figure 2.5. Equivalent Circuit for Mode I.

Mode II $[t_1, t_2]$

Once the inductor current has reached I_p, switch S_1 is turned off at zero voltage disconnecting the source V_s from the rest of the circuit so that v_{C2} will ring down to zero. The equivalent circuit for this mode is given in Figure 2.6. The initial conditions for this circuit are $v_{C1}(t_1=0) = v_{C2}(t_1=0) = V_s$ and $i_L(t_1=0) = I_p$. The capacitor voltage and inductor current for this mode are described by the following equations:

$$i_L(t-t_1) = -I_0 + (I_p + I_0)\cos[\omega_1(t-t_1)] + \frac{V_s}{Z_0}\sin[\omega_1(t-t_1)] \tag{2.4}$$

$$v_{C1}(t-t_1) = v_{C2}(t-t_1) = V_s\cos[\omega_1(t-t_1)] - (I_p + I_0)Z_0\sin[\omega_1(t-t_1)] \tag{2.5}$$

where

$$\omega_1 = \frac{1}{\sqrt{L(C_1+C_2)}} \qquad Z_0 = \sqrt{\frac{L}{(C_1+C_2)}}.$$

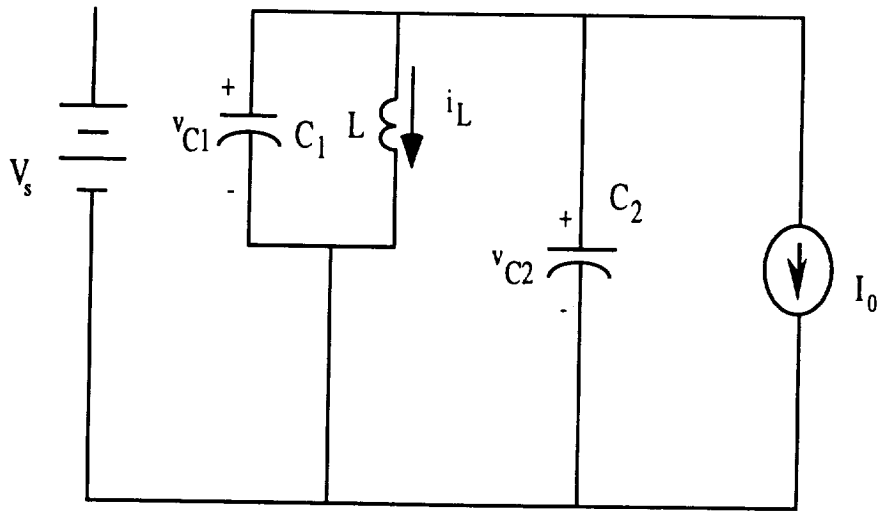

Figure 2.6. Equivalent Circuit for Mode II.

In this mode, the energy stored in the inductor begins to discharge capacitors C_1 and C_2. This interval ends when $v_{C1}(t_2\text{-}t_1) = v_{C2}(t_2\text{-}t_1)=0$. The length of this mode $[t_2\text{-}t_1]$ can be found from equation (2.5) and is

$$(t_2 - t_1) = \frac{1}{\omega_1}\tan^{-1}\left(\frac{V_s}{(I_p + I_0)Z_0}\right). \tag{2.6}$$

Equation (2.5) also gives the necessary condition for the capacitor voltage to reach zero

$$(I_p + I_0)Z_0 > V_s. \tag{2.7}$$

Since the capacitor voltage is zero at the end of this interval, the inductor current has reached its maximum value designated I_{Lmax}.

Mode III $[t_2, t_3]$

Since the end of Mode II is signaled by the capacitor voltage v_{C2} reaching zero, this voltage can be monitored and used as a control signal to turn switch S_2 off and switch S_r on at zero

voltage. The equivalent circuit for this mode is given in Figure 2.7. The capacitor voltage v_{C2}, which is the input voltage for the three-phase inverter, is clamped at zero by switch S_r. The inverter devices are switched on or off during this zero voltage period. Capacitor voltage v_{C1} continues to decrease from zero to a peak negative value of - v_{C1max} and then returns to zero. Note that v_{C1max} will exceed the value of V_S; however, this capacitor is not connected to the bus so that the source voltage is constant at V_S. The inductor current begins this mode at I_{Lmax} and decreases, actually becoming negative before the end of the mode.

Using the initial conditions of $v_{C1}(0) = v_{C2}(0) = 0$ and $i_L(0) = I_{Lmax}$, the solution for the circuit variables are

$$v_{C2}(t - t_2) = 0 \tag{2.8}$$

$$v_{C1}(t - t_2) = -V_{C1max} \sin \omega_2 (t - t_2) \tag{2.9}$$

$$i_L(t - t_2) = I_{Lmax} \cos \omega_2 (t - t_2) \tag{2.10}$$

where

$$\omega_2 = \frac{1}{\sqrt{LC_1}} \quad \text{and} \quad V_{C1max} = \sqrt{\frac{L}{C_1}} I_{Lmax} = \omega_2 L I_{Lmax}.$$

This mode ends when the voltage v_{C1} returns to zero; therefore the length of this mode is

$$t_3 - t_2 = \pi \sqrt{LC_1} = \frac{\pi}{\omega_2}. \tag{2.11}$$

From equation (2.10), the inductor current has a value of -I_{Lmax} at the end of this mode.

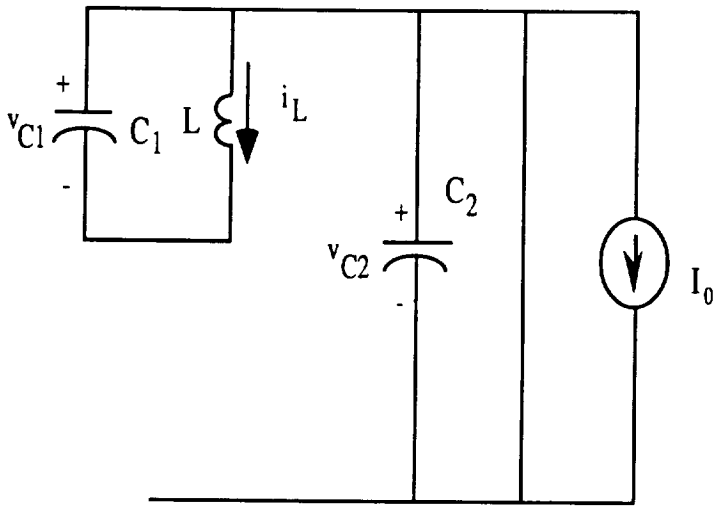

Figure 2.7. Equivalent Circuit for Mode III.

Mode IV [t_3, t_4]

At the beginning of this mode, both v_{C1} and v_{C2} are zero and i_L equals - I_{Lmax}. Switch S_2 is turned on at zero voltage while switch S_r is turned off at zero voltage. The equivalent circuit for this mode is given in Figure 2.8, which is the same as that for Mode II. The initial conditions for the circuit variables are $v_{C1}(0) = v_{C2}(0) = 0$ and $i_L(0) = - I_{Lmax}$. The solutions for the capacitor voltages and inductor current are

$$i_L(t-t_3) = (I_0 - I_{L\max})\cos[\omega_1(t-t_3)] - I_0 \tag{2.12}$$

$$v_{C1}(t-t_3) = v_{C2}(t-t_3) = (I_{L\max} - I_0)Z_0 \sin[\omega_1(t-t_3)]. \tag{2.13}$$

This interval ends when the voltages of equation (2.13) reach V_S. At this point, the diode in anti-parallel with switch S_1 begins to conduct. S_1 can now be turned on at zero voltage. The inductor current at the end of this mode has a value of $-I_0$. The length of this interval is given by

$$t_4 - t_3 = \frac{\pi}{2\omega_1}. \tag{2.14}$$

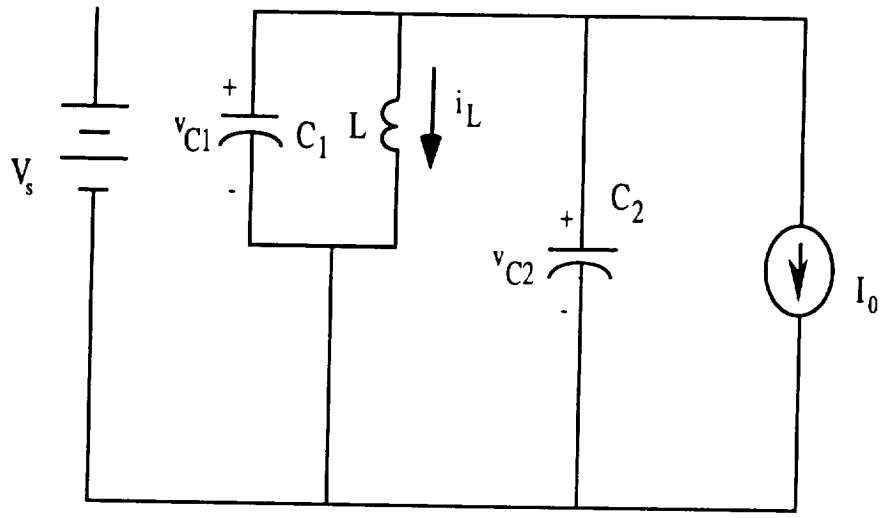

Figure 2.8. Equivalent Circuit for Mode IV.

Mode V [t_4, t_5]

This mode begins when S_1 is turned on at zero voltage. Both of the capacitor voltages have a value of V_s during this mode. The inductor current begins this mode with a negative value and continues to increase toward zero. This current is flowing through the anti-parallel diode of switch S_3; therefore, this switch can be turned off at zero voltage. Using initial conditions of $v_{C1}(0) = v_{C2}(0) = V_s$ and $i_L(0) = -I_0$, the solutions for the capacitor voltages and inductor current are

$$v_{C1}(t-t_4) = v_{C2}(t-t_4) = V_s \tag{2.15}$$

$$i_L(t-t_4) = \frac{V_s}{L}(t-t_4) - I_0. \tag{2.16}$$

This mode ends when the inductor current reaches zero and the anti-parallel diode of S_3 turns off.

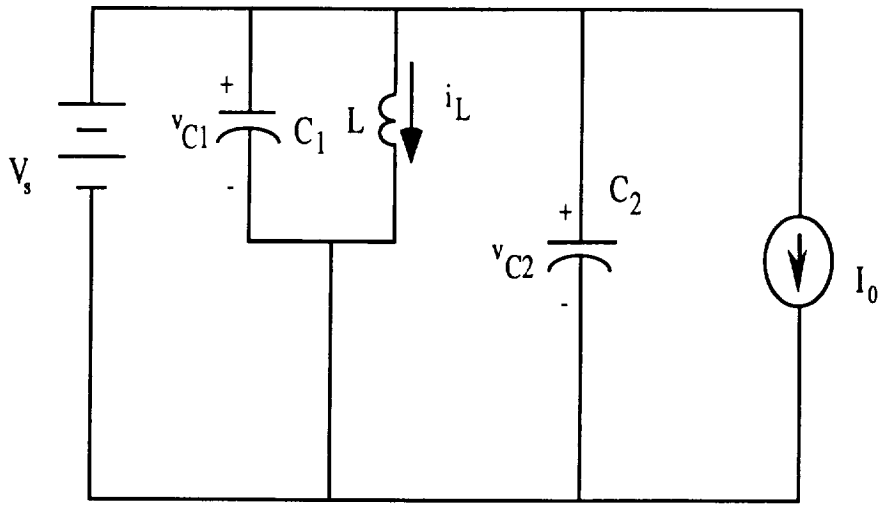

Figure 2.9. Equivalent Circuit for Mode V.

Mode VI [t_5, t_0+T_s]

The waveshaping circuit stays in the mode until the next command is received to turn on switch S_3. The source V_s is supplying energy through switch S_1 to the load. Both capacitors are charged up to the source voltage. The equivalent circuit for this mode is shown in Figure 2.10.

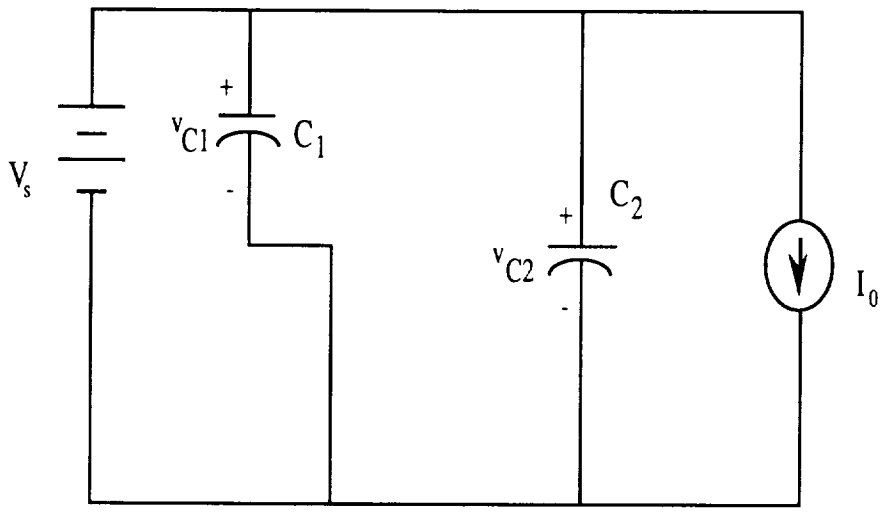

Figure 2.10. Equivalent Circuit for Mode VI.

The analyses of each mode may now be rearranged to produce a set of design equations for the ZVS inverter. Equations (2.11) and (2.14) give the length of Modes III and IV. The length of Modes I and V depends on the inductance L and the source voltage V_S.

$$t_1 - t_0 = \frac{L}{V_s} I_p \tag{2.17}$$

$$t_5 - t_4 = \frac{L}{V_s} I_0 \tag{2.18}$$

The length of Mode II, presented earlier in equation (2.6), may be rearranged as shown below

$$t_2 - t_1 = \frac{1}{\omega_1} \sin^{-1}\left[\frac{V_s}{V_s + 2Z_0 I_0}\right]. \tag{2.19}$$

where I_p has been eliminated.

Two other equations of interest relate I_p and I_{Lmax} in terms of other parameters. Equation (2.20) expresses I_{Lmax} in terms of V_S, Z_0, and I_0.

$$I_{Lmax} = \frac{V_s}{Z_0} + I_0 \tag{2.20}$$

The current I_p, which is the control level for the termination of Mode I, may also be expressed in terms of the same variables

$$I_p = \frac{V_s}{Z_0} \cot\left[\omega_1 (t_2 - t_1)\right] - I_0. \tag{2.21}$$

Examination of the previous equations indicates that there are many different variables to consider in the design of the ZVS inverter. For the design procedure presented here, many of the circuit quantities are expressed in terms of the inductance L and the time interval $t_{32} = t_3 - t_2$ of equation (2.11). Recall that

$$V_{C1max} = \sqrt{\frac{L}{C_1}} I_{Lmax} = \omega_2 L I_{Lmax} \tag{2.22}$$

Substituting equation (2.20) into (2.22) yields

$$V_{C1max} = \sqrt{\frac{L}{C_1}} I_{Lmax} = \frac{\sqrt{\frac{L}{C_1}}}{\sqrt{\frac{L}{C_1 + C_2}}} V_s + \omega_2 L I_0. \tag{2.23}$$

Equation (2.23) is modified by substituting for ω_2 from equation (2.11) and then rearranging

$$V_{C1max} = V_s \sqrt{1 + \frac{C_2}{C_1}} + \frac{\pi L}{t_{32}} I_0. \tag{2.24}$$

Note that V_{C1max} is now expressed in terms of V_S, L, t_{32}, and the ratio of capacitances C_2 and C_1. Define cratio = C_2/C_1. Equation (2.24) can now be rewritten as

$$V_{C1max} = V_s \sqrt{1 + cratio} + \frac{\pi L}{t_{32}} I_0. \tag{2.25}$$

Other circuit quantities can be expressed in terms of the same variables as V_{C1max}.

$$I_{Lmax} = V_s \sqrt{1 + cratio} \frac{t_{32}}{\pi L} + I_0 \tag{2.26}$$

$$Z_0 = \sqrt{\frac{1}{1+cratio}}\frac{\pi L}{t_{32}} \tag{2.27}$$

$$C_1 = \frac{1}{L}\left(\frac{t_{32}}{\pi}\right)^2 \tag{2.28}$$

The ZVS inverter may be designed using equations (2.11), (2.14), (2.17) - (2.19), (2.21), and (2.25) - (2.28). The set of design equations is completed with the addition of equations (2.29) and (2.30).

$$\omega_2 = \frac{1}{\sqrt{LC_1}} \tag{2.29}$$

$$\omega_1 = \frac{1}{\sqrt{L(C_1+C_2)}} = \omega_2 \frac{1}{\sqrt{1+cratio}} \tag{2.30}$$

Equations (2.25) and (2.26) relate the peak capacitor voltage and peak inductor current to V_S, I_0, cratio, t_{32}, and L. V_{C1max} determines the minimum voltage rating for switch S_2. I_{Lmax} determines the current rating for switch S_3 and influences the design of the inductor L. Since V_S and I_{0max} are usually specified for a system, cratio and the ratio of L to t_{32}, designated as (L/t_{32}), may be adjusted to reduce both of these values. Both V_{C1max} and I_{Lmax} are directly proportional to the square root of cratio. The variable cratio could be set equal to zero, which is equivalent to removing C_2 from the circuit. However, this capacitance is retained for filtering at the input to the three-phase inverter [7]. For the design described here, the variable cratio is arbitrarily selected to be 0.1.

One additional quantity which can be adjusted to reduce V_{C1max} and I_{Lmax} is the ratio L/t_{32}. To examine the effects of this ratio on V_{C1max} and I_{Lmax}, equations (2.25) and (2.26) are plotted in Figure 2.11 for V_S = 270 V, I_0 = 100 A, and cratio = 0.1. Note that

V_{C1max} increases linearly with L/t_{32}, while I_{Lmax} decreases with increasing L/t_{32}. A tradeoff exists between V_{C1max} and I_{Lmax}. Smaller values for V_{C1max} correspond to larger values for I_{Lmax} and vice versa. The design calculations presented in this report utilize a ratio (L/t_{32}) of 1. This is extremely difficult to achieve this ratio in actual practice, so the circuit was adjusted such that L/t_{32} was between 0.6 and 1.0.

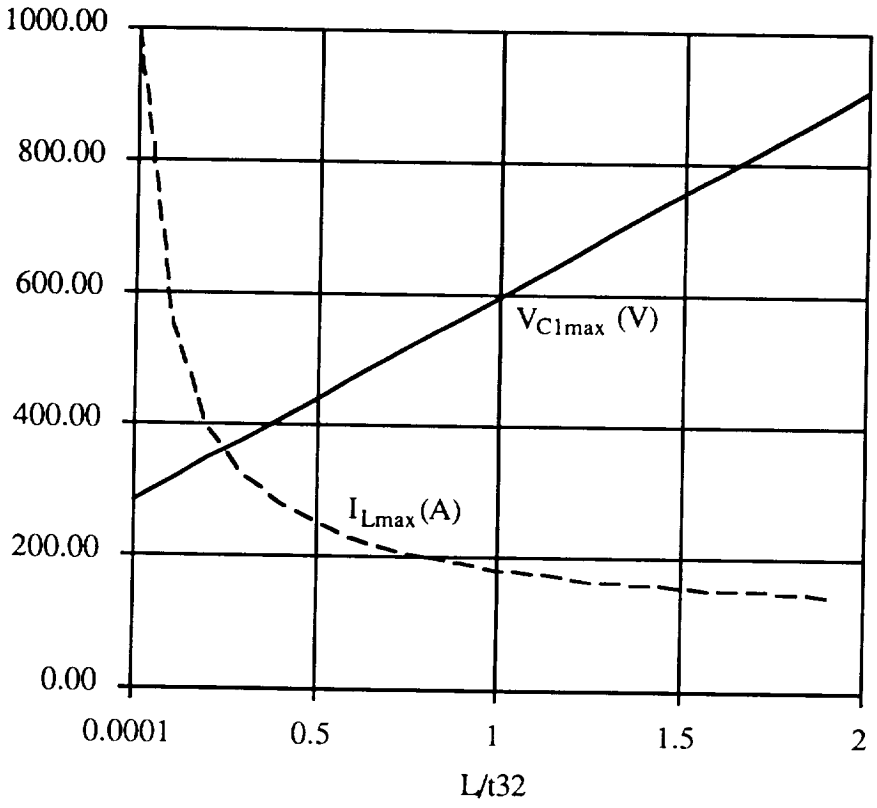

Figure 2.11. V_{C1max} and I_{Lmax} versus L/t_{32}.

Using cratio = 0.1 and L/t_{32} = 1, the circuit parameters may be calculated. The specified values for V_s and I_{0max} are 270 V and 100 A, respectively. A zero-voltage interval t_{32} of 5 μs is selected for these calculations.

$C_1 = 0.50\ \mu F$ $C_2 = 0.05\ \mu F$ $V_{C1max} = 597.3$ V $I_{Lmax} = 190.1$ A

$$I_p = 175.8 \text{ A} \qquad Z_0 = 3\ \Omega \qquad t_1 - t_0 = 3.26\ \mu s \qquad t_2 - t_1 = 0.527\ \mu s$$

$$t_4 - t_3 = 2.62\ \mu s \qquad t_5 - t_4 = 1.85\ \mu s$$

The interval t_5 - t_0 is the time required for the inverter input voltage to be taken to zero, clamped, and then returned back to V_S. Using the times calculated above, the length of this interval is 13.26 μs.

Using the circuit parameters calculated above, capacitor voltages v_{C1} and v_{C2} are plotted in Figures 2.12 and 2.13. Both voltages start at 270 V and begin to decrease after S_1 is opened. When they reach zero, v_{C2} is clamped at zero by the turn-on of S_r, while v_{C1} continues to decrease swinging down to negative V_{C1max}. Even though v_{C1} exceeds the input voltage of 270 V, capacitor C1 is not connected to the bus at this point because S_2 is open. Switch S_2 must have a voltage rating sufficient to withstand this voltage excursion. Switch S_r is opened and S_2 is closed when v_{C1} returns to zero. Both voltages increase toward the input voltage. The diode in anti-parallel with S_1 turns on when they reach the input voltage. Switch S_1 is now turned on at zero voltage. The inductor current during the operation of the PRDCL is shown in Figure 2.14. The current starts at zero and begins to increase with the turn-on of S_3. It reaches a peak value of approximately 190 A, which corresponds to the point where the voltages reach zero. During the interval where the inverter input voltage is clamped, it changes from I_{Lmax} to negative I_{Lmax}. When the current goes negative, it flows through the anti-parallel diode of S_3. This switch is now turned off at zero voltage before the current reaches zero and becomes positive.

Although cratio was selected to be 0.1 in order to reduce V_{C1max} and I_{Lmax}, this selection does have one drawback. Capacitor C_1 must carry about ten times more current than capacitor C_2. The capacitor currents are plotted in Figures 2.15 and 2.16. Note that the negative peak value of i_{C1} is approximately 260 A, while i_{C2} has a negative peak value of about 26 A. Using these waveforms, appropriate capacitors can be selected.

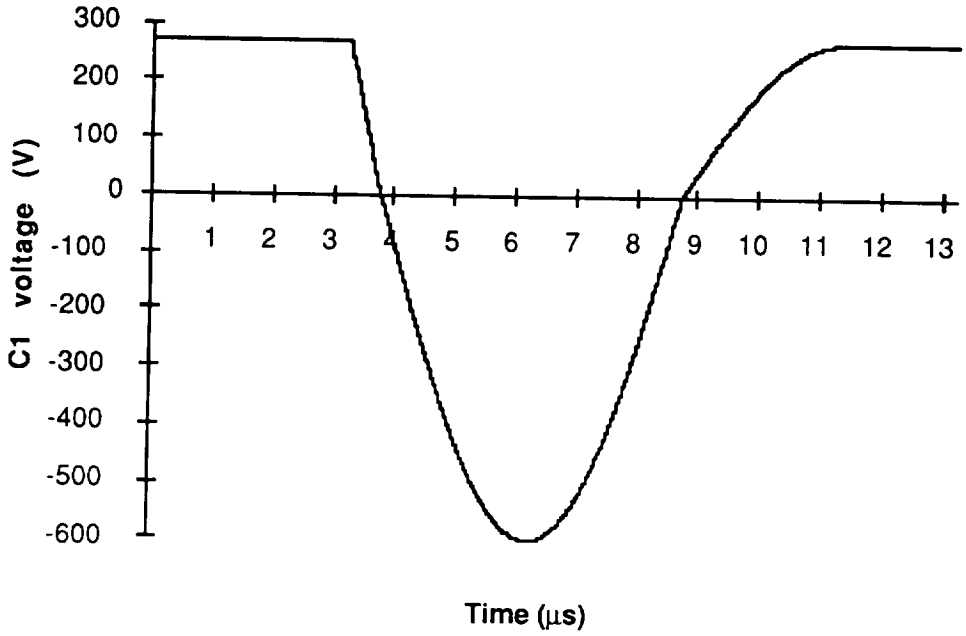

Figure 2.12. v_{C1} versus time.

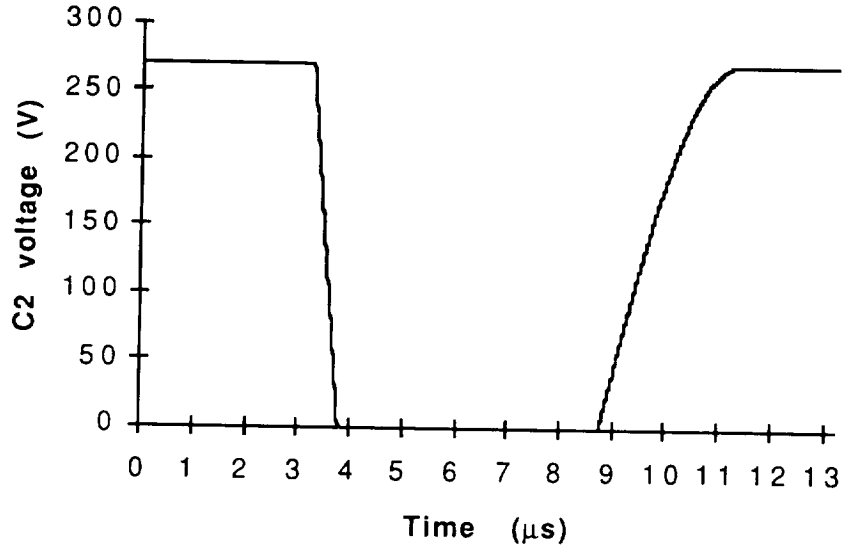

Figure 2.13. v_{C2} versus time.

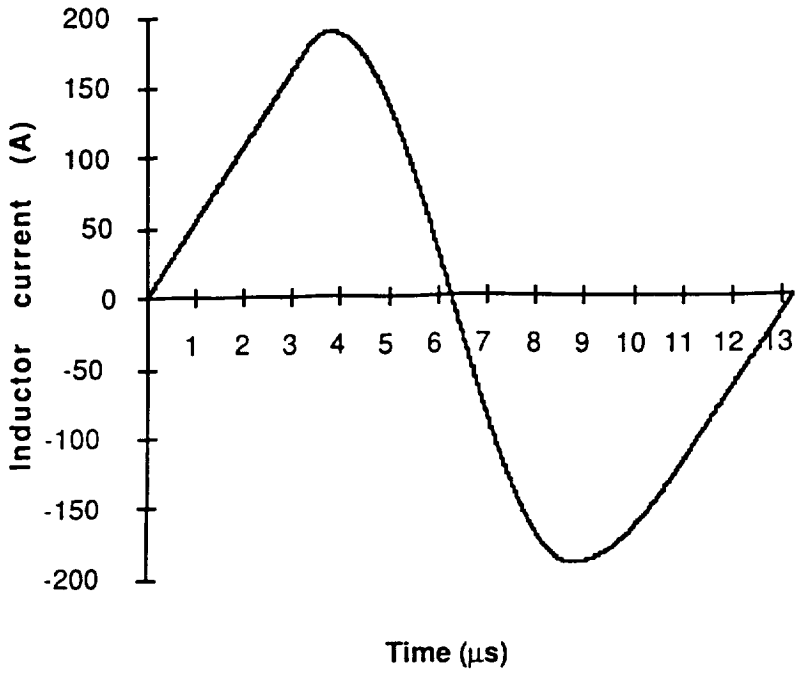

Figure 2.14. i_L versus time.

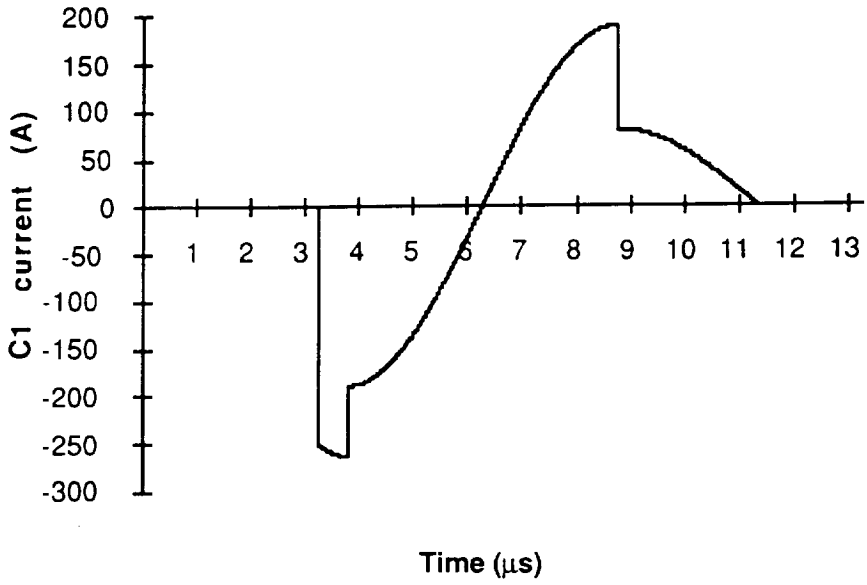

Figure 2.15. i_{C1} versus time.

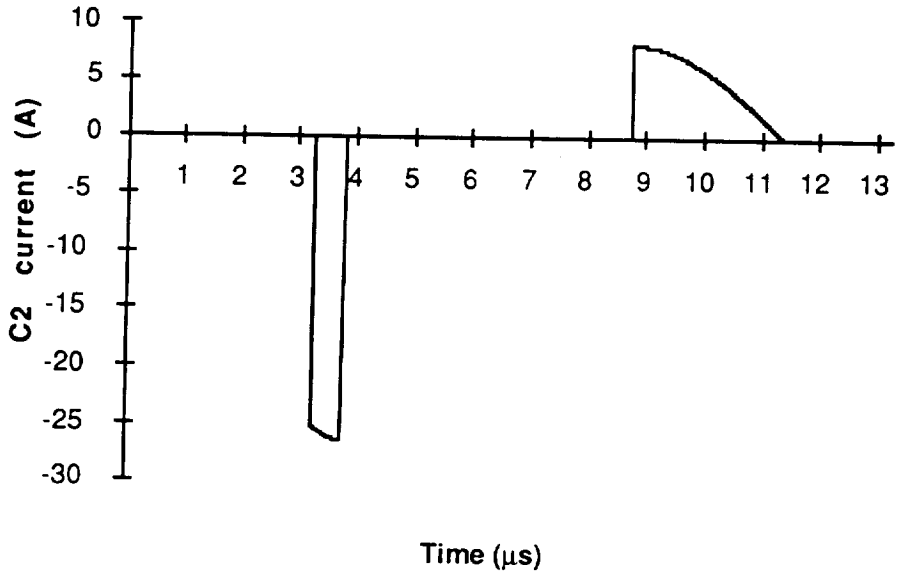

Figure 2.16. i_{C2} versus time.

Chapter 3

EXPERIMENTAL SETUP

The previous chapter discussed the operation and design of the ZVS inverter. This chapter will present the implementation of the circuit. Using waveforms calculated previously, components which are capable of operating under these conditions may be selected. The control algorithm and circuitry are also discussed in this chapter.

Inductor and Capacitors

The 5 μH inductor was designed using the inductor current waveform of Figure 2.14. Note that this inductor must be designed for high peak currents. Two Magnetics, Inc. powdered iron cores (Part. No. 58868-A2) are epoxied together and wrapped with nine turns of copper braided conductor.

The voltage and current waveforms for both capacitors are given in the previous chapter. Capacitor C_2 must have a voltage rating of a least 270 V. A Cornell-Dubilier DPPM10S47K polypropylene capacitor, which has a value of 0.047 μF, is selected for C_2. The voltage across C_1 has a positive value of 270 V and reaches a negative peak of approximately 600 V during the zero-voltage interval t_{32}. It also must be capable of carrying very large currents as seen in the plot of Figure 2.15. A General Electric 97F8585 capacitor is employed for C_1. This capacitor has a capacitance of 0.5 μF and a voltage rating of 1000 V.

Semiconductor Devices

Switches S_1, S_2, S_3, and S_r are implemented with Insulated Gate Bipolar Transistors (IGBTs). S_1, S_3, and S_r must have a voltage rating of at least 270 V. The voltage rating of S_2 is related to the value of V_{C1max}. The largest current for S_1 is the

maximum inverter current (100 A) plus the value of I_p, which is 175.8 A for this design. The frequency at which S_1 sees this peak current depends on how often the switches in the three-phase inverter are required to switch. Operation in the six-step mode requires that some of the inverter switches change status every one-sixth of a cycle. The RMS value of the current through S1 is less for this case than the case where the current is being regulated by a scheme such as PWM because more inverter switchings will occur. As a margin of safety, an IGBT with a current rating of 300 A could be used for this switch.

Switch S_2 is turned on during all modes except Mode III. The largest current that it must conduct is the current I_p. As was the case for S_1, this switch experiences this current at a low duty cycle; therefore, it can be rated at some current level less than the peak value. A 200 A device would be more than acceptable for this application. The remaining switch is S_3, which conducts the inductor current. From Figure 2.14, it can be seen that the peak current is approximately 190 A. An IBGT with a current rating of 200 A could easily be utilized for S_3 because of the low duty cycle for the inductor current.

Powerex IGBTs were selected for the experimental setup. At the time of purchase, only 600 V devices with current ratings of 400 A were readily available. These devices were purchased and used for S_1, S_3, and S_r. Switch S_2 was implemented with a 1200 V, 300 A device.

Block Diagram for the PRDCL circuit

Figure 3.1 is a block diagram for the PRDCL circuit. Note that the voltage across C_2 is measured and fed into a zero voltage detector. This detector determines when this voltage reaches zero so that the turn-off of S_2 and the turn-on of S_r can be synchronized to the zero crossings. A 555 timer, which is operated in the monostable mode, connected to the drive circuit for S2 determines when S_2 is turned back on and S_r is turned off.

Turn-on of S_3 is initiated by the link trigger signal. This signal is generated by the control circuitry for the three-phase inverter. Recall that proper operation of the PRDCL

requires measurement of the inductor current. This is accomplished with a Hall effect current sensor. Current sensors manufactured by F. W. Bell, Co. (part no. ID-5031-M) and Honeywell Microswitch (part no. CSLA1DK) have been utilized in the prototypes. S_1 remains on until the inductor current reaches I_p. It can be seen in Figure 3.1 that the output of the current sensor is connected to a voltage detector which provides a signal to turn off S_1 when the current reaches the desired level. The turn-on signal for S_1 is provided by the 555 timer connected to the drive circuit. This timer is operated in a monostable mode. It is triggered by the current sensor output, and its output does not change for time interval determined by external components such as resistors and capacitors. The turn-on of S_3 is also achieved with a 555 timer.

System Block Diagram

A block diagram for the system is shown in Figure 3.2. The PRDCL circuit is attached to the three-phase inverter in this diagram. The drive signals for switches S_1, S_2, and S_3 are provided by the resonant link controller of Figure 3.1. The link controller has two inputs. The first is a measurement of the current flowing through the inductor in the PRDCL, which determines when S_1 is opened. The second input is provided by a differentiator. Recall that the PRDCL receives a signal from the inverter before it begins the process of ringing the inverter input voltage to zero. This differentiator provides that signal by monitoring the output of the current controller and the output of the LM621 integrated circuit. The LM621, manufactured by National Semiconductor, decodes the Hall effect signals from the brushless dc motor to provide drive signals for the switches in the three-phase inverter.

When the three-phase inverter operates in the six-step mode, all of the drive signals are provided by the LM621. The Hall effect signals are decoded to determine the status of the six inverter switches. Only two inverter switches are conducting at any time: one of the top three and one of the bottom three. Two switches in the same inverter leg (i.e. T_1 and

T_4) are not allowed to conduct at the same time. Switches T_1 and T_5 conduct for a one-sixth of a cycle followed by the conduction of T_1 and T_6 for the next one-sixth of a cycle.

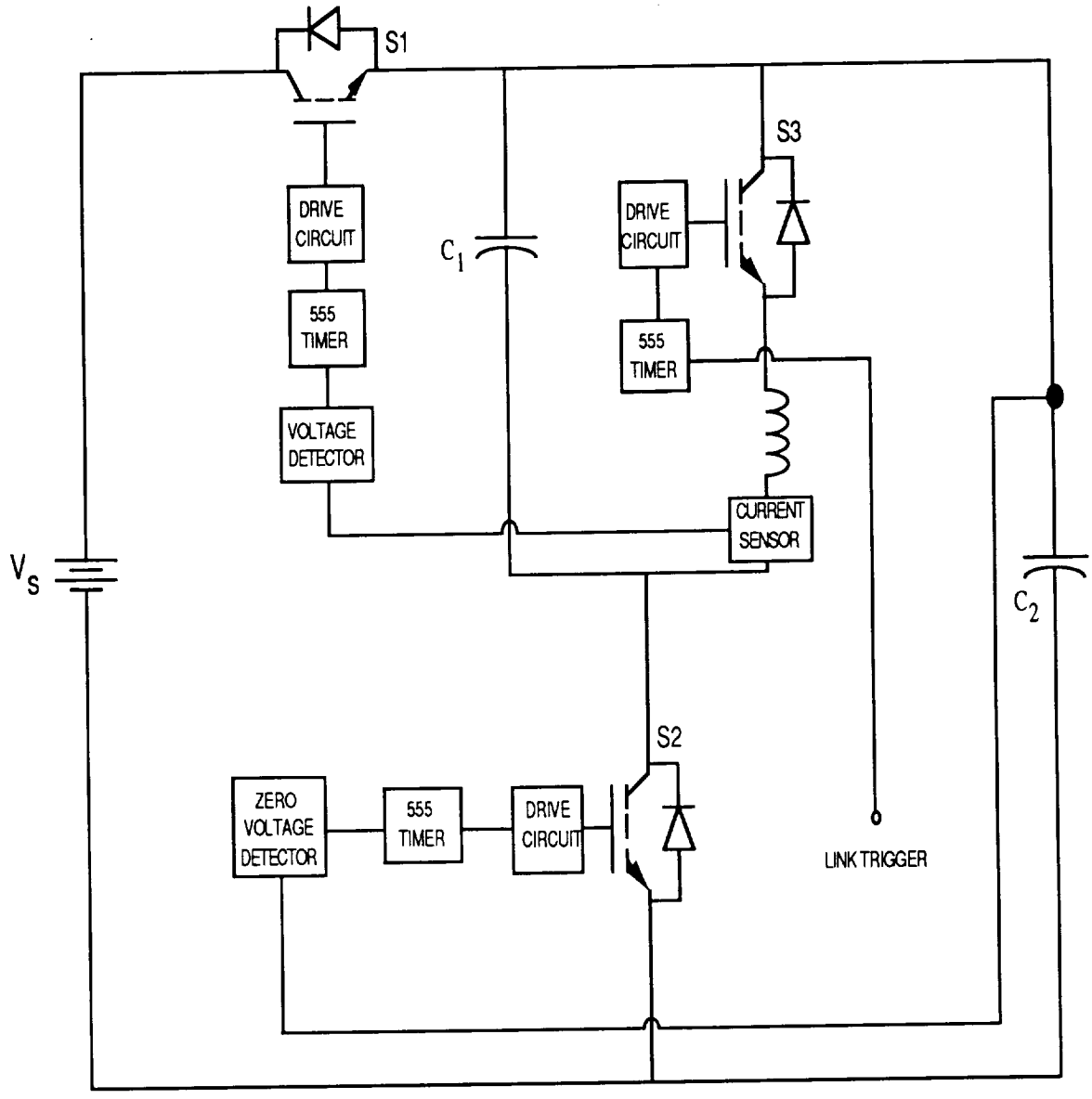

Figure 3.1. Block Diagram for the PRDCL Circuit.

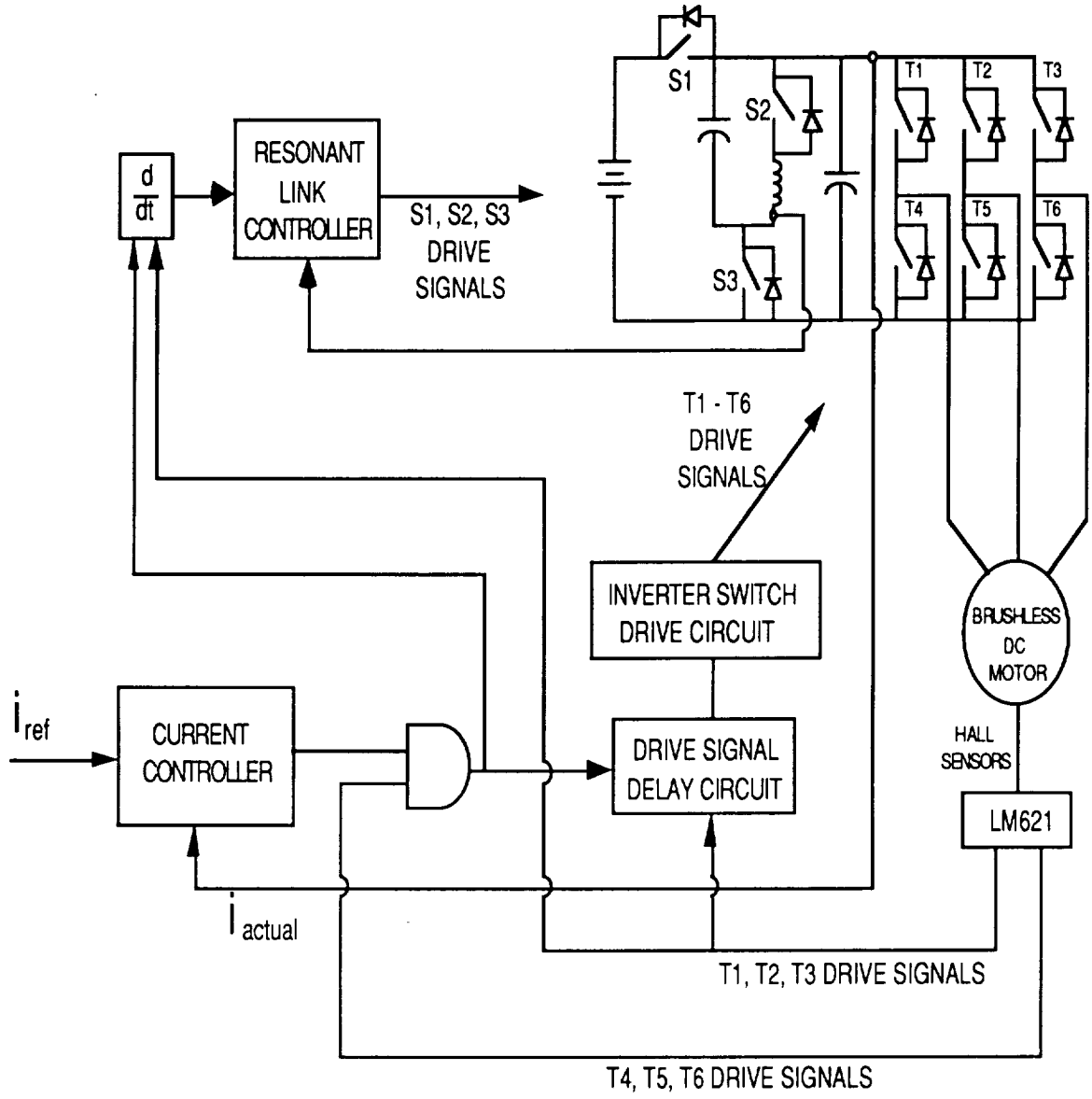

Figure 3.2. System Block Diagram.

Regulation of the current flowing in the brushless dc motor is achieved via the current controller of Figure 3.2. During six-step operation, two of the inverter switches are closed at a time. Of the two switches closed, the bottom switch is toggled on and off to control the current. When the actual current is below the reference current, the bottom switch is turned on causing the actual current to increase. When the actual current exceeds the reference current, the bottom switch is turned off causing the current to decrease due to the back emf of the motor. This procedure is illustrated in Figure 3.3.

The motor current must be measured so that it can be an input to the current controller. All three motor currents could be measured using current sensors. As an alternative, two of the three currents could be measured and a signal proportional to the third, unmeasured current could be synthesized using operational amplifiers. Another approach has been implemented in this experimental setup. Instead of measuring any of the motor currents, the inverter input current is measured as can be seen in Figure 3.2. This current is equal to the motor current when two of the switches, one from the top and the other from the bottom, are conducting. When the bottom switch is toggled off, the inverter input current is not equal to the motor current but falls to zero. A fixed time delay is inserted into the system to prevent the bottom switch from being turned back on almost instantaneously due to the measured current being zero. This time delay is designated as Δt in Figure 3.3. The amount of time delay is determined by such quantities as the motor inductance and probably will vary from system to system.

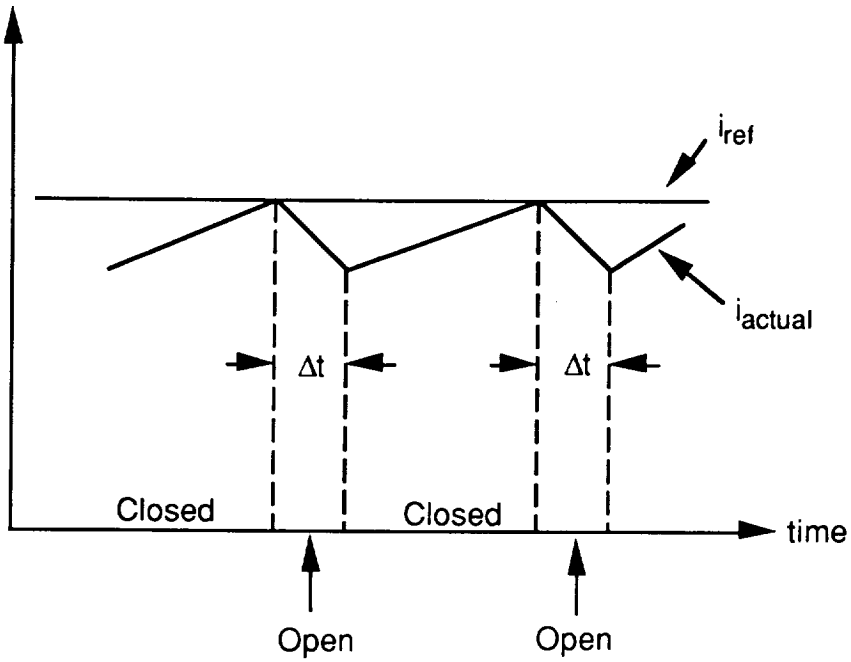

Figure 3.3. Diagram of Current Control Algorithm.

Chapter 4

EXPERIMENTAL RESULTS

This chapter will discuss experimental results obtained using the setup described in the previous chapter. Two experimental setups have been constructed at Auburn University. One of these will be referred to as the AU controller. It was tested in the laboratory at Auburn University and uses different component values from those described earlier in this report. The second controller, referred to as the MSFC controller, was constructed using earlier calculated component values. It was tested in the EB24 laboratory at Marshall Space Flight Center during the week of August 23 - 26, 1994.

AU Controller

This controller supplied a Reliance Electric brushless dc motor which has the following ratings:

Rated power - 5 Hp

Rated speed - 4000 RPM

Rated current - 30 A

Rated voltage - 270 V

Commutation signals are provided by Hall effect sensors. This motor is loaded by a 4.5 kW DC generator connected in a separately-excited configuration. The field circuit for the generator was supplied by a variable DC supply. A variable resistance was connected to the generator armature terminals. The output power of the DC generator could be varied via the variable field supply or by changing the resistance.

The input voltage for the AU controller was provided by rectifying the output of a variable AC supply. The range of input voltages was 0 - 100 V. The inductance in the waveshaping circuit was 114 μH. In contrast to the MSFC controller, $C_1 = C_2 = 0.1$ μF

for the AU controller. All of the IGBTs in the PRDCL circuit and three-phase inverter are International Rectifier IRGPC40U with ratings of 600 V and 40 A. All diodes are Motorola 1N3913.

Figure 4.1 is a plot of the voltage v_{C2} (which is the voltage at the terminals of the three-phase inverter) and the inductor current for an input voltage of approximately 70 V and a load current I_0 of approximately 3 A. Note that the voltage is clamped at zero for slightly more than 10 μs. When S_3 is closed, the inductor current increases linearly until I_p is reached at which time S_1 is opened. The glitch on the inductor current corresponds to the opening of S_1 at a current of about 5 A. The inductor current reaches a positive peak value of appoximately 5.5 A, goes negative, and then returns to zero. The current completes its cycle in about 36 μs.

Various circuit quantities can be calculated using the equations of Chapter 2 and compared with those obtained from the oscilloscope trace of Figure 4.1. The calculated values are as follows:

$$I_{L\max} = 5.92 \text{ A}$$
$$I_p = 5.43 \text{ A}$$
$$t_1 - t_0 = 8.84 \ \mu\text{s}$$
$$t_2 - t_1 = 1.6 \ \mu\text{s}$$
$$t_3 - t_2 = 10.6 \ \mu\text{s}$$
$$t_4 - t_3 = 7.5 \ \mu\text{s}$$
$$t_5 - t_4 = 4.9 \ \mu\text{s}$$
$$t_5 - t_0 = 33.44 \ \mu\text{s}$$

The calculated values for I_{Lmax} and I_p are less than their corresponding measured values, while the measured value of $(t_5 - t_0)$ is larger than the calculated value.

Zero-voltage switching of the IGBTs in the three-phase inverter is illustrated by simultaneously monitoring v_{C2} and the drive signal for one of the IGBTs. In Figure 4.2, the top trace is v_{C2} while the bottom trace is a drive signal. A 15 V level indicates that the IGBT is now on. It can be seen in this figure that the drive signal does not change to the 15 V level until the voltage reaches zero. The turn-off of the IGBT also occurs at zero voltage as can be seen in Figure 4.3. The top trace is the voltage v_{C2} and the bottom trace is the drive signal. The transition from the 15 V level to zero, which indicates that the IGBT is off, does not occur until the voltage in the top trace has reached zero.

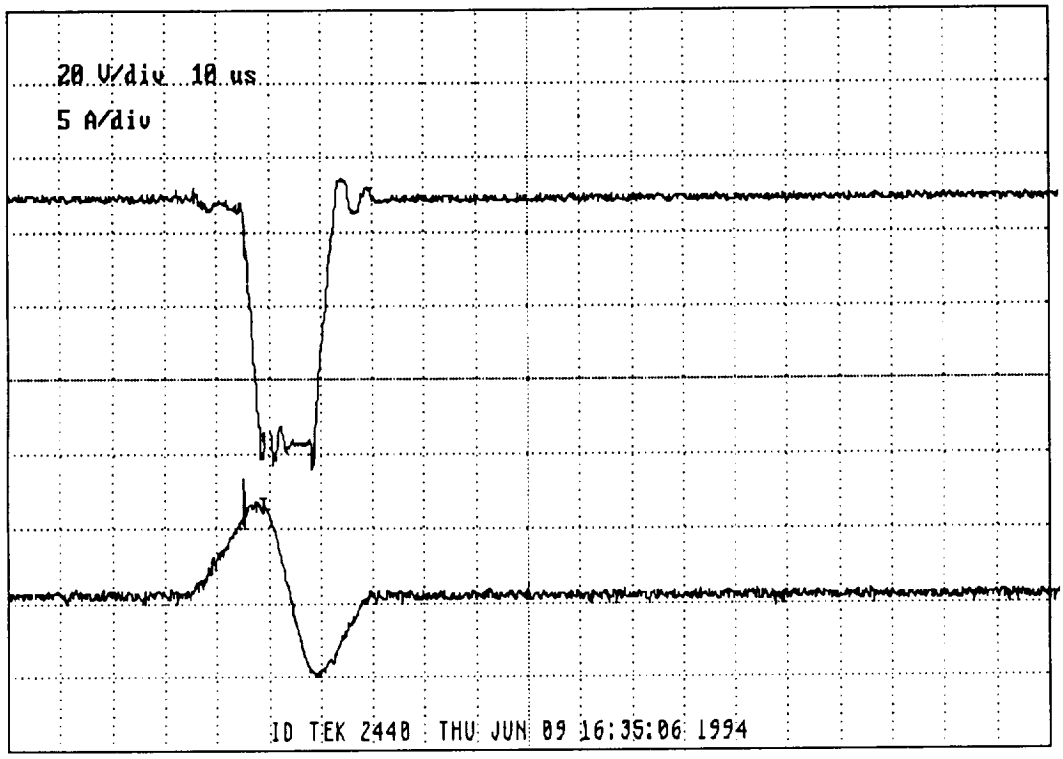

Figure 4.1. Voltage v_{C2} (top) and Inductor Current (bottom) vs. Time for 70 V Input.

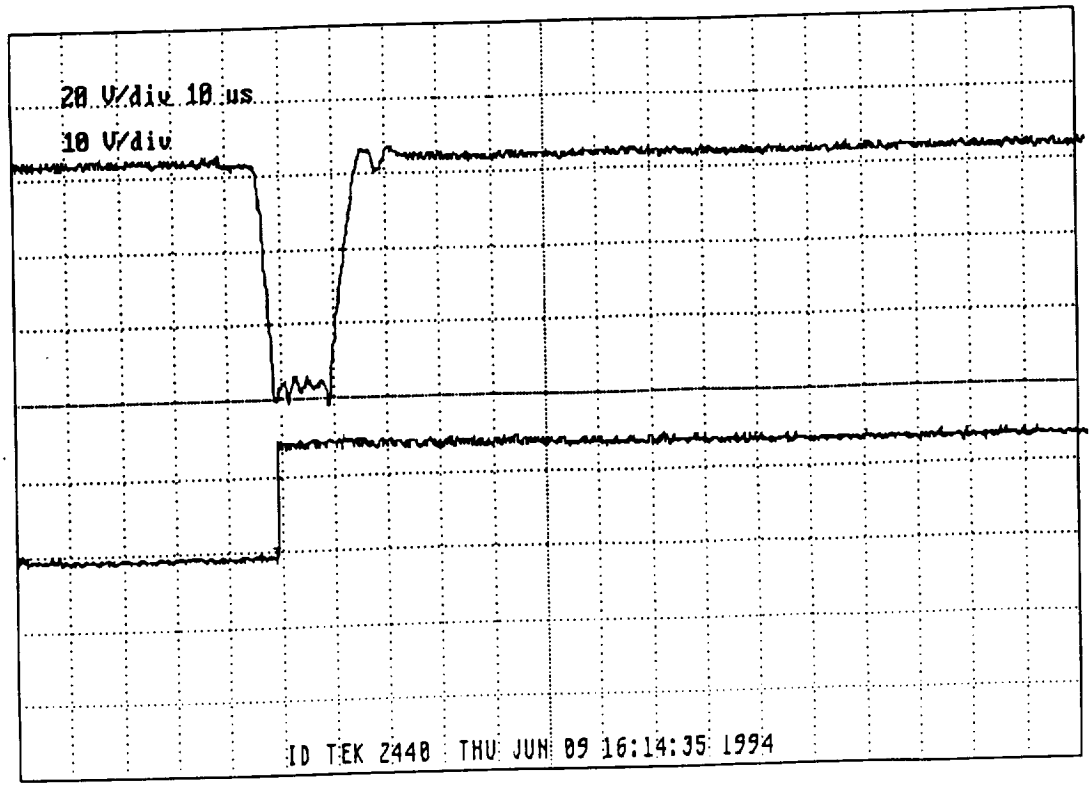

Figure 4.2. Voltage v_{C2} (top) and IGBT Drive Signal (bottom) vs. Time at Turn-on.

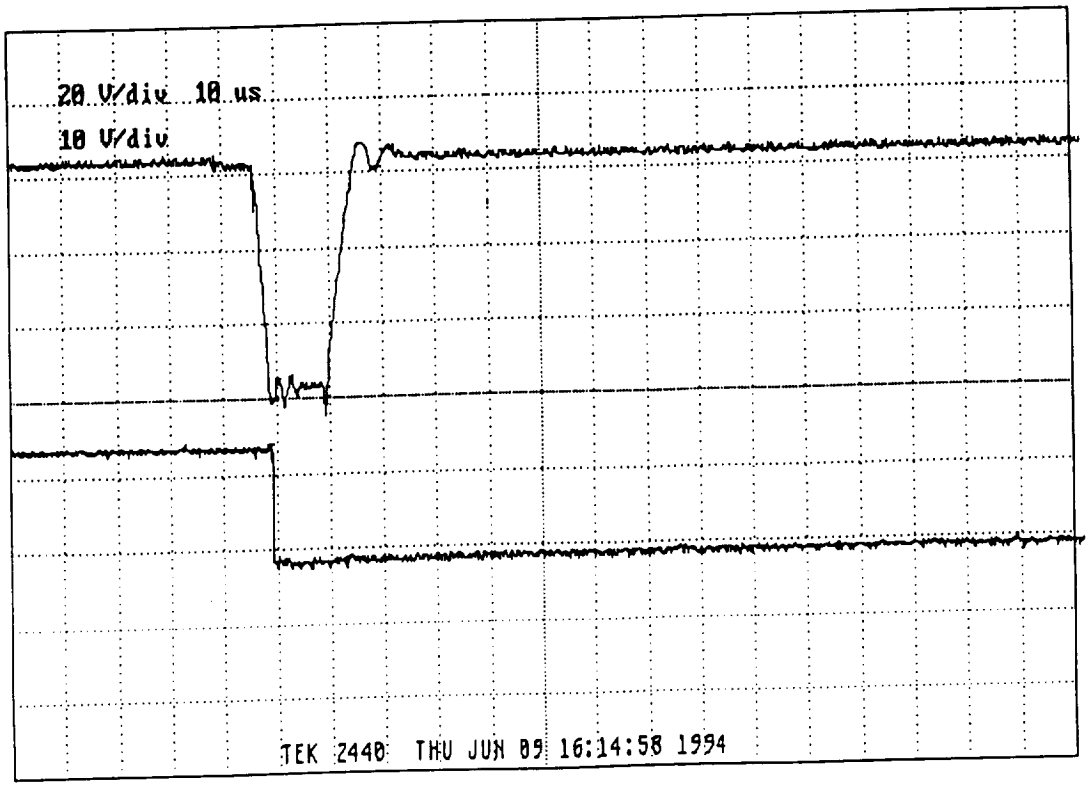

Figure 4.3. Voltage vC2 (top) and IGBT Drive Signal (bottom) vs. Time at Turn-off.

The current control scheme discussed in the previous chapter is illustrated by the waveforms in Figure 4.4. Both of the waveforms were captured for an input voltage of 50 V and an inverter input current of approximately 4 A. The top trace is v_{C2} and the bottom trace is the current I_0. Recall that two switches in the inverter are conducting at any time - one top switch and one bottom switch. When the current reaches a value of approximately 4 A, the bottom switch is turned off. This is indicated by the current dropping to zero. This switch remains off for a predetermined amount of time as discussed earlier. For this case, the switch remains off for about 50 μs. During the time that the bottom switch is off, the current flowing in the motor is decreasing due to the motor's back emf. With the turn-on of the bottom switch at the end of the 50 μs interval, the inverter input current again equals the current flowing in the motor and begins to increase slowly.

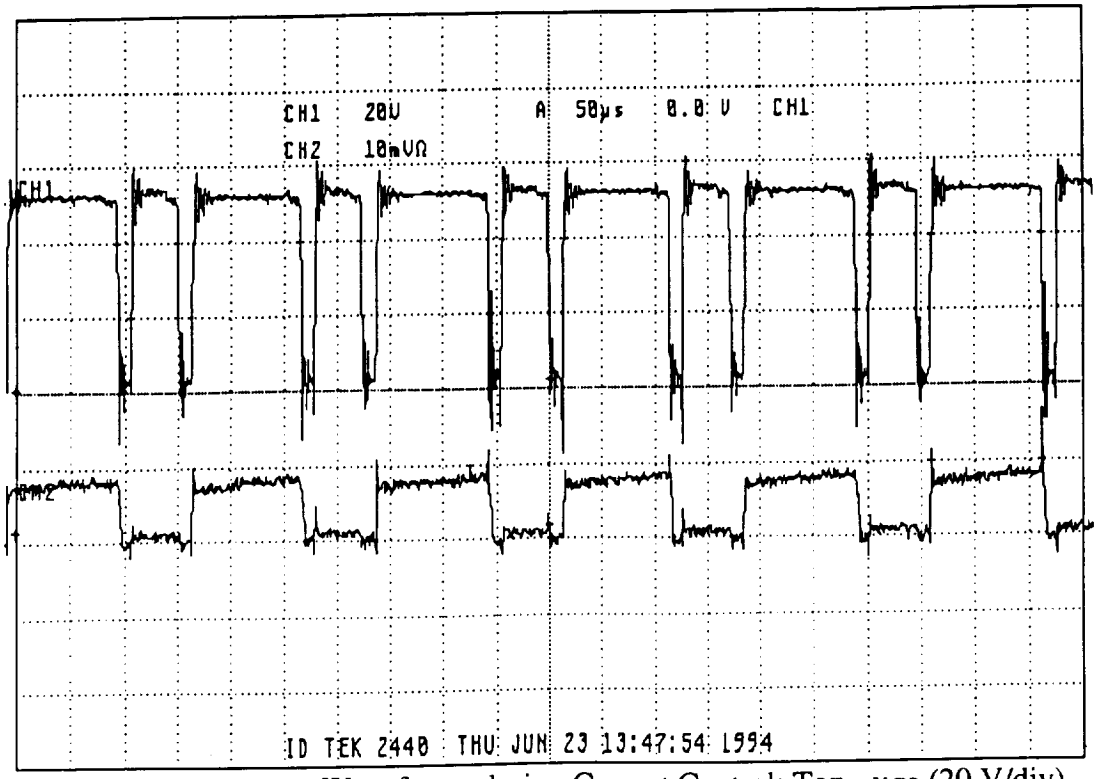

Figure 4.4. Inverter Waveforms during Current Control: Top - v_{C2} (20 V/div), Bottom - Inverter Input Current (5 A/div).

MSFC Controller

The circuit parameters for this controller were calculated in Chapter 2. The implementation of the controller was discussed in Chapter 3. Two printed circuit boards were designed and fabricated to interface the ZVS inverter to the test setup in the EB24 laboratory at MSFC. One of the circuit boards controlled the PRDCL circuit, and the other board contained control circuitry associated with the three-phase inverter such as the LM621 brushless dc motor hall effect signal decoder and the current controller. The circuit schematic for the two boards is not included in this report because of the circuit size and complexity. They have been provided to MSFC personnel on a floppy disk and on D size plotter paper.

The controller was successfully tested during the week of August 23 - 26, 1994 at the MSFC EB24 laboratory. All tests were performed at low voltage. The brushless dc motor used in the tests was connected to a dynamometer which permitted testing with different steady-state load levels and under transient conditions produced by the sudden application and removal of the load.

Chapter 5

CONCLUSION

The EMA systems proposed for future space transportation applications are high power systems operating at voltages up to 270 Vdc and at current levels on the order of hundreds of amperes. The position of the actuator is controlled by modulating the flow of energy from the source to an electric motor with an inverter. Hard-switching of the semiconductor devices in the inverter results in considerable device switching stresses and losses and in the generation of substantial amounts of EMI. Both of these can be reduced by employing zero-voltage-switching techniques in the inverter. This project has focused on the development of a ZVS inverter for the Marshall Space Flight Center EMA prototypes, which utilize brushless dc motors to convert electrical energy to mechanical energy.

An inverter which permitted zero-voltage switching and a quasi-PWM operation was selected for study and implementation. A waveshaping circuit is added to the front of a standard three-phase inverter to achieve the desired switching properties. This circuit causes the input voltage of the three-phase inverter to ring to zero where it is clamped for a short period of time. During this zero-voltage period, any of the semiconductor switches in the three-phase inverter are switched on or off at zero voltage resulting in a reduction in switching losses and EMI. The operation of this waveshaping circuit and its interaction with the three-phase inverter were described in chapter 2. The different circuit modes were analyzed using equivalent circuits. Based on this analysis, design relationships were developed for calculating component values for the circuit elements in the waveshaping circuit. Waveforms of various voltages and currents in the waveshaping circuit were plotted and used to determine the ratings of the semiconductors in the waveshaping circuit. The implementation of this inverter was described in chapter 3. Block diagrams for the

overall control system and the waveshaping circuit control were presented and discussed. The current control scheme employed in the controller was also described. Experimental results from two controllers were discussed in the previous chapter.

Both of the controllers implemented for this project worked satisfactorily in the laboratory. However, the present implementation could be improved. First, an LM621 brushless dc motor decoder chip is utilized to decode the Hall effect signals from the motor. This chip has been discontinued by its manufacturer, National Semiconductor. Future designs should use alternate technologies such as those employed by personnel in EB24 at MSFC. Secondly, the current controller or current control loop needs to be redesigned. The present scheme employs measurement of the inverter input current only. This current is the same as the motor phase current when two of the switches, one top and one bottom, are conducting. When this current reaches the desired current level as determined by the control loop, the bottom switch is turned off. During this time, the inverter input current is no longer equal to the motor phase current but drops to zero. The bottom switch remains off for some predetermined time before being turned on again. Future implementations should monitor at least two of the individual motor phase currents. A signal proportional to the unmeasured motor phase current can be produced by taking the negative of the sum of the two measured currents. The use of a tolerance band in the current regulator would eliminate the current offset which results from switching when the current reaches the commanded level. The third improvement would be a redesign of the control circuitry to reduce the tuning requirements. In its present form, the controller implementation requires too much circuit tuning to provide acceptable operation.

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