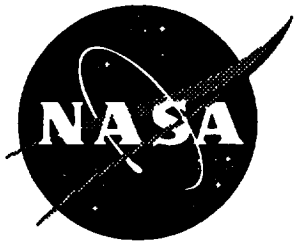
NASA Contractor Report 198165



Advanced Flight Computer

Special Study Final Report

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National Aeronautics and
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Langley Research Center
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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

AD, ADI	Analog Devices, Inc.
AFC	Advanced Flight Computer (NASA program)
AISM	Advanced Insertion of Standard Microelectronics (Phillips Lab program)
ASCM	Advanced Spaceborne Computer Module (Phillips Lab program)
ASPS	Advanced Spaceborne Processor Subassembly (Space Systems Loral)
ATIM	Advanced Technology Insertion Module (ASCM follow–on)
BEOL	Back–end–of–the–line VLSI fabrication phase
BiCMOS	Bipolar–CMOS
CFP	Ceramic Flat Pack
DMA	Direct Memory Access
DoD	Department of Defense
DSP	Digital Signal Processor
ECC	Error Correction Code
ECL	Emitter–Coupled Logic
FP	Flat Pack
GaAs	Gallium Arsenide
GVSC	Generic VHSIC Spaceborne Computer (Phillips Lab program)
HDI	High Density Interconnect
HMC	Hermetic Memory Card
IBM	International Business Machines Corporation
JTAG	Joint Test Action Group
LaRC	Langley Research Center (NASA)
L_{eff}	Effective Channel Length of a Transistor Gate
LOCOS	Locally Oxidized Silicon
MCM	Multi–Chip Module
MESI	Modified, Exclusive, Shared, Invalid cache coherency states
NASA	National Aeronautics and Space Administration
PBEOL	Planar Back–end–of–the–line VLSI fabrication method/phase
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect bus
POWER	Performance Optimized With Enhanced RISC (IBM architecture)
PPC	PowerPC
PVS	PowerPC Visual Simulator
QFP	Quad Flat Pack

RAD6000 –SC/–MC	Radiation hardened RISC System/6000 CPU, –Single Chip / –Multi Chip
RHCMOS	Radiation Hardened CMOS
RHSRAM	Radiation Hardened SRAM
RSC	IBM RISC System/6000 Single Chip CPU
SBC	Single Board Computer
SCM	Single Chip Module
SEU	Single Event Upset
SiO_2	Silicon Dioxide
SOA	State–of–the–art
SOG	Sea of Gates design method
SOI	Silicon On Insulator
SOP	State–of–the–practice
STI	Shallow Trench Isolation
TI	Texas Instruments Corporation
TSOP	Thin Small Outline Package
UTMC	United Technologies Microelectronics Center
VCOS	Loral VLSI Chips On Silicon multi–chip module
VLSI	Very Large Scale Integration
XCVR	Transceiver

EXECUTIVE SUMMARY

The Advanced Flight Computer (AFC) is a NASA effort to define and develop a 32–bit radiation hardened, SEU tolerant flight computer module which significantly reduces power, weight, and volume when compared with current approaches, while maintaining or increasing throughput and memory capacity. The AFC is intended for flight qualifiable readiness in 1998, with potential use in missions beginning in 2000. Demonstrable prototypes would be available in 1995–96, including full function brassboard(s) and tools, with a clearly defined low–cost, low–risk path to final packaging and flight qualification.

The purpose of this report is to document the results of a special study conducted by Loral Federal Systems – Manassas for NASA Langley Research Center (LaRC), to define an AFC architecture and to investigate current or near–term technologies and development efforts that contribute to the AFC design and development.

The special study consisted of the following task elements:

Architecture: Define a highly modular computer architecture initially suitable for fault tolerant processing as a single computer node, with provisions for future multi–node applications. Address task distribution, task partitioning (node coupling), and multi–tasking for multi–node applications.

VLSI Technology: Define a set of VLSI parameters and/or characteristics which are essential in the development of a specification for the Advanced Flight Computer. Specifically examine the use of SOI and/or other technologies for increasing device densities, including device layout. Also evaluate reduced voltage technologies and system logic level threshold margins.

Packaging: Define the packaging approach required to achieve the 1998–2000 AFC performance goals, as listed in Table 1. Study the application of three dimensional and other high density packaging technology for logic and memory circuits.

Other tasks include: Development of a high–level plan for the AFC which supports the schedule goals through 2000; Identification of required trade studies; and study reports.

Table 1. Advanced Flight Computer 1998 Performance Goals

Power Consumption	2–8 Watts
Weight	0.2 pounds
Volume	4 cubic inches
Performance	3–5 MIPS/Watt
Throughput	10–40 MIPS
Local Memory	1 MByte minimum
I/O	1 interface minimum, such as 1553B or 1773
Test Interface	To be defined

The AFC baseline is to build on state–of–the–art 32–bit commercial and/or current DoD development programs, in order to ensure cost–effective transfer of technology into future space missions. The AFC should not require new instruction set architecture development, relying on commercially available Ada, C, and software development tool suites.

In addition to the task requirements above, initial baselines were established to control the scope of this study. For the architecture study task, two processors were used in defining the processor node: the IBM/Motorola PowerPC 604 was chosen for general purpose embedded command and control applications, while the Analog Devices AD21060 was chosen for signal processing applications. The latter was included late in the study at the request of NASA LaRC to address AFC suitability for earth science and remote sensing payload applications.

One goal of this study was to define an AFC architecture whose technologies could be demonstrated in prototype development in 1996, with actual AFC development and build in 1998 for flight operations in the year 2000. The PowerPC 604 and AD21060 processors were chosen in part because they represent the anticipated state–of–the–art processing capabilities for space applications during these time frames. These processors are part of the near–term technology transfer plans for Loral Federal Systems Manassas. Loral has an established capability of transferring commercial designs to the radiation–hardened CMOS fabrication process at Manassas. For instance, Loral already has transferred and developed flight solutions for the RAD6000, a single– and multi–chip line of radiation hardened flight processors that are identical in design, function, and performance to the IBM RISC System/6000 CPU architectures. Loral is currently under contract negotiations for Phil-

lips Laboratory's Advanced Insertion of Standard Microelectronics (AISM) program, to develop a rad–hard version of Analog Devices' AD21020 digital signal processor. Development and flight units using the RAD6000–SC (single chip) and rad–hard AD21020 represent the prototype demonstrations during the 1996 time frame.

In addition, Loral currently has or is developing advanced packaging solutions for space applications. These include 3D memory cubes (working with Irvine Sensors and IBM Microelectronics), VLSI Chips on Silicon (VCOS) multi–chip modules, and innovative hermetic packages for stacked memory chips. These capabilities form the initial baseline for the scope of this study.

To achieve the 1998–2000 AFC weight and volume goals, highly integrated modules are needed. The approach for this study was to define modular processing nodes, each node consisting of a set of multi–chip modules that provide processing, global memory, and I/O functions. These multi–chip modules were defined in the architecture study task, and trade studies were conducted during the packaging study task on various packaging alternatives for each module. The VLSI technology study task evaluated radiation hardened CMOS and other fabrication technologies, with respect to projected architectures and commercial products that are or will become available during the AFC 1998 development time frame.

This study defined an AFC processing node that consists of a processor MCM and an I/O MCM. An additional global memory MCM may also be added to the node. The processor MCM may be a general purpose command and control CPU (in this case, the rad–hard PowerPC 604), or a signal processing MCM with multiple digital signal processors (in this case, up to four rad–hard AD21060 DSPs). The I/O MCM may have one or more of any number of standard interfaces, including MIL–STD–1553B, 1773, high–speed serial, etc. For this study, a 1553B interface was used as a worst case representative with respect to the AFC performance goals. Stacked memory die was used to achieve the 1 MByte local memory density on the processor MCM. This 3D packaging approach was also used for the global memory MCM to maximize density for the multi–chip module package. The packaging study task showed that it is feasible to develop these defined MCMs on a standard 2.1 inch square multi–chip module package.

The VLSI technology study task identified the following parameters and/or characteristics essential to the development of an AFC specification: Feature size, Technology type, Voltage level, Number of wiring levels, Device isolation, Radiation hardness. Compatibility with commercial VLSI process was identified as a desirable but not essential feature, due to the increasing reliance on commercial development for space applications. These features showed that the AFC 1998 goals could be met with technology that would be available in the 1996 time frame.

The AFC processing node architecture defined in this study is feasible in the 1998 time frame. On–going development activity today that involves RAD6000–SC flight computers, additional commercial technology transfer, 3D memory packaging, and other advanced packaging techniques, will lead to demonstrable prototypes for the AFC architecture by 1996. The MCM building block approach used to define the AFC processing node was chosen due to its existing industry support, and because it presents a realistic low–risk, low–cost solution to achieving the AFC performance goals in 1998 and beyond. Current VLSI technology trends show that AFC 1998 goals can be met with mostly 3.3 V rad–hard CMOS processes. SOI is not essential for AFC during this time frame, but other technologies are necessary to achieve higher data transfer rates for earth science and remote sensing applications. Additional trade studies identified for AFC include: cost, yield, and manufacturability issues for the various packaging alternatives; beyond–2000 AFC goals versus radiation hardened CMOS capabilities; advanced 3D packaging (i.e., stacking) for multi–chip modules to achieve higher integration.

1. OVERVIEW

This report documents the special study conducted by Loral Federal Systems – Manassas for NASA LaRC, to define a 32–bit radiation hardened, SEU tolerant flight computer architecture, and to investigate current or near–term technologies and development efforts that contribute to the Advanced Flight Computer (AFC) design and development. The AFC is intended for flight qualifiable readiness in 1998, with potential use in missions beginning in 2000. A full function brassboard with a clearly defined low–cost, low–risk path to final packaging and flight qualification would be prototyped in the 1995–96 time frame and show intermediate progress toward 1998 capability.

The requirements for the Advanced Flight Computer are that it should build on state–of–the–art 32–bit commercial and/or current DoD development programs, in order to ensure cost–effective transfer of technology into future space missions. Hardware selection should be based on components which will not require development of an Instruction Set Architecture. The AFC should demonstrate compatibility with commercially available Ada, C, and other software development tool suites.

The Loral special AFC study consisted of the following task elements:

Architecture: Define a highly modular computer architecture initially suitable for fault tolerant processing as a single computer node, with provisions for future multi–node applications. Address task distribution, task partitioning (node coupling), and multi–tasking for multi–node applications.

VLSI Technology: Define a set of VLSI parameters and/or characteristics which are essential in the development of a specification for the Advanced Flight Computer. Specifically examine the use of SOI and/or other technologies for increasing device densities, including device layout. Also evaluate reduced voltage technologies and system logic level threshold margins.

Packaging: Define the packaging approach required to achieve the 1998–2000 AFC performance goals, as listed in Table 1. Study the application of three dimensional and other high density packaging technology for logic and memory circuits.

Other tasks include: Development of a high–level plan for the AFC which supports the schedule goals through 2000; Identification of required trade studies; and study reports.

This report presents the results of the Architecture, VLSI Technology, and Packaging study tasks in Sections 2, 3, and 4, respectively. AFC challenges, issues, and potential future trade studies are discussed in Section 5. A high level development plan which supports the AFC 1995–2000 time frame is presented in Section 6.

NOTE: The use of brand names in this report is for completeness and does not imply NASA endorsement.

2. ARCHITECTURE DEFINITION

2.1 Architecture Study Concept and Approach

The approach for the AFC architecture study was to examine current flight computer architectures, including performance, form factor, I/O, and packaging. These current capabilities were then projected to determine the state of technology for performance, manufacturing, and packaging in the 1998 time frame. The key points listed below influenced the approach and outcome of this study.

- Spacecraft computing increasingly relies on commercial processor designs, as well as commercial off-the-shelf (COTS) components, for space missions with minimal environmental radiation requirements. To achieve necessary radiation hardness, technology transfer to rad-hard VLSI processes is necessary. The resulting one- to three-year technology lag, while much shorter than design-from-scratch approaches for space systems, means that current state-of-the-art designs that began development one or two years ago will be in flight by 1994-1996. Similarly, developments in 1996 will be deliverable in 1998 and flown in 1998-2000.
- Radiation hardened CMOS VLSI foundries typically implement gradual improvements in the fabrication process, such that enhancements or changes made to a process are kept in place for at least 3 years. This allows projections to be made for the AFC 1998 goals by analyzing plans and trends in VLSI technology through 1996-1997.
- Packaging approaches for achieving high integration are influenced by the use of standard package formats and sizes. Rather than designing unique, custom packages for AFC modules, the low-cost and low-risk approach is to rely on packages that are either standard or widely supported throughout the industry. This means that a highly integrated AFC module will likely be some form of multi-chip module with standard dimensions for package and pins.

2.1.1 AFC System Architecture Concept

Based on the technology projections, current flight computer designs can be shrunk from subsystem circuit board implementations to multi-chip modules. A modular architecture was developed, where an AFC processing node would consist of one to three multi-chip modules:

1. Processor Module: containing a node processor and local memory
2. Global Memory Module: containing high density, large storage global memory
3. Interface Module: containing the external and intra-node I/O communications

AFC processing nodes may function as spacecraft control processors, consisting of a general-purpose control CPU. It may also function as a signal processing node, and consist of one or more Digital Signal Processor (DSP) chips. For this study, a control Processor Module using the

RAD6000–SC/PowerPC was analyzed, as well as a DSP multi–node module using the Analog Devices 21020/21060.

A block diagram of the AFC system architecture is shown in Figure 1, where each of the shaded blocks comprises a multi–chip module. Each multi–chip module is discussed in detail in subsequent sections. This system architecture represents a loosely coupled, distributed, shared bus configuration, consisting of heterogeneous processing nodes to support control and signal processing applications. The RAD6000–SC or PowerPC processor node performs the spacecraft command and data handling, guidance, navigation and control functions. The DSP multi–node module performs the compute–intensive signal processing and payload data communications for applications such as earth science and commercial remote sensing. Each processing node may have an I/O module for interfacing to sensors or instruments via MIL–STD–1553B, 1773, or other standard links. Uplink and downlink communications can interface directly to the I/O module or via the standard buses. The system uses the commercial Peripheral Component Interconnect (PCI) bus, as well as a shared memory bus.

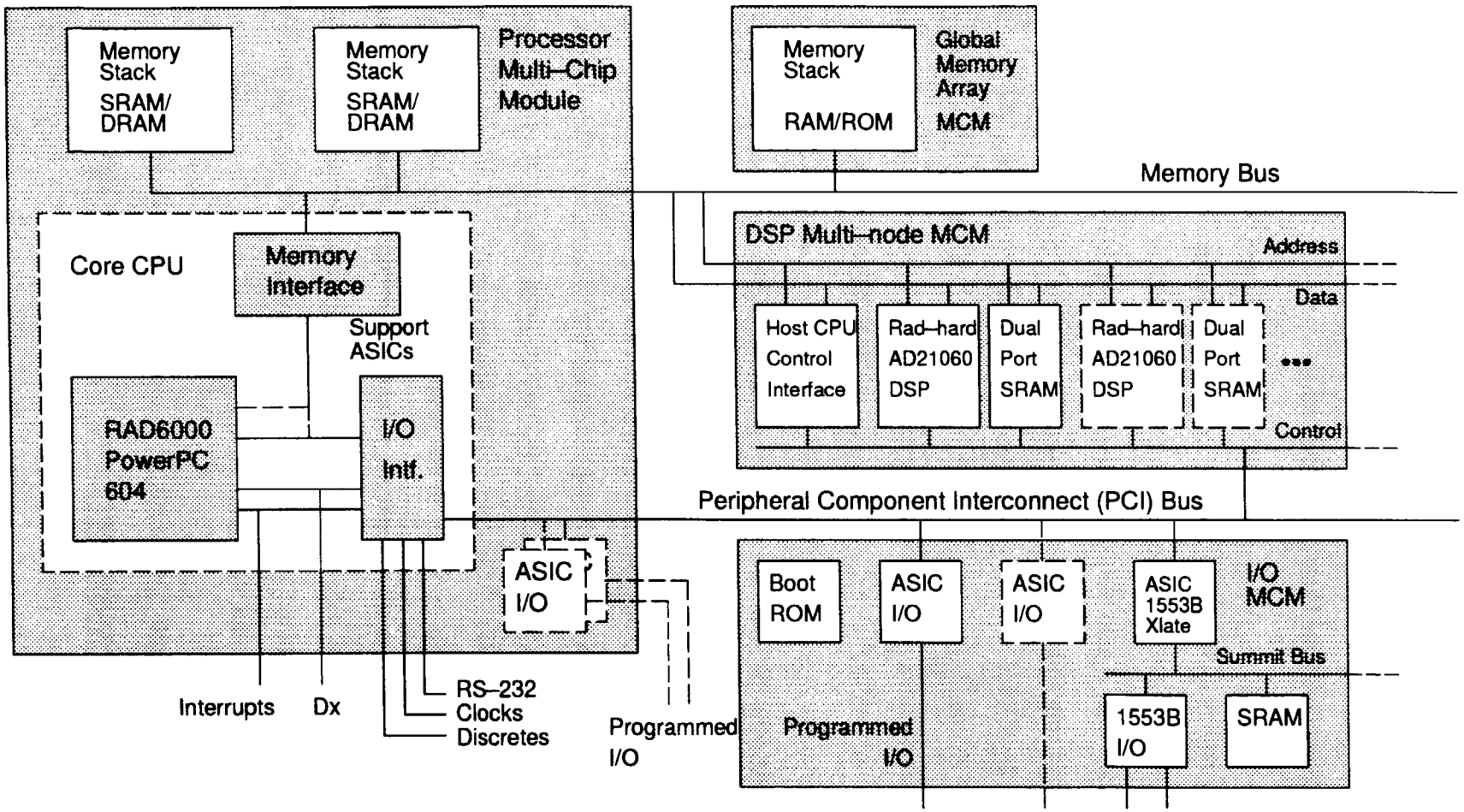

Figure 1. AFC System Architecture Concept Layout Diagram

2.1.2 Initial Baselines

2.1.2.1 Control / General Purpose Processor

The baseline processor for the AFC architecture study is the RAD6000–SC single chip CPU. The RAD6000–SC is Loral's radiation hardened 32–bit Reduced Instruction Set Computer (RISC) processor, and offers the highest MIPS per watt and MIPS per MHz of any radiation hardened space processor available. The RAD6000–SC was developed by transferring IBM's commercial RISC System/6000 single chip CPU (RSC) design to the Loral Federal Systems – Manassas VLSI line. This means that the RAD6000 is the only 32–bit radiation hardened processor that is a gate–for–gate duplicate of its commercial equivalent. The RAD6000–SC therefore enjoys the support of existing software development tools hosted on the IBM RISC System/6000 workstations, such as: Ada and C compilers, an efficient run time environment, a UNIX operating system (AIX), and extensive simulation and debug tools under the Powerbench suite. No new instruction set architecture is required for the RAD6000–SC. In fact, no code translation or optimization is needed between the RAD6000–SC and commercial RSC processors.

Following the success of the RAD6000 effort, Loral has baselined the RAD6000–SC into the JPL Mars Pathfinder mission, as well as the Phillips Laboratory ATIM program. To maintain a growth and evolution path for Space–related processor technology, Loral's plan is to selectively follow the evolution of the IBM commercial RISC System/6000 architectures. Loral is negotiating with IBM to develop a radiation hardened equivalent to the PowerPC 604 processor, which was developed by IBM and Motorola for commercial workstations, PCs, and embedded processing applications. As part of this AFC special study, the planned demonstrable computer prototype for the 1996 time frame will be the RAD6000–based Mars Pathfinder flight computer. The radiation hardened PowerPC 604 would be used for 1998 production capability.

The radiation hardened PowerPC 604 is identical to the commercial PowerPC 604 CPU. The 32–bit PowerPC 604 RISC processor uses a 6–stage pipeline to achieve high frequency operation: fetch, decode, dispatch, execute, completion, and writeback. A superscalar design allows concurrent operation of six independent execution units: branch, three integer, floating point, and load/store.

This allows a sustained maximum of 4 instructions per cycle. It uses dynamic branch prediction to enhance instruction prefetching, as well as speculative execution techniques. Instructions are executed out of order, and are completed in–order to support precise exceptions. The PowerPC 604 supports two separate 16KB instruction and data caches, with byte parity on both caches. On–chip memory management supports 32–bit real and 52–bit virtual addressing. Multiprocessing is fully supported via the following features: software cache control, bus snooping, and a full 4–state MESI (Modified, Exclusive, Shared, Invalid) cache coherency protocol.

2.1.2.2 Digital Signal Processor

Under sponsorship of Phillips Laboratory, Loral is negotiating a license arrangement with Analog Devices, Inc. (ADI) to develop a radiation hardened version of ADI's 21020 DSP device. The rad–hard AD21020 will be fabricated on Loral's RHCMOS process, with an SOI version planned for outyear funding. The existence of this baseline guided the AFC study approach in selecting the rad–hard AD21060, which is an enhanced DSP whose commercial counterpart will be available in 1995. The assumption made was that the rad–hard AD21060 would be available during the 1998 time frame for AFC.

The AD21060 DSP features a super–Harvard (superscalar) architecture, with concurrently executing arithmetic, multiplier, and shifter units. A 32x48 bit instruction cache is available on–chip, as well as a very large 4 Mbit dual–ported SRAM. This large memory is targeted at high–end, multiprocessor signal processing systems in coarse–grain configurations. The AD21060 supports multiprocessing through glueless connection capability of up to six 21060 DSPs, via on–chip link ports. Additional multiprocessing support includes built–in bus arbitration logic, bus–lock sequences for semaphores, and DMA control to the dual–ported SRAM. A host CPU or controller interface is supported to manage the communication between the multiple DSPs and the system bus. For the radiation hardening effort at Loral, it is conceivable that the large on–chip SRAM will not be implemented on–chip, in order to reduce SEU sensitivity. Hence, for sizing purposes in this study, an assumption was made that dual–ported RHSRAMs would be available and stackable during the 1998 time frame.

2.1.2.3 *Advanced Memory Packaging*

This AFC special study includes a trade study on the various, advanced 3–D memory packaging technologies that are either available or being developed today. Both "short stacks" and "cube loaf" orientations are analyzed in Section 4. Short stack memories were part of the initial architecture baseline, due to their smaller dimension profiles, and current availability. The stacked memory device is a process developed by Irvine Sensors, Inc. Currently, up to 5 unpackaged memory die can be stacked, resembling a "short stack" of pancakes, with the I/O signal lines on each die routed to one side of the stack and down to a ceramic interposer. The interposer connects the lines to either an external pin–out package, or to the silicon substrate of a VCOS module. Four of the 5 die in the stack are known good, and are used actively. It is possible to implement up to 6 or 7 die before encountering structural or topological problems, where the height of the stack far exceeds other devices and constrains the hermetic cap on the module. The height of the stack is also influenced by the memory die configuration, since 4 or 8 active die are preferred to achieve byte or word orientation in a stack.

2.2 Comparison to AFC 1998 Performance Goals

The AFC architecture approach outlined above, and discussed in detail in the subsequent sections, results in a processing node that meets or exceeds the 1998 AFC performance goals. A comparison of the goals versus the architecture is shown in Table 2 below.

The weight and volume figures include only the dimensions and mass for the multi–chip module VCOS package and the silicon die within. No second level packaging effects were included in the AFC architecture study, that is, these figures do not count the weight and volume of a printed wiring board to which the MCM modules are attached. Note that the effects of second level packaging were considered and included in the results of the packaging study in Section 4.

Using a radiation hardened PowerPC 604 processor, the AFC processing node that consists of a Processor and I/O Module would achieve over 41 Million Instructions Per Second (MIPS) running at 25 MHz. The PowerPC 604 has an internal clock multiplier that scales the system clock. This allows performance throughput and power consumption to be controlled. At the target operation of

25 MHz, power consumption for the Processor Module is 7.6 watts, using 1 MB SRAMs. A typical 1553 I/O Module would already exceed the AFC goal of 8 watts maximum. However, optical interfaces such as 1773, or simple serial I/O lines, when coupled with the DRAM local memory, will reduce I/O power such that the combined Processor and I/O modules will approach the power goals.

Table 2. Comparison to AFC 1998 Performance Goals

Feature	AFC Goal	PowerPC 604 + I/O	Comments
Power Consumption	2 – 8 Watts	7.6W (1 MB SRAM) 4.1W (16 MB DRAM) at 25 MHz	Excludes I/O power. Full 1553B I/O interface will exceed power goal alone. 1773 interface may fit within goal using DRAM modules.
Weight	0.2 lbs (3.2 ounces)	0.17 lbs (2.7 oz.)	No second level packaging included.
Volume	4 cubic inches	3.76 cubic inches	Includes Processor and I/O Modules. No second level packaging included.
Performance	3 – 5 MIPS/Watt	5.4 MIPS/W (SRAM) 10.0 MIPS/W (DRAM)	Processor node power only, using 25 MHz operation.
Throughput	10 – 40 MIPS	41 MIPS @ 25 MHz	Performance scales with clock. 604 has an internal clock multiplier of 1x, 1.5x, 2x, & 3x from the bus clock.
Local Memory	1 MByte minimum	1 MB SRAM, or 16 MB DRAM	Using short stack packaging for memory die.
I/O	1 interface minimum, eg. 1553B, 1773	1553B I/O module	Conceptual architecture consists of a processor MCM plus an I/O MCM.
Test Interface	To Be Defined	IEEE 1149.1 JTAG	

2.3 Description of the AFC System Architecture

2.3.1 AFC Processor Module Architecture

The AFC Processor Module consists of a general purpose control CPU, local memory, and local inter–node bus interface circuitry, on a 308–pin MCM package. In the current (through 1996) time frame, the Loral RAD6000–SC processor will be used. For the 1998 time frame, the rad–hard PowerPC 604 processor will be used. All subsequent performance figures in this section pertain to the rad–hard PowerPC 604.

The Processor Module layout diagram is shown in Figure 2. It supports simplex or dual lock–step compare operation for fault protection on critical missions. Local memory consists of up to 16 MB DRAM or 1 MB radiation hardened SRAM (RHSRAM). Memory devices are packaged in two short stack configurations. Each short stack contains 4 to 5 active 128Kx8 bit RHSRAMs, or 4Mx4 bit IBM LUNA DRAMs, plus error correction code bits. Target operation frequency is 25 MHz, with a throughput of 41 MIPS and power consumption of 7.6 watts at 3.3 Volt power, using 1 MB SRAM for local memory. When using 16 MB DRAM, power consumption is 4.1 watts. The I/O and Memory Interface chip supports the PCI bus interface for the internal system bus.

The multi–chip module occupies a 2.4" x 2.4" footprint, with a base volume of 1.55 in^3 (2.1" x 2.1" x 0.35"). The MCM weighs 1.1 ounces (31 grams) using 1 MB SRAM in a short stack package configuration. The MCM is a Loral VLSI Chips On Silicon (VCOS) package, which is further described in Section 4. Test and debug is supported via a IEEE 1149.1 (JTAG) interface. In addition, the RAD6000–SC supports the IBM Common On–chip Processor (COP) test interface.

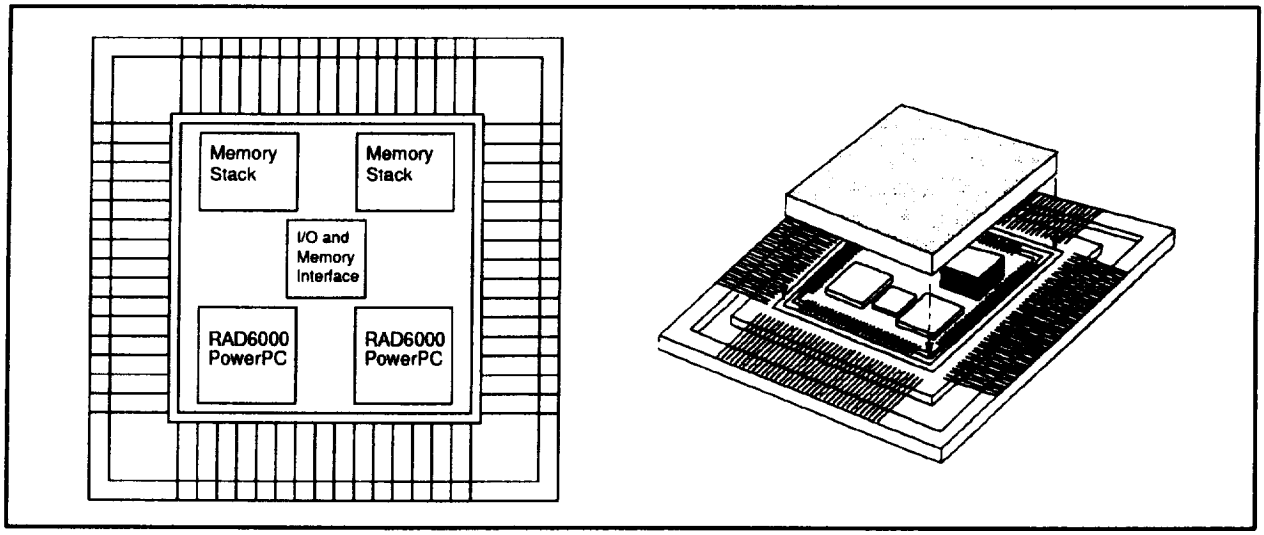

Figure 2. AFC Processor Module Architecture

2.3.2 AFC Global Memory Module Architecture

The AFC Global Memory Module is a VCOS multi–chip module that contains memory that can be shared by multiple nodes over the memory bus (see Figure 1). The memory consists of stacked DRAM or RHSRAM, and may also contain start–up ROM. The global memory module may also

be used as a highly integrated storage buffer for manipulation of image data in signal processing applications. Densities of up to 3.5 MB can be achieved using stacked 1 MB radiation hardened SRAM, or up to 56 MB using 16 Mbit DRAMs, both of which are available today. Note that the Global Memory Module is not included in the performance figures on Table 2, since not all nodes require an additional memory module.

The multi–chip module occupies a 2.4" x 2.4" footprint, with a base volume of 1.55 in^3 (2.1" x 2.1" x 0.35"). The MCM weighs 1.3 ounces (37 grams) using 1 MB SRAM in a short stack package configuration. In the layout shown in Figure 3, the global memory module contains 3.5 MB using stacked RHSRAM, plus storage for error correcting code (ECC). Power consumption is 4.5 watts worst case, operating at 25 MHz.

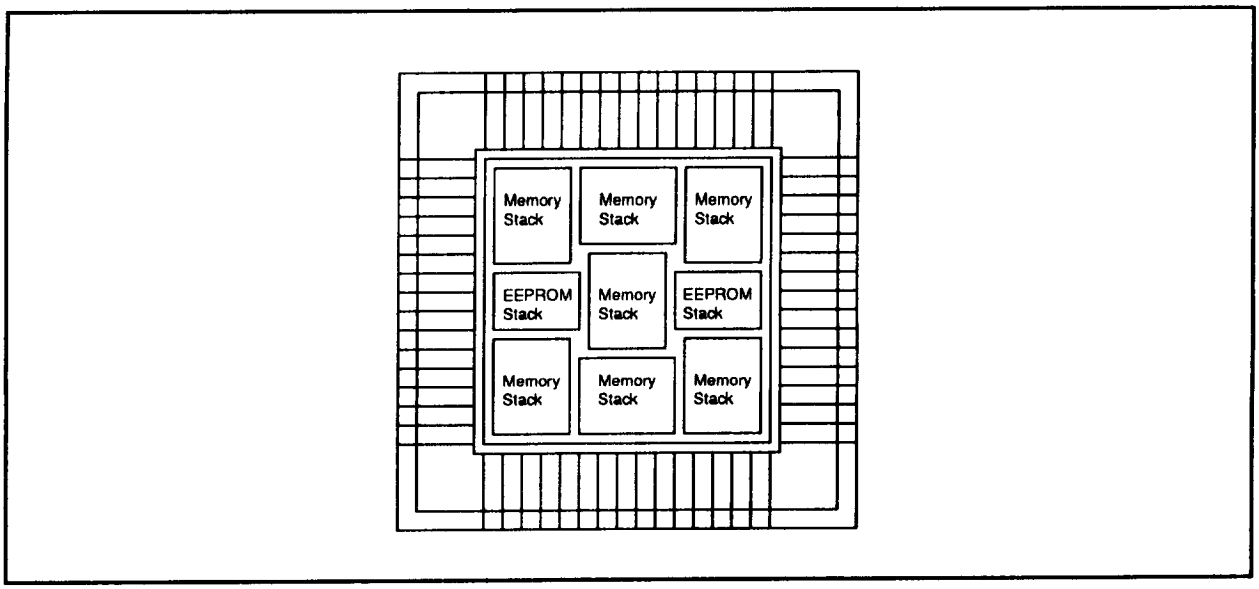

Figure 3. AFC Global Memory Module Architecture

2.3.3 AFC I/O Module Architecture

The AFC I/O Module is a high density MCM–C (ceramic) package, with devices on both top and bottom of a ceramic substrate. In the configuration shown in Figure 4, a hermetic cap seals the bare die that are mounted on the top of the ceramic substrate, while individually packaged surface–

mount components are mounted on the bottom of the substrate. Loral is currently using this approach for the I/O module on the Globalstar flight computer.

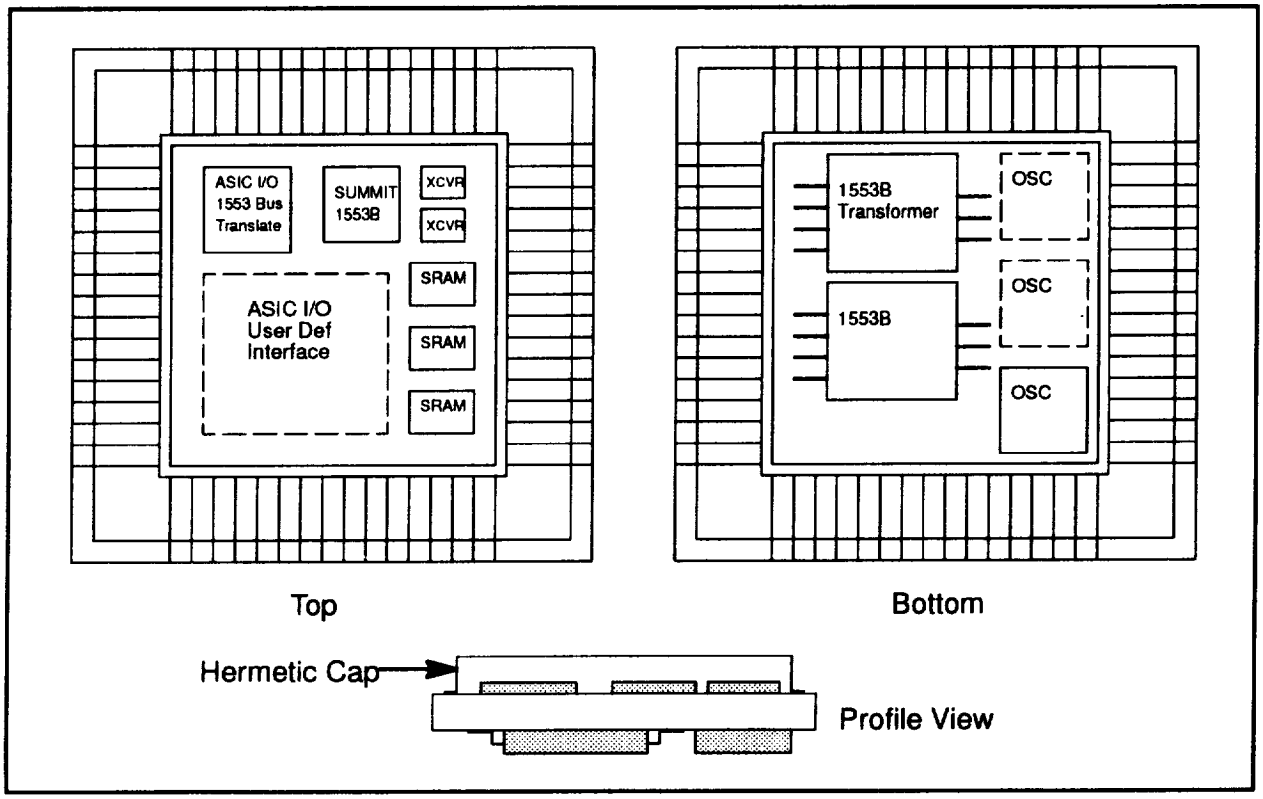

Figure 4. AFC Global Memory Module Architecture

For sizing and analysis purposes, the I/O Module contains a MIL–STD–1553B interface, using a United Technologies Summit series UT69151 LX 1553 chip with separate transceiver devices. An assumption was made that bare die for these chips would be available from United Technologies for mounting on the MCM–C substrate. The UT69151 can access up to 64K x 16 bits of external RAM memory, used for command and configuration tables. Three 8K x 8 RHSRAMs are included on this I/O Module, as well as an interface chip for communication between the 1553/Summit device and the PCI local system bus. Additional space is available on the top of the MCM–C substrate for custom I/O or ROM. The 1553B transformers and system clock oscillators are individually packaged and mounted on the bottom of the substrate. These packaged devices increase the

mass of the I/O Module, for a total of 3.4 ounces. The two–sided mounting also increases the volume to 2.21 in^3 (2.1" x 2.1" x 0.5").

The I/O Module can be configured to have an optical 1773 interface, replacing the 1553 components and thereby saving on power and weight. 1773 interface chips are available today that can fit within the space of existing 1553 components. The opto–coupler modules are about the same size as a multi–chip module, and would be kept separate from the I/O Module.

2.3.4 AFC Digital Signal Processor Module Architecture

During the later half of this study period, the sponsors at NASA LaRC requested an additional study to include digital signal processors as a possible processing node in an AFC system. As a result, a signal processing module architecture was developed, and is described below. Figure 5 shows a layout of the DSP Module.

The AFC Digital Signal Processor (DSP) Module is a VCOS MCM with one or more DSP devices in a shared memory/bus configuration.

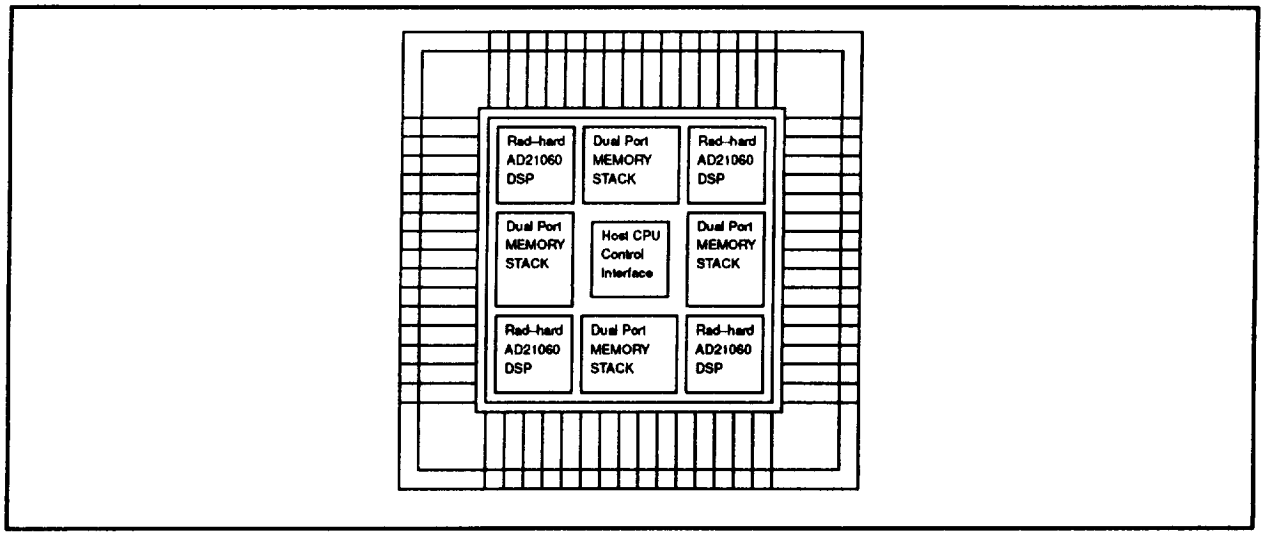

Figure 5. AFC Multi–Node DSP Module Architecture

The multi–chip module occupies a 2.4" x 2.4" footprint, with a base volume of 1.55 in^3 (2.1" x 2.1" x 0.35"). The MCM weighs 1.1 ounces (31 grams), assuming 4 Mbit of dual–ported SRAM in a short stack package configuration for each of the four DSP devices. A Host CPU/Control Interface chip provides the interface to the system PCI bus, as well as to the global memory bus (see

Figure 1). Power consumption is 14 watts worst case, operating at 25 MHz with all devices active on the MCM. Performance for each DSP is 25 MIPS / 50 MFLOPS at 25 MHz, or 100 MIPS / 200 MFLOPS for a 4–node DSP MCM.

2.3.5 Processor Comparisons

The following table summarizes the key features of the processors included in this study.

Table 3. Summary of AFC System Processor Features

Feature	RAD6000–SC	PowerPC 604	AD21060 DSP
Technology Used Channel length L_{eff}:	RHCMOS 3.3V or 5V 0.8 μm	RHCMOS 3.3V 0.5 μm	RHCMOS 3.3V 0.5 μm
Chip Power @ 25 MHz	3 W	2.5 W	2.3 W (incl. 4 Mb SRAM)
Signal I/O Pin Count	213	171	est. 170
Performance @ 25 MHz	27 MIPS	41 MIPS	25 MIPS, 50 MFLOPS
Superscalar Features	2 instructions/cycle, On–chip fixed and floating point units.	4 instructions/cycle, On–chip integer (3), floating pt., & branch proc units.	Single multi–function instr exec/cyc, parallel ALU, multiplier, and shifter units.
On–chip Cache	Shared instr/data cache, 8 KByte, 2–way set assoc.	Separate instr & data caches, each 16 KByte 4–way set associative.	32 x 48 bit instruction cache.
Multiprocessing Support	Distributed processing thru peripheral I/O logic.	Bus snooping, 4–state MESI cache coherency protocol.	Glueless connection of up to six 21060 DSPs. On–chip link ports and bus arbitration.
Fault Tolerance Support	SECDED on memory data bus, parity on I/O addr/data bus, Boundary chk/gen. 16 external interrupts plus checkstop.	Parity on memory_I/O data and address bus. ECC support with peripheral I/O logic via 12 interrupts plus 3 error flags & checkstop.	Parity and ECC support via peripheral I/O logic. 4 definable interrupts and 5 flags.
Languages, OS Software Development Environment	C, Ada (Verdix), OSOpen, Vxworks in development. RISCwatch + RS/6000, std UNIX dev tools.	C, planned Ada & Vxworks. PVS sim/emulation tool + RS/6000, std UNIX tools.	C, Ada (Verdix). EZ–ICE emul tool, PC–based dev system.
Test and Debug	Common On–chip Processor (COP) interface.	COP and IEEE 1149.1 JTAG interface.	IEEE 1149.1 JTAG interface.

The RAD6000–SC is currently manufactured at Loral Federal Systems Manassas. As discussed in the Initial Baselines (Section 2.1.2), Loral is negotiating under separate efforts with IBM and Analog Devices to develop radiation hardened equivalents of the PowerPC 604 and AD210x0, respectively.

2.3.6 Node Connection Comparisons

The system architecture presented in this study supports both centralized and heterogeneous, distributed, shared bus node connections. The architecture diagram shown in Figure 1 on page 9 depicts a shared bus, loosely coupled multi–node connection consisting of a heterogeneous mix of processors, both general–purpose and DSPs. This same configuration can become a simple, centralized architecture with a single controller or general purpose processor, as shown in Figure 6 below.

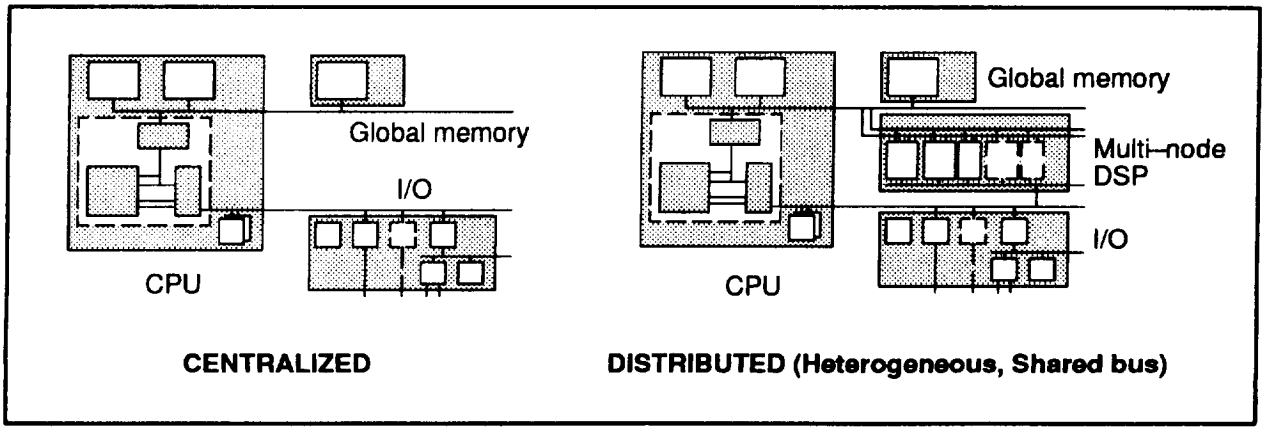

Figure 6. AFC Node Connection Alternatives

The AD21060 supports glueless connection with up to six AD21060 processors for multiprocessing in snugly or tightly coupled configurations. This capability, which also supports a host CPU or interface control chip, allows for DSP organizations in two– and three–dimensions well suited in signal processing applications. An example of this organization is a toroid network, shown in Figure 7, which consists of sixteen DSP nodes. Each node contains an AD21060 DSP with local memory, and is connected to its four nearest neighbor nodes. Two I/O nodes are shown in the figure, providing communication between the toroid network and the system bus.

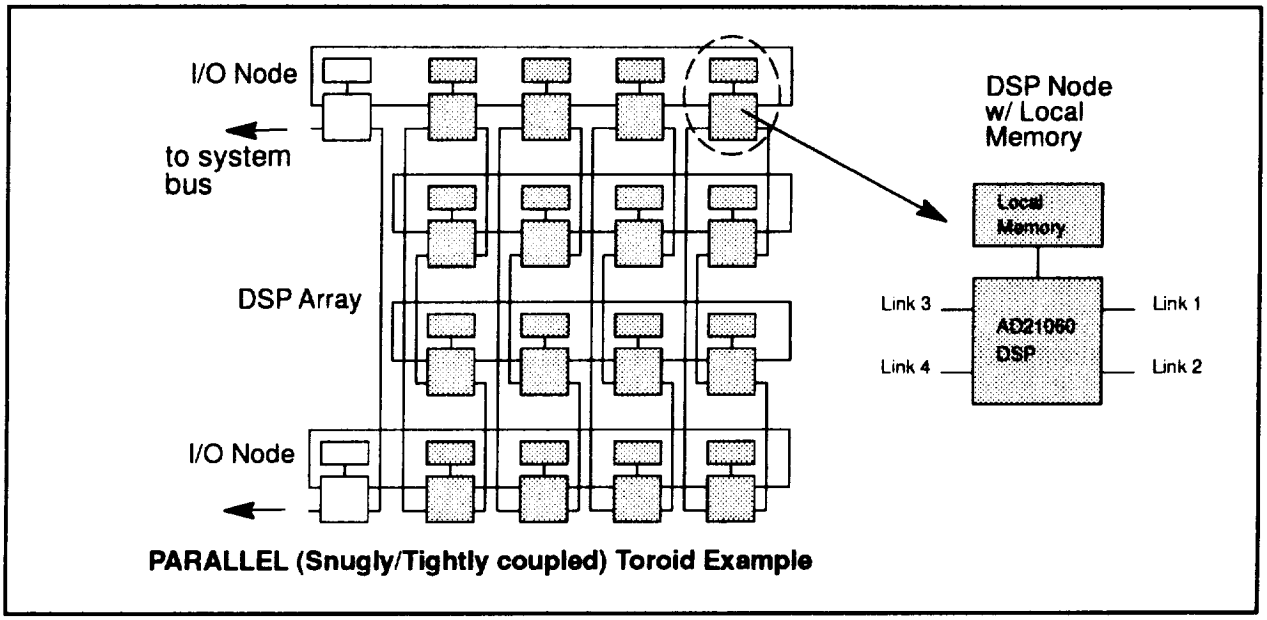

Figure 7. AFC DSP Node Connection Alternative

Node connection and architecture for Space will be mission and application dependent. Trade–offs for choosing an architecture and network organization include: processing throughput required; on–board, real–time processing activities for the mission; spacecraft and subsystem mass, volume, power, and level of integration requirements; as well as cost and schedule risk. Since these influences are not easily classified or bound, the scope of the DSP architecture study was kept to the loosely coupled, distributed organization. This architecture, when considered with the capabilities of a high performance DSP such as the AD21060, can meet most of the on–board signal processing requirements for near–term space missions.

3. VLSI TECHNOLOGY

3.1 Essential Parameters/Characteristics for AFC

For this AFC study, a set of VLSI parameters and characteristics essential to the development of an AFC specification were identified. These parameters/characteristics are listed below, and discussed in following sections.

- **Feature Size**: Involving transistor sizing groundrules and channel lengths.
- **Technology Type**: Bulk Silicon CMOS, Silicon–on–insulator (SOI), BiCMOS, etc.
- **Voltage Level**: 5.0 volts, 3.3 volts, 2.5 volts.
- **No. of Wiring Levels**: Layers of metalization in the fabrication process.
- **Device Isolation**: Method of isolating logic gates in VLSI.
- **Radiation Hardness**: For applications in Space and radiation environments.
- **Compatibility with Commercial VLSI Process**: Not an essential characteristic, but highly desirable for rad–hard foundries.

Table 4 on page 22 summarizes the VLSI technology parameters and characteristics listed above, including descriptions and comments that are discussed further below.

3.1.1 Feature Size

The feature size of a VLSI process typically refers to two parameters: the technology **groundrules**, and the effective channel length L_{eff} of a transistor gate. The technology groundrules typically refer to the physical dimensions of the circuits that can be fabricated under a VLSI process, such as the width of a polysilicon line or the minimum space between two metal lines. These groundrules determine the smallest transistor gate that can be fabricated, and hence, also influence the L_{eff} of the gate. Both these parameters are expressed in units of microns (μm), with current VLSI technology capable of creating devices with 1.0 down to 0.5 μm gate effective channel lengths. New developments in CMOS VLSI technology are pushing L_{eff} to the 0.35–0.25 μm range using 0.5 μm groundrules, but are not expected to be in production processes before the end of the decade. The 1998–2000 AFC goals can be met with state–of–the–art VLSI technology that will be well–established in the 1996 time frame, using feature sizes of 0.7 to 0.5 μm for fabricating the RAD6000–SC and PowerPC 604 processors and related components.

Table 4. VLSI Technology Parameters/Characteristics Essential to AFC Specification

Characteristic	Benefit	Description	Comments, Issues
Feature Size	Circuit density (Number of bits or gates per square area), Performance	Typically involves two parameters: Technology ***groundrules*** and effective channel length L_{eff}. SOP values range from 1.0, 0.7, and 0.5 μm.	Future trend toward L_{eff} = 0.35–0.25 μm. Can meet AFC 1998–2000 goals with 0.7 to 0.5 μm technology. Issues: Smaller features require tighter processing tolerances & new precision fabrication tools.
Technology Type	Varied	***Bulk Silicon CMOS*** is the common VLSI technology. Silicon–on–Insulator (***SOI***) offers 30% or better improvement in size, power, & speed. Gallium Arsenide (***GaAs***) offers speedup at less power, but major differences to CMOS technology. Bipolar–CMOS (***BiCMOS***) offers speedup like Bipolar but higher power.	Bulk Si RHCMOS will meet AFC goals, but beyond yr. 2000 will likely need SOI. Issues: In near term, should address ability to handle increasing data rates (up to 800 Mbps) within power envelope. GaAs, BiCMOS, optical technology are needed for data interfaces. Also, SOI must improve total dose &/or latchup.
Voltage Level	Power consumption	Current practice for CMOS and TTL technology is ***5.0V***. Major migration to ***3.3V*** is underway, but not complete.	Can meet AFC goals with 3.3V system. Future trend toward 2.5V, then 1.5V.
Number of Wiring Levels	Circuit density, Performance	Typical CMOS fab processes can have 2 to 3 ***metal levels*** for connecting devices. VLSI processes that produce a ***Planar topology*** result in better metalization & help achieve a "***sea of gates***" design.	Can meet AFC goals with 3 to 4 metal wiring levels. SOA processes (incl Loral, which has a planar back–end–of–the–line PBEOL process) can have 2 to 4 metal levels, migrating up to 5 metal levels.
VLSI Device Isolation	Circuit density	Current CMOS fab processes use locally oxidized silicon (***LOCOS***) approach to isolate devices on a VLSI die. To achieve higher density on a die, the LOCOS approach is being replaced by shallow trench isolation (***STI***).	Can meet AFC 1998–2000 goals with LOCOS processes. Beyond 2000 will likely require STI. Issues: STI approaches must also demonstrate radiation hardening ability. (Planned in 1996 with Loral's RHCMOS–5L STI process.)
Level of Radiation Hardness	Operation in radiation environments	With increasing reliance on ***commercial OTS*** technology, space programs must ensure that VLSI devices meet the radiation hardness requirements for a given mission/application.	Commercial VLSI processes have total dose hardness up to 50K rads, good latchup protection, but poor ***SEU***. Issues: 100K rads inadequate for certain space applications.

The benefits of decreasing the feature size in a VLSI process are the increased circuit densities and performance. By shrinking the device feature sizes, more bits or gates can be packed in the same square area of silicon. The increased density means that signals do not have to travel as far to accomplish the same logical operation, thus leading to increased performance. Increasing density also

reduces overall die size, which can lead to reduced size and weight at the system level. Note that packaging issues also affect system level dimensions, and these factors are studied in Section 4.

3.1.2 Technology Type

The most common VLSI technology type, in both commercial and radiation hardened processes, is **bulk Silicon CMOS**. Several companies involved in rad–hard VLSI manufacturing, including Loral, have investigated using Silicon–On–Insulator (**SOI**) technology, which offers 30% or better improvement in size, power, and speed compared to bulk CMOS. Each of these companies must still address radiation effects in their respective SOI processes. For Loral, this means improving the total dose capability from 50K rads(Si) to over 100K rads(Si). For other companies, this means resolving crucial latch–up issues. Bulk Silicon Rad–Hard CMOS (RHCMOS) meets the AFC 1998–2000 goals, but SOI may be preferable as the technology matures.

Technology type is also an issue (and perhaps more pressing) in dealing with the higher data rates encountered in imaging instrument interfaces. Multi–spectral imagers on spacecraft can stream image data at rates approaching 1 Gigabit per second. Today, solid state recorders are being designed to handle data rates of 640 Megabits per second (Mbps). The interfaces for these data rates must drive and receive signals at compatible speed. In order to achieve this at acceptable power levels, Gallium Arsenide (**GaAs**) and Bipolar–CMOS (**BiCMOS**) devices are employed as interface transceivers. Mature bipolar Emitter–Coupled Logic (**ECL**) is also used today, although incurring slightly higher power consumption. The interface medium may be optical or metal, both of which are supported by GaAs and BiCMOS devices.

3.1.3 Voltage Level

Most VLSI devices operate at the common 5.0 volt power level. Within the past several years, commercial designs have begun a migration to 3.3 V technology, driven by reduced power requirements especially in the mobile computing area. Entire 3.3 V systems (including processor, memory, and interfaces) for Space–based applications are not yet available, given the established interface standards and protocols for 5.0 V technology. In order to meet AFC goals especially in power consumption, 3.3 V should be the dominant technology. However, despite current research

trends towards 2.5 V and 1.5 V operation, more studies are needed to determine the optimum (3.3 V or 5.0 V) voltage in relation to total system battery energy and the mission requirements [see reference article by R. Wilson, *Call It Energy Management*].

3.1.4 Number of Wiring Levels

Typical CMOS fabrication processes can have two to three levels of metal for connecting components on silicon die. The capabilities of the fabrication process determine the width of a metal signal line and the space between metal lines on a given level, which influences the groundrules of that process. To increase performance through higher component densities, one approach is to place the components on a die closer together, and increase the number of metal levels to reduce the metal–to–metal spacing issues. This is also referred to as the "sea of gates" (SOG) design method. In order to increase the number of metal levels, a key effort in the fabrication process is to maintain a **planar topology** on the surface of the silicon wafer.

Current fabrication processes use two to four metal levels. As shown later in the technology roadmap on Figure 8, Loral's current RHCMOS 4L/4S process uses 2 to 4 metal levels with a planar back–end–of–the–line (PBEOL) process to maintain planar wafer topology. Part of the PBEOL process involves milling the surface of a silicon wafer during fabrication. This is done before the metal layers are deposited, in order to reduce extreme changes in wafer topology caused by the overlap and/or absence of oxide and polysilicon over the wafer. Such a non–planar surface can cause metal line breakage or hasten breakage due to electromigration, since a metal line may be weakened where it crosses over an abrupt change in the topology. Plans are to migrate to up to 5 metal levels, although the AFC goals can be met with current processes.

3.1.5 Device Isolation

Most CMOS fabrication processes currently use the locally oxidized silicon (**LOCOS**) approach to isolate devices on a VLSI die. This large silicon dioxide (SiO_2) isolation reduces parasitic effects and helps achieve total dose radiation hardening. To achieve higher circuit density on a die, the LOCOS approach is being replaced by the IBM–patented Shallow Trench Isolation (**STI**) approach at Loral's Manassas line. As its name implies, STI uses a shallow, diffused sidewall that serves as

a trench in the silicon to isolate devices. This approach reduces the area needed for isolation and allows devices to be placed closer together, thereby achieving higher circuit density on a die. Loral plans to implement STI in its RHCMOS–5L VLSI process in 1996.

3.1.6 Radiation Hardness

Space programs are increasing reliance on commercial off–the–shelf (COTS) technology as a means of reducing cost and development time for spacecraft systems. While this has resulted in a reduction of radiation hardness requirements for some missions, the need for rad–hard VLSI devices remains strong in critical and/or highly autonomous applications. Many commercial VLSI processes now have total exposure dose hardness of up to 50K rads(Si), with good latch–up protection. However, many applications require 100K rads(Si) hardness or better, up to 1M rads(Si).

The Processor Module will achieve radiation hardness levels of 1×10^6 rads(Si) total dose, and single event upset (SEU) rates of 1×10^{-7} errors per bit–day in a worst case geo–synchronous orbit with no enhancement to the commercial PowerPC 604 latches. When implementing the PowerPC 604 design on Loral's radiation hardened VLSI process, the commercial latch designs can be replaced with hardened latches to improve SEU immunity to 1×10^{-10} errors per bit–day. Loral's radiation hardened bulk CMOS process (RHCMOS) is latch–up immune. The I/O and Global Memory Modules will have total dose levels of 1×10^6 rads(Si), and SEU rates of 1×10^{-10} errors per bit–day.

While total dose hardening is achieved through the VLSI fabrication process, single–event upset (SEU) protection is achieved through the circuit design. Spacecraft systems often require fault detection and recovery circuitry above that typically offered in commercial designs. This ranges from simple parity protection and error correction codes to fault isolation and recovery, including hardware/software protection for single event upsets (SEU). Most radiation hardened VLSI foundries have standard library cells of circuit latches that are more SEU resistant than similar commercial designs. For instance, a typical commercial 256 Kbit SRAM chip may suffer 1E–4 to 1E–6 errors per bit per day in space. This equates to one error occurring approximately every hour to

every four days, respectively. Meanwhile, a radiation hardened 256 Kbit SRAM would have 1E–10 errors per bit per day in space, or, one error occurring every 107 years.

3.1.7 Compatibility with Commercial VLSI Process

Some rad–hard VLSI foundries, including Loral Federal Systems Manassas, have developed their processes to be compatible with commercial foundries (in Loral's case, it is IBM's foundry). This allows easy transfer between commercial and radiation hardened designs, with little or no re–design needed for the transfer. Phillips Laboratory's Advanced Insertion of Standard Microelectronics (AISM) program seeks to fund such efforts for military and aerospace applications. The benefit of this capability is reduced development costs in bringing state–of–the–art technology to space applications. Also, rad–hard foundries can focus on improving yield and radiation hardness, relying on help from commercial counterparts for continued evolution in VLSI technology.

Having a commercial–compatible radiation hardened process is not essential to AFC goals. However, with a trend in space programs toward reduced budgets and reliance on COTS technology, this commercial compatibility will likely become a necessity for rad–hard foundries, in order to operate profitably. This capability may also be likely for achieving AFC goals beyond the year 2000. A key issue for these rad–hard foundries is the strategic selection of commercial processes to follow or adapt. Not all enhancements or stages of a commercial VLSI process need to be implemented in the rad–hard foundry, especially if space mission requirements do not warrant the cost of migration over the near term. On the other hand, it may be necessary to follow a commercial process enhancement simply to maintain migration–capability and compatibility for future enhancements.

3.2 A VLSI Technology Roadmap for AFC

The parameters and characteristics discussed in the previous section are shown in Figure 8 on page 28 as they evolve under Loral's rad–hard technology, representing a typical VLSI technology roadmap for AFC. The top of the figure shows IBM's commercial technology evolution timeline that Loral follows. Key contributions from commercial technology to Loral's rad–hard process include: the CMOS transistor design with 1 μm groundrules in the early 1990s, the 0.5 μm transistor design in 1992, the planar back–end–of–the–line (PBEOL) approach in 1993, and the shallow trench isola-

tion (STI) process planned for 1995–96. Note also that chip size increases with time, as circuit densities also improve. Figure 9 on page 29 plots Loral's VLSI circuit density improvement as process enhancements are introduced over time.

3.3 Silicon–On–Insulator (SOI) Technology

As mentioned in Section 3.1, SOI technology is not critical in order to meet AFC 1998–2000 goals. Nonetheless, an outlook on SOI technology was included in this study, due to its potential for significant benefits over bulk Silicon processes, and thus its suitability in meeting future AFC requirements beyond the year 2000.

Recent SOI development at Loral has resulted in fully functional 256 Kbit SRAMs with 0.5 μm feature sizes. A key goal is to preserve compatibility with bulk Si RHCMOS designs, while achieving significant improvement in performance, density, and radiation hardness. Tests on these SOI 256 Kbit SRAMs have shown the following benefits:

- A 30% increase in speed compared to bulk Si designs. When the design is optimized for SOI, a 60% increase in speed can be achieved. Optimizing for SOI involves a modification of the design to take advantage of the higher device densities and improved device performance that are possible with SOI.
- A 30% reduction in power consumption over bulk Si designs. Again, optimized SOI designs can achieve 60% reductions in power.
- A 30% decrease in chip size for optimized SOI designs compared to bulk Si.
- Improved SEU hardening without any re–design from bulk Si designs. The SOI SRAM tests showed a worst case rate of 5E–12 errors per bit per day, compared to 1E–10 for typical bulk Si RHCMOS SRAM.

Additional development is still needed for SOI technology, before it is qualified for use in space programs. While Loral's SOI process showed no latchup during tests, this is reportedly a concern for other companies involved in SOI technology development. Total dose hardening must also be improved from the current levels of 30K to 50K rads(Si). Current plans at Loral call for SOI technology to be phased in towards the end of the decade. Much of this work will depend on continued funding from various federal sources.

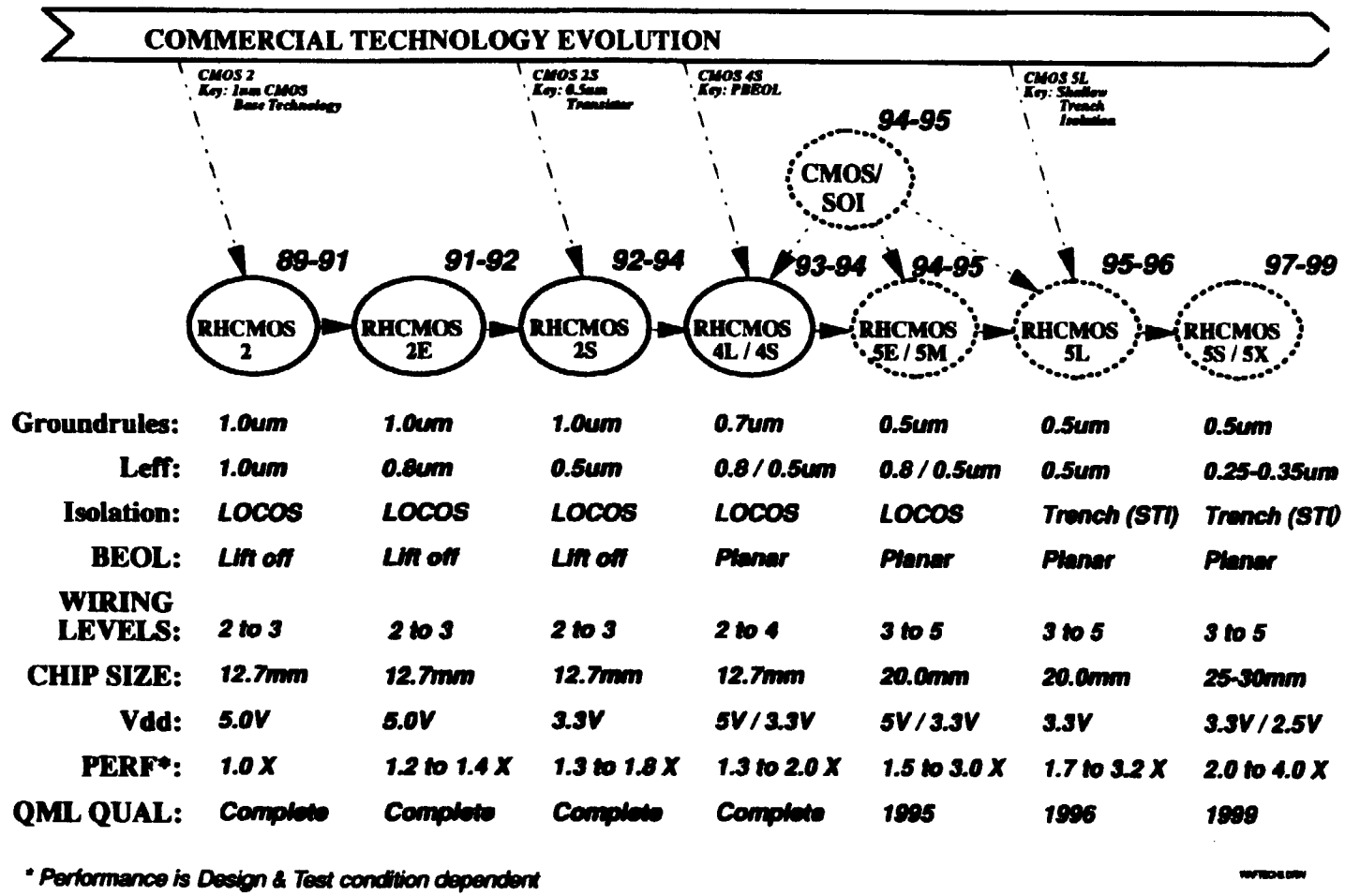

Figure 8. Loral's VLSI Technology Roadmap: A Representative Path for AFC

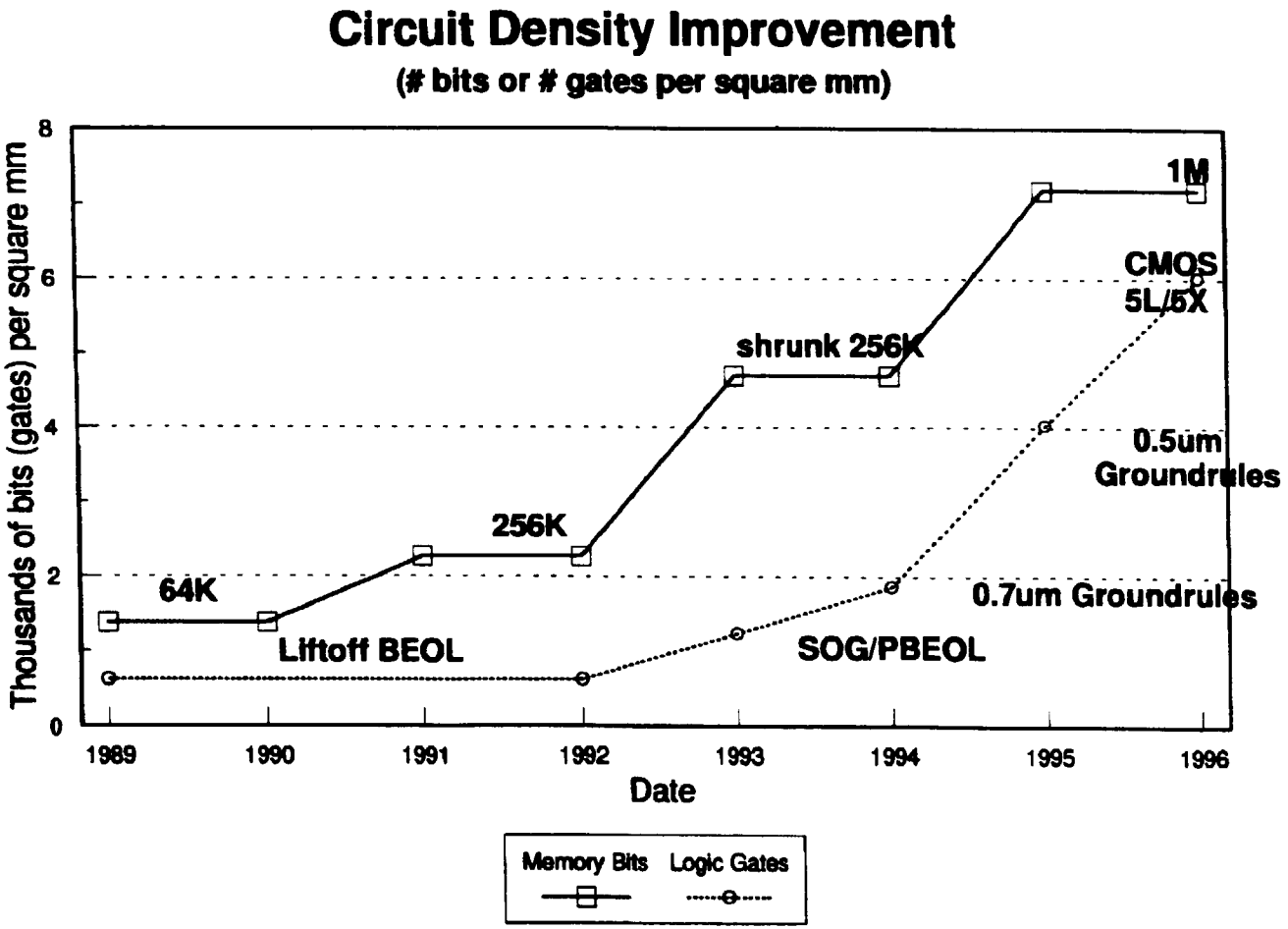

Figure 9. Loral's VLSI Circuit Density Improvement

4. VLSI PACKAGING STUDY

Trade studies on packaging approaches were conducted on the three MCMs that typically comprise an AFC node: Processor, Global Memory, and I/O modules. For the Processor Module, the General Purpose Processor Module was used to conduct the trades. DSP modules were a later inclusion to this overall study, and thus were only included in the architecture study.

Using existing and planned designs as guides, the studies were conducted using the following dimensions for the core chips that populate the three MCMs:

Table 5. Dimensions for Core Chips Used in the AFC Study

Chip	Module	Area (LxW, mm)	# of Signal I/O	Sgl–Chip Pkg
PowerPC 604	Processor	12.4 x 15.8	171	304–pin QFP
Memory–I/F Ctl	Processor	9.4 x 9.4	286	340–pin QFP
1 Mb SRAM	Processor, Global Memory	11.6 x 12.0	30	40–pin FP
16 Mb DRAM	Processor, Global Memory	8.0 x 18.0	27	32–pin TSOP
I/O Translator	I/O	9.4 x 9.4	180	220–pin QFP
UTMC 1553B	I/O	10.5 x 10.5	80	100–pin CFP
1553B XCVR	I/O	5.5 x 5.5	24	N/A
256 Kb SRAM	I/O (1553B)	9.0 x 6.0	28	36–pin FP

Current packaging technologies were used for this study, focusing on multi–chip module approaches (e.g., silicon or ceramic substrate MCMs) and three–dimensional packaging techniques employed in high–density memory applications. These packaging approaches are not expected to change during the 1995–1998 time frame, although additional experience and knowledge will be gained for 3–D packaging for memory and logic circuits, as well as for advanced stacked MCM packaging approaches.

4.1 Packaging Approach Studies

4.1.1 Processor Module Packaging

The trade study for the Processor Module included the following alternative packages, all shown in Figure 10 on page 32:

- Standard Printed Circuit Board (PCB) with single chip packages: this is used as a comparison baseline, representative of state–of–the–practice capabilities. The components are individually packaged and mounted directly onto the PCB.
- Chips First MCM with Face–Mounted SRAM Stack: this is representative of the High–Density Interconnect packaging approach, where bare silicon die including short stack SRAM memories are placed in milled cavities in a ceramic MCM substrate, with levels of metal over the top of the substrate for interconnect.
- VCOS with Face–Mounted SRAM Stack: this is representative of a silicon substrate MCM, where bare silicon die including short stack SRAM memories are mounted on a silicon substrate, which also contains the metal levels for interconnect. The die may be mounted face–down, such as in flip–chip solder ball technology, or face–up with wire or tape bonds to connect the I/O pads on the die to the silicon substrate.
- MCM with Edge–Mounted (Short Loaf) SRAM Stack: this is representative of a standard MCM package with a ceramic substrate (although a silicon substrate is also possible). In this case, the SRAM are mounted in a short loaf configuration; i.e., on a stack edge, rather than a "short pancake stack" configuration.

In order to maintain a common baseline across all packaging alternatives, all MCMs were assumed to have 308–pin, 25–mil lead pitch packages. Also, since space was available on all MCM package alternatives, an extra chip was included in the package sizings. This chip could be used for additional functional interfaces, multiprocessing control, or clock control. Dimensions for all packages consider the actual package footprint, and also include package covers/lids for individual components and MCMs. Finally, no second–level 3–D packaging was assumed; i.e., all MCMs were assumed to be mounted on a standard 2–sided PCB with 0.7" PCB–to–PCB pitch except where increase was necessary to accommodate tall MCM packages. The second–level PCB package was assumed to add 0.03 pounds per square inch to all MCM alternatives. Note that this second–level adder was not included in the dimensions discussed in the architecture study.

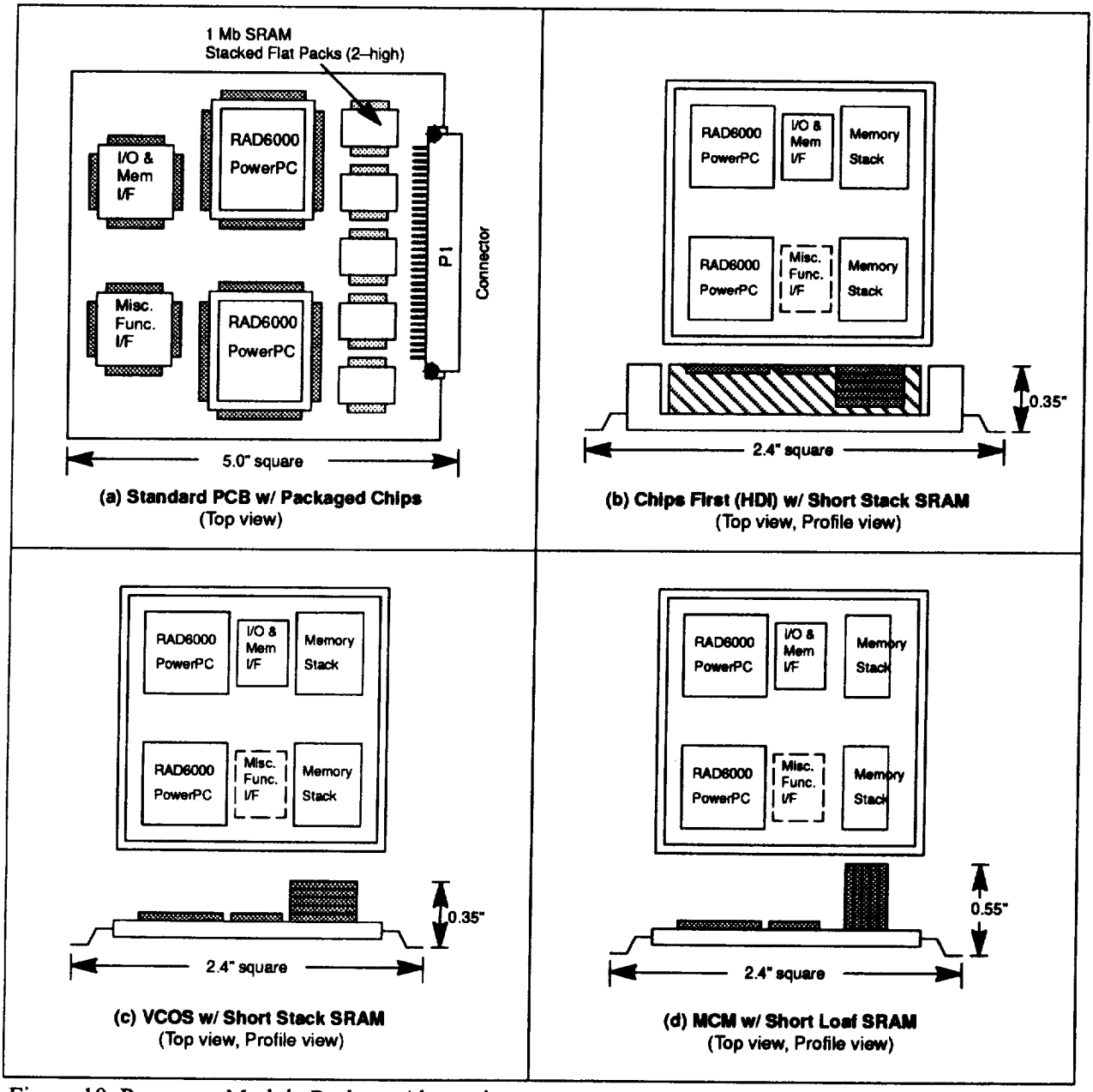

Figure 10. Processor Module Package Alternatives

The volume and weight of each packaging alternative is listed in Table 6. Naturally, the standard PCB package has the most volume and mass compared to the MCM alternatives. The three MCM packages (b, c, and d in Figure 10) have comparable volume and weight. The Chips First package has the second highest weight due to the added mass of the thick ceramic layer in which the die

cavities reside, shown as the cross–hatched area in Figure 10(b), profile view. The MCM with Short Loaf SRAM has the lowest weight, since, unlike the short stack configuration, the short loaf memory stack does not require a ceramic interposer to interconnect the memory die to the substrate. Rather, the signal lines on each memory die are routed to one edge of the die, similar to a short stack, and connections to the lines are simply made to the substrate when the short loaf is mounted on edge. On the other hand, the height of the short loaf when mounted on edge gives this packaging alternative a larger volume. As a result, the VCOS MCM with Short Stack SRAM has the lowest volume and weight of these alternatives.

Table 6. Summary of Processor Module Package Alternatives

Package	Size (LxWxH, in.)	Volume (in^3)	Weight (lbs)
Standard PCB	5.0 x 5.0 x 0.35	8.75	0.871
Chips First, Short Stack SRAM	2.4 x 2.4 x 0.35	2.016	0.260
VCOS w/ Short Stack SRAM	2.4 x 2.4 x 0.35	2.016	0.239
MCM w/ Short Loaf SRAM	2.4 x 2.4 x 0.7	4.032	0.210

4.1.2 Global Memory Module Packaging

The alternatives for global memory packaging included in this study include advanced 3–D techniques being developed at Irvine Sensors, Inc. and IBM Microelectronics in Burlington, VT. The study focused on two categories for global memory: Static RAM (SRAM) and Dynamic RAM (DRAM). DRAM is a recent development in space–based memory applications, having wider use due to the acceptance of COTS products in space, and because of its higher density compared to SRAMs. The 3–D memory packaging development at IBM Burlington, in conjunction with Irvine Sensors, uses IBM's 16 Mbit DRAM devices. Up to 48 DRAM die are connected in a loaf fashion, forming what is commonly called a memory cube. Each cube yields 40 working die, with a storage capacity of 640 Mbits. Both DRAMs and SRAMs are being developed in short stack and loaf configurations by several companies, including Irvine Sensors and Texas Instruments. For the Global Memory package study, short stack and cube memories were assumed to be mounted as a single unit package, as shown in Figure 11. Loral is baselining this cube memory package in several space–based memory applications.

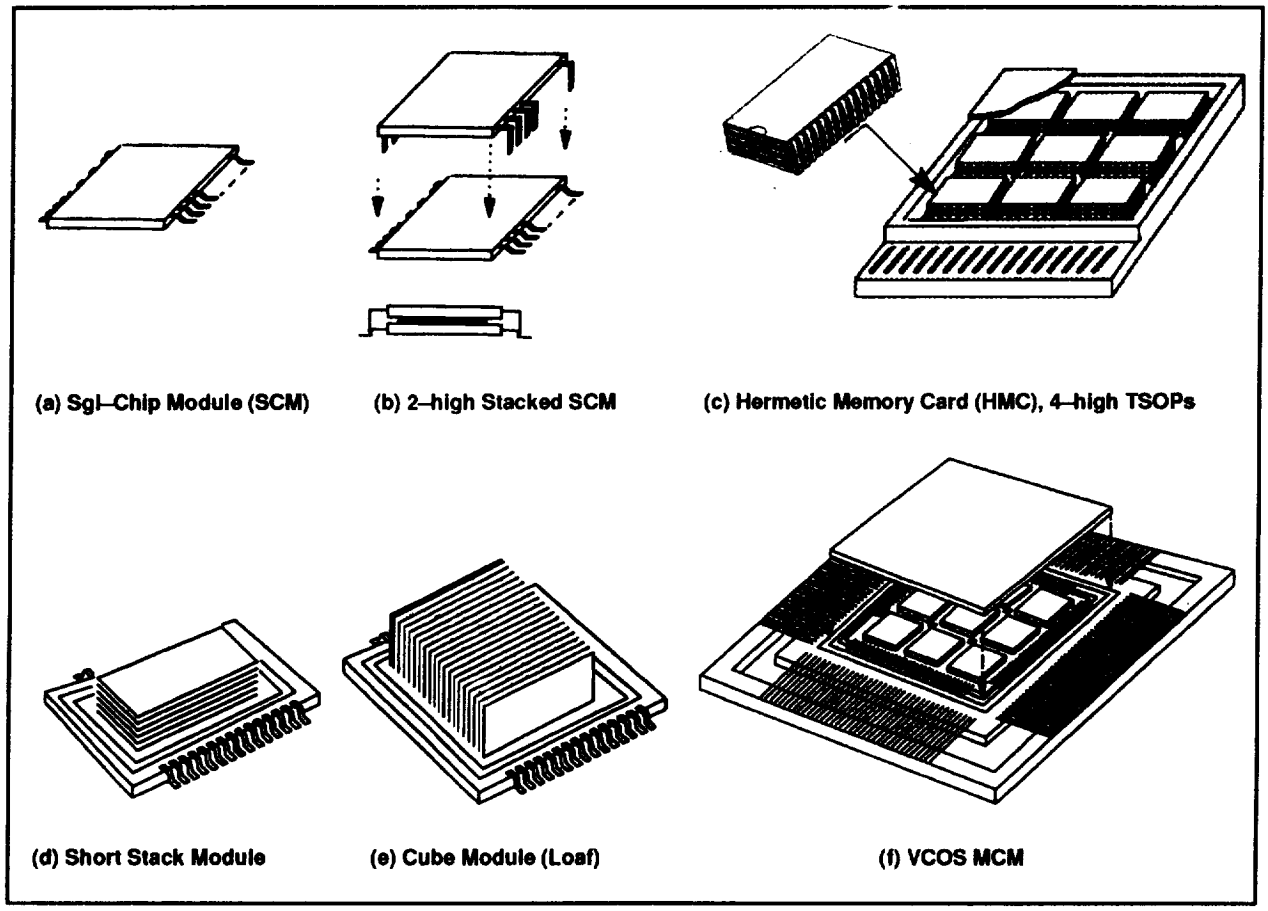

Figure 11. Global Memory Module Packaging Alternatives (not shown to scale)

In addition to 3–D die packaging, single–chip modules (SCM) and stacked modules were also considered. SCMs are standard SRAM packages used in space applications. These can be stacked two–high, as was done in the Standard PCB packaging alternative for the Processor Module in Section 4.1.1. IBM Burlington has also stacked 16 Mbit DRAMs in single–chip thin small outline packages (TSOP) to create a 4–high, 64 Mbit stack. Loral has developed a hermetic memory card (HMC) containing nine 4–high TSOP stacks, for a total storage capacity of 512 Mbits plus error correction bits per HMC. This HMC package is used on the JPL Mars Pathfinder flight computer.

In summary, the alternatives for SRAM packaging include: single–chip modules (SCM), both 1–high and stacked 2–high; multi–chip modules (MCM), with 1–high and stacked 4–high bare die; and short stack modules, both 4–high and 6–high bare die. (Note that the 6–high short stack, while considered here, may ultimately be developed as a 5–high or 8–high product, subject to busi-

ness conditions for 3–D packaging manufacturers. HMC and cube loaf packaging were not considered for SRAMs because no manufacturer has announced plans for such a product.) Alternatives for DRAM packaging include: SCM; MCM; hermetic memory card (HMC); short stacks; and the cube loaf module. The SRAM and DRAM alternatives are summarized in Table 7 and Table 8 below.

Table 7. Comparison of SRAM Global Memory Packaging Alternatives

	SCM 1–hi	SCM 2–hi	MCM 1–hi	MCM 4–hi	Stack 4–hi	Stack 6–hi
Chips/Module	1	2	9	36	4	6
Capacity (Mb)	1	2	9	36	4	6
Weight (gm)	5	10	30	37	10	11
Area (in^2)	0.8	0.8	5.8	5.8	0.9	0.9
Card Pitch (in) *	0.7	0.8	0.7	0.9	0.7	0.9
Mb/in^2	1.3	2.5	1.6	6.2	4.4	6.7
Mb/in^3 *	3.6	6.3	4.4	13.8	12.7	14.8
Mb/lb *	28.6	43.5	37.5	141.0	81.6	117.2

* Notes:
1 Mbit SRAM chips/die used in all cases in this table.
Second level packaging included in these calculations. This adds 0.06 lb/in^2 to weight.
Also, the card pitch assumes that modules are mounted on both sides of the 2nd level package (i.e., the printed circuit board).

Table 8. Comparison of DRAM Global Memory Packaging Alternatives

	SCM 1–hi	SCM 2–hi	HMC 4–hi	MCM 1–hi	MCM 4–hi	Stack 4–hi	Stack 6–hi	Loaf
Chips/Module	1	2	36	9	36	4	6	40
Capacity (Mb)	16	32	576	144	576	64	96	640
Weight (gm)	5	10	110	30	36	10	11	30
Area (in^2)	0.7	0.7	9.0	5.8	5.8	0.8	0.8	1.5
Card Pitch (in) *	0.7	0.8	0.8	0.7	0.9	0.7	0.9	1.4
Mb/in^2	22.9	45.7	64.0	24.8	99.3	80.0	120.0	426.7
Mb/in^3 *	65.3	114.3	160.0	70.9	220.7	228.6	266.7	609.5
Mb/lb *	500.0	744.2	1125.0	600.0	2274.9	1391.3	1991.7	5765.8

* Notes:
16 Mbit DRAM chips/die used in all cases in this table.
Second level packaging included in these calculations. This adds 0.06 lb/in^2 to weight.
Also, the card pitch assumes that modules are mounted on both sides of the 2nd level package (i.e., the printed circuit board).

In comparing the packaging alternatives for global memory, the second–level packaging effect was included. A standard printed circuit board with modules populated on both sides of the PCB was assumed for the second level package. The card pitch; i.e., the distance between two PCBs, takes into account the height of the modules on each side of a PCB. Also, the second–level package adds 0.03 pounds per square inch to the weight of each module, or 0.06 lbs/in^2 for a PCB with modules on each side. The reason for including the second–level package effects was that it provided a more realistic comparison among the alternatives. For instance, short stack modules would reflect even higher storage capacity per pound when compared to SCMs without the effect of the second–level packaging, given the small mass of the short stack modules.

For both SRAM and DRAM package alternatives, multi–chip modules with stacked memory die show slightly better storage density than short stack modules. Note that this comparison considers only the storage density for global memory, and not the cost or design flexibility for any given alternative. As the tables show, MCMs and cube loafs have the highest density per weight and per volume.

4.1.3 I/O Module Packaging

The I/O Module package study focused on highly integrated, modular packaging alternatives for various interface standards and peripheral system logic. MCM packaging was chosen for compatibility with the Processor Module architecture, as well as with the Global Memory Module results. This study did not address those parts of an I/O architecture that can or must be packaged separately from a processing node, such as the optical coupling assembly for 1773B interfaces. Only those parts that interface with the processor node were considered, including the I/O interface circuit, the drivers/receivers, any transformers, and related logic such as oscillators and buffers.

As shown in Figure 4 on page 16, an I/O module contained in a 308–pin MCM package has more than adequate space for a 1553B interface plus peripheral oscillators, when both sides of the MCM substrate can accommodate devices. This allows critical system clocks and other I/O logic to be placed on the MCM as well.

For the packaging study, the I/O Module defined in Section 2.3.3 was sized using a Chips First (e.g., HDI) MCM approach, as well as a standard MCM with devices mounted on both sides of a ceramic substrate. For the Chips First package, it was assumed that a 3–D approach is possible, where die can be placed in milled cavities on the top and bottom of a ceramic substrate, with levels of metal interconnect over the top and bottom of the substrate. Since both approaches have very similar die arrangements, the results of the sizing study show identical volumes, with only a slightly higher weight for the Chips First approach, due to the thicker ceramic substrate that holds the milled die cavities. The results are summarized in Table 9 below.

Table 9. Comparison of I/O Module Packaging Alternatives

Package	Size (LxWxH, in)	Volume (cu. in.)	Weight (lbs)
Chips First (HDI)	2.4 x 2.4 x 0.475	2.734	0.267
MCM Ceramic Subs.	2.4 x 2.4 x 0.475	2.734	0.257

4.2 Packaging Study Observations

The following observations relevant to AFC were noted during the course of the VLSI packaging study:

- Realistic measures of storage density per weight and volume are heavily influenced by the second level package effects. The system level requirements can dictate the second level board packaging for a given mission, and hence can also determine the optimum type of packaging used for mass memory. Also, memory chip stacking yields the greatest bit density for mass storage.
- The volume and weight of an AFC package is influenced by the number of signal pins required, and the lead pitch (e.g., the distance between pins) of the package. As memory and processor logic densities increase, the node level designs become I/O constrained, where the size of the board/package is determined by the physical limitations of the pin–outs, rather than by the size of the silicon die. This study showed that AFC goals can be met with state–of–the–art and near–term processor and memory designs, using standard 2" square 308–pin I/O MCM packages.
- An additional worthwhile packaging study would be to investigate ways to reduce second level packaging effects, such as by stacking MCMs whereby an AFC processing node would consist of an MCM stack, containing a Processor Module, I/O Module, and, if necessary, a Global Memory Module.

5. ISSUES AND FUTURE TRADE STUDIES

Architecture

Earth science and remote sensing missions are raising the processing throughput requirements for on–board computers, due to significant improvements in imaging instruments over the recent years. Image manipulation activities, including filtering, cropping, and compression, are being migrated from ground stations to on–board processors. To address these applications, digital signal processors that can survive in space environments are being developed, such as the Loral/Analog Devices AD210x0 effort.

To leverage COTS technology for space, another DSP being adapted for space is the Texas Instruments (TI) 320C30 DSP. The 320C30 is a widely used commercial programmable DSP, and is also targeted as a microcontroller for space use. Towards the end of this study, Loral Federal Systems Manassas became involved in the effort by Phillips Laboratory and TI to develop a radiation hardened 320C30. The timing of this event did not allow for the TI 320C30 to be included in this study. Also, since the plans for this effort are not yet final, the Development Plan in Section 6 does not reflect any work on the TI 320C30. However, it is feasible that a rad–hard 320C30 would become available during the AFC 1996–2000 development schedule time frame.

VLSI Technology

As processor and memory devices improve in performance and power consumption, interface circuitry becomes a more dominant power concern. The increasing data rates for image processing applications in space require higher speed interfaces. Standard CMOS drivers and receivers may not be capable of such speeds, or may require too much power to do so. Other technologies, such as BiCMOS, GaAs, and ECL, can be used to achieve the proper throughput and power. These technologies are also associated with optical interfaces. A future trade would be to study these technologies, including SOI, to establish design baselines for image processing applications.

Packaging

The packaging study focused mainly on weight, volume, packing and storage density, and high integration of the AFC node architecture. Other issues that are either candidates for trade studies, or

are to be addressed during a given mission systems definition, include yield, rework, testability, reliability, and thermal characteristics of the packaging approach. Especially for MCM solutions, yield and rework are important drivers in choosing or developing a packaging approach. This relates to the ease and cost of achieving fully functional modules throughout the manufacturing process, and extends from the VLSI fabrication stage through packaging.

6. DEVELOPMENT PLAN

The AFC Development Plan described in this section relies on current and planned efforts at Loral Federal Systems Manassas. In some cases, these efforts rely on the completion of third party developments, such as the short stack SRAM memories by Irvine Sensors.

6.1 Product Development at Loral

To provide a perspective on Loral's space products development, Figure 12 shows an evolution of space processor products over recent years at Loral. The products are categorized according to performance throughput, with lower throughput (0 to 5 MIPS) processors based on the 16–bit, MIL–STD–1750A GVSC heritage. The most recent Loral GVSC effort is to supply flight computers for Space System Loral's Globalstar constellation and the future generation of Omegasat spacecraft.

The RAD6000–SC processor provides the product core for flight computers in the 5 to 35 MIPS range on Figure 12. Current and planned products include the JPL Mars Pathfinder flight computer, the Phillips Laboratory ATIM 32–bit computer, and the RAD6000–SC MCM for Global Positioning System (GPS) designs at Space Systems Loral. Note that the shaded, horizontal arrows along the top of Figure 12 show the parallel evolution of IBM's commercial POWER and PowerPC architecture, which provides the design baseline for Loral's general–purpose space processors.

For performance over 35 MIPS, Loral has the RAD6000 multi–chip (MC) processor chip set. This was actually developed before the RAD6000–SC, and the development work on RAD6000–MC VME boards led to the JPL Mars Pathfinder solution. For future high performance processing, Loral plans to license and transfer the PowerPC 604 architecture from IBM. The PowerPC 604 is being baselined in for future ASCM/ATIM development, as well as in this AFC study.

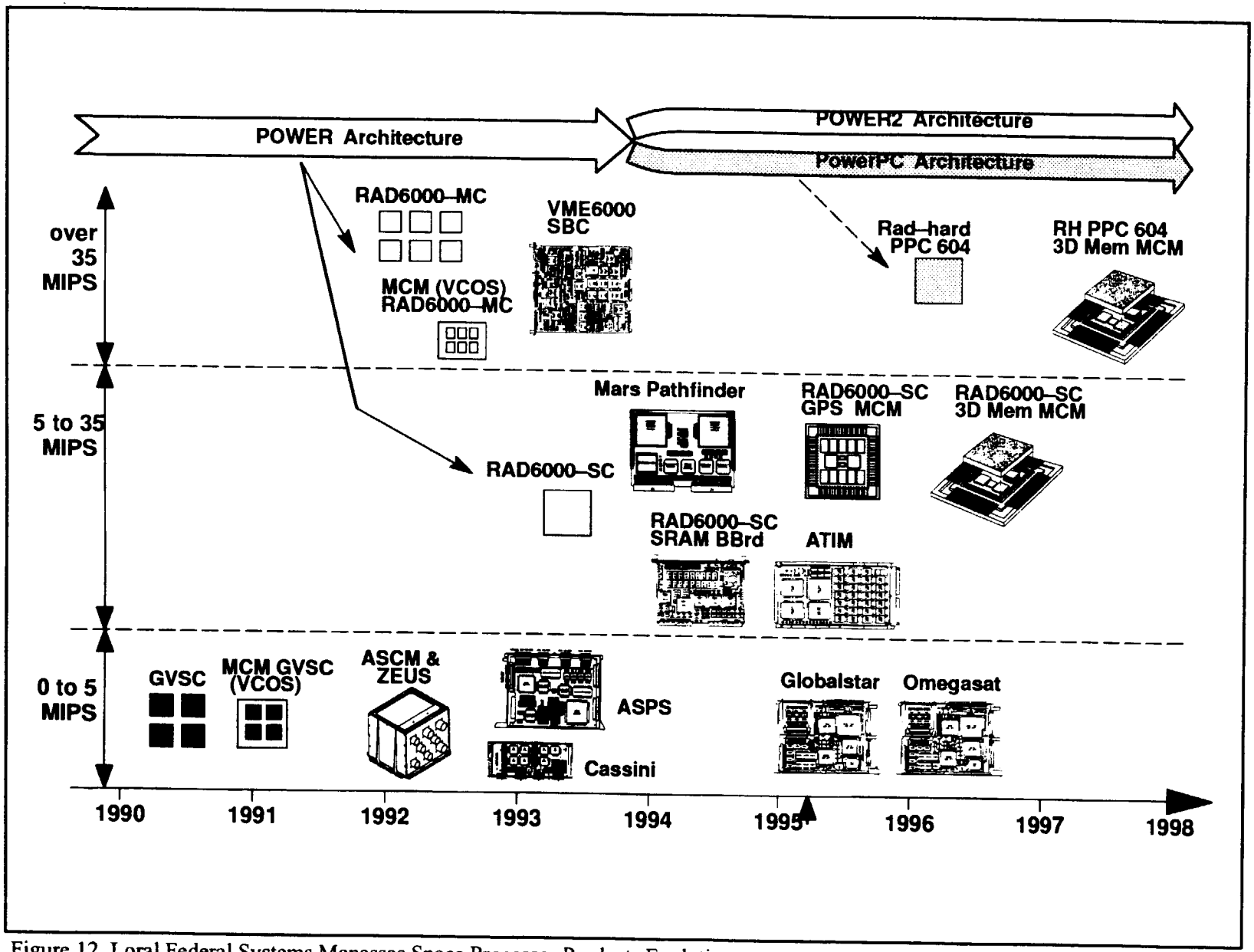

Figure 12. Loral Federal Systems Manassas Space Processor Products Evolution

6.2 Development Plan

Figure 13 presents a high level development plan for the AFC processing node architecture defined in this study. The plan relies on existing and near–term development work at Loral, including: ASCM/ATIM 32–bit RAD6000–SC flight computer; JPL Mars Pathfinder flight computer; AISM radiation hardened DSP; and high density memory cubes. The latter two programs also rely on development by other companies, specifically Texas Instruments, Analog Devices, Irvine Sensors and IBM Microelectronics. It should be noted that this schedule represents a road map and general time table for the AFC development goals in the 1995–2000 time frame, and should not be construed as the actual development schedules or milestones for the specific programs included.

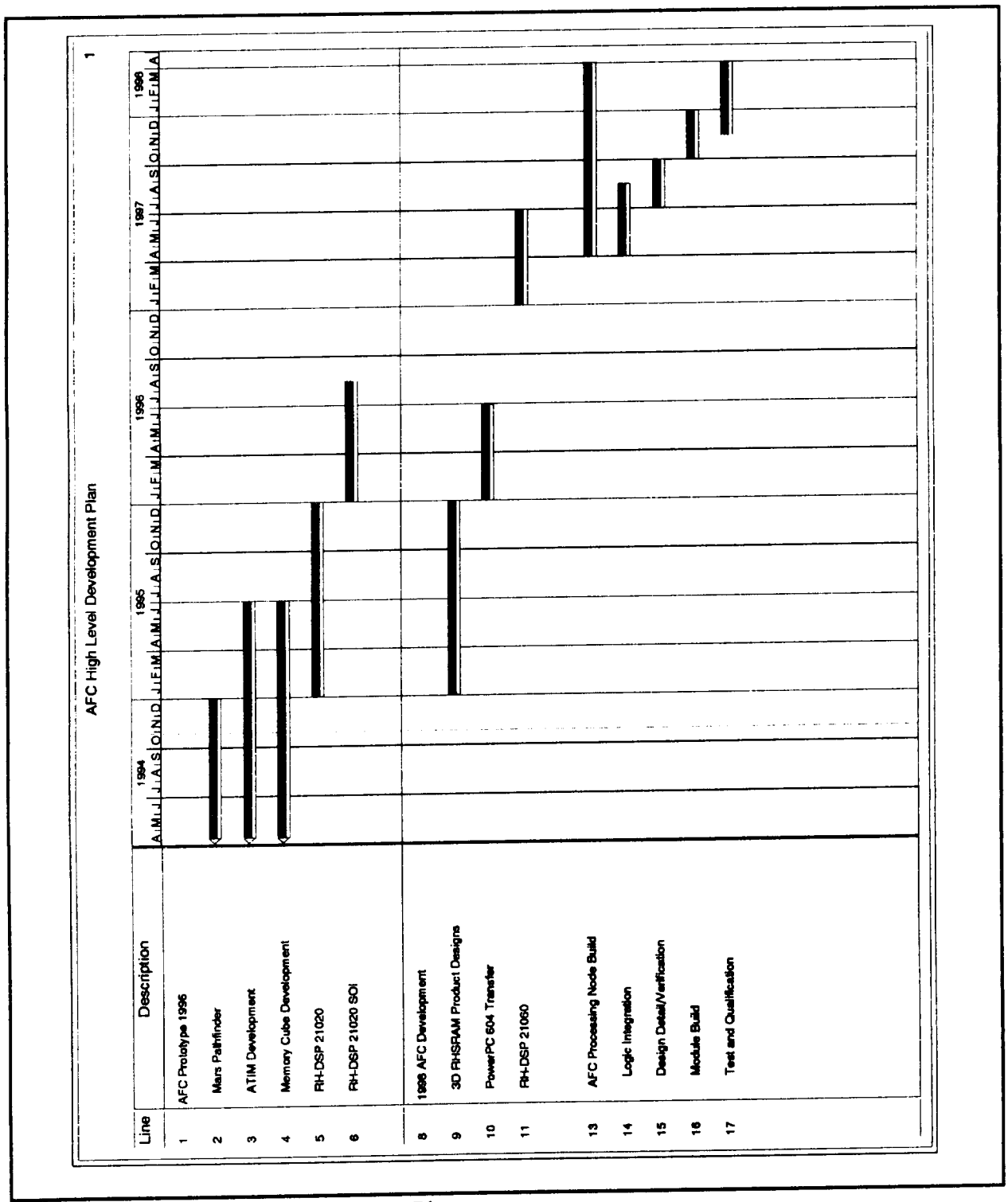

Figure 13. High Level AFC Development Plan

7. CONCLUSION

This special study has defined an AFC processing node architecture that consists of one or more multi–chip modules. Each node may consist of a processor MCM and an I/O MCM, with additional processor, I/O, and global memory MCMs as needed. The modular, building block approach uses VLSI technology and packaging methods that demonstrate a feasible AFC module in 1998 that meets the AFC goals. The defined architecture and approach rely on current state–of–the–art development and technology that can demonstrate a clear low–risk, low–cost path to the 1998 production goal, with intermediate prototypes in 1996.

The Architecture study task showed that current commercial processor designs, when transferred to radiation–hardened VLSI processes for space use over the next few years, are capable of providing single–node and multi–node processing for both spacecraft control and payload signal processing applications. Existing federal and civilian government programs, specifically the Phillips Laboratory ASCM/ATIM/AISM programs and the JPL Mars Pathfinder mission, provide the architecture and design heritage for fault tolerant flight computers that will be incorporated into the AFC development. In addition, as digital signal processors become more widely used and available for space applications in the near future, additional design trades can be conducted on the various DSPs that are suitable for space missions.

The VLSI technology study task showed that radiation hardened CMOS processes can meet AFC 1998 goals, but that additional studies would be beneficial to determine RHCMOS capabilities to meet beyond–2000 AFC performance. SOI technology is likely to become mature enough to meet future AFC requirements. Other technologies, such as GaAs, BiCMOS, and ECL, are needed to meet the increasing data transfer rates required by image processing instruments on spacecraft. This study identified parameters and characteristics of VLSI technology that are essential or desirable to development of an AFC specification.

To foster compatibility between commercial and rad–hard fabrication, and to foster design transfer between the two, the space community should encourage and pursue technology drivers that are common to both commercial and space areas. These drivers include low power designs and

technologies, design for fault tolerance, static designs, integrated packaging, and licensing of VLSI fabrication technologies.

The packaging study task showed that the defined AFC processing node architecture approach using MCM building blocks is feasible, using existing standard 2.1" square MCM packages. This represents a low–cost, low–risk path to the 1998 AFC module. Additional trade studies would be beneficial to evaluate cost, yield, and manufacturability issues with more advanced MCM packaging, including stacked MCMs.

The packaging study also showed that second level package effects can heavily influence overall system–level weight and volume for a processing node. Also, the volume and weight of an AFC package is influenced by the number of signal pins required, and the distance between the pins on the package.

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13. ABSTRACT (*Maximum 200 words*)

This report documents a special study to define a 32-bit radiation hardened, SEU tolerant flight computer architecture, and to investigate current or near-term technologies and development efforts that contribute to the Advanced Flight Computer (AFC) design and development. An AFC processing node architecture is defined. Each node may consist of a multi-chip processor as needed. The modular, building block approach uses VLSI technology and packaging methods that demonstrate a feasible AFC module in 1998 that meets that AFC goals. The defined architecture and approach demonstrate a clear low-risk, low-cost path to the 1998 production goal, with intermediate prototypes in 1996.

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