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# NASA Dryden Flight Research Center

# "PSC Implementation and Integration"

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 1

## PSC Hardware Description

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# Dual Engine PSC Architecture
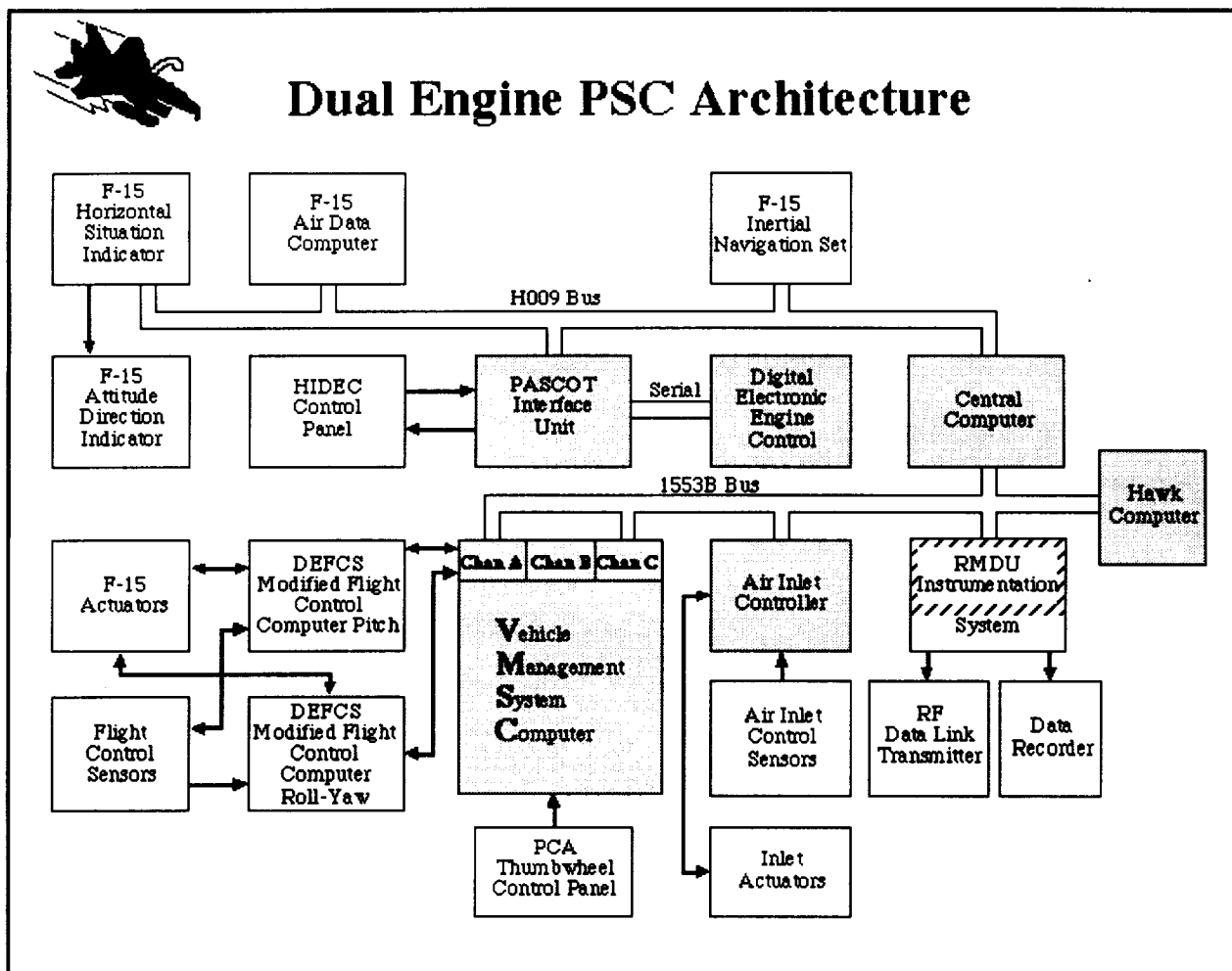


## PSC HARDWARE DESCRIPTION

In this section, the PSC hardware will be described. The Hardware Architecture, Vehicle Management System Computer, Pilot Interface, and PSC Mode Selection will be discussed.

The primary computers in the system architecture are the Digital Electronic Engine Controls (DEECs), Electronic Air Inlet Controllers (EAICs), Vehicle Management System Computer (VMSC), Central Computer (CC), and the PASCOT interface unit. The ROLM HAWK computer was used for early testing of the PSC logic and hosted the PCA algorithm. These computers are linked together by data buses which allow information exchange from one to another.

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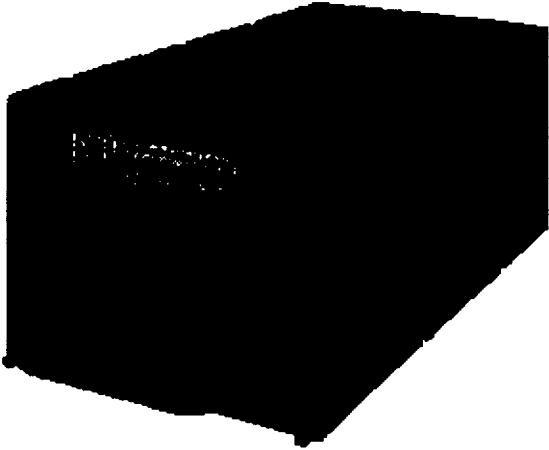
## "PSC Implementation and Integration", page 2

## Vehicle Management System Computer (VMSC)

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# Vehicle Management System Computer

## Advanced Computer Architecture

- Motorola 88000 RISC Architecture
- Three Redundant Channels
- Three Processors/Channels
- High Speed FO Bus Provisions for VMS
- 1553 I/O for Avionic and VMS

## Flight Quality Design

- F-15 Flight Worthiness
- Replaces DEFCC
- Expands VMS Flight Demo Capability
- Flight Tested in NASA F-15

## VMSC Provides

- State-of-the-Art Capabilities
- High Throughput (11-15 MIPS/ Processor)
- Large Memory to 4.5 MBYTE/ Processor Plus Global Memory
- Integrated Ada and Fortran Environment

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VEHICLE MANAGEMENT SYSTEM COMPUTER (VMSC)

The Vehicle Management System Computer (VMSC) has state–of–the–art capabilities which make dual engine optimizaton possible. The VMSC has three redundant channels with up to three processors per channel. It features high speed inter–channel communication and Motorola 88000 RISC architecture. Each processor has large local memory and is capable of operating at 11 to 15 million instructions per second.

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**"PSC Implementation and Integration", page 3**

**VMSC Channels**

VMSC Circuit Card Layout
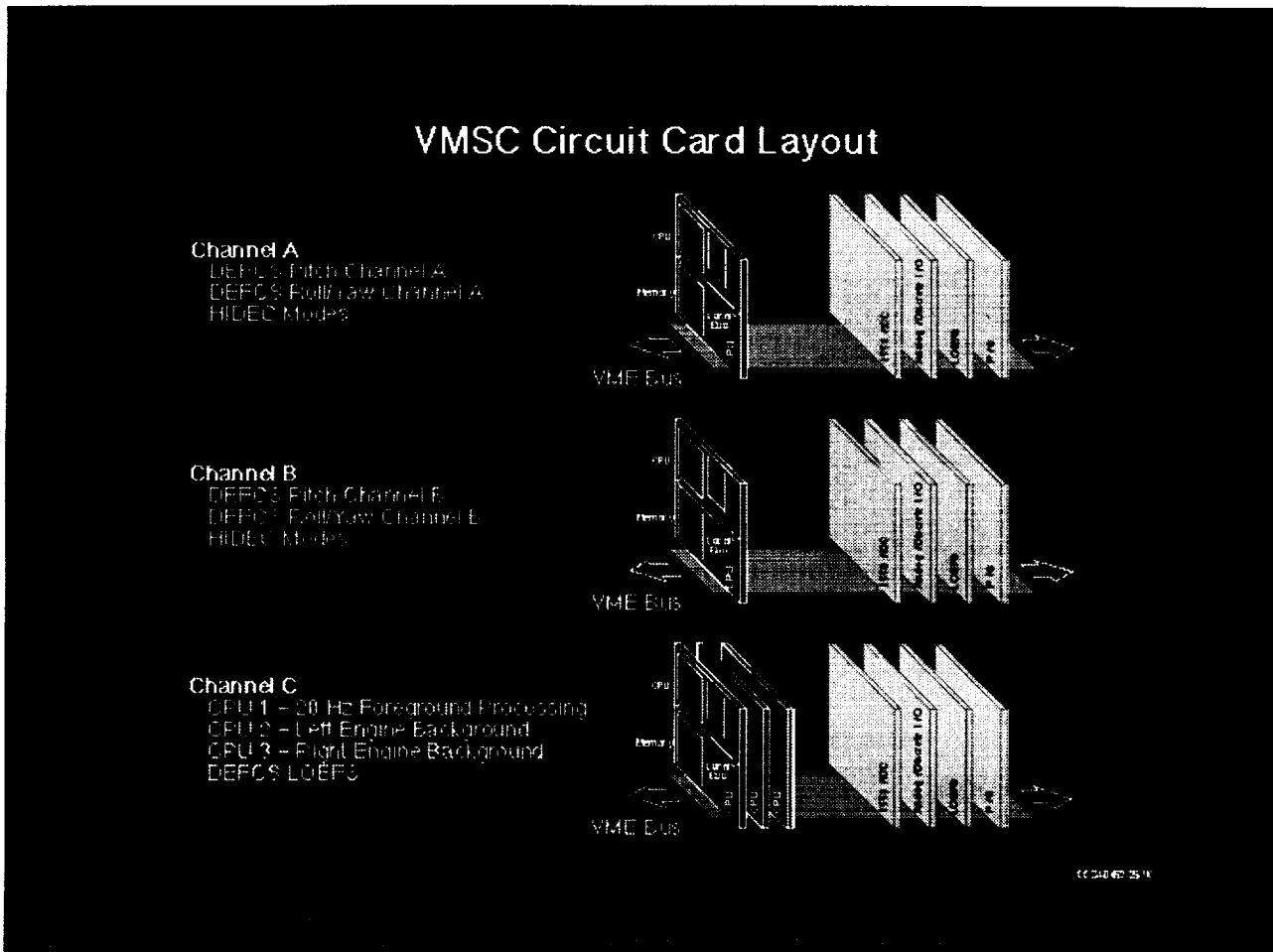
**VMSC CHANNELS**

Channels A and B of the VMSC contain the basic F–15 flight control laws. Each channel contains one 1553/Inter–channel communication (ICC) card, two analog/discrete I/O cards, one power supply (P/S) card, and one CPU. Each CPU contains Pitch and Roll/Yaw flight control laws thus providing dual redundancy.

Channel C is dedicated to the PSC control laws. It contains one 1553/Inter–channel communication (ICC) card, one analog/discrete I/O card, one P/S card, one LOFES card and three CPUs. The first CPU contains the foreground logic which executes at 20 hertz. The second CPU contains the logic for the left engine optimization and the third CPU contains the logic for the right engine optimization. The three CPUs operate concurrently.

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## "PSC Implementation and Integration", page 4

## Pilot Interface

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F-15 No. 8 PSC Crew Station

PSC Upfront Panel

Paddle Switch

Couple/ Uncouple

NCI

PSC Control Panel

Computer Control Panel
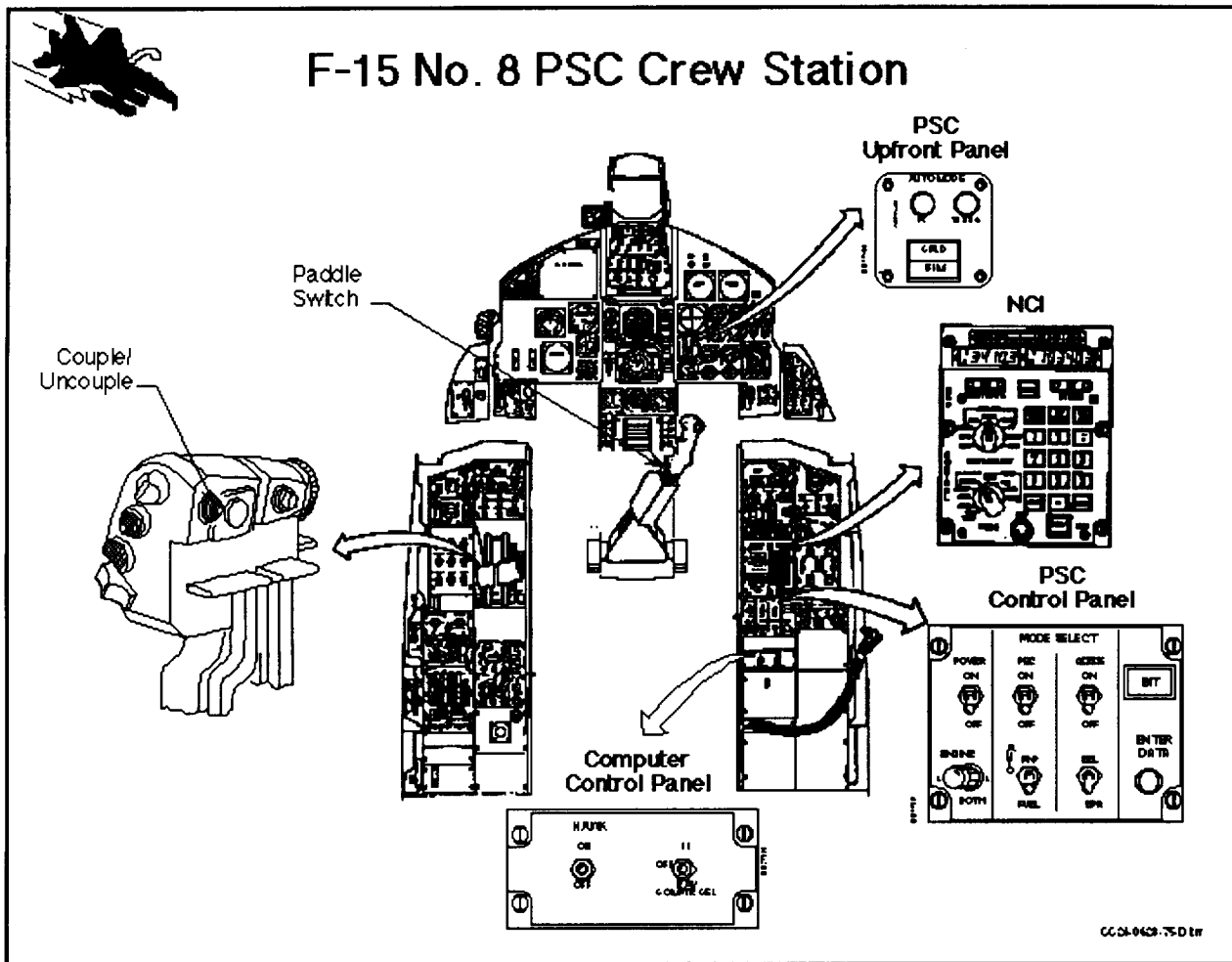
## PILOT INTERFACE

The crew station in F–15A ship 8 has been configured to allow the pilot to interface with the PSC control laws. The pilot interfaces are the couple button, the paddle switch, the PSC control panels, the HUD, and the NCI.

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 5

### PSC Couple Button

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## PSC System Engagement

PSC Couple Button

Autopilot/ Disengage Switch (Paddle Switch) PCS Emergency Disengage
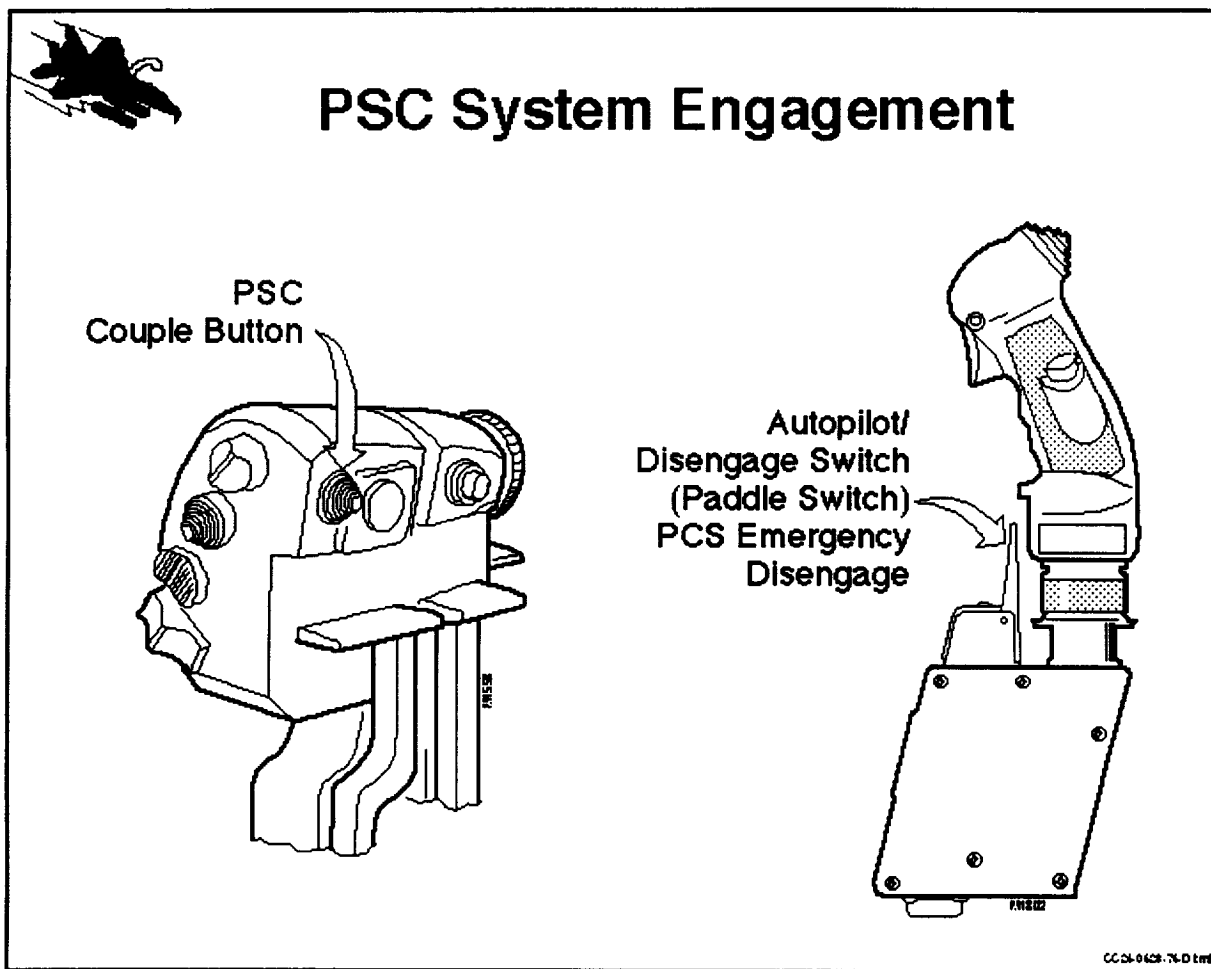
## PSC COUPLE BUTTON

The PSC couple button, located on the throttle, is the only means of coupling PSC. The couple button can also be used to uncouple PSC by depressing the button when PSC is coupled. The paddle switch, located on the stick allows the pilot to rapidly uncouple PSC in case of an emergency.

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 6

## PSC Control Panels

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# PSC Control Panels

### Control Panel

| MODE SELECT | | |
|---|---|---|
| POWER | PSC | ADECS |
| ON | ON | ON |
| OFF | OFF | OFF |

BIT

ENTER DATA

ENGINE

L  R

BOTH

A U T O

FNP

FUEL

EEL

EPR

— PSC Mode Switch

### Computer Control Panel

HAWK

ON

OFF

OFF

I I

RAV

### Upfront Panel

AUTO MODE

H I D E C

FC   TH/ENG

CPLD

IFIM
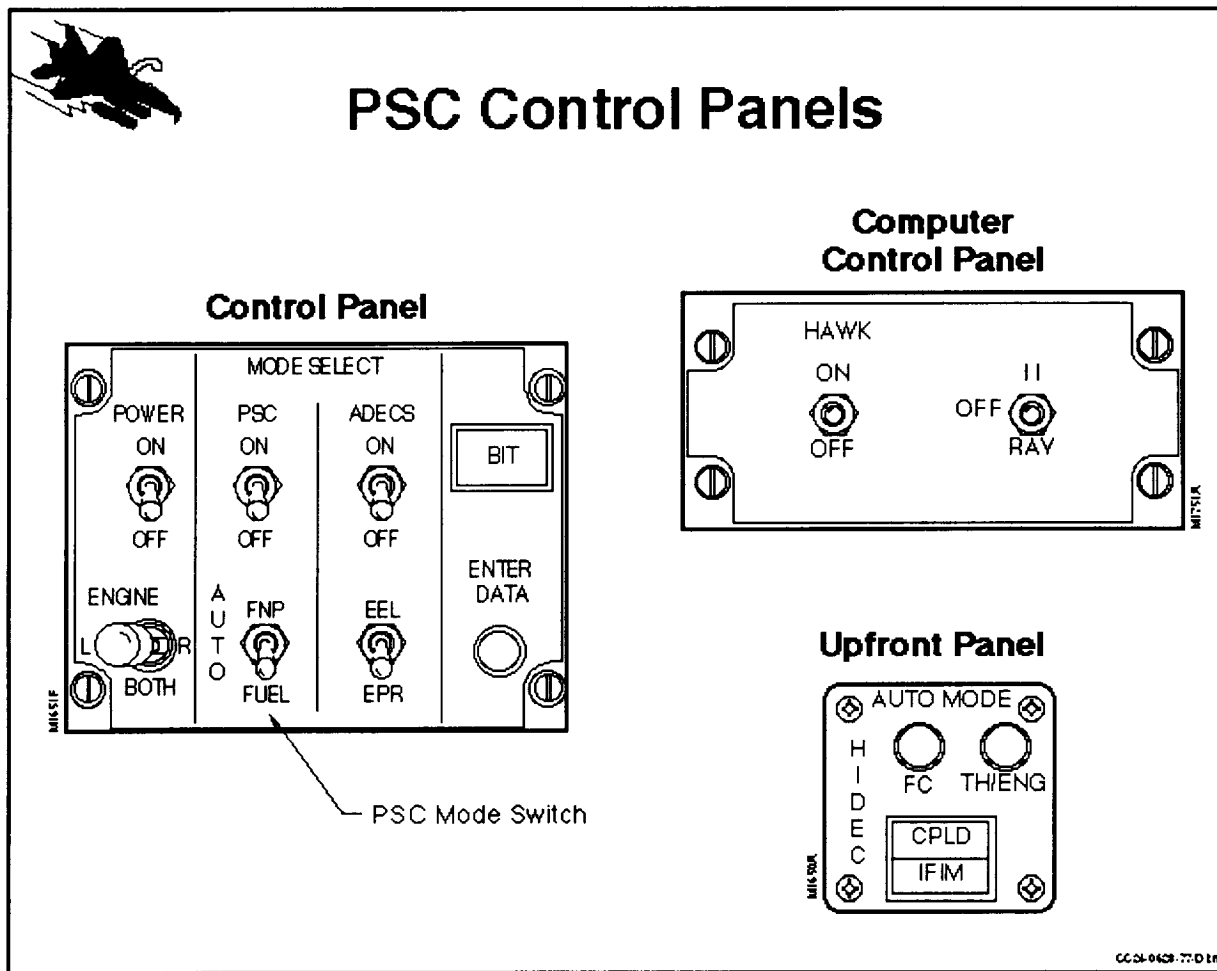
## PSC CONTROL PANELS

The PSC control panel and the computer control panel allow the pilot to select various PSC or HIDEC modes, select the engine to be optimized, initiate BIT, enter NCI data, power the Hawk computer, and reset VMSC channel C. The upfront panel indicates that a mode has been selected which will send trims to the engine by lighting the TH/ENG light, that PSC is coupled by lighting the CPLD light, and that a system in–flight integrity management error has occurred by lighting the IFIM light.

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## "PSC Implementation and Integration", page 7

## Navigation Control Indicator (NCI)
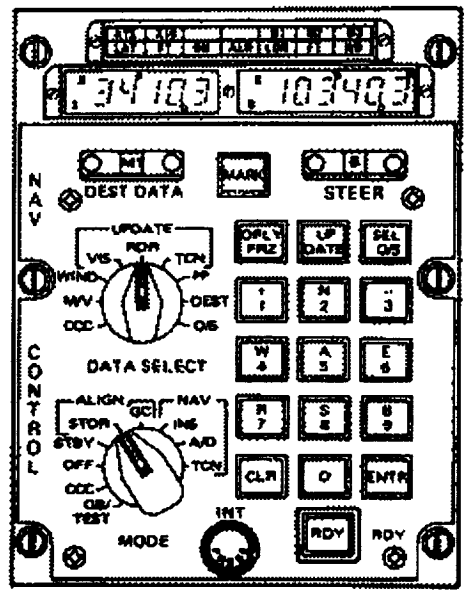
# NCI Selectable Options

## • NCI Can Be Used By Pilot to Modify the Control Laws In-Flight

### Navigation Control Indicator

**Input Procedure**

1. Mode Switch = INS
2. Data Select to Destination
3. Destination Data to "8" or "9" or "10" or "11"
4. Depress Ready (RDY) Button (Lights)
5. Enter Data:
   Latitude:   N X X X X X ENTER
   Longitude: W X X X X X X ENTER
   Altitude:    A+ X X X X X ENTER
6. Depress Enter Data Button on PSC Control Panel

## NAVIGATION CONTROL INDICATOR (NCI)

The NCI can be used by the pilot to modify the PSC control laws in-flight. It is used to select sensor bias corrections, system gains, trim biases, optimization limits, and logic switches. The NCI is also used to select ground maintenance functions and initiate preflight BITs during ground tests.

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 8

## PSC Algorithm Design Flexibility

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# Algorithm Flexibility

## NCI Entries Allow Inflight Selections

### Mode Selections
- Engine Only Optimization
- Explicit Thrust
- Optimization Without CIVV
- Optimization Without RCVV
- Velocity Hold
- Maximum Thrust at Constant FTIT
- Supersonic Rapid Decel Mode
- New/Old Stabilator Trim Drag

### System Constants Selections
- Bias on Engine Commands
- One Shot Kalman Filter
- Nominal Efficiency Curves
- Calculated Alpha and Beta in Calculator/Predictor
- Inlet Percent Critical
- Inlet Shock Displacement
- FTIT Limit
- Alpha/Beta Predictor Lead Time
- Excess Stall Margin
- Bleed Air Multiplier
- Stored Tables of Component Deterioration
- Filter Time Constant on Commands
- HAMSTR Inlet Recovery

*Maximum Flight Test Flexibility*

CC-96-0853-14

## PSC ALGORITHM DESIGN FLEXIBILITY

The PSC algorithm has been designed to have great flexibility to maximize flight test effectiveness. The NCI and the PSC control panel are used to select various optimization modes and system constants. This allows the control laws to be modified during or between flights without generating a new OFP.

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 9

## PSC Software Descriptions

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PSC SOFTWARE DESCRIPTION

The PSC software is distributed among the Vehicle Management System Computer, Central Computer, DEECs and EAICs. This section describes the major PSC modules, VMSC logic, VMSC Ch. C memory requirements, VMSC Ch. C timing, NCI variables and where they are located.

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## "PSC Implementation and Integration", page 10

## Major PSC Modules

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MAJOR PSC MODULES

The majority of the PSC modules reside in channel C of the VMSC. These modules are split between the foreground processor and two background processors. The major foreground modules are the supervisory logic, the Kalman Filter, and the stall protection logic. The major background modules are the compact engine model, compact inlet model, optimization logic, and inverse DEEC. VMSC channels A and B, the Central Computer (CC), the DEECs and the EAICs also contain important PSC modules. VMSC channels A and B contain the alpha and beta calculator/predictor logic. The CC contains the BIT/IFIM logic and the DEEC/VMSC and EAIC/VMSC data transfer logic. The DEECs and EAICs contain PSC trim command interface logic.

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# VMSC Logic Partioning
## Channels A, B and C

### Channels A and B

- One CPU Card Per Channel

- Each Channel Executes the Following Logic:
  - Digital Flight Control Laws
  - HIDEC Logic
    - ADECS
    - Inlet Integration
    - Extended Engine Life
  - Alpha/Beta Calculator Predictor
  - MUX I/O (Channel A Only)
  - Inter-Channel Communication Logic

### Channel C

- 3 CPU Cards
  - CPU 1 - FG OFP
  - CPU 2 - BG OFP (Left)
  - CPU 3 - BG DFP (Right)

Channel A  Channel B  Channel C

VMSC LOGIC PARTITIONING

The VMSC has three redundant channels with up to three CPUs per channel. Channels A and B each contain one CPU. Each CPU contains digital flight control laws, HIDEC logic, Alpha/Beta calculator predictor, MUX I/O, and inter-channel communication logic. The logic in channel A is identical to that in channel B. Channel C contains three CPUs. CPU No. 1 contains the PSC foreground logic which operates at 20 hertz. CPU No. 2 contains the left PSC background logic and CPU No. 3 contains the right PSC background logic. The three CPUs operate concurrently.

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 12

## PSC Logic in VMSC Channel C

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# PSC in the VMSC

Right BG CPU

Left BG CPU

FG CPU

### ROM

PSC OFP
- Executable Code
- Constants
- Initial Values
- NVM Data

Operating System
- ICC
- MUX
- Error Handling

### RAM

OFP
- Initialized Variables
- Variables

Operating System Shell
- Variables

Read - Only   Read/Write

CPU   *Motorola
88000
RISC Processor*

- OFP Is Executed Out of **ROM**

- Operating System Shell, PSC OFP
  Are Stored in ROM on the CPU Card

- FG and BG OFPs Execute in a
  **Multi-Processor/Multi-Memory**
  Environment

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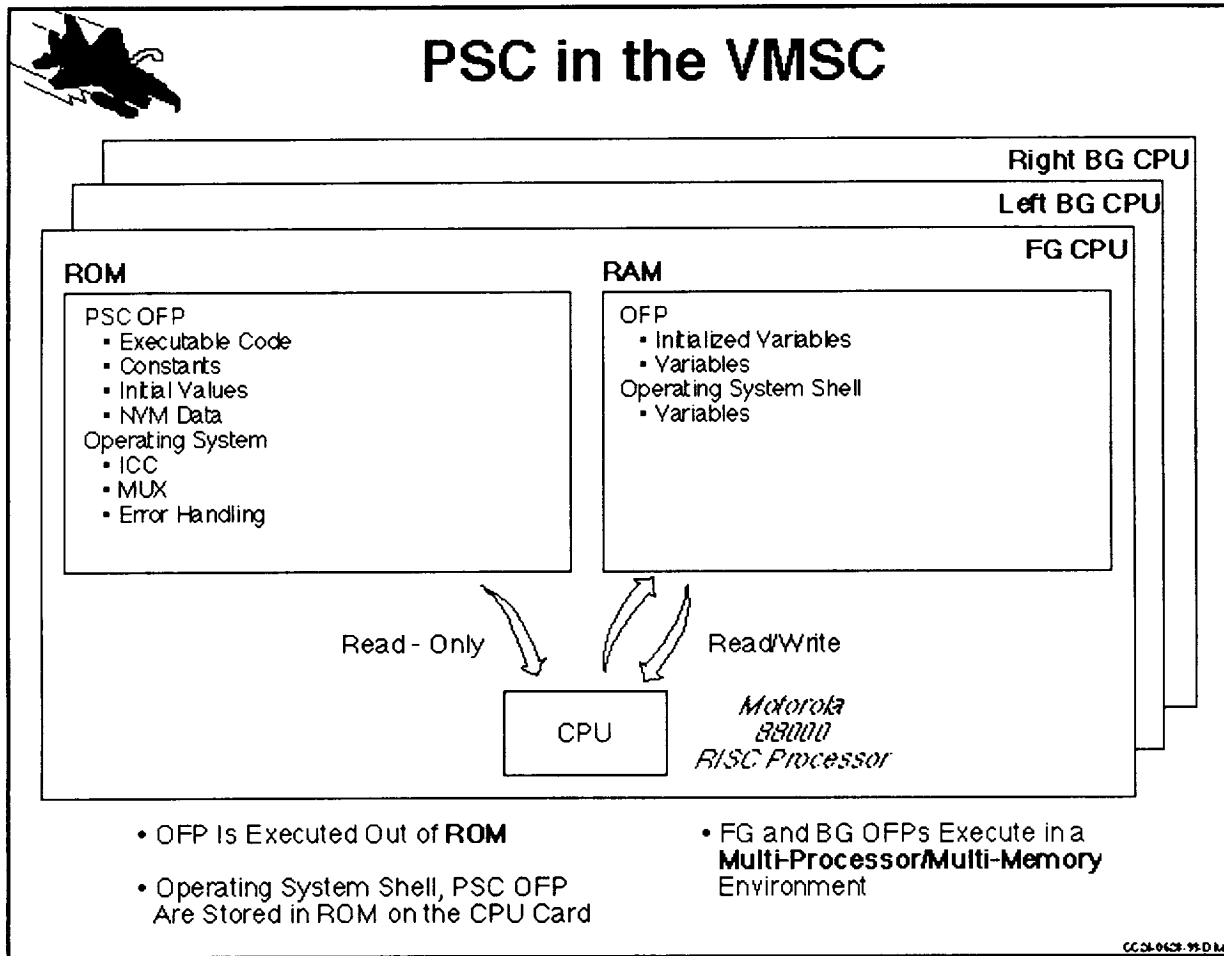
## PSC LOGIC IN VMSC CHANNEL C

The PSC logic in VMSC channel C executes in a multi-processor/multi-memory environment, unlike the Hawk which executed in a single processor. Each processor contains Read-Only-Memory (ROM) and Random-Access-Memory (RAM). The executable code, constants, initial values and the operating system are stored in ROM. The limited amount of RAM is reserved for variable memory. The CPU reads from both ROM and RAM but it only writes to RAM. The implementation is the same for all three CPUs.

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## "PSC Implementation and Integration", page 13

## VMSC Channel C Memory Requirements

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## Dual Engine Memory Requirements

**CPU 1**

**"Foreground"**
1553 MUX Interface,
Supervisory, Kalman Filter, One-Shot, . . .

Requires: 436 Kb ROM, 48 Kb RAM

**Per Card
Available Memory**
508 Kb ROM
256 Kb RAM

**CPU 2**

**"Background No. 1"**
Supersonic Inlet Model,
PSC Optimization Logic, Engine Model

Requires: 479 Kb ROM, 42 Kb RAM

**CPU 3**

**"Background No. 2"**
Supersonic Inlet Model,
PSC Optimization Logic, Engine Model

Requires: 479 Kb ROM, 42 Kb RAM

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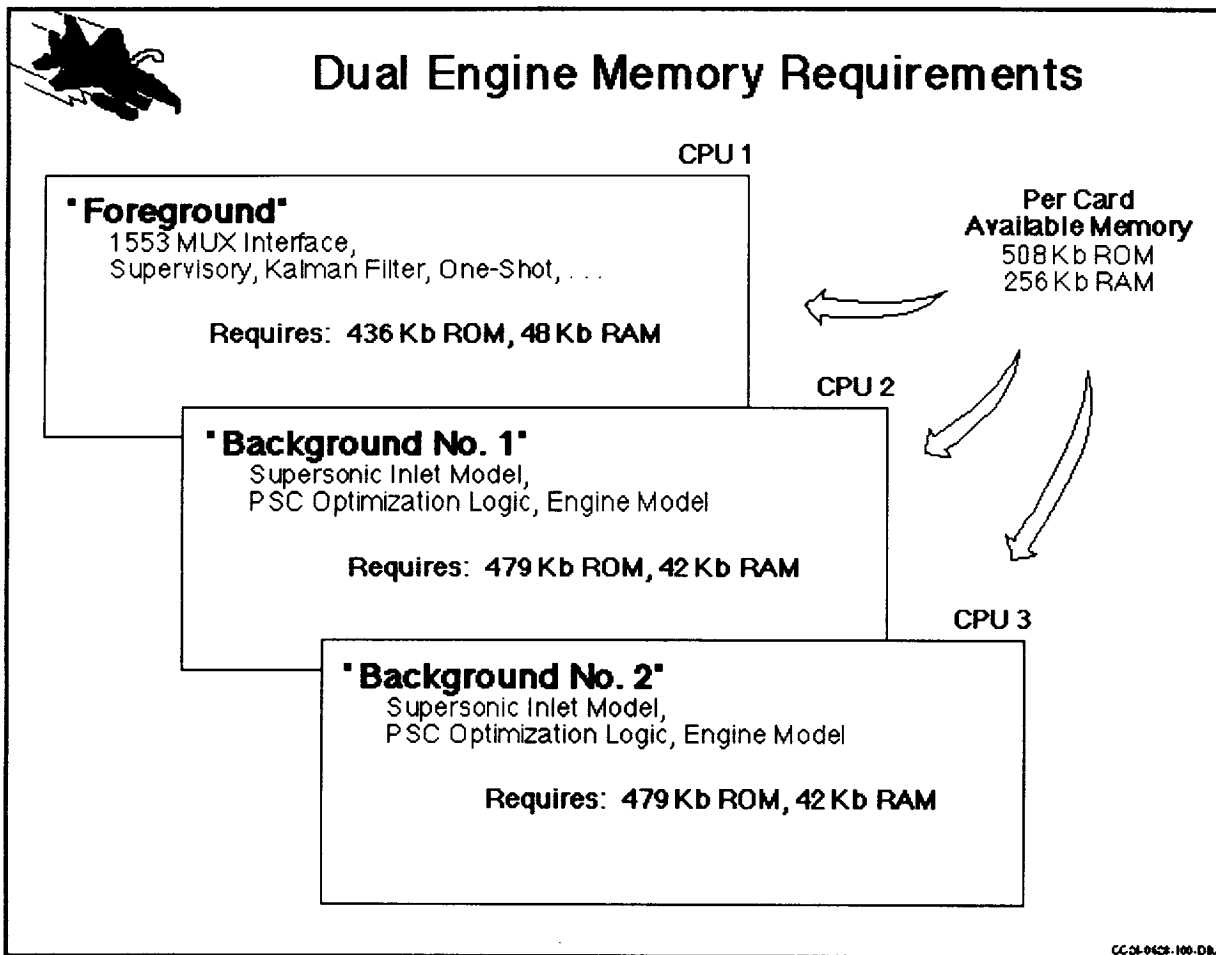
### VMSC CHANNEL C MEMORY REQUIREMENTS

The PSC control laws in channel C of the VMSC reside in three separate CPUs. Each CPU has 508
Kb of Read–Only–Memory (ROM) and 256K of Random–Access–Memory (RAM) available. Due to the
limited RAM, the executable logic is run from ROM on each CPU. The foreground Operational
Flight Program (OFP) uses 436 Kb of ROM and each background OFP uses 479 Kb of ROM. Only a
small portion of RAM is utilized. The foreground uses 48 Kb of RAM and each background uses 42
Kb of RAM.

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"PSC Implementation and Integration", page 14

VMSC Channel C Timing; Foreground Operational Flight Program (OFP)

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# Foreground Execution Rate
# in the VMSC

- **Foreground OFP Executes at a Fixed Rate**
  - 20 Hz, 50 Millisecond (mS) Frame

- **Critical Module Timing Data:**
  - Kalman Filter: 3.4 mS
  - Stall Protection: 1.4 mS

- **Foregound Frame Utilization**
  - Single Engine: 14 mS Out of 50 mS Frame
  - Dual Engine: 21 mS Out of 50 mS Frame

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## VMSC CHANNEL C TIMING

The PSC foreground Operations Flight Program (OFP) operates at a fixed rate of 20 Hz. Timing analyses have been conducted to ensure that the PSC logic will complete in the 20 Hz frame. The background logic runs at a variable rate which depends on flight conditions. Background timing is important because it corresponds to the time between PSC trim applications.

The PSC foreground OFP contains the supervisory logic which executes at 20 Hz. If a failure is detected in the supervisory logic, the system must be uncoupled quickly. Timing data has been taken which shows that during single engine operation 14 ms out of the 50 ms frame is used. During dual engine operation, 21 ms out of the 50 ms frame is used. Two key foreground modules, the Kalman Filter and stall protection use 3.4 ms and 1.4 ms, respectively.

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**"PSC Implementation and Integration", page 15**

**Background OFP**

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# Background Execution Rate in the VMSC

- **Background Runs at Variable Rate**
- **Critical Module Timing Data (Per Call Basis)**
  - Compact Engine Model:
    - 32 mS (Milliseconds)
  - Compact Inlet Model:
    - Subsonically:   16 mS
    - Supersonically:   160 mS
  - Linear Programming Logic:
    - 10 - 20 mS (Constraint Dependent)
- **Background Execution Rate is Dependant on Flight Condition**
  - Subsonically:   0.2 - 0.3 Seconds (6 Optimization Loops)
  - Supersonically:   0.45 - 0.65 Seconds (3 Optimization Loops)

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BACKGROUND OPERATIONAL FLIGHT PROGRAM (OFP)

The PSC background OFP runs at a variable rate. The execution rate is dependent on flight condition. At subsonic conditions, the background completes in 0.2–0.3 seconds, while at supersonic conditions, the background completes 0.45–0.65 seconds. The timing data show that the compact engine model and linear programming logic take 32 ms and 10–20 ms, respectively. The compact inlet model timing depends on flight condition. Subsonically it takes 16 ms while supersonically it takes 160 ms. The supersonic portion of the compact inlet model is the main reason for the large execution times required at supersonic conditions.

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## "PSC Implementation and Integration", page 16

## NCI Variables

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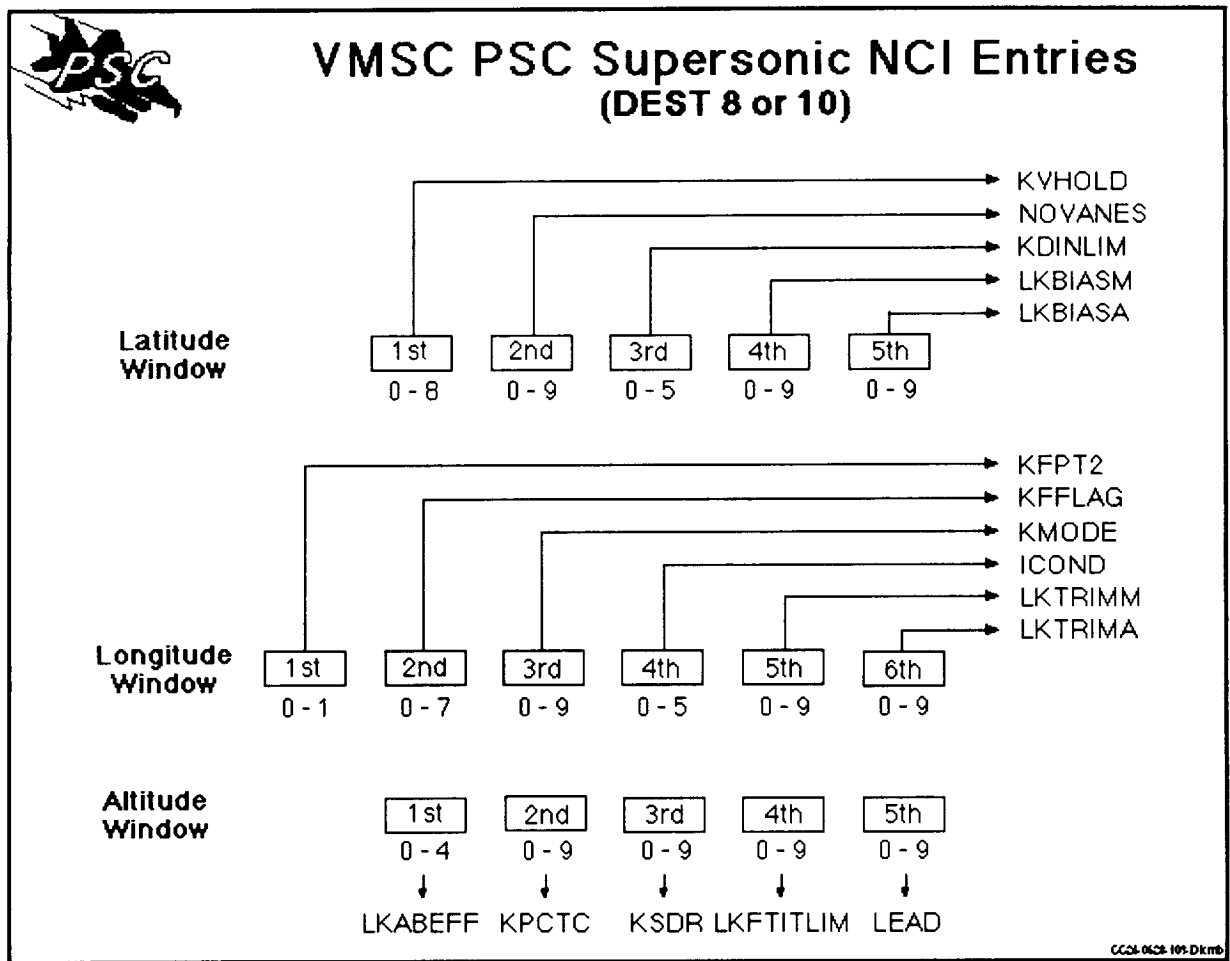


## NAVIGATION CONTROL INDICTOR (NCI) VARIABLES

The aircraft Navigation Control Indicator (NCI) is used by the pilot to modify the PSC control laws in–flight. The longitude, latitude, and altitude entries are decoded by the PSC control laws when the DATA SELECT switch is in the DEST position. The NCI is used to select switches or table pointers in the PSC control laws. This greatly enhances the experimental capabilities of PSC. There are five entries available in the latitude and altitude windows and six in the longitude window. Beyond this, the pilot can choose 2 separate definitions for each entry by setting the DEST DATA switch to an odd number for one definition or an even number for the other definition. This results in 32 available entries to modify the control laws in–flight. This chart shows the 16 entries available when an even DEST DATA position is selected.

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"PSC Implementation and Integration", page 17

Implementation of Safety Design Features

# Couple/Uncouple Logic

- Designed to Prevent Uncommanded, Unsafe, or Invalid Trim Application

- Coupling Is Initiated Only by the Pilot

- All Coupling Criteria Must Be Satisfied Before the Trims Are Applied to the DEEC/EAIC

- The Aircraft Resumes Normal F-15 Operation If Any Coupling Criteria Becomes Unsatisfied

- Pilot May Uncouple at Any Time

- Several Uncouple Methods Available to Pilot

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IMPLEMENTATION OF SAFETY DESIGN FEATURES

Several system safety design features have been implemented for PSC. These include the couple/uncouple logic, extensive In-Flight Integrity Management (IFIM), trim command limiting, engine stall protection, VMSC safety features, NCI data entry restrictions, and a limited flight test envelope.

The PSC couple/uncouple logic is designed to prevent uncommanded, unsafe, or invalid trim application. Coupling of the system can be initiated only by the pilot. An extensive set of coupling criteria must be satisfied before the system couples and if the criteria becomes unsatisfied while coupled, the system automatically uncouples. In this case, the aircraft reverts to normal F-15 operation. The pilot has the authority to uncouple at any time.

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## "PSC Implementation and Integration", page 18

## Manual and Automatic Methods for Uncoupling System

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## PSC UNCOUPLE REASONS

- PADDLE SWITCH DISENGAGE

- PILOT INITIATED UNCOUPLE

- POWER SWITCH OFF

- MODE NOT SELECTED

- INCOMPATIBLE MODES

- LANDING GEAR HANDLE DOWN (WITHOUT OVERRIDE)

- IFIM FAILURE

## MANUAL AND AUTOMATIC METHODS FOR UNCOUPLING SYSTEM

There are several manual and automatic methods for uncoupling the system. The manual methods available to the pilot are to depress the paddle switch disengage, depress the couple/uncouple button, turn the power switch off, turn the selected mode off, select an incompatible mode, and set the landing gear handle down. Automatic uncoupling ocurs when there is an IFIM failure.

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## "PSC Implementation and Integration", page 19

## PSC In-Flight Integrity Management (IFIM)

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HELP is Available

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## PSC UNCOUPLE/IFIM REASONS

The uncouple/IFIM reasons listed cause the PSC system to uncouple and illuminate the IFIM light on the upfront panel in the cockpit.

- CC Self Test Fail
- VMSC Self Test Fail
- DEEC Self Test Fail
- EAIC Self Test Fail
- 1553 MUX Check Fail
- H009 MUX Check Fail
- Loss of CC Power
- Loss of PASCOT Power
- Loss of VMSC Power
- INS Validity Failure
- INS Attitude Validity Failure
- Mach Number Validity Failure
- Pressure Ratio Validity Failure
- ADC True Airspeed Validity Failure
- CAS Disengagement (Any Axis)
- VMSC NVM Checksum Failure (Any Channel)
- VMSC OFP Checksum Failure (Any Channel)
- VMSC Channel C Background CPU Failure
- VMSC Input Data Out of Range
- VMSC Arithmetic Error Fault
- PSC Optimization Unbounded

- VMSC Mechanical/Autothrottle PLA Mismatch
- Stall on Selected Engine(s)
- Reversion to BUC on Selected Engine(s)
- Augmentor Failure on Selected Engine(s)
- UART Did Not Receive Valid Data in Time
- EPR Trim Out of Range
- Airflow Trim Out of Range
- CIVV Trim Out of Range
- RCVV Trim Out of Range
- A/B Fuel/Air Trim Out of Range
- N1C2 Trim Out of Range
- AJ Trim Out of Range
- Autothrottle Trim Out of Range
- CC/VMSC Wrap Failure, Declared by CC
- CC/VMSC Wrap Failure, Declared by VMSC
- DEEC/VMSC Wrap Failure, Declared by Selected DEEC(s)
- DEEC/VMSC Wrap Failure, Declared by VMSC
- EAIC/VMSC Wrap Failure, Declared by VMSC
- CC/DEEC Wrap Failure, Declared by CC
- CC/DEEC Wrap Failure, Declared by DEEC(s)

## PSC IN-FLIGHT INTEGRITY MANAGEMENT (IFIM)

The PSC In-Flight Integrity Management (IFIM) logic is designed to automatically uncouple the PSC system and notify the pilot via the IFIM light in the event of certain hardware or software failures. An IFIM failure is declared when a computer fails a self check, the multiplex bus fails a check, a computer loses power, validity bits are not transmitted or received from the INS or ADC, CAS disengages, Checksum fails, PSC logic gives erroneous results, the DEECs receive invalid trim commands, or wrap words fail to increment.

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# Trim Command Limiting

- DEEC Limits Trim Commands to Protect Engine Stability and Dynamic Response
  - Range Checking
  - Rate Limiting
  - Commands Overridden to Maintain Safe Operation
  - Commands Cancelled if a Failure Is Detected

- EAIC Commands Are Limited to Maintain Stable Flow to the Engine
  - MUX Scaling Limits the Magnitude of Trim Commands (±5 deg)
  - Commands Cancelled if a Failure Is Detected

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 21

## Engine Stall Protection

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ENGINE STALL PROTECTION

The PSC software contains stall protection logic which limits the amount of EPR uptrim during aircraft maneuvers to maintain an adequate fan stall margin. The stall protection logic runs in the foreground CPU at 20 Hz.

¥ PSC sends commands to the DEEC which could potentially stall the engine

¥ Engine Stall Protection Logic included in the DEEc to decrease this risk

¥ The DEEC Limits only maintain adequate stall margin for straight and level flight

¥ The PSC Stall Protection Logic operates at 20 Hz and limits the amount of EPR uptrim to maintain adequate stall margin during all aircraft maneuvers

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 22

## VMSC Safety Features

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VMSC SAFETY FEATURES

Re-hosting the PSC control laws in the VMSC required the addition of several safety features to the system. Wrap checks with the CC and both DEECs were added. Since the PSC operates in three CPUs, wrap checks between the foreground and background CPUs were added. In addition, logic was added to perform checksums, timing checks, and power-up tests.

¥ CC to VMSC Channel C Foreground Wrap Failure Check

¥ DEEC to VMSC Channel C Foreground Wrap Failure Checks (Left and Right Engines)

¥ VMSC Channel C Background CPU Failure Checks

¥ OFP Checksum Failure Checks

¥ NVM CHecksum Failure Checks

¥ Watch Dog Timers

¥ Power Up Tests

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# Data Entry Restrictions

- NCI Panel Can Be Used to Input Code Words
  to Reconfigure PSC Control Laws

- The Code Word Is Used by the VMSC Only When
  - "Enter Data" Button on the PSC Control Panel
    Is Depressed and
  - The PSC System Is Uncoupled

*Transients Avoided by Preventing Data Entries While Coupled*

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## PSC Flight Test Envelope
### Revised CAS On, Clean F-15A#8 Flight Test Supersonic Placard

**Revised Aerodynamics, Revised Thrust Transient, "Rigid" Rudder Hinge Moments, Assuming Engine Stall Transient With No Recovery, and No Pilot Reaction**

Caution 0.8 G Lateral ($N_y$) for Unrecovered Engine Stall

Caution 1.0 G Lateral ($N_y$) for Unrecovered Engine Stall

PSC Region II

700 KCAS

675 KCAS

No Pilot Commanded SEC Transfers Baseline Region II

1.28 M

Do Not Fly Baseline Region I

Do Not Fly PSC Region I

800 KCAS Design Limit

Altitude ft — 0, 10,000, 20,000, 30,000, 40,000, 50,000

Mach — 0.8, 1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 2.2, 2.4, 2.6

## PSC FLIGHT TEST ENVELOPE LIMITATIONS

The PSC flight test envelope has been limited based on a simulation study performed on a clean F–15/A with CAS on. The study assumed an engine stall on one engine with no recovery and no pilot action to counter the large yaw moment. Region 1 is a "do not fly" region. Region 2 is a "no commanded SEC tranfer" region. Also shown are 0.8 g and 1.0 g lateral acceleration lines which are pilot discomfort boundaries.

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# NASA Dryden Flight Research Center

## "PSC Implementation and Integration", page 25

## Software Verification and Validation Process and System Integration Test

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## PSC Laboratory System Integration Test Set-Up



SOFTWARE VERIFICATION & VALIDATION PROCESS AND SYSTEM INTEGRATION TEST

The Software Verification and Validation Process consists of laboratory system integration tests, hardware–in–the–loop simulation and aircraft ground tests.

The System Integration Test is performed in the McDonnell Douglas Software Test Facility and Flight Control Laboratory. The purposes of the test are to validate the communication interfaces between the various flight computers, verify the system safety features, and verify proper operation of the PSC control laws.

Actual flight hardware and software are used for the CC, PASCOT, and VMSC in the System Integration Test. Software models of the engines, inlets, and nozzles reside in the Harris host computer. The DEECs and EAICs have been modeled since these units will not be available.

The Harris also contains the simulation software for cockpit displays (e.g., HUD) and an F–15 aircraft with six degree of freedom dynamics.

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# NASA Dryden Flight Research Center

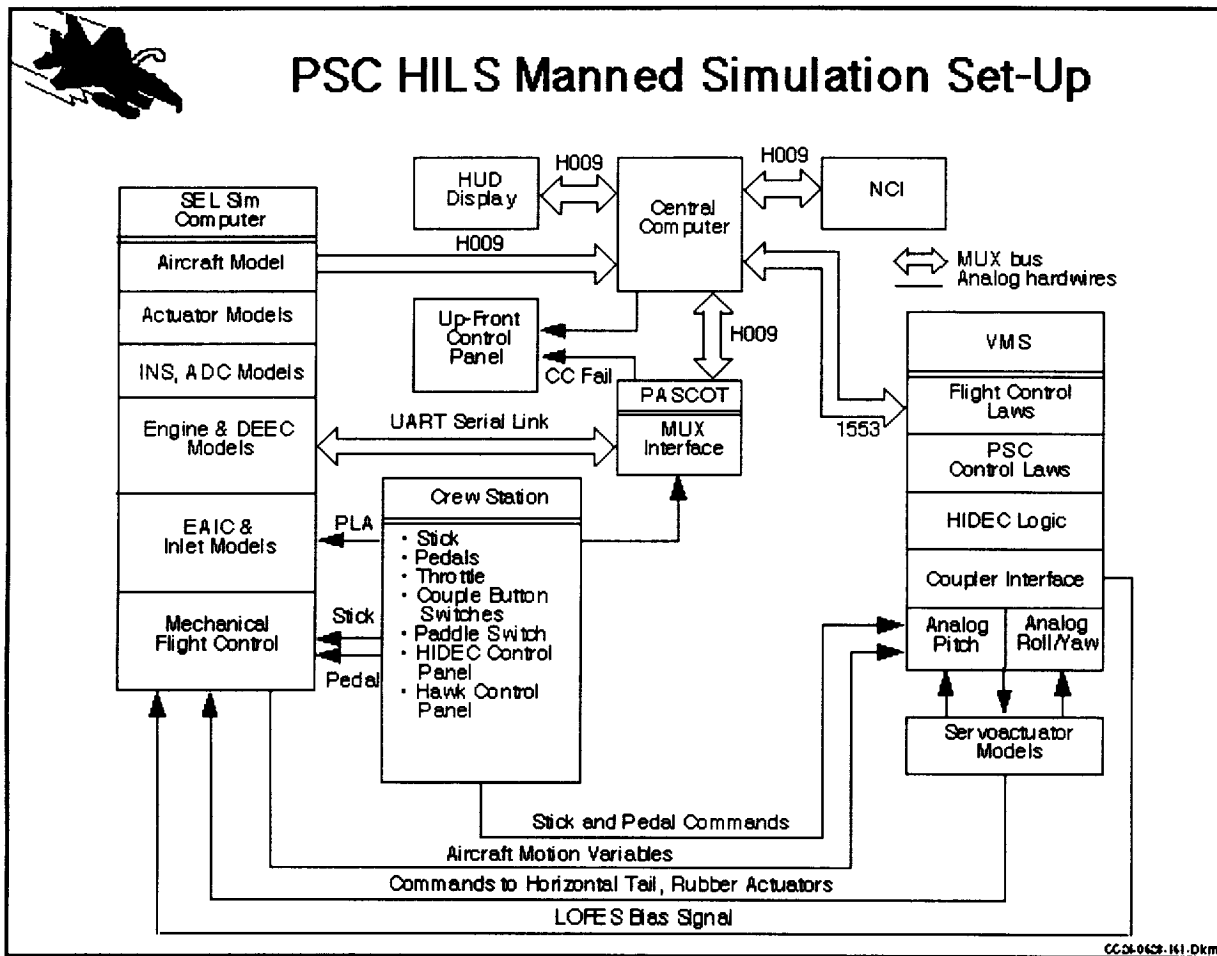## "PSC Implementation and Integration", page 26

## Hardware–In–The–Loop (HILS) Simulation

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## PSC HILS Manned Simulation Set-Up

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HARDWARE–IN–THE–LOOP SIMULATION (HILS)

The Hardware–in–the–Loop Simulation is conducted at the McDonnell Douglas manned simulation facility. The purposes of the test are to verify proper operation of the PSC control laws under realistic variations in altitude, Mach number and power setting throughout the flight envelope, verify that the flight control system has not been adversely affected by the additional PSC logic, verify PSC system safety features, and familiarize the pilot with the PSC control functions.

Actual flight hardware and software are used for the CC, PASCOT, and VMSC in the Hardware–in–the–Loop Simulation. The crew station is a replication of the F–15 cockpit with all the normal switches, gauges and controls. A high fidelity six degree of freedom F–15 aircraft simulation and models of the Air Data Computer, Inertial Navigation System,

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mechanical Flight Control System, and flight control actuators are installed in the SEL host computer. The engine/DEEC and inlet/EAIC models also reside in the SEL computer.

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