TEXAS INSTRUMENTS

Ka-Band MMIC Subarray Technology Program (Ka-Mist) Final Report

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Table of Contents

List of Figures

List of Tables

1. Executive Overview

The broad objective of this program was to demonstrate a proof of concept insertion of Monolithic Microwave Integrated Circuit (MMIC) device technology into an innovative (tile architecture) active phased array antenna application supporting advanced EHF communication systems.

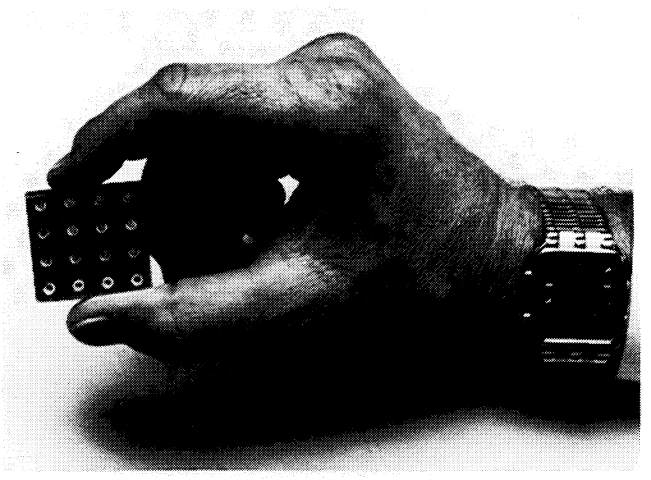


Figure 1-1. Subarray Module

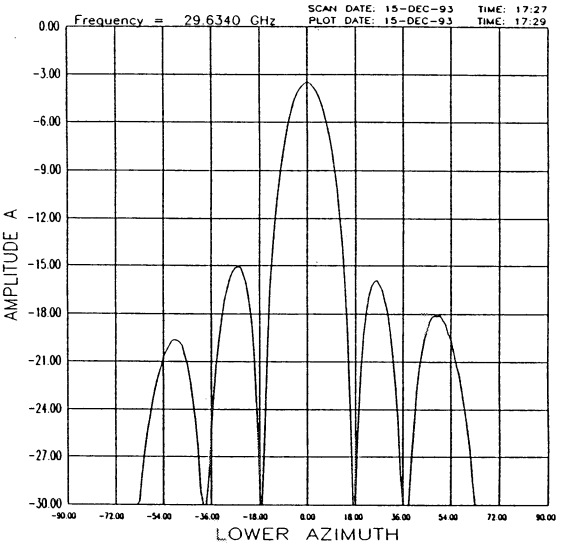


Figure 1-2. Broadside Pattern of Subarray Module

Ka-band MMIC arrays have long been considered as having high potential for increasing the capability of space, aircraft, and land mobile communication systems in terms of scan performance, data rate, link margin, and flexibility while offering a significant reduction in size, weight, and power consumption. Insertion of MMIC technology into antenna systems, particularly at millimeter wave frequencies using low power and low noise amplifiers in close proximity to the radiating elements, offers a significant improvement in the array transmit efficiency, receive system noise figure, and overall array reliability. Application of active array technology also leads to the use of advanced beamforming techniques that can improve beam agility, diversity, and adaptivity to complex signal environments.

Historically, phased array antenna architectures have been defined by the basic building blocks used for the construction of the array. Two prevalent implementations of array architectures include what are typically called the brick and the slat architectures. Both of these architecture types are built with the MMIC and related support circuitry perpendicular to the radiating structure.

The brick architecture typically uses microwave modules each with a single radiating element backed by MMIC based circuitry which are inserted into a large structure to build the array aperture. As each module acts as a transmitter (and/or receiver), each module must be connected

via beamforming networks along with a significant amount of DC/logic circuitry required to supply and control the devices. This approach yields an array architecture that tends to be not only highly labor intensive, but with a physically large aperture thickness and a very complex mechanical structure. The slat approach uses vertical columns or horizontal rows of radiating elements with each element backed by the same requisite MMIC based circuitry. However, due to the collection of multiple radiating elements, transmit/receive functions, and a portion of the beamforming networks on a single subassembly, slat architectures tend to exhibit a lower mechanical complexity with fewer interconnections resulting in lower cost.

A third type of architecture now commonly referred to as the "tile" approach, has received considerable interest in the recent past due to the promise of significantly reduced weight, array profile, and cost. A tile array architecture is one in which the radiating element, MMIC devices, signal distribution, and related control circuitry are placed in layers parallel to the radiating structure. This construction permits a much higher level of subsystem integration such that a multi-element subarray may be built complete with the all of the requisite radiating elements, MMICs. DC/logic distribution, and signal distribution (beamformer) functions integrated into a thin profile, lightweight subassembly (or subarray). Tile subarrays can easily be used as building blocks for large array structures suitable for high performance applications. The compact size promised by tile array architectures can enable application of the technology to low profile, light weight antennae for aircraft and a variety of mobile platforms.

The specific objective of the Ka-Mist program was to demonstrate the technical feasibility of the tile array packaging architecture at EHF frequencies via the insertion of 1990 MMIC technology into a functional tile array or subarray module. The means test of this objective was to demonstrate and deliver to NASA, a minimum of two 4 X 4 (16 radiating element) subarray modules operating in a transmit mode at 29.6 GHz. Available (1990) MMIC technology was chosen to focus the program effort on the novel interconnect schemes and packaging requirements rather than focusing on MMIC development.

A secondary objective developed in the course of the program execution was to integrate two of the subarray modules into a single 4 X 8 (32 radiating element) array for the purpose of voice/data/video communications experiments via the Advanced Communications Technology (ACTS) satellite. This 32 element array was designed to be self contained and operate both in airborne and ground based mobile experiments. Figure 1-1 shows the front view of one of the 4 X 4 subarray modules delivered, while Figure 1-2 shows the measured boresight antenna pattern.

The program was intended to show the viability of designing and producing a limited quantity of a highly integrated (tile architecture) millimeter wave active phased array antennae. It was understood from the initiation of the program that there were significant technical obstacles to overcome to achieve the program objectives. Since the program was to use existing 1990 MMIC designs, the primary risks were tied to the feasibility of integrating the MMICs and the requisite control functions into an acceptable array architecture. To accomplish this task, a number of

significant technical milestones were required focusing primarily on the novel interconnection and packaging challenges. Major highlights of the technical achievements include the following;

- Development and successful demonstration of a true tile architecture for an active phased array where the radiating elements, active beamforming network, RF power amplification, and DC bias/logic distribution functions are provided as an integrated layered system as opposed to traditional brick or slat architecture
- Achievement of a low insertion loss MMIC phase shifter through the use of PIN diode switches
- Development of an Application Specific Integrated Circuit (ASIC) for logic control to reduce the number of digital input/output ports required
- Development of a complex (9 layer) multi-layer thin film network board for DC bias and logic distribution
- Development of a cavity backed aperture coupled patch radiating element
- Development of a orthogonal coax to microstrip feed
- Development of techniques for alignment of MMIC carrier plates with the radiating apertures
- Integration of individual RF channel on/off control within the subarray module
- Integration of reparability features into the subarray module
- Development of RF characterization and testability at a carrier plate subassembly level
- Demonstration of 77 watts EIRP for a single subarray module
- Development of a 29.6 GHz single input, dual output driver amplifier assembly with 27 dB gain and 22 dBm output power for each output
- Integration of two subarray modules into a self contained flight worthy assembly with integrated power supplies, fail-safe circuitry, and a demonstrated EIRP of over 300 Watts.

The successful integration of two of the subarray modules into a single antenna array is considered the most significant accomplishment from the MMIC array viability point of view. This 32 element array demonstrates a transmit EIRP of over 300 watts yielding an effective directive power gain in excess of 55 dB. (i.e., the 32 element array package requires less than -3 dBm CW power input to achieve the EIRP of 300 Watts (54.7 dBm) at 29.63 GHz. The main significance of this array is that it has been actively used as the transmit link in airborne/terrestrial mobile communication experiments accomplished via the ACTS satellite launched in August 1993. This use represents a viable demonstration of the tile technology insertion into a test vehicle usable outside of the laboratory. Success of the communication experiments has provided a strong measure of credibility regarding the potential of insertion of millimeter wave MMIC technology into compact, high reliability antenna systems for mobile satellite communication applications.

2. Subarray Module Requirements

The major objective of the Ka-Mist program was to advance array packaging technology that resulted in the demonstration of a light weight, low cost, compact, EHF phased array antenna. This led to the development of specific performance goals for the demonstration of the technology which are shown in Table 2-1.

Table 2-1. Specific Requirements for the 4 X 4 Subarray Module

Parameter	Value
Center Frequency	29.63 GHz
Array Type	Transmit
Array Geometry	4 X 4 rectangular grid
Number of elements	16
Number of Beams	1
Radiating element	Aperture coupled patch element
Element gain	5 dB
Subarray bandwidth	5%
Scan requirements	± 30 °
Grating lobes	None in visible space for broadside beam
RF drive power	125 mW
RF transmit power	1.5 W
EIRP	75 W
Polarization	Vertical
Pointing accuracy	1/4 of a beamwidth
RF amplifier type	GaAs MMIC
RF phase shifter type	GaAs MMIC
DC power supply	Regulated, V_{cc},V_{drain},V_{gate},$V_{phase(+)}$,$V_{phase\ (-)}$
Thermal management	Circulated chilled water, cold plate
Power up sequence	Manual (adjust individual voltages)
External controller	486 PC with serial data output
Operating environment	Laboratory

The subarray module requirements shown in Table 2-1 were determined to a large extent by the essential need to use existing MMIC designs to allow the program to focus on the packaging technology rather than MMIC development. The existing MMIC device performance levels and mechanical dimensions heavily influenced the development of the subarray level requirements shown in Table 2-1.

Development of the requirements generated a number of key subarray module attributes that influenced the final configuration including;

- ***Wider than optimum interelement spacing*** due to the physical size of the MMIC die. The die size drove the subarray layout in that it was considered critical to make certain that the

DC/logic distribution layer would not cover the radiating structure or the MMICs. This alleviated the concern than back radiation from the MMIC to element coupling would cause interference within the subarray module.

- ***Integration of the DC/logic functions*** within the subarray module to simplify the external interface requirements. The need to integrate this level of functionality led to the development of a custom ASIC and a highly sophisticated multi-layer DC/logic distribution thin film network to allow the input/output terminals to be reduced to a single serial data input for each half of the subarray and terminals for the various supply voltages. The end result was a subarray package with only sixteen DC/logic terminal pins.
- ***Testability of individual carrier plates*** external to the subarray module to ensure functionality and optimum power matching prior to module assembly. This attribute led to the use of conventional MMIC and wire interconnect technology for both the carrier plates and the final subarray module assembly.
- ***Good thermal control of the subarray module*** to ensure reliable operation of the MMICS. This was of particular concern as the major heat producers (power amplifiers) were placed adjacent to the radiating structure which was physically removed from the available cooling surfaces.

These and other related issues were addressed in the design/validation phase of the program.

3. Subarray Module System Description

The subarray module block diagram is shown in Figure 3-1. Key subsystems of the module include the radiating aperture, RF distribution network, DC power/logic distribution, and thermal management. RF power is supplied via a single K-series coaxial connector and is transmitted through an uniform microstrip sixteen way power division using one two way power divider (which is an integral part of the orthogonal feed) and two eight way power divider networks. Each of the sixteen RF lines feeds a single 4 bit MMIC P-I-N diode switched line length phase shifter and a single three stage P-HEMT power amplifier. The output of the power amplifier is coupled via a slot feed to the radiating elements which are cavity backed patch elements.

KEY SUBSYSTEMS
- RF
- CONTROL
- THERMAL

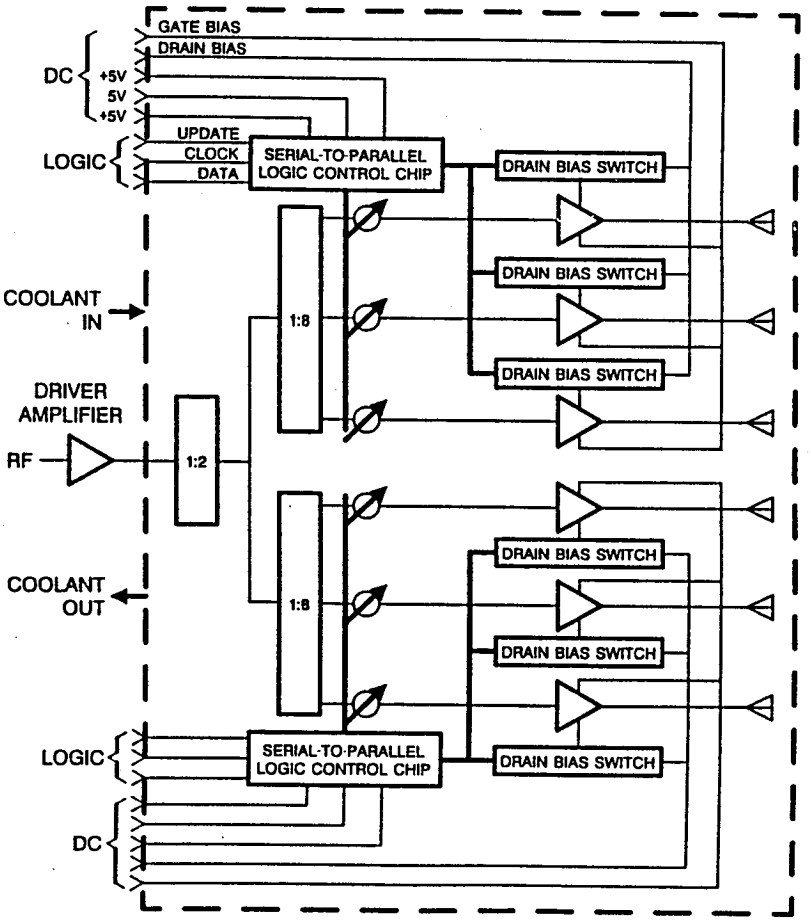


Figure 3-1. Subarray Module Block Diagram

Logic commands for selection of individual phase bits and enable/disable of the individual power amplifiers are routed through a serial data bus to an ASIC which converts the serial data to parallel data prior to transmission to the individual control elements via a multi-layer thin film network PWB. The data bus provides individual control over each phase shift bit by element in addition to the capability to enable or disable each of the sixteen amplifiers through control of the DC drain bias voltage. DC power (five discrete voltages) is supplied via individual through wall

contact pins and is routed via the same multilayer TFN to provide amplifier gate bias, amplifier drain bias, ASIC power, and phase shift bit control.

Control of the subarray module is provided by a 486 class PC acting as a beam steering controller. The 486 PC uses a specially designed interface card controlled by an array control program written in Basic. For a desired beam pointing angle (azimuth/phi) the control software uses a calibration lookup table created during range testing of the subarray to calculate the optimum phase shifter bit settings. Once the bit settings are determined, the interface board clocks in the serial data using one cycle for each subarray half (i.e. it requires two clock cycle to update all 16 phase shifters. The array controller PC provides a visual display that mimics the location of each phase shifter/amplifier pair with a indicator showing the phase bit selected and the enable/disable status of each amplifier. The control software is designed to allow manual control of each phase shifter/amplifier pair as well as full beam steering control. This feature of the array controller is particularly useful in the generation of array calibration files as it allows each element to be activated and controlled individually.

Thermal management for the subarray module is provided by a cold plate chilled by circulated water mounted to the side opposite the radiating elements.

The power dissipation of the subarray module is approximately 10 Watts which for bench/antenna range testing was easily handled by maintaining the water flow through the chiller at approximately 18°C.

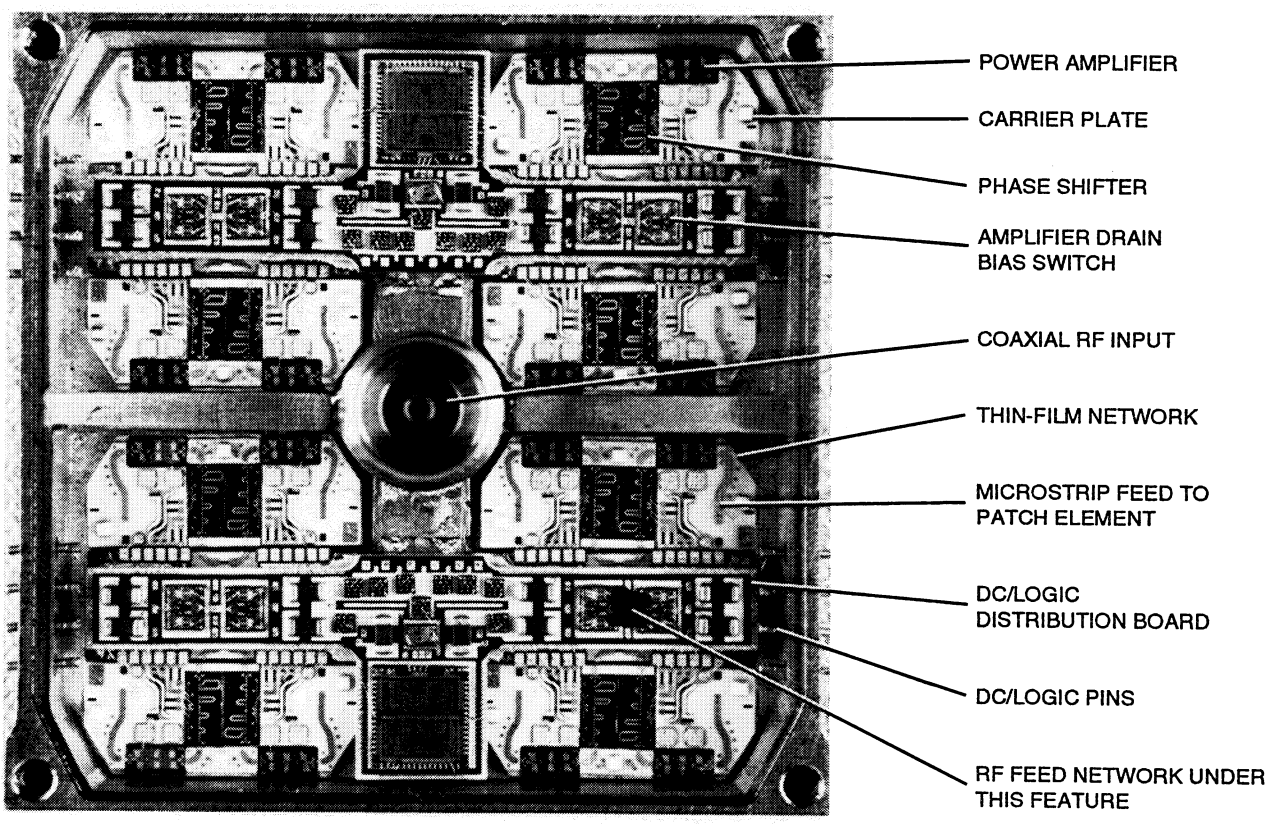


Figure 3-2. Subarray Module Layout

Figure 3-2 shows the actual layout (photograph) of the subarray. The physical architecture of the subarray module is arranged such that each half of the subarray is identical and contains; eight radiating elements, four carrier plates, one ASIC, one thin film network DC/logic distribution board subassembly, and one eight way power divider. Each pair of radiating elements is fed by a single carrier plate which carries two amplifiers, two phase shifters, and thin film networks for feeding the amplifier/phase shifter circuit (RF and DC/control) as well as providing the slot for coupling the output of the amplifier to the patch radiator. The output of the amplifier is fed to a microstrip TFN which couples the RF to the patch antenna through a slot etched on the ground plane side of the microstrip line. A cylindrical hole in the carrier plate is part of the cavity which backs the patch radiator while gold plated quartz used for the actual radiating element. The phase shifters are 4-bit switched line length with an average insertion loss of 4.5 dB while the amplifiers are three stage P-HEMT devices with approximately 20 dB of gain and an output power of approximately 100 mW. The DC/logic distribution board subassembly includes an ASIC, drain bias switches, gate bias voltage regulators, and filtering components. This board provides regulated power to the amplifier gate and drain lines, and provides serial to parallel data conversion (via the ASIC) for individual control of the amplifier and phase shifters. The RF feed network which lies underneath the DC/logic distribution board, provides a uniform power distribution from the orthogonal launch and has an insertion loss of approximately 5 dB. To overcome the power distribution losses to supply proper drive to the MMIC power amplifiers requires an input power at the K connector of approximately 125 mW.

Figure 3-3 shows the front side of the aperture which consists of 16 radiating elements arranged in a 4 x 4 planar configuration. The radiating elements are arranged in a square grid, with an inter-element spacing of 0.33" ($\approx .8\ \lambda$). Any further reduction in the inter-element spacing was constrained by the existing MMIC chip sizes and hybrid packaging scheme used for the module construction. The actual subarray module aperture size is 1.33" x 1.33".

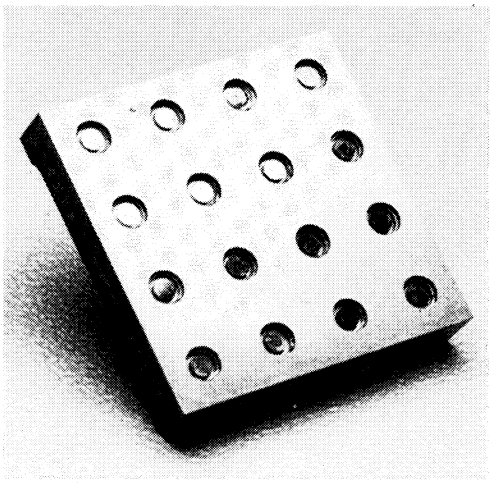


Figure 3-3. Subarray Module Aperture

4. Subarray Module Components

Critical components of the subarray module include the radiating element, RF manifold, MMIC phase shifters, MMIC power amplifiers, carrier plate subassemblies, and the DC/logic distribution board subassembly. A brief discussion of each of the components follows.

4.1 Radiating Element

The radiating element used for the subarray module is an electromagnetically coupled patch antenna. This antenna provides a wireless connection from the power amplifier to the radiating element. The patch elements are embedded in dielectrically loaded and hermetically sealed cavities formed in the base of the module housing. A comparison between desired and achieved performance of the radiating element in an isolated environment is given in Table 4-1.

Table 4-1. Radiating Element Isolated Performance

Parameter	Performance Goal	Measured Value
Center Frequency	29.6 GHz	29.6 GHz
Bandwidth	5 %	8%
3 dB beamwidth	< 30 degrees	< 30 degrees
Front-to Back ratio	15 dB	13 dB
Element gain	4 dB	6 dB
Cross polarization	< -15 dB	< -20 dB

The patch element was chosen over dipole and waveguide elements since these elements lend themselves to low profile construction and can be easily integrated with the MMICs. Given the patch element as the preferred candidate, the primary design trade offs existed in the construction techniques and the method of coupling the power amplifier to the patch.

Patch elements are commonly constructed on a continuous dielectric substrate using a simple photolithographic etching process. Unfortunately, the dielectric substrates commonly available are poor conductors of the heat generated by the power amplifiers particularly when the amplifiers are mounted on the ground plane side of the patch elements. Use of a continuous dielectric substrate also leads to generation of undesirable surface waves for thick substrates. To eliminate these problems, a dielectrically loaded cavity structure was selected for the radiating element. The radiating element consists of z-axis quartz dielectric with a circular patch printed on the top of the dielectric substrate. The sides of the quartz are also gold plated to allow hermetic sealing of the elements to the housing. RF is coupled from the microstrip feed via a .004 thick slot in the backside of the carrier plate feed TFN. With this configuration, the resonant frequency is essentially determined by the size of the patch and the substrate dielectric constant. Figure 4-1 shows the construction of the radiating element.

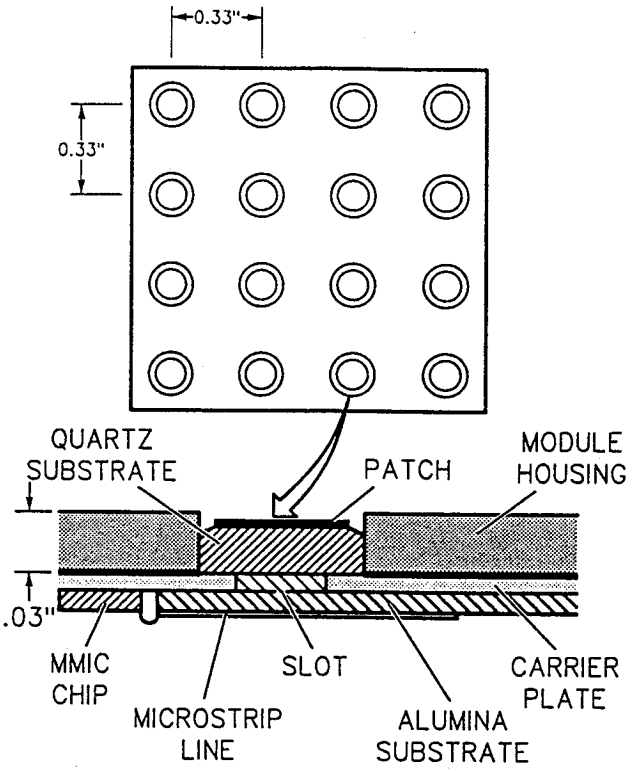


Figure 4-1. Radiating Element Construction

The specific radiating element design was arrived at through empirical and analysis tasks. The starting point of the element design was based on the computer analysis tools available for patch elements on continuous dielectric substrates. This analysis provided the patch size for given dielectric substrate thickness and its dielectric constant. The cavity diameter was selected through experimental iteration. The cavity diameter was selected such that the effect on the resonant frequency with and without cavity was minimum. Figure 4-2 shows the measured VSWR of an isolated radiating element. The result shows better than 8 percent bandwidth for 2:1 VSWR.

Figure 4-3 shows the measured gain over the operating frequency band. As seen from the figure, a 6 dB gain was achieved with an isolated element.

Figure 4-4 shows the isolated element E-and H-plane patterns. As seen from these figures, the front-to-back lobe ratio is about 13 dB. The minimization of the back radiation effects on subarray stability led to important design considerations in the module packaging and shielding.

The effect of mutual coupling on the element scan performance was an important area of concern particularly due to the fact that the inter-element spacing was about 0.8 wavelength. To address this concern, a passive 4 x 4 element array was fabricated and measured to determine the mutual coupling between elements. From the mutual coupling data, the reflection coefficient was computed as a function of a scan angle and plotted against infinite and finite array cases where the patch elements are mounted on a continuous dielectric sheet of uniform thickness and dielectric constant. For the case of a finite 4 x 4 array with cavity backed elements, the results show a well behaved VSWR performance over scan volume. The three cases are plotted in Figure 4-5

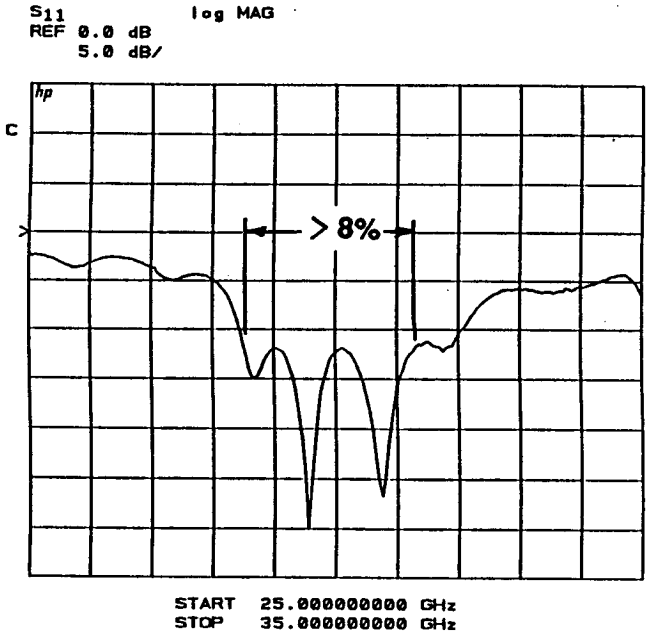


Figure 4-2. VSWR of Isolated Radiating Element

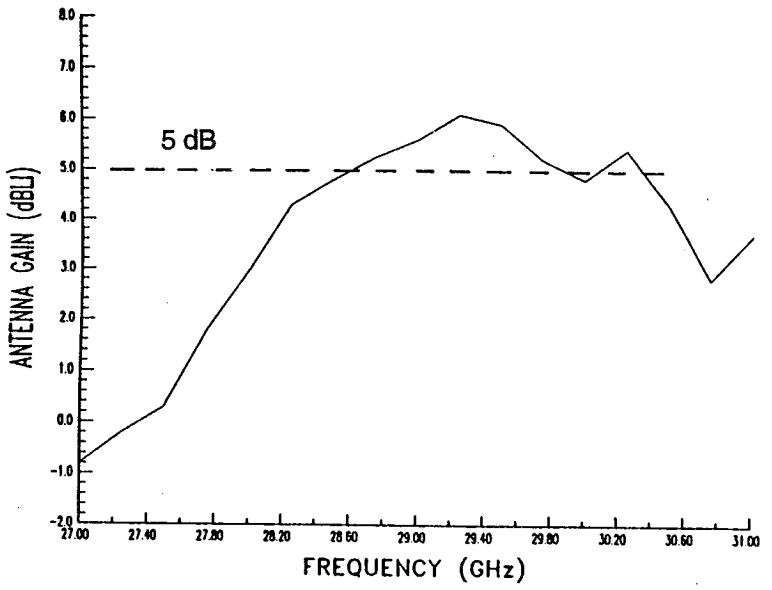


Figure 4-3. Gain of Isolated Radiating Element

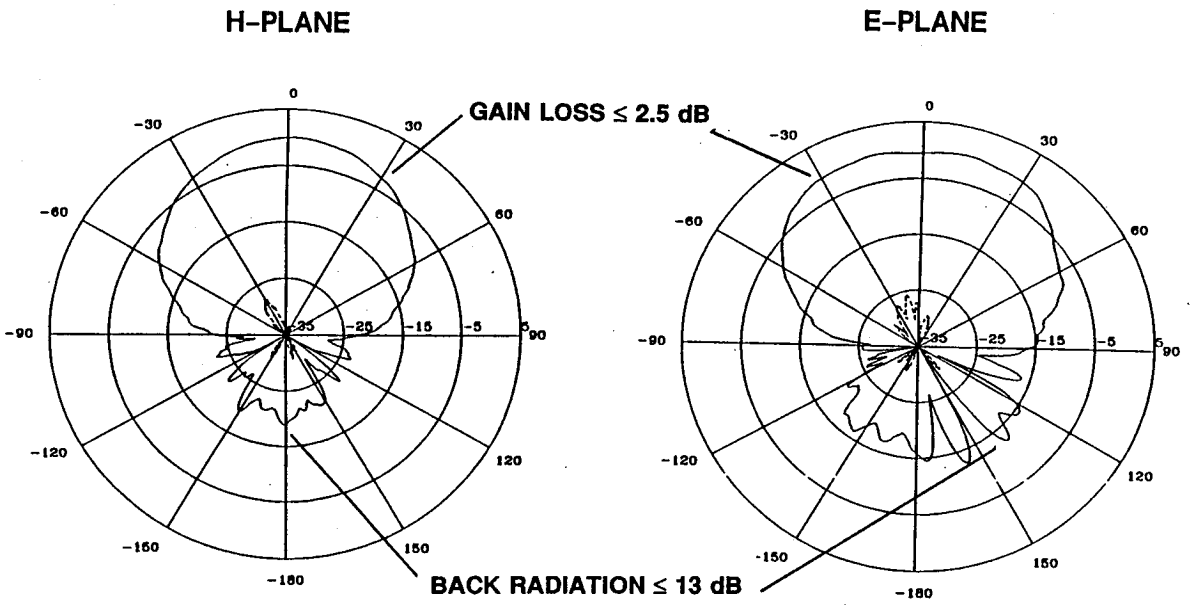


Figure 4-4. Isolated Radiation Patterns

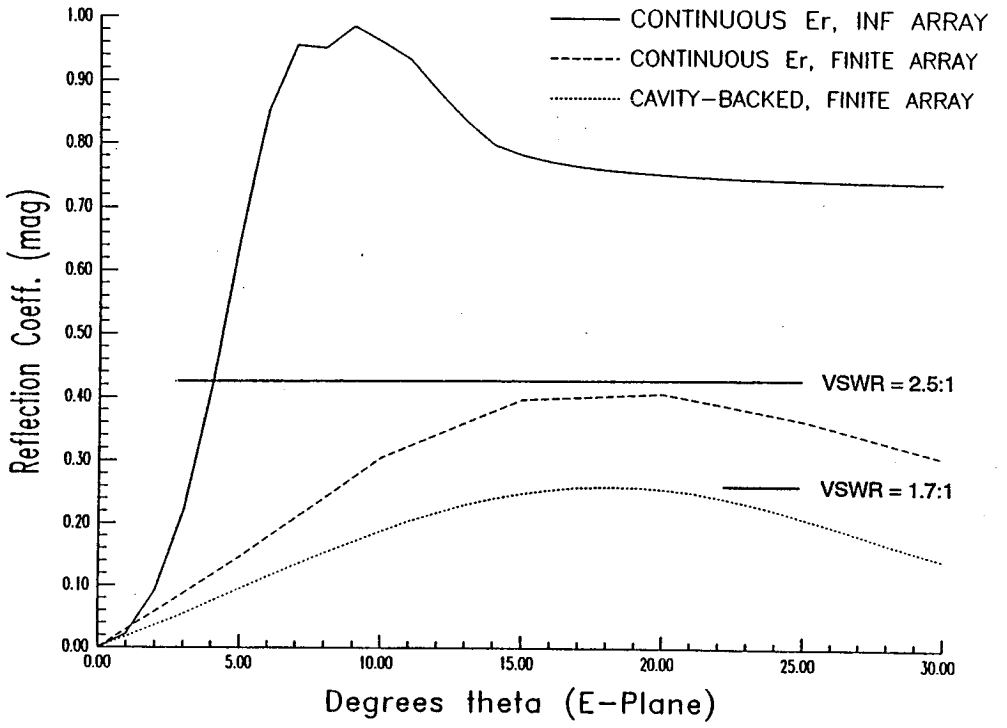


Figure 4-5. Element Mismatch Versus Scan Angle

Table 4-2 shows the mechanical dimensions for the final element configuration.

Table 4-2. Radiating Element Mechanical Dimensions

Parameter	Value
Antenna Element Dielectric Constant	4.6
Patch Diameter	0.089 Inches
Cavity Diameter	0.120 Inches
Cavity Depth	0.030 Inches
Feed Substrate Thickness	0.010 Inches
Feed Substrate Dielectric Constant	9.8
Slot Length	0.071 Inches
Slot Width	0.004 Inches
Feed Line width	0.010 Inches
Stub Length	0.020 Inches

4.2 RF Manifold

The primary requirement for the RF manifold is to provide a uniform sixteen (16) way power split for efficient distribution of the subarray module RF drive power. The centerpiece of the manifold is an orthogonal coax to stripline launch which provides an equal power split between the subarray module halves followed by a transition to microstrip. The orthogonal launch consists of a K connector attached to a multilayer duriod laminate which includes a mode suppresser, matching tees, and a quarter wave transition from stripline to microstrip. Figure 4-6 shows a cross sectional view of the launch while Figure 4-7 shows details of the mode suppresser, matching stubs and stripline to microstrip transition.

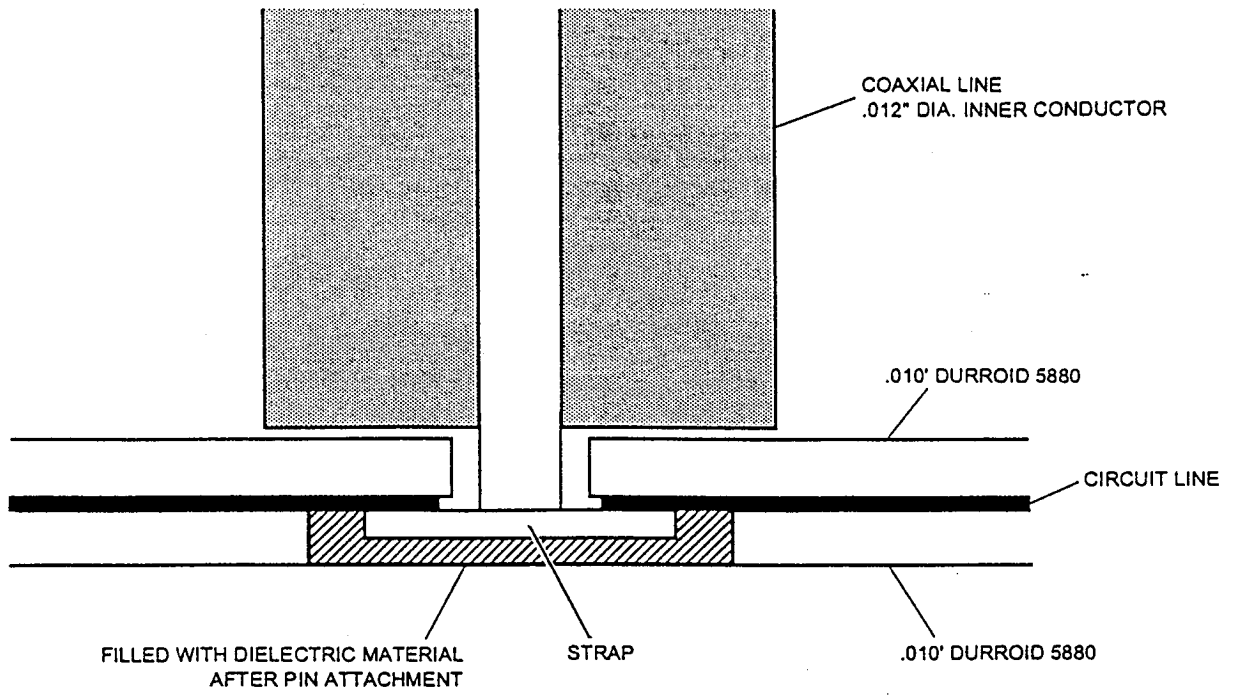


Figure 4-6. Cross Section View of the Orthogonal Launch

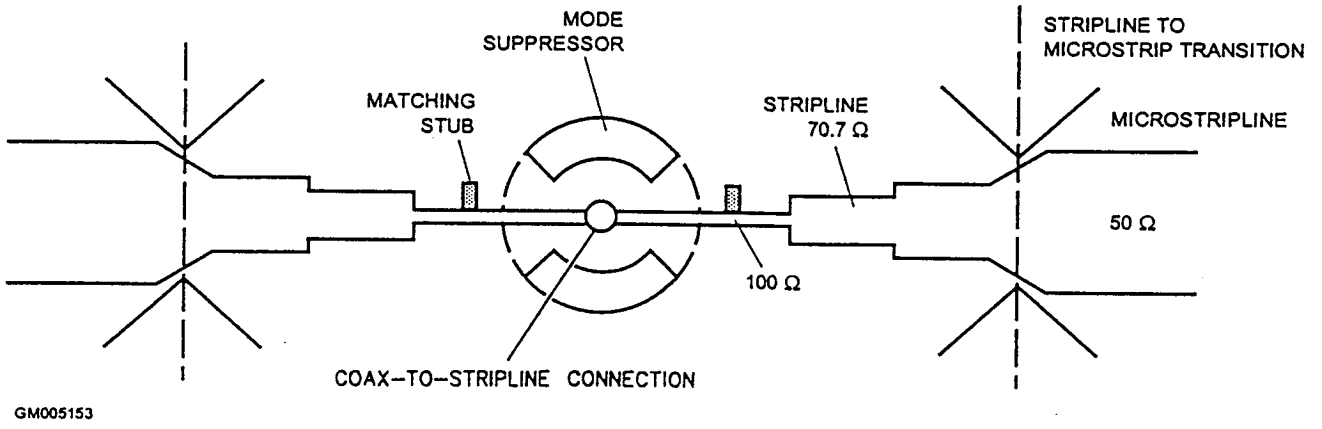


Figure 4-7. Transmission Line Circuit for Coax to Stripline to Microstrip

The manifolding is symmetrical for each half of the subarray module and consists of a single two way power divider and a pair of four way power divider microstrip thin film networks fabricated on .010 alumina substrate. Reactive tees are used on the four way dividers to prevent interline coupling and to provide improved input match and amplitude tracking. Return loss of the RF manifold is better than 20 dB with an insertion loss of approximately 5 dB at 30 GHz. Figure 4-8 shows a view of the subarray module with the DC/logic distribution boards removed to uncover the RF distribution manifold.

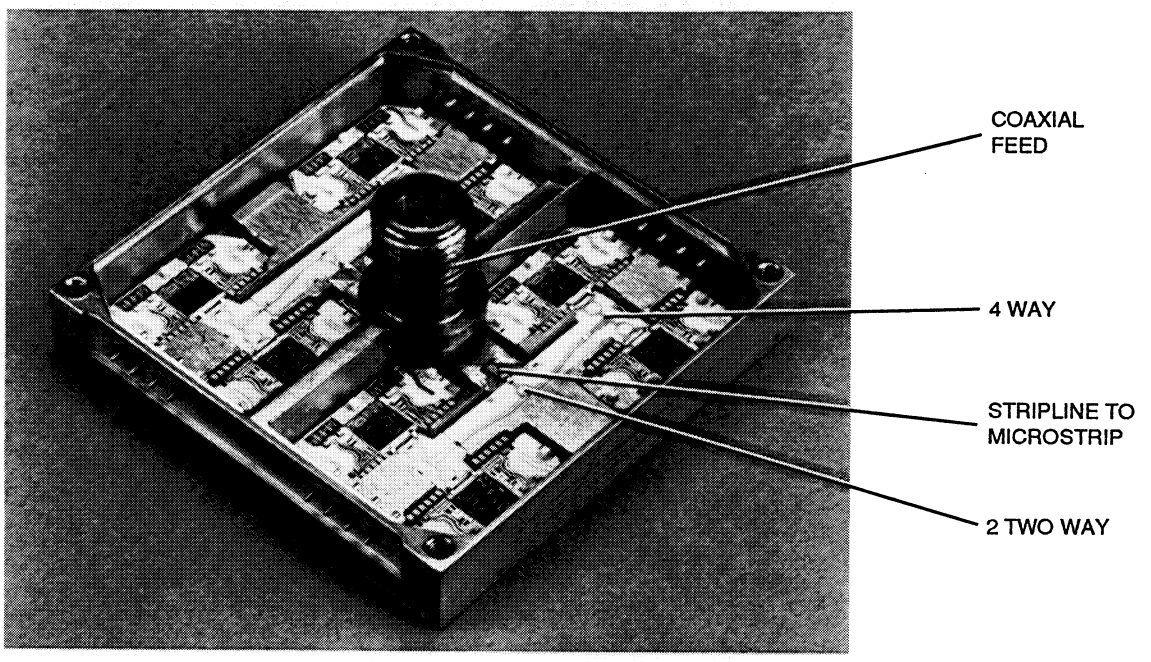


Figure 4-8. Subarray Module RF Manifold

4.3 MMIC Phase Shifter

The MMIC phase shifter used in the subarray module (shown in Figure 4-9) is a four bit switched line length design that utilizes P-I-N diodes as switch elements. It was designed and fabricated by Texas Instruments Central Research Laboratories (CRL) and is based on a broadband (20 to 40 GHz) design originally developed for the Army LABCOM. The design iteration for this program optimized performance over a narrower frequency range, restructured the P-I-N diode orientation to simplify logic control and added coplanar probe pads to facilitate on wafer characterization. The MMIC measures 0.122 x 0.058 x .004 inches, requires one bias input per bit, and includes a DC block. The MMIC exhibits extremely low insertion loss for a MMIC operating at this frequency.

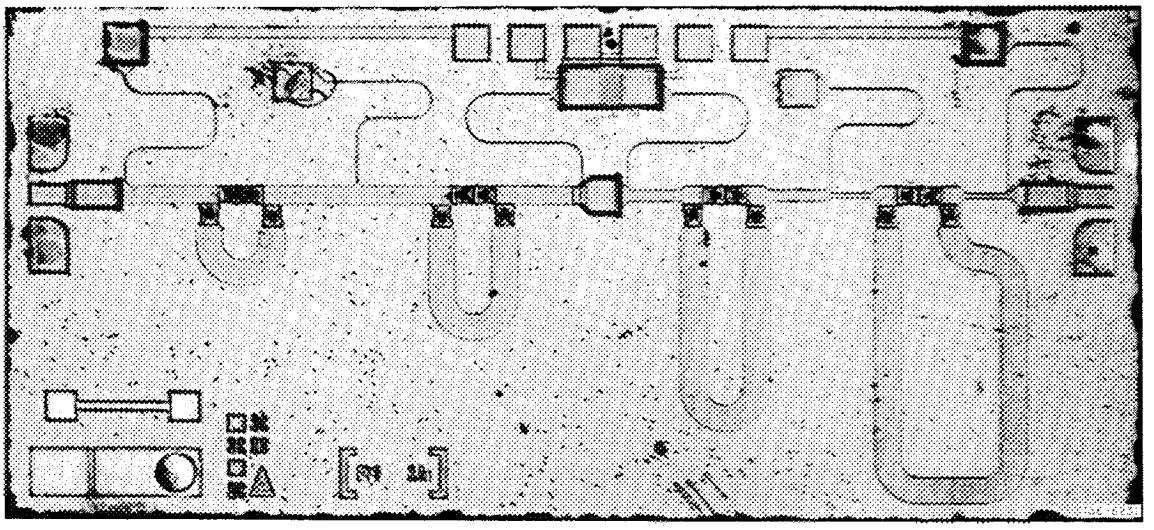


Figure 4-9. Phase shifter MMIC

Phase states on the MMIC are selected by applying a positive or negative bias voltage to the input pad of each phase bit. This forward biases the diodes in the reference or delay path and reverse biases the diodes in the opposite path. This configuration was defined in concurrence with the output state of the controller ASIC (which switches between these voltages and sources/sinks the diode bias currents) to allow the ASIC to directly control the phase shifter diodes without any additional drive circuitry. Phase shifter performance requirements and measured data are shown in Table 4-3.

Table 4-3. MMIC Phase Shifter Performance

Parameter	Specified	Measured
Phase Accuracy	± 10 % of bit size	± 12 % of bit size
Insertion Loss	< 8 dB	< 6 dB
Loss Variation Vs state	< ± 1 dB	< ± 1 dB
Part to Part Loss variation	< ± 1 dB	< ± 1.5 dB
Input VSWR	< 2:1	< 2:1
Output VSWR	< 2:1	< 2:1
Bias Current	< 10 mA per bit	< 10 mA per bit

Figure 4-10 shows sample RF probe data for 6 phase shifters at a single reference state only, Figure 4-11 shows RF probe data for a single phase shifter at different phase states, and Figure 4-12 shows phase accuracy of a single phase shifter at different phase states. Examination of the MMIC phase shifter data shows the achievement of very good performance for an EHF device.

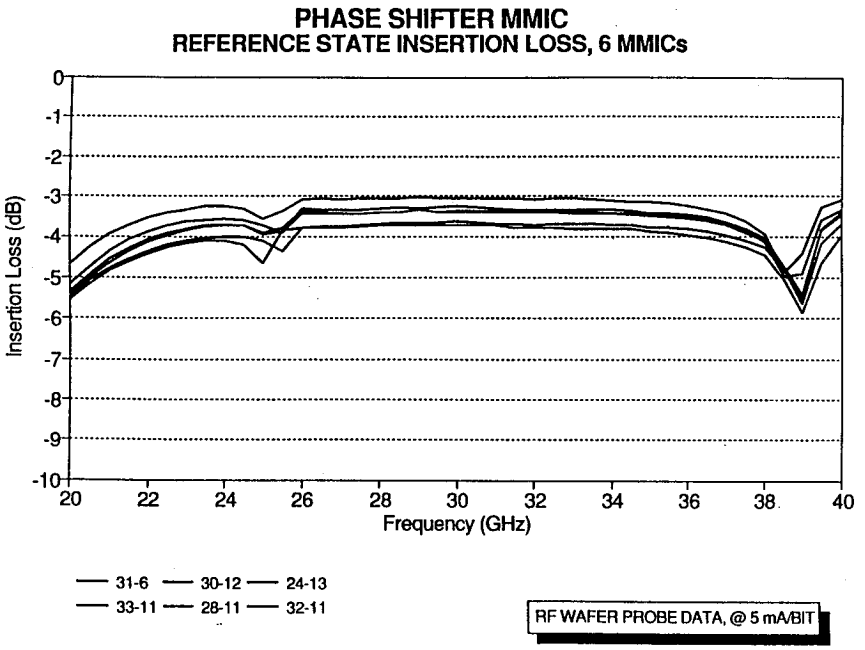


Figure 4-10. Phase Shifter MMIC to MMIC Loss Variation

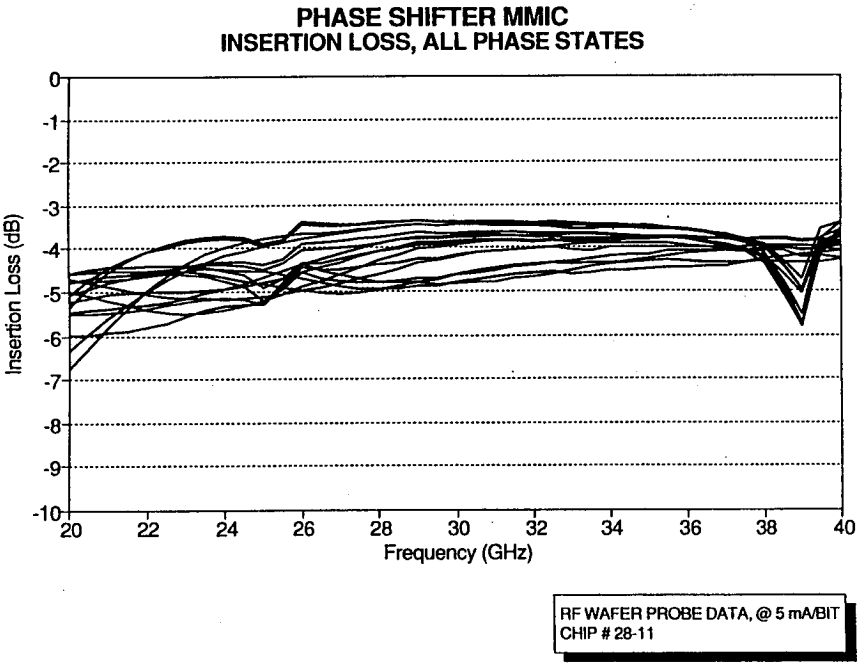


Figure 4-11. Phase Shifter MMIC Loss Variation with Phase State

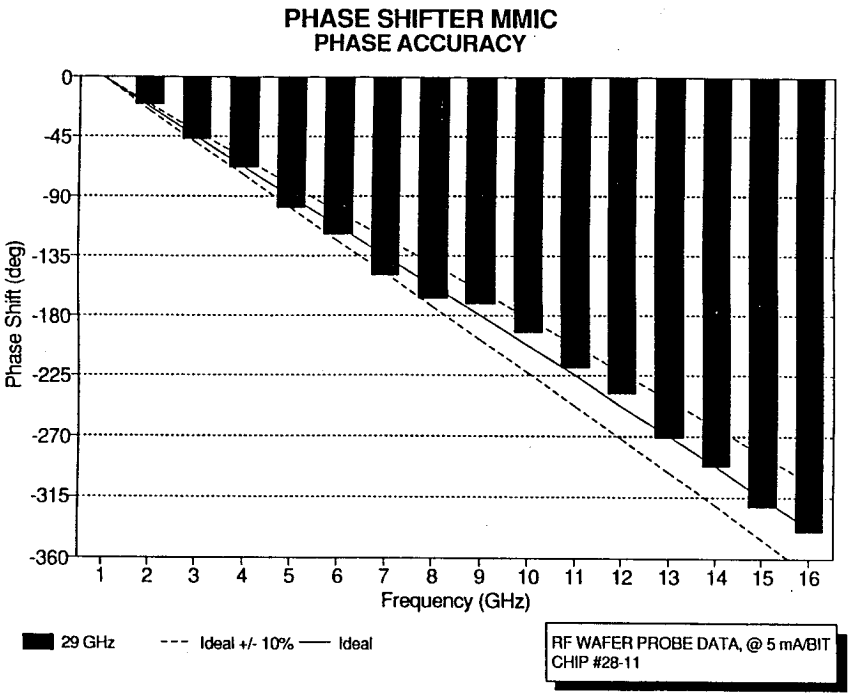


Figure 4-12. Phase Shifter MMIC Phase Shift Accuracy

4.4 MMIC Power Amplifier

The MMIC power amplifier used in the subarray module is a three stage design utilizing P-HEMT devices. It is based on a MMIC developed on a previous NASA program and was designed and fabricated by CRL. For this application, the interstage matching networks were modified to center the operating band to approximately 30 GHz with the addition of coplanar probe pads to facilitate on wafer probing and screening. The MMIC die size measures 0.094 x 0.041 x 0.004 inches. Bias requirements consist of a positive drain voltage (typically 4.5 V), and a negative gate voltage (typically -0.3 V). Drain current is typically 80 to 100 mA when biased for maximum power output. Power added efficiency for the amplifiers is approximately 22 percent. Table 4-4 shows typical performance for a single MMIC power amplifier. Figure 4-13 shows the amplifier used in the delivered subarrays while Figure 4-14 shows a representative power output curve for the amplifier.

Table 4-4. MMIC Power Amplifier Performance

Parameter	Specified	Measured
Output power	> 100 mW	> 100 mW
-1 dB bandwidth	± 700 MHz	± 800 MHz
Associated gain	>15 dB	>20 dB
Efficiency	> 20 %	> 22 %
Input VSWR	< 2:1	< 2:1
Output VSWR	< 2:1	< 2:1

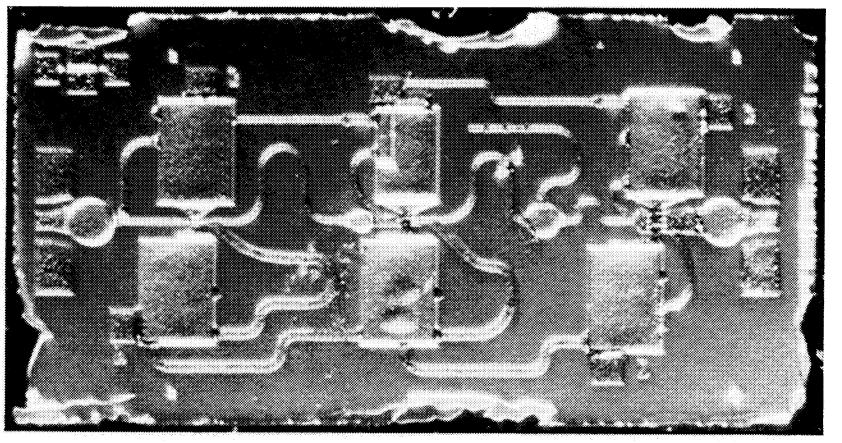


Figure 4-13. 3 stage P-HEMT MMIC Power Amplifier

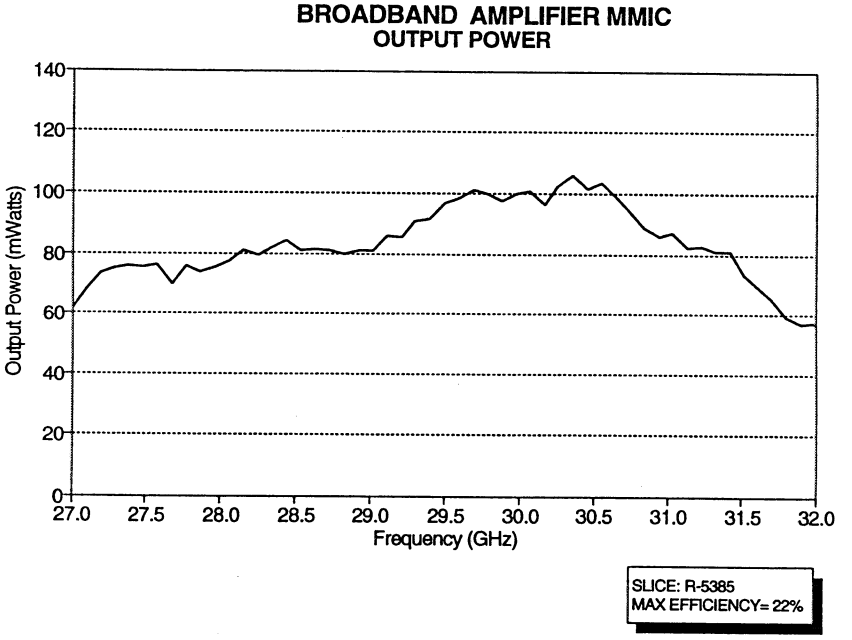


Figure 4-14. MMIC Power Amplifier Power Output

4.4.1 Power Amplifier Reliability

For MMIC arrays to yield the maximum potential in terms of graceful degradation, the reliability of the components is of critical importance. Considering that the power amplifier is typically the component with the highest stress due to power dissipation and thermal stress, reliability of the power amplifier is considered the key to the long term reliability of MMIC phased arrays.

As indicated previously, the power amplifiers developed for this program were a variation of an existing design based on an available (1990) process technology. Due to the limited number of devices required to populate the needed subarrays, only a single set of wafers were originally processed for the program. As they were processed in a single lot, all of the devices bore the same performance characteristics. Considerable testing of individual amplifiers was accomplished both in standard test blocks and in carrier plate test formats that yielded a good indication of the performance parameters of the original amplifier lot.

During antenna range testing of the first subarray module assembled, unanticipated failures of several power amplifiers occurred. Failure analysis via visual inspection (scanning electron microscope) showed several cases of failure of the third FET (output stage) indicative of overcurrent stress on the device. Continuing failure analysis and testing of individual amplifiers outside the subarray environment led to the conclusion that the amplifiers were marginally stable and exhibited a tendency towards natural oscillation in the 30 to 500 MHz range under various bias conditions. In addition to the natural instability, the original process lot of amplifiers exhibited a drain breakdown voltage of approximately 7-9 VDC. The failure analysis led to the conclusion that the failures in the subarray environment were the result of the instability of the individual devices, limited isolation of the drain voltage bus in the subarray, and the low breakdown voltage of the devices.

Due to low process yield of the original lot of amplifiers, a second lot was processed and became available during the failure analysis. The second lot showed the same instability tendency but exhibited considerably improved breakdown resistance (12-15 volts). In the array environment, the instability problem and the drain bias isolation was resolved by the addition of a 5 ohm decoupling resistor and a 470 μF capacitor on the drain and gate bias lines for each amplifier (placement of the decoupling resistor can be seen in Figure 4-15). Use of the new process lot amplifiers and the additional filtering circuits successfully resolved the instability and failure problem. It is important to note that as of the writing of this report, the 32 element array built using two subarrays has accumulated an estimated 400-500 operational hours in fairly harsh environments including airborne and ground mobile Satellite On The Move experiments without a known amplifier failure.

4.5 Carrier Plate

As originally proposed, the selected approach for mounting/carriage of the amplifier and phase shifter MMIC's was the use of a carrier plate. Each carrier plate provides two transmit channels and includes: two four bit phase shifter MMICs, two power amplifier MMICs, two microstrip feed lines for coupling to the antenna elements, RF interconnect lines, and the appropriate DC bias/filtering provisions. As envisioned, this approach allowed the RF testing and characterization of the RF performance prior to installation into the subarray module. In a number of cases, this test capability allowed identification and resolution of defects prior to installation and, provided a means of selecting carrier plates with closely matched power output profiles. Figure 4-15 shows the front and back sides of a single carrier plate.

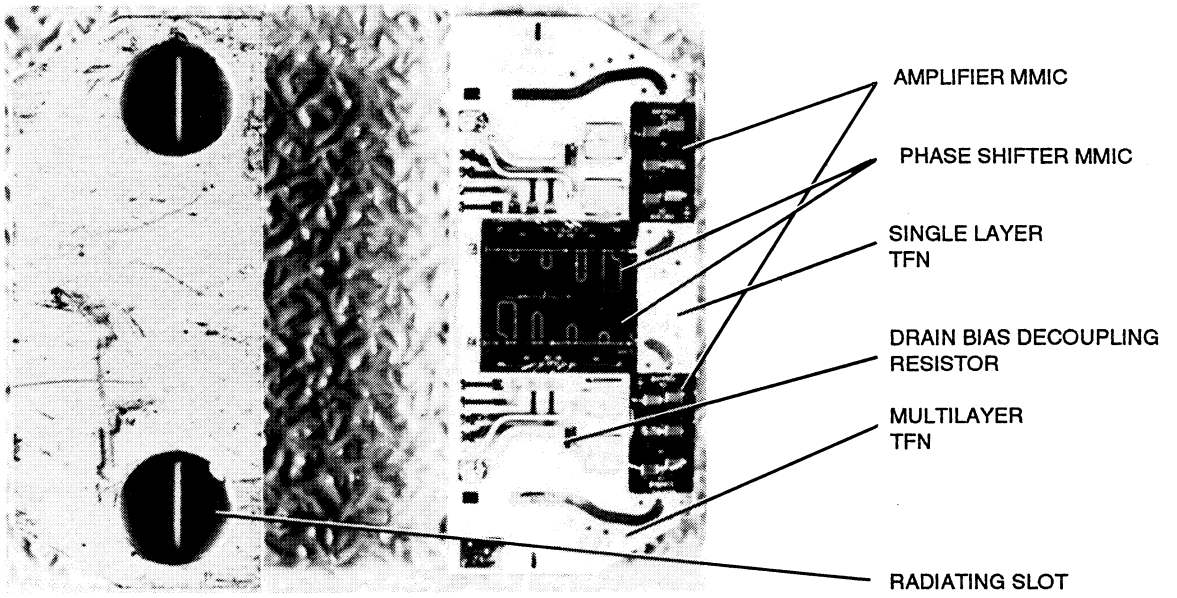


Figure 4-15. Carrier Plate

For the base carrier plate, THERMKON 65M, which is a copper molybdenum alloy, was chosen as the preferred material due to good thermal conductivity and a coefficient of thermal expansion (CTE) value in line with that of the GaAs MMICs and the Alumina used for the thin film networks. The base itself was machined using conventional techniques and tolerances and gold plated to improve adhesion of the bonding epoxies used and to provide a satisfactory RF ground.

Distribution of the RF, DC bias and provision for proper RF and DC isolation required the use of four thin film networks (TFN) fabricated on .010 thick alumina substrate. Of the four, two were single layer TFN's that provided a matched RF input line from the (subarray) RF distribution network and the RF interface from the phase shifter MMIC and the Amplifier MMIC. The remaining two TFN's were multi-layer (6 layers) TFN's that contained on the various layers the radiating slot, a microstrip feed line for the slot, DC bias lines with bias resistors for phase shifter control, DC bias lines for the amplifier MMIC's, and mounting pads for gate/drain isolation capacitors. In addition, the last version of the multi-layer TFN's contained a decoupling resistor in the MMIC amplifier DC bias line.

In light of the functions provided by the carrier plate assembly, proper alignment of the TFNs and MMICs were highly critical factors affecting the RF performance of the individual radiating elements. Alignment of the radiating slot relative to the feedthrough in the carrier plate and relative to the patch element in the subarray housing was of critical importance to prevent significant mismatch and back radiation. Actual assembly of the carrier plates into the subarray

module is done manually using registration marks on the individual carrier plates and geometric references marked on the inside walls of the subarray housing.

Testing of the carrier plates was accomplished by the use of specialized fixtures an example of which are shown in Figure 4-16.

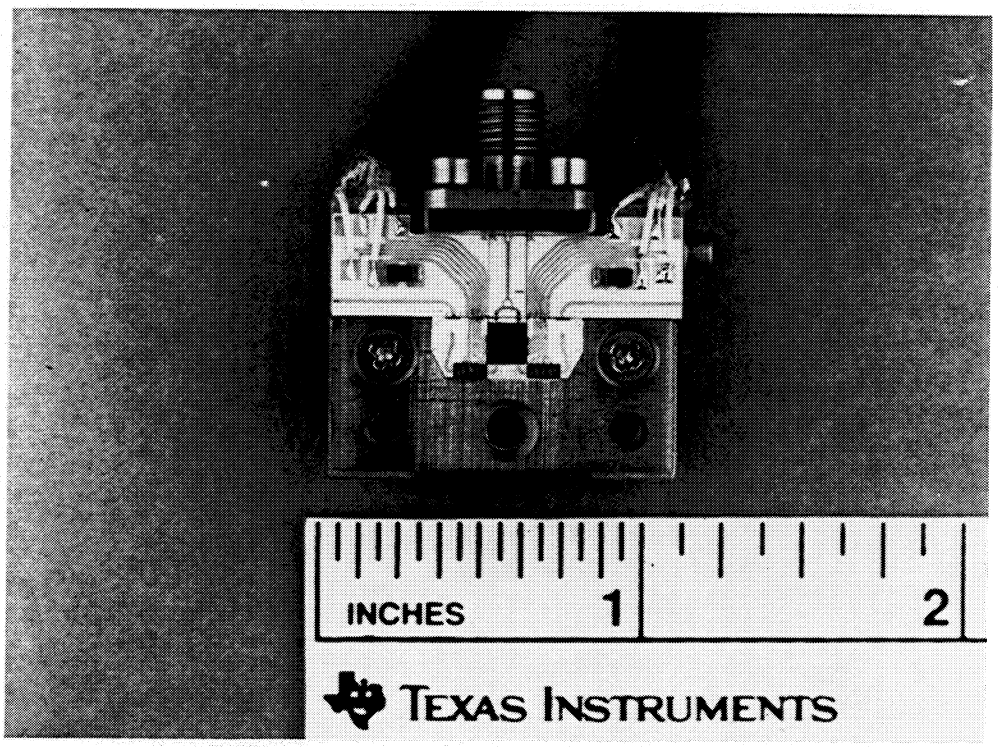


Figure 4-16. Carrier Plate Installed In Test Fixture

In the test fixture, RF is fed through a K-connector microstrip launch onto a microstrip circuit feeding the carrier plate. The amplifier output microstrip is positioned over a patch array which radiates into a absorber lined box containing a small horn antenna for sensing the output. The output of the horn is fed to a scalar network analyzer which allows comparative power output measurements. This measurement capability was used primarily to verify functionality of each carrier plate prior to subarray installation and to provide a comparative measure of compression behavior, operating bandwidth and power output to allow best matching of carrier plates for a single subarray.

An example of the scalar display for various levels of RF drive power for a single amplifier on a carrier plate is shown in Figure 4-17.

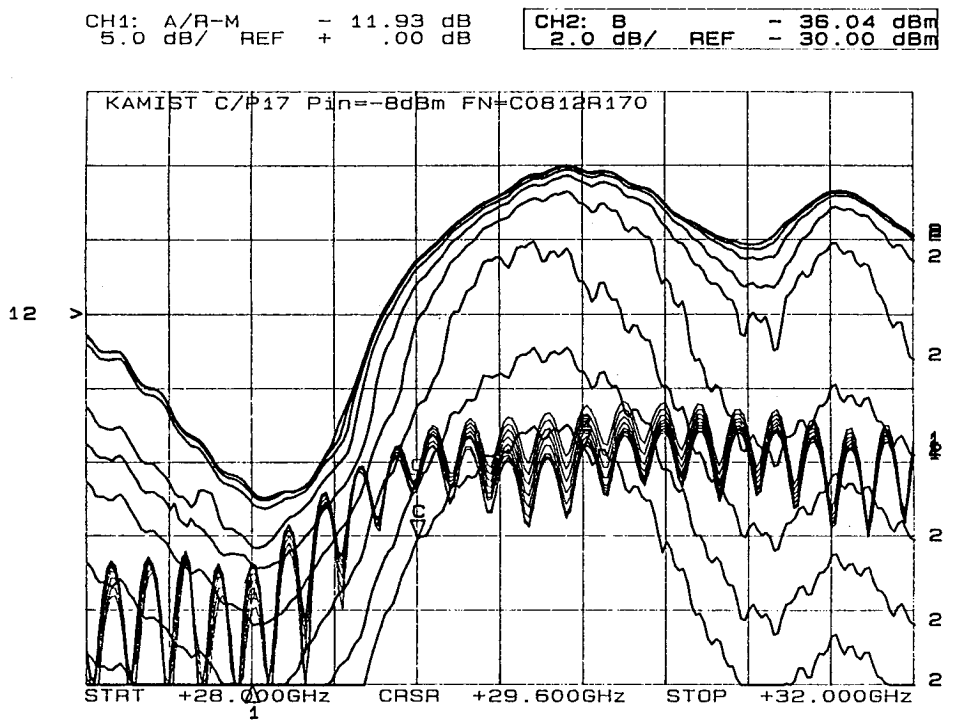


Figure 4-17. Carrier Plate Power Compression

4.6 DC/Logic Distribution & Control

Control of the subarray module and the distribution of the DC and logic commands is provided by a pair (one for each subarray half) of multi-layer thin film network PWBs (TFN-PWB). The TFN-PWB consists of a total of nine distinct layers alternating between polyimide insulators and metallic conductors. The multilayering approach was driven primarily by the number of logic and DC lines that were required to provide power and control logic to the individual radiating channels. Each TFN-PWB is populated with an ASIC, voltage regulator for the amplifier gate voltage, silicone IC switches (4) for enable/disable of the amplifier drain voltage, chain resistors for individual adjustment of gate voltage, and filtering capacitors. The ASIC provides the function of converting the serial logic provided by the controller to the parallel logic required by the subarray module. The ASIC is a serial to parallel latched shift register with TTL outputs to the drain switch IC's and bipolar outputs to the phase shifters. Serial data consisted of a clock, update strobe, and, amplifier control, phase shifter enable, and phase shifter bit set logic words. Figure 4-18 shows the layout of the multilayer board and Figure 4-19 shows the block diagram of the ASIC control circuit.

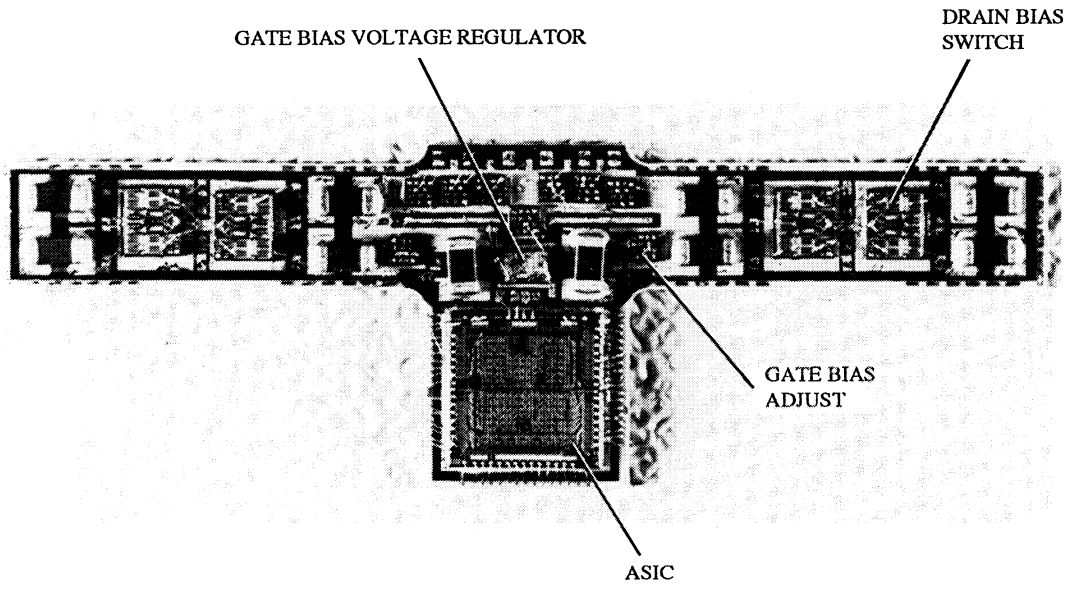


Figure 4-18. Multilayer TFN DC/Logic Distribution Board

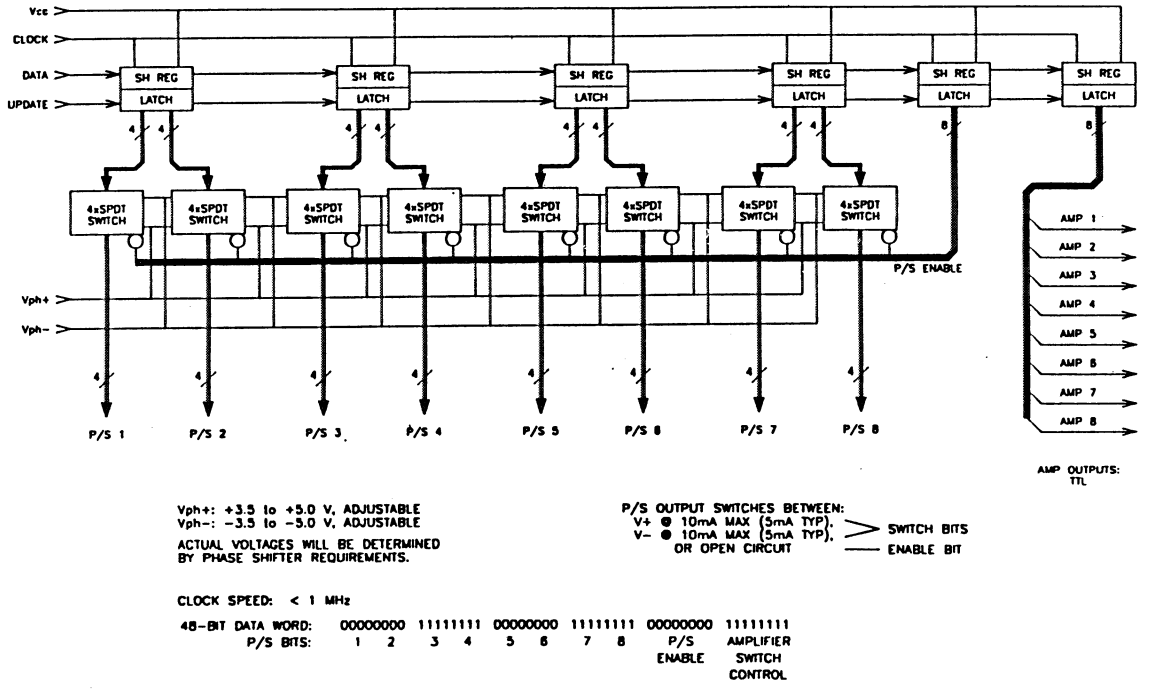


Figure 4-19. DC/Logic Distribution Block Diagram

5. SUBARRAY MODULE ASSEMBLY

Physical assembly of the subarray module in most cases utilized standard Texas Instruments microwave assembly techniques such as glass to metal sealing, furnace soldering, laser welding/trimming, MMIC, ASIC die bonding, component (capacitors, resistors, IC) bonding, wirebonding, and chisel bonding. However, due to the high level of integration, close tolerancing, and limited real estate in the subarray module, the processes used in most cases, pushed the threshold of processing capability.

The assembly process consists of a number of critical steps for installation, alignment, and testing of the various subsystems used the subarray module. The basic assembly process is described in the following. The process is described with all of the subassemblies (carrier plates, thin film networks, etc.) completed and with functional testing completed.

Install radiating elements. DC/logic input pins are installed with glass feed throughs and fired in a standard glass to metal seal furnace process. Cylindrical Sn96 solder preforms are installed into the housing diameters machined for the radiating elements and sized using a precision diameter pin. Radiating elements are then inserted into the housing diameter and held in place with an additional solder preform wrap. The housing subassembly is then fired in a vacuum solder reflow furnace with a specialized tool used to prevent significant movement of the radiating element during the liquid phase of the solder. Hermiticity tests are conducted to ensure proper flow of solder during the operation.

Install RF input assembly. The RF input subassembly is first bonded to the inside floor of the subarray module housing holding the position of the two RF microstrip output lines to within .002 of a registration feature on the housing. The upper portion of the K connector housing is then laser welded to the inside wall separating the two halves of the subarray module housing. The dielectric pin assembly for the connector is then inserted followed again by a laser welding operation to fasten the connector threads.

Install RF distribution carrier plate. The RF distribution carrier plate is a machined KOVAR piece bonded with conductive epoxy to the inside floor of the subarray module housing and serves as the carrier for the two way and four way power dividers and as a mounting pad for the DC/logic distribution TFN. The carrier plate is also used to match the height of the RF distribution network to the center RF feed and the RF transition to the MMIC carrier plates. Location of the distribution carrier plate is held to within .0015 ".

Install RF distribution thin films. Two way and four way power dividers are bonded to the surface of the RF distribution carrier plate maintaining alignment of ±.0015 between the RF input assembly and thin film microstrip lines.

Install MMIC carrier plates. MMIC carrier plates are bonded to the floor of the subarray module housing. Alignment of the radiating slot on the underside of the carrier plate feed thin films and the radiating elements is achieved through the use of a registration process. An intentional feature on the carrier plates which was used to correctly assemble the MMIC and thin films, is used to properly locate the carrier plate in the subarray module housing. Alignment of the microstrip feed lines from the RF distribution must simultaneously be maintained within ±.002 to minimize mismatch losses.

Alignment of RF interconnects. Steps 3, 4, and 5 are done simultaneously to ensure the best alignment possible of the RF interconnects. The individual subassemblies are installed using conductive epoxy and properly aligned relative to the feed and the radiating elements prior to cure of the epoxy.

Install DC/Logic distribution board. The DC/Logic distribution board is conductivly bonded to the pads on the RF distribution carrier plate.

Test. Functional testing of the subarray module is performed at this stage and includes measurement of individual RF channel performance, power consumption, and MMIC bias conditions. Individual control of each RF channel (on/off, phase bit control) enabled the functional testing of the subarray module in a bench test environment. Active range testing of the subarray module follows functional bench testing.

5.1 Subarray Module Performance

Each of the three subarray modules delivered for this program were characterized using a millimeter wave indoor rectangular antenna range at Texas Instruments facilities in McKinney, Texas. For the test, an individual subarray module is mounted flush with an 18 x 1 inch ground plane with the outer 10 inches on all sides covered with absorbing material. RF drive power of approximately 125 mW is supplied to the subarray input connector. DC power and control logic is provided using discrete power supplies and the 486 class PC used as the array controller connected to the subarray via a single cable. Cooling of the subarray in the range is provided by chilled water circulated through a cold plate mounted to the backside of the subarray module. Figure 5-1 shows a single subarray mounted on the positioner mast in the antenna range.

To generate the calibration files required for the array controller, an automated data collection sequence was established in the Antenna Test Range. An HP-IB type data interface card was installed in the array controller PC and connected to the range receiver. A short control program was written to automatically command the array controller to enable a single amplifier, cycle through all 16 phase states, read the phase and amplitude measured by the range receiver, and store the phase data in a calibration file. This process was repeated for each element and used to build a calibration map file for the operation of the full subarray module. Amplitude data was also stored but is not used by the array calibration file.

Figure 5-1. Subarray Module in Antenna Range Fixture

Using the data collection program, insertion phase and amplitude measurements were recorded for each element and phase state. The phase data is inserted into a calibration file used by the subarray controller to calculate proper phase state setting for steering the beam. Amplitude measurements are not used in the subarray control but were used to examine the performance of the power amplification in the subarray environment. Figure 5-2 shows an example amplitude map where relative power measured at the range receiver is plotted versus phase state. As can be seen in the amplitude map, the power output of individual elements is insensitive to phase state. Power output variation between elements ranges from approximately 3-4 dB.

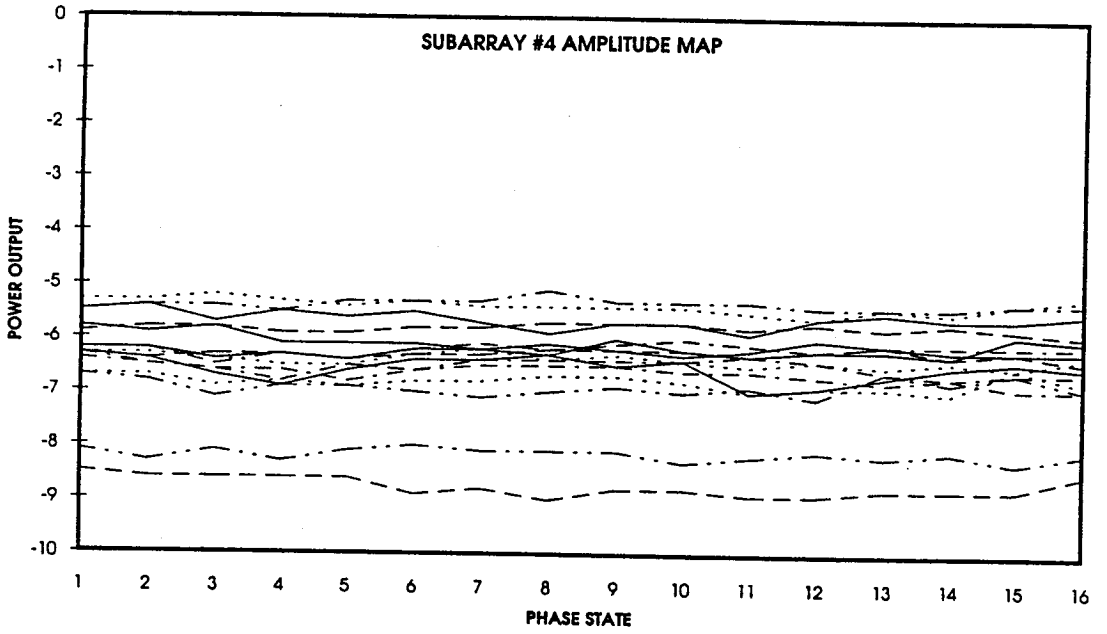
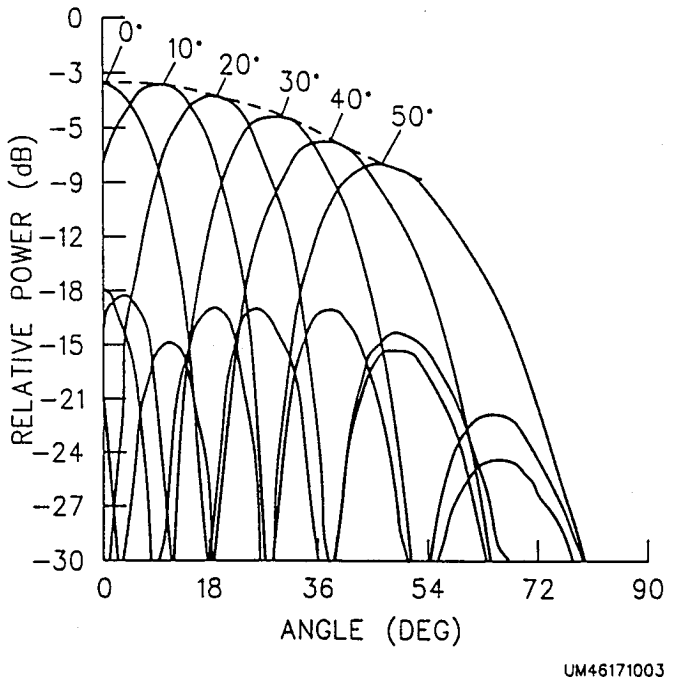


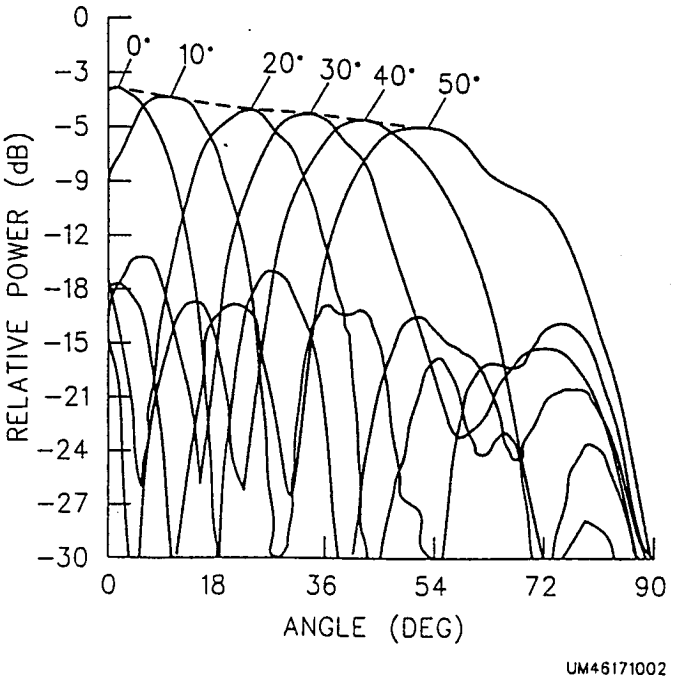
Figure 5-2. Amplitude Map of Subarray

Figure 5-3 shows the measured scanned beam patterns in the H and E planes. As shown in the figure, the gain rolloff as a function of scan angle is less than 3 dB over a 30 degree scan angle. Measured EIRP of the best performing subarray module was 77 watts (1.6 watts total RF power) with a power consumption of approximately 10 watts yielding a DC to RF efficiency of approximately 16 percent for the entire subarray.

Comparison of the measured data against the established requirements noted in Table 2-1 shows the performance of the subarray module met all the goals and requirements of the program.



(a) H–Plane



(b) E–Plane

Figure 5-3. Scanned Performance of the Subarray Module

6. 32 Element Array System Description

With the original program objectives having been achieved with the antenna range demonstration of a single subarray module, the next objective was to integrate two of the subarrays into a single 4 x 8 (32 element) array capable of being used in a controlled flight environment. This objective was critical as it provided the opportunity for the subarray modules to be used in non laboratory environment. As this represented a practical use of what essentially was a laboratory based concept validation program, a new set of requirements were generated reflecting the added packaging complexity of providing RF drive, DC power, associated regulation, logic distribution, logic control, thermal management, and the appropriate interfaces.

Table 6-1 shows the specifications generated for the 32 Element Array.

Table 6-1. Specific Requirements for the 32 Element Array Assembly

Center Frequency	29.63 GHz
Array Type	Transmit
Array Geometry	4 X 8 rectangular grid
Number of elements	32
Number of Beams	1
Radiating element	Aperture coupled patch element
Element gain	5 dB
Subarray bandwidth	5%
Scan requirements	± 30 °
Grating lobes	None in visible space for broadside beam
Transmit RF power	3.0 W
Input RF power	1 mW Maximum, (.3 mW minimum)
EIRP	200 W Minimum
Polarization	Vertical
Pointing accuracy	1/4 of a beamwidth
Thermal management	Thermoelectric, forced air cooling
DC power input	28 VDC unregulated, single input
Power up sequence	Automatic timing
External controller	486 PC with serial data output
Interface	Standard RF, aircraft type connectors
Operating environment	Controlled flight pressurized to 8,000 ft

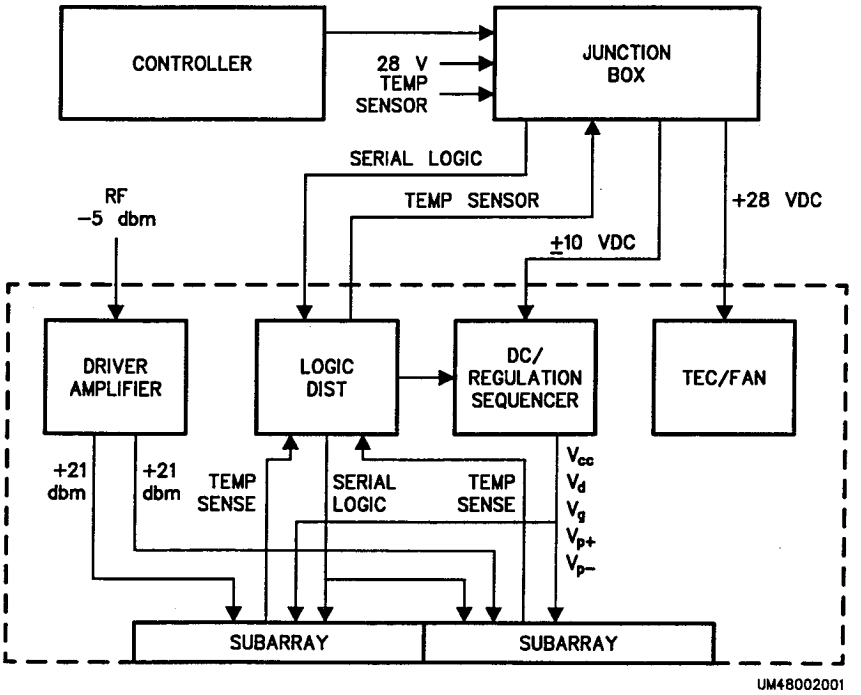


Figure 6-1. Block diagram of the 32 Element Array Assembly

A block diagram of the array assembly equipment package is shown in Figure 6-1 with the basic mechanical layout shown in Figure 6-2. The basic equipment consists of the array assembly, junction box, controller, and interface cabling. The array assembly contains an RF driver amplifier/power splitter assembly, DC power conversion and regulation for the subarray module bias voltages, distribution circuits for the serial logic control signals, timing circuit for automatic sequential application of bias/supply voltages, thermoelectric cooling devices, cooling fan, and two subarray modules. The array assembly is shown in Figure 6-3 and Figure 6-4. As discussed in the array thermal analysis, the physical size of the array was driven by a desire for maximum reliability of the subarray modules. It should be noted that for this application, space was not a constraint so the cooling structure was made intentionally large. If needed, this structure size could be significantly reduced to accommodate flush mounting applications for the use of tile subarrays.

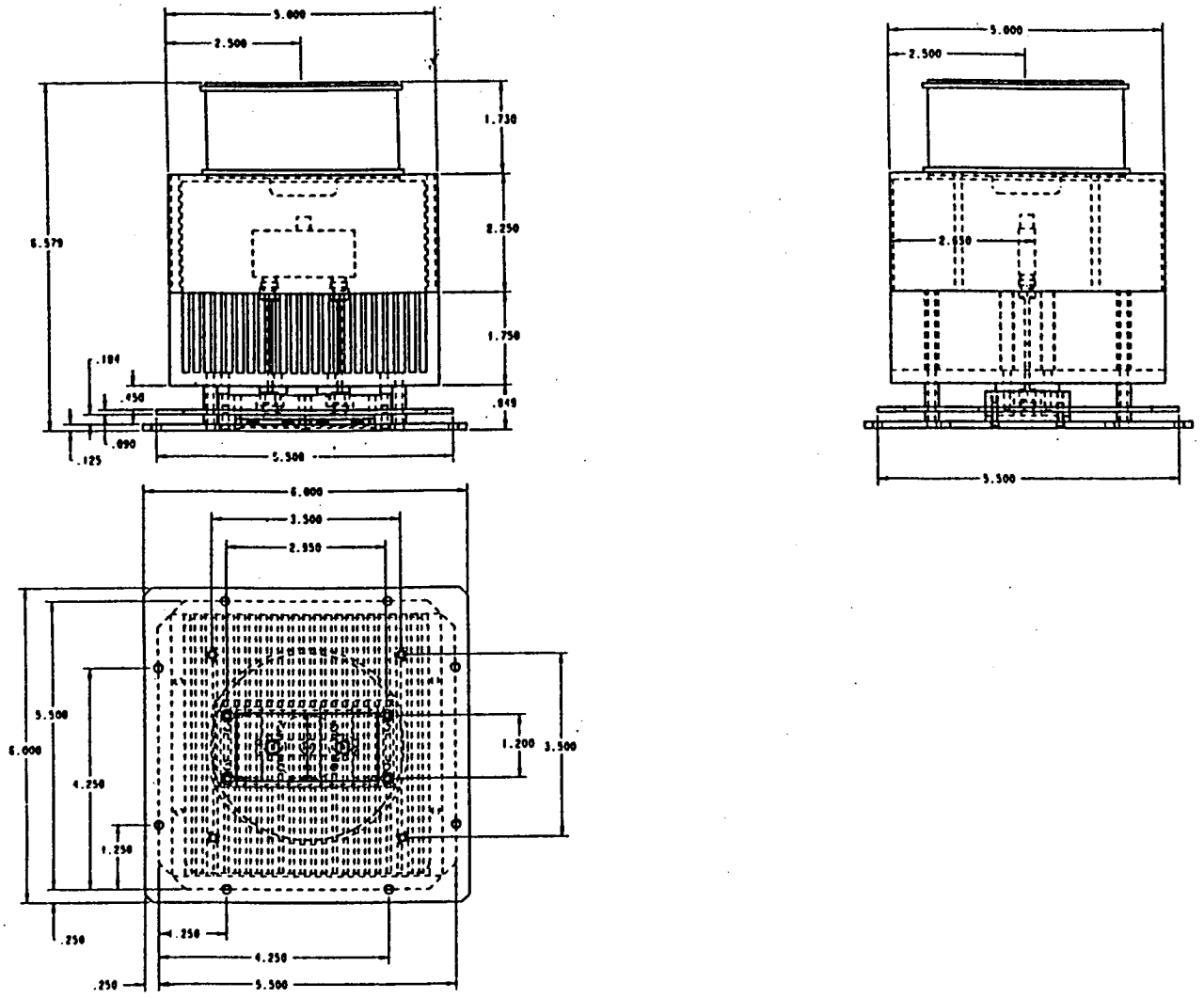


Figure 6-2. Mechanical Layout of the 32 Element Array Assembly

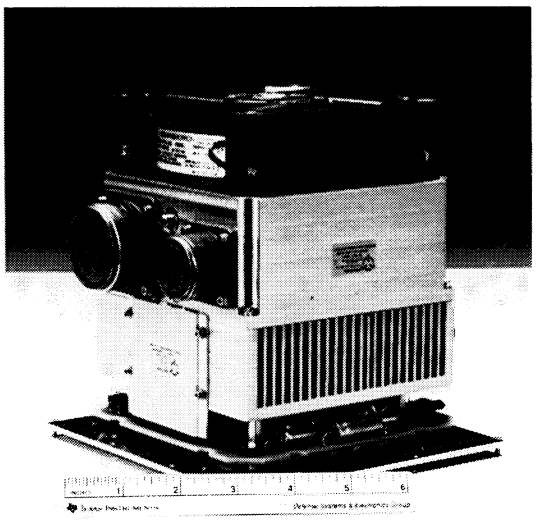


Figure 6-3. Side View of the 32 Element Array Assembly

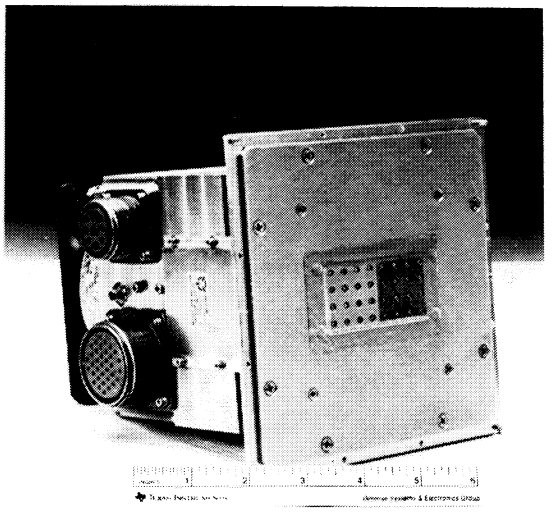


Figure 6-4. Front View of the 32 Element Array Assembly

The junction box contains two DC to DC power supplies for conversion of the 28 VDC unregulated supply to +10 and -10 drive voltage, a voltage controller for the thermoelectric cooling devices, and the appropriate routing for interfacing the controller to the array assembly. The array assembly envelope is approximately 6 x 6 x 7 inches while the junction box envelope is approximately 6 x 7 x 4 inches. The same 486 PC controller used for the subarray modules was used as the controller for the array assembly.

The individual subarray module designed for a laboratory operating environment required five different regulated DC power supplies (V_{cc} , V_{drain}, V_{gate}, V_{phase} (+), and V_{phase} (-)) to operate. As multiple power supplied were not desirable for the flyable array, DC regulation was provided occurring in two stages. The junction box which contained DC to DC power supplies provided the initial stage and fed +10 and -10 VDC to the array via one of the interface connectors. Additional regulation and conversion to the required operating voltages was accomplished in the array assembly via use of appropriate circuits. An additional circuit built into the array assembly provided an automatic power up sequence by applying the bias circuits in a specific order to prevent unintentional damage to the amplifiers and ASIC. This provision enabled the power up sequence (from a users point of view) to be completed with the flip of a single switch.

A critical feature of the array assembly is that RF drive power for the two individual subarray modules is provided by an integral drive power amplifier subassembly. The driver amplifier requires a minimum input of -5 dBm at a single connector and provides approximately 22 dBm at each of the two output connectors. DC regulation and turn on sequence is integrated into the subassembly.

6.1 32 Element Array Thermal analysis

The baseline packaging approach was driven by the desire to provide a large design margin specifically in the areas of thermal management and DC power regulation. It has been well established that GaAs MMICs provide exceptional reliability under high levels of thermal stress at frequencies commonly used for radar applications. Extended periods of time with MMIC junction temperatures of 130°C are considered normal operating parameters for MMICs in wide use today. However, as the amount of readily available reliability data proving similar attributes of the high frequency P-HEMTs used is limited, the choice to provide significant thermal design margin was made. To maintain the array mechanical structure at a reasonable size, thermoelectric cooling coupled with forced air was used as the baseline approach. Thermal analysis of the structure using measured power consumption of the individual subarrays and the integrated DC regulation , logic distribution circuits determined the actual size of the delivered array package. The objective of the thermal management approach and array packaging was to maintain the subarray module face at approximately 25-30°C which would translate into amplifier MMIC junction temperatures in the 80-100°C range. To provide the requisite cooling, three individual thermoelectric devices with a combined heat transfer load of 45 W are attached thermally to the backside of the subarray modules. Heat transferred from the TEC devices is conducted to a finned heat sink cooled by forced air. Experience gained during the testing of the array indicated

that with the TEC devices driven to approximately 50 percent of capacity, the stable temperature of the array remained in the 25-30°C range even when operated continuously for 3-4 hours under ambient atmospheric conditions. Relative temperature of each subarray is monitored via an IC physically attached to each subarray module with the output routed to connections on the junction box. The IC's provide a current output proportional to the temperature of the subarray in degrees Kelvin. This capability was used to monitor changes in temperature during operation on a real time basis.

6.2 32 Element Array Performance

Test and characterization of the 32 element array assembly was accomplished in the same manner as the individual subarray modules. The array controller was modified to handle 32 elements instead of 16 and was used in conjunction with the automated range set up to generate phase state tables for the proper control and pointing of the array. E and H plane patterns were measured both in the typical azimuth/phi scans as well as multiple off axis pointing vectors needed for the planned series of airborne and land mobile tests. Figure 6-5 shows the E-plane boresight pattern and Figure 6-6 shows the H-plane boresight pattern. Figure 6-7 shows a series of E-plane patterns to demonstrate the scan performance out to 50 degrees scan. Small steering angle measurements taken during the range testing showed the steering accuracy of the array to be approximately 2 degrees. Measured EIRP of the 32 element array was in excess of 300 watts.

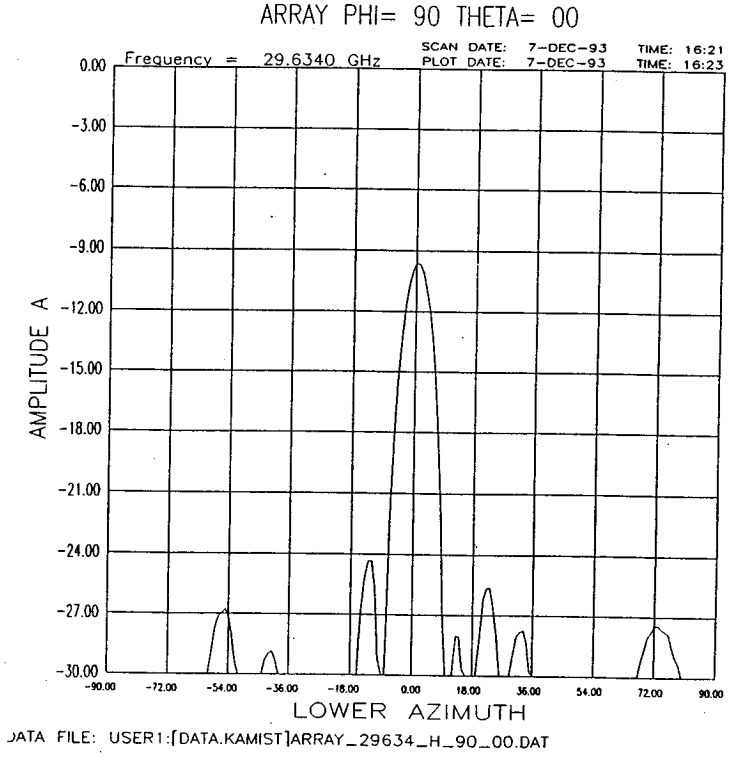


Figure 6-5. E-Plane Boresight Pattern

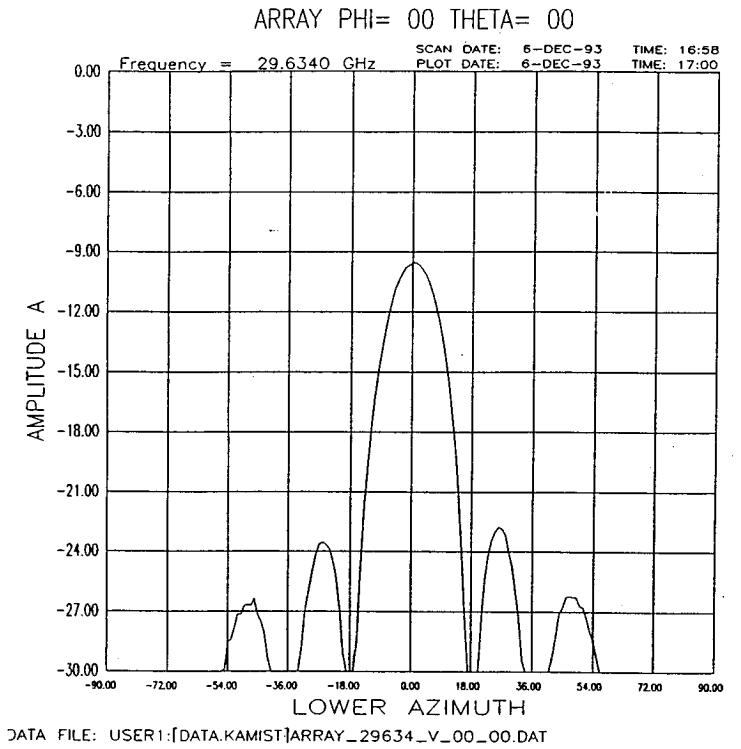


Figure 6-6. H-Plane Boresight Pattern

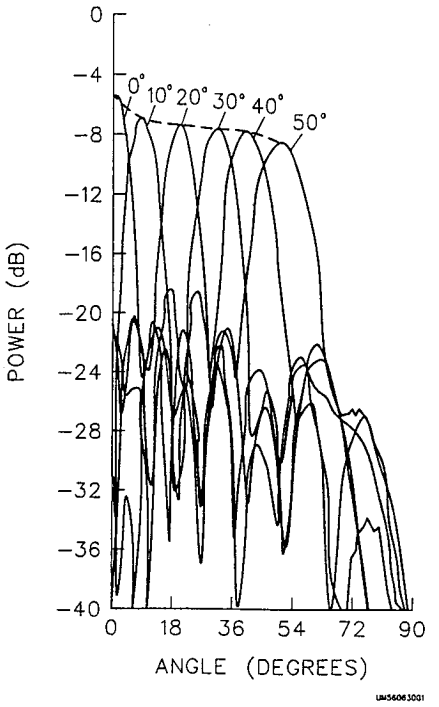


Figure 6-7. Scanned Performance of the 32 Element Array

7. Summary and Next Steps

The original objective of this program was to demonstrate in a laboratory environment, the insertion of MMIC device technology into an application supporting advanced communication satellite antenna systems. This objective was clearly met with the first demonstration of a single subarray module. This subarray module showed the technical viability of a true tile phased array architecture while overcoming a number of technical roadblocks related to the efficient integration and control of millimeter wave phased array building blocks. However, the success did not end with attainment of the primary objective. As the objectives of the program evolved over time to require a higher level of integration for support of the AERO-X and land mobile experiments, the resultant successes of the program went well beyond the original scope. In addition to proving the viability of the tile phased array architecture, this effort produced a sub-system capable of practical use and demonstration in a real world application.

For the potential represented by the achievement of the Ka-Mist Subarray Module to be realized, the work begun on this program must be continued with the goal of simplifying the construction and the cost of the array. Significant applications both military and commercial will be realized when the tile array technology moves out of the technology development arena and into a product development arena. This will happen when the using community perceives that the technology can be made affordable. Specific areas to be worked in the future include use of monolithic approaches to the MMIC insertion, soft substrates for lower fabrication costs, and elimination of the conventional wirebonding interconnection techniques through the use of mutilayer vertical interconnect technology.