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Silicon Satellites: Picosats, Nanosats, and Microsats

Siegfried W. Janson, Mechanics and Materials Technology Center
The Aerospace Corporation, El Segundo, CA, 90009

Abstract

Silicon, the most abundant solid element in the Earth's lithosphere, is a useful material for spacecraft construction. Silicon is stronger than stainless steel, has a thermal conductivity about half that of aluminum, is transparent to much of the infrared radiation spectrum, and can form a stable oxide. These unique properties enable silicon to become most of the mass of a satellite; it can *simultaneously* function as structure, heat transfer system, radiation shield, optic, and semiconductor substrate.

Semi-conductor batch-fabrication techniques can produce low-power digital circuits, low-power analog circuits, silicon-based radio-frequency circuits, and micro-electromechanical systems (MEMS) such as thrusters and acceleration sensors on silicon substrates. By exploiting these fabrication techniques, it is possible to produce highly-integrated satellites for a number of applications. This paper analyzes the limitations of silicon satellites due to size. Picosatellites (~ 1 gram mass), nanosatellites (~1 kg mass) and highly-capable microsatellites (~10 kg mass) can perform various missions with lifetimes of a few days to greater than a decade.

I. Why Silicon?

I.A. Silicon as a Structural Material

Mechanical properties of silicon, aluminum, stainless steel, titanium, and diamond are given in table 1. Silicon is already used as the structural material for microelectromechanical systems (MEMS) due to it's high strength[1] and should be considered for spacecraft structure as well. Single crystal silicon is stronger than aluminum, stainless steel, or titanium, yet it is less dense. Materials with intrinsically high strength-to-density ratios are particularly valuable for spacecraft due to launch costs of ~$10,000 per kg to Low Earth Orbit (LEO) and ~$50,000 per kg to geosynchronous Earth orbit (GEO). Note that titanium has a higher strength-to-density ratio than aluminum or stainless steel, yet it is still more than an order-of-magnitude less than what silicon provides. Single crystal diamond has the best strength-to-density ratio, but the material cost (~$10,000 for a man-made 2 gram crystal) is many orders-of-magnitude higher than the launch cost. Single crystal silicon carbide (see ref. 1) has a strength-to-density ratio between silicon and diamond, and should also be considered for some spacecraft applications.

Table 1. Mechanical properties of silicon compared to other structural materials.
(Data from references 1, 2, 3, 4, and 5)

	Density ($g\ cm^{-3}$)	Yield Strength (MPa)	Strength/Density (MN-m/kg)	Young's Modulus (GPa)
Silicon (single crystal)	2.3	7,000	3.0	~170
Aluminum (2024-T3)	2.8	350	0.13	73
Stainless Steel (304)	8.0	1,000 (cold worked)	0.13	200
Titanium (Ti-6Al-4V)	4.4	900	0.20	115
Diamond (single crystal)	3.5	50,000	14.3	~1,000

While metals are available in a variety of shapes and sizes, single crystal silicon is available in 10, 12.5, 15, and 20 cm diameter cylinders up to 2 meters long. Present manufacturing costs are about $185 per kg which could drop to ~$50 per kg by adopting new refinement techniques.[6] Even though the material cost (per kg) of single crystal silicon is much more expensive than typical spacecraft structural materials, it is still more than an order-of-magnitude less than the launch cost. Silicon is a viable structural material, especially for small satellites.

Thermal properties of silicon, aluminum, stainless steel, titanium, and diamond are given in table 2. Silicon has a high specific heat and a much higher melting point than aluminum. Silicon is a very good heat conductor; it has a higher thermal conductivity than stainless steel and titanium, and about 50% that of aluminum. Silicon also has a thermal expansion coefficient that is ~4 times lower than titanium and about an order-of-magnitude lower than aluminum and stainless steel. Once again, diamond has superior properties, but it must be used sparingly due to its high cost.

Table 2. Thermal properties of silicon compared to other structural materials. Specific heat, thermal conductivity, and thermal expansion coefficient at 300 K.

	Thermal Conductivity (W/m °K)	Thermal Expansion Coefficient (cm/cm °K)	Melting Temperature (K)
Silicon (single crys.)	150	2.5×10^{-6}	1700
Aluminum (2024-T3)	240	2.2×10^{-5}	~850
Stainless Steel (304)	16	1.7×10^{-5}	~1700
Titanium (Ti-6Al-4V)	8	9×10^{-6}	~2100
Diamond (single crys.)	2,100	1.0×10^{-6}	4200

I.B. Silicon as an Optical Material

Silicon can be used as an optical material throughout most of the infrared spectrum. As shown in figure 1, it is transparent between 1.4 and 7 microns (wavelength) and from 25 to beyond 100 microns. The maximum transmission of 54% results from the index-of-refraction of ~3.5 over this wavelength range. Index-matching coatings or surface texturing can be used to bring transmission efficiencies close to 100% over selected ranges of interest.

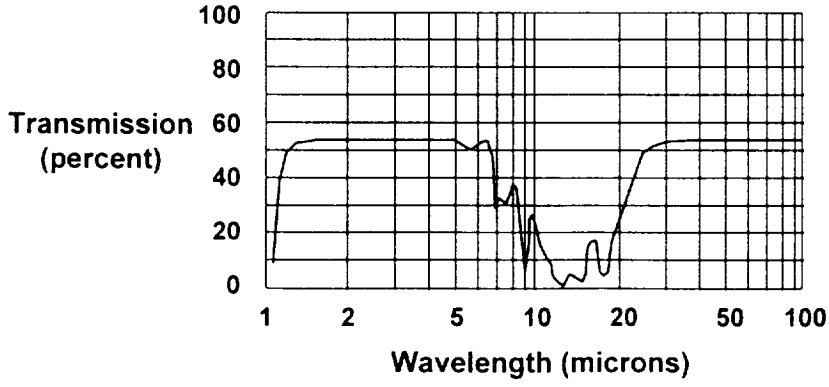

Figure 1. Optical transmission of silicon in the infrared.

I.C. Silicon as a Substrate for Electronics

Microprocessors, microcontrollers, memory, and other digital integrated circuits (ICs) are batch-fabricated primarily on silicon wafers. These wafers are cut from larger single crystals which have been ground into a cylindrical shape. Hundreds of identical devices are fabricated on a single side of a 0.5 to 1 mm thick, 10 to 20 cm diameter, silicon wafer which is cut apart to release the individual rectangular silicon dice. These dice are then mounted in plastic or ceramic carriers which provide hermetic sealing against the environment, mechanical rigidity, improved heat dissipation, and electrical connections which can be soldered or plugged into a circuit board.

Almost the entire mass and volume of spacecraft electronic systems is determined by packaging; i.e. enclosures ("boxes"), connectors, circuit boards, and chip carriers. Multi-chip modules (MCMs) place multiple electrically-connected die in a single carrier to reduce wasted space and increase active device area density. MCMs can achieve 10 to 15 times greater IC packaging densities on circuit boards than conventional single-die packages with greater system performance and reliability at lower cost.[7] The next step in reducing packaging size and mass is to produce wafers with interconnected dice. This wafer-scale integration eliminates unnecessary dicing, wiring, and packaging.

How much silicon "real estate" (area) is required for typical functions? Silicon die areas currently range from ~0.2 cm^2 for microcontrollers to ~2 cm^2 for high end microprocessors. A PIC16C71 microcontroller dice is 0.4 cm x 0.5 cm in size[8] while a PowerPC 604 dice is 1.24 cm x 1.58 cm.[9] Dynamic random access memory (DRAM) die, suitable for use with microcontrollers and microprocessors, require ~0.03 cm^2 of silicon per million bits of storage capacity. Feature sizes are steadily decreasing with time and high-end integrated circuits are becoming more complex. Projections of dice size for DRAMs and high-end microprocessors over the next 15 years, given in table 3, show the interesting result that dice size for these products is expected to increase with time. By the year 2010, high-end microprocessor and DRAM dice could be several cm on a side. To support efficient packing of rectangular dice on circular silicon wafers during fabrication, 30 cm diameter and larger silicon wafers will become common.

Table 3. Roadmap projections for semiconductor technology. (From reference 10)

Year	Smallest Feature (μm)	Dynamic RAM: Dice Size (cm^2)	Dynamic RAM: Billions of Bits per Dice	Microprocessors: Dice Size (cm^2)	Microprocessors: Millions of Transistors per cm^2
1995	0.35	1.9	0.064	2.5	4
1998	0.25	2.8	0.256	3.0	7
2001	0.18	4.2	1	3.6	13
2004	0.13	6.4	4	4.3	25
2007	0.10	9.6	16	5.2	50
2010	0.07	14.0	64	6.2	90

A single ~4 cm x 4cm DRAM dice in the year 2010 could hold 8 *gigabytes* of information; more capacity than is currently available on CD-ROMs and most personal computer hard disk drives. A single DRAM could hold an uncompressed 1000 km x 400 km image with 10-meter spatial resolution and 16 bits of intensity resolution. The command and data handling (C&DH) system for a future satellite could reside in 1 or 2 dice and fit on a 10 cm diameter wafer with extra silicon area for communications systems, power controllers, etc.. If circuit complexity remains fixed, circa 2010 dice could be much smaller than today's versions due to a factor of 5 reduction in feature size. A future microcontroller

equivalent to the PIC16C71, for example, would fit on a dice smaller than 1 mm on a side. The total silicon area required for the C&DH system in a current generation microsatellite would shrink from ~ 2 cm^2 to ~ 0.1 cm^2.

Microprocessors and microcontrollers have been steadily increasing in performance due to increases in operating speed, partially enabled by smaller feature sizes, and improvements in processing architectures. Microprocessor clock speeds were a few MHz during the early 1970's, are in the low 100 MHz range today, and are expected to reach the GHz range by 2010. The INTEL 8086 microprocessor, introduced in 1978, had a 0.33 million-instructions-per-second (MIPS) performance with a 5 MHz clock speed while the INTEL Pentium, introduced in 1993, had a 112 MIPS performance with a 66 MHz clock speed.[11] By extrapolating the exponential performance increases in microprocessors over the last 15 years (about a 1.5 times increase in performance per year), the predicted performance by 2010 is 100,000 MIPS. This is quite staggering when one realizes that NASA's Galileo probe uses a mere 0.5 MIPS processor for C&DH.

While silicon has been the substrate of choice for commercial digital circuits, operating frequencies of ~1 GHz and higher will require special wafers or another substrate such as gallium-arsenide. Currently, silicon offers lower cost and simplified power requirements while gallium arsenide offers higher frequency operation and higher efficiency. A comparison of silicon and gallium-arsenide transistor circuits is given in table 4. The gallium arsenide cost in table 4 is based on a total manufacturing cost of $1500 per 10 cm diameter wafer with a 75% yield.[12]

Table 4. Basic comparison between gallium-arsenide and silicon transistor integrated circuits. Data from reference 12.

Parameter	Gallium-Arsenide MESFET	Silicon Bipolar
Cost per mm^2	$0.25 (10 cm diameter wafer)	$0.10 (20 cm diameter wafer)
Cutoff frequency	18 to 25 GHz	12 to 18 GHz
Breakdown Voltage	15 to 20 V	5 to 9 V
Substrate	Insulating	Conductive
Noise figure @ 5 GHz	1.5 dB	6.0 dB
Bias requirements	positive and negative	positive
Power added efficiency	60%	40%

While data processing circuits may not yet run at GHz clock speeds, satellite communications circuits routinely operate from ~100 MHz to greater than 20 GHz. Below ~1 GHz, conventional CMOS technologies on conventional silicon wafers can provide inexpensive radio-frequency integrated circuits. One group at UCLA is investigating 2-chip and single-chip fully-integrated (rf, analog, and digital) CMOS transceivers for operation in the 900 MHz industrial, scientific, and medical (ISM) band.[13] Their goal is to produce a frequency-hopped spread-spectrum transceiver with up to 160 kilobit/sec data transfer rates at 20 mW power output and 100 milliampere, 3 Volt DC input.[14]

Above 1 GHz, gallium arsenide offers increased DC-to-RF conversion efficiency for power amplifiers and decreased noise for preamplifiers (low noise amplifiers at the receive antenna) used in communications systems. Standard silicon microwave monolithic integrated circuits (MMICs) usually perform poorly above a few GHz because commercial wafers have a resistivity on the order of 10 Ω-cm,

which is too low to act as a good dielectric.[15] Better performance can be achieved using high-resistivity silicon substrates (10,000 Ω-cm and higher for up to 40 GHz operation) or silicon-on-insulator (SOI) construction. A more recent development is silicon-germanium (SiGe) technology that offers higher than 70 GHz operation on silicon substrates.[16,17] Today's silicon technology can be used for satellite communications bands from VHF (very high frequency; ~140 MHz) to S-band (2.5 to 2.7 GHz). Future advancements in silicon technology will push the operating frequency range higher.

I.D. Silicon as a Radiation Shield

The near-Earth space environment is much harder on electronics than the surface environment due to the presence of high-energy electrons, protons, and heavier ions. Elastic scattering of high energy protons and ions results in displacements of stationary target atoms while inelastic scattering results in secondary particle "showers" of lower-energy target atoms or fission daughter products. High-energy electrons, protons, and ions all leave ionizing tracks behind them. Anomalous effects in semiconductor circuits due to these interactions range from a temporary change in logic state, due to the sudden appearance of charge, to permanent substrate atom and charge dislocations which produce altered current-voltage characteristics and possible device failure.[18] Single-event upsets (SEUs) are particle-induced "bit-flips" while latchups are more serious high-current flow conditions generated by new low-resistance paths created by particle-induced ionization trails. Both SEUs and latchups can be controlled by appropriate choice of semiconductor technology, "watchdog" and error-correction circuits, and error-correction software. Continual accumulation of radiation damage, however, ultimately results in device failure.

Table 5, adapted from reference 19, gives rough radiation hardness levels for different types of semiconductor devices. A *rad* is the amount of particle radiation that deposits 100 ergs of energy per gram of target material and the radiation hardness level represents total dose required for device failure. Typical low-power consumer electronic components (CMOS) are designed to operate in our low-radiation biosphere (roughly 0.3 rad/year) but can tolerate 1 to 10 kilorad integrated radiation doses. Unfortunately, the radiation tolerance varies widely from design to design so radiation testing should be performed on selected components. Transistor-transistor logic (TTL) and emitter-coupled logic (ECL) circuits are inherently more radiation hard than CMOS, but they require more power. NMOS, PMOS, I^2L, and silicon-on-sapphire MOS circuits can be fully immune to latchup. Radiation hardening requires a balance between power and circuit availability for choice of technology, mass requirements for shielding, and circuit complexity for latchup and SEU control.

How much silicon radiation shielding is required for a given mission? Dose rates for a silicon target are usually given as a function of grams/cm^2 or thickness of spherical aluminum shielding for a given orbit and given solar conditions (i.e. minimum or maximum solar activity). Silicon and aluminum are next to each other on the periodic table; their nuclei and average atomic masses differ by only one proton, and they have similar densities. Both materials have similar ability to slow down incident energetic electron and protons while silicon generates a slightly higher level of bremsstrahlung X-rays because bremsstrahlung is proportional to the square of the atomic number (14^2 for Si vs. 13^2 for Al). Aluminum and silicon shielding thicknesses in grams/cm^2 are equivalent within the uncertainties of radiation environment estimates.

Table 5. Radiation hardness levels for semiconductor devices

Technology	Total Dose in rads (silicon)
CMOS (soft)	10^3 - 10^4
CMOS (hardened)	5×10^4 - 10^6
CMOS (silicon-on-sapphire: soft)	10^3 - 10^4
CMOS (silicon-on-sapphire: hardened)	> 10^5
ECL	10^7
I^2L	10^5 - 4×10^6
Linear integrated circuits	5×10^3 - 10^7
MNOS	10^3 - 10^5
MNOS (hardened)	5×10^5 - 10^6
NMOS	7×10^2 - 7×10^3
PMOS	4×10^3 - 10^5
TTL/STTL	> 10^6

Figure 2 shows the yearly dose rate due as a function of aluminum shielding thickness (full sphere shielding) for 700 km altitude orbits with inclinations of 28.5° and 98.2°. CMOS circuits with an assumed total radiation dose tolerance of ~3000 rads will require at least 0.3 g/cm^2 aluminum (or 1.3 mm of silicon thickness) shielding for a 1 year on-orbit lifetime in a 700 km, 28.5° inclination orbit. For the more interesting sun-synchronous (98.2° inclination) orbit, about 0.8 g/cm^2 (or 4 mm silicon thickness) is required for a 1 year lifetime and about 3 g/cm^2 (1.3 cm silicon) for a 10 year lifetime. At lower altitudes, significantly less shielding is required, while at higher altitudes, significantly more shielding may be required. Use of more radiation-resistant technologies is the only solution for some orbits.

Figure 3 shows the dose rate dependence as a function of circular equatorial orbit altitude inside spherical aluminum shields with densities of 0.5 g/cm^2 (0.18 cm thick aluminum or 0.21 cm thick silicon) and 3.0 g/cm^2 (1.1 cm thick aluminum or 1.3 cm thick silicon). Note the rapid rise in dose rate with altitude below 1000 nmi (1850 km), the existence of a hard-to-shield proton belt at ~2000 nmi (3700 km), and the existence of an easier-to-shield electron belt at ~10,000 nmi (18,500 km). At geosynchronous Earth orbit (GEO; 35,786 km or 19,320 nmi altitude and 0° inclination) with a maximum dose of 3,000 rads, 0.5 gm/cm^2 (0.22 cm silicon) and 3.0 gm/cm^2 (1.3 cm silicon) shielding give lifetimes of roughly 11 days and 3 years, respectively.

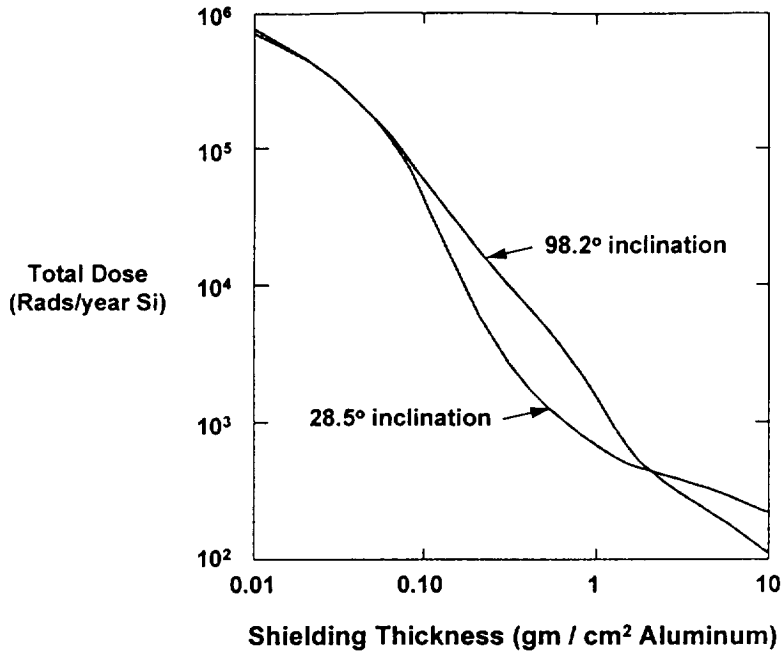

Figure 2: Total yearly dose, under solar maximum conditions, in silicon as a function of aluminum shielding thickness for 700 km circular orbits. Data adapted from reference 20.

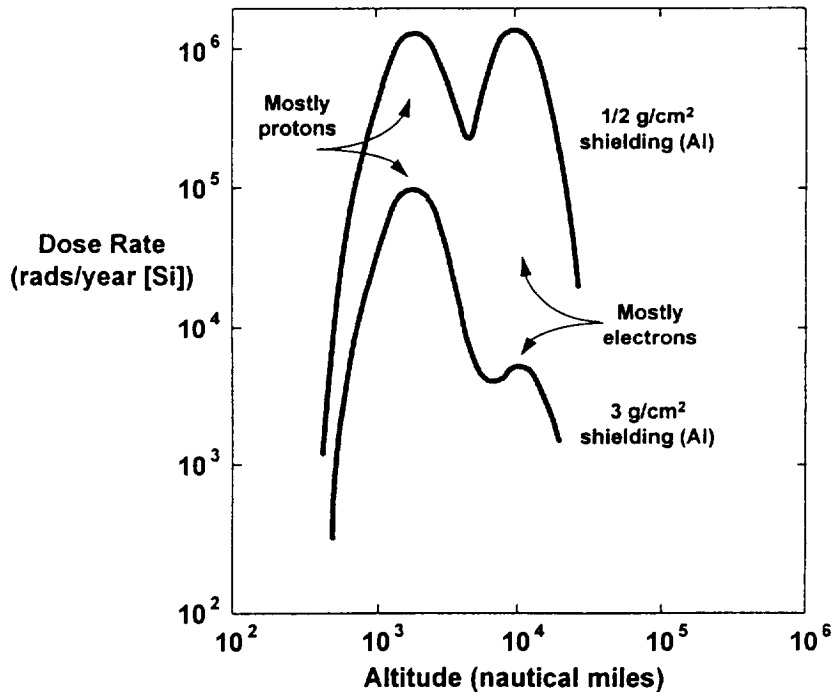

Figure 3. Radiation environment for circular equatorial orbits. (Adapted from ref. 19)

I.E. Silicon as a Substrate for Spacecraft Systems

Microelectro-mechanical systems (MEMS) such as micron-scale silicon diaphragm pressure sensors, acceleration sensors, chemical sensors, and valves have already been demonstrated.[21,22,23,24] Concepts for silicon-based, batch-fabricated chemical and electric propulsion systems suitable for small satellites have also been presented.[25] Integration of MEMS with microelectronics for data processing, memory, signal conditioning, power conditioning, and communications results in a stand-alone "application-specific integrated microinstrument" (ASIM). Examples of MEMS and ASIM applications for spacecraft can be found in reference 26 and in other papers from this conference.

II. Silicon Satellites

II.A. Introduction

The silicon satellite, as introduced in references 27 and 28, presented a new paradigm for space system design, construction, testing, architecture, and deployment. Integrated spacecraft complete with some degree of attitude and orbit control can be designed for mass-production using batch-fabrication techniques. Integrated circuits for C&DH, communications, power conversion and control, on-board sensors, attitude sensors, and attitude control devices can be manufactured on thick silicon substrates that provide structure, radiation shielding, and thermal control. Some conventional components such as batteries and individual solar cells will still be required, but the total number of parts and assembly time will be drastically reduced. The spacecraft, as shown in figure 4, is essentially a multi-ASIM module.

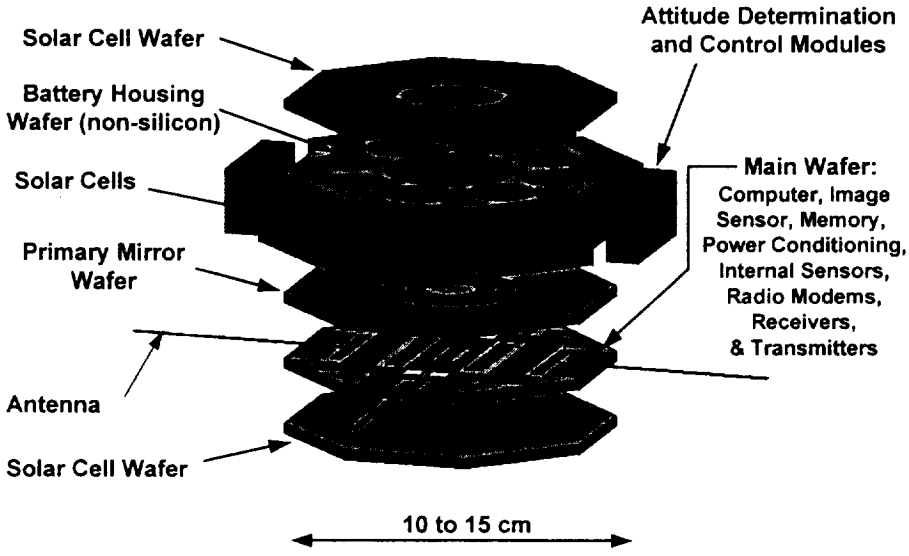

Figure 4. A hypothetical silicon satellite.

Silicon wafers are routinely produced with diameters up to 20 cm which will increase to 30 cm within a decade. Low-volume (10 to 1000 wafers) production of custom circuits and MEMS uses wafers with diameters less than 15 cm. Simple ASIM-based integrated satellites will have dimensions of 10 to

20 cm while more complex configurations using additional non-silicon mechanical structure (i.e. truss beams, honeycomb panels and inflatable structures) will be much larger.

The benefits of batch-fabricated silicon satellites are:

1. Reduced parts count due to integrated electronics, sensors, and actuators on a single substrate,
2. The ability to add redundancy and integrated diagnostics without significantly impacting production cost,
3. Decreased material variability and increased reliability due to rigid process control,
4. Rapid prototype production capability using electronic circuit, sensor, and MEMS design libraries with existing (and future) CAD/CAM tools and semiconductor foundries,
5. Elimination of labor-intensive assembly steps (welding, wiring cable harnesses, etc.)
6. Automated testing of systems and subsystems, and
7. Paper less documentation of designs, fabrication processes, and testing.

Low cost per function is a direct result of the fabrication process; semiconductor batch fabrication techniques evolved within the constraints of consumer-driven market economics. Low mass and volume are simply byproducts of the fabrication process that can be exploited for space applications.

II.B. Satellite Classification

The term "microsatellite" has traditionally been used for satellites with masses between about 100 kg and 10 kg. Recently, the terms "nanosatellite" and "picosatellite" have been used almost interchangeably for 1 kg class vehicles. In an attempt to standardize these names and still keep within the spirit of the prefixes "micro", "nano", etc., I propose a new classification scheme given in table 6.

Table 6. Satellite classification by mass

Classification	Mass Range
Microsatellite	1 kg to 100 kg
Nanosatellite	1 gram to 1 kg
Picosatellite	1 milligram to 1 gram
Femtosatellite	1 microgram to 1 milligram

II.C. Power Considerations

How much solar power can small satellites produce? Assuming that all of the available surface area is covered by solar cells, the extremes occur for a cubic satellite and for a satellite spread out into a ~10 micron-thick sheet; i.e. a flat all-solar-array satellite. Figure 5 shows the power extremes for 20% solar conversion efficiency, random pointing for a cubic satellite, and optimum pointing for a thin sheet satellite with average density equal to silicon. Picosatellites through microsatellites can produce power levels in the 1 to 100 Watt range while femtosatellites are in the microwatt to milliwatt range.

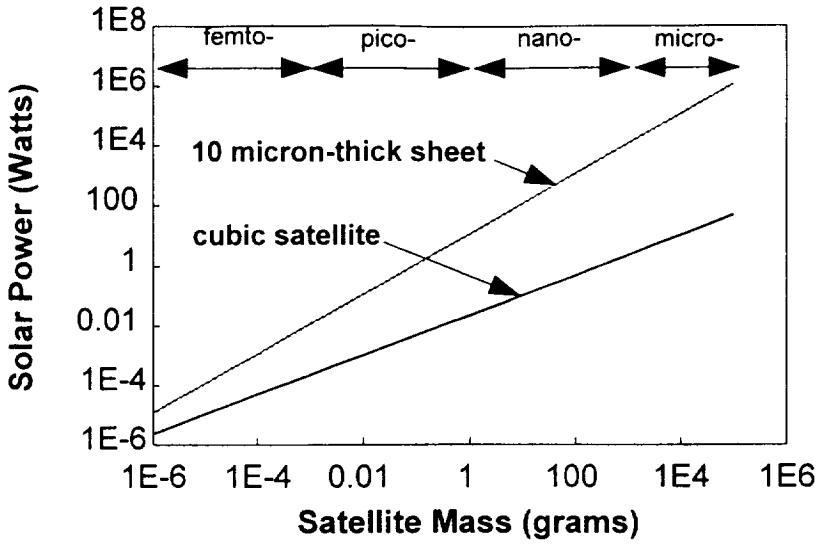

Figure 5. Solar power output ranges, in full on-orbit sunlight, for satellites with an average density equal to silicon and 20% power conversion efficiency over all exterior surfaces.

II.D. Thermal Considerations

The overall thermal balance of a spacecraft is determined by its orbit, its geometry, its surface properties, and its internal design. Solar flux (~1370 W/m^2) has an effective blackbody temperature of 5800 K. The Earth reflects ~30% of this incoming solar radiation back to space; the average reflectance or albedo ranges from 23% at the equator to 74% over Antarctica.[29] Over 95% of direct and reflected solar energy is carried by photons with wavelengths between 0.2 and 2.5 microns. Thermal radiation from the Earth has an effective blackbody temperature of ~300 K which has 98% of the energy carried by photons with wavelengths greater than 5 microns. The primary energy input to a satellite, averaged over an orbit, is direct and reflected solar radiation while the primary energy outflow is infrared emission from the spacecraft at wavelengths greater than 5 microns. The average emissivity (or absorptivity) α in the visible and near infrared wavelength range (0.4 to 2 microns) controls the major heat input to spacecraft surfaces while emissivity ε in the medium to long infrared wavelength range (5 to 50 microns) controls the heat rejection capability of spacecraft surfaces.

At thermal equilibrium, the heat radiated by a satellite to space is just the sum of the energy absorbed plus heat generated internally:

$$\alpha A_s G_s + \alpha A_e G_r + \varepsilon A_e G_e + Q = \varepsilon \sigma T^4 A_r \qquad (1)$$

where A_s is the surface area for absorption of solar energy, A_e is the surface area for absorption of solar energy reflected by the Earth, G_r is the local flux of sunlight reflected from the Earth, G_e is the local flux of thermal energy radiated by the Earth, Q is the internal heat generation rate, σ is the Stefan-Boltzmann constant (5.67 x 10^{-16} W/(m^2*T^4), T is temperature, and A_r is the surface area for heat radiation. As spacecraft shrink in size, surface-area-to-volume ratios and hence surface-area-to-mass ratios increase. Small satellites with body-mounted solar arrays can have power-to-mass ratios equivalent to large satellites with deployable solar arrays, yet still be power-limited. High fractional surface coverage for

solar cells is generally the rule, which results in spacecraft whose thermal balance is determined by solar cell absorptivity and emissivity. This does not allow much latitude in controlling spacecraft temperature ranges for small satellites.

Consider thermal control of a 10 cm diameter, 1.2-kg mass spherical silicon microsatellite at an altitude of 700 km. The IR flux from the Earth G_e is ~200 W/m^2 over the entire orbit and the reflected solar flux G_r is ~260 W/m^2 over about half the orbit. If we assume that the surface is completely covered by 20% efficient solar cells, the orbit average electric power is ~1.5 Watts. With an absorptivity of 0.8 and an emissivity of 0.83, the maximum equilibrium temperature (full sunlight + reflected sunlight + Earth IR + internal heat generation) from eq. (1) is 306 K while the minimum equilibrium temperature (Earth IR + internal heat generation) is 209 K. Conventional spacecraft electronics and batteries cannot tolerate these temperature extremes. Fortunately, the satellite's thermal mass and appropriate insulation techniques can be used to control temperature fluctuations for key spacecraft systems.

Figure 6 shows spacecraft temperature, as a function of time, for 4-cm-diameter, 10-cm-diameter, and 20-cm-diameter solid silicon spheres (nanosatellites and microsatellites) fully covered by solar cells. Their masses are 80 grams, 1.2 kg, and 9.8 kg, respectively. The orbit is a 700 km altitude circular equatorial orbit (0° inclination) and the solar cells have the same efficiency, emissivity, and absorptivity used in the previous equilibrium temperature calculations. The dynamic spacecraft temperature is calculated in one-minute time intervals by numerically integrating a lumped-heat-capacity energy equation:

$$\alpha A_s G_s + \alpha A_e G_r + \varepsilon A_e G_e + Q - \varepsilon\sigma T^4 A_r = \frac{d}{dt}\left(mc_p T\right) \qquad (2)$$

where d/dt is the first time derivative, m is the spacecraft mass, and c_p is the constant-pressure heat capacity of silicon (736 joules/kg*K). As diameter increases, mass and thermal capacity increase, which results in reduced temperature swings over an orbit.

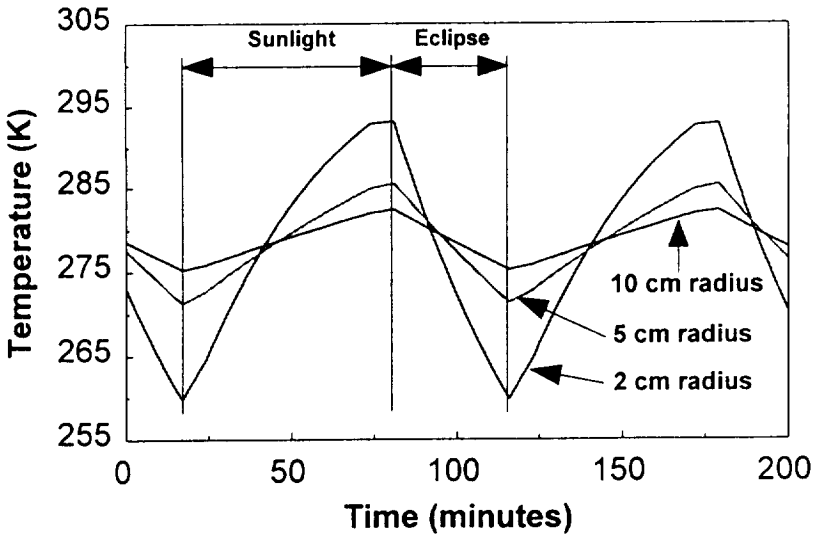

Figure 6: Spacecraft temperature as a function of time for a solid spherical silicon spacecraft covered completely by solar cells with absorptivity of 0.8 and emissivity of 0.83. These temperatures were calculated using a lumped heat-capacity model assuming a circular orbit at an altitude of 700 km.

Figure 6 indicates that passive thermal control is possible for nearly spherical nanosatellites and microsatellites. When dimensions drop below 2 cm, the temperature extremes exceed typical electronics and battery limits. Femtosatellites, with their extremely low mass, can reach the equilibrium sunlight (or eclipse) temperature within minutes.

II.E. Orbit Lifetime Considerations

The Earth's atmosphere effects spacecraft motion even at altitudes beyond 1000 km. The main effects are atomic oxygen erosion and orbital decay due to atmospheric drag. The drag force F_D on a satellite is given by

$$F_D = \frac{1}{2}\rho V^2 S C_D \tag{3}$$

where ρ is the local atmospheric density, V is the satellite velocity, S is effective cross-sectional area of the spacecraft, and C_D is the satellite drag coefficient (C_D~2 for most satellites). Orbit decay rates are often parameterized by introducing the ballistic coefficient W, defined as the satellite mass M divided by the cross-sectional area S times the drag coefficient C_D. A spherical solid silicon satellite with a diameter of 10 cm would have a ballistic coefficient of ~150 kg/m^2. Figure 7 shows the maximum ballistic coefficient as a function of mass for a cubical satellite and a 10-micron-thick sheet satellite. Note how the ballistic coefficient is constant (and extremely small!) for the thin sheet satellite while it is a function of mass for a cubic satellite.

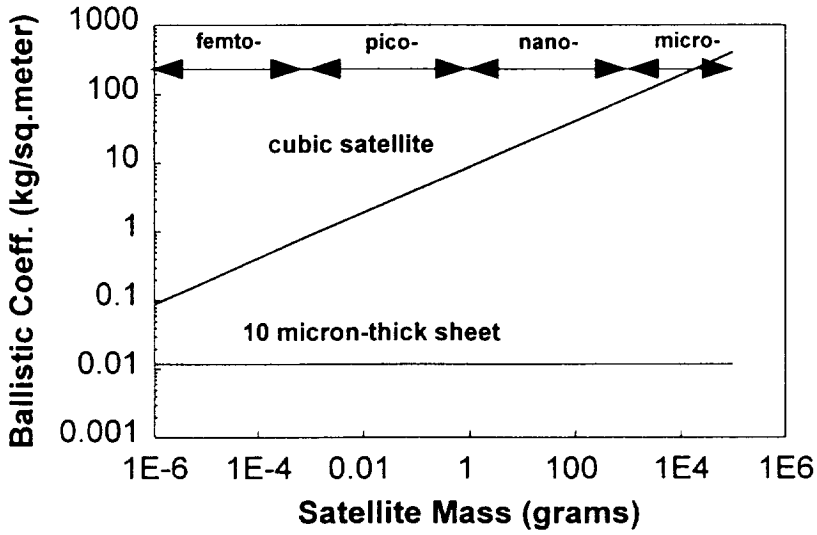

Figure 7. Maximum ballistic coefficient as a function of mass for solid silicon satellites.

Figure 8 shows calculated orbital decay rates as a function of ballistic coefficient and altitude for worst-case solar-maximum conditions (4 to 6 years from now). Currently, we are in solar-minimum conditions, which produces decay rates about an order-of-magnitude lower at 300 km altitude and about 3 orders-of-magnitude lower at 700 km altitude. For satellites with ballistic coefficients of ~100 kg/m^2, note that at 700 km altitude the solar-maximum orbit decay rate is only ~10 km per year, while at 500 km altitude the decay rate is high enough to produce an orbital lifetime of only ~1 1/2 years. Roughly spherical (or cubical) picosatellites will have worst-case orbit decay rates of 100 to 1000 km per year even at an altitude of 700 km. For a 500 km altitude, orbit lifetimes would be from a few days to a few months. If orbit altitudes below 500 km and/or mission lifetimes of

greater than a few years are required, drag make-up propulsion for femtosatellites and picosatellites will be mandatory.

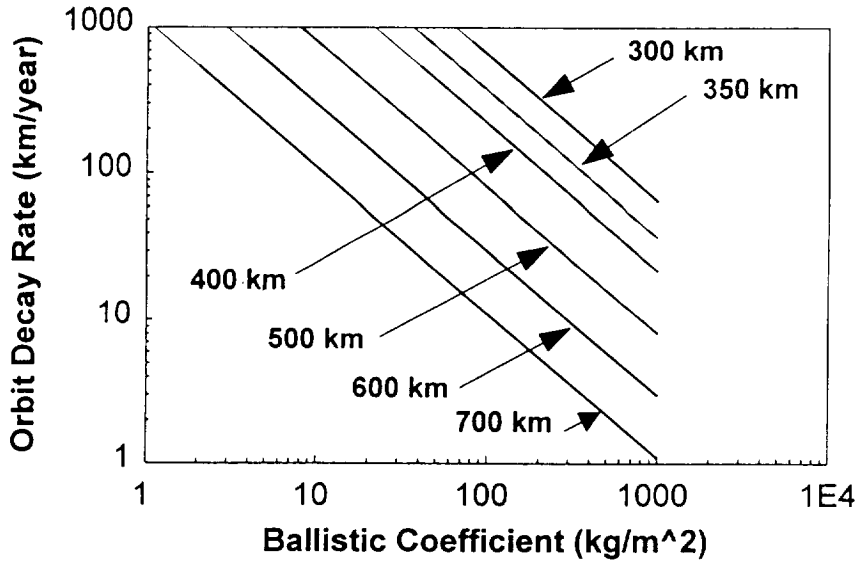

Fig. 8. Orbit decay rates as a function of ballistic coefficient and altitude for circular orbits under very active solar conditions.

III. Conclusions

III.A. Femtosatellites and Picosatellites

Femtosatellites don't have enough radiation shielding or a high enough ballistic coefficient to survive more than a week on-orbit. At altitudes below 500 km where radiation shielding (0.38 mm maximum for a 1 milligram cubic femtosatellite) may be adequate for radiation-hardened electronics, the high ballistic coefficient limits lifetimes to a few days. At higher altitudes, rapidly increasing radiation levels also limit lifetime to a few days. Femtosatellites should be nearly spherical in shape to minimize air drag and maximize radiation shielding. Maximum power generation levels will therefore be in the sub-milliwatt range. Active femtosatellites are an extremely difficult challenge due to their low thermal mass and wild temperature swings.

Picosatellites are the smallest useful satellites, but active thermal control will be required. A thermally passive picosatellite will have temperature swings of 90 K between sunlight and eclipse in low Earth orbit. Cubic picosatellites can have as much as 0.18 cm silicon radiation shielding and a ballistic coefficient of ~9 kg/m^2. Orbit lifetimes can be several years at 700 km altitude under solar-maximum conditions and several years at 500 km under solar-minimum conditions. Nearly spherical satellites are needed to provide radiation shielding, and if low-inclination orbits are used (below 700 km altitude), radiation-soft CMOS electronics may be feasible. Power outputs will be in the 10's of milliwatts range. Picosatellites may be good for disposable or short-duration (i.e. 1-week) missions.

III.B. Nanosatellites

Nanosatellites are the smallest satellites that don't require active thermal control. Silicon radiation shielding thicknesses greater than 1 cm are possible with power outputs in the Watt range. Nearly spherical nanosatellites can operate for several years at altitudes below 500 km in LEO due to their modest ballistic coefficients, and in GEO due to increased radiation shielding. Flattened nanosatellites, i.e. 2 cm thick disks, can produce several Watts of solar power and still retain good thermal control, radiation shielding, and modest ballistic coefficient.

III.B. Microsatellites

Microsatellites have the best power, radiation shielding, orbit lifetime, and thermal characteristics. Flattened silicon microsatellites offer mission lifetimes of years or decades with power levels of 10 to 100 Watts.

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