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HIGH DENSITY MEMORY BASED ON QUANTUM DEVICE TECHNOLOGY

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ABSTRACT

We explore the feasibility of ultra-high density memory based on quantum devices. Starting from overall constraints on chip area, power consumption, access speed, noise margin, we deduce boundaries on single cell parameters such as required operating voltage and standby current. Next, the possible role of quantum devices is examined. Since the most mature quantum device, the resonant-tunneling diode (RTD), can easily be integrated vertically, it naturally leads to the issue of 3D integrated memory. We propose a novel method of addressing vertically integrated bistable two-terminal devices, such as resonant-tunneling diodes (RTDs) and Esaki diodes, that avoids individual physical contacts. The new concept has been demonstrated experimentally in memory cells of FETs and stacked RTDs.

1 Introduction

Progress in computer memory design has largely been evolutionary instead of revolutionary, because of the large number of constraints involved.[1] For 64 Gbit DRAM using planar technology the projected minimum feature size is 0.07 μm and a first shipment date of 2010.[2] To do better than this, it will be necessary to consider new approaches such as using quantum effect devices and 3D integration.

Memory is unique among computer building blocks in the sense that the basic memory cell does not necessarily require the use of transistors. Cells consisting of only resonant-tunneling diodes (RTDs) and single tunnel barrier diodes have already been demonstrated.[3] However, since a complementary "quantum device" logic does not presently exist (there is no fast pull-up device), surrounding logic should use CMOS technology to satisfy low power constraints.

In what follows, we concentrate on the basic memory cell and consider the application of tunneling-based devices to memory. Our experimental results have been obtained with III/V material RTDs, but the same ideas apply to Esaki diodes (and any other two-terminal bistable device), opening up a wide range of possible material systems, including Silicon.

2 Constraints

We separate constraints on a conceptually new memory system into four groups: area, power, speed, and noise margin. From these we infer limits on the design options.

The area constraint comes from considerations of wiring delays and yield problems. The 0.07 μm design rule of 2010, results in a 64 Gbit chip area of about 12.5 cm^2. For a 1 terabit chip the corresponding area would be around 200 cm^2, making it unwieldy. Achieving higher bit densities is possible using a 3D memory architecture where bit cells are stacked vertically on chip. However, full 3D processing, where each bit cell is physically contacted, must be avoided to minimize wiring complexity.[4] If we assume fabrication by epitaxy and standard processing, without regrowth steps, it follows that the basic memory cells must be vertically stacked two-terminal devices. We thus have the following logical chain:

3D => no wires to each device => stacked two-terminal devices.

Thus far, the planar (2D) approach has worked well enough that a solution of this 3D "wireless" addressing problem has not been required.

Power dissipation of large memories is entirely dominated by standby power, i.e. the additional energy expended during writing to or reading from the memory is negligible. The power per bit cell is given by the expression:

$$P = V_{cell} I_{st} , \qquad (1)$$

where V_{cell} is the (average) voltage drop over one bit cell and I_{st} is the standby current through the cell. Let C be the capacitance that is charged/discharged when the bistable cell switches between its two states

and let I_{sw} be the average current available from the cell during switching. Then a rough estimate for the switching time, t, of the cell is given by:

$$t\, I_{sw} = V_{cell}\, C = \text{charge moved during switching.} \tag{2}$$

Combining Eqs. (1, 2):

$$P\, t = C\, V_{cell}^2\, I_{st}/I_{sw} \ , \tag{3}$$

which is the "static power switching delay product" per bit cell.

It is clear from Eq. (3) that, for given C, V_{cell}, and I_{sw}/I_{st} ratio, standby power and switching speed can be traded off against each other. If we specialize to a bi-stable current device, such as an RTD or Esaki diode, then we can associate I_{sw}/I_{st} with the peak-to-valley current ratio (PVR),[5] and take C about 4 fF/μm^2 x A, where A is the device area (assuming about 250 Å separation between the cathode/anode charges). This leads to a single equation relating power, speed, and cell area with the voltage drop over the cell and PVR:

$$P\, t / A = 4{\cdot}10^{-15}\, V_{cell}^2 / \mathrm{PVR}\ . \tag{4}$$

A is the conducting cell area in μm^2. Figure 1 shows power per cell versus cell switching time for various values of V_{cell} and A and a conservative PVR of 20.

We did not include in C of Eq. (3) the data line capacitance. This capacitance may be larger than the device capacitance by orders of magnitude (few 100 fF versus < 1 fF). If an extremely high PVR (10^4) can be achieved for some two-terminal device, it may be possible to drive this capacitance directly with the cell switching current. However, just as is expected for future generations of DRAM cells,[6,7] a gain stage at the cell will likely be needed.

In addition to some of the noise sources present in high-density DRAMs,[1,8] we have to consider the probability of resetting a device with two current minima separated by a voltage DV. For thermal noise we find:

$$V_{noise} = (kT/C)^{1/2} = 2\, A^{-1/2}\ (\text{in mV})\ , \tag{5}$$

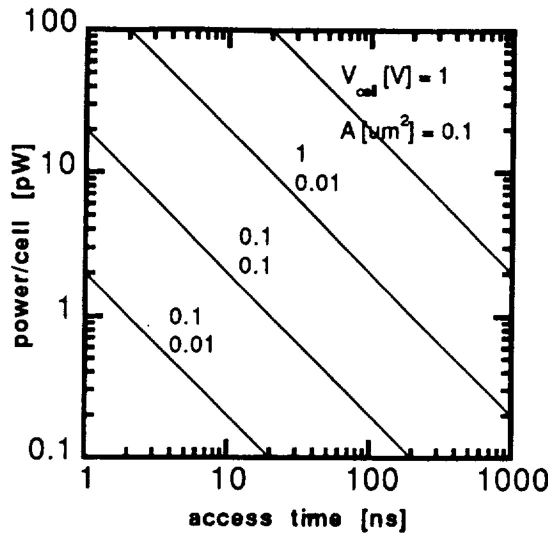

Figure 1. Static power dissipation vs. access speed for various memory cell voltages and cross sectional areas.

(room temperature) and for shot noise induced current fluctuations:

$$I_{shot} = (2eI_{st}B)^{1/2} = 0.06\ A^{-1/2}\ I_{st}\ , \tag{6}$$

where B is the noise frequency bandwidth. The effects of each of these sources is negligible as long as $A \geq 0.01\ \mu m^2$ and $\Delta V \geq 0.1$ V, consistent with earlier analyses.[9]

3 Design options

Quantum mechanical tunneling is responsible for the nontrivial current-voltage characteristics of both the RTD and the Esaki diode. As pointed out above, a practical 3D integrated memory implies the use of stacked two-terminal devices (although addressing these has been left open for the moment). Another big advantage of using two-terminal devices as bit cells is their potential for very low voltage operation. It is well-known that reduction of the CMOS circuit operating voltage below 1 V poses serious problems because any lowering of the threshold voltage is accompanied by an exponential rise in subthreshold current (at $V_{GS} = 0$ V).[10] However, for RTDs and Esaki diodes, two current minima can occur much closer than 1 V and a separation as low as 0.1 V should be realizable. Although surrounding circuitry would still use standard voltage levels, the product of cell power and access time decreases by a factor 100 if the cell voltage drops from 1 to 0.1 V.

Let us assume then that $V_{cell} = 0.1$ V, $A = 0.01\ \mu m^2$ and PVR = 20 in Eq. (4). This yields:

$$P\,[\mathrm{pW/cell}]\ \tau[\mathrm{ns}] = 20 \tag{7}$$

This equation shows that a terabit memory would be feasible with total power in the 1 W range and access times below 100 ns.

If the power per bit cell is indeed 1 pW, then it follows from Eq. (1) that the standby current density should be about 0.1 A/cm^2. If using bistable diodes, their valley current density will have to be of the same order of magnitude (or below). These numbers are about 4 orders of magnitude lower than standard values. Figure 2 shows the I-V characteristic of an ultra-low current RTD that we designed and fabricated. The valley current density is 1 A/cm^2 and the PVR is about 7. There is no fundamental problem to lower this current density even further and we fully expect to improve the PVR with future designs.

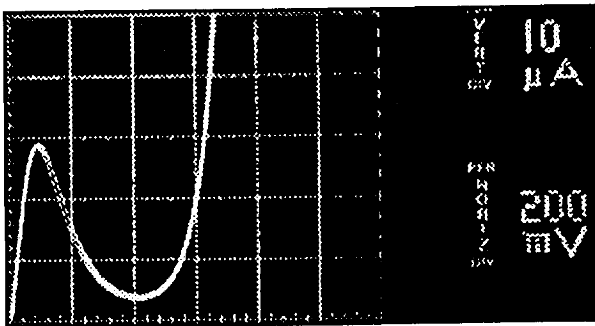

Figure 2. I-V curve of 20x20 mm^2 low-current RTD.

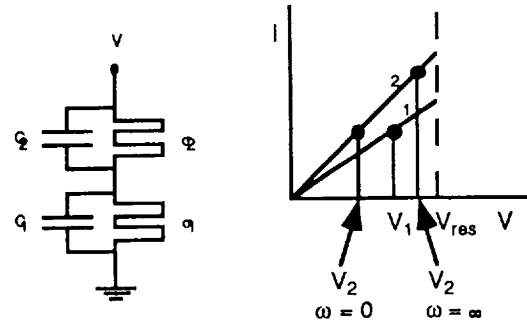

Figure 3. Lumped element model of RTDs and V_2 vs. V_1 relation for low and high frequencies.

4 Slew Rate Addressing

The outstanding issue is now whether it is possible to access bits stored in vertically stacked bi-stable diodes without physically contacting these devices. If a voltage ramp is applied over two RTDs (or Esaki diodes) in series, one RTD will switch prior to the other. This event can be analyzed with a lumped element RTD model[11] taking only intrinsic parallel capacitance into account, as is shown in Fig. 3. Let s_n be the conductance associated with the pre-peak I-V slope and C_n the capacitance of RTD n.

A sinusoidal applied voltage with angular frequency w produces voltages V_1 and V_2 over each RTDs 1 and 2 with a ratio

$$V_1/ V_2 = (s_2 + jw C_2)/ (s_1 + jw C_1) . \tag{8}$$

When the real part of one of these voltages reaches the corresponding RTD peak voltage, a switching event takes place (and the current linear analysis breaks down). Now let the peak currents and capacitances satisfy $I_1 < I_2$ *and* $C_1 > C_2$. Then for low frequencies RTD_1 switches first, while for high frequencies RTD_2 switches first. Another way of understanding this behavior is to think of the parallel RTD capacitance as shunting away current that would otherwise have been available for conduction through the RTD, and that this happens more for RTD_1 than for RTD_2 at higher frequencies.

Figure 4 shows a simulation of this switching order reversal. In this case, the relevant slew rate lies below the intrinsic RTD slew rate, which is just the RTD speed index (I/C). Therefore, when the first switching RTD goes beyond its peak, the voltage over it increases faster than the overall ramp voltage and the voltage over the other RTD must decrease. If the relevant slew rate would lie much above this, both RTDs would "switch" (and one of them would "switch back" if the applied voltage was suddenly held constant).

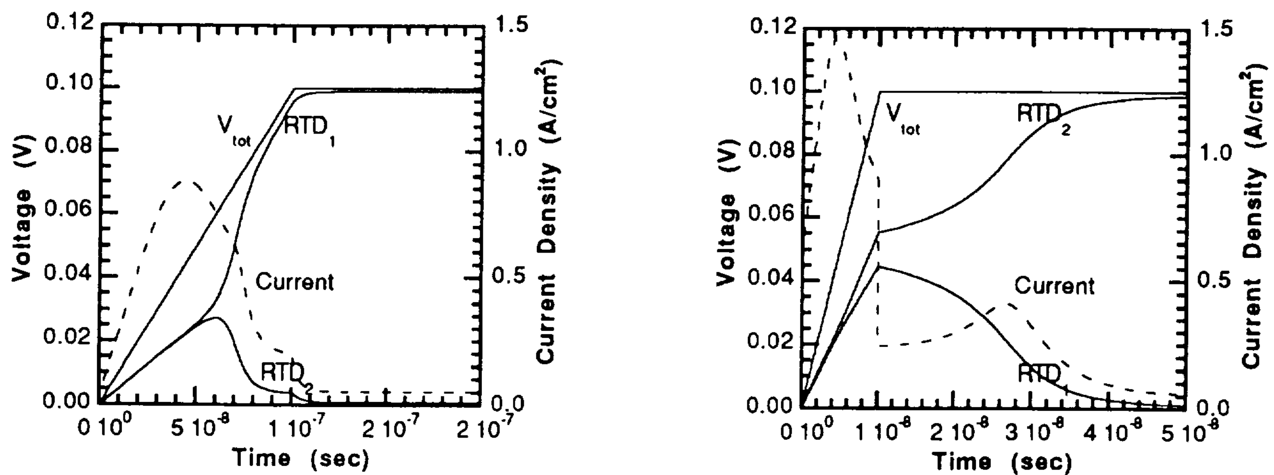

Figure 4. Simulated RTD stack switching under applied voltages with different slew rates. The slew rate is 10x higher on the righthand side (note different time scales).

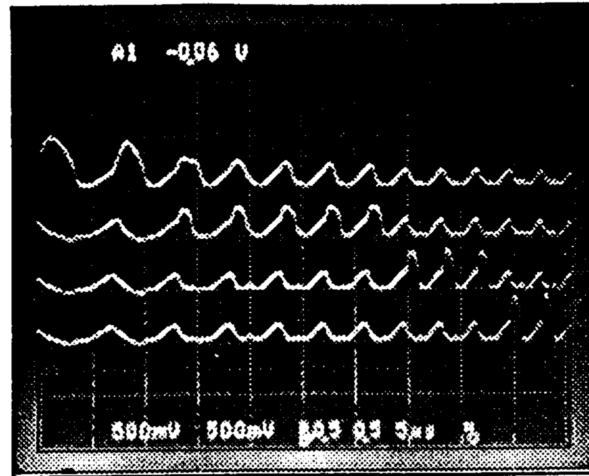

Figure 5. Voltages of four series connected RTDs under an applied frequency sweep from 100 to 340 kHz.

These ideas generalize to multiple RTDs connected in series. Figure 5 shows the voltages over four RTDs connected in series. We used standard high-current RTDs and slowed these down by adding external capacitors, so that slew rate dependent "addressing" of the individual RTDs can be observed in the few hundred kHz range. Peak currents form an ascending and capacitances a descending series as a function of RTD number. Using TI SPICE augmented with RTD models, we have been able to accurately reproduce these experimental results. These results show that by using more information of the applied signal than just its final levels, one can "address" individual stacked RTDs without extra contacts.

Since propagating slew rate information over word lines to a memory cell may pose problems, we have looked at a model stacked memory cell for which the desired slew rates are locally generated from a multiple-valued word line level. The schematic circuit is shown in Figure 6. The pass FET acts as a variable resistor, and together with the capacitances of the RTDs forms an adjustable low frequency filter (the pass capacitor merely provides DC isolation between the top of the RTD stack and the bit line). After the word line voltage "opens" the pass FET to some degree, a positive step voltage step on the bit line generates a corresponding upward ramp on the "storage node," which in turn switches the desired RTD from a low voltage to a high voltage state. SPICE simulations confirm the proper operation of this circuit over full write cycles without unwanted "resets" when the word and bit line return to their original values.

Fig. 7 shows experimental results obtained for the case of two series connected RTDs. As in the case of Fig. 5, external capacitances were added to standard current density RTDs. Word level 1 (- 0.8 V) selects RTD1 (when bit line goes high), while word level 2 (0.0 V) selects RTD2. In order to be able to

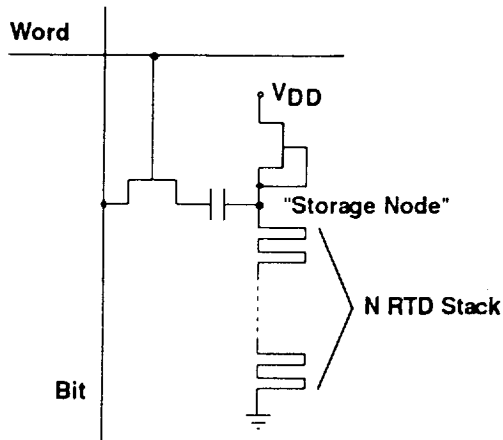

Figure 6. Multiple-valued Word Line Memory Cell.

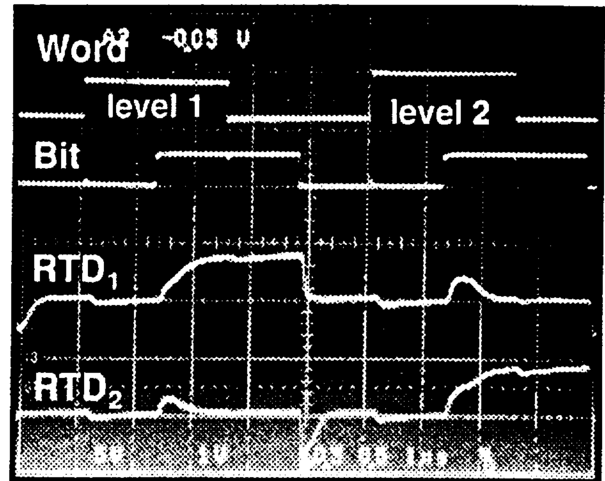

Figure 7. Write Operation for 2 RTD Stack. Vertical: 5, 1, 0.5, and 0.5 V/div, Horizontal: 1 ms/div.

display this process on an oscilloscope, the entire RTD stack was reset at the negative edge of the bit pulse.

The above results were obtained by adding external capacitances to standard RTDs. However, we have also observed the switching order reversal with ultra-low current RTDs *without* any added capacitance, justifying our more convenient testing of the slew rate based addressing concept with externally added capacitances.

Finally, we should remark that reading the data from an RTD stack is more complex than writing to it. We are currently investigating circuit topologies for fast readout of all bits stored in an RTD stack.

5 Conclusion

We have discussed a possible rôle for quantum effect devices in high density memory. Two-terminal bistable diodes, such as the RTD and the Esaki diode, may enable a practical form of 3D integration. However, this would require a “contactless” method of selecting vertically stacked bit cells. We have developed and experimentally verified such a contactless scheme utilizing the slew rate of an addressing signal.

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