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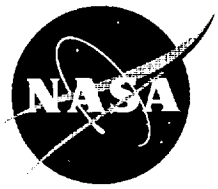
Solid State Radiation Dosimeters for Space and Medical Applications

Martin G. Buehler
Editor

December 9, 1996



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ABSTRACT

This report describes the development of two radiation monitors (RADMONs) for use in detecting total radiation dose and high-energy particles. These radiation detectors are chip-size devices fabricated in 1.2-μm CMOS and have flown in space on both experimental and commercial spacecraft. They have been used to characterize protons and electrons in the Earth's radiation belts, particles from the Sun, and protons used for medical therapy. Having proven useful in a variety of applications, the detector is now being readied for commercialization.

PREFACE

The dosimeters reported on here operate on two principles. The total dose monitors use p-FETs (Field Effect Transistors) whose threshold voltage shifts as radiation-induced charge is trapped in the gate oxide. The p-FETs have the unique feature that they only need to be powered at the time of measurement and not during exposure to radiation. Since the dosimeter is generally measured infrequently, these dosimeters require low average power. The particle detectors use a special SRAM (Static Random Access Memory) that flips state in response to a high energy particle that strikes a powered memory cell. Because this detector is a modified SRAM, the power requirement is minimal.

The radiation detector effort was started in the Product Assurance Technology Program at JPL in the 80's. During the past seven years, these papers and reports were generated by workers at JPL and associated institutions. The first radiation detector was developed in 1984 and delivered to the Combined Release and Radiation Effects Satellite (CRRES) in 1985. The launch of the CRRES was delayed until 1990 due to the Shuttle Challenger accident. Since then, dosimeters have been delivered for use on MSX, the Clementine spacecraft, the Clementine booster, STRV-1b, Telstar, SAMMES-1, Intelsat, and STRV-2. These spacecraft are both experimental and communication satellites. All orbit the Earth except for the Clementine spacecraft which circled the Moon and now is in heliocentric orbit. In addition to space applications, dosimeters have been used to characterize the proton beam at the Loma Linda University Proton Therapy Facility.

Currently, the dosimeter development is aimed at commercialization. The surrounding electrons are being placed in the same package as the dosimeters in order to provide a digital interface between the sensor and the micro-controller. This will greatly facilitate their use by eliminating the need to design the analog circuitry on a separate board. In addition, it will allow multiple dosimeters to be placed throughout the spacecraft to map the radiation field around the Earth and within the spacecraft.

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ALPHA-PARTICLE SENSITIVE TEST SRAMs

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Abstract

A bench-level test is being developed to evaluate memory-cell upsets in a test SRAM designed with a cell offset voltage. This offset voltage controls the critical charge needed to upset the cell. The effect was demonstrated using a specially designed 2-μm n-well CMOS 4k-bit test SRAM and a Po-208 5.1-MeV 0.61-LET alpha-particle source.

I. Introduction

The characterization of SRAMs due to ion induced upsets is essential to evaluating the susceptibility of SRAMs and ASIC registers to Cosmic Ray upsets [1]. This characterization usually requires evaluations at a heavy ion source such as a cyclotron. Such evaluations are time consuming and expensive. In recent years laser pulses have been proposed as substitutes for the heavy ion sources. However the laser simulations are limited by metal layers that frequently block the laser pulses from SEU-sensitive nodes and by the complexity of the ion-photon calibrations [2] [3].

In order to overcome these difficulties, six-transistor cell SRAMs were designed to be easily upset by a laboratory ion source. This simulation closely emulates the Cosmic Ray upset of SRAMs. The test SRAM (SEU chip) as shown in Figure 1 is a 4k-bit device. In the experiments, a Polonium 208 alpha-particle source was used to upset the SEU chip. The cells of the SEU chip were designed with an offset voltage which controls the critical charge needed to upset the cells. The purpose of this paper is to explore the potential for using test structures to quickly and inexpensively characterize the SEU sensitivity of an integrated circuit family. In the next phase of this development, the SEU chip's upset rate will be characterized by heavier ions. The purpose is to explore the possibility of extrapolating the alpha particle results to results obtained by heavier ions. Next, this approach will be extended to study the upset of latches designed from standard cells. Finally, the methodology will be included as a part of an integrated circuit qualification procedure for custom ICs.

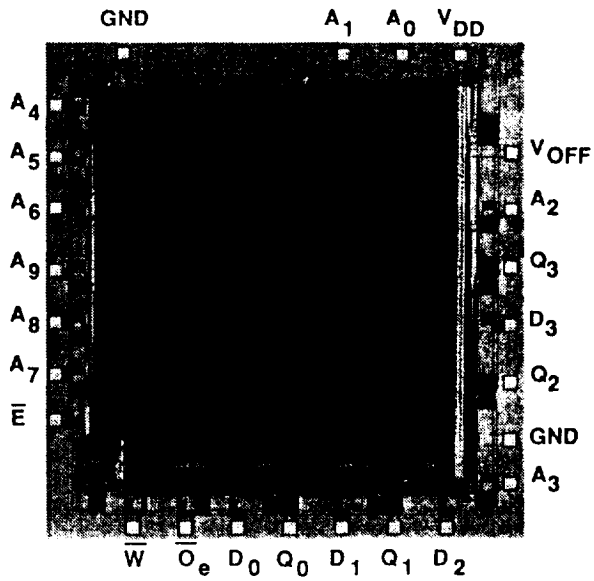

Figure 1: The 4k-bit SEU chip designed to be upset by alpha particles. This chip, designed for a 2-μm CMOS n-well process, is 3.84 mm by 4.05 mm and fits in a 28-pin dual-in-line package. The substrate doping is $7.0 \pm 1.5 \times 10^{11} cm^{-3}$.

II. SRAM Design

A schematic diagram of the SRAM cell used in these experiments is shown in Figure 2. The pulsed current source is used to model the alpha particle strike. The offset volt-age, V_{OFF} is varied to alter the critical charge required to upset the cell. The cells are always biased so that V1-node is low and the V2-node is high. This means that the drain diodes Dp1 and Dp2 are reverse biased and susceptible to upsets by heavy ions. Since Mpw is "on" the V2-node, voltage is equal to V_{OFF}, which was varied from V_{DD} = 5V to 1.9 V.

In order to emphasize ion hits on the Dn2-diode, its area was enlarged to 117 μm^2; whereas, the Dp1-diode was designed with a minimum area of 22 μm^2. The layout of

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the cell is shown in Figure 3 and its critical dimensions are listed in Table 1. The dimensions of the MOSFETs were chosen so that the cell can be operated as a "standard" SRAM when $V_{OFF} = V_{DD}$.

In order to minimize power line noise, the V_{DD}, GND, and V_{OFF} lines were made as wide as possible. This reduces the possibility that one cell will trip another cell from the current transient demanded by the flipping cell.

Table 1: Dimensions of the transistors and drains in the memory cell.

DEVICE	L(μm)	W(μm)	Ad(μm^2)
Mn1	2	3	28
Mn2	2	4	117
Mp1	4	3	22
Mp2	4	3	19

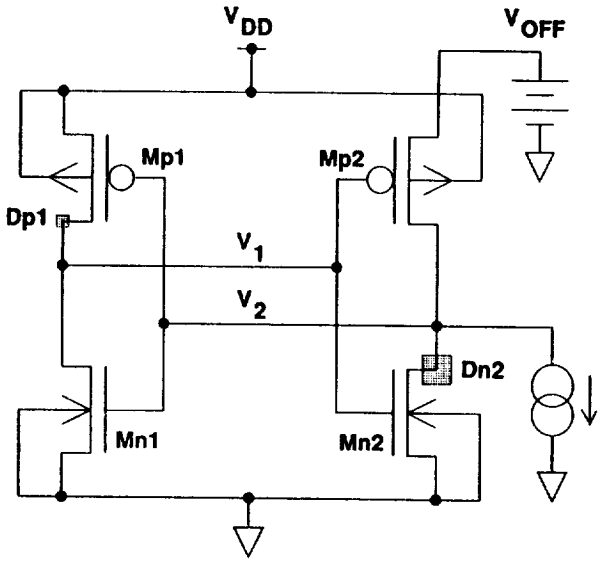

Figure 2: Memory cell schematic diagram showing the placement of V_{OFF} and the bloated n-drain, Dn2. The dimensions of the transistors and drains are listed in Table 1.

III. SPICE Analysis

The principle of operation of the cell is illustrated by the transfer curves shown in Figure 4. When the cell is biased with V_{OFF} above 1.9 V, the cell exhibits two stable states. For V_{OFF} less than 1.9 V, the cell has only one stable state. As the critical V_{OFF} is approached, cells begin to flip according to the distribution in cell parameters. The voltage span for this spontaneous flipping action is about 30 mV for the cells in the SEU chips studied here.

The critical charge, Q_c, was determined for this circuit using SPICE and MOSIS supplied parameters. The V1-node and V2-node capacitances were modeled by fixed metal and polysilicon interconnect capacitances and by the drain depletion capacitances given by their areas and peripheries and by the SPICE LEVEL 2 junction capacitance parameters. A current generator was placed on the V2-node as shown in Figure 2 and a triangle pulse with a 1:19 rise:fall shape was used to upset the cell. For a given pulse height, transient simulations were evaluated up to 100 ns where the response was compared to $V_{DD}/2$ to determine if the cell had flipped. The pulse height was adjusted using the binary search algorithm until the difference in charge (area under the pulse) between successive simulations differed by less than 0.1 fC. The resulting critical charge Q_c versus V_{OFF} is shown in Figure 5. The results were invariant with current pulse widths between 20 ps and 500 ps. For pulse widths (PWs) in excess of 500 ps, critical charge curves deviated from the 500 ps curve. The deviation of the PW = 2 ns curve from the PW < 500 ps curve is shown in Figure 5. Thus, the cell time constant exceeds 500 ps. Since the alpha particle pulse width is about 200 ps [4], the response of this circuit exceeds the alpha particle pulse. As determined from this analysis, the details of the pulse shape is unimportant which simplifies the analysis.

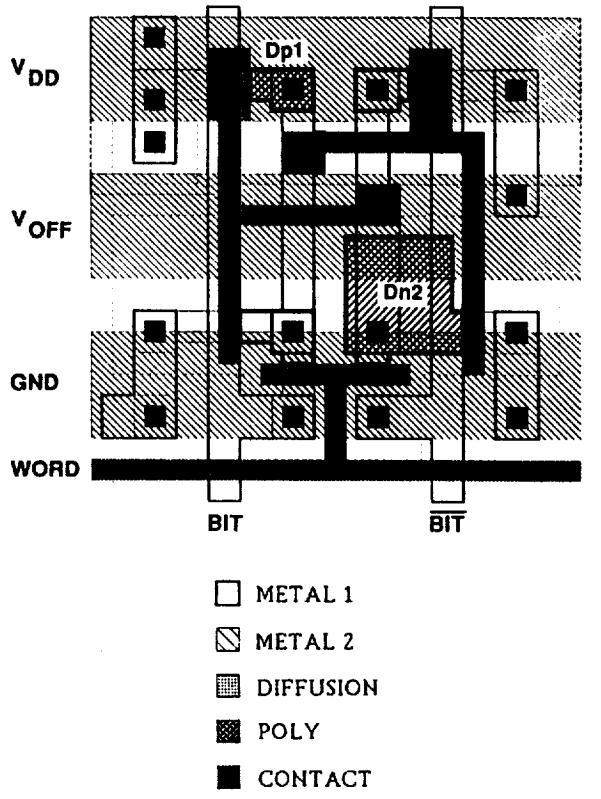

Figure 3: Memory cell layout, designed for 2-μm CMOS n-well process, is 42.0 μm by 45.0 μm. The alpha sensitive region is the bloated n-drain in the p-substrate. The offset voltage, V_{OFF}, is used to enhance its upsetability.

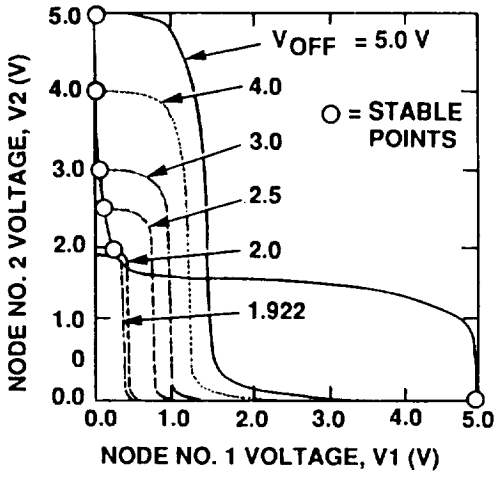

Figure 4: Memory cell transfer curves showing the effect of V_{OFF} on the stable points.

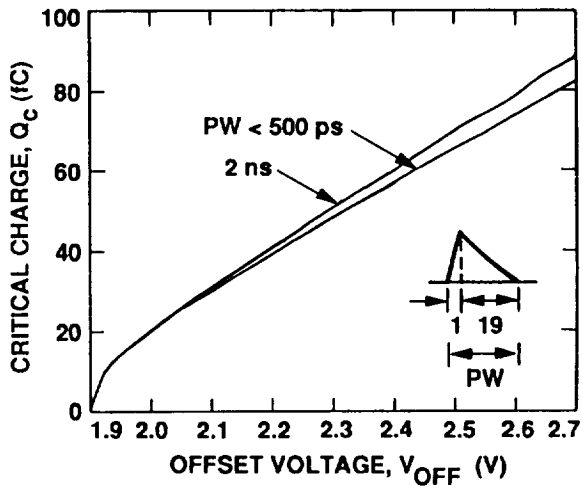

Figure 5: Memory cell SPICE analysis for the critical charge.

IV. Alpha Particle Behavior in Silicon

The energy loss of an alpha particle passing through Silicon is shown in Figure 6 [5]. This figure shows that a 5 MeV alpha particle has a range of 23.7 μm. The differential of the energy curve leads to the Linear Energy, LET, curve shown in Figure 7. This shows that as the particle penetrates the Silicon its LET increases up to the Bragg peak and than falls to zero. The integral of the LET curve leads to the silicon deposited charge, Q_s, curve shown in Figure 8. This curve is based on the electron-hole pair production rate of 3.6 eV/e-h pair. The charge deposition curve shown in Figure 8 indicates that a 5-MeV alpha particle can deposit about 225 fC in Silicon assuming no over layers. This amount of charge is about 10 times larger than the charge needed to upset the cell as shown by the SPICE analysis presented in Figure 5. Thus it should be anticipated that the enlarged diode, Dn2, will be upset by alpha hits that strike a considerable distance from the diode. In a later section the lateral hit distance was determined to be 6.2 μm.

V. Experimental Results

In the following experiments a 1 μCi Po-208 alpha particle emitter was used. This source was placed 32.5 mm above the SRAM cell. This distance is very close to the range of alphas in air of 35.2 mm. The cell and the source were placed in a vacuum chamber. The flux at the SRAM cell, measured with a pin diode, was 214 alphas/cm^2 · sec. The partial vacuum pressures were measured using a Wallace & Tiernan FA 112 pressure gauge. The offset voltage was applied for a duration that allowed 1 to 30 upsets to occur, and this measurement was repeated 30 times and averaged to give results with deviations less than 18 percent for data

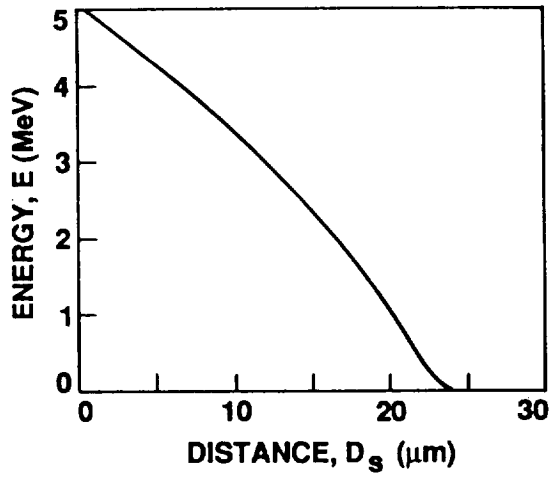

Figure 6: Energy profile of a 5-MeV alpha particle in silicon with a range of 23.7 μm.

larger than 0.01 counts/sec and 6 percent for data larger than 0.2 counts/sec. For this experiment the "on" time for the offset voltage varied from 1 to 60 seconds.

The response of the cell follows the detector equation where it is assumed that all the memory cells are initially placed in the same state:

$$\frac{dN}{dt} = \phi\sigma(N_t - N) \qquad (1)$$

where N is the number of flipped cells at time t, N_t = 4096 is the total number of cells in the SRAM, ϕ is the alpha particle flux, and σ is the cell cross section. The cross section is determined from the initial slope for N approaching zero:

$$\sigma = \frac{1}{\phi N_t}\frac{dN}{dt}\bigg|_0 \qquad (2)$$

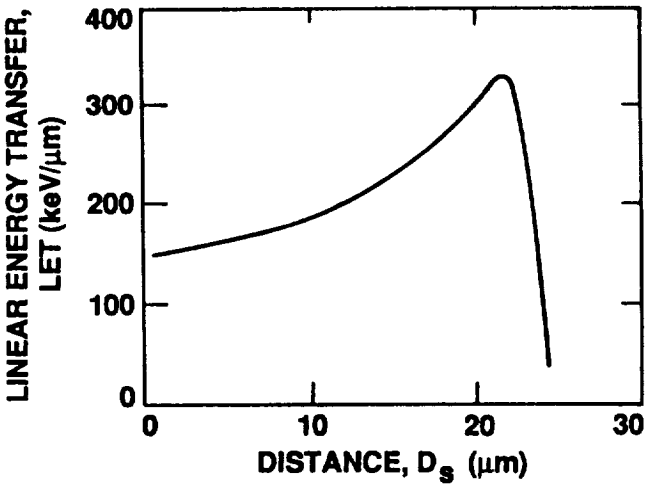

Figure 7: Linear energy profile of a 5-MeV alpha particle in silicon.

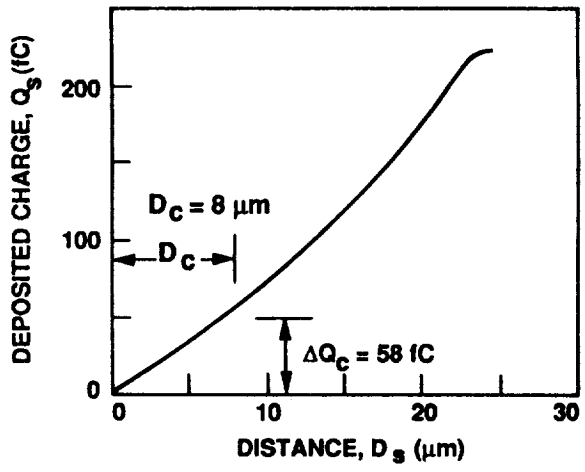

Figure 8: Deposited charge profile of a 5-MeV alpha particle in silicon.

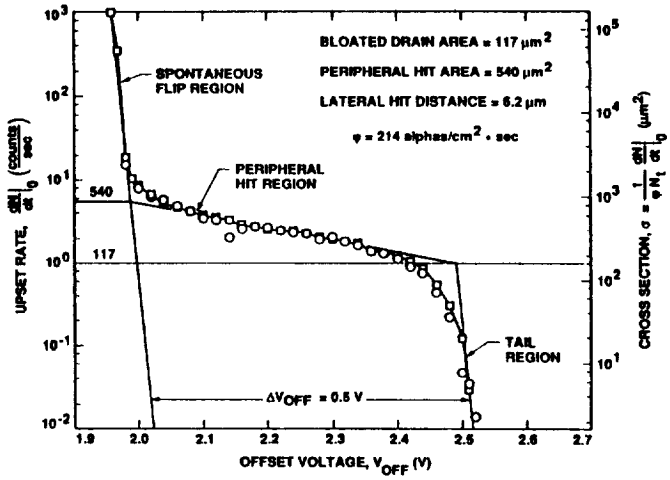

Figure 9: SEU chip upset rate characteristics induced by Po-208 alpha particles 32.5 mm above the SRAM in a vacuum. The cross section observed by extrapolating the peripheral hit and tail regions agrees with the designed cross section of 117 μm^2. Repeatability of the measurements is demonstrated by the overlap of the data taken from 1.9 to 2.7 V (squares) and data taken from 2.7 to 1.9 V (circles).

VI. Vacuum Test Results

The response of the SRAM is shown in Figure 9 for alpha particle irradiation in a vacuum. Three regions are apparent in the figure. Region I, the spontaneous region, is governed by cell parameter distributions and indicates that the transfer curves, as seen in Figure 4, no longer overlap ($V_{OFF} < 1.922$ V). Region II is termed the peripheral hit region because the cross section exceeds the design cross section of 117 μm^2. For this cell the extent of the peripheral hit area is 540 μm^2. Assuming the bloated drain is a square 117 μm^2 and the peripheral hit region is a square 540 μm^2, then the lateral hit distance is 6.2 μm. Region III is the tail region; in this region the upset rate falls with a slope that is identical to Region I which indicates that this region is also governed by the spread in cell parameters.

As seen in Figure 9, a change in V_{OFF}, ΔV_{OFF} of 0.5 V is required to bring the cells from the spontaneous flip region where the critical charge, Q_c is zero to a point where the alpha particles are just able to trip the cells (tail region in Figure 9). By aligning the V_{OFF} value in Figure 9 where the spontaneous-flip line intercepts the physical cross-section line (V_{OFF} = 2 V) with the origin of Figure 5 (V_{OFF} = 1.9 V), then ΔV_{OFF} = 0.5 corresponds to V_{OFF} = 2.4 V in Figure 5 and to a critical charge, ΔQ_c = 58fC. This leads to a collection depth, D_c, of 8 μm, as determined from Figure 8. The analysis for D_c depicted in Figure 8 does not include the effect of over layers. The inclusion of over layer in this analysis, requires a detailed knowledge of the thickness and composition of the over layers. Such information is often unavailable. However, an estimate of the effect of over layers on the calculation of

D_c can be obtained by assuming the over layers have the same density as silicon. Using this assumption, the determination uses the curve in Figure 8. The over layers add a few micrometers to the point at which ΔQ_c is applied to the curve. Since the curvature of the curve of Figure 8 is slight, the error in D_c is similarly small.

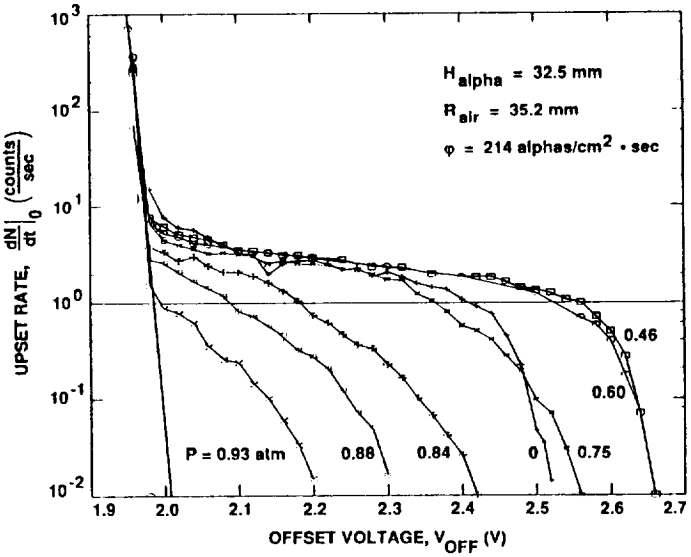

Figure 10: SEU chip upset rate characteristics induced by Po-208 alpha particles 32.5 mm above the SRAM in a partial vacuum. The distortions that appear in the curves for pressures above 0.75 atm are due to the straggle induced by the passage of the alpha particles through air.

VII. Partial Vacuum Test Results

The response of the SRAM, as a function of partial vacuum, is shown in Figure 10. The region II behavior is affected by alpha particle straggle. This behavior is noticeable for pressures in excess of 0.75 atm. This behavior can be explained qualitatively as shown in Figure 11. For P = 0, The alpha particles penetrate 23.7 μm but as determined from the vacuum results, only 8 μm are effective in supplying charge to the junction. As the air is introduced into the chamber, the energy of the alpha particles as they enter the silicon is reduced which reduces the penetration of the alpha particles into the Silicon. For this experiment where the alpha particle source is placed approximately at the range of the alphas in air, the upset rate goes to zero at atmospheric pressure.

The data shown in Figure 10 is analyzed in Figure 12. The V_{OFF} values were determined from the data shown in Figure 10 at an upset rate of 1 count/second. The V_{OFF} values were converted to critical charge using the SPICE results shown in Figure 5. The experimental results are plotted in Figure 12.

A simple model was fitted to the data shown in Figure 12. The model parameters assumed an over layer of 2 μm and a collection depth of 7 μm. For pressures below 0.65 atm the range of the alphas exceeds the collection depth. In this region, the range of the alphas in silicon decreases as the pressure increases because the incident energy of the alphas decreases with increasing pressure. Thus, the alphas deposit more charge in the collection depth as the pressure increases and the critical charge increases with increasing pressure. At the peak in the model curve, the collection depth equals the alpha particle range. For pressures above 0.65 atm, the alpha particle range is less than the collection depth. Thus the deposited charge falls rapidly to zero.

The model used in this analysis does not consider alpha particle straggling. At the end of its range, alpha particle straggling is about 1 μm longitudinally and 1 μm in the transverse direction [6]. A more complete model must take particle straggling into account. However, it is encouraging to see that a simple model provides a qualitative explanation of the data.

A simple theoretical model was fitted to the data assuming an over layer of 2 μm and a collection depth of 7 μm. This model assumes that the collection depth "slides" along the critical charge curve (Figure 5) as the pressure changes from vacuum to atmospheric. As the collection depth slides along the curve the LET increases and so the ΔV_{OFF} increases. Once the end of range is reached, the charge is reduced and thus ΔV_{OFF} decreases.

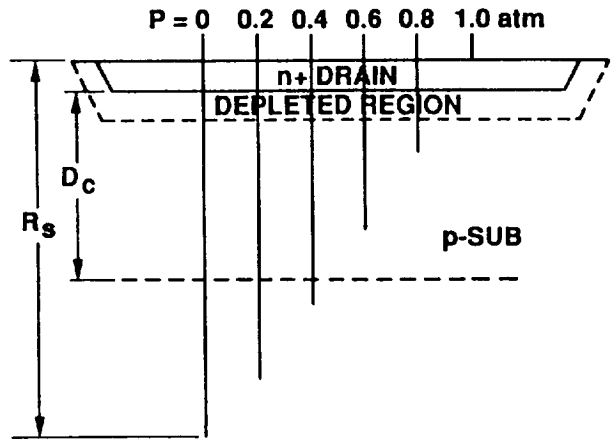

Figure 11: Alpha particle range variations due to energy loss in air before particles reach the silicon.

VIII. Conclusion

In conclusion, this test SRAM has been made sensitive to alpha particles through the use of a cell offset voltage and this has allowed a bench-level characterization in a laboratory setting. The experimental data was linked to alpha particle interaction physics and to SPICE circuit simulations through the alpha particle collection depth. The collection depth was determined by two methods and found to be about 7 μm. In addition, alpha particles that struck outside the bloated drain were able to flip the SRAM cells.

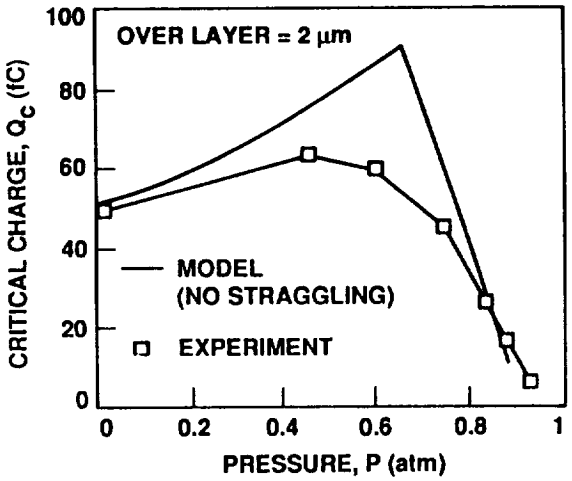

Figure 12: Variation of the critical charge with pressure. For a collection depth of 7 μm, Q_c increases due to an increase in LET with increasing pressure followed by a decrease in Q_c due to the collection of alphas at the end of their range.

This lateral charge collection was observed to be more than 6 μm. This effort will be extended to the evaluation of more complex SRAMs and latches.

IX. Acknowledgement

The authors are indebted to the USC/ISI/MOSIS project for the fabrication of the SEU chip used in this study. The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Defense Advanced Research Projects Agency, DoD, and the National Aeronautics and Space Administration. The assistance of V. Bobin from the U. of Idaho is deeply appreciated. The technical expertise of G. Soli in developing the the alpha particle interaction physics data is greatfully acknowledged.

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IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 38, NO. 6, 1486-1492, DECEMBER 1991

BENCH-LEVEL CHARACTERIZATION OF A CMOS STANDARD-CELL D-LATCH USING ALPHA-PARTICLE SENSITIVE TEST CIRCUITS

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ABSTRACT

This paper describes a methodology for predicting the SEU susceptibility of a standard-cell D-latch using an alpha-particle sensitive SRAM, SPICE critical charge simulation results, and alpha-particle interaction physics. Measurements were made on a 1.6-μm n-well CMOS 4k-bit test SRAM irradiated with an Am-241 alpha-particle source. A collection depth of 6.09 μm was determined using these results and TRIM computer code. Using this collection depth and SPICE derived critical charge results on the latch design, an LET threshold of 34 Mev cm^2/mg was predicted. Heavy ion tests were then performed on the latch and an LET threshold of 41 MeV cm^2/mg was determined.

I. INTRODUCTION

The characterization of digital ICs to heavy ion induced upsets is essential for qualifying their use in critical systems to be used on spacecraft. These characterizations are usually carried out at a heavy ion source such as a cyclotron. Such sources are expensive to use and there is usually a large lead time in scheduling time on the source.

The purpose of this paper is to introduce a technique utilizing test structures to quickly and inexpensively characterize the SEU sensitivity of standard cell latches intended for use in a space environment. This bench-level approach utilizes alpha particles to induce upsets in a low LET sensitive 4k-bit test SRAM. This SRAM consists of cells that employ an offset voltage to adjust their upset sensitivity and an enlarged sensitive drain junction to enhance the cell's upset rate [1,2].

We demonstrate that SRAM alpha particle data can be used to predict the latch LET threshold. The latch is modified by equipping it with an offset voltage so that its LET threshold can be lowered into the alpha particle range for direct comparison to the SRAM. The normal latch, with its offset voltage set to V_{DD} = 5 volts, is then tested with heavy ions to verify the SRAM LET threshold prediction.

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II. TEST SRAM AND D-LATCH DESIGNS

The test SRAM and latch designs studied in this paper were submitted to the MOS Implementation System (MOSIS) and fabricated at a 1.6-μm n-well double-metal CMOS/bulk foundry. A schematic diagram of the test SRAM cell is shown in Figure 1. This figure does not include the read/write transistors. The pulsed current source is used to model an alpha particle strike on drain Dn2 when calculating the critical charge of the cell with SPICE. This cell differs from that of a standard six-transistor SRAM cell in three ways: (1) the source of the p-MOSFET, Mp2, is connected to an adjustable offset voltage, V_O, instead of V_{DD} to provide a control of the cells critical charge; (2) the drain area of n-MOSFET Mn2, Dn2, has been enlarged by a factor of four over minimum to enhance upset rates, thus reducing measurement time; and (3) the cell is imbalanced by widening Mn2 over minimum to enhance its SEU sensitivity versus V_O response. The dimensions of the MOSFETs and their drains are given in Table 1. The bloated drain, Dn2, is fabricated in a p-type substrate doped to $5x10^{14}$ cm^{-3}. This substrate doping value was determined through a dopant profiling measurement utilizing a large edgeless n-MOSFET. The Dn2 junction

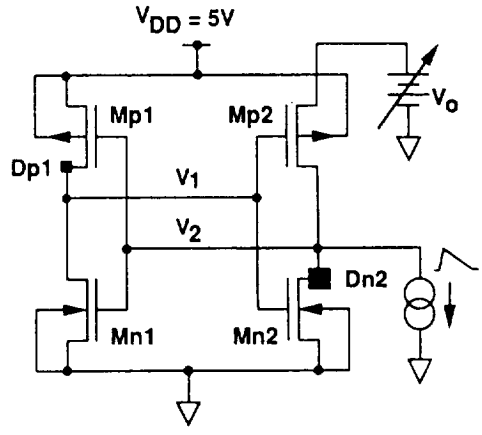

Figure 1. Schematic diagram of test SRAM cell showing the placement of V_O and the bloated n-drain, Dn2. The dimensions of the transistors and drains are listed in Table 1.

Table 1. SRAM Memory Cell As-Drawn Dimensions.

DEVICE	L (μm)	W (μm)	AD (μm^2)
Mn1	1.6	2.4	17.92
Mn2	1.6	3.2	74.88
Mp1	3.2	2.4	12.16
Mp2	3.2	2.4	12.16

has enhanced charge collection due to funneling compared to charge collected by the p-MOSFET drain formed in the n-well, where truncation of the ion-induced plasma track occurs.

In operation all the memory cells are written into a "sensitive" state where Mn2 is turned OFF and Mp2 is turned ON, connecting V_O to the bloated drain, Dn2. V_O is then lowered from V_{DD} = 5 V for a period called the stare time. Thereafter V_O is returned to V_{DD} and the cells read to determine the number of upsets. This cycle is repeated at different values of V_O and can be repeated a number of times at a given V_O to improve the resolution of the measurement.

The latch results presented in this paper were obtained from a 64-cell modified transparent D-latch array fabricated through the same foundry as the test SRAM. The schematic diagram of this latch in the zero state showing the reverse biased SEU-sensitive drain diodes is shown in Figure 2. The offset voltage, V_O was added to sensitize the latch to alpha particles. The source of Mp2 is tied to V_{DD} in the unmodified latch. The diodes designated with solid squares collect the most charge when struck by an ionized particle because they sit in the p-substrate. The layout of the latch cell is shown in Figure 3. This layout includes an inverter that generates an enable-bar, and inverters that buffer the V1-node and V2-node.

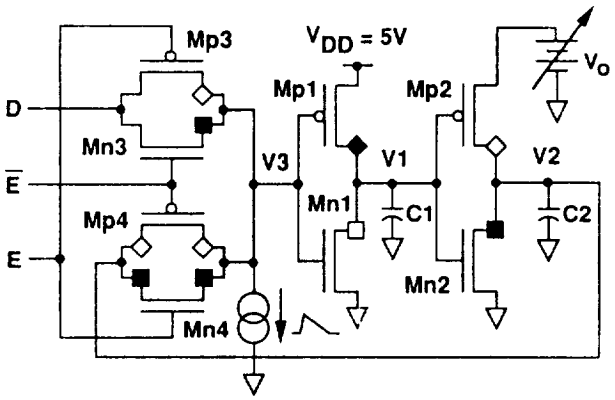

Figure 2. D-latch in the zero state. The reverse-biased diodes are SEU sensitive: p-substrate diodes (solid squares) and n-well diode (solid diamond). The zero-biased diodes are not SEU sensitive: p-substrate diode (open square) and n-well diodes (open diamonds).

The sensitive diode areas at the V2-node and V3-node that are designated with solid squares in Figure 2, are outlined with a bold line in Figure 3. These diodes each have an as-drawn area of 69 μm^2.

III. SPICE ANALYSIS

The critical charge, Q_C of the test SRAM cell and of the D-latch cell were determined as a function of V_O using MOSIS supplied parameters and SPICE. The parasitic nodal capacitances were modeled by fixed metal and polysilicon interconnect capacitances and by the drain depletion capacitances given by their areas and peripheries and by the SPICE LEVEL 2 junction capacitance parameters. A triangle current pulse with a 1:19 rise:fall shape was used to upset these cells. For a given pulse height, the transient simulation was evaluated to 100 ns where the response was compared to $V_{DD}/2$ to determine if the cell had flipped. The pulse height was adjusted using the binary search algorithm until the difference in charge (area under current pulse) between successive simulation runs differed by less than 1 fC. The resulting critical charge versus V_O response for the V2-node of the test SRAM cell and for the average of the V2-node and V3-node for the D-latch is shown in Figure 4. These results were found to be invariant with current pulse widths up to 500 ps. Since the alpha particle width is about 200 ps [3,4], the response of these circuits exceeds that of the alpha particle

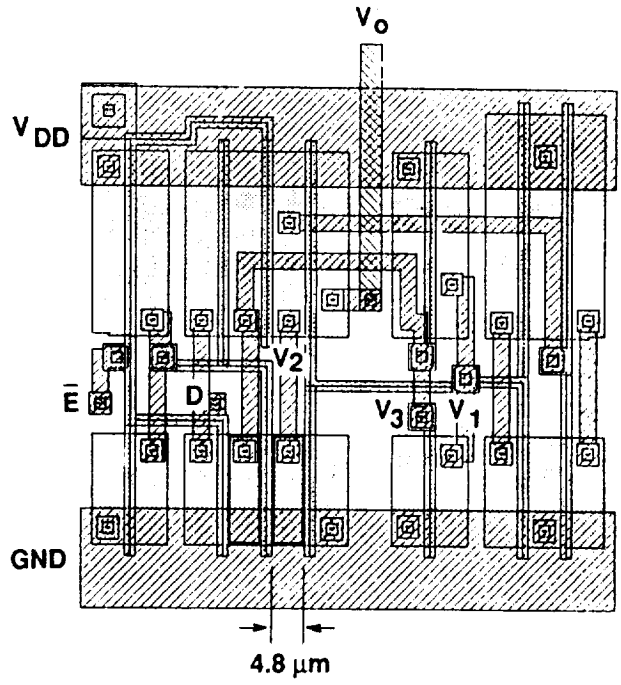

Figure 3. Layout of standard cell latch showing sensitive drains (solid squares in Figure 2) and offset voltage V_O connection. In the unmodified latch the metal 1 V_O trace is connected through a via to the metal 2 V_{DD} bus.

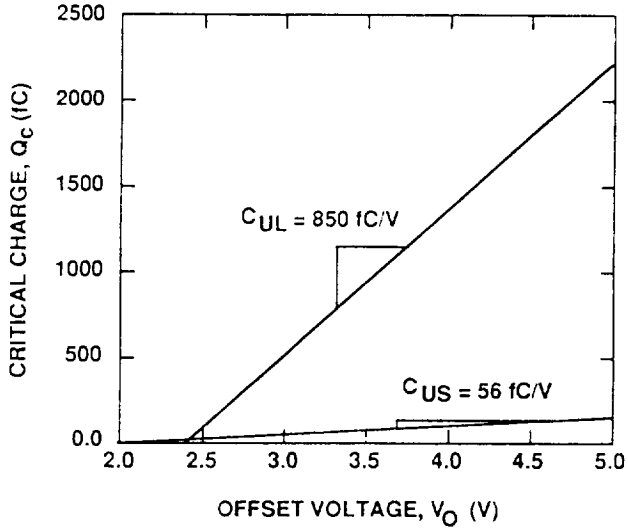

Figure 4. SRAM and latch critical charge calculated using SPICE.

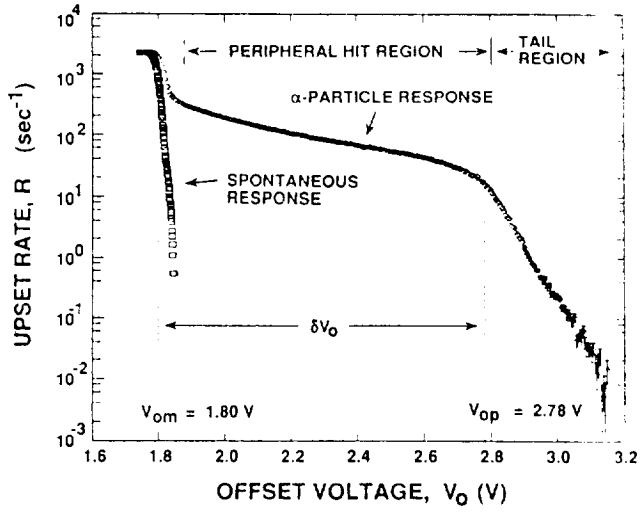

Figure 5. SRAM upset rate versus V_O response to a 4.6 μCi Am-241 source. The data used in this analysis were taken on 5-mV centers and are an average of 200 samples with a 2-second stare time.

current pulse. The critical charge of the latch V2-node and V3-node, which are connected through the "on" MOSFET Mn4, were averaged because their values differed little and it simplifies the LET-threshold analysis.

As V_O decreases the critical charge of the SRAM cell and D-latch decreases approximately linearly and goes to zero at $V_O = V_{om}$. For the SRAM cell V_{omS} = 1.8 V and for the latch V_{omL} = 2.4 V. DC SPICE simulations of these bistable circuits show that the sensitive state and metastable state approach each other as V_O decreases until they are equal when $V_O = V_{om}$. For $V_O \leq V_{om}$ the circuit spontaneously goes to the flipped state and is no longer bistable. V_{om} is a function of the threshold voltages and geometries of the n- and p-MOSFETs. Process induced dispersion in the MOSFET parameters give rise to a dispersion in V_{om} for the array of SRAM cells. The slopes of the critical charge curves in Figure 4 are defined as their upset capacitances, $C_U = \delta Q_C/\delta V_O$. The upset capacitance of the SRAM cell C_{US} = 56 fC/V and of the latch cell C_{UL} = 850 fC/V.

IV. TEST SRAM ALPHA-PARTICLE RESPONSE

The response of the SRAM to alpha particles from a 4.6 μCi Am-241 source placed 0.508 cm above the SRAM in air is shown in Figure 5. This source-to-SRAM distance was chosen to minimize test time while maintaining essentially normally incident alphas [2]. Also shown, is the spontaneous response which was measured without the alpha-particle source present. As V_O is lowered from V_{DD}, the SRAM begins to upset at V_O < 3.2 V in a region termed the tail region. As V_O is further lowered, the upset rate increases more slowly; this region is termed the peripheral hit region. Finally, as V_O reaches V_{om} = 1.8 V, the upset rate increases very rapidly in what is termed the spontaneous flip region. The spontaneous response remained constant (negligible total dose shift) throughout the 33.3 hours of alpha particle exposure.

In the peripheral hit region, cells upset when the alpha particles hit the Dn2 drain or come close to, but miss, the Dn2 drain. This effect can be explained by a delayed field-funneling effect [4] and to diffused charge that is collected by Dn2. Since the cell critical charge decreases as V_O decreases, the alpha particles can strike further from the Dn2 depletion edge and still upset the cell.

The upset rate R, displayed in Figure 5, was obtained by dividing the average measured number of upsets N_a that occurred in a stare time t by t, or $R = N_a/t$, where

$$N_a = \frac{1}{k}\sum_{i=1}^{k} N_i \pm \frac{1}{k}\left(\sum_{i=1}^{k} N_i\right)^{1/2} \qquad (1)$$

and the number of samples, k = 200. The stare time t, in this case, was fixed at 2 seconds. The spontaneous upset data was also divided by t so that both responses saturate at N_t/t= 2048, where N_t is the number of cells in the memory array (4096 in this case). In the analysis to follow, the spontaneous response is approximated by the step function N_t [1-u(V_O-V_{om})] = 4096[1-u(V_O-1.8)], where u(V) is the unit step function. This is justified for the SRAM data shown in Figure 5 because the slope of the spontaneous response is 2048 cells/34 mV· sec

which is much steeper than the SRAM alpha-particle response in the tail region. The response of the SRAM cells is given by the detector equation:

$$\frac{dN}{dt} = \sigma\Phi(N_t - N) \qquad (2)$$

where σ is the device cross section (Dn2 drain area), and Φ is the total integrated flux whose particles deposit energies exceeding the critical energy, E_C required to trip a cell. The homogeneous solution of (2) with initial condition at t = 0 of no tripped cells (N = 0) is:

$$N = N_t(1 - \varepsilon^{-\sigma\Phi t}) \qquad (3)$$

The upset capacitance C_U, the spontaneous upset voltage V_{om}, and the hole-electron pair charge-energy factor for silicon K = 44.2 fC/MeV enable one to calibrate the offset voltage, V_O axis in terms of the critical energy by:

$$E_C = \frac{C_U}{K}(V_O - V_{om}) \qquad (4)$$

or for this SRAM, $E_C = 1.267(V_O - 1.8)$ MeV.

The effective flux, Φ is a function of V_O and is given by:

$$\Phi(V_O) = \int_{V_O}^{\infty} \phi(V)\, dV \qquad (5)$$

where the source spectral flux $\phi(V) = \phi(E)$ and the energy $E = (C_U/K)(V - V_{om})$. Applying (5) to (3) and solving for dN/dV_O one gets:

$$\frac{dN}{dV_O} = \frac{dR}{dV_O} = -\sigma t\left(1 - \frac{N}{N_t}\right)\phi(V_O)$$

$$\approx -\sigma t\, \phi(V_O) \quad ; \; N << N_t \qquad (6)$$

This is the condition under which the data in Figure 5 was taken, therefore dR/dV_O is the average particle spectrum in the collection region of the sensitive drain Dn2.

Figure 6 illustrates the relationship between upset rate R, the SRAM spontaneous density n, the source spectra ϕ, and the SPICE derived critical charge curve. The spontaneous density, n, is the derivative of the spontaneous response data shown in Figure 5, and was found to be gaussian with a mean and standard deviation of $V_{om} = 1.8 \pm 0.011$V. The area under the $n(V_O)$ curve is equal to N_t. The critical charge curve of Figure 6 , characterized by (4) when there is no dispersion in n, functions as a calibration for mapping the source spectra onto the V_O axis. In this case, $V_O = V_{om} =$ 1.8 V represents zero energy. As V_O is lowered from $V_{DD} =$ 5 V, no cell upsets occur until $\Phi > 0$ which occurs when

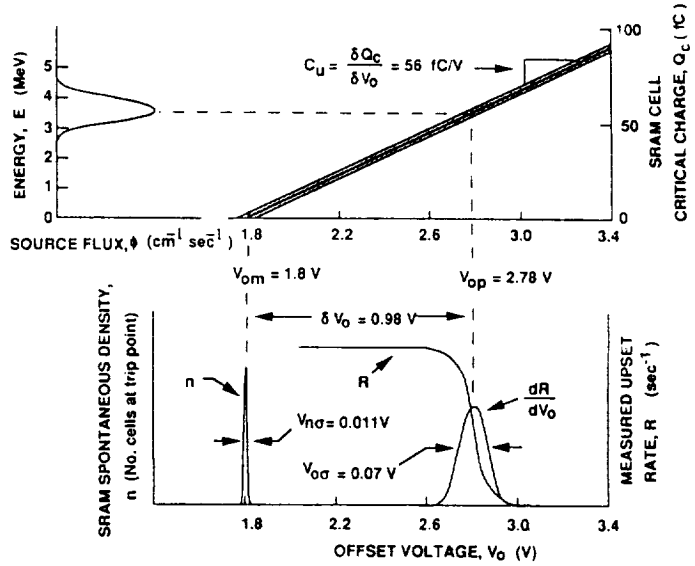

Figure 6. Relationship between measured upset rate, the spontaneous density function, the source spectra, and the SRAM critical charge response.

V_O <3 V. As V_O is further reduced below 3 V, the upset rate increases giving the tail-region response in Figures 5 and 6. When V_O reaches 2.6 V, all of the source spectrum is effective in upsetting SRAM cells and the upset response saturates at a maximum. In the absence of the peripheral hit effect, the response would remain at this maximum value as V_O was decreased below 2.6 V, as shown in Figure 6.

The tail-region response shown in Figure 5 was smoothed and differentiated using a twenty-five point least squares difference algorithm [5,6]. This differential response, shown in Figure 7, is composed of a number of peaks plus the onset of the peripheral hit response. These peaks are due to to the selective degradation of the alpha-particle energies as the particles pass through the various regions found in the bloated drain, Dn2. The major peak, shown on Figure 7, is due to the alpha particles that pass through the thickest regions, those covered with metal 2 (M2). This M2 region is 38.2 μm^2 [2]. In the region covered with M2, the alpha particles lose more energy than in other regions so that they have the highest linear energy transfer (LET). The cross section for the M2 portion of the bloated drain was calculated using half the total alpha-particle flux , $\Phi(V_{om})/2$ and found to agree closely with the as-drawn area [2]. With V_O set at the peak, V_{op}, only half of the alpha particles have sufficient energy (or LET) to flip the memory cells, thus $\Phi(V_{op}) = \Phi(V_{om})/2$.

A schematic view of the path of the alpha particle through the silicon is shown in Figure 8. Relating the full-width-half-maximum of the response shown in Figure 7, V_{of} to the energy straggle of the alpha particles in the collection region

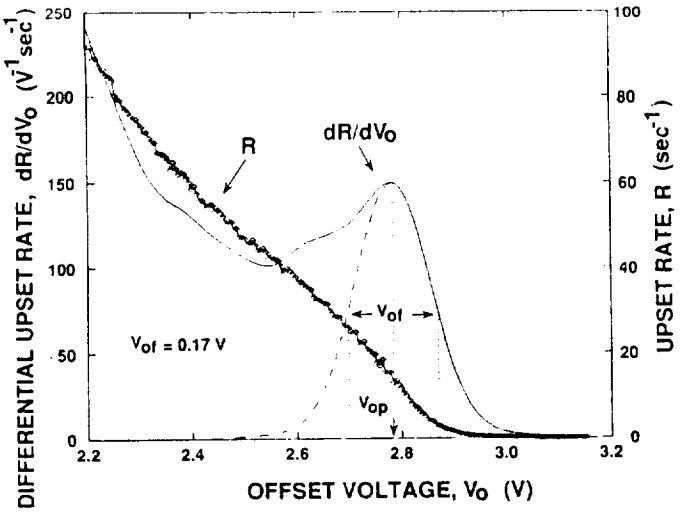

Figure 7. Test SRAM differential upset rate response showing peak at V_{op} = 2.78 V with full-width-half-maximum of V_{of} = 0.170 V.

of the silicon, the Si thickness $X_4 - X_2$ = 13.58 μm was obtained [2]. The full-width-half-maximum, V_{of} in Figure 7 is related to the one standard deviation of a gaussian, $V_{o\sigma}$ in Figure 6 by $V_{of} = 2.35V_{o\sigma}$. Next the Si collection layer, δX_4, was determined by matching the charge deposited by the alpha particles in δX_4 to the shift in the offset voltage, $\delta V_O = (V_{op} - V_{om}) \pm V_{o\sigma}$ = 0.98V ± 0.07V [2]. Finally the over-layer thickness, δX_3 was calculated by $\delta X_3 = (X_4 - X_2) - \delta X_4$ = 7.59 μm. This over-layer thickness is applicable to 50% of the Dn2 drain area (that covered by metal 2). An effective Dn2 over-layer thickness of 4.3 μm was obtained using an average V_{op} of 2.66 V. This value of V_{op} was determined by first obtaining a reduced differential response where the peripheral hit response was removed (fitting an exponential to the dR/dV_O response between V_O = 2 V and 2.2 V and then subtracting this exponential function from the dR/dV_O data shown in Figure 7). Then the average V_{op} is the weighted average of the reduced dR/dV_O response.

Using the offset voltage shift and upset capacitance, the SRAM-cell collected charge $Q_{cS} = C_{US}\ \delta V_O$ = 54.9 ± 3.9 fC. Also, the energy deposited in the silicon collection layer δX_4, and its straggling $E_{\sigma 4}$ shown in Figure 8 is: $\delta E = (E_4 - E_3) \pm E_{\sigma 4} = Q_{cS}/K$ = 1.24 ± 0.088 MeV.

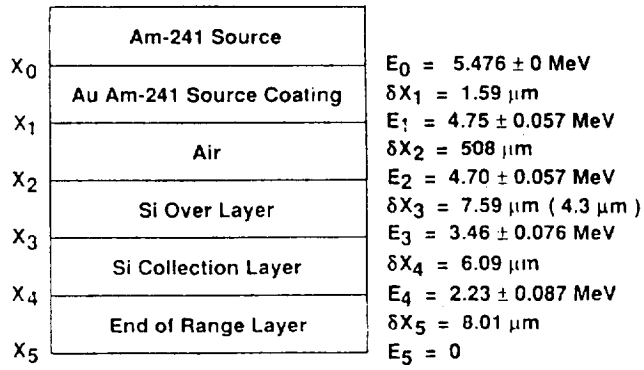

Figure 8. Schematic view of the alpha-particle path from the source to the SRAM. The over-layer thickness δX3 = 7.59 μm corresponds to the Dn2 region covered by metal 2. An average over-layer thickness for the whole Dn2 area of 4.3 μm was obtained.

V. D-LATCH ALPHA PARTICLE RESPONSE

The alpha-particle response of the latch array was obtained in the same manner as for the SRAM except that the Am-241 source was placed 0.558 cm above the latch chip in air. The results, shown in Figure 9, include the spontaneous data obtained before and after exposing the part to alpha particles. The shift observed in these responses is due to total dose effects such as the charging of gate oxides. The average of the pre- and post-radiation spontaneous data was used in the analysis of this part. This small shift, due to total dose effects, was neglected for the SRAM because the δV_O shift in the SRAM alpha-particle response was much larger than that of the latch.

The dispersion in the latch alpha-particle response, shown in Figure 9, is primarily that of the spontaneous response because the offset voltage dispersion due to the alpha-particle energy spectrum is much smaller than the dispersion in the spontaneous response. This is a consequence of the reduced energy detection sensitivity of the latch (K/C_{UL} = 0.052 V/MeV for the latch versus K/C_{US} = 0.789 V/MeV for the SRAM). The dispersion in the latch alpha-particle response, $V_{o\sigma}$ = 34 mV, was found by fitting the data to a gaussian function. As shown in Figure 9 the shift in the offset voltage, δV_O, was obtained between the points on the average spontaneous curve and the alpha-particle curve where, on the average, half of the latch cells are flipping ($N_f/2$ = 32). Using the SPICE derived upset capacitance of the latch, C_{UL} = 850 fC/V, the collected charge required to upset a modified latch cell with its LET threshold lowered into the alpha-particle range is δQ_{cL} = 50.2 ± 28.9 fC which agrees with that obtained with the SRAM, Q_{cS}.

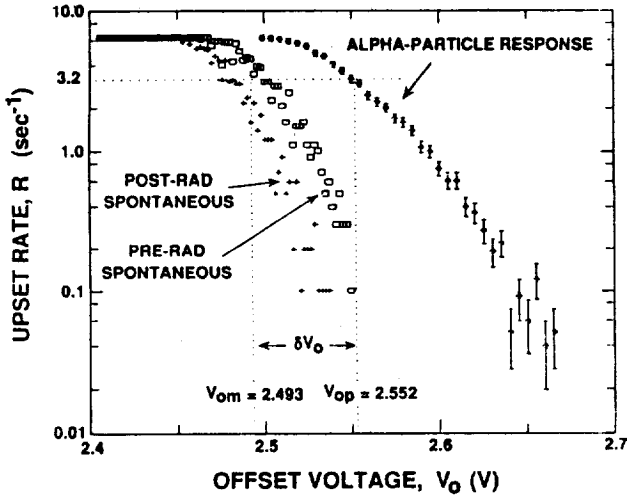

Figure 9. D-latch alpha-particle response. The data used in this analysis were taken on 5-mV centers and are an average of 10 samples with a 10-second stare time.

When the offset voltage for the SRAM and the latch is swept through the alpha particle δE peak, the charge required to upset their cells is equivalent. $Q_c = K\,\delta E$ where δE is the energy deposited in the silicon collection layer $\delta X4$ which is the same for the SRAM and latch because they are both fabricated through the same process (p-type substrate doped to 5×10^{14} cm^{-3}). For the same alpha-particle beam the charge loss mechanisms (X4 is less than the alpha particle range) are equivalent in the SRAM and the latch. Since $Q_{CL} \approx Q_{CS}$, it is valid to apply the collection depth δX_4 obtained with the SRAM to the analysis of the latch.

For the latch, the LET threshold for V_{DD} = 5 V operation can be predicted from the SPICE derived upset capacitance, C_{UL}, the measured mean spontaneous offset voltage, V_{om}, and the collection depth obtained from the SRAM alpha-particle response, δX_4:

$$LET = \frac{C_{UL}\,(V_{DD} - V_{om})}{K\,\rho\,\delta X_4} = 34\,\frac{MeV\,cm^2}{mg} \qquad (7)$$

where, C_{UL} = 850 fC/V, V_{om} = 2.49 V, K = 44.2 fC/MeV, ρ = 2320 mg/cm^3 for Si, and $\delta X_4 = 6.09 \times 10^{-4}$ cm.

VI. D-LATCH HEAVY ION RESPONSE

Heavy ion tests were performed with 317 MeV I-127, 279 MeV Br-79, and 255 MeV Fe-56 at the Brookhaven National Laboratory on the latch array with $V_{DD} = V_O$ = 5 V. These measurements were made by gating the ion beam on and then off when a fluence, $F = 1.13 \times 10^7/\cos\theta$ was reached, where θ is the angle if incidence. This fluence was chosen to maintain an experimental error of less than 3.2% and caused V_{om} to shift by 0.4 mV for each heavy ion beam. The stare time was set so that an average of two upsets would occur each test cycle. This assured that essentially all N_t = 64 latch cells in the array were susceptible to upset and allowed the effective cross section to be calculated by:

$$\sigma = \frac{N}{N_t\,F\cos\theta} \qquad (8)$$

where N is the total number of upsets that occur while the ion bean is gated on.

Using the average over layer thickness, δX_3 = 4.3 μm, and the collection depth, δX_4 = 6.1 μm obtained from the SRAM alpha particle measurements, the energies of the ions used in the test were computed from TRIM [7] at the entry point of the Si collection layer, X3 and at the exit point of the Si collection layer, X4. The average LET of the ion in the collection layer was then calculated by:

$$LET = \frac{E(X3) - E(X4)}{\rho\,\delta X4} \qquad (9)$$

These results are shown in Table 2 and in Figure 10.

Table 2. Heavy Ion Test Results.

ION	PLOT SYMBOL	ANGLE, θ (degrees)	σ (cm^2)	LET (MeVcm^2/mg)
I-127	□	0	232	58.8
Br-79	■	45	209	57.3
Br-79	○	35	144	49.5
Br-79	●	0	63.8	40.3
Fe-56	×	45	33.0	37.5

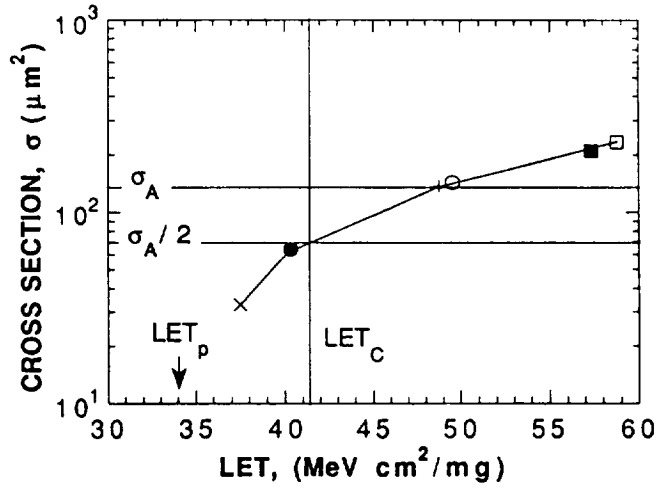

Figure 10. Heavy ion test results performed on latch with $V_O = V_{DD}$ = 5 V.

The critical LET in Figure 10 is at one half the as-drawn cross section because at a δE peak (see Figure 6) only half of the particles can cause upsets. The increase in the measured LET over the predicted value indicates a charge loss, relative to alpha particles, for these heaver ions. This loss might be due to faster recombination in the denser plasma tracks. Experiments are planned to quantify this relative charge loss.

VII. CONCLUSIONS

A test SRAM, designed to be upset-sensitive (LET soft) and having an electrically adjustable critical charge has been characterized with alpha particles using an inexpensive laboratory setup. The LET threshold of a standard-cell D-latch was predicted using the SRAM alpha-particle results and SPICE simulation results. The predicted LET threshold of 34 MeV cm^2/mg compares favorably with the heavy ion test result of 41 MeV cm^2/mg. This discrepancy in the predicted LET threshold could be due to less efficient charge collection for the heavier ions. Experiments are being planned that will directly measure decreases in charge collection efficiency.

VIII. ACKNOWLEDGMENT

The authors are indebted to the USC/ISI/MOSIS project for the fabrication of the test SRAMs and latch arrays used in this study. The research described was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration.

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PROTON-SENSITIVE CUSTOM SRAM DETECTOR

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ABSTRACT

Because of the recently discovered importance of protons to the upset of spaceborne electronics, a custom 4k-bit SRAM chip was tested with protons. The SRAM was developed to determine the Single Event Upset hardness of CMOS latches using alpha particle measurements, by adjusting an offset voltage that reduces the charge required to upset a cell. The proton experiments were designed to observe both proton and silicon recoil produced ionization. The silicon recoils were generated by protons undergoing nuclear coulomb scattering. It was discovered that silicon recoil produced charge can be collected from very deep in the silicon substrate. This paper describes a calibration procedure for the SRAM detector. Source spectra were acquired with this chip by measuring the number of upset cells versus offset voltage.

I. INTRODUCTION

A custom 4k-bit SRAM chip, developed to measure the Single Event Upset hardness of CMOS latches through alpha particle measurements [1], can also function as a proton detector. The SRAM detector has an offset voltage that adjusts the cell critical charge to upset, allowing a threshold to be set, below which its cells will upset. This threshold can be set below the charge deposited by protons passing through, or stopping in, a charge collection region. Because of the recently discovered importance of protons to the upset of spaceborne electronics, as observed on the CRRES (Combined Release Radiation Effects Satellite) [2], the SRAM detector was tested with protons.

The proton experiments were designed to observe both proton and silicon recoil produced ionization. The silicon recoils were generated by protons undergoing nuclear coulomb scattering. A charge collection region thickness of 6.64 μm was measured for proton produced ionization, which compares favorably with the charge collection region thickness of 6.33 μm for alpha particle produced ionization [1]. The charge collection region thickness for silicon recoil produced ionization was discovered to be nearly equal to the protons range in the silicon substrate.

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This paper describes a calibration procedure for the SRAM detector, allowing spectrometers to be designed for measuring proton, helium, and heavier ion environments inside spacecraft computers. The detector was calibrated for protons using the Caltech Tandem Van de Graaff. The SPICE circuit simulation program is used to compute an effective calibration curve and this curve is then used, with the proton data, to compute an effective charge collection depth, allowing calibration [1,3,4].

II. SRAM DETECTOR DESIGN

The SRAM design was submitted to the MOS Implementation System (MOSIS) and fabricated at a 1.6-μm n-well double-metal CMOS/bulk foundry. A schematic diagram of the SRAM cell is shown in Figure 1. The pulsed current source is used to model a particle strike on drain Dn2 when calculating the critical charge of the cell with SPICE. This cell differs from that of a standard six-transistor SRAM cell in three ways: (1) the source of the p-MOSFET, Mp2, is connected to an adjustable offset voltage, V_O, instead of V_{DD} to provide a control of the cell's critical charge; (2) the drain area of n-MOSFET Mn2, Dn2, has been enlarged by a factor of four over minimum to enhance upset rates, thus reducing measurement time; and (3) the cell is imbalanced by widening Mn2 over minimum to enhance its SEU sensitivity versus V_O. The bloated drain, Dn2, is fabricated in a p-type substrate doped to 5×10^{14} cm^{-3}. This substrate doping value was determined through a dopant profiling measurement utilizing a large edgeless n-MOSFET.

In operation all the memory cells are written into a "sensitive" state where Mn2 is turned OFF and Mp2 is turned ON, connecting V_O to the bloated drain, Dn2. V_O is then lowered from V_{DD} = 5 V allowing the SRAM to accumulate upsets at a given V_O value. Thereafter V_O is returned to V_{DD} and the cells read to determine the number of upsets. This cycle is repeated at different values of V_O.

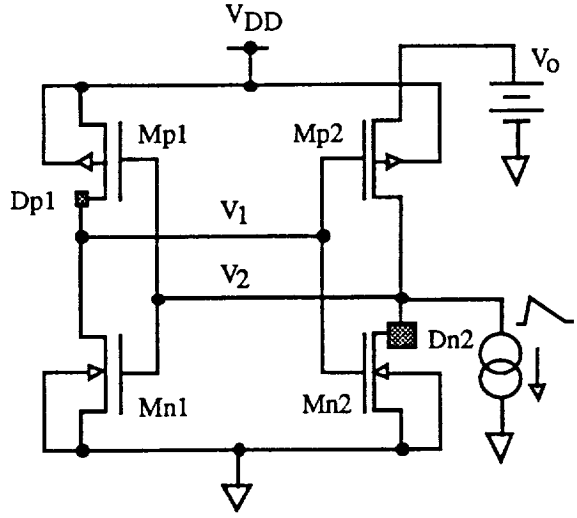

Figure 1. Schematic diagram of the SRAM cell showing the placement of V_O and the bloated n-drain, Dn2

III. SPICE ANALYSIS

The critical charge, Q_c of the SRAM cell was determined as a function of V_O using MOSIS supplied SPICE parameters. The parasitic nodal capacitances were modeled by fixed metal and polysilicon interconnect capacitances and by the drain depletion capacitances given by their areas and peripheries and by the SPICE level-2 junction capacitance parameters. A triangle current pulse with a 1:19 rise:fall shape was used to upset these cells. For a given pulse height, the transient simulation was evaluated to 100 ns where the response was compared to $V_{DD}/2$ to determine if the cell had flipped. The current pulse height was adjusted using the binary search algorithm until the difference in charge (area under current pulse) between successive simulation runs differed by less than 1 fC. These results were found to be invariant with current pulse widths up to 500 ps. Since the proton width is about 200 ps [1], the response of these circuits exceeds that of the proton current pulse. The resulting critical charge versus V_O for the V2-node of the SRAM cell is shown in Figure 2. This curve is the effective calibration curve used with the proton data to calibrate the SRAM detector.

As V_O decreases the critical charge of the SRAM cell decreases approximately linearly and goes to zero at $V_O = V_{om}$ = 1.8 V. DC SPICE simulations of these bistable circuits show that the sensitive state and metastable state approach each other as Vo decreases until they are equal when $V_O = V_{om}$. For $V_O \leq V_{om}$ the circuit spontaneously goes to the flipped state and is no longer bistable. V_{om} is a function of the threshold voltages and geometries of the n- and p-MOSFETs. Process induced dispersion in the MOSFET parameters gives rise to a dispersion, $V_{om\sigma}$=0.011 V, in V_{om} for the array of SRAM cells. The slope of the critical charge curve in Figure 2 is defined as the upset capacitance, $C_u = \delta Q_c/\delta V_O$ = 56 fC/V.

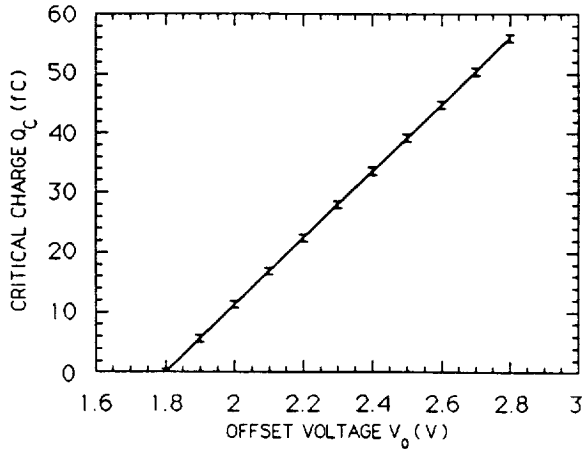

Figure 2. SRAM critical charge calculated using SPICE showing error bars associated with spontaneous upset data [1]. The SRAM calibration curve.

IV. SRAM PROTON RESPONSE

The response of the SRAM to protons from the Caltech tandem Van de Graaff is shown in Figures 3 and 4. Each data point was obtained by setting the offset voltage, V_O, and allowing the SRAM to accumulate upsets until an independently measured fluence, F, was reached. Upon reaching the preset fluence the SRAM memory was cleared and the process repeated for k runs. The sum of the number of upsets for k runs was recorded by a NIM counter.

The normalized cross section, $A = A_m/A_a$, where A_m is the measured cross section and, A_a = 68.8 μm^2, is the as-drawn Dn2 sensitive drain area. The data points above the A = 1 line in Figure 3 contain a contribution from protons hitting outside the sensitive cell areas. Some of the charge deposited by these peripheral hits is collected by the Dn2 drain [1]. If this effect were not present, all data points would have an $A \leq 1$. The alpha particle data, shown in Figures 3 and 4, was taken from Figure 5 in Reference 1 and its A values were derived with Equation 6 in Reference 4 using the sensitive drain area, A_a.

For the proton data, the average number of upset cells per run, <n>, in k runs is <n> = N/k, where N is the accumulated number of upsets recorded by a NIM counter. k = 50 for all data points except for the 5.0 MeV data at two points, k = 10 at V_O = 2.1 and 2.2 V. <n> is related to the normalized cross section, A, by the equation:

$$A = \frac{-1}{A_a F} \ln\left(1 - \frac{\langle n \rangle}{N_T}\right) \qquad (1)$$

where F is the independently measured fluence and N_T = 4096, is the total number of SRAM cells. Equation 1 is the homogeneous solution of Equation 2 [also Equation 2 in

reference 1] with the initial condition at t = 0 of no upset cells, ie. <n> = 0:

$$\frac{d<n>}{dt} = A_m\phi(N_T - <n>) \qquad (2)$$

where ϕ is the flux and $F = \phi t$ is the fluence.

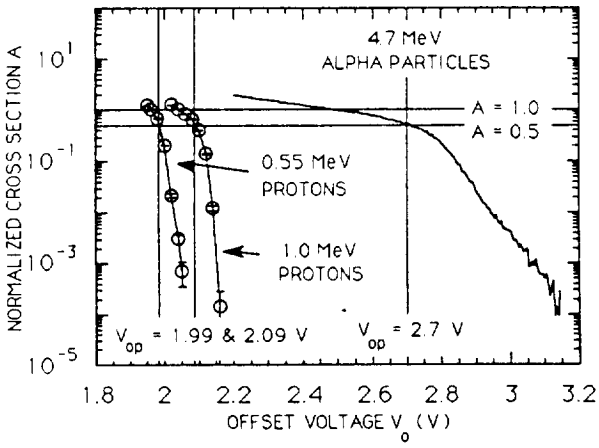

Figure 3. The SRAM response to direct ionization from 0.55 and 1.0 MeV protons and 4.7 MeV alpha particles. The mean offset voltage values are shown at one half the cross section. The measured cross section is normalized to unity at the Dn2 drain area.

The dispersion in F is, $F_\sigma = \sqrt{F/A_c}$, where $A_c = 0.02 + 0.0 - 0.0004$ cm^2 is the proton counter cross section. The counting system was calibrated with an alpha source calibrated silicon surface barrier detector. This calibration compared favorably with Moliere scattering in the gold foil used to produce a uniform proton beam over the SRAM and the position of the counter relative to the SRAM. The number of counts equals the fluence divided by 50 + 0.0 - 1.0. Each k run was for 1,000 counts, except for 5.0 MeV data at offset voltages above 1.94 V. At 1.95, 1.96, and 1.98 V the number of counts was 1E4, and at 2.1 and 2.2 V the number was 1E5. The dispersion in <n> is given by:

$$<n_\sigma> = \frac{1}{km}\left(\sum_{i=1}^{m} N_i\right)^{1/2} \qquad (3)$$

where m is the number of experiments each consisting of k runs. The number m = 1 for all data points except for the 0.55 MeV data at two points, m = 6 at V_O = 1.95 V and m = 2 at V_O = 2.0 V. The dispersion in A is given by:

$$\left(\frac{A_\sigma}{A}\right)^2 = \left(\frac{F_\sigma}{F}\right)^2 + \left(\frac{<n_\sigma>}{FA_m(N_T - <n>)}\right)^2 \qquad (4)$$

The data points in Figure 3,with 1 > A > 0.01, are shown in the Figure 4 as the percent probability that particle i will deposit a charge equivalent voltage V_{oi} that is greater than the energy threshold equivalent offset voltage V_o. The A values ≥ 1 cannot be plotted on probability paper and the large errors on the A values ≤ 0.01 place little weight on these points. The percent probability A values are fit to a line to measure the mean, $V_{op\mu}$, which is equivalent to a probability density gaussian peak centroid, and the standard deviation, $V_{op\sigma}$, of these integral gaussian distributions.

The 0.55 MeV mean is a measure of the proton energy minus the energy lost in the device overlayers. The 0.55 MeV proton is stopped in the charge collection region of the Dn2 drain. This is true because the standard deviation is the sum, in quadrature, of the proton beam energy dispersion, the drain overlayer material straggling, and the SRAM spontaneous upset voltage, V_{om}, standard deviation, $V_{om\sigma}$. The proton beam dispersion was generated by a 1.2 μm thick gold foil placed up stream to produce a uniform beam over the SRAM. The 0.55 MeV proton beam energy was measured with an alpha source calibrated silicon surface barrier detector at 557 ± 11.5 keV. No contribution to the SRAM energy peak dispersion from straggling in silicon below the overlayer material is measured for 0.55 MeV protons. The 1.0 MeV proton data shows a significant contribution to its measured standard deviation from straggling in silicon below the overlayer material and is therefore a delta energy peak.

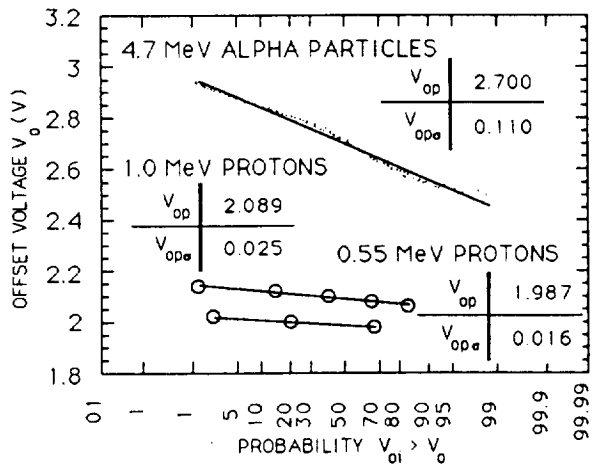

Figure 4. The proton and alpha particle normal voltage distribution means and standard deviations.

The upset capacitance C_u, the spontaneous upset voltage $V_{om\mu} \pm V_{om\sigma}$, and the hole-electron pair charge-energy factor for silicon K = 44.2 fC/MeV give the mean and standard deviation voltages, shown in Figure 4, in terms of energy by the following equations:

$$E_{op\mu} = \frac{C_u}{K} (V_{op\mu} - V_{om\mu}) \quad (5)$$

$$E_{op\sigma} = \frac{C_u}{K} V_{op\sigma} \quad (6)$$

where (C_u/K) = 1.267 MeV/V, $V_{om\mu}$ = 1.80 V, and $V_{om\sigma}$ = 0.011 V.

Applying Equations 5 and 6 to the data mean and standard deviation values gives, $E_{op\mu} \pm E_{op\sigma}$ = 1.140 ± 0.139 MeV for 4.7 MeV alpha particles, $E_{op\mu} \pm E_{op\sigma}$ = 0.237 ± 0.020 MeV for 0.55 MeV protons, and $E_{op\mu} \pm E_{op\sigma}$ = 0.366 ± 0.032 MeV for 1.0 MeV protons.

The Dn2 drain overlayer and charge collection region thicknesses, shown in Table 1, are computed from Equation 5 and the alpha particle and proton range tables for silicon [5]. Silicon is used for both the overlayer and charge collection region materials.

Table 1. Proton and alpha particle delta range and delta energy in the SRAM silicon equivalent overlayer and silicon charge collection regions.

Particle E (MeV)	Alpha 4.7	Proton 0.55	Proton 1.0
Overlayer			
ΔE (MeV)	0.68	0.313	0.191
ΔR (μm)	4.32	4.32	4.32
Collection			
ΔE (MeV)	1.14	0.237	0.366
ΔR (μm)	6.33	-------	6.64

Because the 0.55 MeV proton stops in the charge collection region, the difference between the incoming proton energy and the energy given by Equation 5, 0.237 MeV, equals the energy lost in the silicon equivalent overlayer, 0.313 MeV and the overlayer thickness is the difference in their respective ranges, 4.32 μm. After passing through 4.32 μm, the 1.0 MeV protons deposit 0.366 MeV, from Equation 5, in the charge collection region. The difference in the ranges of the proton entering the collection region and exiting the region after losing 0.366 MeV is 6.64 μm, the effective charge collection region depth for protons. After passing through a 4.32-μm silicon equivalent overlayer, the alpha particles have an effective charge collection region depth of 6.33 μm. A 5.1-μm effective charge collection region depth for this CMOS/bulk process was measured with 255 MeV iron. This measurement required using a D-latch circuit having an offset capacitance of 850 fC/V [1].

The SRAM has a 4.32-μm silicon equivalent overlayer thickness and a 6.64-μm effective charge collection depth for normal incident protons. These depths are a function of the SPICE computed upset capacitance, C_u, and would change for different computed values. But for the purpose of predicting the SRAM response to low energy protons and alpha particles this calibration procedure is functional. Analysis of proton straggling in these silicon regions demonstrates the functionality of the SPICE assisted calibration [4]. The energy straggling is given by the following equation:

$$E_\sigma = (4\pi z^2 e^4 n Z \Delta R)^{1/2} \quad (7)$$

where z and Z are the proton and silicon atomic numbers, n is the number density of silicon, and ΔR is the silicon thickness. The standard deviations given by Equation 6 is equivalent to:

$$E_{op\sigma} = [(E_{om\sigma})^2 + (E_{Au\sigma})^2 + (E_{Si\sigma})^2]^{1/2} \quad (8)$$

The spontaneous upset standard deviation is 14 keV, the 1.2-μm Au foil produces a 12 keV standard deviation in the proton beam energy, and 4.32 μm of Si produces a 9 keV standard deviation. It follows from Equation 8 that $E_{op\sigma}$ = 21 keV for the 0.55 MeV data which compares favorably with the value of 20 keV given by Equation 6. For the 1.0 MeV proton beam, 11 μm of Si produces a 14 keV standard deviation. Applying Equation 8 gives, $E_{op\sigma}$ = 23 keV, which is 22 keV less, in quadrature, than the 32 keV given by Equation 6. This difference is equivalent to a 0.31-μm standard deviation in the effective charge collection depth.

The large tail on the 5.0 MeV data shown in Figure 5 is generated by Rutherford Scattering (RS). Because 5.0 MeV protons lose energy as they penetrate the substrate to a total range of 213 μm, the RS cross section must be summed over the effective range. The normalized cross section, A, for RS is given by the equation:

$$A = n \sum_{i=1}^{R/\Delta R} (\sigma_c(T_1))_i (\Delta R)_i \quad (9)$$

where σ_c is the RS cross section, n is the silicon number density, and R is the effective RS path length of the protons in the SRAM substrate. σ_c is given by:

$$\sigma_c (T_1) = (4\pi / BT_1) \int_{T_4}^{BT_1} (d\sigma_c / d\Omega) \, dT_4 \quad (10)$$

where T_1 is the proton energy before scattering and $(d\sigma_c/d\Omega)$ is the Rutherford differential scattering cross section. The maximum proton energy transferable to a silicon nucleus, in a head-on collision, is BT_1 and T_4 is the minimum silicon recoil energy required to upset an SRAM cell. $B = (4M_1 M_2)/(M_1 + M_2)^2$, where M_1 and M_2 are the proton and silicon mass numbers. T_4 is given by the equation:

$$T_4 = \frac{C_u}{K} (V_O - V_{op\mu}) \quad (11)$$

where $V_{op\mu}$ = 1.852 volts, given by the V_O value at A = 0.5 for the 5.0 MeV data in Figure 5.

The proton effective path length, R, used in Equation 9 is given by:

$$R = R(T_{max}) - R(T_{min}) \quad (12)$$

where $R(T_{max})$ is the incoming proton path length in silicon and $R(T_{min})$ is the proton path length when its energy has just dropped below that required to produce an upset, in a head-on collision.

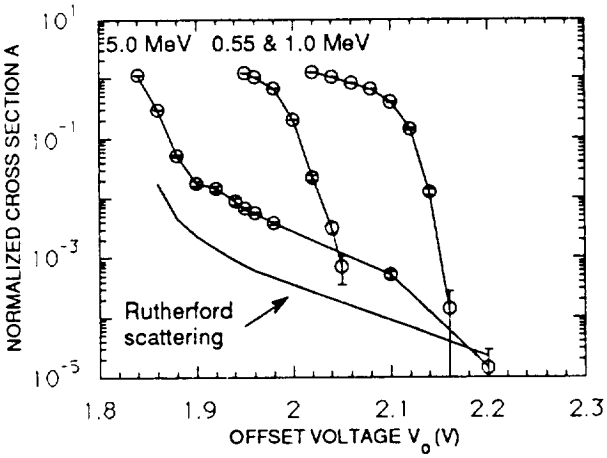

Figure 5. Rutherford scattering compared to the 5.0 MeV proton data assuming that all the silicon recoil charge is collected.

The Rutherford scattering curve falls below the 5.0 MeV data, indicating that the sensitive node cross section is larger for RS than for direct ionization. The protons undergoing RS do not need to pass directly through the sensitive node to cause a flip.

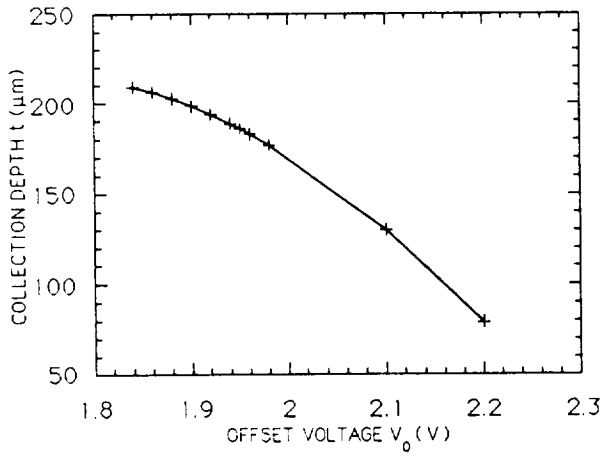

Figure 6. The maximum depth from which silicon recoil produced charge can upset the SRAM.

The data indicates that silicon recoil produced charge is collected from very deep in the substrate. The effective Rutherford scattering path length, R, in Equation 9, is plotted as a function of offset voltage in Figure 6, and is the maximum depth from which silicon recoil charge can upset the SRAM for 5.0 MeV protons.

V. CONCLUSIONS

The SPICE assisted calibration utilizing 56 fC/V and the proton data identified a 4.32-μm silicon equivalent overlayer and a 6.64 ± 0.31 μm effective charge collection depth for protons and a 6.33-μm collection depth for alpha particles. These collection depths can be used to predict the SRAM detector response to proton produced ionization in space. The SRAM cross section is larger for Rutherford scattering than for direct ionization. Rutherford scattering charge is collected from very deep in the SRAM substrate.

VI. ACKNOWLEDGMENT

The authors are indebted to the USC/ISI/MOSIS project for the fabrication of the test SRAMs used in this study. And to Alen Rice at the Caltech Tandem Van de Graaff for his assistance in performing the proton experiments. The research described was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration.

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CRRES MICROELECTRONIC TEST CHIP ORBITAL DATA II

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ABSTRACT

Data from a MOSFET matrix on two JPL CRRES chips, each behind different amounts of shielding, is presented. Space damage factors are nearly identical to ground test values for pMOSFETs. The results from neighboring rows of MOSFETs show similar radiation degradation. The SRD (Space Radiation Dosimeter) is used to measure the total dose accumulated by the JPL chips. A parameter extraction algorithm that does not underestimate threshold voltage shifts is used. Temperature effects are removed from the MOSFET data.

INTRODUCTION

The MEP (microelectronics package) of the CRRES (Combined Release and Radiation Effects Satellite) included 12 custom JPL test chips [1]. The chip layout, identifying the MOSFET matrix, is shown in Figure 1. This paper presents MOSFET matrix data on chip A3, located on the MEP outer board, and chip B4, located on the MEP middle board. The middle board is located behind the outer board which shields chip B4.

The MOSFET matrix layout is shown in Figure 2. Each row is identical, except for the two field oxide devices in row one, and each pair of columns contains a different size transistor. The drawn transistor width and length, W/L, in micrometers and the channel type, n or p, are shown in Figure 2. Neighboring rows of transistors, of the same size and in the same column, show nearly identical radiation degradation. Data is presented from orbits 500 to 700, with a major solar flare occurring at orbit 596 on March 23, 1991. Space pMOSFET damage factors nearly equal ground test values and their threshold voltages track SRD (Space Radiation Dosimeter) total radiation dose through the flare.

The on-chip MOSFET matrix cell addressing circuitry is shown in Figure 3 [1]. This addressing circuitry is controlled by digital signals coming from the row and column decoders and works without effecting MOSFET measurements, even when considerable radiation degradation occurs [2]. In this experiment the pMOSFET matrix failed at 60 krad.

These, and earlier results [3], based on radiation-induced threshold voltage shifts, have laid the ground work for space experiments utilizing pMOSFETs as flight dosimeters. On-chip pMOSFET dosimeters will be flown on the JPL neural net and SRAM chips on the United Kingdom STRV (Space Technology Research Vehicle).

CRRES ENVIRONMENT

The CRRES was launched on July 25, 1990 into a 9 hour 50 minute 18.2° orbit with a 350 km perigee and 33,580 km apogee. The satellite experienced a major solar flare resulting in an increased dose rate to the CRRES chips after orbit 596.

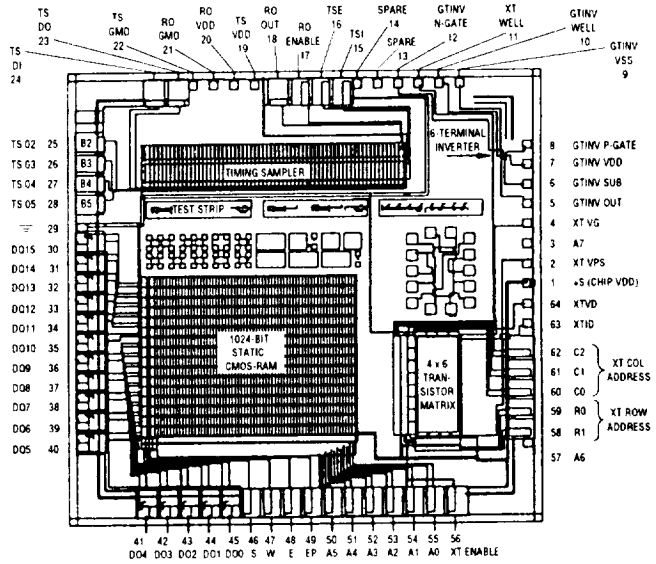

Figure 1. The JPL CRRES chip containing a MOSFET matrix, timing sampler, and 1k-bit SRAM.

The CRRES SRD (Space Radiation Dosimeter) [4] data was used to measure the total dose seen by the CRRES chips. The SRD consists of four silicon surface-barrier diode charge particle detectors, each shielded by an aluminium dome of a given thickness. In this paper SRD data from dome 2 was taken as representative of the dose for the middle board, and data from dome 1, for the outer board. The data is shown in Figures 4, and 5, respectively. The step increase in the dose shown in Figure 4 at orbit 590 identifies the solar proton flare and the increase beginning at orbit 596 is due to electron belt formation induced by the flare. The electron belt is responsible for the large increase in total dose observed by the SRD and the MOSFET matrix. The total dose curve slope in Figure 5 identifies four dose rate regions. Only two dose rate regions are identified in Figure 4.

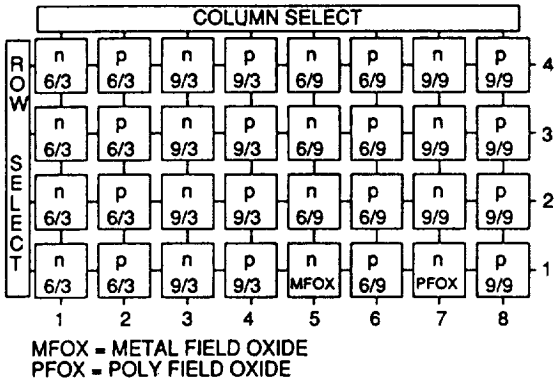

Figure 2. The MOSFET matrix layout showing the row and column placement, channel type (n or p), and transistor size (W/L) in μm/μm.

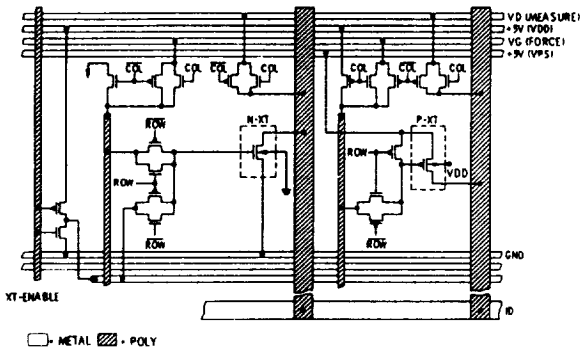

Figure 3. The MOSFET matrix cell layout showing digital switch addressing circuitry and the MOSFETs under test, N-XT and P-XT.

JPL CRRES CHIP

The CRRES chip was fabricated using a non-radiation hard 3-μm CMOS/bulk p-well process with a gate oxide thickness of 500 Å (50 nm). As shown in Figure 1, each CRRES chip in the MEP contains: (a) a MOSFET Matrix with 32 addressable MOSFETs for characterizing the effects of total dose on MOSFET parameters [1], (b) a Timing Sampler for measuring radiation-induced degradation of signal propagation delay, and (c) a 1k-bit SRAM for evaluating SEUs. This paper presents results from only the MOSFET matrix.

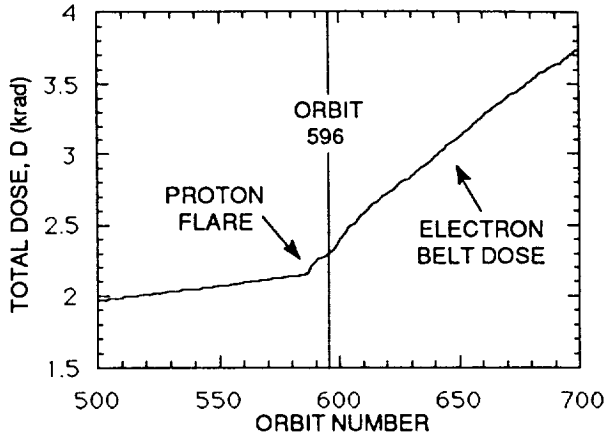

Figure 4. CRRES MEP middle board dose as measured by the SRD 232.5 mil (5.906 mm) Al dome number two.

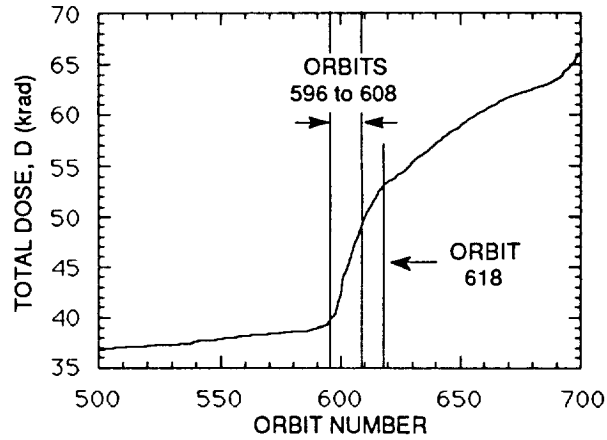

Figure 5. CRRES MEP outer board dose as measured by the SRD 82.5 mil (2.096 mm) Al dome number one. Four dose rate regions are identified by the total dose curve slope.

A total of 120 IV data points where measured per transistor. This extensive collection of MOSFET data allows the radiation effects evaluation of critical MOSFET parameters and represents a first attempt at acquiring MOSFET curve-tracer data from space. The MOSFETs were biased in the OFF state when not being measured, which is the worst case bias condition [5]. ID was measured for 10 settings of VD and 12 settings of VG. The measurement resolution for VDD is 5 V ±2%, VDS, and VGS ranges from 0 to 5 V ± 1mV, and IDS from 2 nA to 1mA ±0.5%. If the measured current is less or equal to 1 nA then it is set to 1 nA [6]. In order to reveal spurious data, MOSFET I-V curves were plotted every 100 orbits in the linear, saturation, and subthreshold regions. This paper presents results taken from the saturation region for orbits 500 to 700.

EXPERIMENT RESULTS

Threshold voltage damage factors, threshold voltage shifts, and channel mobility degradations are evaluated over orbits 500 to 700 on MOSFET matrix transistors located on two CRRES chips. Chip A3(00) is located on the outer board and chip B4(03) is located on the middle board. Figure 6 shows a damage factor measurement on device 00VP12, which is on chip (00), is a threshold voltage damage factor on a pMOSFET (VP), and is located in row 1 at column 2 (12) in the MOSFET matrix. This matrix location has a W/L of 6/3 μm/μm as shown in Figure 2. Orbits 596 to 608, shown in Figure 6, are defined by the low data density caused by the high dose rate region shown in Figure 5. The absolute value of threshold voltage in Figure 6 allows pMOSFET values to be plotted as positive numbers.

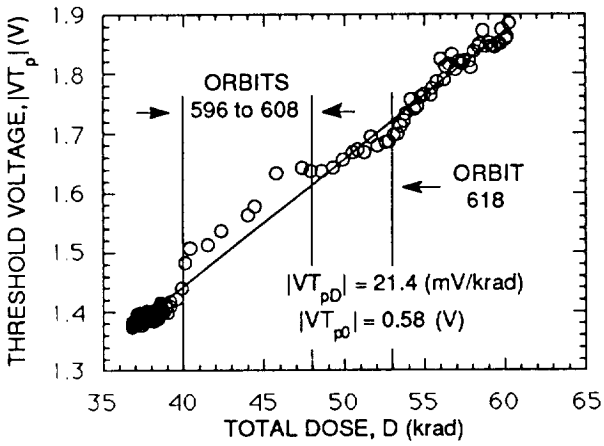

Figure 6. Outer board damage factor measured over orbits 500 to 660 on MOSFET 00VP12. The data density identifies the four dose rate regions shown in Figure 5. The space damage factor, |VTpD|, is very close to the ground test value of 21.7 mV/krad.

The pMOSFET damage factor, $|VT_{pD}| = 21.4$ mV/krad, is very close to the Co-60 ground test value of 21.7 mV/krad [1]. The zero dose threshold voltage, $|VT_{p0}|$, is very close to the value, 0.56 V, measured during the first few orbits. A damage factor of 22 mV/krad was previously measured over the first 200 orbits using the SRD to measure the dose [6]. The space and ground measured pMOSFET damage factors are nearly equivalent because the threshold voltages track the total dose as shown in Figure 7 for device 00VP12. Figure 8 compares the SRD measured dose to the 00VP12 MOSFET measured dose, using the ground measured damage factor of 21.7 mV/krad. The MOSFET curves in Figures 7 and 8 are nearly identical. The value of presenting pMOSFET data, as dosimeter data, as shown in Figure 8, is recognized by its ability to explain the anonymously high damage factor shown in Figure 9.

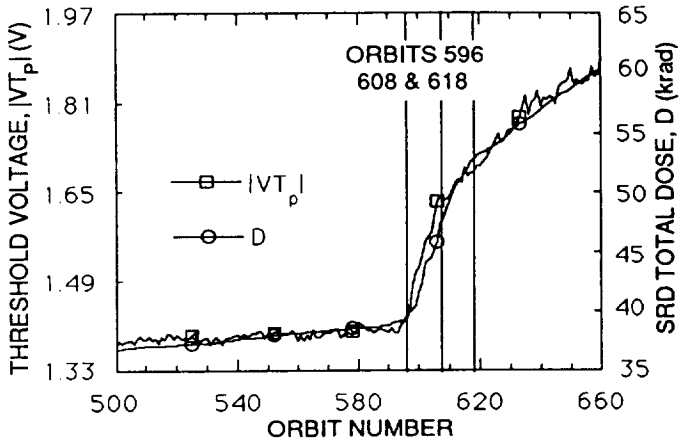

Figure 7. The pMOSFET 00VP12 threshold voltage tracks the SRD dome 1 total dose through the solar flare. The pMOSFET threshold voltage was scaled to dose using $|VT_{pD}| = 21.4$ mV/krad and $|VT_{p0}| = 0.58$V shown in Figure 6.

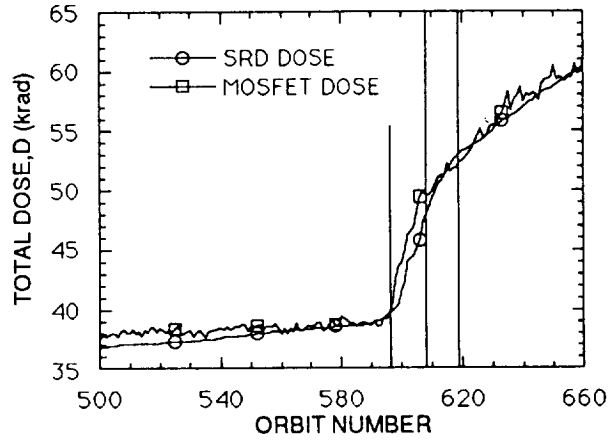

Figure 8. The pMOSFET 00VP12 dose and SRD dome 1 dose versus orbit number. The pMOSFET dose was derived from its threshold voltage scaled to dose via the ground test damage factor of 21.7 mV/krad and $|VT_{p0}| = 0.56$ V.

The pMOSFET $|VT_p|$ values plotted in Figures 7 and 8 are temperature corrected [6], and scaled to dose using the following equation:

$$|VT_p| = |VT_{p0}| + |VT_{pD}| \cdot D \qquad (1)$$

where the damage factor is given by:

$$VT_{pD} = \frac{\partial VTp(D)}{\partial D} \qquad (2)$$

In Figure 7, D is the SRD dose. The pMOSFET threshold voltages were converted to dose using the SRD dose and $|VT_{pD}|$, and $|VT_{p0}|$ from Figure 6. In Figure 8, D is computed

from Equation 1 using (a) the pMOSFET threshold voltages, (b) $|VT_{pD}|$ = 21.7 mV/krad derived from Co-60 ground test [1], and (c) $|VT_{p0}|$ = 0.56 V measured during the first few CRRES orbits.

This data indicates that pMOSFETs used as on-chip dosimeters are capable of tracking the high dose rates induced by large solar flares. The outer board data is truncated at orbit 660 due to MOSFET failure at 62 krad. The pMOSFET is a good dosimeter right up to its catastrophic failure dose.

Figure 9 shows a threshold voltage damage factor measurement on device 03VP22. This pMOSFET is located on the middle board in row 2 and column 2. The space measured damage factor of 25.6 mV/krad is too large because of a dose rate region mismatch between the SRD and the MOSFET shown in Figure 10. The ground test measured damage factor of $|VT_{pD}|$ = 21.7 mV/krad, $|VT_{p0}|$ = 0.55 V measured during the first few CRRES orbits, and Equation 1 are used to compute the MOSFET dose shown in Figure 10. The high dose rate region between orbits 596 and 618, shown in Figure 10, increases the damage factor fit line slope shown in Figure 9. The mismatch is due to the low quality of the shielding over the middle board. The shield quality is a function of the uniformity of its thickness and density. The middle board is shielded by the outer board; whereas, the SRD is shielded by the high quality aluminum dome. Gaps in the outer board shield allowed more electrons to penetrate creating the high dose rate region between orbits 596 and 618 at the middle board, as shown in Figure 10.

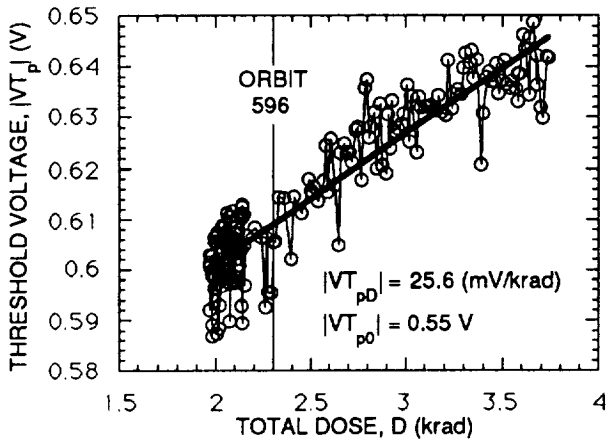

Figure 9. Middle board device 03VP22 measured over orbits 500 to 700. The SRD dome 2, shown in Figure 4, is used for total dose. The damage factor is high because of low quality shielding over the middle board.

MOSFET data on the middle and outer boards is used to compute damage factors for W/L = 6/3 μm/μm for both n and pMOSFETs in matrix rows 2 and 3. The damage factors are shown in Figure 11. The pMOSFET values were very close to the ground test measured value of 21.7 mV/krad. The ground test measured value of - 37.9 mV/krad for the nMOSFETs is greater than the space measured value, - 9.4 mV/krad, because of nMOSFET annealing.

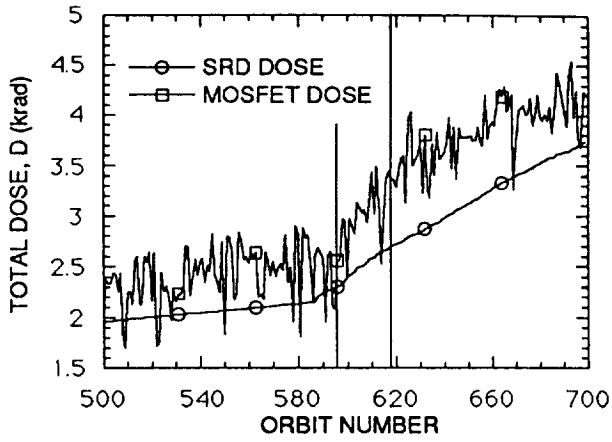

Figure 10. Dose measured by MOSFET 03VP22 using the ground test damage factor of $|VT_{pD}|$ =21.7 mV/krad and $|VT_{p0}|$ = 0.55 V. The MOSFET dose identifies a third dose rate region between orbits 596 and 618 that is not shown by the SRD dose.

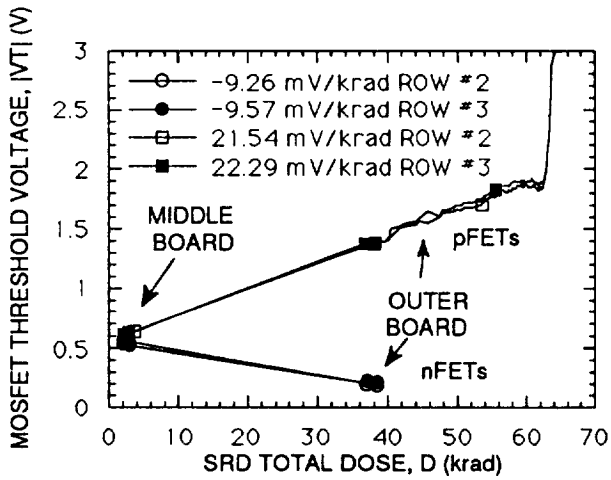

Figure 11. Linear fits used to compute damage factors for MOSFETs on the middle and outer boards. The pMOSFET damage factors are very close to the ground test value of 21.7 mV/krad. The MOSFET W/L = 6/3.

The MOSFETs located in neighboring matrix rows show nearly identical radiation degradation. The pMOSFETs fail at 62 krad, as shown in Figure 11, and the nMOSFETs fail at 39.5 krad at orbit 597. The pMOSFET failure curve shown in Figure 11 above 62 krad is not included in the damage factor linear fit.

All of the data presented up to this point represents equivalent geometry MOSFETs with a W/L of 6/3. Other W/L

values, for the middle board 03 chip, are shown in Figure 12. This data shows that equivalent geometry pMOSFETs experience similar radiation degradation by comparing devices from neighboring matrix rows.

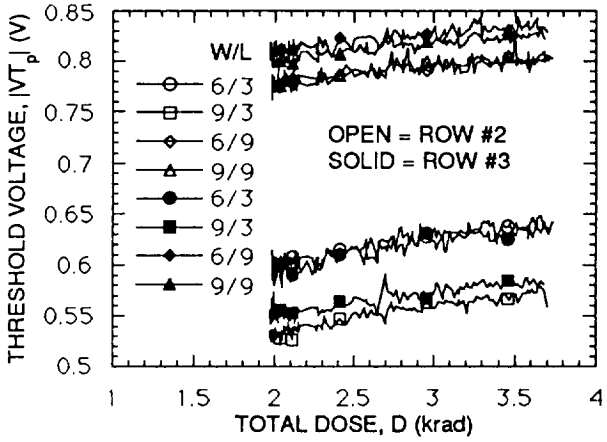

Figure 12. Middle board data showing that equivalent geometry pMOSFETs experience similar radiation degradation.

MOSFET ANALYSIS

A simple model was used to extract the threshold voltage, VT, and mobility, μ, from the saturation region of the MOSFET using the largest VD for both n- and p-channels. In the saturation region the drain current is given by,

$$ID = \frac{\beta\,(VG - VT)^2}{2\,(1+\theta\,(VG - VT))} \tag{3}$$

and

$$\beta = \frac{KP \bullet W}{L} \tag{4}$$

where ß is the channel conduction factor, $KP=\mu C'_{ox}$ is the intrinsic conduction factor, and μ is the channel mobility. C'_{ox} is the gate oxide per unit area, θ is the mobility degradation factor and W and L are the as-drawn channel width and length respectively. The mobility degradation is caused by an increase in the carrier mean-free-path due to the vertical electrical field produced by the gate voltage [7]. This degradation decreases the rate of increase in the drain current with increasing gate voltage as shown in Figure 13.

Applying the Taylor series approximation,

$$\frac{1}{\sqrt{1+\theta VG}} = 1 - \frac{\theta}{2}VG \tag{5}$$

and letting θ • VT terms vanish, a linear equation is derived for the square root of the drain current.

$$\sqrt{ID} = \sqrt{\frac{\beta}{2}}\,(-VT + VG - \frac{\theta}{2}VG^2) \tag{6}$$

This equation is used to fit the IV data as shown in Figure 13.

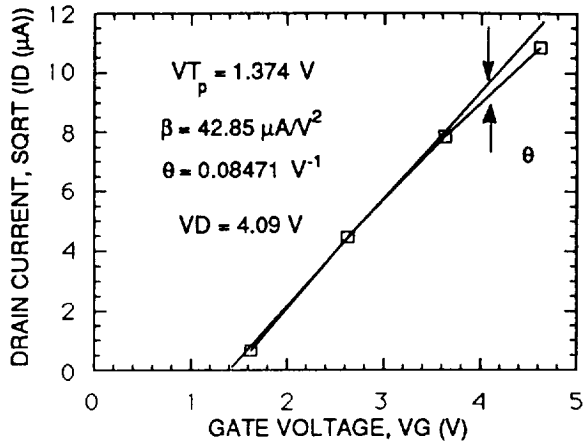

Figure 13. Values for 00P12 (chip A3(00), p-MOSFET, row 1, column 2) at orbit 500. The absolute value symbols are not shown.

The temperature coefficients for the threshold voltage and channel mobility are given by,

$$VT_T = \frac{\partial VT(T)}{\partial T} \tag{7}$$

$$\mu(T)=\mu(T_O)\left(\frac{T}{T_O}\right)^n \tag{8}$$

where the values, VT_T=-2 mV/°C for n-channels, -1 mV /°C for p-channels and the n-factor in Equation 8 is equal to -1.2. These equations are used to remove the 35 orbit temperature periodicity, shown in Figure 14, from the MOSFET data [6].

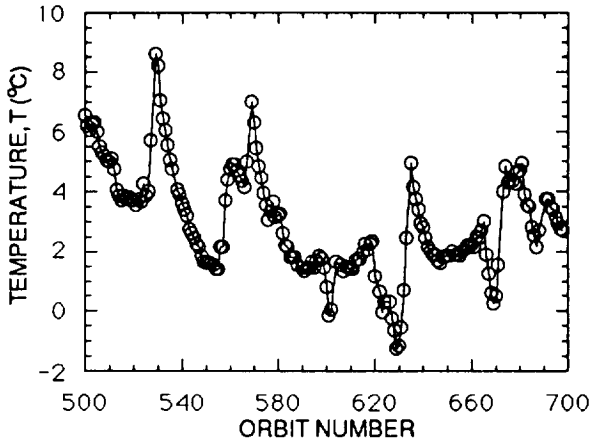

Figure 14. Temperature measured on the outer board from orbit 500 to 700 showing a 35 orbit periodicity.

CONCLUSIONS

This experiment demonstrated the ability to obtain curve-tracer type transistor data from a spacecraft environment. The pMOSFET threshold voltages track total radiation dose and their damage factors are very close to the ground test value. This allows pMOSFETs to be used as on-chip radiation dosimeters. Equivalent geometry MOSFETs located in neighboring matrix rows experience nearly identical radiation degradation. Equivalent geometry MOSFETs located on different chips, under different amounts of shielding, have nearly identical damage factors. The pMOSFETs accurately measure total dose right up to catastrophic matrix failure. The nMOSFETs show annealing effects and failed at the solar flare onset.

ACKNOWLEDGEMENTS

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STRV RADMON: AN INTEGRATED HIGH-ENERGY PARTICLE DETECTOR

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The RADMON (Radiation Monitor) was developed as a compact device with a 4-kbit SRAM particle detector and two p-FET total dose monitors. Thus it can be used as a spacecraft radiation alarm and in situ total dose monitor. This paper discusses the design and calibration of the SRAM for proton, alpha, and heavy ion detection. Upset rates for the RADMON, based on a newly developed space particle flux algorithm, are shown to vary over eight orders of magnitude. On the STRV (Space Technology Research Vehicle) the RADMON's SRAM will be used to detect trapped protons, solar flares, and cosmic rays and to evaluate our ability to predict space results from ground tests.

1. MISSION OVERVIEW

The STRV (Space-Technology Research Vehicle) consists of two spacecrafts as shown in Figure 1. Each vehicle is approximately a cube 44 cm (17 in.) on a side that will be launched into a geosynchronous transfer orbit (GTO) with 200-km perigee, a 36,000-km apogee, and an 11-hour period. This orbit provides the opportunity to profile the Earth's radiation belts.

The STRV contains a number of radiation measuring instruments including the JPL RADMON (Radiation Monitor), the DRA CREDO (Cosmic Environment Dosimeter), and the ESA REM (Radiation Environment Monitor). The CREDO and REM use PIN diodes or surface barrier (SB) detectors with pulse-height detection circuitry to discriminate particle energy. The area of the CREDO and REM detectors is between 22 to 400 mm^2; whereas, the area of the RADMON is only 0.17 mm^2. Thus the upset rates are much higher for the CREDO and REM than for the RADMON.

The purpose of this paper is to present the methodology for calculating the RADMON's upset rate using a newly developed algorithm for the space environment and the RADMON's device parameters. After launch, the upset rate for the CREDO, REM and RADMON will be compared to determine the validity of the ground predictions and the relative sensitivity of the three particle detectors.

The space particles relevant to RADMON upsets are: (a) trapped protons (TP), (b) galactic cosmic rays (GCRs), and (c) solar flare particles (SFP). Electrons in the electron belt will not upset the RADMON. Electrons provide a total dose which causes a slow drift in the RADMON baseline which is constantly monitored.

2. SEU SRAM

The RADMON, shown in Fig. 2, is a 28-pin chip with a 4-kbit SRAM for SEU (single-event upset) detection and two p-FETs [1] for total dose monitoring. The SRAM contains a six-transistor memory cell which is illustrated in the schematic cross section of Fig. 3. This figure shows that the memory cell has been modified in two ways to increase the cell's sensitivity to upsets. First, the drain area, σ_m, of diode Dn2 has been increased to increase its particle capture cross section. Second, the diode Dn2 is biased with an offset voltage, V_o, which is applied through p-FET Mp2. This allows the cell to be operated near its metastable point which in turn allows the cell's upset sensitivity be adjusted via V_o.

The interaction of high-energy particles with the RADMON is described in terms of the various layers the particle passes through as seen in Fig.4. In passing through the layers, the particle loses energy and in general increases its LET (linear energy transfer) or its ability to deposit charge. Thus knowing the thickness of the shield and device overlayer is key to calculating particle upset rates.

The response of the RADMON to protons is illustrated in Fig. 5 where 0.55, 1.0, and 2.0 MeV protons upset the cells. The figure also includes the spontaneous upset curve which has a mean value of $V_{os\mu}$. The spontaneous curve defines the metastable point for each of the SRAM cells. This curve represents the baseline for the device.

In operation the RADMON is operated at a V_o greater than $V_{os\mu}$ or $\delta V_o = V_{op\mu} - V_{os\mu}$ where $V_{op\mu}$ is the mean particle offset voltage defined by the $\sigma_m/2$ crossing point shown in Fig. 5. For the STRV, the RADMON is operated with three δV_o values corresponding to a proton threshold, an alpha particle threshold, and a heavy ion threshold. These thresholds are listed in Table 1.

The vertical axis of Fig. 5 displays the particle cross section. It is calculated using:

$$(1) \quad \sigma = N/(\phi_m \cdot t_m \cdot N_t)$$

where ϕ_m is the measured particle flux, t_m is the measurement time, and N_t is the number of bits in the SRAM in this case $N_t = 4096$. This equation is applicable for $N \ll N_t$ which is satisfied when the number of flipped bits is less than 10 percent of N_t. This equation indicates that the cross section is proportional to the number of flipped bits, N. The proportionality factor, the denominator, normalizes the data with respect to flux and measurement time.

In order to predict the RADMON's upset rate, σ_m, δQ_c, and $\delta X4$ must be known. The device cross section is taken from the physical layout and in this case $\sigma_m = 42.1$ μm^2. The critical charge is related to V_o through:

$$(2) \quad \delta Q_c = C_u \cdot \delta V_o$$

where C_u is the upset capacitance. The collection depth, $\delta X4$, is shown in Fig. 3. Both C_u and $\delta X4$ are determined experimentally and in this discussion $C_u = 28.9$ fC/V and $\delta X4 = 2$ μm are used.

The RADMON's proton response, shown in Fig. 5, reveals a non-monotonic behavior between the particle energy and δV_o. This behavior is explained by analyzing the proton charge depth curves [2] shown in Fig. 6. The vertical lines indicate the

width of the overlayer and the width of the collection depth; that is, δX_3 = 5.6 μm and δX_4 = 2 μm. The figure shows that the 0.55 MeV proton stops in δX_4 and the 1.0 and 2.0 MeV protons stop beyond δX_4. The 0.2 MeV proton stops in the overlayer so it can not be detected. The explanation for the non-monotonic energy versus δV_0 behavior follows from the charge deposited in the collection layer, δQ_c, as indicated in Fig. 6. This charge is proportional to δV_0 as given in Eq. 2 and thus explains the non-monotonic behavior.

It is concluded that the SRAM detects protons in the 0.5 to 2.0 MeV range. Higher energy protons can be detected only if their energy is brought in to the detection range by using a shield which drops the proton energy into the 0.5 to 2.0 MeV energy range. The STRV contains 16 RADMONs; half are shielded by a 2.0-mm Al shield and the other half are shielded by a 5.5-mm Al shield. The effect of shielding on the detection of protons is discussed in a later section.

3. GALACTIC COSMIC RAY AND SOLAR FLARE PARTICLE UPSETS:

Galactic cosmic ray (GCR) and solar flare particle (SFP) upsets are illustrated in Fig. 7. These curves were obtained by fitting Adam's curves [3]; the GCR are for solar minimum conditions. The curves show that shielding has a significant effect on the SFPs but relatively little effect on the GCRs.

The number of upsets per SRAM is given by:

$$(3)\quad U = N \cdot \Omega \cdot t \cdot \sigma_m \cdot F$$

where N is the number of bits per SRAM, Ω is the solid angle, t is the observation or stare time, σ_m is the area sensitive to upsets, and F is the integral particle flux. The Petersen Equation [4] is commonly used to calculate SRAM upsets. The flux expression is:

$$(4)\quad F(1/\mu m^2 \cdot ster \cdot sec) = 4.4 \times 10^{-12} / [L(MeV \cdot cm^2/mg)]^2$$

where L is the linear energy transfer. The conversion factor for L in silicon is $L(MeV \cdot cm^2/mg) = L(fC/\mu m)/10.25$ where $L(fC/\mu m) = \delta Q_c(fC)/\delta X_4(\mu m)$. The Petersen equation holds for a 0.63-mm Al shield in a 10 percent worse case environment (10%WC).

The effect of shielding on the particle flux was obtained by fitting the Adam's data [3]. The flux is:

$$(5)\quad F(1/\mu m^2 \cdot ster \cdot sec) = F_0 \cdot (L/L_0)^{a+b \cdot LOG(1+D/Do)}$$

where D is the shielding thickness in g/cm^2. The shielding thickness is given by $\delta X1 = D/\rho$ where ρ is the shield density in g/cm^2. The values for F_0, L_0, a, and b are listed in Table 2.

The upsets expected for the RADMON are shown in Fig. 8 where the three LET thresholds are labeled. For the SFPs the RADMON will experience numerous upsets during the 600 sec stare time. For the GCRs, the RADMON will experience less than one upset per 600 sec stare time. The results are summarized in Table 1.

4. PROTON BELT UPSETS:

The profile of the proton belt is shown in Fig. 9. It shows that the STRV remains in the vicinity of proton belt peak for several hundred seconds. Before reaching the RADMON the protons must pass through the Al shields. From the proton range curves [2], it can be shown that the protons must have $E_0 > 18.5$ MeV to pass through a 2.0-mm Al shield and $E_0 > 32.5$ MeV to pass through a 5.5-mm Al shield. The proton energy must be lowered by the shield so that it has an energy between 0.5 and 2.0 MeV when it enters the RADMON's collection in order to be detected. This effect is shown graphically in Fig. 10 where two solid horizontal lines have been drawn at the bounds of the RADMON's detection range. The problem now is to determine δE_0, the incremental incident proton energy that can be detected by the RADMON.

The number of protons that upset the RADMON during the stare time, t, is:

$$(6) \quad N = \sigma_m \cdot \phi_d \cdot t \cdot N_t \cdot \delta E_0$$

where ϕ_d is the differential incident proton flux which is determined from the peak of the proton belt curves shown in Fig. 9. For $E_0 < 30$ MeV, $\phi_d = 600$ $p/(cm^2 \cdot sec \cdot MeV)$ and for $E_0 > 30$ MeV, $\phi_d = 200$ $p/(cm^2 \cdot sec \cdot MeV)$. The δE_0 is given by:

$$(7) \quad \delta E_0 = (dE_0/dE_1)\delta E_1$$

where δE_1 is the incremental exit proton energy. The dE_0/dE_1 is determined from the proton range curves shown in Fig. 10 where $dE_0/dE_1 = 0.36$ for both the 2.0- and 5.5-mm Al shields.

A value for δE_1 is obtained by assuming that most of the proton energy is lost in the shield and virtually none is lost in the chip overlayer. Thus $\delta E_1 = \delta E_2 = \delta E_3 = 2.0 - 0.5 = 1.5$ MeV. Using Eq. 7, $\delta E_0 = 0.54$ MeV for both Al shields. Thus the RADMON will detect protons through the 2.0-mm Al shield with $E_0 = 18.77 \pm 0.27$ MeV and through the 5.5-mm Al shield with $E_0 = 32.77 \pm 0.27$ MeV. This shows that the RADMON is really an energy detector for high-energy protons.

The number of trapped-proton induced upsets, calculated using Eq. 6, is listed in Table 3. It shows that several hundred upsets can be expected near the peak of the proton belt. The above calculation does not include particle scattering in the Al shield. Including this effect will increase the number of upsets.

5. DISCUSSION:

The number of upsets estimated for the RADMON varies over eight orders of magnitude and depends on the type of the space environment encountered. The upset estimates depend on the accuracy of the environmental models and device parameters such as the collection depth. A simple algorithm was developed for estimating space particle flux that includes the effect of shielding. The flight of the RADMON on the STRV along with the CREDO and REM will provide data to quantify the sensitivity of the three particle detectors and validate ground predictions.

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7. ACKNOWLEDGMENTS: The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Ballistic Missile and Defense Organization, Innovative Science and Technology Office. The RADMONs were fabricated through MOSIS, ISI, USC. The authors are indebted to E. J. Daly, ESA, for the data shown in Fig. 9 and for his observation that the RADMON detects high-energy protons that fall in a narrow band of energies. File: STRV3B04.DOC.

Table 1. RADMON Particle Thresholds and LETs.

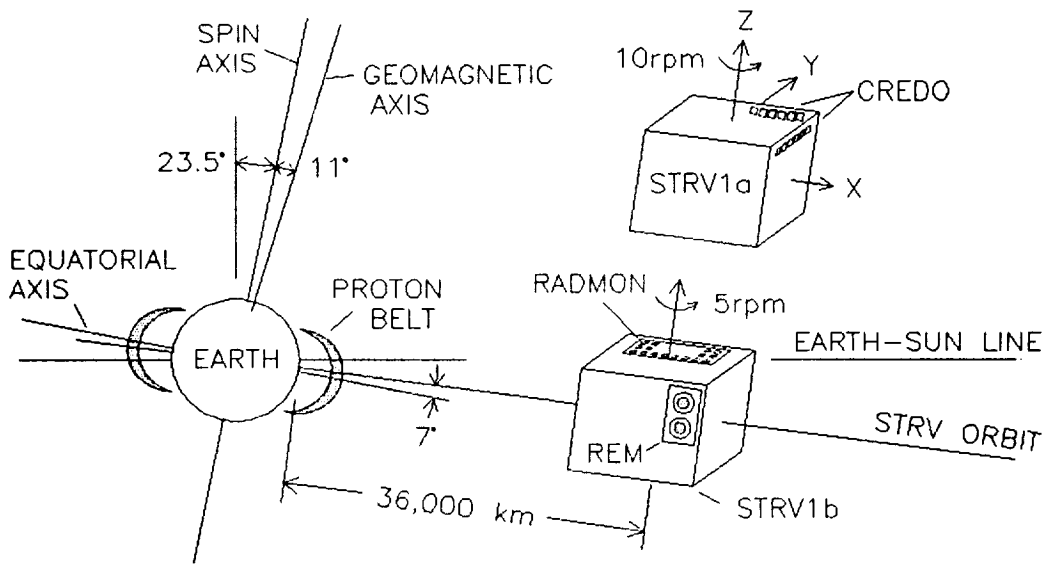
THRESHOLD	VDD V	Vosμ V	δV_o V	LET$_2$ MeV·cm^2/mg
PROTON	3	1.139	0.61	0.086
ALPHA	3	1.139	0.250	0.353
HEAVY	5	1.720	3.280	4.628

Table 2. GCR and LSF Flux Parameters

PARAMETER	UNITS	GCR	LSF
F_o	1/(μm^2·ster·sec)	1x10^{-5}	1x10^{-2}
L_o	MeV·cm^2/mg	1x10^{-4}	1x10^{-3}
D_o	mg/cm^2	78.36	0.5990
a	unitless	-1.92	-1.425
b	unitless	-1.35	-0.974

Table 3. RADMON Anticipated Upset Rates

ENVIRONMENT	PROTON BELT U(upsets/SRAM)	SOLAR FLARE U(upsets/SRAM)	10% WORSE CASE U(upsets/SRAM)	GCR U(upsets/SRAM)
Al-SHIELD	2.0-mm 5.5-mm	2.0-mm 5.5-mm	0.63-mm	2.0-mm 5.5-mm
PROTON	3.3E+2 1.1E+2	1.7E+3 5.4E+2	1.93E-1	7.5E-3 7.2E-3
ALPHA		1.5E+2 3.5E+1	1.15E-2	5.0E-4 4.7E-4
HEAVY		2.0E+0 2.3E-1	6.68E-5	3.6E-6 3.3E-6



EARTH RADIUS = 6371 km
PERIGEE = 200 km
APOGEE = 36,000 km
STRV2A27.PLT

Figure 1. STRV orbit relative to the earth's proton belt.

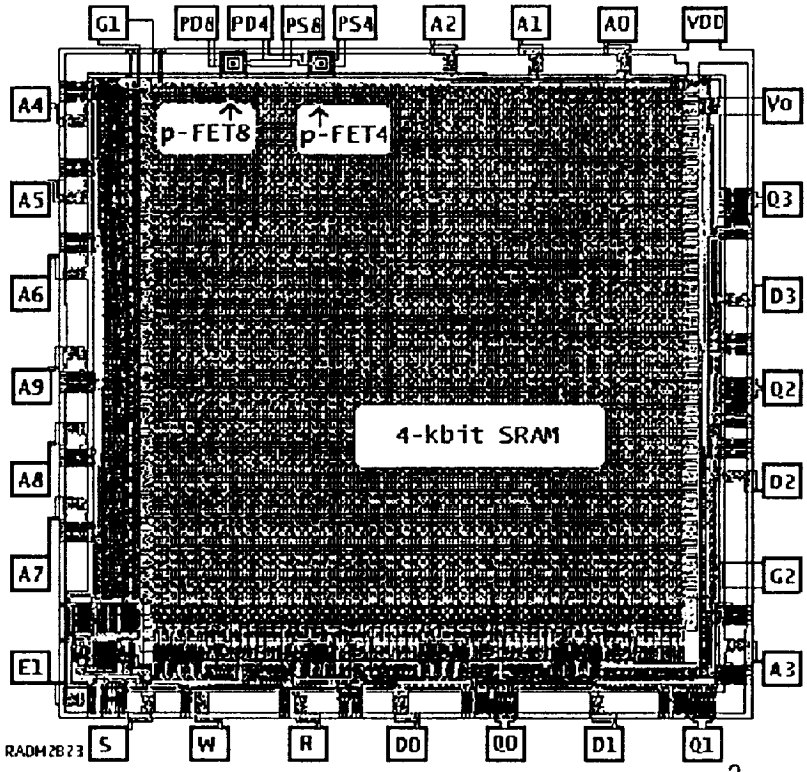


Figure 2. STRV-RADMON chip 2.57 x 2.70 mm^2.

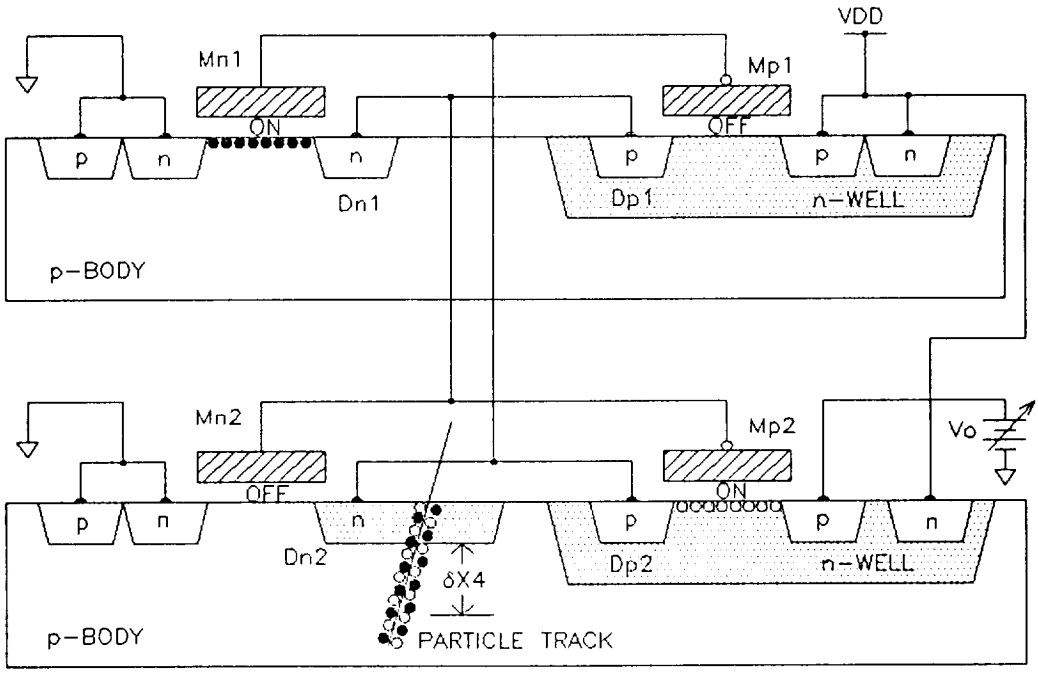


Figure 3. Cross section of SEU-SRAM showing a particle track through diode Dn2 which can cause a bit flip if sufficient charge is deposited.

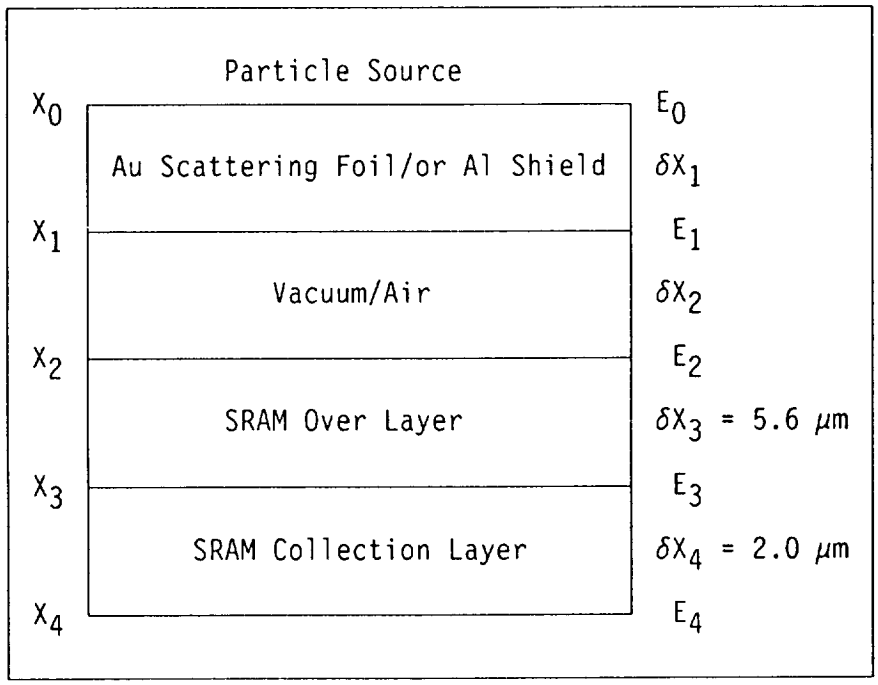


Figure 4. Schematic view of the particle path from the source to the SRAM.

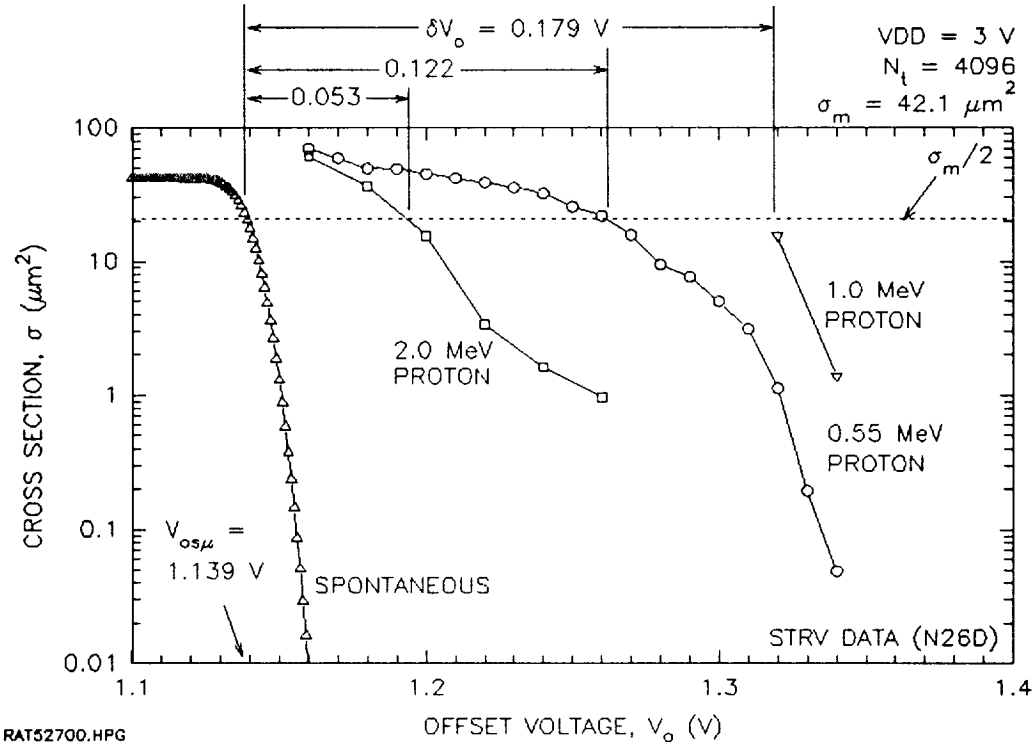


Figure 5. SRAM cross section/bit for protons with three different incident energies ($E_1 = E_2$).

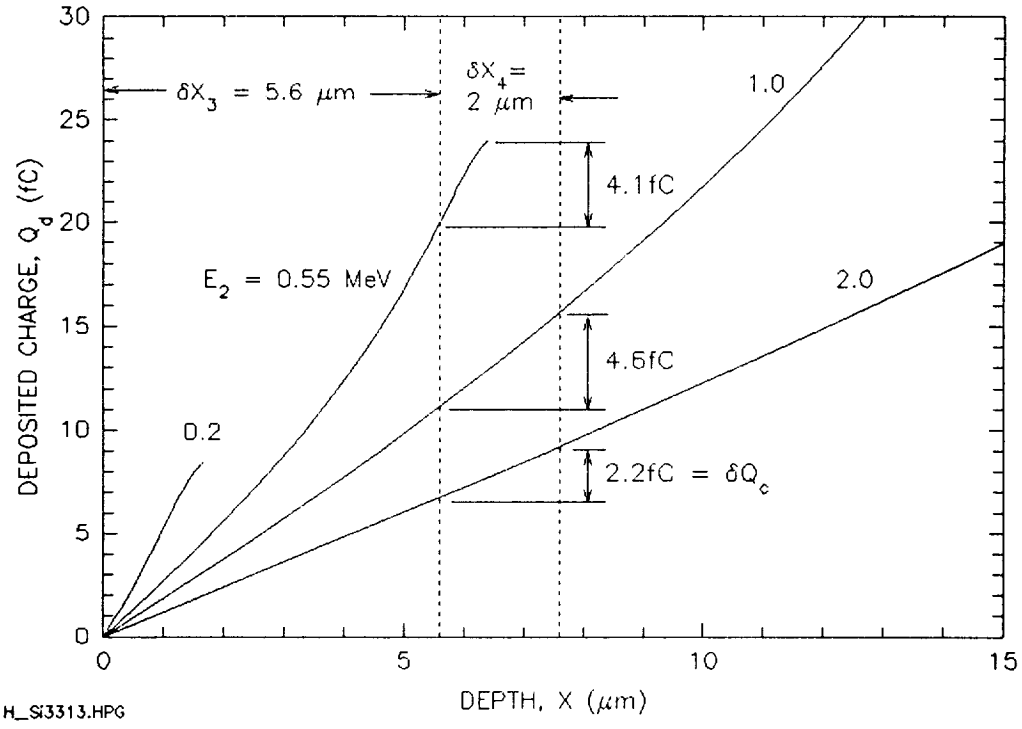


Figure 6. Proton charge deposited in silicon [2].

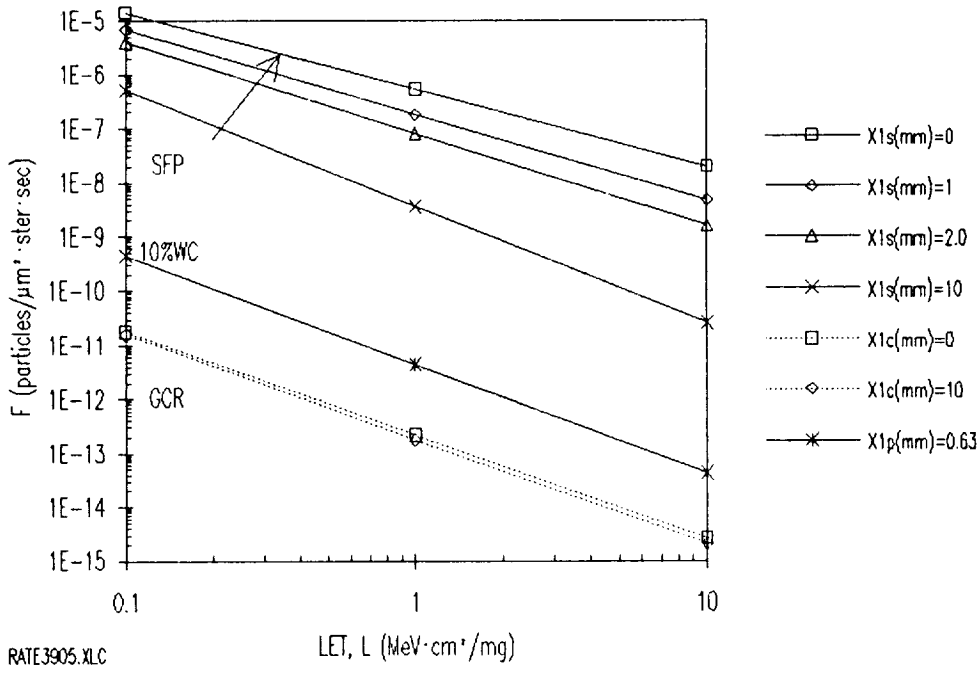


Figure 7. Integral LET interplanetary spectra for various aluminum shields [3] due to galactic cosmic rays (GCR), 10 percent worse case environment (10%WC), and solar flare particles (SFP).

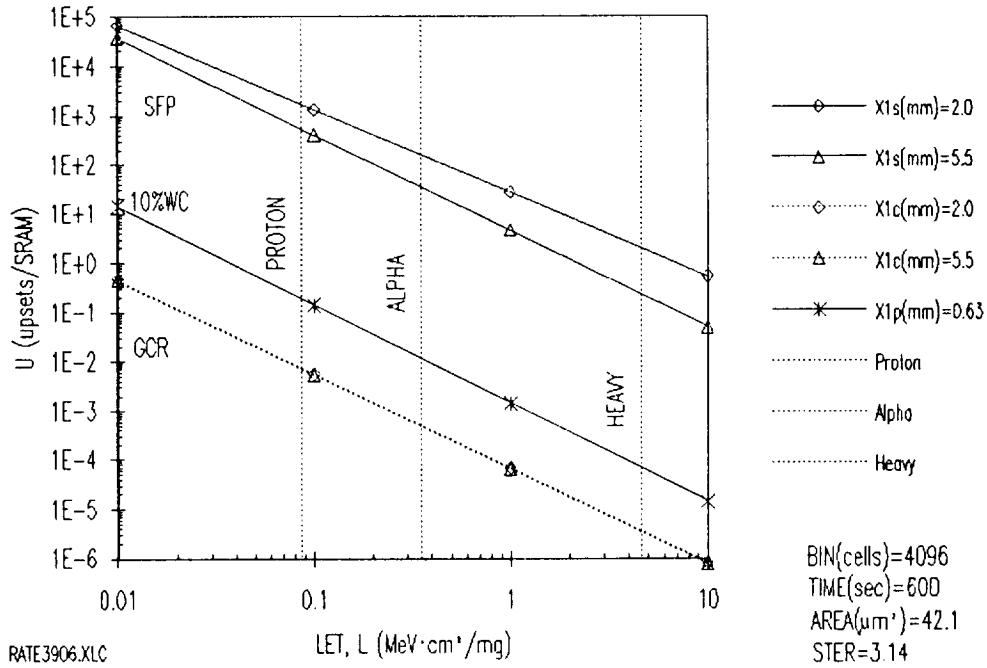


Figure 8. STRV RADMON SEU SRAM upset rate due to galactic cosmic rays (GCR), 10 percent worse case environment (10%WC), and solar flare particles (SFP).

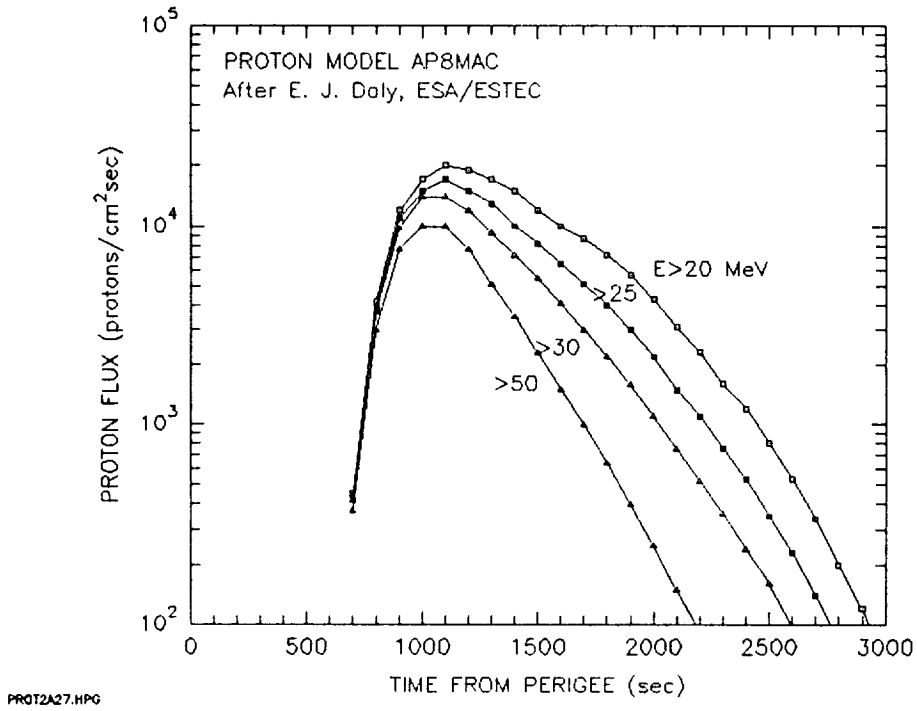


Figure 9. STRV traverse of the earth's proton belt.

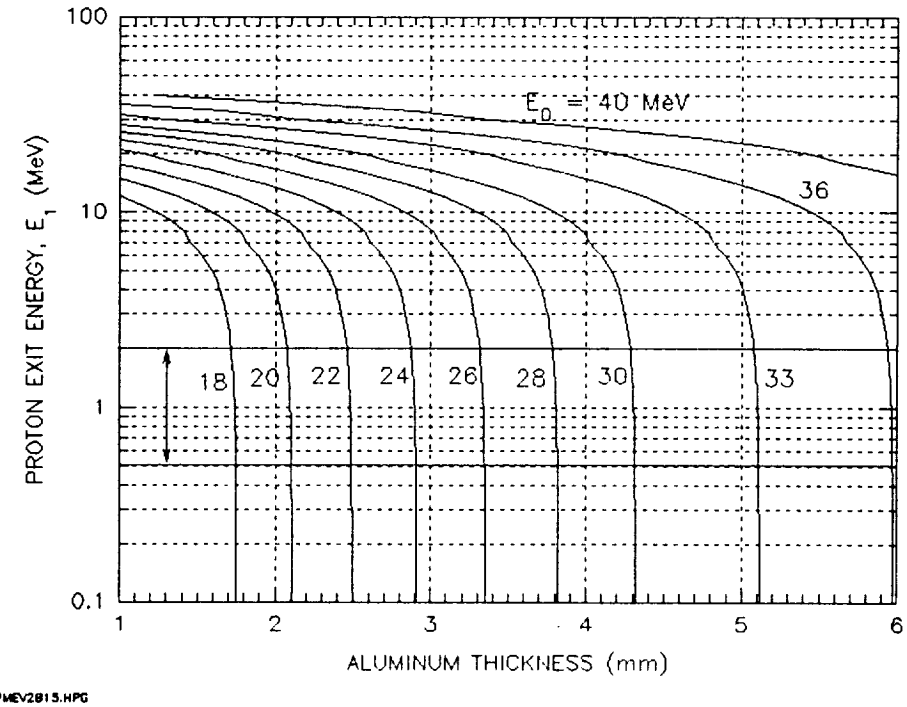


Figure 10. Proton exit energies for various aluminum thickness and incident proton energies. For X_{Al} = 2 mm, E_0 ≈ 20 MeV and for X_{Al} = 5.5 mm, E_0 ≈ 35 MeV.

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ON-CHIP p-MOSFET DOSIMETRY

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ABSTRACT

On-chip p-FETs were developed to monitor the radiation dose of n-well CMOS ICs by monitoring threshold voltage shifts due to radiation induced oxide and interface charge. The design employs closed geometry FETs and a zero-biased n-well to eliminate leakage currents. The FETs are operated using a constant current chosen to greatly reduce the FET's temperature sensitivity. The dose sensitivity of these p-FETs is about -2.6 mV/krad(Si) and the off-chip instrumentation resolves about 400 rad(Si)/bit. When operated with a current at the temperature-independent point, it was discovered that the pre-irradiation output voltage is about -1.5 V which depends only on design-independent silicon material parameters. The temperature sensitivity is less than 63 µV/°C over a 70°C temperature range centered about the temperature insensitive point.

1. INTRODUCTION

The use of FETs (Field-Effect Transistors) as dosimeters was pioneered by Holmes-Siedle [1]. A number of these devices have flown on Earth-orbiting satellites [2-4].

In recent years, p-FET dosimeters have been developed with specially-grown thick-gate oxides which have a large number of oxide traps. Sensitivities of >10 mV/rad(Si) [5] have been achieved. The sensitivity to radiation can be enhanced by applying a large positive bias during radiation which forces more of the positive oxide charge to the interface. The sensitivity to temperature can be minimized by operating the p-FET with a current at the temperature-independent point [6, 7].

In this work, a p-FET dosimeter is developed under the constraint that the dosimeter be useful in predicting the radiation dose of an IC fabricated with a non-radiation hardened 1.2-µm CMOS process. As shown in Fig. 1, two p-FETs were fabricated on the RADMON (Radiation Monitor), which also includes an SEU-SRAM for monitoring particle upsets. This appears to be the first time a p-FET dosimeter was fabricated in a fine-line, thin-oxide semiconductor technology.

The p-FET is biased to about -1.5 V during measurement and is unbiased when not being measured. This approach to biasing is intended to provide a known bias environment at all times. In certain applications, the availability of spacecraft power is unpredictable. Thus, being unbiased during irradiation provides a known bias scenario.

On-chip dosimetry provides the advantage that the dose is measured directly next to the IC. This reduces the uncertainty inherent in dosimetry calculations which are complicated especially for highly shielded electronics.

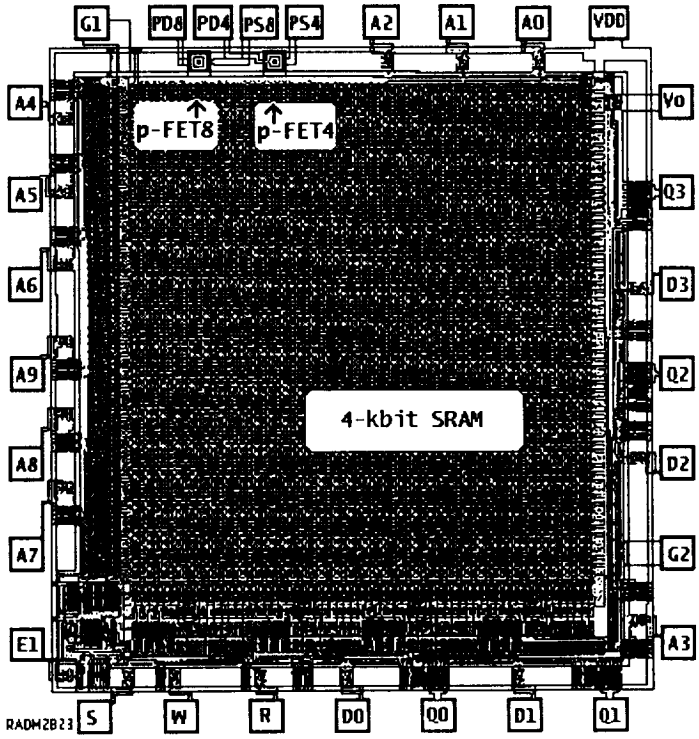

Figure 1. STRV-RADMON chip 2.6 mm x 2.7 mm.

2. p-FET DESIGN

The RADMON, shown in Fig. 1, contains two p-FETs. The geometry of p-FET4 is W/L = 182/4 µm/µm and p-FET8 is W/L = 182/8 µm/µm where W and L are the channel width and length,

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respectively. The layout of the p-FET, shown in Fig. 2, features a closed geometry design where the drain completely surrounds the source. The closed geometry eliminates the bird's beak or channel-edge leakage encountered in a linear FET.

The schematic cross section of the device, shown in Fig. 3, indicates that the n-well and source are separated so they can operate at slightly different biases required by the operational amplifier, U1. This allows all the forced current to flow through the p-FET channel. Drain-to-well leakage is shunted to ground. Grounding the n-well is a departure from normal CMOS circuit operation where the n-well is normally connected to VDD.

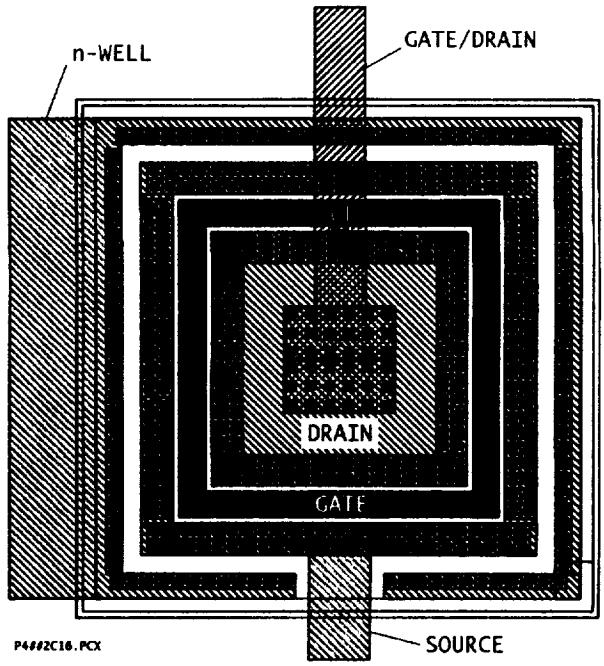

Figure 2. p-FET, MP4, layout where the gate length is L = 4 μm and width is W = 182 μm.

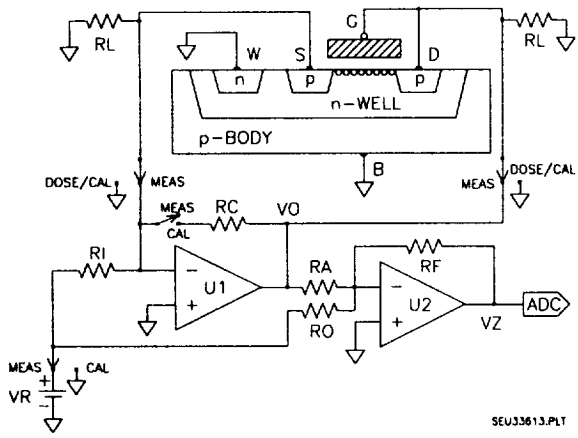

Figure 3. p-FET total dose circuitry.

In operation, all terminals of the p-FET are operated near ground except the drain which operates near VO = -1.5 V. During irradiation, the device is biased in the off state. The two RL resistors are used to bleed off any charge remaining on the p-FET. The instrumentation is calibrated by positioning the switch to CAL shown in Fig. 3. This replaces the p-FET with calibration resistor RC.

The p-FET constant drain current, ID, is established by VR and RI or ID = VR/RI. The output of amplifier U1 is scaled by U2 so that it makes maximum use of the range of the 8-bit ADC (Analog-to-Digital Converter). As seen in Fig. 3, the gate is connected to the drain. This insures that the p-FET is operated in saturation.

3. p-FET MODEL EQUATIONS

In saturation the p-FET drain current [7] is:

$$(1)\quad ID = \frac{\beta}{2} \cdot \frac{(-VO + VT)^2}{1 + \theta(-VO + VT)}$$

where VO is the p-FET output voltage, ß = $KP \cdot W_e/L_e$, $KP = \mu \cdot C_o$ and VT is the p-FET threshold voltage. $W_e = W - DW$ and $L_e = L - DL$ are the effective channel width and length, respectively, μ is the zero-field channel mobility, C_o is the gate oxide capacitance per unit area, and θ is the mobility electric-field degradation parameter.

The above equation was simplified by taking its square root. Then the term was linearized using Taylor Series expansion:

$$(2)\quad \sqrt{ID} = \sqrt{ß/2}(-VO + VT)\left[1 - \frac{\theta}{2}(-VO + VT)\right]$$

Expressions for the temperature and dose dependence of VT, ß, and θ are given below. The equations are expanded about the reference temperature T_o. In these equations, the temperature and dose effects are assumed to be independent. That is, the equations do not include a dose·temperature product term.

The threshold voltage is described by:

$$(3)\quad VT = VT_o + VT_T(T - T_o) + VT_D \cdot D$$

where D is the dose, VT_o is the threshold voltage at T_o and D = 0, $VT_T = \partial VT/\partial T|_{T \to To}$ and $VT_D = \partial VT/\partial D|_{D \to 0}$. The temperature [7] and dose dependence [8] of ß is given by:

(4) $ß = ß_0(T/T_0)^{-n} + ß_D \cdot D$

where $ß_0$ is ß evaluated at T_0 and D = 0, $ß_D = \partial ß/\partial D|_{D\_0}$, n characterizes the mobility temperature dependence, and T is the absolute temperature. For $D_T = \partial D/\partial T = 0$:

(5) $ß_T = \partial ß/\partial T = -n \cdot ß/T$

The temperature and dose dependence of θ is given by:

(6) $\theta = \theta_0 + \theta_T \cdot (T - T_0) + \theta_D \cdot D$

where θ_0 is θ evaluated at T_0 and D = 0, $\theta_T = \partial\theta/\partial T|_{T\_To}$ and $\theta_D = \partial\theta/\partial D|_{D\_0}$.

4. p-FET TEMPERATURE EQUATIONS (INCLUDING θ)

In this section the p-FET equations are derived including the θ parameter. This allows an accurate analysis at the operating or measurement temperature, T_m. This temperature is usually different from the reference temperature, T_0. The measurement temperature, T_m, might be the mean spacecraft operating temperature.

The p-FET output voltage follows from Eq. 2. The solution requires solving the equation which is quadratic in VO:

(7) $VO = VT - \frac{1}{\theta} \cdot (1 - \sqrt{1 - \theta} \cdot \sqrt{[8 \cdot ID/ß]})$

The sign of the square root is negative which can be verified by evaluating this equation in the limit $\theta \rightarrow 0$. The value of VO at T_m is calculated from:

(7a) $VO_m = VT_m - \frac{1}{\theta} \cdot (1 - \sqrt{1 - \theta_m \cdot \sqrt{[8 \cdot ID_m/ß_m]}})$

The current, ID_m, at the measurement temperature is found from the above equation by setting $\partial VO/\partial T|_{T\_Tm} = 0$ and solving the resulting quadratic equation for ID_m:

(8) $\sqrt{ID_m} = + \frac{A}{2} - C \pm E \cdot \sqrt{[1 + B \cdot (-C + A/4)]}$

where

(9) $A = a^2 b/d^2$
(10) $B = b$
(11) $C = c/d$
(12) $E = a/d$
(13) $a = VT_T + \theta_T/\theta_m^2$
(14) $b = -\theta_m \cdot (8/ß_m)$
(15) $c = \theta_T/\theta_m^2$
(16) $d = -[(2\theta_T/\theta_m) - (n/T_m)]/\sqrt{(2ß_m)}$

The sign of the square root in Eq. 8 is positive for $\theta > 0$ and negative for $\theta < 0$.

5. p-FET TEMPERATURE EQUATIONS (θ = 0)

The equations derived in Section 4, include the θ parameter. Since θ is small, it is neglected in this section to gain physical insight into the meaning of the equations.

The p-FET IV characteristics are plotted in Fig. 4 using Eqs. 1, 3, and 4 for D = 0 and the parameters [7] listed in the Fig. 4. This figure shows that the so called "temperature independent" point is in fact ill-defined when viewed in detail.

In this analysis, the most important p-FET parameter is VO. Its temperature dependence is analyzed by expressing Eq. 2 as follows:

(17) $VO = VT - 2ID/ß$

The VO is calculated for D = 0 using Eqs. 3 and 4 and plotted in Fig. 5. These curves show that there is a point at which VO is independent of temperature. This point is determined by differentiating Eq. 17 with respect to temperature and setting the result to zero. This leads to the simple expression for the measurement current:

(18) $ID_m = 2ß_m^3(-VT_T/ß_{Tm})^2$

The value for ID_m = 19.2 μA was calculated using the parameters shown in Fig. 5. The five curves were plotted with ID values that vary by one percent. This shows the effect of missing the target current of ID_m. As seen in the figure, the peak in the curve moves to higher temperatures as ID increases. The value of VO changes by 0.25 percent for a one percent change in ID.

The temperature sensitivity of VO can be expressed simply by combining Eqs. 4, 5, 17, and 18 which leads to:

(19) $VO_T = \partial VO/\partial T = VT_T[1 - (T_m/T)^{1-n/2}]$

This shows that $VO_T = 0$ at $T = T_m$ for any n or $VO_T = 0$ for n = 2 for all T.

The effect of temperature variations on VO_T is analyzed with the help of the horizontal line shown in Fig. 5. This line is 1 mV below the target value of VO_m = -1.5 V. The value of 1 mV was chosen because it is the same magnitude as the dose effects to be measured. The VO_T = -63 μV/°C at point "a" and 63 μV/°C at point "c" seen in Fig. 5. The temperature range between "a" and "c" is more than 70°C. This means that VO_T is less than ±63 μV/°C over the 70°C temperature range centered at the measurement temperature, T_m. This is a significant improvement in the

uncompensated temperature sensitivity of VT_T = 2 mV/°C used in calculating Figs. 4-6.

The solution for n = 2 means that the curves shown in Fig. 5 have zero slope. For this case, the p-FET IV characteristics display a true temperature insensitive point as shown in Fig. 6.

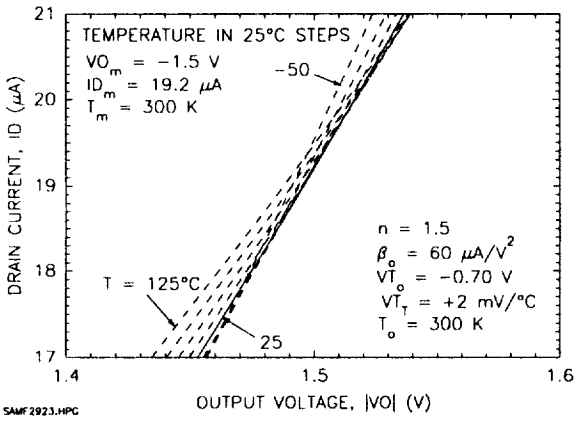

Figure 4. Expanded p-FET IV characteristics showing that the "temperature independent" point is not a point. Note n ≠ 2.

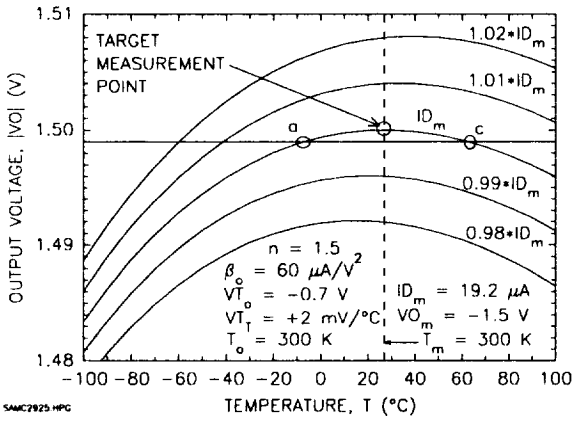

Figure 5. The temperature and current dependence of the p-FET output voltage using Eq. 17.

Next, ID_m is analyzed for design purposes by substituting $ß_m = KP_mW_e/L_e$ into Eq. 18; this leads to:

$$(20)\quad ID_m = 2KP_m(VT_T \cdot T_m/n)^2 W_e/L_e$$

This equation shows that ID_m depends on the silicon parameters, KP_m, VT_T, and n, the measurement temperature, T_m, and the FET geometry. Thus, once the silicon parameters and T_m are known, the designer is free to choose ID_m by adjusting W and/or L.

Finally, VO is analyzed for design purposes by substituting Eqs. 5 and 18 into Eq. 17:

$$(21)\quad VO_m = VT_m - 2VT_T \cdot T_m/n$$

This equation shows that VO_m depends on the silicon parameters, VT_o, VT_T, and n and the measurement temperature, T_m. Note that VO_m is independent of FET W/L geometry. Thus the designer has no control over this value. In this study, the value for VO_m is about -1.5 V. With irradiation, VO_m becomes more negative. The initial VO_m value is important from an instrumentation stand point. Since the ADC shown in Fig. 3 has an input voltage range between 0 to 5 V, the pre-radiation value for VZ in Fig. 3 is set to zero volts by compensating VO_m by setting $RO = -RA \cdot VR/VO_m$.

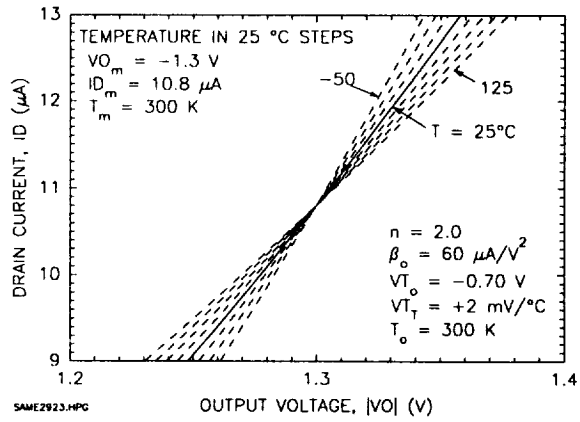

Figure 6. Expanded p-FET IV characteristics showing a true temperature independent point for n=2.

6. p-FET TEMPERATURE DATA ANALYSIS

The p-FETs were measured in packages in an oven using an hp4062 parametric test system. The temperatures are estimated to be accurate to within ±1°C. The measurements were obtained by forcing VO = 2 V and measuring ID_5. Then four additional currents were forced at $\sqrt{ID_1}$ = $0.2 \cdot \sqrt{ID_5}$, $\sqrt{ID_2}$ = $0.4 \cdot \sqrt{ID_5}$, $\sqrt{ID_3}$ = $0.6 \cdot \sqrt{ID_5}$, and $\sqrt{ID_4}$ = $0.8 \cdot \sqrt{ID_5}$. Once these values are determined, they are used throughout the rest of the measurements.

The experimental data, shown in Fig. 7, was fitted using the method of least squares. In the analysis, the following parabolic equation was

used. The coefficients of the equation were related to the parameters in Eq. 2:

(22) $\sqrt{ID} = a_0 + a_1 \cdot VO + a_2 \cdot VO^2$

where

(23) $a_0 = \sqrt{(ß/2)} \cdot VT \cdot (1 - \theta \cdot VT/2)$

(24) $a_1 = -\sqrt{(ß/2)} \cdot (1 - \theta \cdot VT)$

(25) $a_2 = -\sqrt{(ß/2)} \cdot \theta/2.$

The "a" parameters are used to obtain VT, ß, and θ for each IV curve. The VT solution was obtained by setting VO = VT at ID = 0. This leads to a quadratic equation whose solution is:

(26) $VT = a_1/(2a_2) \cdot (-1 + \sqrt{1 - 4a_0a_2/a_1^2})$

The sign of the square root is positive. This can be verified by setting $\theta = 0$ or $a_2 = 0$. The solution for ß is:

(27) $ß = 2(a_1 + 2a_2 \cdot VT)^2$

The solution for θ is:

(28) $\theta = 2a_2/(a_1 + 2a_2 \cdot VT)$

The IV points, shown in Fig. 7, were fitted using the above procedure. The ß, VT, and θ values are listed in Table 1 for three temperatures.

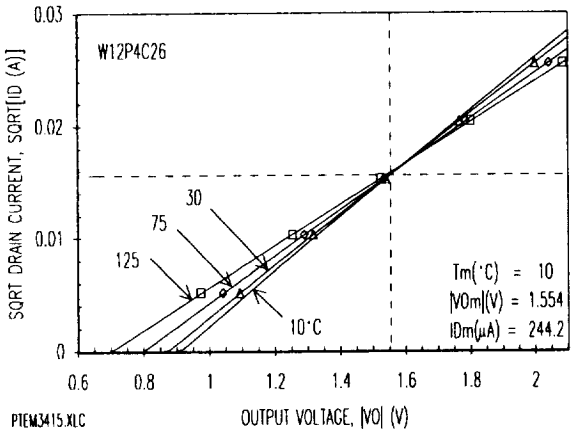

Figure 7. 1.2-μm CMOS p-FET IV temperature response for flight chip number W12P4C26.

The temperature parameters for VT and θ were extracted by least squares fitting the data listed in Table 1 by using Eqs. 3 and 6. The temperature parameter for ß was extracted using Eq. 4 after it was linearized by taking the logarithm. The temperature parameters are listed in Table 2.

Values for ID_m and VO_m were calculated using Eqs. 7a and 8 and the parameters listed in Table 2. The results are listed in Table 2 and plotted as the vertical and horizontal lines in Fig. 7.

Table 1. Flight p-FET4 Parameters (W12P4C26)

T °C	VT V	ß mA/V^2	θ 1/V
30	-0.874	1.100	0.056
75	-0.800	0.891	0.041
125	-0.703	0.708	0.027

Table 2. Flight p-FET4 Parameters
(T_o = 300 K, T_m = 10°C, W12P4C26)

PARAM	UNITS	MEAN STDEV
X_o	nm	21.8*
W	um	182
L	um	4
DL	um	0.3459*
VT_o	V	-0.8821±0.0051
VT_T	mV/°C	1.8002±0.0800
$ß_o$	mA/V^2	1.1240±0.0110
KP_o	$μA/V^2$	24.7041±0.2423
n	--	1.6140±0.0528
$ß_{To}$	$(μA/V^2)/°C$	-6.0471
θ_o	1/V	0.0571±0.0013
θ_T	(1/kV)/°C	-0.3153±0.0210
VT_m	V	-0.9125
$ß_m$	mA/V^2	1.2339
θ_m	1/V	0.0624
$ß_{Tm}$	$(μA/V^2)/°C$	-6.6384
ID_m	μA	244.2
VO_m	V	-1.554

* MOSIS supplied parameter.

7. p-FET DOSE DATA ANALYSIS

The p-FET dose dependence was determined using Cobalt-60 irradiation. The devices were irradiated with their lids on, at room temperature, at 1 rad/sec, and at zero bias. The p-FETs were measured at room temperature within 15 minutes after the Cobalt-60 irradiation. The p-FET were also annealed at room temperature for times measured after the final irradiation.

The p-FET irradiation results, shown in Fig. 8, were fitted using Eq. 22. This produced a set of

VT, ß, and θ values for each dose value. These values are plotted in Figs. 9 to 11 for four p-FETs. The radiation results are listed in Table 3 for one of the p-FETs.

The VT values, plotted in Fig. 9, show a high degree of linearity during irradiation and a slight recovery with annealing. The group average slope of the VT vs dose curve during irradiation is VT_D = -1.698±0.038 mV/krad(Si). The shift in VT with radiation is consistent with the build up of positive oxide charge and interface states. The slight recovery of VT during room temperature annealing is consistent with the slight loss of oxide charge. The interface state density is stable as seen by the flat response of the mobility during annealing.

The ß values were converted to zero-field hole channel mobility using:

(29) $\mu = (L - \Delta L)\cdot ß/(W\cdot C_O)$

In this analysis, the value for C_O was calculated using the MOSIS supplied value for the gate-oxide thickness, X_O = 21.8 nm.

Table 3. Ground Test p-FET Cobalt-60 Radiation Parameters for Chip Number W12P4C05

PAR.	UNITS	MEAN STDEV
VT_D	mV/krad(Si)	-1.674±0.004
$ß_D$	µA/V²/krad(Si)	-3.585±0.164
KP_D	µA/V²/krad(Si)	-0.079±0.004
θ_D	1/kV/krad(Si)	-1.184±0.018
$V\theta_{Dm}$	mV/krad(Si)	-2.591±0.018

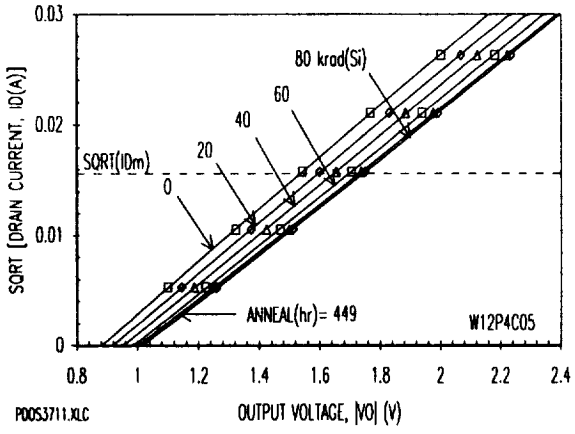

Figure 8. 1.2-µm CMOS p-FET IV dose/anneal response for chip number W12P4C05.

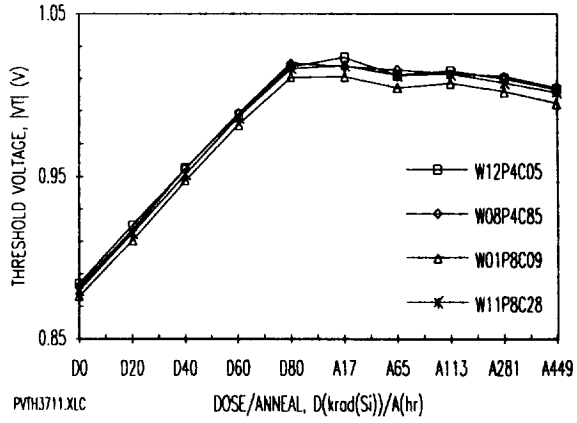

Figure 9. Four 1.2-µm CMOS p-FET threshold voltage dose/anneal responses.

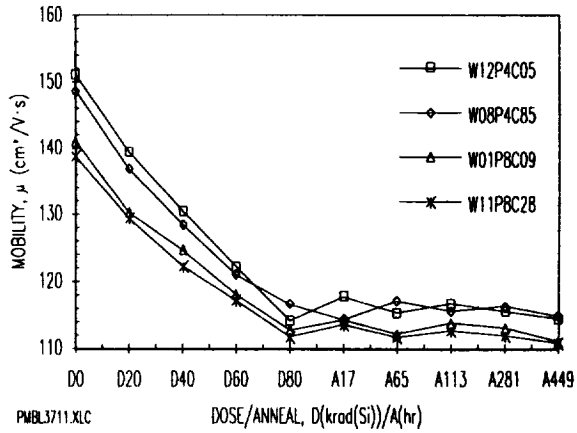

Figure 10. Four 1.2-µm CMOS p-FET hole mobility dose/anneal responses.

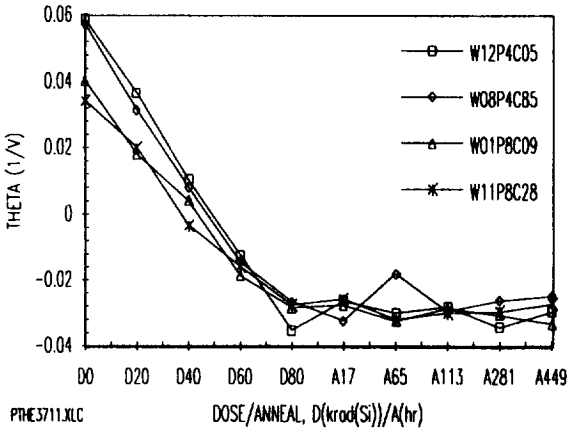

Figure 11. Four 1.2-µm CMOS p-FET theta dose/anneal responses.

The data, shown in Figure 10, are clustered according to the p-FET's W/L ratios. This ratio is designated by the "P" number given in the wafer number listed in the figure. That is, for P4 the ratio is W/L = 182/4 μm/μm and for P8 the ratio is W/L = 182/8 μm/μm. This dependence on the W/L ratio does not affect the output voltage, for VO is geometry independent as seen in Eq. 21.

As seen in the Fig. 10, μ is stable after annealing. The build up of positively charged interface states during irradiation degrades the mobility due to the increase in channel scattering centers [9]. Since the mobility does not anneal at room temperature, the interface state density is stable.

The θ values, shown in Fig. 11, are clustered according to the p-FET W/L ratios. The characteristics show no annealing, which indicates that the interface state density is stable during annealing.

The θ parameter represents the curvature term for the parabolic equation given in Eq. 2. The curvature is difficult to see in Fig. 8 because θ is very small. As seen in Fig. 11, the maximum value for θ is 0.06 1/V. The influence of θ in Eq. 2 is less than 3 percent because it enters as $\theta/2$. This small value for θ justifies the use of the Taylor Series expansion in simplifying Eq. 2.

As shown in Fig. 11, the charge is positive at low dose and negative after high dose and annealing. The sign of θ indicates the direction of the √ID vs VO parabola given by Eq. 2. This point is illustrated in Fig. 12. For θ > 0 the parabola points down and for θ < 0 the parabola points up. For θ = 0, the √ID vs VO relationship is a straight line.

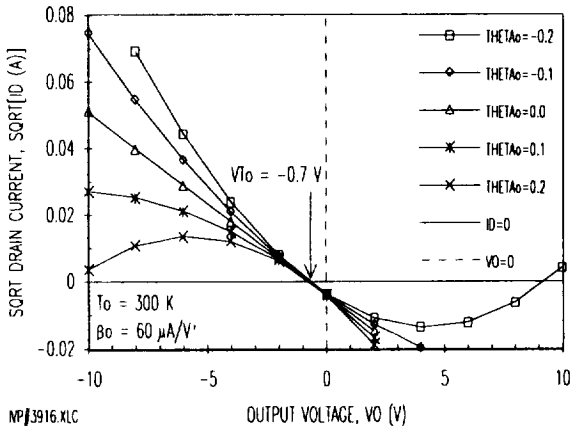

Figure 12. Plot of Eq. 2 for different θ values.

8. DOSIMETRY

The device dose sensitivity is derived in this section. Since the dose is measured at the constant current, ID_m, the radiation dose sensitivity of VO is greater than VT_D. This is evident in Fig. 8 where the spread in the curves is wider at ID = ID_m than at ID = 0 due to the dose dependence of the mobility.

In this section the output-voltage dose sensitivity, VO_D, for θ = 0 is calculated by differentiating Eq. 17 with respect to dose at ID = ID_m. Then ID_m, given in Eq. 18, is substituted into the result. The output-voltage dose sensitivity is:

$$(30)\quad VO_{Dm} = \partial VO/\partial D|_{Tm} = VT_D - VT_T \cdot \beta_D/\beta_{Tm}$$

A value for VO_{Dm} = -2.59 mV/krad(Si) was calculated using the values listed in Tables 2 and 3. This result is considerably larger than VT_D = -1.67 mV/krad(Si).

The output voltage for the four p-FET samples is shown in Fig. 13. This plot was obtained from data sets like those shown in Fig. 8 where the VO values were obtained at ID_m. The data shows a nearly linear rise in VO with dose and a slight annealing effect.

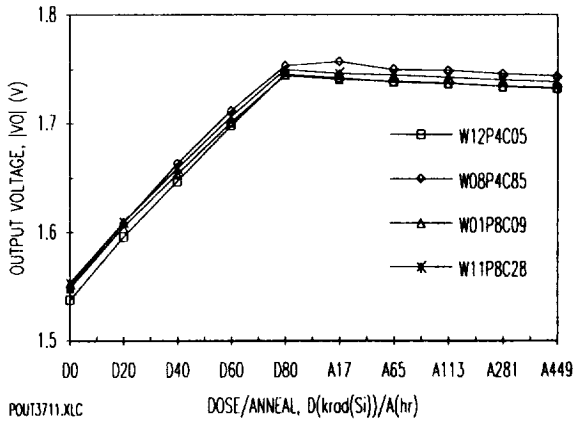

Figure 13. Four 1.2-μm CMOS p-FET output voltage dose/anneal responses determined at the current, ID_m.

The similarity of the data is remarkable considering the p-FET samples came from different wafers from the same run. This means that the sample set can be assumed to be uniform and that the results can be used to calibrate the flight parts which, of course, can not be irradiated on the ground.

For the circuitry shown in Fig. 3, which uses an 8-bit ADC to span 100 krad(Si), the resolution is 100k/256 = 390 rad(Si)/bit. This means that the

p-FET dosimeter can easily resolve a dose of 1 krad(Si).

9. CONCLUSION

The use of on-chip p-FET dosimeters has been established and provides a radiation sensitivity of -2.6 mV/krad(Si) for the 1.2-μm CMOS used in this study. The temperature dependence is less than ±63 μV/°C over a temperature range of 70°C centered about the p-FET temperature independent point. At this point, the pre-irradiation output voltage was determined to be about -1.5 V and this value is design independent. The use of on-chip p-FETs provides a direct measure of the radiation dose experienced by the associated CMOS IC.

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INVERTER MATRIX FOR THE CLEMENTINE MISSION

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ABSTRACT

An inverter matrix test circuit was designed for the Clementine space mission and is built into the RRELAX (Radiation and Reliability Assurance Experiment). The objective is to develop a circuit that will allow the evaluation of the CMOS FETs using a lean data set in the noisy spacecraft environment. As will be shown, only nine data points are needed to acquire ten CMOS FET parameters.

INTRODUCTION

An inverter matrix was designed for the RRELAX and included on the Clementine space mission. Two RRELAX units were fabricated. One unit is included on the Clementine spacecraft which will orbit the moon and fly-by the asteroid Geographos. The second unit is included on the Inter-Stage Adaptor (ISA) which goes into a translunar orbit. The Clementine is scheduled for launch on January 25, 1994.

The RRELAX, shown in Fig. 1, is by 4" x 4" x 1.5" (10 x 10 x 3.8 cm), weighs 22 oz (0.62 kg) and requires 2.5 watts peak power.

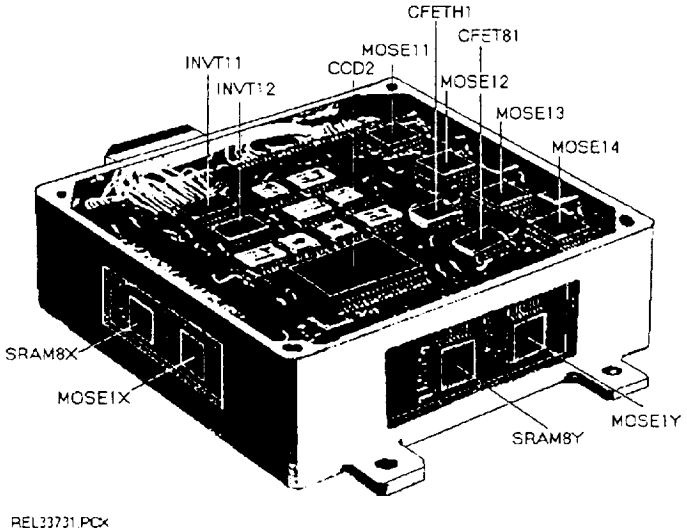

Figure 1. RRELAX showing the arrangement of test devices. The inverter matrices are labeled INVT11 (Z08) and INVT12 (Z07).

The unit contains an 80C86 microprocessor operating at 2.4 MHz and data acquisition circuitry to measure the experimental devices. The data is stored in the RRELAX memory and the results sent to the spacecraft through a serial port for down-linking.

The labels in Fig. 1 point to the experimental devices including SRAMs for Cosmic Ray detection, p-FETs for total dose measurement, and a CCD for radiation effects analysis. The locations of the two inverter matrices are shown in the figure. One matrix has a 7-mil (0.18 mm) Al equivalent shield and the other a 37-mil (0.94 mm) Al equivalent shield. [0.18 mm and 0.94 mm]

The inverter matrix was developed to evaluate CMOS FETs fabricated at a rad-soft rapid-prototype CMOS foundry in order to evaluate its space worthiness. The FETs included in the inverter matrix are typical of FETs found in integrated circuits. In addition the matrix was designed to require a small data set in order to minimize spacecraft down-link capacity. As will be shown, only nine data points are needed to characterize ten n- and p-FET parameters.

The layout of the inverter matrix, shown in Fig. 2, is similar to the inverter matrix developed in the

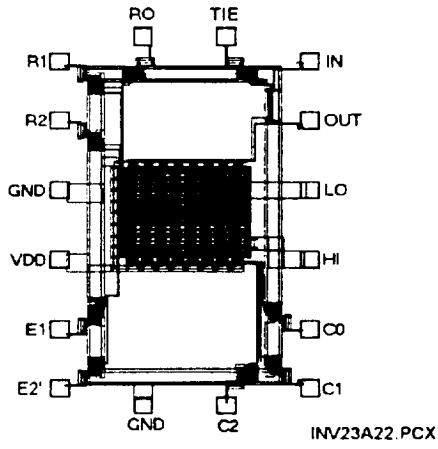

Figure 2. Inverter matrix with 64 test inverters arranged in four identical quadrants. The chip size is 1.63 x 2.58 mm^2.

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middle 80's for evaluating process statistics [1] and [2]. The matrix consists of 64 inverters arranged in four identical quadrants. In two of the quadrants, the gates are biased high during radiation and in the other two quadrants, the gates are biased low during irradiation. The dimensions of the inverter matrix FETs are listed in Table 1.

The key to this approach is the dependence of the inverter threshold voltage, VT_i, on geometry [3]:

$$(1)\quad VT_i = \frac{VDD + VT_n\sqrt{\beta_r} - VT_p}{1 + \sqrt{\beta_r}}$$

where VT_n is the n-FET threshold voltage, and VT_p is the magnitude of the p-FET threshold voltage. The dependence of VT_i on geometry, shown in Fig. 3, indicates how VT_i depends on the geometry of the inverter, β_r:

$$(2)\quad \beta_r = \frac{\beta_n}{\beta_p} = \frac{KP_n(W_n - \Delta W_n)(L_p - \Delta L_p)}{KP_p(W_p - \Delta W_p)(L_n - \Delta L_n)}$$

where $KP = \mu_o \cdot C_o$; μ_o is the zero-field channel mobility and C_o is the gate capacitance per unit area. The FET design width is W, and L is the design length. The actual width and length are described using ΔW and ΔL. Notice that for $\beta_r \to 0$, $VT_i = VDD - VT_p$ and for $\beta_r \to \infty$, $VT_i = VT_n$.

The transfer curves for the 16 inverters listed in Table 1 are shown in Fig. 4. The inverter threshold voltage is located at the intersection of transfer curve and the positive sloping Vout-Vin line.

FET MODEL

The analysis uses the fact that at the inverter threshold both n- and p-FETs are in saturation. Thus the following simple square-law drain-current expression adequately describes the n-FET behavior [4]:

$$(3)\quad ID_n = \frac{\beta_n(VT_i - VT_n)^2}{2[1 + \theta_n(VT_i - VT_n)]}$$

where

$$(4)\quad \beta_n = KP_n(W_n - \Delta W_n)/(L_n - \Delta L_n)$$

and

$$(5)\quad \theta_n = \theta L_n/(L_n - \Delta L_n)$$

The p-FET equations are:

$$(6)\quad ID_p = \frac{\beta_p(VDD - VT_i - VT_p)^2}{2[1 + \theta_p(VDD - VT_i - VT_p)]}$$

where

$$(7)\quad \beta_p = KP_p(W_p - \Delta W_p)/(L_p - \Delta L_p)$$

and

$$(8)\quad \theta_p = \theta L_p/(L_p - \Delta L_p)$$

The above FET models were chosen after numerous alternative models were tried. It was found that giving VT a spatial description led to unstable solutions. This is understandable since the data points, as seen in Fig. 5, are not located near the VT extraction points. Also θ is described by an L- dependence only. When the offset term, θ_o, was introduced into the model, θ parameters were too unstable and fluctuated about zero. When θW was introduced into the model, these values also fluctuated about zero. the net result is a simple model that fits the data reasonably well and extracts reasonable parameters. Also the extraction procedure is robust.

DATA FITTING PROCESS

The above equations were combined into the following equation set and fitted to the data shown in Fig. 5. The FET geometries for the cardinal points shown in Fig. 5 are given in Table 3. The equations for the n-FETs are:

$$(9)\quad \sqrt{I_n} = a_0 + a_1 \cdot VT_i + a_2 \cdot \frac{(VT_i - VT_n)^2}{(L_n - \Delta L_n)}$$

where

$$(10)\quad I_n = 2 \cdot ID_n(L_n - \Delta L_n)/(W_n - \Delta W_n)$$
$$(11)\quad a_0 = -VT_n \cdot \sqrt{KP_n}$$
$$(12)\quad a_1 = \sqrt{KP_n}$$
$$(13)\quad a_2 = -\theta L_n \cdot \sqrt{KP_n}/2$$

Using the above "a" coefficients, the n-FET parameters are:

$$(14)\quad VT_n = -a_0/a_1$$

$$(15)\quad KP_n = a_1^2$$
$$(16)\quad \theta L_n = -2a_2/a_1$$

The above equations are plotted as curves #4, #5, and #6 in Fig. 5.

The equations for the p-FETs are:

$$(17)\quad \sqrt{I_p} = b_0 + b_1 \cdot VT_i + b_2 \cdot \frac{(VDD - VT_i - VT_p)^2}{(L_p - DL_p)}$$

where

$$(18)\quad I_p = 2 \cdot ID_p(L_p - DL_p)/(W_p - DW_p)$$
$$(19)\quad b_0 = VT_p \cdot \sqrt{KP_p}$$
$$(20)\quad b_1 = -\sqrt{KP_p}$$
$$(21)\quad b_2 = -\theta L_p \cdot \sqrt{KP_p}/2$$

Using the above "b" coefficients, the p-FET parameters are:

$$(22)\quad VT_p = VDD + a_0/a_1$$

$$(23)\quad KP_p = a_1^2$$

$$(24)\quad \theta L_p = 2a_2/a_1$$

The p-FET curves are plotted as curves #1, #2, and #3 in Fig. 5.

The solution for the FET parameters, VT KP, and θL were obtained by using a least squares fitting procedure to determine the "a" and "b" coefficients of the linear equations, Eqs. 9 and 17. The least squares procedure was embedded inside a Simplex solver. The Solver changed DL, DW, and VT in order to optimize the least squares coefficient of determination with the constraint that the estimated VT value equals the least squares VT value within a precision of 0.01.

The fit of the data to the cardinal points is shown by the curves given in Fig. 5. The fit is reasonable considering the simplicity of the FET model given in Eqs. 9 and 17. By design, the curves converge to a single value of VT_n and VT_p. The matrix contained additional FET geometries and so these were included in the analysis as "bonus" points which help stabilize the extraction of VT_n. As will be shown, VT_p has considerable variability because the data points are far from the VT_p extraction point.

The test results for the data plotted in Fig. 5 is listed in Table 2. The listing indicates that 5 p-FET and 5 n-FET parameters have been extracted from the data. The RRELAX extracted results are compared to results published by MOSIS. The RRELAX results are surprisingly close to the MOSIS results. The discrepancies can be explained by differences in extraction procedures and wafer-to-wafer parameter variations. The MOSIS parameter extraction occurs in the FET linear region; whereas, RRELAX parameter extraction occurs in the FET saturation region.

CIRCUIT DESCRIPTION

The inverter matrix, shown in Fig. 6, consists of an 8-by-8 array of test inverters fabricated in a 1.2-um n-well CMOS process. The chip has enables, E1 and E2', that allow two or more chips to be bussed together; power, VDD (5V) and ground, GND for decoder logic; row address, R0 - R2 and column address C0 - C2 for selecting the test inverter; test inverter power, HI, ground, LO, input, IN, and output, OUT; and logic input, TIE, that tristates IN and connects OUT to the addressed test inverter input. The 64 test inverters are arranged in 4 identical quadrants. The quadrants contain 16 test inverters having unique n- and p-FET geometries listed in Table 1. When the chip is deselected (E1 and/or E2' inactive), the inverter inputs are biased low (0 V) in QUAD#1 and QUAD#3 and high (5 V) in QUAD#2 and QUAD#4.

The inverter matrix circuit diagram in Fig. 6 shows one test inverter (MN1 and MP1) and supporting select transistors. The dashed lines indicate connections to the remaining seven rows and seven columns of the matrix. Row and column decoders are used to select one of the 64 test inverters for measurement. These decoders are deselected (no selected outputs) when one or both chip enables are inactive, putting all test inverters in a known biased condition. Two of the quadrants have the test inverter inputs I* connected to D as shown in Fig. 6 while the other two quadrants have inputs I* connected to U.

Fig. 7 is an equivalent circuit of an enabled inverter matrix and the support electronics used to obtain measurements. The RRELAX inverter matrix measurements use a 12-bit Analog-to-Digital Converter (ADC). The inverter output voltage is measured when the output switch is in the V position and the current through the inverter (IDD) is measured when the output switch is in the I position. OP-amps OP1 and OP2 function as a current-to-voltage converter which holds the LO point at a virtual ground. All current measurements are corrected by a baseline leakage measurement made on the matrix when it is deselected. When the matrix is deselected, the matrix baseline leakage current is the sum of leakage currents through 32 off n-FETs and 32 off p-FETs.

When TIE is low the Digital-to-Analog (DAC) drives the inverter input and allows the measurement of inverter transfer characteristics. The data analyzed in this paper was all obtained with TIE high, where the internal feedback connection is made, bringing the circuit to the inverter threshold condition.

DISCUSSION

Representative ground test results from the inverter matrix, shown in Figs. 8 to 10, were obtained from the Clementine spacecraft. Test results, shown in Figs. 11 to 13, were obtained from the Inter-Stage Adapter (ISA). The first results, shown in these figures, were obtained at JPL (Pasadena, CA) using an HP 4062 parametric tester to measure inverter matrix packages. Subsequent results were obtained from the inverter matrices mounted in the RRELAX. The second results were also obtained at JPL where the RRELAX was in a noise free environment. The third and fourth results were obtained with one RRELAX unit integrated into the Clementine spacecraft and the other RRELAX unit integrated into the Inter-Stage Adapter. The third result came from NRL (Naval Research Laboratory, Washington DC); and the fourth

result came from VAB (Vandenberg Air Force Base, Lompoc, CA).

The symbols used in Figs 8 to 13 are explained in Table 4. The symbols indicate (a) the bias on the inverter gates during irradiation and (b) the amount of shielding. Thus test results are expected to diverge into four trends once the devices receive sufficient radiation.

The results shown in Fig. 8 to 13 indicate that the laboratory results have least variability. On occasion results from RRELAX can be noisy. The source of the noise is under investigation.

The measurement has the interesting attribute that it requires only a single input voltage namely VDD and the output is an easily measured voltage that ranges between the VTn and VDD - VTp. This makes the measurement extremely simple and robust. These are the kind of attributes needed in the noisy environment of a spacecraft.

CONCLUSION

The inverter matrix developed for the RRELAX meets the design goal of providing FET parameters from a lean data set. The quality of the data could be improved by designing the inverter matrix FETs with geometries closer to the VT extraction points. This is important because it would reduce the uncertainties in the data extraction process and provide parameters with less variations.

The noise encountered in the RRELAX is due to the spacecraft operating environment. The noise enters through the power supplied to the RRELAX. Also the RRELAX experimental devices are lightly shielded to allow a maximun exposure to radiation. This allows RF from spacecraft operations to be picked up by the RRELAX electronics. Hopefully, these noise sources will be small enough so that radiation effects will be clearly observed in the data.

ACKNOWLEDGMENTS

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory. California Institute of Technology, and was sponsored by the Ballistic Missile Defense Organization/Innovative Science and Technology Office. The authors are indebted to T. Sorensen, JPL, for task management; to K. Hicks, JPL, for his role as cognizant engineer; to J. Pepoon, JPL for parts procurement; and to P. Rustan and H. Garrett, BMDO/IST, for their encouragement and support of this effort. The devices used in this study were fabricated through MOSIS, Information Sciences Institute, University of Southern California. FILE: ICMT4324.DOC

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Table 1. Inverter matrix inverter geometries

DIMENSIONS (μm)			
Wp	Lp	Wn	Ln
7.2	1.2	9.6	1.2
28.8	1.2	2.4	2.4
28.8	1.2	2.4	1.2
28.8	1.2	9.6	1.2
7.2	2.4	2.4	1.2
7.2	2.4	9.6	1.2
7.2	1.2	2.4	2.4
7.2	1.2	2.4	1.2
2.4	2.4	12.0	1.2
14.4	1.2	2.4	2.4
12.0	1.2	2.4	2.4
7.2	2.4	2.4	2.4
2.4	3.3	2.4	1.5
1.8	2.4	2.4	1.2
19.2	2.4	19.2	2.4
2.4	2.4	14.4	1.2

Table 2. Inverter matrix test results (CZ071vab1) for the data shown in Fig. 5 and from MOSIS.

		--- RRELAX ---		--- MOSIS ---	
PARAM	UNITS	n-FET	p-FET	n-FET	p-FET
DL	μm	0.470	0.686	0.227	0.116
DW	μm	0.616	0.768	0.524	0.620
VT	V	0.690	0.952	0.728	0.903
θL	μm/L	0.136	0.118	---	---
KP	$\mu A/V^2$	65.324	20.160	86.400	26.600
CC	--	0.998	0.995	---	---

Table 3. FET Dimensions for the curves shown in Fig. 5.

CURVE	W(μm)	L(μm)
#1	7.2	2.4
#2	7.2	1.2
#3	28.8	1.2
#4	2.4	2.4
#5	2.4	1.2
#6	9.6	1.2

Table 4. Symbols for Figs. 8 to 13.

DEVICE	SHIELD mil Al	GATE-HIGH-BIAS QUAD#1 QUAD#3	GATE-LOW-BIAS QUAD#2 QUAD#4
Z07-INVT12 Z08-INVT11	37 7	SQUARE DIAMOND	PLUS (+) CROSS (x)

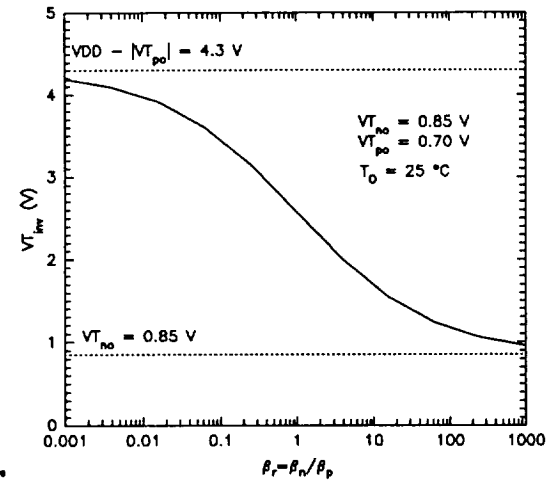

Figure 3. Spatial dependence of the inverter threshold voltage.

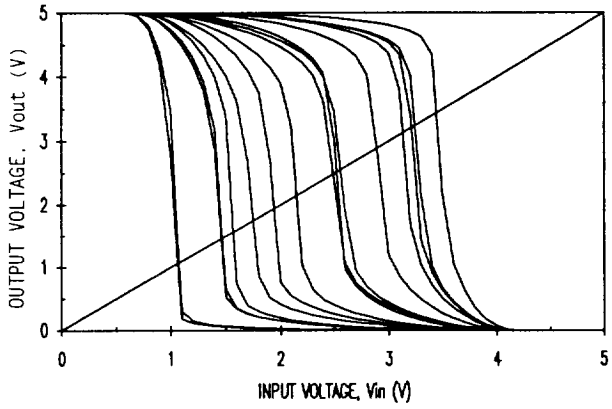

Figure 4. Inverter matrix transfer curves for one of the four quadrants.

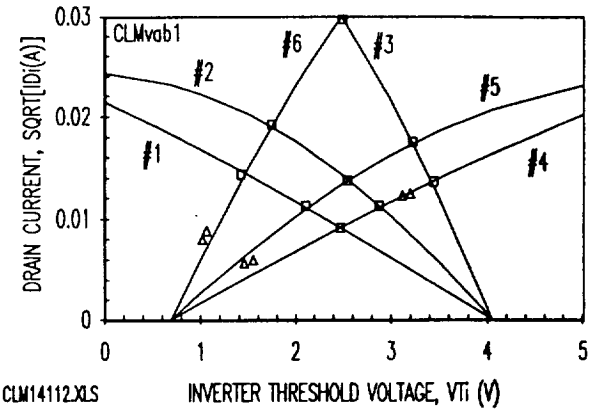

Figure 5. Inverter matrix data analysis showing the nine cardinal points (squares) and six bonus points (triangles). (CZ071vab1)

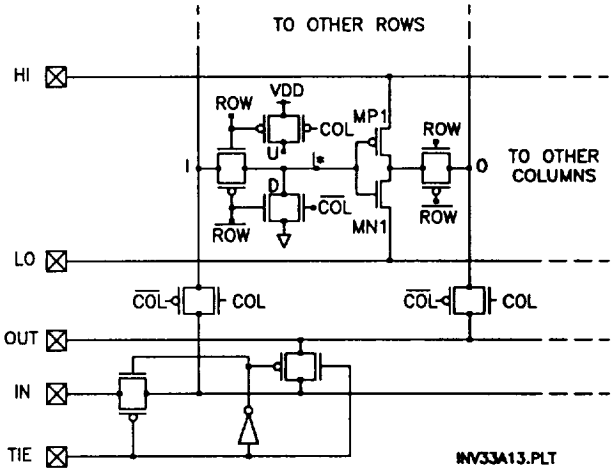

Figure 6. Inverter matrix circuit diagram showing one test inverter (MN1 and MP1) and signal steering transistors.

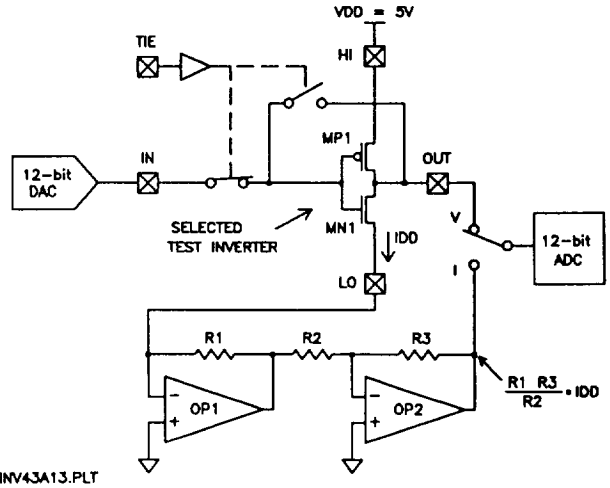

Figure 7. Test inverter measurement circuitry.

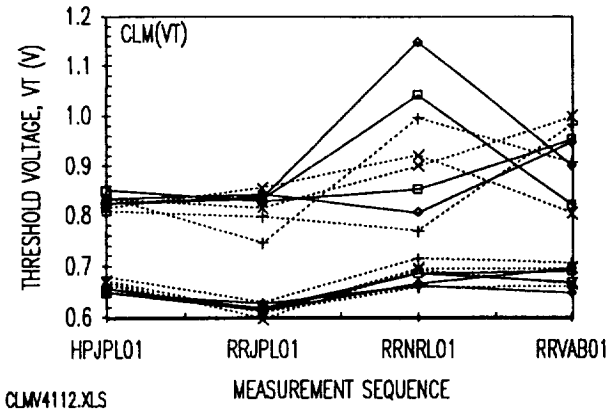

Figure 8. Clementine VT with VT_n below and VT_p above.

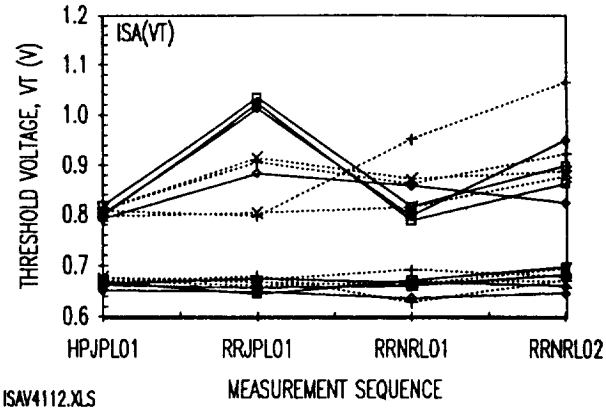

Figure 11. ISA VT with VT_n below and VT_p above.

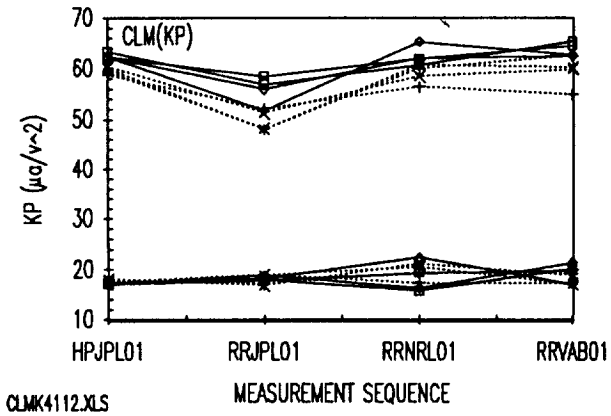

Figure 9. Clementine KP with KP_n above and KP_p below.

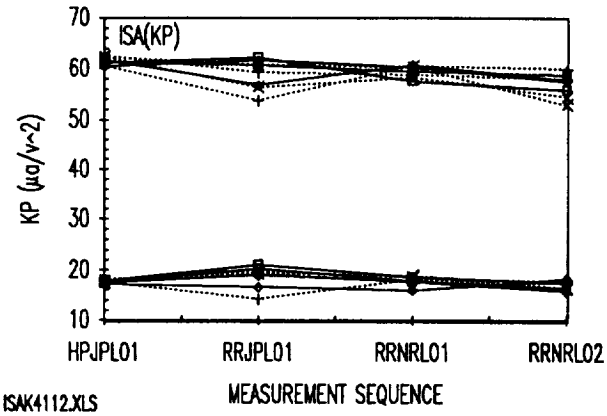

Figure 12. ISA KP with KP_n above and KP_p below.

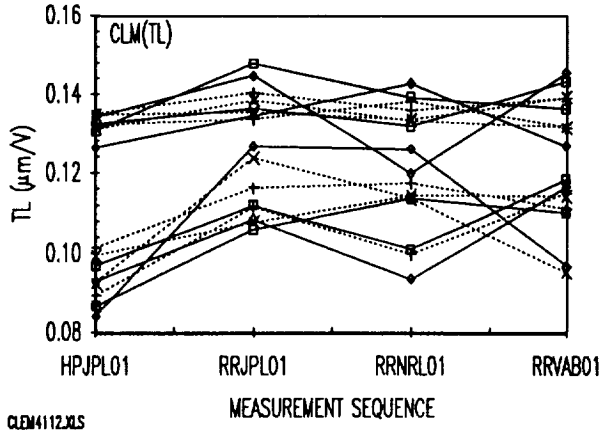

Figure 10. Clementine TL = θL with TL_n = θL_n above and TL_p = θL_p below.

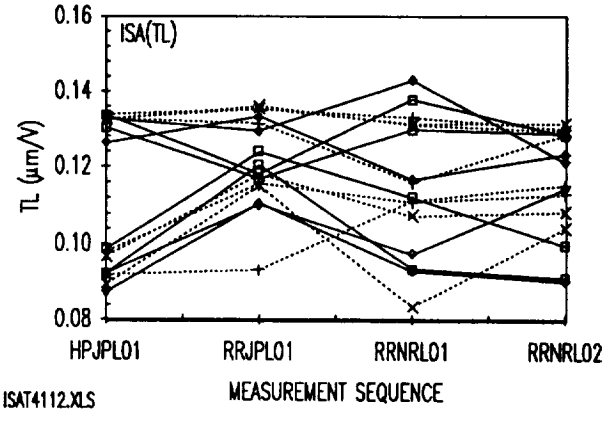

Figure 13. ISA TL = θL with TL_n = θL_n above and TL_p = θL_p below.

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SEU/SRAM as a Process Monitor

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Abstract— **The SEU/SRAM is a 4-kbit static random access memory (SRAM) designed to detect single-event upsets (SEU's) produced by high-energy particles, either in space or on the ground. This device was used to determine the distribution of the memory cell spontaneous flip potential. The variance in this potential was determined to be due to the variation in the threshold voltage of one of the n-FET's found in the memory cell. For a 1.2-μm CMOS process, the standard deviation of the n-FET VT was found to be 8 mV. This structure provides substantial statistical data; 4096 data points are measured. Using cumulative distribution and residual plots, outlier cells, such as stuck cells and nonnormally distributed cells, are easily identified.**

I. Introduction

THE use of matrixed test structures has been shown to be an effective approach to collecting statistical data with respect to inverter threshold voltages [1], metal steps [2], linewidths [2], and contact resistances [3]. Such structures require digital-to-analog converters (DAC) to stimulate the structure and analog-to-digital converters (ADC) to measure the required values. In this paper, the SEU/SRAM is used to obtain analog information about the cells without the use of an ADC. In this case, a DAC is used to force voltages and the on-chip latches (memory cells) are used to perform the ADC function. This allows rapid measurement of the SEU/SRAM.

The structure used in this study is the radiation monitor (RADMON), shown in Fig. 1. The structure consists of a 4-kbit SRAM for the detection of particles that cause single-event upsets in the memory cells and two p-FET's used to detect total dose radiation [4]. This structure was fabricated in a 1.2- μm CMOS process which is a scaled version of a RADMON fabricated using a 1.6-μm CMOS process [5].

The size of the RADMON, as shown in Fig. 1, is 7.0 mm^2. The memory cell layout is shown, in Fig. 2. The dimensions of the MOSFET's in the cell are listed in Table I. The SRAM was fabricated with a 1.2-μm n-well CMOS process at a MOSIS brokered foundry.

The SRAM cell schematic, shown in Fig. 3, has a six-transistor memory cell with an offset voltage V_o that is used to evaluate the spontaneous cell flip potential. The two internal nodes of the cell are labeled $V1$ and $V2$. These nodes will be used subsequently to describe the transfer curves for the inverter.

The timing diagram for the operation of the cell is shown in Fig. 4. This diagram shows that the memory cell has three states of operation: Read, Write, and Stare. In the Read and Write cycles, $V_o = 5$ V. Initially, all the cells are written into an initial state which is described in Fig. 3. Then the Stare cycle voltages are applied to the cells. In this cycle V_o is gradually lowered to a potential well above the spontaneous flip point. In this state, ionizing particles that deposit sufficient charge flip individual cells.

If V_o is lowered sufficiently, the memory cells will flip spontaneously. This is the behavior that is analyzed in this

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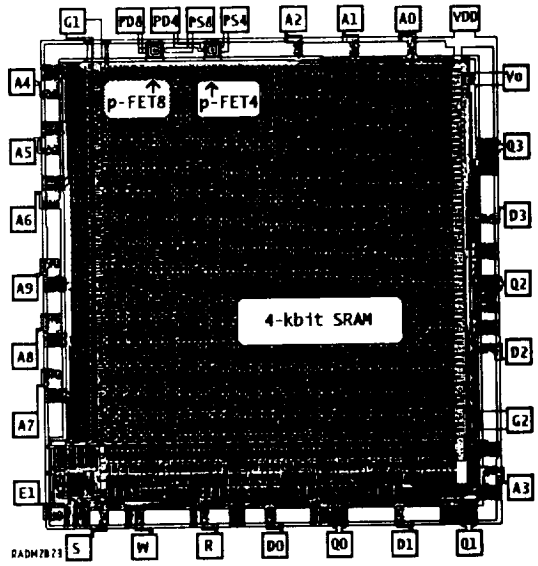

Fig. 1. RADMON chip, 2.6 mm × 1.7 mm, was fabricated in 1.2-μmCMOS.

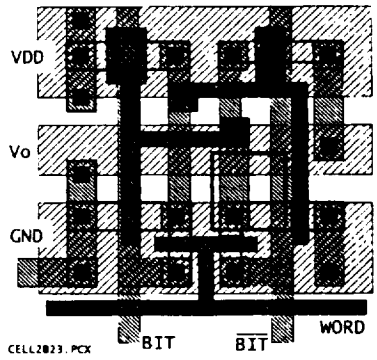

Fig. 2. Memory cell: 33.6 μm × 36.0 μm. The n-well and n- and p-select layers are omitted.

TABLE I
DIMENSIONS AND DRIVE CAPABILITY OF SEU/SRAM MOSFET'S USED IN THE SRAM MEMORY CELL SHOWN IN FIG. 3

FET	L (μm)	W (μm)	Ad (μm^2)	β (μA/V^2)
Mn1	1.5	2.4	11.16	110.4
Mn2	1.2	2.4	42.12	138.0
Mp1	3.3	2.4	8.64	16.7
Mp2	2.4	1.8	6.84	17.3
Mt1	1.2	1.8	—	103.5
Mt2	1.2	1.8	—	103.5

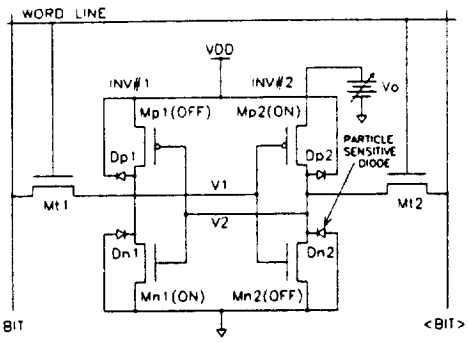

Fig. 3. SRAM memory cell circuit biased into the Stare state.

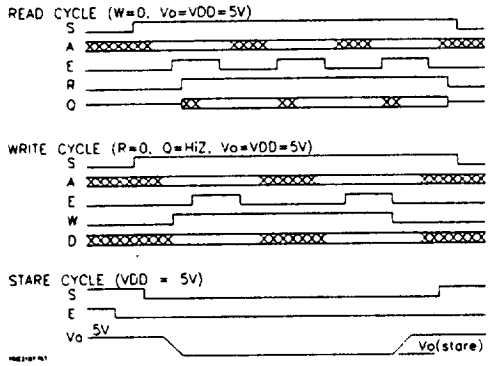

Fig. 4. SRAM memory cell timing diagram.

paper. It will be shown that the spontaneous flip potential is a measure of the uniformity of the threshold voltage of inverter 1, VT_{i1} as seen in Fig. 3. As such, the SEU/SRAM provides data that is useful for process control and lot acceptance.

II. Memory Cell Model

The cell spontaneous flip behavior is explained by the SRAM transfer curves shown in Fig. 5. These curves were generated using a simple model for the MOSFET drain current which does not include channel length modulation [6]. The inverter's input voltage is V_{in} and its output voltage is V_{out}. These voltages are related to the memory cell voltages: that is, V_{in} is $V2$ for INV1 and is $V1$ for INV2. Likewise, V_{out} is $V1$ for INV1 and $V2$ for INV2.

The CMOS inverter transfer curve is divided into five regions [7]. These five regions are described in Table II with respect to VT_{n}, the n-FET threshold voltage, VT_{p} the p-FET threshold voltage, and VT_{i} the inverter threshold voltage. The inverter threshold voltage appears at the output of an inverter when its output is connected to its input.

The MOSFET drain currents used in calculating the curves in Fig. 5 are listed below [7]. In the following expressions I_{nlin} and I_{plin} describe the n- and p-drain currents in the linear region of operation and I_{nsat} and I_{psat} describe the n- and p-drain current in the saturation region of operation.

$$I_{\text{nlin}} = \beta_n(V_{\text{in}} - VT_{\text{n}} - V_{\text{out}}/2)V_{\text{out}} \quad (1)$$

$$I_{\text{nsat}} = (\beta_n/2)(V_{\text{in}} - VT_n)^2 \quad (2)$$

$$I_{\text{plin}} = \beta_p(VDD - V_{\text{in}} - VT_{\text{p}} - (VDD - V_{\text{out}})/2) \cdot (VDD - V_{\text{out}}) \quad (3)$$

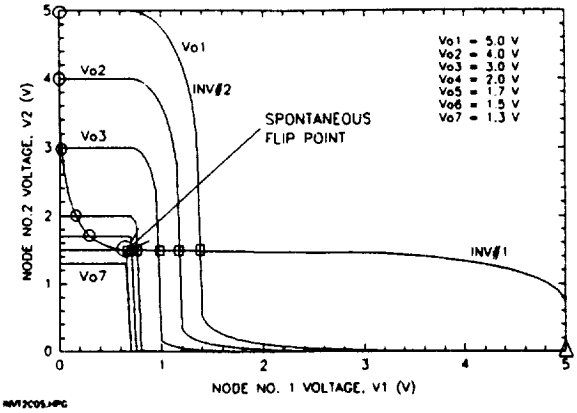

Fig. 5. SRAM transfer curves showing the variation in the stable point, indicated by circles, as the offset voltage V_o is lowered to the spontaneous flip point.

TABLE II
V_{in} Regions and MOSFET Currents Used to Calculate the Transfer Curves Shown in Fig. 5

Region	V_{in}	Current	V_{out}
I	$0 \le V_{\text{in}} \le VT_{\text{n}}$	$I_{\text{n}} = I_{\text{p}} = 0$	V_{DD}
II	$VT_{\text{n}} \le V_{\text{in}} \le VT_{\text{i}}$	$I_{\text{nsat}} = I_{\text{plin}}$	—
III	$V_{\text{in}} = V_{\text{out}} = VT_{\text{i}}$	$I_{\text{nsat}} = I_{\text{psat}}$	VT_{i}
IV	$VT_{\text{i}} \le V_{\text{in}} \le VDD - VT_{\text{p}}$	$I_{\text{nlin}} = I_{\text{psat}}$	—
V	$VDD - VT_{\text{p}} \le V_{\text{in}} \le VDD$	$I_{\text{n}} = I_{\text{p=0}}$	0

TABLE III
MOSFET Model Parameters (Run N26D, $T_o = 20°C$)

Parameter	Units	Mean	Standard Deviation
n-FET Results			
VT_o	V	0.69±	0.0101
KP_o	$\mu A/V^2$	69.00±	1.2000
ΔW	μm	0.46±	0.0200
ΔL	μm	0.46±	0.0116
p-FET Results			
VT_o	V	0.95±	0.0087
KP_o	$\mu A/V^2$	23.00±	0.5200
ΔW	μm	0.30±	0.0310
ΔL	μm	0.35±	0.0180

$$I_{\text{psat}} = (\beta_p/2)(VDD - V_{\text{in}} - VT_{\text{p}})^2 \quad (4)$$

where $\beta = KP \cdot W_e/L_e$ and VT is the threshold voltage. For p-FET's VT is the magnitude of the threshold voltage. Also $KP = \mu C_{\text{ox}}$, where μ is the channel mobility, and C_{ox} is the gate oxide capacitance/area. Finally $W_e = W - \Delta W$ and $L_e = L - \Delta L$ where W and L are the as-drawn channel width and length, respectively, ΔW and ΔL are the channel width and length correction factors, respectively. The MOSFET values used in the following analysis are shown in Table III.

III. Spontaneous Cell Flip Behavior

The key to the measurements presented here is the spontaneous flip behavior described by the transfer curves shown in Fig. 5. As seen in the figure, the memory cell has two stable states and one metastable state. One stable state is inscribed by a triangle and is located at $V1 = 5$ V and $V2 = 0$. The

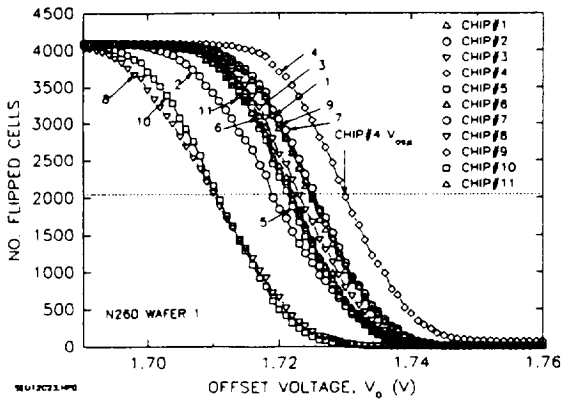

Fig. 6. SEU/SRAM spontaneous flip response from 11 chips taken from 1.2-μm CMOS wafer 1.

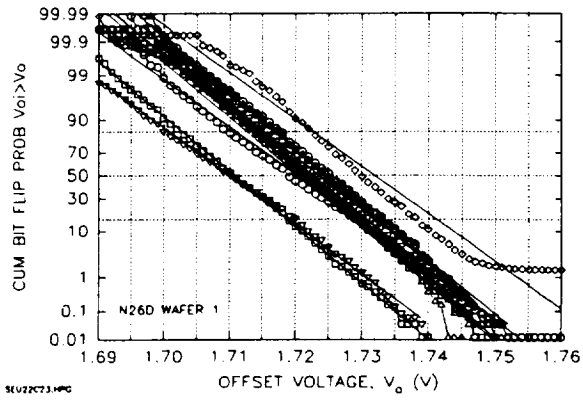

Fig. 7. Cumulative distribution plots for the chips shown in Fig. 6.

other stable state is identified by the circles. The metastable states are inscribed by squares. A stable state is a bias state to which the inverter will return if momentarily biased away from by noise. If an inverter is debiased from a metastable state, it will not return to the metastable state but will proceed to a stable state.

The initial state of the cell for $V_o = 5$ V, is located at the upper left-hand corner of the chart. As V_o decreases from 5 V, the stable point follows a path described by the circles and the metastable point follows a path described by the squares. When the circles meet the squares, the cell flips to the stable point described by the triangle. This occurs when $V_o = 1.5$ V and is termed the spontaneous flip voltage, V_{os}. At this point the cell has only one stable point described by the triangle.

In essence, the transfer curve of INV2 is used to probe the transfer curve of INV1. In this process the metastable point for the cell is determined.

The above process takes place by operating the SRAM through the Write, Stare, and Read cycles. That is, with $V_o = 5$ V, the cells are written into the circle state. The V_o is carefully lowered somewhat and returned to 5 V. Then the cells are Read to see how many have flipped. Then the process is repeated; that is, V_o is lowered to an even lower bias and returned to 5 V. Again the cells are Read and the number of flipped cells noted. This process is repeated until all the cells have flipped.

In terms of measurement technology, the external stimulus is a DAC that provides the voltage, V_o. The ADC action is provided by each cell which serves as a 1-bit comparitor. This means that the ADC action is taking place on-chip within each cell.

IV. Experimental Results

The memory cell V_o distributions are shown in Fig. 6 for 11 chips, from Wafer 1. As seen in Fig. 6, the SRAM's have a distribution of offset voltages at which the cells flip. As mentioned above, the data is acquired by lowering the offset voltage, V_o, and counting the number of flipped cells at that V_o value. The memory is then reset and the offset voltage lowered to a new V_o that is 1 mV lower than the previous value and again the number of flipped cells determined. This process is repeated until all 4096 cells flip. Note that these curves are completely deterministic within the limits of noise. That is for a given V_o, the same cells flip. The noise limit for these measurements was about 5 cells.

The distributions shown in Fig. 6 are Gaussian in nature and can be characterized by the normal distribution with a mean of $V_{os\mu}$ and a standard deviation of $V_{os\sigma}$. The cumulative distribution plots for the chips shown in Fig. 6 are shown in Fig. 7. This data is characterized by the cumulative probability function using:

$$P(V_{oi} > V_o) = 100 \cdot (N - 0.5)/N_t \tag{5}$$

where N is the number of flipped cells at V_o and for this memory $N_t = 4096$. The analytical formula that describes the cumulative distribution is

$$N = N_t\{1 - \text{erf}\,[(V_o - V_{o\mu})/V_{o\sigma}\sqrt{2}]\}/2 \tag{6}$$

where erf is the error function. The result of a least squares fit to each of the curves shown in Fig. 7 is listed in Table IV. The entire range of data was fitted. Notice that the curves with the largest standard deviations, namely, chips 2 and 4, have cells that deviate significantly from the main distribution. For chip 4, the problem is a stuck column and for chip 2, the problem is a stuck bit.

The standard deviations for these devices is the tightest observed to date being about 8 mV. Previously observed standard deviations for a 1.6-μm CMOS process were about 10 mV [5].

Selected chips are examined in detail in Figs. 8 to 10 where the cumulative and residual distributions are shown. The cumulative distribution allows a critical examination of the tails of the distribution. The residual distribution allows a critical examination of the deviation of the response from the fitted behavior. An example of a stuck column is shown in Fig. 8 and a stuck cell is shown in Fig. 9. Acceptable behavior is shown in Fig. 10.

The scale for the vertical axes in Fig. 7 is expressed in terms of probabilities. This is equal to the scales used to describe the vertical axes shown in Figs. 8 to 10 which are expressed in terms of sigmas. The number of sigmas is $(V_o - V_{o\mu})/V_{o\sigma}$. The relation between the number of sigmas and probability is listed in Table IV [8].

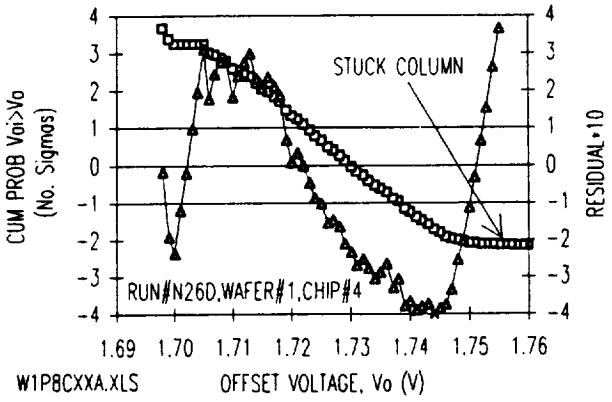

Fig. 8. Results from chip 4 (Fig. 6) showing a stuck column. The squares are the cumulative probability and the triangles are the residual.

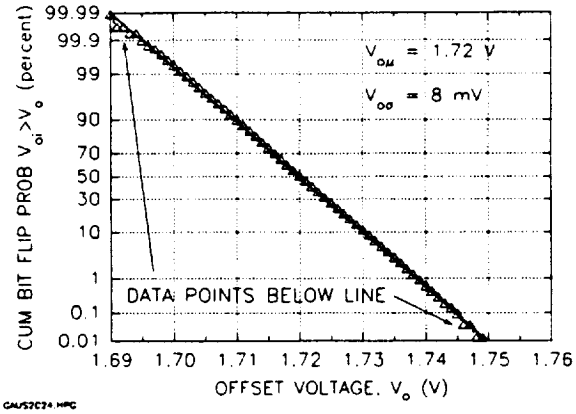

Fig. 11. Ideal cumulative distribution plot for $V_{o\mu} = 1.72$ V and $V_{o\sigma} = 8$ mV.

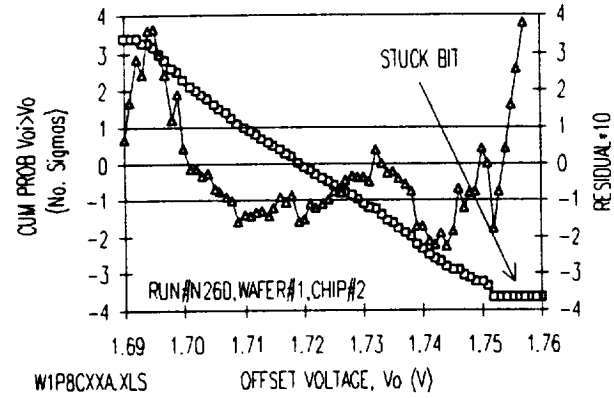

Fig. 9. Results from chip 2 (Fig. 6) showing a stuck bit. The squares are the cumulative probability and the triangles are the residuals.

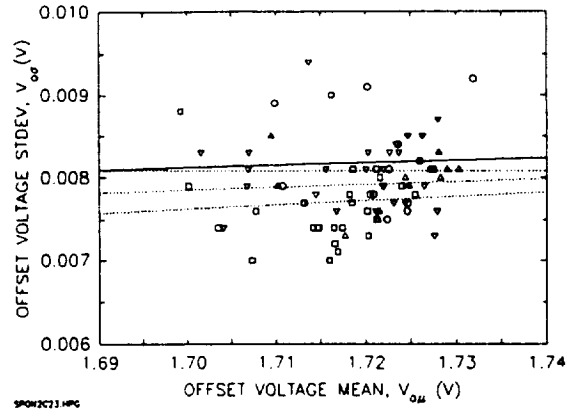

Fig. 12. Standard deviation vs. mean offset voltage for chips fabricated on four wafers. The lines are linear regression fits to data from each wafer.

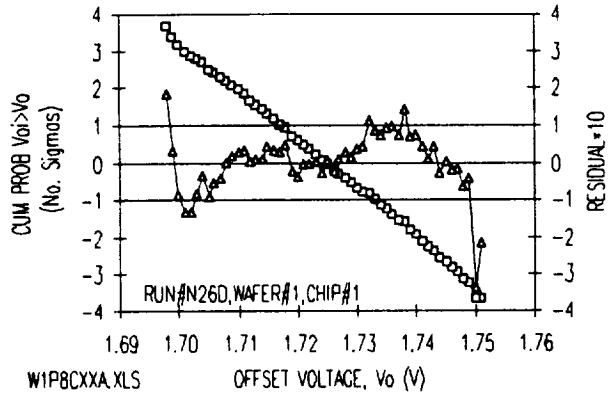

Fig. 10. Results from chip 1 (Fig. 6) showing acceptable behavior. The squares are the cumulative probability and the triangles are the residuals.

TABLE IV
CUMULATIVE DISTRIBUTION PROBABILITIES RELATED TO THE NUMBER OF SIGMAS [8]

Number of Sigmas	Cumulative Probability
4	0.99997
3	0.99865
2	0.97724
1	0.84135
0	0.50000
−1	0.15865
−2	0.02276
−3	0.00135
−4	0.00003

The results were simulated using a normally distributed sample data set. As seen in Fig. 11, several data points fall slightly below the fitted line in the tails of the distribution. This same behavior was also observed in the experimental data shown in Fig. 10 and so is considered normal for the tails of the distribution.

A summary of the results from all the wafers included in this study are shown in Fig. 12. These samples came from four wafers and are tightly clustered. The mean offset voltage has a span of 30 mV and the standard deviation of the offset voltage varies from 7 to 9 mV. This is considered excellent cell distributions for cells located 1) within a chip, 2) between chips, and 3) between wafers.

V. Data Analysis

The interpretation of results follows from observing the nature of the transfer curves shown in Fig. 5. A close examination of this figure reveals that the spontaneous flip point is determined when V_o reaches the threshold voltage of inverter 1, VT_{i1}. The CMOS inverter threshold voltage is determined

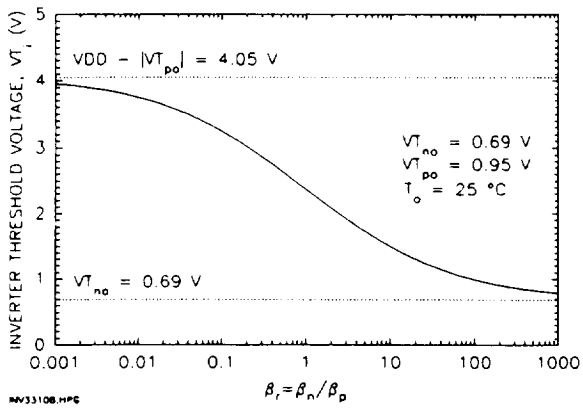

Fig. 13. Inverter threshold voltage dependence on the MOSFET geometry factor β_r.

by the conditions given in region III (see Table II):

$$VT_i = \frac{VDD + VT_n\sqrt{\beta_r} - VT_p}{1 + \sqrt{\beta_r}} \tag{7}$$

where VT_n is the n-MOSFET threshold voltage, and VT_p is the magnitude of the p-MOSFET threshold voltage. The Beta factor is

$$\beta_r = \frac{\beta_n}{\beta_p} = \frac{KP_n(W_n - \Delta W_n)(L_p - \Delta L_p)}{KP_p(W_p - \Delta W_p)(L_n - \Delta L_n)} \tag{8}$$

The inverter threshold equation is plotted in Fig. 13 and shows that for $\beta_r = 0$, $VT_i = \mathrm{VDD} - VT_p$ and for $\beta_r \to \infty$, $VT_i = VT_n$.

Using propagation of error analysis, the variance of the inverter threshold voltage is

$$VT_{i\sigma^2} = \frac{VT_{p\sigma}^2}{(1+\sqrt{\beta_r})^2} + \frac{\beta_r VT_{n\sigma}^2}{(1+\sqrt{\beta_r})^2} + \frac{\beta_r(VDD - VT_n - VT_p)^2}{4(1+\sqrt{\beta_r})^4} G \tag{9}$$

where

$$G = \frac{W_{n\sigma}^2}{W_{en}^2} + \frac{W_{p\sigma}^2}{W_{ep}^2} + \frac{L_{n\sigma}^2}{L_{en}^2} + \frac{L_{p\sigma}^2}{L_{ep}^2}. \tag{10}$$

These equations show that for $\beta_r = 0, VT_i = (VDD - VT_{p\mu}) \pm VT_{p\sigma}$ and for $\beta_r \to \infty, VT_i = VT_{n\mu} \pm VT_{n\sigma}$.

Using (7) and (8), the spontaneous flip voltage was calculated to be 1.48 V. This was determined by first calculating $\beta_{r1} = 10.7$ and $\beta_{r2} = 15.1$. Then $VT_{i1} = 1.48$ V and $VT_{i2} = 1.39$ V were calculated and the assignment was made that $V_{os} = VT_{i1} = 1.48$ V. This value compares with the experimentally observed average value for V_o of 1.72 V as displayed by the data shown in Fig. 12.

The discrepancy between 1.48 V and 1.72 V is explained by the simplistic MOSFET model given in (1)–(4). If channel length modulation was included in the MOSFET model, then the transfer curve for INV1 would have a finite slope at the midpoint of its transfer curve. This effect will increase the modeled spontaneous flip point from 1.48 V and bring the result closer to the experimental average value of 1.72 V.

TABLE V
SEU/SRAM V_o RESULTS

	WAFER 1	
Chip	$V_{o\mu}$	$V_{o\sigma}$
1	1.7246	0.0076
2	1.7202	0.0091
3	1.7226	0.0081
4	1.7319	0.0092
5	1.7209	0.0078
6	1.7224	0.0075
7	1.7247	0.0077
8	1.7099	0.0089
9	1.7236	0.0084
10	1.7108	0.0079
11	1.7205	0.0078

The standard deviation of V_{os}, $V_{os\sigma}$, is due to the variation in the n-FET threshold voltage. This can be verified by introducing the FET model parameters, listed in Table III, into (9) and (10). This leads to

$$VT_{i\sigma}^2 = 0.055 \cdot VT_{p\sigma}^2 + 0.586 \cdot VT_{n\sigma}^2 + 0.008G \tag{11}$$

for inverter 1. A close examination of this equation reveals that the coefficients are small except for the $VT_{n\sigma}$ term. Thus it is the dominant parameter.

Now the results in Fig. 12 and Table V can be summarized as follows. The mean offset voltage is determined by the inverter threshold voltage of inverter 1, that is,

$$V_{os\mu} \sim VT_{i1} \tag{12}$$

and the standard deviation of the offset voltage is determined by the variation in the threshold voltage of the n-FET in inverter 1, that is,

$$V_{os\sigma} \sim VT_{n\sigma 1}. \tag{13}$$

The result, given in (12) and (13), is a function of the layout of INV1. Thus by changing the layout of the cell, other features of the cell can be sensed. In this case, $\beta_{r1} = 10.7$ is relatively large which emphasizes VT_{n1}. If β_{r1} were made small, then VT_{p1} could be monitored.

VI. CONCLUSION

The SEU/SRAM provides data on the uniformity of a CMOS process. The 4-kbit SRAM memory cell offset voltages were found to be normally distributed. The offset voltage depends on the threshold voltage of inverter 1 and its distribution depends on the variation in VT_{n1}. Cumulative distribution plots reveal SRAM's with stuck bits and other anomalies which appear in the tails of the distribution.

The observed threshold voltage variances were about 8 ± 1 mV for all "good" chips. Since this variance applies to within a chip, chip-to-chip, and wafer-to-wafer values, it is considered excellent threshold-voltage control. This result provides a measure of excellence to be met by future CMOS foundry runs.

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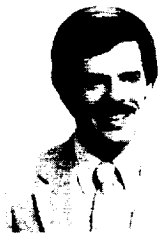

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Clementine RRELAX SRAM Particle Spectrometer

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ABSTRACT

The Clementine RRELAX radiation monitor chip consists of a p-FET total dose monitor and a 4-kbit SRAM particle spectrometer. Eight of these chips were included in the RRELAX and used to detect the passage of the Clementine (S/C) and the innerstage adapter (ISA) through the earth's radiation belts and the 21-Feb 1994 solar flare. This is the first space flight for this 1.2-μm rad-soft custom CMOS radiation monitor. This paper emphasizes results from the SRAM particle detector which showed that it (a) has a detection range of five orders of magnitude relative to the 21-Feb solar flare, (b) is not affected by electrons, and (c) detected microflares occurring with a 26.5-day period.

1. INTRODUCTION

The Clementine spacecraft was launched January 25, 1994 (day 25) from Vandenberg Air Force Base on a Titan IIG booster. The spacecraft, shown in Fig. 1, contains a number of advanced light weight cameras used to photograph the moon during its 2.4-month lunar orbit. The S/C and ISA also contain a RRELAX (Radiation and Reliability Assurance Experiment) which was located on the S/C and ISA as seen in Fig. 1.

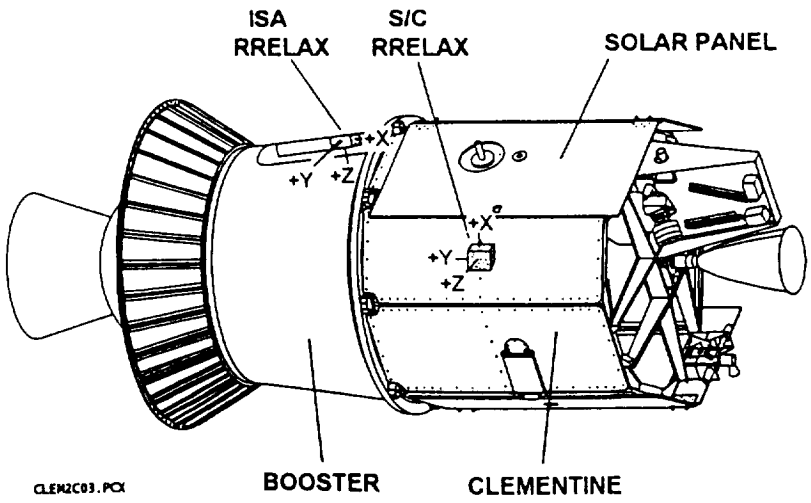

Figure 1. Launch configuration for the Clementine spacecraft (S/C) and the inner stage adapter (ISA) with a RRELAX box mounted on each. The S/C RRELAX is actually located on the opposite panel.

The total dose profile for the S/C is shown in Fig. 2. These measurements were obtained from p-FETs which were measured with a constant current set to the temperature-insensitive point [1]. The figure shows the passage of the S/C through the earth's electron belt followed by moon orbit which began on day 50. Shortly after beginning moon orbit, a solar flare was encountered on day 52. After leaving the moon on day 123 the S/C again passed through the earth's radiation belt and shortly thereafter ceased operation.

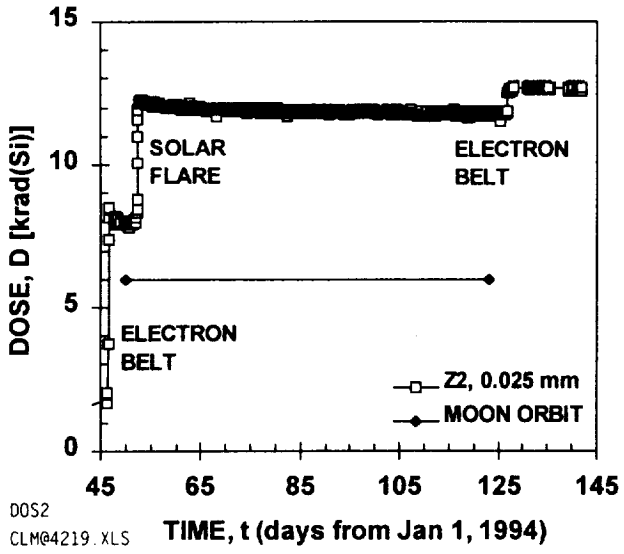

Figure 2. Overview of the S/C p-FET dose profile for lightly shielded device Z2.

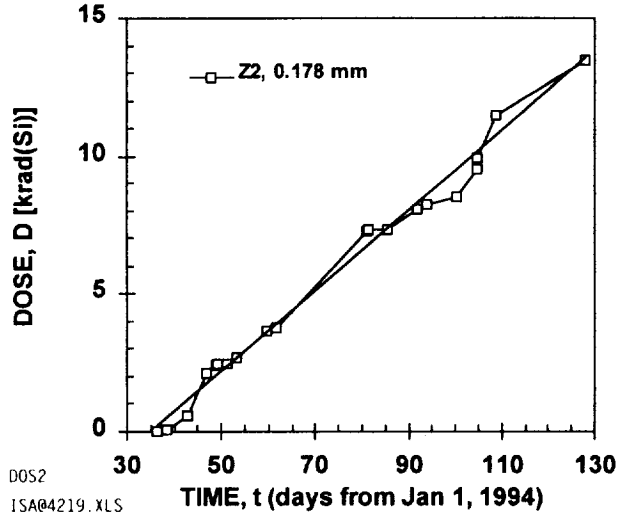

Figure 3 Overview of the ISA p-FET dose profile for lightly shielded device Z2.

The total dose profile for the ISA is shown in Fig. 3. The ISA was in a 2.1-day earth orbit from Feb 4 (day 35) until it re-entered the atmosphere on about May 8 (day 128). During this time it experienced essentially a linear increase in total dose as shown in Fig. 3. The solar flare was not visible in the ISA p-FET data because the ISA is more heavily shielded than the S/C.

2. RRELAX

The RRELAX is a 624 g, 2.4 watt microprocessor controlled experiment, shown in Fig. 4, that contains 166 test devices designed to evaluate the effects of radiation and the thermal environment on the performance of these devices. This paper discusses results from six RADMONs (Radiation Monitors), Z2, Z3, Z5, Z4, X1, and Y1 mounted on X-, Y-, and Z- faces of the RRELAX.

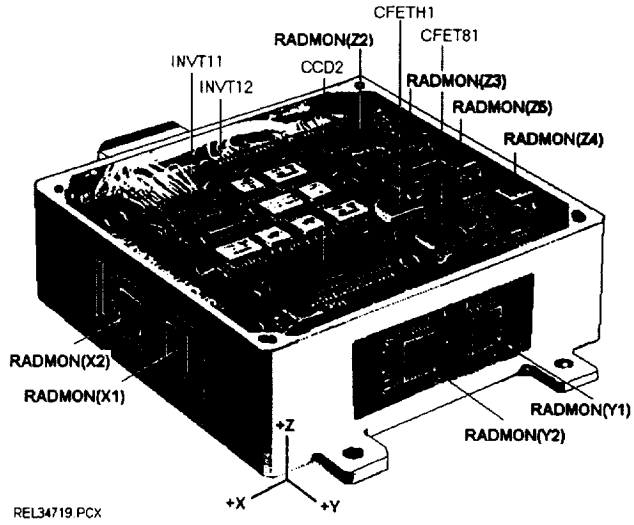

Figure 4. RRELAX components arranged in a 10.2 cm x 10.2 cm x 3.8 cm box.

3. SRAM PARTICLE SPECTROMETER

The RADMON chip, shown in Fig. 5, was fabricated in 1.2-μm radiation-soft CMOS. The chip is a full custom designed chip that contains seven components. In this paper only the results from the p-FET and the 4-kbit SRAM are presented. The p-FET was used to determine the total radiation dose and the SRAM was used to determine the particle flux.

The SRAM as a particle detector enhances the single-event-upset (SEU) effect that is detrimental to SRAMs when used as memory elements [2]. The SRAM has a six-transistor cell with an offset voltage, V_0, to adjust the sensitivity of the cell to particle upsets induced by for example protons [3] or alpha particles [4]. In addition, the sensitive drain of the n-FET was bloated to A_0 = 42.1 μm^2 so the 4-kbit SRAM active area is 0.0017 cm^2.

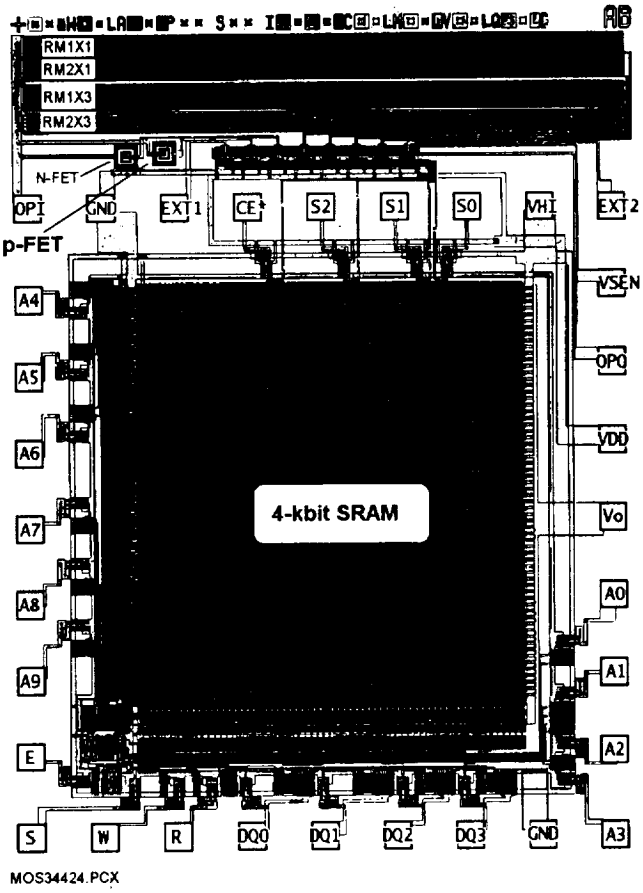

Figure 5. RADMON chip 2.6 x 3.4 mm^2 fabricated in 1.2-μm CMOS contains both a p-FET total dose monitor and an SRAM particle detector.

The calibration of the cell, shown in Fig. 6, used both protons and alpha particles. The experimental data points were obtained at various incident ion energies, E2, for an offset voltage that corresponds to a cross section of $A_0/2$. The cross section is the upset rate divided by the particle flux times the number of cells which is 4096 in this case. The solid lines were fitted to the experimental data using the deposited ion energy derived from the range-energy curves [5]. These calculations require the overlayer thickness, DX3, and the collection layer thickness DX4. Values for these thicknesses are shown in the figure. The deposited energy is expressed as the difference between the energy at the start of the collection layer, E3, and the energy at the end of the collection layer, E4. During the rising portion of the curve, the ions stop in the collection layer and so E4 = 0. Finally, the offset voltages are stated relative to the spontaneous offset voltage $V_{os\mu}$ = 1.148 V.

The SRAM was operated with two threshold voltages which were 0.15 V and 1.0 V above the spontaneous upset point, $V_{os\mu}$. As seen in Fig. 6 for DV_0 = 0.15 V, protons in the 0.55 to 0.8 MeV range can upset the SRAM and alpha particles with energies above 1.8 MeV can upset the SRAM. When operated with this threshold, the SRAM is said to be sensitive to particles with atomic numbers of Z≥1. For DV_0 = 1.0 V only heavy ions such as oxygen or iron can upset the SRAM.

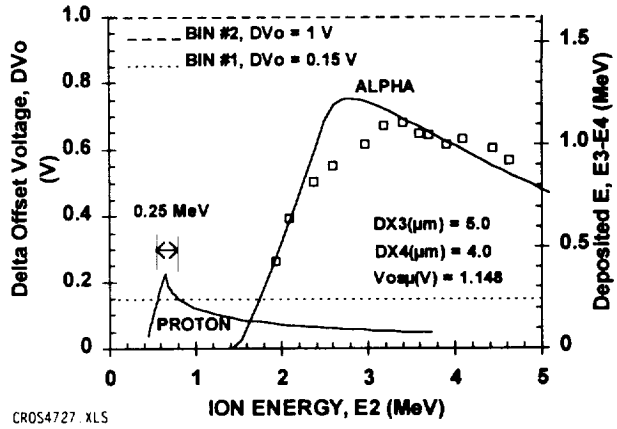

Figure 6. Calibration curves and operational thresholds for the SRAM particle detector.

In operation [6], the SRAM is written with ones with V_0 = VDD = 5 V. Then V_0 is lowered to a value DV_0 above $V_{os\mu}$ for a stare period of 100 s. Then V_0 is returned to VDD and the number of zeros or particle flipped cells read. In addition to lowering V_0, the VDD for the chip was also lowered to 3 V to reduce the chip power consumption. During satellite operation,

each SRAM was operated for 100 s with DV_0 = 0.15 V and then for 100 s with DV_0 = 1 V. This cycle was continued for 1 hour. The number of upsets reported is the sum of the upsets recorded during the 18 x 100 s = 30 minutes that the SRAM spent in each state.

The RADMONs were shielded by different lids as listed in Table 1. The devices were packaged

Table 1. Shields in mm and Normal Incident Proton Energy in MeV.

DEV NO.	NO. LIDS	S/C mm	S/C mil	S/C MeV	ISA mm	ISA mil	ISA Mev
Z2	0	0.025	1	1.3	0.178	7	4.6
Z3	1	0.787	31	11.4	0.940	37	12.7
Z5	2	1.549	61	16.9	1.702	67	17.8
Z4	3	2.311	91	21.1	2.464	97	21.9
X1	1	0.787	31	11.4	0.940	37	12.7
Y1	1	0.787	31	11.4	0.940	37	12.7

with an integral number of 0.25-mm Kovar lids. A conversion factor of three was used to convert Kovar thickness to Al thickness. That is 1 mm of Kovar is equivalent to 3 mm of Al. The 0-lid device was covered with 13-μm Al-coated Kapton and the RRELAX box was similarly covered with this Kapton. Thus the 0-lid device is listed as having a 25-μm Al shield. The equivalent thickness of each shield in mm and mils of Al is listed in Table 1. These numbers represent the thickness of the lid, box covering, and, for the ISA RRELAX, 0.152-mm thermal blanket.

The mean proton energy needed to penetrate the shield and upset the SRAM when operated with DV_0 = 0.15 V is also listed in Table 1. The values shown in the table were obtained from proton range-energy curves [5]. The shields slow the protons so their energy is reduced to between 0.55 and 0.8 MeV when they reach the collection region of the SRAM and thus can cause an upset.

4. TEST RESULTS

An overview of the S/C and ISA SRAM particle detector data is presented in Figs. 7 to 9 for Z≥1 and heavy ion particles. Zero upsets are shown as 0.2 upsets. The 21-Feb solar flare is clearly visible at day 52 in Figs. 7 to 9.

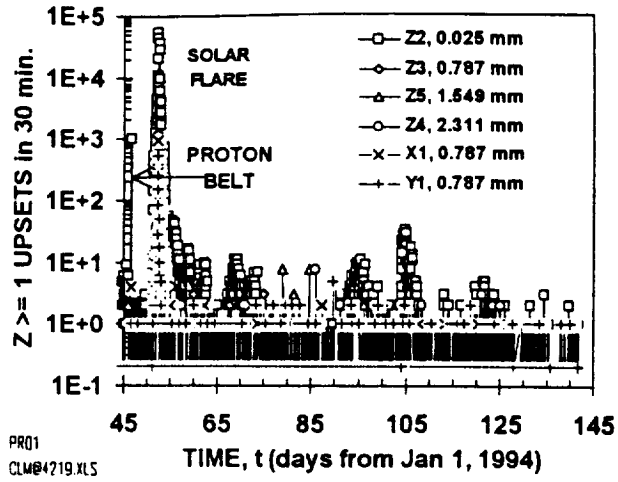

Figure 7. Overview of the Z≥1 upsets for S/C Z2, Z3, Z5, Z4, X1, and Y1 SRAMs.

The data shown in Fig. 8 was heavily censored for there were a great many system glitches of unknown origin on the ISA which caused massive SRAM upsets. These upsets are most likely due to noise on the power supplied to the RRELAX. Thus, a lesson learned is that the power supply must be stable especially during the 100 s stare period.

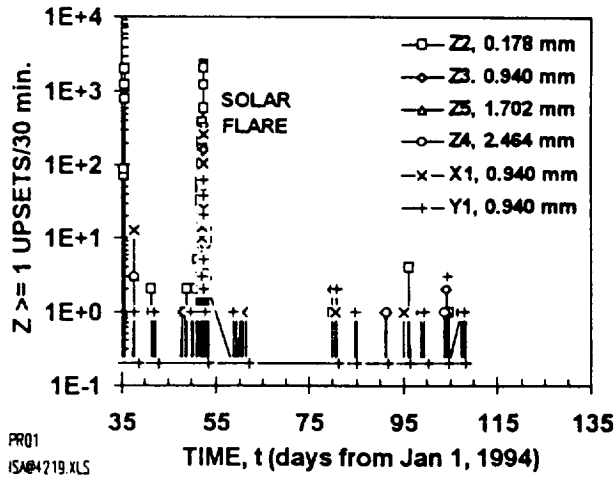

Figure 8. Overview of the Z≥1 upsets for ISA Z2, Z3, Z5, Z4, X1, and Y1 SRAMs.

As shown in the following figures, most upsets follow a pattern where the lightly shielded SRAMs have more upsets than the heavily shielded SRAMs. As seen in Figs. 7 to 9, this pattern is broken during quiet times when the

background radiation can upset the more heavily shielded SRAMs more often than the lightly shielded SRAMs.

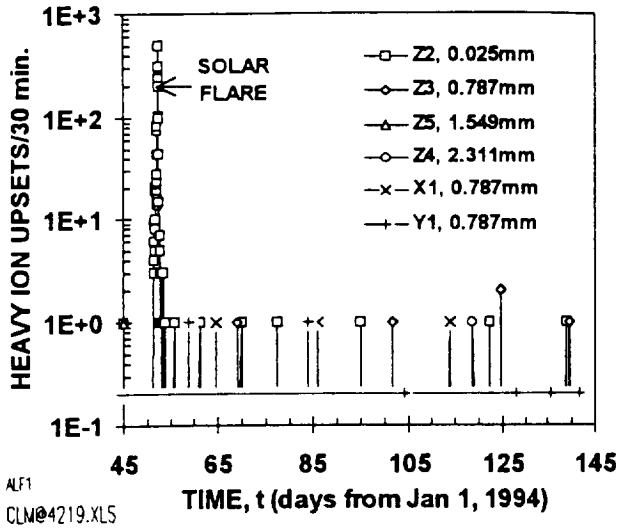

Figure 9. Overview of the heavy ion upsets for S/C Z2, Z3, Z5, Z4, X1, and Y1 SRAMs.

The effect of shielding on the 21-Feb solar flare is shown in Fig. 10. The shielding thickness is listed in the legend and the corresponding protons energies are listed in Table 1. The figure illustrates how the upsets decrease with shielding thickness.

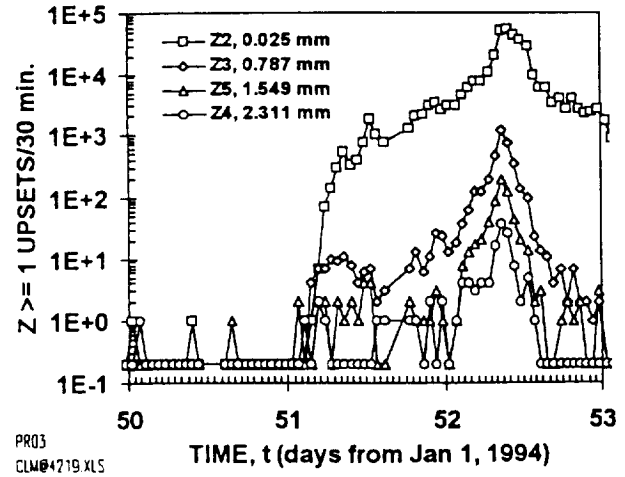

Figure 10. Effect of shielding on the upset response of the S/C Z2, Z3, Z5, and Z4 SRAMs during the 21-Feb solar flare.

The energy dependence of proton flux at the solar flare peak is shown in Fig. 11. This data was corrected for the reduction in the memory cell count during the stare cycle using $N_0 = -N_t \cdot \ln(1 - N/N_t)$ where $N_t = 18 \cdot 4096$ and N is the number of upsets shown in Fig. 10. The field-of-view was assumed to be π sr. As seen in Fig. 10 for Z2, N = 56,503 and N_0 = 107,202.

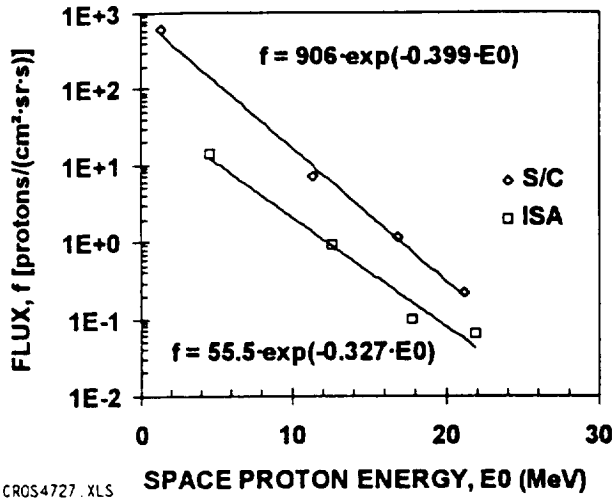

Figure 11. Peak proton flux energy dependence for the 21-Feb solar flare for S/C and ISA.

As seen in Fig. 11, the flare was more intense for the S/C than for the ISA. In comparison with other worst case flares [7], this flare was several orders of magnitude lower in its intensity.

The effect of orientation is shown in Figs. 12

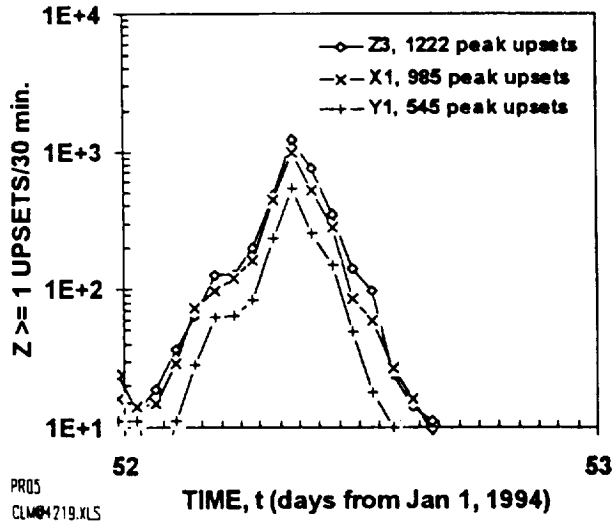

Figure 12. Effect of orientation on the upset response of the S/C Z3, X1, and Y1 SRAMs during the 21-Feb solar flare.

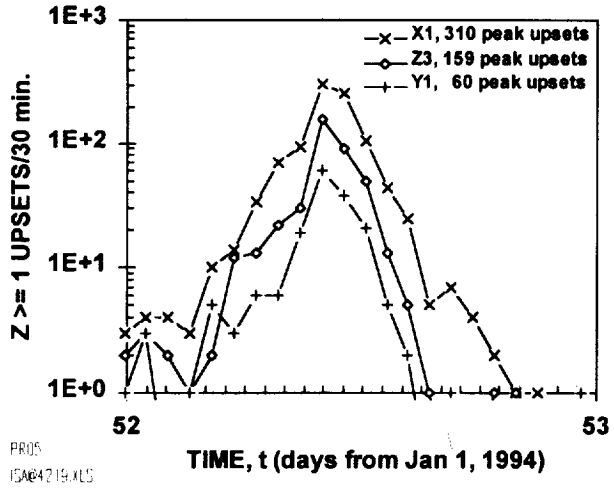

Figure 13. Effect of orientation on the upset response of the ISA Z3, X1, and Y1 SRAMs during the 21-Feb solar flare.

and 13. The ordering of the data follows approximately the field-of-view of each SRAM as seen in Fig. 1.

For the S/C, the field-of-view or solid angle for the Z-axis is approximately 2π; whereas, for the X- and Y- axes, it is closer to π. Thus the Z-axis should have the most upsets but the curves for the X- and Y- axes should be closer. For the ISA, the field-of-view is largest for the X-axis and smallest for the Y-axis. The ISA contains a large spherical tank the occludes the RRELAX field-of-view. The ISA results fit intuition better than the S/C results.

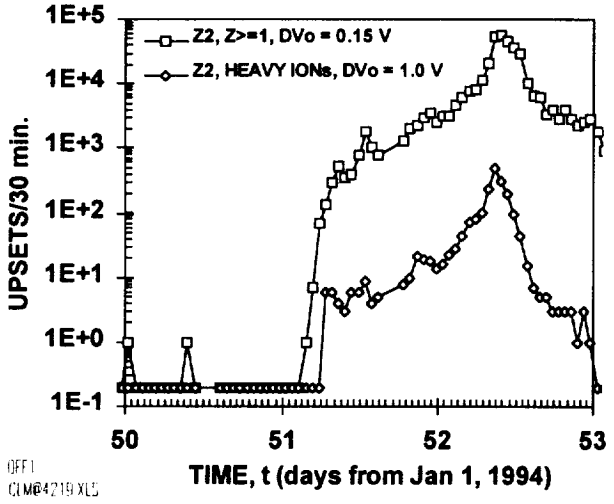

Figure 14. Effect of thresholding on the upset response of the S/C Z2 SRAM during the 21-Feb solar flare.

The effect of thresholding on upsets is shown in Figs. 14 and 15. These figures indicate that the number of upsets decreases as the threshold increases. The upper curve is due to $Z \geq 1$ particles and the lower curve is due to heavy ions. This shows how the SRAM is used to electronically discriminate between light and heavy particles. In Fig 14, there is a significant shift between the light and heavy particle responses.

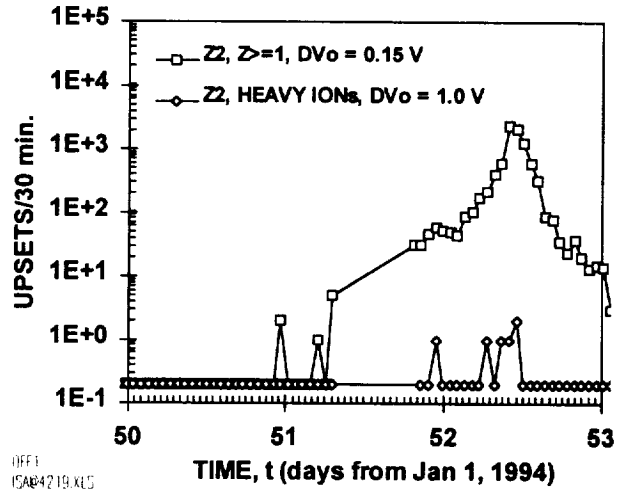

Figure 15. Effect of thresholding on the upset response of the ISA Z2 SRAM during the 21-Feb solar flare.

A comparison of the p-FET and SRAM response is shown in Fig. 16 during the passage of the S/C through the earth's radiation belts. First the SRAM is upset by protons in the proton belt and then the p-FET is dosed by electrons in the electron belt. The p-FET responds to total ionizing charge; whereas, the SRAM responds only to ion strikes and not electrons.

The 21-Feb solar flare response of the S/C Z3 SRAM was compared to the GOES-7 particle detector in Fig. 17. During the flare, the S/C was in moon orbit and the GOES-7 in geosynchronous orbit. This explains the one-hour shift in the responses.

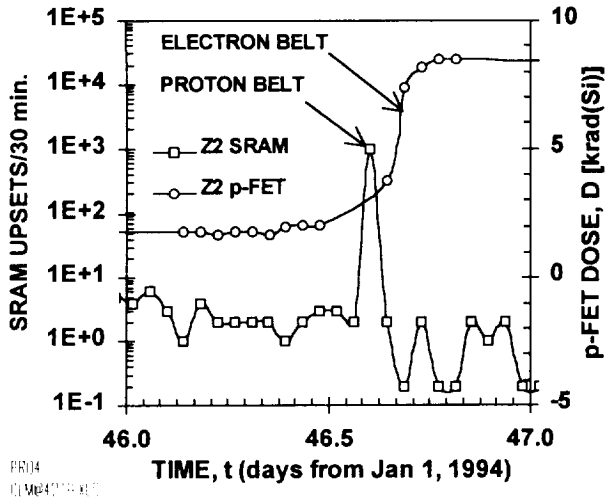

Figure 16 Response of the S/C Z2 p-FET which detected the electron belt passage and the SRAM which detected the proton belt passage.

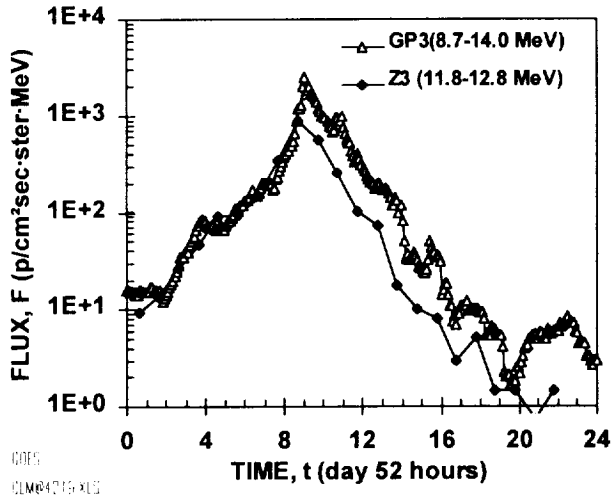

Figure 17. Comparison of the GOES-7 particle spectrometer with the S/C Z3 SRAM detector.

Two microflare series are shown in Fig. 18 for the Z2 SRAM. This SRAM is very lightly shielded with a 25-μm Al shield which means that it responds on the average to 1.3 MeV protons. Note the data shown in the figure was not corrected for memory cell depletion during the stare cycle.

The microflare at day 105 is apparently associated with the 21-Feb solar flare. This feature was also seen in the SAMPEX's [8] MAST [9] data as seen in Fig 19. In this figure the

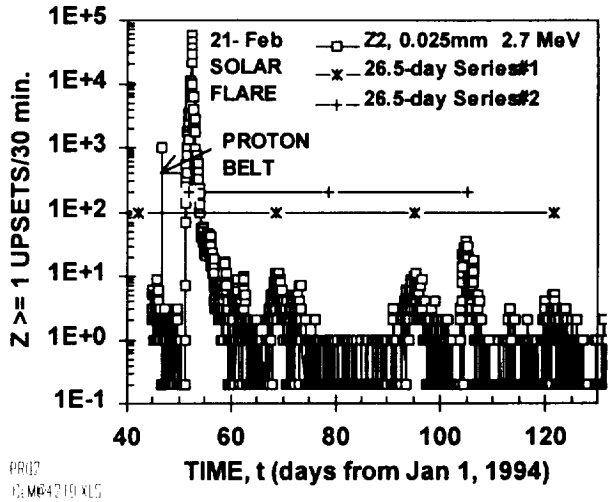

Figure 18. Microflares appear in two cycles with a 26.5-day period.

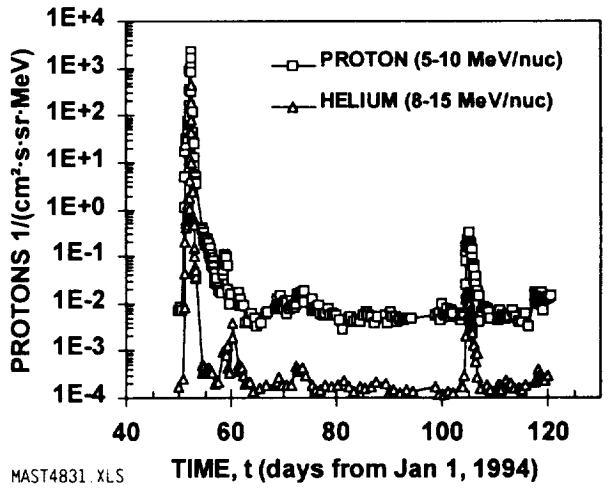

Figure 19. A microflare appears at day 105 in this data from the SAMPEX MAST detector. This feature is displaced by two 26.5-day periods from the 21-Feb (day 52) solar flare.

Series #2 upsets are due to both protons and helium ions. Notice that there is no microflare after the first 26.5-day period at day 78.5. The data shown in this figure was not corrected for detector dead time which will increase the flux near the solar flare peak.

The Series #1 microflares, seen in Fig. 18, were also observed by the SAMPEX's LEICA instrument [10]. This series is composed of 0.5 - 6.6 MeV/nuc helium atoms.

5. DISCUSSION

The upsets, shown in Fig. 19, indicate that the SRAM has a dynamic range of five orders of magnitude relative to the 21-Feb solar flare. The response in passing through the earth's radiation belts, shown in Fig. 16, indicates that the SRAM does not respond to electrons but responds only to protons.

As seen in Fig. 7. the SRAM has most upsets when it is virtually unshielded. The active area of the SRAM is 0.00172 cm^2 which is smaller than centimeter-size pin diode and surface-barrier detectors used in particle spectrometers for measuring space background radiation particles. Because the active area of the SRAM is small, its usefulness lies in analyzing higher density particles found in solar flares and the earth's radiation belts.

The spectrometer aspects of the SRAM are determined by the shielding and V_0. Shielding filters the external particle spectrum so that only those particles that fall into the energy detection window can upset the SRAM; see Fig. 6. The offset voltage, V_0, sets the upset threshold as depicted in Fig. 6 so the SRAM can discriminate between light and heavy particles.

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DEPTH MEASUREMENTS USING ALPHA PARTICLES AND UPSETABLE SRAMs

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ABSTRACT

A custom designed SRAM was used to measure the thickness of integrated circuit over layers and the epi-layer thickness using alpha particles and a test SRAM. The over layer consists of oxide, nitride, metal and junction regions.

INTRODUCTION

It is more difficult to measure the thickness of integrated circuit layers than the width. Traditional methods such as ellipsometry require areas that are large compared to integrated circuit features, and cross sectioning techniques are time consuming. In this paper, alpha particles are used to measure the over layer and collection layer using a custom SRAM.

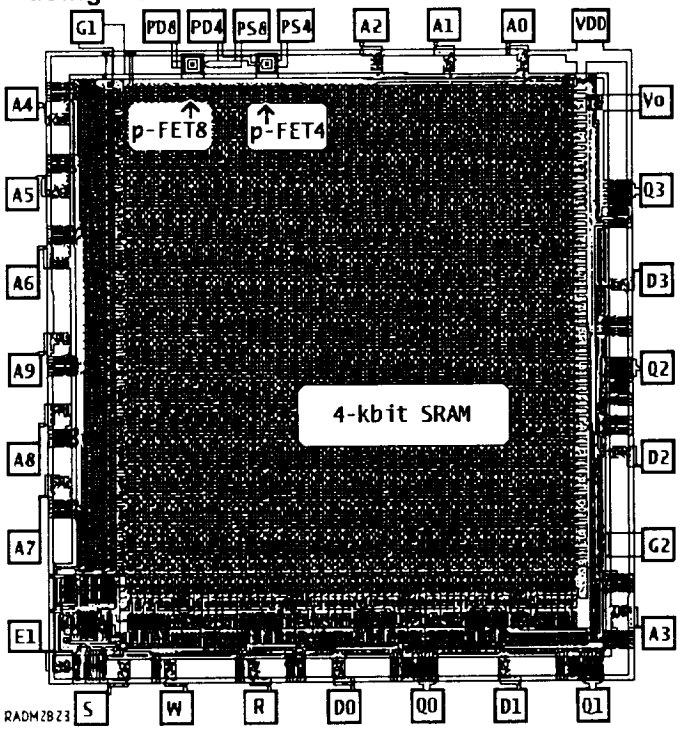

Figure 1. STRV-RADMON chip 2.57 x 2.70 mm².

This structure was designed as a radiation monitor, RADMON, and its chip-level layout is shown in Fig. 1. The device is currently flying on the Space Technology Research Vehicle (STRV-1b) in a Geosynchronous Transfer Orbit. This is a joint US-UK project designed to evaluate the effects of space radiation on advanced technology.

The device is a custom designed 4-kbit SRAM with a traditional six-transistor cell [1]. A cross-section through the two inverters which form the memory cell is shown in Fig. 2. As

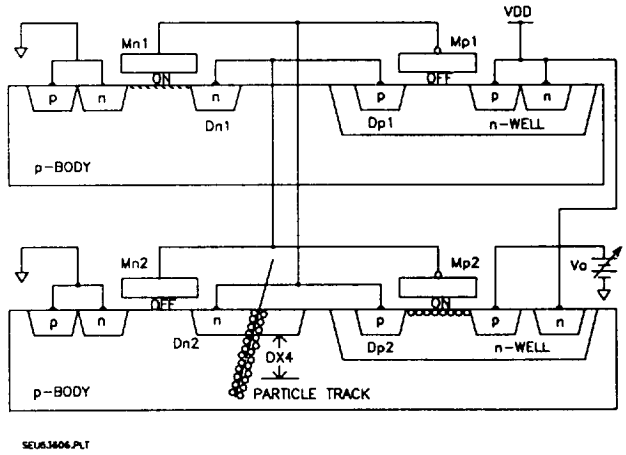

Figure 2. Cross section of the RADMON memory cell showing a particle track creating hole-electron pairs beneath drain Dn2.

indicated in the figure, particles create hole-electron pairs as they pass through the silicon and if enough charge is deposited in the collection layer, DX4, the cell will change state. In the experiments described here, the alpha energy is initially low enough so the alphas do not reach DX4. As the energy is increased the alphas enter DX4 and reach end-of-range before exiting DX4. At higher energies, the alphas pass through DX4 and reach end-of-range in the substrate. The amount of charge deposited in DX4 will vary

according to the Bragg curve. In general, the deposited charge will increase and then decrease as the alpha energy increases.

The cell features an offset voltage, V_O, connected to inverter #2. This voltage is used to increase the sensitivity of the SRAM to particle upsets by biasing the inverter relative to the cell's metastable point. When biased close to the metastable point, a particle that creates a small amount of charge in DX4 can upset the cell.

In operation the SRAM is written with all ones. Then V_O is lowered and the SRAM is placed in the stare state for a period of time during which the particles flip the cells. Then, V_O is raised and the number of zeroes read.

As indicated in Fig. 2, the drain of the n-FET, Mn2, is connected to V_O through p-FET Mp2. The drain, Dn2, of Mn2 is enlarged to increase its cross section to particles.

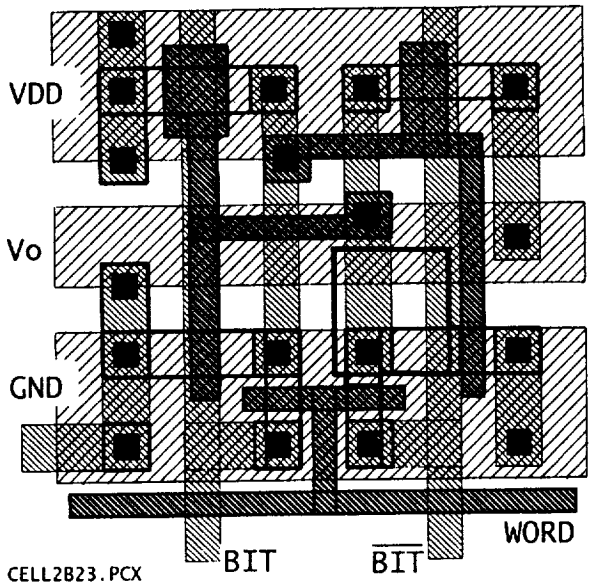

Figure 3. Memory cell layout showing the enlarged drain, Dn2, in bold outline.

This is shown in greater detail in the cell layout shown in Fig. 3 by the area outlined with a bold line. A close inspection of this region indicates that it can be subdivided into three areas each with a different over layer thickness. A cross section of the drain, Dn2, is shown in Fig. 4. There are three distinct areas: (a) no metal (M0), (b) metal-1 or metal-2, (M1&M2) or (c) metal-1 and metal-2 (M1+M2) and these are listed in Table 1. The over layer consists of the insulator layers including the deposited oxides and nitrides, the metal layers, and the diffused junction. The thickness of the three regions and the epi-layer is the subject of this paper.

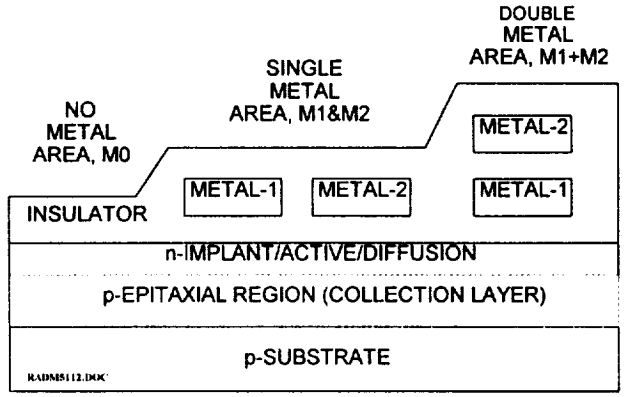

Figure 4. Cross section through sensitive diode Dn2.

Table 1. Over Layer Thickness

REGION	AREA μm²	EST DX3 μm	ALPHA DX3 μm	ALPHA DX4 μm
MO	5.6	4.0	4.3	3.3
METAL-1	7.5	4.8		
METAL-2	12.4	5.4		
M1&M2	19.9	5.3	5.2	3.6
M1+M2	16.6	6.3	6.5	3.6
TOTAL	42.1			

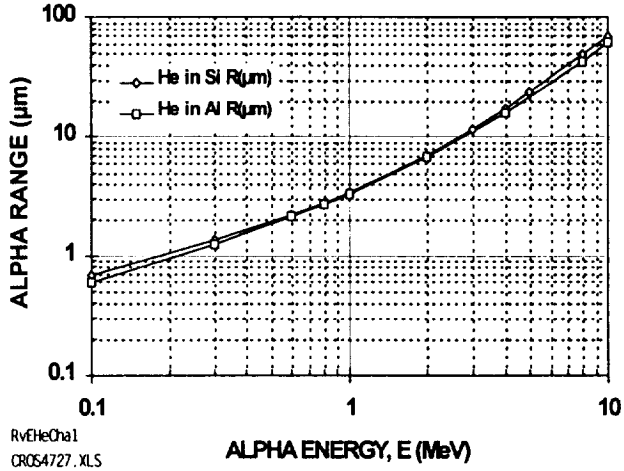

Figure 5. Alpha particle range-energy curve for silicon and aluminum [2].

The range-energy dependence of alphas in silicon and aluminum is shown in Fig. 5. This graph indicates that there is little difference in the range-energy response for

alphas in silicon and aluminum. However, for other materials the range-energy relation must be computed as discussed below.

The analysis for the over layer thickness used the energy-range curve for alphas in silicon. An algorithm was fitted to the data shown in Fig. 5. The algorithm is given in the Appendix.

The CMOS over layers consist of a number of different materials and the range of alphas in these materials was converted to an equivalent range in silicon using the Bragg-Kleeman rule [3]:

$$R1/R2 = (\rho 2/\rho 1)\cdot\sqrt{A1/A2} \qquad (1)$$

where ρ is the density and A is the atomic weight of material 1 and 2. In the analysis, material 2 is silicon and the non-silicon layer is material 1. The average thickness of each layer was obtained from the silicon broker, MOSIS. The estimated equivalent silicon thickness for each layer is listed in Table 1.

The nomenclature used to describe the thickness and energy of the layers is shown in Table 2. Experiments were performed in a vacuum of less than 10^{-4} Torr. Gold scattering foils were used to adjust the energy of the alpha particles. The energy of the alpha particles was determined using a pin diode detector and particle spectroscopy equipment. The energy of the alphas as they enter the silicon chip is given by E2.

Table 2. Layer Notation

	PARTICLE SOURCE	
X0		EO
	SCATTERING FOIL	DX1
X1		E1
	VACUUM	DX2
X2		E2
	SRAM OVER LAYER	DX3
X3		E3
	SRAM COLLECTION LAYER	DX4
X4		E4
	SRAM SUBSTRATE	DX5

EXPERIMENT

The RADMON was fabricated in a 1.2-µm CMOS process and test results are shown in Fig. 4. These results were derived using the detector equation which describes the rate at which cells are upset:

$$dn/dt = \phi\cdot A_O(N_t - n) \qquad (2)$$

where N_t = 4096 cells, ϕ is the particle flux, A_O is the memory cell cross section. In the limit where the number of upset cells is small compared with N_t, the cross section is:

$$A_O = R_O/(\phi\cdot N_t) \qquad (3)$$

where $R_O = dn/dt|_{t \Rightarrow 0}$. For this SRAM, A_O is 42.1 µm². The physical meaning of the cross section is the number of upset cells, dn, for a given ϕ, N_t, and dt, the stare time. The stare time is the time the SRAM is exposed to the alpha particles.

In these experiments, the alpha sources were Americium-241 and Gadolinium-148. The incident energy was adjusted using gold scattering foils with various thicknesses. The Am-241 flux was 145 alphas/cm²·sec with a stare time of 1000 sec. The Gd-148 flux was 87.8 alphas/cm²·sec with a stare time of 1000 sec.

The results seen in Fig. 6 indicate that the SRAM has a spontaneous (SPON) response when V_O is lowered below 1.143 V. The SPON curve has a normally distributed set of values due to the spread in cell parameters [1]. This curve is characterized by the mean value, $V_{OS\mu}$. When alpha particles strike the cell, the cells flip at higher V_O values which depend on the flux and energy of the particles.

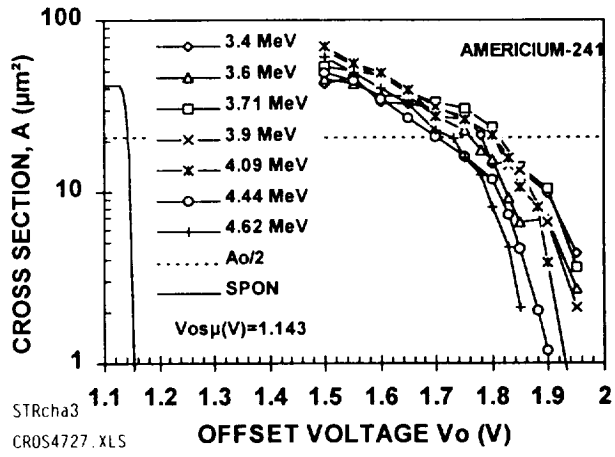

Figure 6 Upset cross section of the SRAM as a function of V_O and various alpha particles.

The Am-241 data is shown in greater detail in Fig. 7 and the Gd-148 data is shown in Fig. 8. This data shows that the cross section is significantly greater than A_O = 42.1 µm². This is due to the capture of charge that strikes active regions, such as M0 or M1&M2 or M1+M2.

The results were analyzed at $A_O/2$ and displayed as the square data shown in Fig. 9.

At $A_O/2$, half the particle flux has sufficient energy to flip the memory cells due to energy dispersion of the alpha particles. The data is shown as the differential offset voltage given by the relation: $DV_O = V_O - V_{OS\mu}$.

The data plotted in Figs. 7 and 8 shows four distinct regions if plotted as in Fig. 10. A three dimensional representation is shown in Fig. 11. Three distinct peaks are shown on the left-side of the graph and these have been correlated to the three areas of the memory cell.

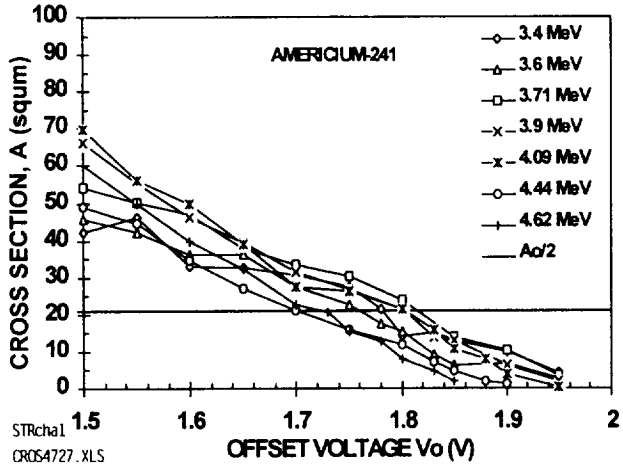

Figure 7. SRAM cross-section versus offset voltage response to Am-241 alpha particles.

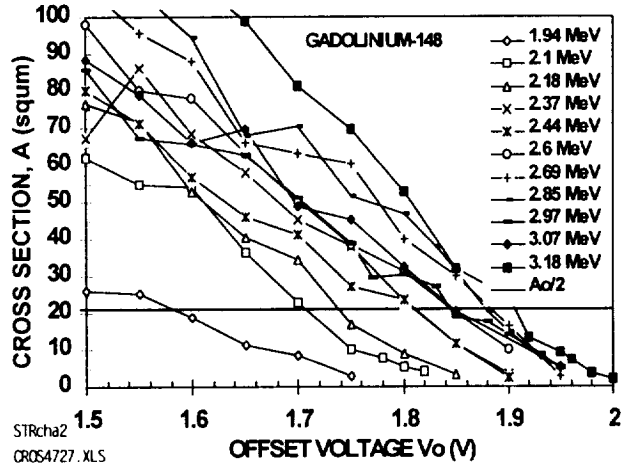

Figure 8. SRAM cross-section versus offset voltage response to Gd-148 alpha particles.

The analysis for the layer thickness is shown by the three solid lines given in Fig. 9. These curves were obtained assuming values for DX3 and DX4. These parameters were adjusted manually until a reasonable fit was obtained. The energy deposited in the over layer, DX3, is E3 - E4. The range-energy algorithms listed in the Appendix were used in these calculations. The layer thicknesses are listed in the inset of Fig. 9 and in Table 1. The thickness values listed in Table 1 are in good agreement with the thickness estimates derived from the manufacturer's target values.

The solid curves shown in Fig. 9 have three regions. In the first region, particles have insufficient energy to reach DX4 and stop in the DX3. Particles with these low energies will not upset the cells and thus $DV_O = 0$. Particles with sufficient energy will stop in DX3 and deposit sufficient charge to upset the cells. This is seen as the rising portion of the curves in Fig. 5. Finally, particles with more energy pass through DX4 and stop in DX5. This is seen as the falling portion of the curves in Fig. 5. The point at which the alphas just reach DX5 is the point at which the slope of the rising portion of the curve begins to decrease near the top of the curve.

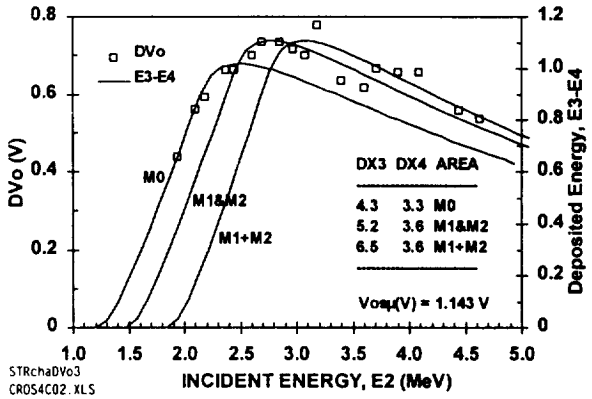

Figure 9. Particle physics fitted to experimental data showing fitted values for the over layer thickness, DX3, and the collection depth, DX4.

An additional layer, which was measured by this technique, is the epi-layer noted as DX4. Two values, 3.3 and 3.6 μm, are listed for DX4 in the inset to Fig. 9.

DISCUSSION

The use of a custom SRAM is shown to have the potential for measuring the over layer and epi-thickness of integrated circuit layers. This method is effective in measuring the thickness of both conducting and insulating layers. The method requires a knowledge of the alpha particle range-energy dependence and the conversion of the thickness of non-silicon layers to an equivalent silicon thickness.

The memory cell used in this study has regions with different over layer thicknesses

and suffers from the collection of peripheral charge. A simpler structure should be designed with a single over layer thickness on each memory cell and the cells should be designed with a channel stop to prevent the collection of peripheral charge. The memory could be designed as a scribe-line monitor and used for end-of-line over layer and epi-thickness measurements.

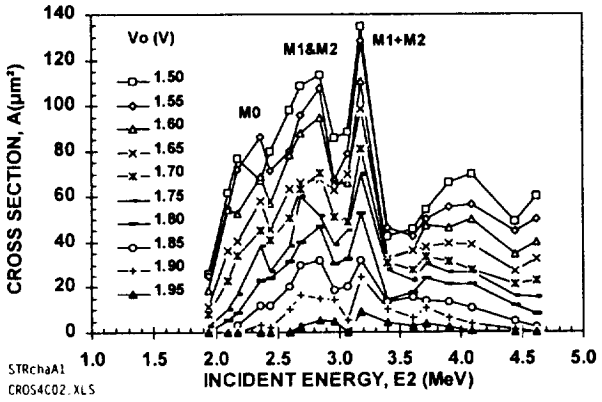

Figure. 10. SRAM cross-section versus alpha energy and V_o values showing three major peaks and one minor peak.

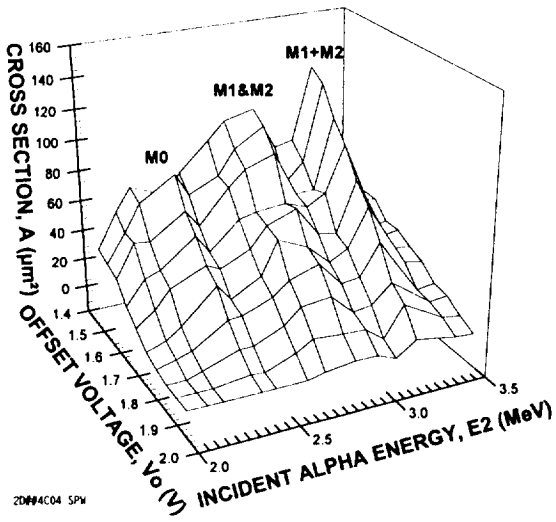

Figure 11. SRAM cross-section response due to three memory cell regions: no metal (M0), Metal-1 and metal-2 (M1&M2), and metal-1 plus metal-2 (M1+M2).

APPENDIX

The range-energy curves [2] for alpha particles in silicon shown in Fig. 4 was fitted with the following parabolic equation where E has units of MeV:

$$Y = \log_{10}(E) = a \cdot X^2 + b \cdot X + c \qquad (A1)$$

where $X = \log_{10}(R)$ and R has units of μm. The coefficients of this equation are:

$$a = -0.2867$$
$$b = 1.4395$$
$$c = -0.7151.$$

The inverse equation was determined by solving the above quadratic equation.

$$X = \log_{10}(R) = A(-1 + \sqrt{[1 - B \cdot (C - Y)]} \qquad (A2)$$

where

$$A = b/2a = -2.51046$$
$$B = 4a/b^2 = -0.55343$$
$$C = c.$$

It is essential that the inverse equation be derived from the initial a, b, c fitting parameters using this procedure. Attempting to fit the inverse relation, that is the logR vs logE curve, leads to different parameters that ruin the analysis.

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Clementine Dosimetry

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This paper presents radiation dosimetry results from the radiation and reliability assurance experiments on the Clementine spacecraft and Interstage Adapter Satellite. The dosimetry instruments utilize low-dose-response *p*-channel field-effect-transistor and proton-sensitive static-RAM dosimeters. These dosimeters successfully demonstrated an order-of-magnitude decrease in instrument weight and power from previous systems. The data confirm prelaunch predictions of the total-dose effects on charge-coupled-device dark current and on complementary-metal–oxide–semiconductor 1.2- and 0.8-μm technology design and process parameters in the space environment. A solar proton event during the early phases of the mission allowed a comparison between the Clementine measured proton fluence and energy spectra and the Geostationary Operational Environmental Satellite 6 measured proton fluence and energy spectra. These data confirmed the proton-spectrometer design and operation.

Nomenclature

a_n = second-order polynomial coefficients
C_u = upset capacitance
D_s = space-measured radiation dose
$D(T)$ = temperature-corrected space radiation dose
E_g = silicon bandgap energy
F(E) = external proton frequently
f_e = proton internal environment fraction
f_{on} = SRAM on-time fraction
G = *p*-channel field-effect transistor (*p*FET) temperature-independent circuit gain
I_D = complementary metal–oxide–semiconductor (CMOS) drain current
I_d = charge-coupled-device (CCD) dark-current damage factor, nA/cm^2 · krad
Ig = prelaunch CCD2 dark current
K = charged-particle-produced ionization per unit energy loss in silicon, fC/MeV
Kp = planetary magnetic index
k = Boltzmann's constant
N = SRAM-measured number of counts per hour
N_T = number of pixels per SRAM chip
T_s = space-measured temperature of *z* DUT board
V_c = CCD2 current-to-voltage conversion factor
V_{DD} = SRAM chip bias voltage
V_d = *p*FET temperature-independent threshold voltage damage factor, mV/krad
V_G = CMOS gate voltage
V_g = ground-measured voltage
V_o = SRAM adjustable offset voltage
V_s = space-measured voltage
V_T = CMOS threshold voltage
V_{Td} = CMOS threshold-voltage damage factor, mV/krad
V_{Ts} = CMOS space-measured threshold voltage
V_{Tt} = CMOS threshold-voltage temperature factor, mV/°C
V_0 = CCD2 extended pixel voltage mean
ΔE = static-RAM (SRAM) proton energy window width
ΔV_p = SRAM offset voltage above metastable point
σ = SRAM pixel sensitive area or "cross section"
Ω = Clementine SRAM field of view

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Introduction

THE mission goal of the Clementine Engineering Experiments Program was to evaluate the effects of the space environment on advanced Ballistic Missile Defense Organization (BMDO) technologies being flight-tested on the main Clementine spacecraft and the Interstage Adapter Satellite (ISAS). The radiation and reliability assurance experiment (RRELAX) instrument contributed to the flight qualification of advanced BMDO technologies by performing radiation dosimetry in the space environment. The RRELAX dosimetry instruments utilized Jet Propulsion Laboratory (JPL) low-dose-response *p*-channel field effect transistor (*p*FET) and proton-sensitive static RAM (SRAM) integrated-circuit chip (IC-chip) dosimeters. These dosimeters, collectively called Radiation monitors (RADMONs), demonstrated an order-of-magnitude decrease in instrument weight and power from previous systems.

Dosimetry data for the Clementine spacecraft, on Feb. 21, 1994 and April 27, 1995, and ISAS, throughout its mission, are presented in this paper. The ISAS *p*FET data confirmed prelaunch predictions of the total-dose effects on charged-coupled device (CCD) dark current and on Hewlett-Packard (HP) 1.2- and 0.8-μm technology design and process parameters in the space environment. A solar proton event during the early phases of the mission allowed a comparison between the Clementine RRELAX measured proton fluence and energy spectra and the Geostationary Operational Environmental Satellite 6 (GOES-6) measured proton fluence and energy spectra. These data confirmed the SRAM proton spectrometer design and operation.

RRELAX Experiment Design

Two identical RRELAX experiments flew on the Clementine missions—one on the Clementine spacecraft and one on the ISAS. The RRELAX experiments are autonomous microprocessor-controlled data handling and analog test systems. They were contained on three device under test (DUT) boards. These boards, termed the *x*, *y*, and *z* DUT boards, are shown in Fig. 1. The *z* DUT board, which contains most of the RRELAX experiments, is mounted on the top of the RRELAX box normal to the *z* axis.

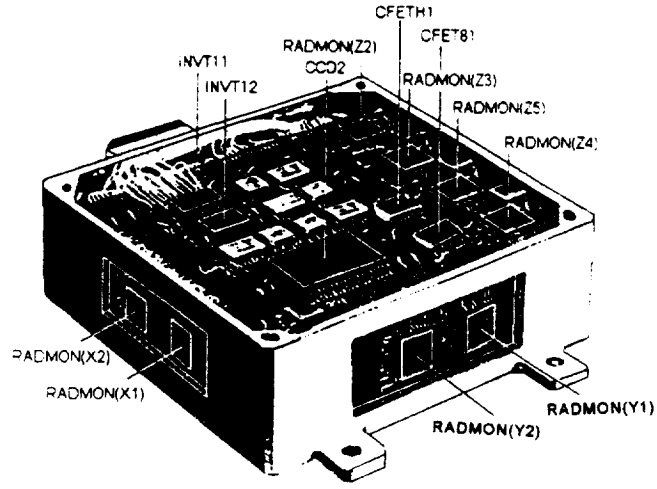

Fig. 1 RRELAX experiment layout in 4 × 4 × 1.5-in. box.

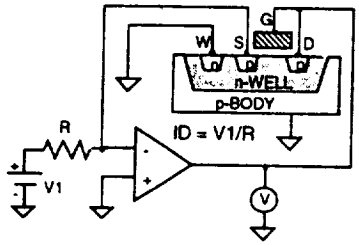

Fig. 2 Chip dosimeter (*p*FET on SRAM) and operating-mode circuit diagram.

The data presented in this paper were generated by the z DUT board RADMONs and CCD2. Each DUT board was covered with a 0.5-mil (Al equivalent) aluminized kapton dust cover, and RADMON(Z2), which had no Kovar lid, was covered with an additional 0.5-mil aluminized kapton dust cover. CCD2 had a 15-mil Kovar lid, RADMON(Z3) a 10-mil Kovar lid, RADMON(Z5) two 10-mil Kovar lids, and RADMON(Z4) three 10-mil Kovar lids. The ISAS RRELAX was also covered by a 6-mil (Al equivalent) thermal blanket. [0.5, 6, 10 mil = 13, 15, 25 μm]

The z-DUT-board RADMONs were fabricated through MOSIS at HP Corvallis in 1.2-μm technology, and the JPL CCD2s at Loral. A *p*FET dosimeter and SRAM proton counter was contained on each 1.2-μm RADMON IC chip (Z2, Z3, Z5, Z4) on the z DUT board, shown in Fig. 1.

Design of the *p*FET Dosimeter System

The *p*FET dosimeter system was designed to measure the total dose from all radiation types. The sensors were placed behind four different shielding thicknesses to produce dose-depth curves for the Clementine and ISAS experiments.

The dosimeter consisted of a *p*FET that was operated in a constant-current mode (Fig. 2). This allowed the temperature effects on channel mobility and threshold voltage to cancel each other. The objective of this design was to minimize temperature effects and emphasize dose dependence. The *p*FETs have a closed geometry gate, eliminating the source-to-drain bird's-beak leakage path. Dosimetry measured via the *p*FET threshold-voltage shifts was influenced by two second-order effects: 1) the temperature sensitivity of the transconductance factor and the threshold voltage V_T and 2) the source-to-drain bird's-beak leakage current. The goal in developing the advanced *p*FET dosimeter was to minimize or eliminate these effects.[1]

The *p*FET dosimeters were only powered during readout and accumulated dose while in an unpowered state. The four *p*FET dosimeters were read once per hour, and their data from the previous hour overwritten. Because *p*FETs are integrating dosimeters and have a larger radiation damage factor when unpowered, this mode of operation is satisfactory.

Design of the SRAM Proton Spectrometer System

The SRAM proton spectrometer system was designed to measure the proton energy spectrum and fluence for use in computing proton fluence and energy at the Clementine experiments. Four shielding thicknesses were used to pick off the external proton environment at four different energies, allowing the energy spectrum to be measured. Two energy bins were used to allow heavy-ion- and proton-induced nuclear reactions to be subtracted from the proton data. The threshold of the proton-sensitive bin was set just below the proton injection peak to optimize the energy measurement.

The SRAM detector was fabricated in 1.2-μm, n-well, double-metal CMOS. A schematic diagram of the SRAM cell, or pixel, is shown in Fig. 3. This cell differs from that of a standard six-transistor SRAM cell in three ways: 1) the source of the *p*FET, Mp2, is connected to an adjustable offset voltage V_o instead of V_{DD}, to provide control of the cell's upset capacitance; 2) the drain area Dn2 of *n*FET Mn2 has been enlarged by a factor of 4 over minimum to enhance upset rates, thus reducing the measurement time; and 3) the cell is unbalanced by widening Mn2 over minimum to enhance its SEU sensitivity vs V_o.

In operation, all the memory cells were written into a sensitive state, where Mn2 was turned off and Mp2 was turned on, connecting V_o to the bloated drain, Dn2. V_{DD} was then lowered to 3 V and V_o was lowered below V_{DD} = 3 V, allowing the SRAM to accumulate upsets at a given V_o value. Thereafter V_o and V_{DD} were returned to 5 V and the cells read to determine the number of upsets.[2]

Four SRAM chips were mounted to face along the z axis of the experiment, two facing the x axis and two facing the y axis, for a total of eight chips, as shown in Fig. 1. The SRAM portion of each chip was controlled using a single V_{DD} and V_o for all eight chips. All z-axis SRAMs, and one SRAM on the x axis and one on the y axis, were fabricated in 1.2-μm technology. One SRAM on the x axis and one SRAM on the y axis were fabricated in 0.8-μm technology.

The SRAMs were made sensitive to upset by applying 3-V V_{DD} and V_o voltages that have the following ΔV_p values above the spontaneous flip voltage:

$$\Delta V_p = 0.150 \text{ V}$$

$$\Delta V_p = 1.0 \text{ V}$$

The spontaneous flip voltage is the value of V_o where the SRAM cell becomes metastable and spontaneously flips. The offset voltage was set above the spontaneous flip voltage by an amount ΔV_p to sensitize the SRAM cell to protons, heavy ions, and nuclear reactions (ΔV_p = 0.150 V) or to heavy ions and nuclear reactions only (ΔV_p = 1.0 V). The integration period for these sensitive states was a constant of 100's. At the end of each integration period, each of the eight SRAMS was evaluated for bit changes, or upsets, and the total number for each chip stored in the data structure. The data structure and software flow are shown in Fig. 4.

When the evaluation of SRAM response was complete, software accumulated the upset totals. Each chip had its own accumulation, or running total, for each value of ΔV_p. The SRAM contents were then restored to their starting state and the second value of ΔV_p set for the next integration time. The experiment software alternated between the two ΔV_p values on a 1:1 ratio. This was done by the SWITCH VOLTAGE box in Fig. 4.

The 100-s integration records together with their time stamp were called the high-resolution SRAM data record. Software maintained each record for one hour before disposing of it. This generated 18

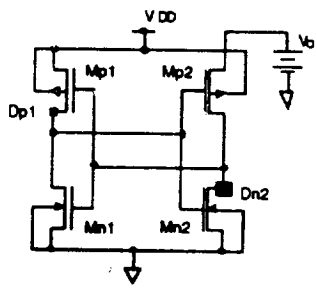

Fig. 3 Schematic diagram of the SRAM cell showing the placement of V_o and the bloated *n*-drain, Dn2.

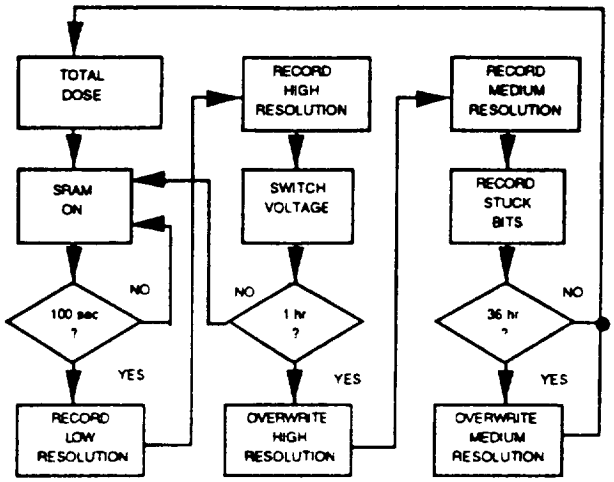

Fig. 4 Software flow diagram showing SRAM data-handling strategy.

consecutive sets (18 periods per hour) of 16-word records (one for each SRAM and ΔV_p value), which were stored in memory. These records formed the highest-resolution data set per SRAM and per ΔV_p value.

A high-resolution SRAM record that was about to be discarded was accumulated into a medium-resolution record. The medium-resolution record accumulated, or summed, the 18 high-resolution records for each SRAM and ΔV_p value. Each completed medium-resolution record holds integration results for a one-hour period for each SRAM and ΔV_p value. The medium resolution records time entry represented the time when the record was formed. The software retained medium resolution records for 36 h for a total of 576 medium-resolution records. This group of records formed one medium-resolution data set per SRAM and per ΔV_p value.

Each SRAM, for each ΔV_p value, measured the total fluence over the whole mission. This process used memory locations that were only added to and never overwritten. The data set was called the low-resolution data set.

The SRAMs were calibrated during each medium resolution data set by measuring the numbers of stuck zeros and ones. The temperatures of the analog board and the x, y, and z DUT boards and a temperature circuit calibration measurement were then stored, overwriting the previous calibration data record.

Ground Test Data

Selected pFET dosimeters from the flight fabrication run were calibrated with the JPL ^{60}Co source. The ^{60}Co irradiation was done at room temperature to a total dose of 100 krad(Si). The pFETs were tested at dose levels of 20, 40, 60, 80, and 100 krad and at −30, 20, and 50°C at each dose level. The pFETs were measured using an HP 4062 parametric test system in an oven that was also cooled with liquid nitrogen so that total-dose effects could be measured as a function of temperature. A temperature-independent threshold voltage damage factor V_d of 3.68 mV/krad was measured. The pFET was operated in the saturation region, which was ensured by connecting the gate to the drain as shown in Fig. 2, and at the temperature-independent point.[1]

A JPL CCD from the flight fabrication run was ground-tested to 4.8 krad(Si) in the JPL ^{60}Co source at room temperature and annealed at 25°C for 72 h. The CCD was characterized in the JPL CCD laboratory, and a dark-current damage factor I_d of 7.38 nA/cm^2 · krad at 25°C was measured.[3]

An SRAM from the flight fabrication run was calibrated using the Caltech Tandem Van de Graaff proton accelerator with protons at 0.75, 1.0, and 2.0 MeV. The SRAM ground-test response was analyzed using the TRIM (transport reactions in matter) computer code.[4] Calibration data are shown in Fig. 5. The model used in the calibration assumed a 5-μm overlayer (dead layer) and a 7-μm charge collection depth (depletion depth). The proton calibration data points are the mean values of the offset voltage, ΔV_p, where one-half the protons hitting a cell sensitive volume,

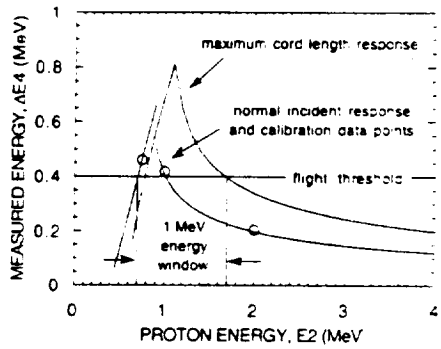

Fig. 5 Clementine 1.2-μm-technology proton calibration curves showing the flight energy threshold and the 1-MeV-wide energy window.

Dn2, cause the cell to flip. The proton data calibrated the 1.2-μm-technology SRAM at an upset capacitance, $C_u/K = 2.667$ MeV/V, where $K = 44.2$ fC/MeV for charged-particle-produced ionization per unit energy loss in silicon. The measured energy ΔE_4, shown in Fig. 5, is given by $\Delta E_4 = (C_u/K)\,\Delta V_p$. The 1-MeV energy window, shown in Fig. 5, is the measure of the SRAM response to protons in the space environment.[2]

Space Data

The ground-test-measured ^{60}Co damage factor, $V_d = 3.68$ mV/krad, was used to compute the space-measured pFET total dose. The downlinked numbers were bits, with one least-significant bit equal to 1.22 mV, from a 12-bit ADC measuring between 0 and 5 V:

$$D_s = \frac{V_s - V_g}{G V_d}\ \text{krad(Si)} \tag{1}$$

where V_s (mV) is the space-measured pFET voltage, V_g (mV) is the ground-measured voltage, and $G = 32.7$ is the circuit gain. The zero-dose voltages V_g (mV) and aluminium-equivalent shield thickness d (mils) for each flight RADMON on the ISAS RRELAX at $T = 25$°C and on the Clementine spacecraft RRELAX at $T = -2.41$°C are listed in Table 1.

The p-FET total-dose flight results for the Clementine spacecraft on April 27, 1995, and the ISAS on April 20, 1994 (ISAS 1994 day 110), are shown in Fig. 6. The Clementine spacecraft total dose after 457 days in space is less than the ISAS over its mission life. On the Clementine spacecraft, the RADMON dosimeter-circuit dynamic range was exceeded for pFET Z2 because $G = 32.7$ for that circuit and a total dose of 142.95 krad (Si) was extracted with the CMOS experiment circuit for that pFET. The ISAS pFET-dosimeter mission dose profile is shown in Fig. 7. The ISAS is in a 2.13-day lunar transfer orbit that penetrates the Earth's radiation belts, causing the rapid increase in total dose.

The ISAS RRELAX CCD experiment was shielded by 52 mils (1.3 mm) (Al equivalent). Power-law dose-depth curves were fit to the pFET data as a function of shield thickness. The pFET-measured dose at CCD2 was then extrapolated from these curves as shown in Fig. 8.

The CCD2 sensor chips were 512-pixel line arrays manufactured at Loral in n-channel metal–oxide system (nMOS) buried-channel technology. The RRELAX CCD experiment measured the dark-current-generated voltage in the last 8 pixels, pixel 505 through 512, and the extended pixels with no photosensors, 513 through 519. The data presented here had a photosensor dark-current integration time of 1 s. ISAS CCD2 data showing the prelaunch pixel voltage mean V_g and the extended pixel voltage mean (for ground and space data) V_0 are presented in Fig. 9. The ISAS CCD2 had a prelaunch dark current measured on the flight CCD[3] of $I_g = 1.4$ nA/cm^2 at 25°C and a voltage conversion of $V_c = I_g/(V_g - V_0) = 11.7$ nA/cm^2 · V.

The 25°C dark-current damage factor $I_d = 7.38$ nA/cm^2 · krad was used to compute the space-measured total dose:

$$D_s = \frac{V_c(V_s - V_g)}{I_d}\ \text{krad(Si)} \tag{2}$$

Table 1 Zero-dose *p*FET ground voltages V_g and aluminium equivalent shield thickness *d* for each flight RADMON on the ISAS RRELAX at $T = 25°C$ and on the Clementine spacecraft RRELAX at $T = -2.41°C$

RADMON	Spacecraft		ISAS	
*p*FET	V_g, mV	*d*, mils	V_g, mV	*d*, mils
Z2	129.9	1	621.8	7
Z3	74.8	31	335.4	37
Z5	274.8	61	592.2	67
Z4	381.0	91	494.0	97

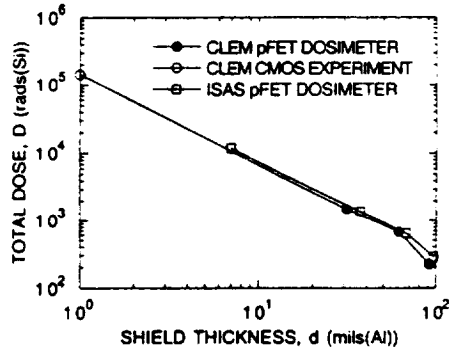

Fig. 6 Total radiation dose on RADMON *p*FET Z2 as a function of aluminium equivalent shield depth for the Clementine spacecraft on April 27, 1995, and the ISAS on April 20, 1994.

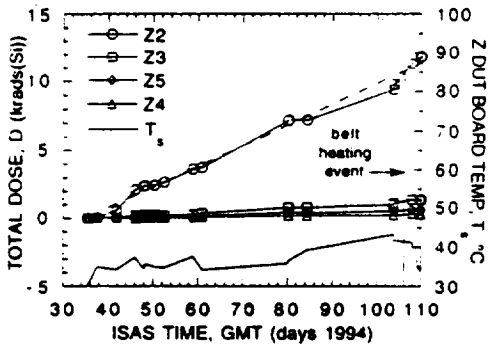

Fig. 7 Mission dose profile for the ISAS RADMON *p*FETs in a 2.13-day lunar transfer orbit and the associated temperature variation.

where V_t (V) is the space-measured CCD voltage mean for pixels with photosensors, pixels 505 through 512. The total dose at 25°C, $D(T)$, in kilorads (Si), is given by

$$D(T) = D_s\left(\frac{T}{T_s}\right)^{\frac{3}{2}}\exp\left(\frac{E_g}{2kT_s} - \frac{E_g}{2kT}\right) \tag{3}$$

where $E_g = 1.21$ eV, T_s is the *z*-DUT-board temperature, D_s is the space-measured dose from Eq. (2), and $T = 25°C$. Temperature-corrected CCD dose data are shown in Fig. 10. The temperature correction given by Eq. (3) is due to temperature changes in the intrinsic carrier density associated with bulk current.[5]

The CCD2 dark-current measured dose is compared with the *p*FET measured dose at the CCD in Fig. 11. Two prominent geophysical events were observed during the mission. The first, a solar proton event on day 52 of 1994 (Feb. 21, 1994), had a planetary magnetic index Kp of 7+ and was observed at a number of spacecraft (the proton observations will be discussed shortly). The increased dose rate after the second major event (the sudden commencement of a storm followed by a brief but intense geomagnetic storm on day 107) is due to trapped-electron-belt heating on days 106 and 107 of 1994 (April 16–17, 1994). The increase implies more and higher-energy trapped electrons along the ISAS orbit. Consistent with this interpretation, $Kp = 8+$ for the event, indicating a large increase in the trapped ring current and subsequent electron-belt heating. There was, however, no large solar proton event associated with the event.

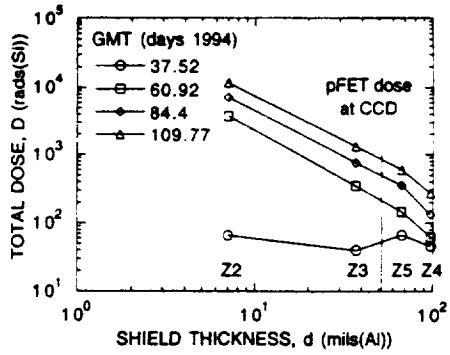

Fig. 8 ISAS dose–depth curves showing *p*FET dose at CCD2.

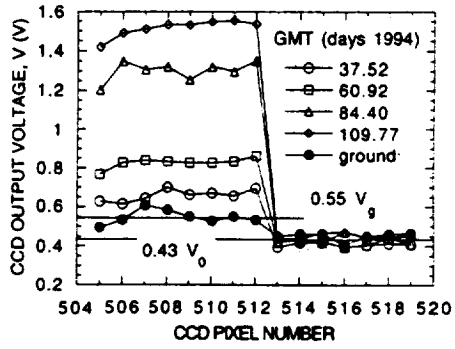

Fig. 9 A sample of the RRELAX ISAS CCD2 data showing the prelaunch, zero-dose pixel voltage mean V_g and the extended pixel voltage mean V_0 for ground and space data.

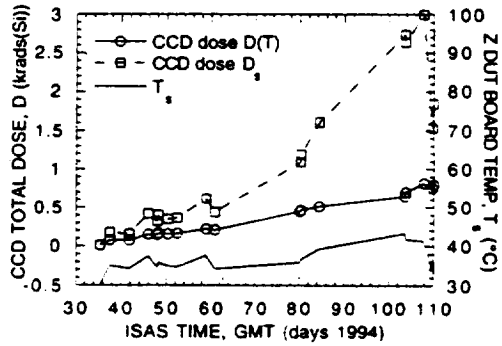

Fig. 10 CCD temperature corrected [$D(T)$] and uncorrected [D_s] dose data as a function of temperature.

The ISAS *p*FET dosimeter, operated at its temperature-independent drain current, measured a total dose of 11.83 (krad) on day 109.99. The ISAS *p*FET complementary metal–oxide–semiconductor (CMOS) experiment, using the same *p*FET operated at the five different drain currents shown in Fig. 12, measured a total dose, $D(T)$ given by Eq. (6), of 11.47 krad on day 109.99. The space-measured threshold voltage V_{Ts} is computed with Eq. (5) from second-order polynomial coefficients generated by fitting flight data[1] on the drain current I_D vs the gate voltage, V_G with Eq. (4) as shown in Fig. 12:

$$\sqrt{I_D} = a_0 + a_1 V_G - a_2 V_G^2 \tag{4}$$

$$V_{Ts} = \frac{a_1}{2a_2}\left(-1 + \sqrt{1 - \frac{4a_0a_2}{a_1a_1}}\right) \tag{5}$$

$$D(T) = \frac{V_{Ts} + V_{Tt}(T_s - T)}{V_{Td}} \tag{6}$$

where $V_{Tt} = 1.24$ mV/°C, $T = 25°C$, and $V_T = 883.7$ mV measured on the ISAS *p*FET prior to launch, and $V_{Td} = 1.674$ mV/krad measured on W12P4C05 for the HP 1.2-μm technology.[1] The CMOS experiment *p*FET dose verifies the dosimeter design and ground

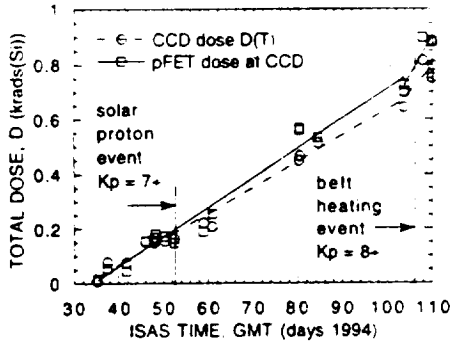

Fig. 11 CCD dose $D(T)$ and pFET dose at the CCD, showing increased dose rate after day 106.

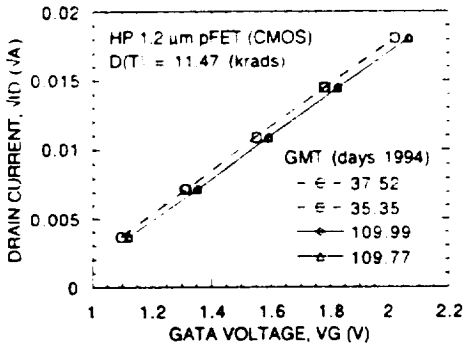

Fig. 12 ISAS CMOS HP 1.2-μm pFET gate voltage shift on day 109.99, April 20, 1994.

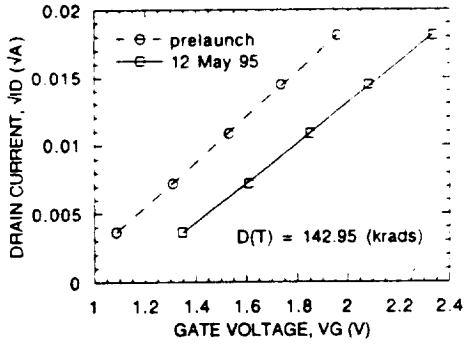

Fig. 13 Clementine CMOS HP 1.2-μm pFET Z2 gate voltage shift on April 27, 1995.

calibration methodology. The same equations are used to extract the pFET Z2 total dose on the Clementine spacecraft on April 27, 1995, shown in Fig. 13, where $T_t = 3.32$°C and $T = -2.41$°C, $V_T = 863.9$ mV measured on the Clementine pFET prior to launch, and the other variables are the same. CMOS radiation damage factors for n- and p-channel transistors in HP 1.2- and 0.8-μm technologies are being utilized in radiation test-structure designs for the active-pixel image sensors (APS).

SRAM detector proton data from the Feb. 21, 1994, solar proton event have been compared with GOES-6 proton data. First, the Novice code was used to compute the proton environment as a function of energy inside the SRAM shields. Table 2 lists the external environment energy windows, E_{min} to E_{max}, in the 1-MeV-wide energy window measured in Fig. 5. The mean values f_e of the internal environment fraction inside the shields are also listed in Table 2. Next the environment fractions were computed with the Novice code from a 2π-sr omnidirectional fluence of 1.96×10^9 p/cm^2 · MeV at all energies outside the shields. The proton fluence was then reduced by the factor f_e inside the shields.

The SRAM spectrometers are sensitized to protons for 100 s, every other 100-s period, for one hour, giving an on-time fraction f_{on} of 0.5. The energy window width ΔE (Fig. 5) is 1 MeV. The instrument was designed with a 2π-sr field of view Ω. The SRAM pixel sensitive area has an as-drawn cross section σ of 42.12 μm^2. The spectrometer hourly frequently $F(E)$, in p/cm^2 · MeV · h is given by

$$F(E) = \frac{18}{\sigma \Omega \Delta E f_e f_{on}} \ln\left(\frac{N_T}{N_T - N/18}\right) \qquad (7)$$

Each pixel can only count one proton in each 100-s proton-sensitive period, and there are 18 sensitive periods each hour. There are $N_T = 4096$ pixels on each SRAM chip, and N is the measured number of counts per hour in each chip. The Clementine spectrometer data, $F(E)$ from Eq. (7), for the Clementine SRAM Z2 and Z3 proton energy windows and the GOES-6 hourly fluencies for the proton energy windows P1 and P3 are plotted in Fig. 14 for comparison.

The GOES-6 external environment proton energy windows, E_{min} and E_{max}, are P1: 0.6–4.2 MeV; P2: 4.2–8.7 MeV; P3: 8.7–14 MeV; and P4: 15–44 MeV. The Clementine and GOES-6 energy spectra for the total measured fluence on Feb. 21, 1994, are shown in Fig. 15. The data-point energies are taken at the center of the energy windows, $(E_{min} + E_{max})/2$, listed in Table 2 for the Clementine instrument and at the beginning of this paragraph for the GOES-6 instrument.

Table 2 External environment energy windows and internal environment fractions f_e for Clementine spacecraft, as a function of Kovar shielding

Kovar shields					
RADMON pFET	Thickness, mils	mm	E_{min}, MeV	E_{max}, MeV	Mean f_e (0.7–1.7 MeV)
Z2	0	0	2.16	3.16	0.261 ± 0.031
Z3	10	0.25	11.81	12.81	0.072 ± 0.009
Z5	20	0.5	16.96	17.96	0.047 ± 0.007
Z4	30	0.75	21.04	22.04	0.037 ± 0.006

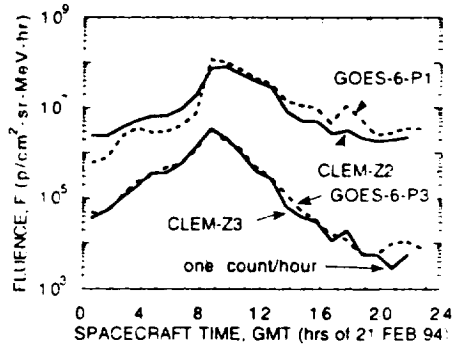

Fig. 14 Comparison of Clementine data with GOES-6 data during Feb. 21, 1994, solar proton event. The proton spectrometer sensitivity of one count per hour is shown.

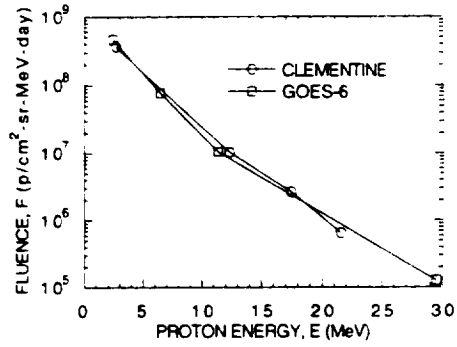

Fig. 15 Clementine spacecraft and GOES-6 external environment proton energy spectra on Feb. 21, 1994.

Dosimetry Conclusions

The primary objective of the RRELAX experiment was to monitor the radiation environment for the Clementine mission. Two conclusions have been presented about this objective. First, the ISAS CCD

and CMOS experiment measurements were shown independently to agree well with the *p*FET dosimeter measured total dose. This demonstrates that the results of the ground radiation tests can be used to accurately predict spacecraft sensor and electronic component radiation degradation. The test-structure approach employed also allowed direct measurement of radiation effects in space and verified our predictive understanding of the space environment's radiation effects on spacecraft sensors and electronic components. Secondly, the SRAM proton spectrometer successfully measured the proton fluence and energy spectrum. The data agreed quite well with GOES-6 data for the same event. We therefore feel confident in stating that the dosimetry system, RADMON, has accurately tracked the proton fluence and energy and total dose for the Clementine Engineering experiments.

Acknowledgments

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INTEGRATED ENVIRONMENTAL MONITORING SYSTEM FOR SPACECRAFT

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Abstract

This paper describes an integrated space environmental monitoring system for geosynchronous satellites. The system provides measurements of surface charging, internal charging, and total dose radiation from the space environment. It is installed on seven of Martin Marietta's commercial communications spacecraft, which are scheduled for launch in the near future. There are two components: an internal charge monitor, and a surface charge detector. Total weight is less than one pound; power consumption is about 0.5 W. Charging flux information from these detectors will permit evaluation of the effects of internal charging on electronic PC boards and will lead to the development of reliable, low-weight methods to detect on-orbit spacecraft charging events and to control charging and discharging.

1. INTRODUCTION

The uncertainties in predicting the effects of energetic particles on satellite systems remain a concern to all spacecraft designers and users. To assist the development of effective mitigation techniques, a lightweight, low-power monitoring system has been designed and built by Martin Marietta Astro Space (now a division of Lockheed Martin) and Jet Propulsion Laboratory. The system consists of two types of instruments -- (1) a radiation dosimeter calibrated to measure internal charging and (2) a surface charging detector. Both instruments will produce continuous telemetry data throughout the mission.

The system will provide a means of monitoring external and internal charging events aboard satellites. It will be very useful in determining the effectiveness of surface ESD control measures, such as conductive coatings, and of protective measures, such as grounded metal shielding, developed for mitigating internal charging effects on PC boards and cables. These evaluations will point the way to future design solutions and to the development of realistic design requirements for control of surface charging and internal charging.

The surface charging monitor was designed to measure charging by magnetospheric plasma electrons with energies from 5 keV to 20 keV and with worst-case current density from 0.1 to 1 nA/cm^2. This range was chosen because it has a probability of occurrence of 99% [1]. The charge monitor will indicate when such an environment is present at the spacecraft's orbital location. Two of these units are being mounted in different places on seven of Martin Marietta's commercial communications satellites scheduled for launch in the near future.

The internal charging detector was designed to monitor flux of, and total dose imparted by, electrons with energies from 200 keV to 6 MeV. This detector will indicate when such an environment is present at the spacecraft's orbital location and will measure the flux of these electrons at various locations inside the spacecraft structure. The key component is a dosimeter designed, fabricated, and tested by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory of the California Institute of Technology [2, 3]. Two of these units are being mounted on seven Martin Marietta satellites.

2. DESIGN DESCRIPTION

2.1 Surface Charging Detector

The surface charge detector has two components -- the charging plate and the associated control electronics. The charging plate is mounted to the spacecraft structure outside the spacecraft and is exposed directly to the space environment. The control electronics unit operates from the +/- 15-volt power lines. It is located inside the spacecraft with the charging plate connected to the input of the instrumentation operational amplifier through a high-input-impedance buffering RC circuit as shown in Fig. 1. The operational amplifier was configured to provide a 0- to 5-volt output compatible with the standard telemetry format.

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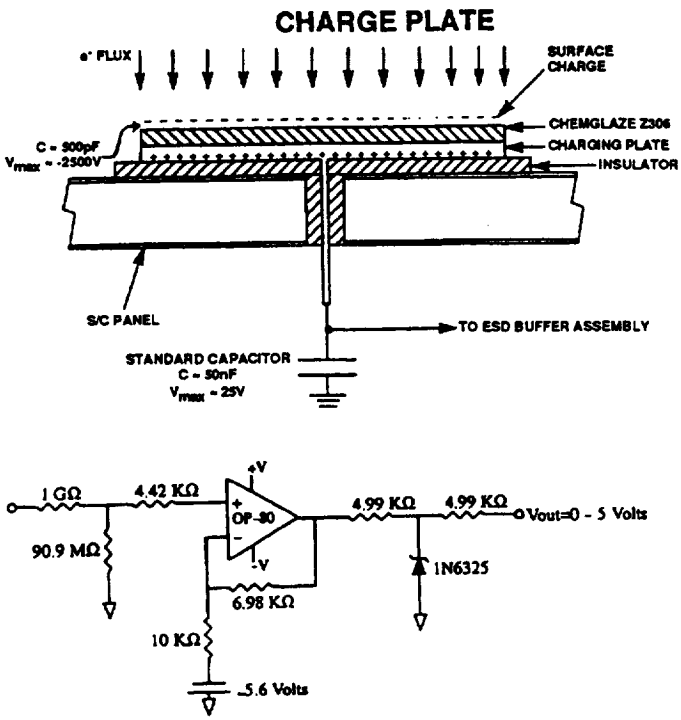

Fig. 1 Surface charging sensor description

Three critical choices during the design of the detector were: charging plate surface material, charging plate substrate, and mounting adhesive. The selection parameters for the surface material and mounting adhesive included electrical conductivity, high voltage leakage current, thermal expansion coefficient, thermo-optical properties, and space environmental stability in the operational temperature range. Surface materials that were considered for the charging plate included S13GLO white paint, Z306 Chemglaze black paint, black anodize, and alumina. Adhesives included RTV 566, CV2946, CV2943, and alumina-loaded Solithane 113. All candidate surface materials and adhesives were tested in a monoenergetic electron beam for their charging potentials, charging and discharging time constants, and compatibility with the readout circuits. A detailed description of the test procedure and test facilities is given in the referenced documents [4-6].

The result of the selection process is a charge collector in the form of a 2" by 2" (5x5 cm) aluminum plate painted with Chemglaze Z306 dielectric paint bonded to the spacecraft with nonconductive CV2946 adhesive. The plate is charged by impinging electrons. The charging potential on the painted surface can vary from slightly positive to several hundred volts negative, with a corresponding potential on the underlying aluminum plate--that is, at the input to the buffer assembly in Fig. 1--varying from +5 to -25 volts.

The sensor was calibrated with 5-keV, 10-keV, and 20-keV electron beams (beam current densities from 0.25 nA/cm^2 to 1 nA/cm^2) over a -40°C to 60°C temperature range. Typical calibration curves are shown in Fig. 2. Because in space spacecraft ground floats with respect to ambient, these calibration curves are only directly applicable to the case of shadowed detectors while the rest of the spacecraft is in the sun. For this condition spacecraft ground floats only about a few volts positive.

For the conditon of the spacecraft in eclipse or for the case of the sunlit sensor, NASCAP analysis is required to develop predictions for sensor response. Several qualification tests were performed on all sensors prior to their integration into the spacecraft. These tests included radiation testing (400 megarads total dose) and thermal cycling (5000 cycles from +60°C to -60°C) on the charge plate, plus radiation testing to a total dose of 30 kilorads on the readout circuit. ESD and DC overvoltage tests were also conducted on the readout circuit.

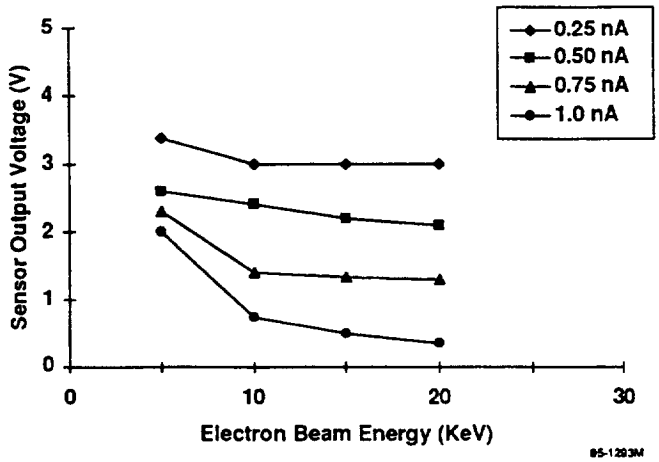

Fig. 2 Surface charging sensor calibration (T=25°C)

2.2 Dosimeter/Internal Charge Monitor

The dosimeter within the charge monitor comprises four identical radiation-sensitive p-FETs, each shielded with a different-thickness Kovar lid. The thinly shielded transistors correspond to components near the surface of a spacecraft; the thickly shielded transistors correspond to components deep within the spacecraft. Shield thicknesses were selected by trading FET lifetime vs. sensitivity to dose. The directly sensed quantity is ON-channel voltage drop at the temperature-independent current. This is related by calibration to total dose. Total dose can then be related by calibration to incident electron fluence. Differentiating the fluence with respect to time gives charging flux. The outermost transistors have a higher charge rate, which leads to better resolution, but, since the ON-channel voltage drop saturates at a certain total dose, this also leads to a shorter lifetime. That is, the outermost transistors will probably saturate before the end of the satellite's mission.

The microchip layout developed on this effort is shown in Fig. 3. It consists of seven components listed in Table 1 including p-FETs P0, P1, P2, and P7, each with different shields (Note: 1 mil = 0.00254 cm). These shields were fabricated in the Kovar lid by chemical etching. The microchip, shown in Fig. 3, was fabricated in a 1.2-mm CMOS rad-soft process. The chip was packaged in a 16-pin flat pack. The equivalent circuit for the chip, shown in Fig. 4, has a multiplexer and decoder used to place each component selectively in the feedback loop of the operational amplifier circuit shown in Fig. 5. The circuitry was designed to force a current at the temperature independent point through the p-FET during measurement. When not operating, the p-FETs are unbiased.

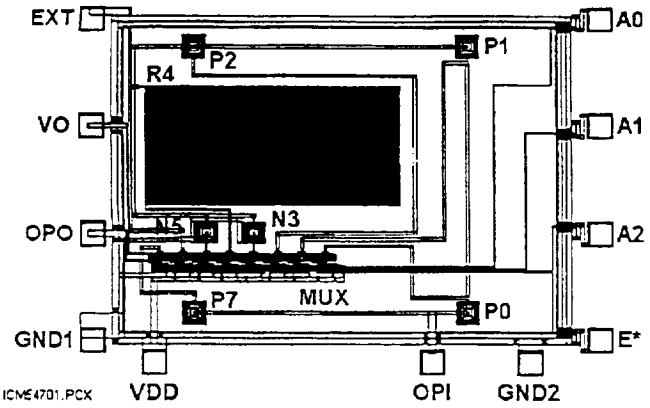

Fig. 3 Microchip with four p-FETs, P0, P1, P2, and P7. Each P-FET is located behind a different shield whose thickness is listed in Table 1.

Table 1
Microchip Devices

Device	Type	Shield mil (μm)
P0	Gate Oxide p-FET	6 (150)
P1	Gate Oxide p-FET	0
P2	Gate Oxide p-FET	2 (50)
P7	Gate Oxide p-FET	10 (250)
N3	Field Oxide n-FET	not used
N5	Gate Oxide n-FET	not used
R4	Metal-1 Resistor	10 (250)
E6	External Device	NA

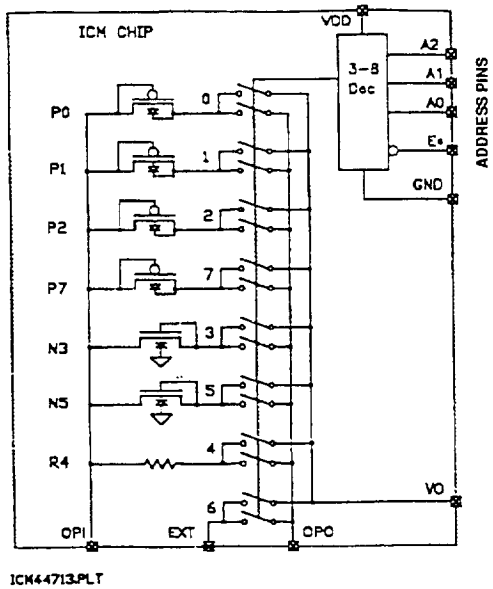

Fig. 4 Microchip schematic

Dose levels and shielding for each of the p-FETs are shown in Table 2. In addition to the Kovar lid, the outside dosimeter is shielded by the thermal blanket and the inside dosimeter by a spacecraft panel. The equivalent shield thicknesses are shown in Table 2.

Table 2
The 250 krad time for each p-FET
in the two dosimeters

Device	P1	P2	P0	P7
Outside Dosimeter				
Lid Thickness (in mil KOVAR)	0	2	6	10
Shield Thickness (in mil KOVAR)	2	2	2	2
Total Thickness (in mil KOVAR)	2	4	8	12
250 Krad Time (months)	0.7	1.6	5.5	13.3
Inside Dosimeter				
Lid Thickness (in mil KOVAR)	0	2	6	10
Shield Thickness (in mil KOVAR)	10	10	10	10
Total Thickness (in mil KOVAR)	10	12	16	20
250 Krad Time (months)	8.9	13.3	26.4	45.9

[SI units on p. 83]

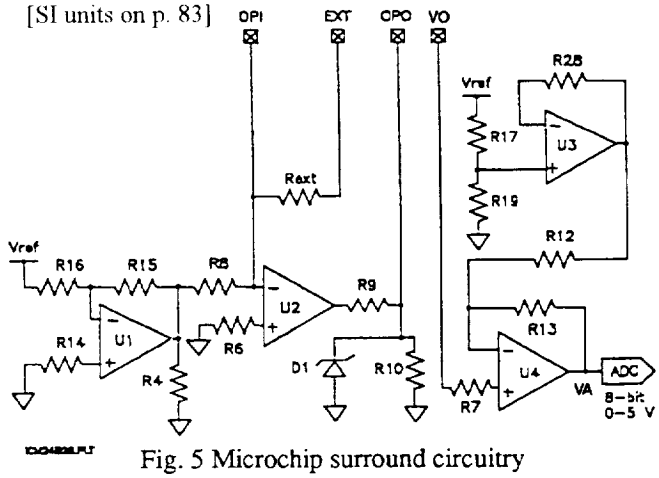

Fig. 5 Microchip surround circuitry

The calibration of the p-FET must account for both dose and temperature effects. The analog voltage, VA, shown in Fig. 5 is:

$$VA(T, D) = VAoo + VA_T(T - To) + VO_D \cdot G \cdot D \quad (1)$$

where VAoo is the initial output voltage determined from ground tests, VA_T is the temperature coefficient determined from ground test data, VO_D is the dose coefficient determined from Co-60 ground tests, G = Gain = R13/R7, and To = 300K. D is the dose in kilorads; T is the temperature in K. The dose is calculated from:

$$D = [VA - VAoo - VA_T(T - To)]/(VO_D \cdot G) \quad (2)$$

The p-FET output voltage, VO (Figs 4 & 5), follows from the square law behavior of the FET operating in saturation [2]:

$$VO = VT - (2 \cdot ID/\beta)^{1/2} \quad (3)$$

where VT is the threshold voltage, β is the transconductance, and ID is the drain current chosen at the temperature independent point. This expression is used to determine the VO-dose calibration curve given VT, β, and ID as discussed below.

The temperature-dose expression for the VT is:

$$VT = VToo + VT_T \cdot (T - To) + \Delta VT[1 - \exp(-D/Do)] \quad (4)$$

where VToo is the threshold voltage at To and D = 0, VT_T is the threshold voltage temperature coefficient, Do is the VT dose coefficient, and ΔVT is the maximum change in VT when the radiation reaches infinity. When D= Do and at constant T, the VT increases by ΔVT[1-1/e]. The expression for VT indicates that VT is rate limited, which depends on the filling of a finite supply of gate-oxide hole traps [7]. The VT equation was solved using the least-squares method to determine VToo, VT_T, and ΔVT. The parameter Do was found using an optimization technique that maximizes the least-squares correlation coefficient.

The dose-temperature expression for β is :

$$\beta = \beta oo(T/To)^{-n}/[1+ (D/Dm)(T/To)^{-n}] \quad (5)$$

where βoo is β evaluated at To and D=0, n is the β temperature coefficient and Dm is the β or mobility dose coefficient. Formula (5) is equivalent to 2.9.1 in [8] with an added term expressing radiation dependence. When D = Dm at T=To, then β is reduced by 50%. This equation was formulated by combining the β temperature and dose dependence as the sum of reciprocals.

The p-FET drain current at the temperature independent operating point, IDm, is found by differentiating the VO expression with respect to temperature. Setting the resulting expression equal to zero at the measurement temperature, Tm (which is the expected on-orbit operating temperature), and D=0 leads to (6):

$$IDm = 2(\beta mo)^3(-VT_T/\beta_{Tmo})^2 \quad (6)$$

where $\beta_{Tmo} = (-n/Tm)\beta mo$ and $\beta mo = (Tm/To)^{-n}$.

The VT, β, and VO results are presented graphically in Figs. 6 through 8. The curves were obtained by fitting the data shown in Fig. 6 to Eq. 4 and the data shown in Fig. 7 to Eq. 5. Thus, the p-FET results can be characterized by seven parameters, namely VToo, VT_T, ΔVT, Do, βoo, n and Dm. These parameters are listed in Table 3 for transistor P0. The device-to-device uniformity was excellent.

VO values were obtained from Eq. 3 using Eq. 4 for VT, Eq. 5 for β, and Eq. 6 for IDm. The VOmo values for each of the four p-FETs, are within 0.1% of each other. The VO values are plotted in Fig. 8 for two different values of IDmo. The curves for the P0 design value of IDmo = 88 μA show that VO is fully temperature compensated at D=0. The curves for the operating value IDmo=100 μA show that temperature compensation occurs near 100 krads and that VOmo=1.507 V. These parameters were used as the target design parameters, thus the 100-μA curve is designated as the calibration curve. The samples from the flight lot of dosimeters were radiation tested and calibrated using a Co-60 gamma source at -25C, +10C and 45C. A burn-in test, centrifuging and temperature cycling testing were also performed on the flight devices.

A similarly fabricated p-FET was flown on STRV-1b, launched June 17, 1994 into a 10.59-hour geosynchronous transfer orbit with an apogee of 36,000 km, a perigee of 300 km and an inclination of 7° south. Four p-FETs were located across the bottom of the JPL experiment box. Two p-FETs termed exposed (E) had an 80-mil (200 μm) Al shield and two p-FETs termed shielded (S) had a 200-mil (560 μm) Al shield. The p-FET temperature coefficient VA_T was determined from the slope of the flight data as shown in Fig. 9 where VA_T=3.5 mV/°C. The dose for the STRV-1b is shown in Fig. 10; the data shown in Fig. 10 was fitted with a linear line using the least squares method. The dose rate for exposed p-FET P4E is 96.0 rads/day and P8E is 75.6 rads/day and the dose rate for the shielded p-FET P8S is 8.0 rads/day and for P4S is 6.2 rads/day. p-FETs P4E and P8S were located near the outside of the box and P4S and P8E were located near the center of the box. Notice that the dose rate for the center p-FETs is 78 percent of the outside p-FETs. This shows the dose is different across the JPL experiment box.

The p-FET dose rates determined from the data shown in Fig. 10 are compared to the NASA models [9] as shown in Fig. 11. The data falls between the electron and proton data and has a slope that is closer to the proton data. There is some concern that the experimental data does not follow either the proton or electron predicted behavior. New experiments are being prepared to acquire space data to clarify this point. The Martin marietta dosimeter is expected to have very little temperature dependence, but if any is observed it can be used to adjust the value of VA_T determined from ground calibration. Additional information on the STR-1b experiment is provided in [10,11].

Table 3
p-FET Design Parameters

Parameter	Description	Units	Value
To	Reference value of temperature	°C	27
Tm	On-orbit value of temperature	°C	10
VToo	Threshold voltage @ zero dose & To	V	-0.8598
VT_T	∂VT/∂T at constant dose D	mV/°C	1.7595
ΔVT	Saturation value of change in VT by dose D	V	-0.4998
Do	Value of D at which [VT] has increased by ΔVT[1-1/e]	kilorads	118.91
βoo	Channel transconductance	$\mu A/V^2$	474.73
Dm	Dose coefficient of β in eq. (5)	kilorads	588.5
n	Temperature coefficient of β in eq. (5)	-	1.7196
IDmo	Design value of temperature - independent drain current	uA	prelim.: 88.36; final: 100
VOmo	Output voltage at ID_{mo}	V	prelim.: -1.47 final: -1.507

3. SPACECRAFT IMPLEMENTATION

As stated above, two surface charge monitors and two dosimeters are being installed on each of seven Martin Marietta commercial communications satellites. Total weight of the system is less than one pound (500 g) and the system requires approximately 0.5 watt of power.

Surface charge monitors were installed on the north and anti-earth panels. The sensor located on the north panel will be continuously shadowed for a period of six months; then it will be continuously exposed to sunlight during the other six months; it

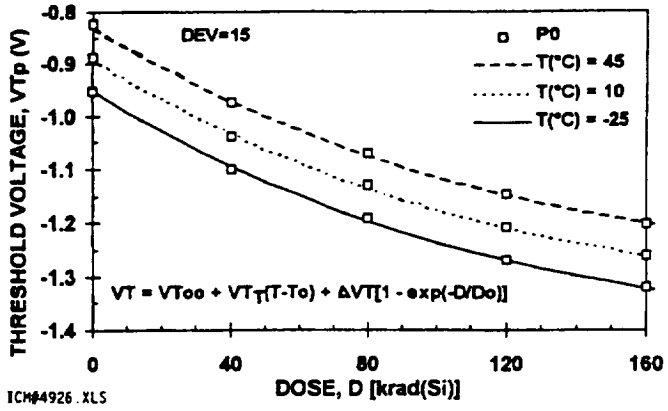

Fig. 6 p-FET threshold voltage dose-temperature fit to Eq. 4

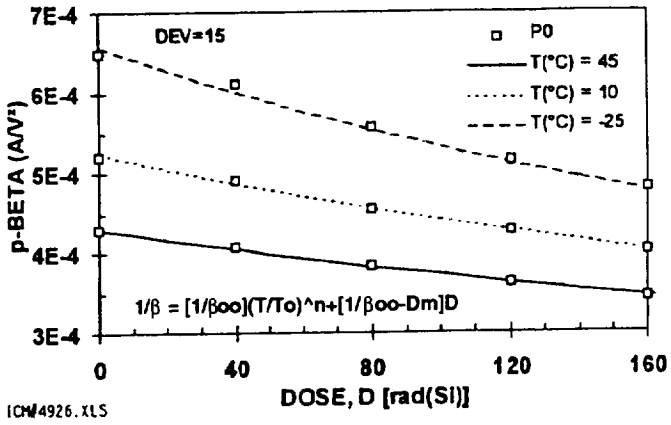

Fig. 7 p-FET beta dose temperature fit to Eq. 5

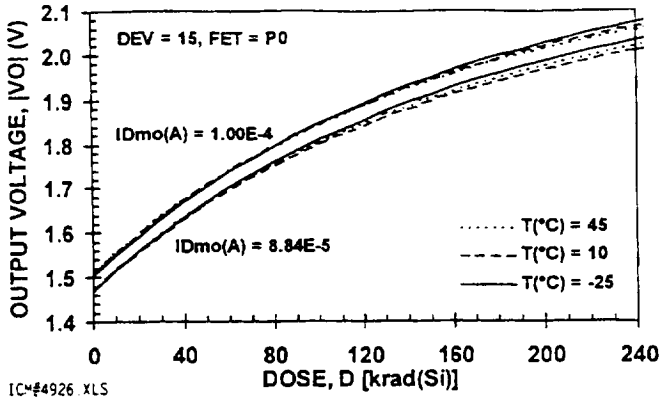

Fig. 8 p-FET output voltage dose dependence

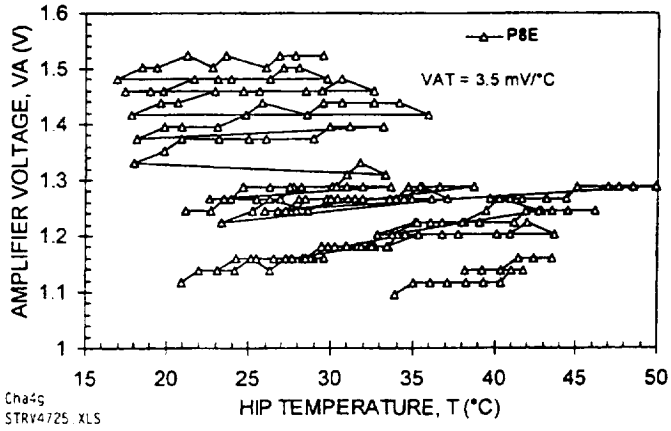

Fig. 9 STRV-1b p-FET VA-temperature dependence, VAT = 3.5 mV/°C

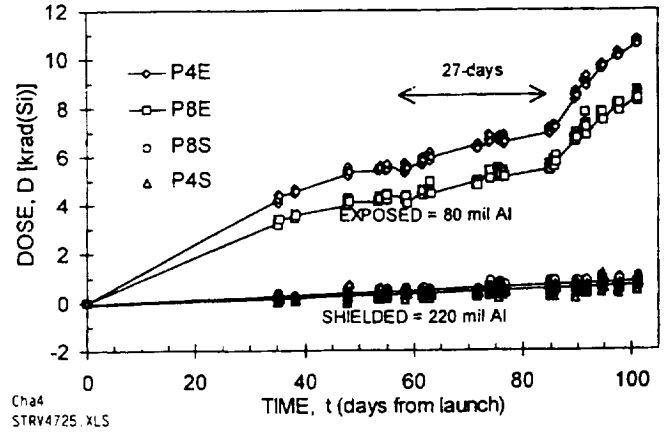

Fig. 10 STRB-1b dose profile for devices behind 80-mm and 220-mm Al shields

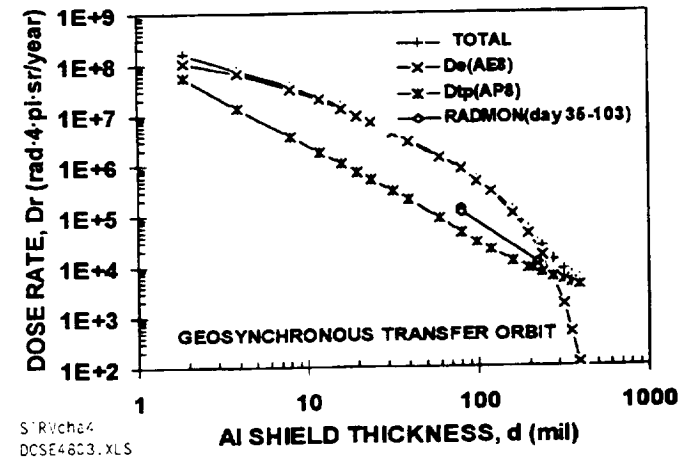

Fig. 11 Comparison of STRV RADMON results with NASA radiation models

will provide data on seasonal variations of spacecraft charging potential. The sensor mounted on the anti-earth panel will be moving in and out of the sunlight on the daily basis; it will provide data on daily variations in spacecraft charging potential.

In addition, two dosimeters will be used to monitor internal charging fluxes and total dose accumulation. One dosimeter was mounted on the north panel internal to the spacecraft structure with the sensor facing the panel. In addition to its Kovar lid, this sensor is shielded from external radiation by the spacecraft panel. This location is typical for most spacecraft components. The second dosimeter is located outside the spacecraft structure on the anti-earth panel. In addition to the Kovar lid, this sensor is shielded from external radiation by a ten-layer Kapton thermal blanket. Thus a total of eight p-FETs with different shield thicknesses will provide electron flux count in eight energy channels.

Support logic is combined with the sensors in order to meet the spacecraft's interface requirements. The sensors were tested for functional performance following their installation on the spacecraft and during spacecraft-level thermal testing.

4. CONCLUSIONS

Development of mitigation techniques for spacecraft charging control requires thorough knowledge of the environmental conditions and of their impact on spacecraft components. An integrated space environmental monitoring system has been developed, built, and installed on a geosynchronous communications satellite. Its low weight and power requirements allow easy incorporation into the spacecraft design. Satellite performance can be correlated with in-situ charging and dose rate. Until now, the only environmental data available was from research satellites, in different time zones and along different flux tubes. We envision that in the future, such systems may become a standard part of the bus telemetry as common as temperature sensors for all geosynchronous spacecraft.

The surface charging monitors must be mounted in carefully selected locations so that the degree of differential charging can be measured. In particular the differences in charging between the shaded and sunlit areas must be detected as the 3-axis-stabilized satellite gradually passes through the stages in its orbit. Fig. 12 shows one possible arrangement to accomplish this. Surface charge monitor #1, on the north panel, is always shaded between the fall and spring equinoxes and always illuminated the other half of the year. Charge monitor #2 is alternately illuminated and shaded during each orbit. During this time, at any time except during eclipse, entry into a charged plasma cloud would give a transient differential reading between a shaded sensor and an illuminated sensor. A differential reading will also occur on emergence from eclipse when the satellite carries a net charge and one of the sensors is facing the sun. Thus the charging monitors will collect a significant datum that is not readily available from scientific satellites that carry particle detectors. The particle detector output readily reveals only the net charge on the satellite and not the differential surface charging. Particle detectors, to provide net charge, would be desirable but not feasible for a commercial communications satellite where weight and power are at a premium.

When an in-situ indication of differential surface charging is available, anomalies can be correlated with this condition and with the deep-charging flux measured by the pair of dosimeters. The instruments on CRRES provided similar correlation opportunities [12,13]. System anomalies are discussed in [12] and discharges, as registered by the Internal Discharge Monitor (IDM), are discussed in [13]. The system described in this paper is a monitoring tool, rather than a research tool, and is therefore much less sophisticated than the collection of instruments available on CRRES. This simplicity and ease of accommodation, however, is necessary to allow widespread use on commercial spacecraft.

5. ACKNOWLEDGMENTS

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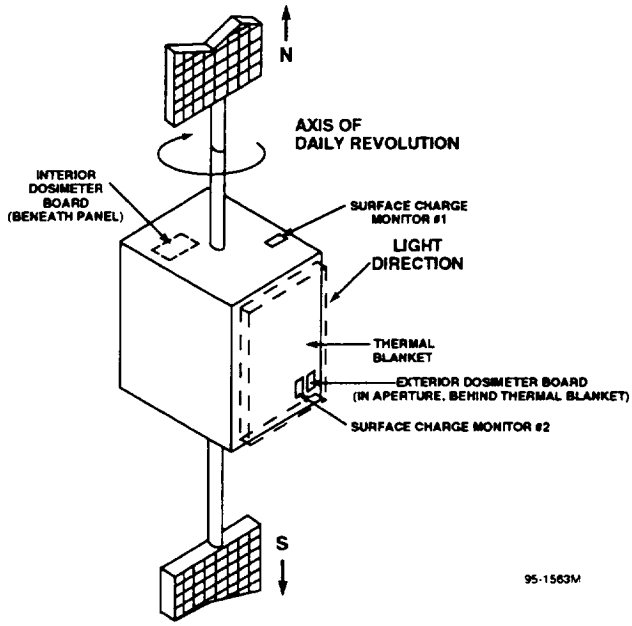

Fig. 12 Internal and surface charge monitoring system. Internal charge monitors are identified as "dosimeters"

Table 2
The 250 krad time for each p-FET
in the two dosimeters (SI units)

Device	P1	P2	P0	P7
Outside Dosimeter				
Lid Thickness (in μm KOVAR)	0	5	150	250
Shield Thickness (in μm KOVAR)	50	50	50	50
Total Thickness (in μm KOVAR)	50	100	200	300
250 Krad Time (months)	0.7	1.6	5.5	13.3
Inside Dosimeter				
Lid Thickness (in μm KOVAR)	0	50	150	250
Shield Thickness (in μm KOVAR)	250	250	250	250
Total Thickness (in μm KOVAR)	250	300	410	510
250 Krad Time (months)	8.9	13.3	26.4	45.9

INTEGRATED CHARGE MONITOR

June 4, 1996

Martin G. Buehler

Microdevices Laboratory
Jet Propulsion Laboratory
California Institute of Technology

1. INTRODUCTION: This effort is a follow-on effort to develop the Integrated Charge Monitor, ICM, for Lockheed Martin for use as dosimeters on their communication satellites. The original ICM1 was delivered in September 15, 1994. This effort differs from the first effort in that the first effort developed only a 1.2-µm device; whereas, in this effort both 1.2- and 0.8-µm devices were fabricated. Also, the maximum radiation level was 160 krad of Co-60; whereas, in this effort the maximum radiation level was krad of 1-MeV electrons. Finally, the field oxide n-FET was replaced by a diode to facilitate on-chip thermometry.

In this effort, 25 1.2-µm CMOS chips and 25 0.8-µm CMOS chips were designed and fabricated through MOSIS at the Hewlett-Packard facility, Corvallis, OR. The chips were packaged and tested at Halcyon Microelectronics, Irwindale, CA. The components were then electron irradiated and tested at JPL. The initial chip set consists of 25 1.2-µm CMOS devices designated ICM212 and 25 0.8-µm CMOS devices, designated ICM208. The ICM212 devices work extremely well; whereas, the ICM208 devices did not operate properly. Thus only 12 ICM2 devices were shipped to Lockheed Martin on May 20, 1996.

2. ICM2 CHIP: The chip is 2.48 mm x 1.76 mm and contains the eight devices listed in Table 1. A schematic layout of the chip in the package is shown in Fig. 1 and a photomicrograph is shown in Fig. 2. The chips were packaged in 16-pin flat packs using conductive epoxy and gold wire bonds. The wire bonding for the chip is shown in Fig. 1. Additional wire bonds were added, as shown in Fig. 3, to ground both the lid and the platform. The lid was attached to the package with conductive epoxy. The lid was altered to allow different shielding over each of the four p-FETs. The target shield thickness for each p-FET is listed in Table 1. The lid is thinned in two places over devices PG0 and PG2 with a 25-mil (0.64-mm)

dimple. A 25-mil (0.64-mm) hole was formed over device PG1. Because the lid contains a hole, the packages are not hermetic.

3. TEMPERATURE TESTS: The ICM2's were tested electrically at room temperature prior to lidding so that rework, if needed, could be easily done. All 25 ICM212s passed initial functional tests. Six ICM2 were measured at three different temperatures and a sample of the data is shown in Figs. 4 to 7. After electrical tests the devices were burned-in without bias at 125°C for 168 hours and centrifuged at 5000 g's.

4. VT DISTRIBUTIONS: Electrical tests were again conducted at room temperature and the results are listed in Table 1. The threshold voltage, VT, distribution is shown in Fig. 8 The VT distribution is very tight so that the devices can be considered identical. The standard deviation for the VT is 5 millivolts. This is important because it means that batch radiation calibration can be used.

At this point 12 devices were shipped to Lockheed Martin on April 29 and electron irradiation began at the JPL dynamatron facility. In the course of this test it was discovered that the lids of the ICMs were not grounded. This caused the devices to fail. Thus the 12 devices previously shipped to Lockheed Martin were recalled and additional bond wires added as shown in Fig. 3. The devices were retested and shipped to Lockheed Martin on May 20. The devices shipped to Lockheed Martin are designated LM in Table 2.

5. ELECTRON RADIATION CALIBRATION: The electron radiation test results are shown in Figs. 9 and 10. The tests were conducted at the JPL Dynamatron facility by Dr. Bruce Anspaugh. The results show the effect of the KOVAR lid in reducing the dose received by the p-FETs. The target Kovar lid thickness over each p-FET is given in Table 1. Measured values from four lids are listed in Table 3. The electron irradiation was conducted using a 1-MeV electron beam that had an 8-inch (20-cm) diameter. The dose rate was 10 rads/sec for dose increments of 40 rads and 20 rads/sec for dose increments of 80 rads. The devices were irradiated at room temperature in a vacuum of 1E-5 torr (1.33×10^{-6} kPa). The results show that the devices perform satisfactorily up to 600 krads of electron irradiation.

The PG1 curve shown in Fig. 9 was fitted with an algorithm developed for the ICM1 dosimeters [1]. The following analysis is applicable to the unshielded device, PG1. The algorithm is based on radiation-induced filling of p-FET gate-oxide traps and the generation of oxide-silicon interface states. The expression for the output voltage at room temperature is:

$$VO = VT_O + \Delta VT[1 - \exp(-D/D_V)] + \sqrt{[(2 \cdot ID/\beta_O) \cdot (1 + D/D_b)]} \qquad (1)$$

where VT_o is the initial threshold voltage, ΔVT is the trap filling voltage, D_V is VT dose coefficient, ID is the temperature-independent operating current (100 μA), β_o is the initial transconductance, and D_b is the β dose coefficient. In the analysis, the square root term was determined from the expression for the temperature independent operating point; see Eq. (17) in Ref 2:

$$\sqrt{[2 \cdot ID/\beta_o]} = VO_o - VT_o \qquad (2)$$

where VO_o is the preradiation value for VO. The fitting parameters are listed in Table 3.

The parameters indicate that the trap filling process is relatively small in that ΔVT = 70 mV and that the process is completed quickly in that D_V = 26.3 krad. The main factor that governs the shift in VO after 100 krads is interface-state generation. The above equation is the calibration curve for the dosimeter. Inserting the parameters listed in Table 1 in to Eq. 1 allows the calculation of VO at a given dose.

The results in Figs. 9 and 10 show that the radiation dose does not decrease as the thickness of the shield increases. The shielding dependence at maximum dose for Figs. 9 and 10 is plotted in Fig. 11. Shielding thickness measurements for the four shields are listed in Table 4. The values were measured using a dial indicator. These results can be explained by the nature of the dimples fabricated above PG0 and PG2. These features are about 25 mils (0.64 mm) in diameter and are difficult to center over the FET's located below. In the future these features should be increased to a diameter of 50 mils (1.28 mm).

Annealing results are shown in Fig. 12. Radiation testing is an accelerated test in that a ten-year mission dose is applied in a few hours. It is well known that higher dose rates lead to greater annealing of the radiation damage. The choice of the dose rate is driven by the economic factor that the electron beam cost/hour is a constant. In this case the dynamatron cost was $200/hour. Thus, one wants to irradiate at the highest dose rate to save money. The annealing behavior shown in Fig. 12 indicates a 4 percent decay in VO over a 20 hour period. This is acceptable and will allow a dose rate of 20 rads/sec to be used in the future.

6. IV CHARACTERISTICS: Typical current-voltage (IV) characteristics for the ICM2s fabricated in 1.2-μm CMOS are shown in Fig. 13. The p-FET characteristics overlap and are separated from the n-FET characteristics. In contrast to this

behavior, the IV characteristics for the ICM208 fabricated in 0.8-μm CMOS are shown in Fig. 14. These results are not satisfactory because the p-FET characteristics do not overlap. A number of explanations were examined briefly including latch-up and Op Amp oscillation. More measurements are needed to determine the cause of these results. It is important to understand the cause for the difficulties with the ICM208 parts because the 1.2-μm CMOS process may not be available in the future.

7. DISCUSSION: The 1.2 μm p-FET's have very tight VT's where the standard deviation is 5 mV so batch radiation calibration can be used. One device was irradiated to 600 krads and was still operating properly. The electron irradiation showed that the trap filling process is completed by 100 krads and thereafter the process is characterized by interface-state creation. As seen in Fig. 11, the radiation dose does not decrease as the shield thickness increases for devices PG0 and PG2. The lid dimples need to be increased from a diameter of 25 mils (0.64 mm) to 50 mils (1.28 mm) to ensure that the p-FETs are correctly centered under the shields. Also the shield thickness values need to be examined. The data from ICM1 flown on Telstar should be evaluated to see if there is sufficient spread in data from the four p-FETs. As seen in Fig. 11, thinner shields are needed to provide a better spread in the radiation response. After redesigning the shields, the effectiveness of the choices needs to be verified by electron radiation tests.

The packages experienced a number of handling and testing steps. This caused some of the package leads to break as noted in Table 2. In this effort the packages were mounted and demounted in the chip carriers and tested at least four times. The insertion of the packages into the chip carriers and subsequent testing places considerable stress on the package leads. It is suggested that the leads of the packages chosen for flight be given a rigorous visual inspection.

The development of ICM208 is imperative because the 1.2-μm CMOS process is an aging process. The redesign of ICM208 should include the use of internal test points to aid in chip probing in case of difficulty. Also certain metal features need to be designed for laser cutting during problem diagnosing. The electrical tests must include chip current measurements to assess the occurrence of latch-up.

8. REFERENCES

1. A. Bogorad, C Bowman, A. Dennis, J. Beck, D. Lang, R. Herschitz, M. Buehler, B. Blaes, and D. Martin, "Integrated Environmental Monitoring System for Spacecraft," IEEE Trans. on Nuclear Science, NS- 42, 2051-2057 (1995).

2. M. G. Buehler, B. R. Blaes, G. A. Soli, and G. R. Tardio, "On-Chip p-MOSFET Dosimetry," IEEE Trans. on Nuclear Science, NS- 40, 1442-1449 (Dec. 1993).

Table 1. ICM2 Devices and Shield Thickness

DEVICE	TYPE	W(μm)	L(μm)	TARGET SHIELD THICKNESS KOVAR mil	mm
PGO	GATE OXIDE p-FET	193.54	9.6	6	150
PG1	GATE OXIDE p-FET	193.54	9.6	0 (hole in lid)	
PG2	GATE OXIDE p-FET	193.54	9.6	2	50
DP3	pn DIODE	---	---	10	250
RM4	METAL-1 RESISTOR	2.4	24214	10	250
NG5	GATE OXIDE n-FET	193.54	9.6	10	250
EX6	EXTERNAL RESISTOR	NA	NA	NA	
PG7	GATE OXIDE p-FET	193.54	9.6	10	250

Table 2. Test Results After Centrifuge and Burn-in. Devices used for temperature tests are noted by TEMP and those used for electron irradiation are noted by E-RAD. Devices delivered to Lockheed Martin are denoted by LM.

DEV NUMBER	COMMENTS	VT(V) PG0	VT(V) PG1	VT(V) PG2	VT(V) PG7	VT(V) NG5	R(ohm) RM4	n DP5
icm21201	OK -Needs lid GNDed	0.870	0.870	0.870	0.867	0.682	3299	1.02
icm21202	E-RAD	0.866	0.866	0.864	0.867	0.671	3384	1.12
icm21203	P7 BAD	0.846	0.846	0.847	-0.237	-0.248	2953	2.48
icm21204	BAD	0.148	0.184	0.161	0.131	0.142	-953	4.61
icm21205	TEMP, E-RAD	0.867	0.868	0.868	0.869	0.674	3367	1.12
icm21206	GND pin bad-useable	0.863	0.862	0.862	0.863	0.683	3366	1.12
icm21207	TEMP, LM	0.862	0.862	0.863	0.862	0.668	3331	
icm21208	TEMP, LM	0.874	0.874	0.868	0.869	0.680	3272	1.06
icm21209	OK- to be repackaged.	0.869	0.865	0.869	0.865	0.674	3360	1.05
icm21210	LM	0.865	0.865	0.862	0.863	0.675	3356	1.11
icm21211	LM	0.867	0.867	0.860	0.866	0.675	3334	1.05
icm21212	E-RAD	0.870	0.870	0.873	0.871	0.681	3293	1.09
icm21213	LM	0.858	0.860	0.858	0.863	0.670	3388	1.12
icm21214	TEMP, E-RAD	0.881	0.874	0.875	0.875	0.669	3287	1.02
icm21215	LM	0.873	0.872	0.873	0.875	0.672	3316	1.02
icm21216	E-RAD	0.863	0.863	0.872	0.869	0.676	3353	1.11
icm21217	BAD VDD pin-rewire	0.860	0.860	0.860	0.860	.668	3361	
icm21218	TEMP, P2 HIGH, LM	0.876	0.876	0.895	0.875	0.670	3272	1.02
icm21219	OK - no lid	0.870	0.870	0.867	0.867	0.663	3308	
icm21220	LM	0.874	0.874	0.864	0.866	0.684	3303	1.02
icm21221	TEMP, LM	0.867	0.869	0.868	0.875	0.677	3343	1.05
icm21222	LM	0.868	0.868	0.872	0.873	0.681	3291	1.02
icm21223	LM	0.872	0.865	0.861	0.861	0.681	3371	1.09
icm21224	LM	0.879	0.879	0.874	0.878	0.667	3309	1.12
icm21225	BAD	0.866	0.866	0.863	0.865	0.660	3380	

Table 3. Electron Calibration Parameters for ICM21216

PARAMETER	UNITS	VALUE
VO_o	V	1.504
VT_o	V	0.868
$\sqrt{[2 \cdot ID/\beta_o]}$	V	0.636
ΔVT	V	0.070
D_v	krad	26.3
D_b	krad	95.0

Table 4. Target and Measured Shield Thicknesses

DEVICE NO.	THICKNESS PG0 (mil, μm)	THICKNESS PG2 (mil, μm)
TARGET	6.0 150	2.0 51
12	5.2 130	3.0 76
16	4.2 110	3.3 84
19	5.0 130	2.7 69
25	4.2 110	3.0 76

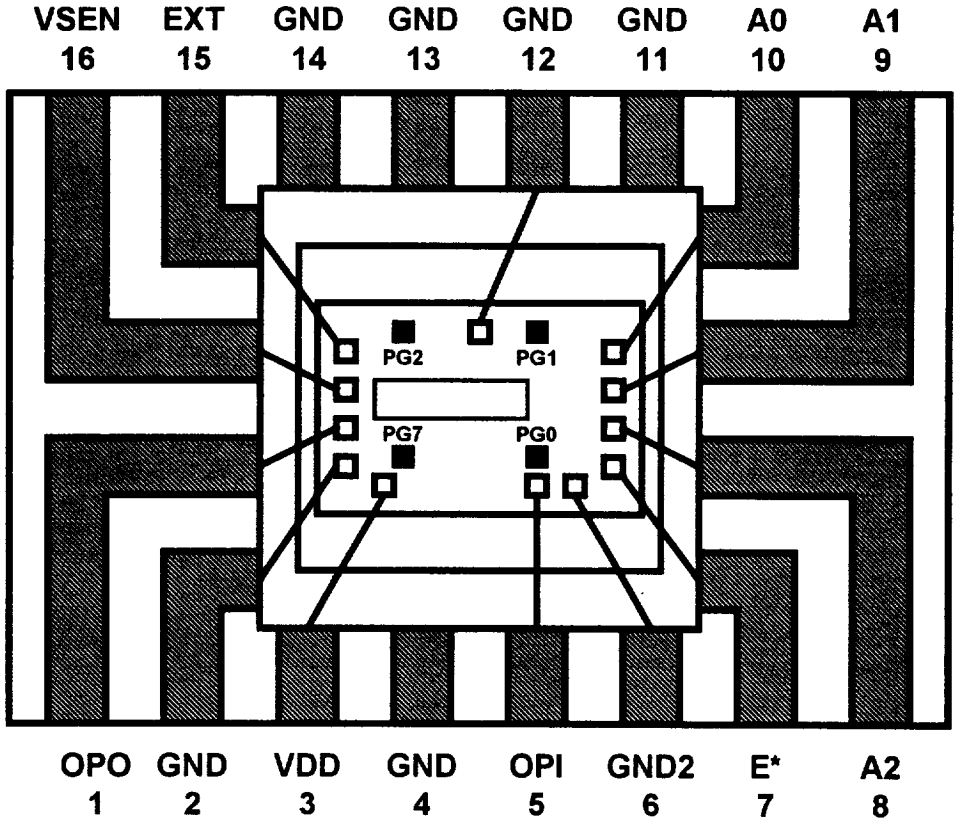

Figure 1. ICM2 chip wire bonded to a 16-lead flat package. The hole in the lid is directly over p-FET PG1 which can be used to locate pin one of the package.

Correct alignment of the lid relative to the chip can be determined by looking through the hole over PG1 and observing the square p-FET PG1 and the words "12" above "ICM2"; see Fig. 2.

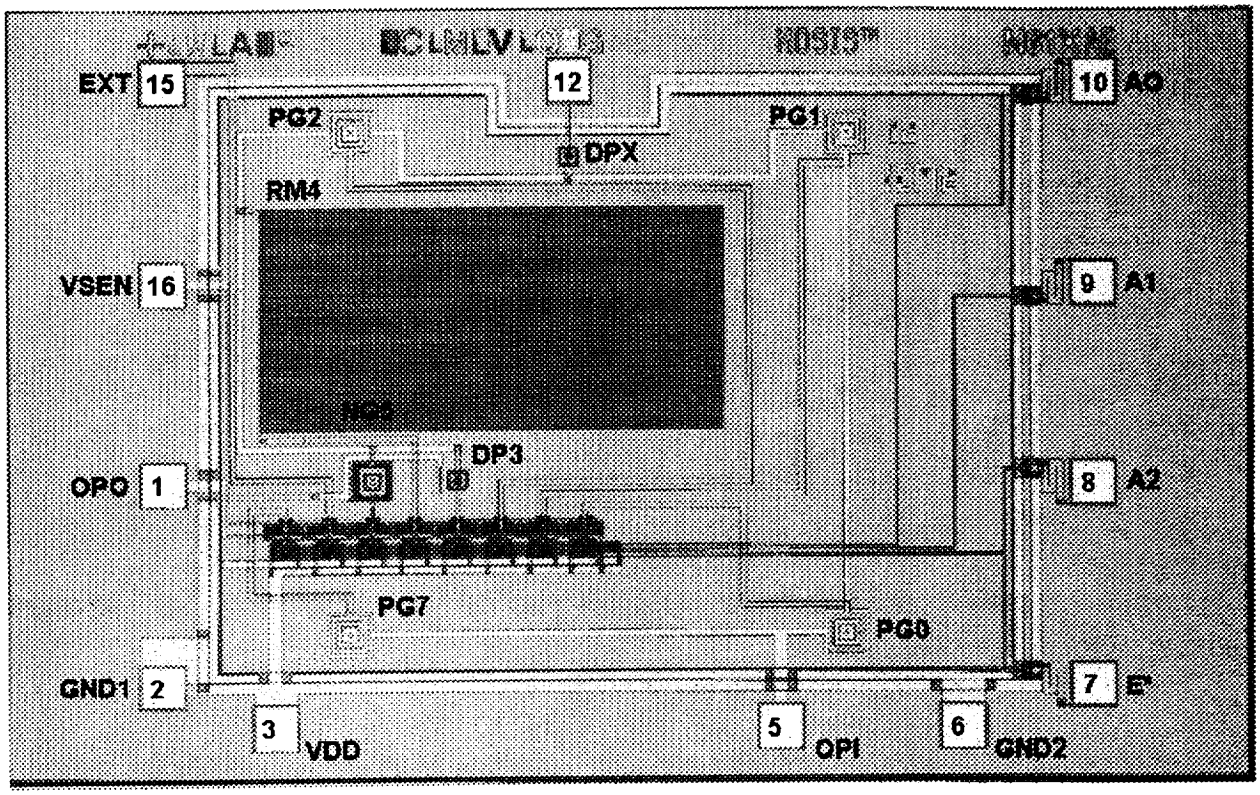

Figure 2. Integrated charge monitor (ICM212) chip 2.48 mm x 1.76 mm.

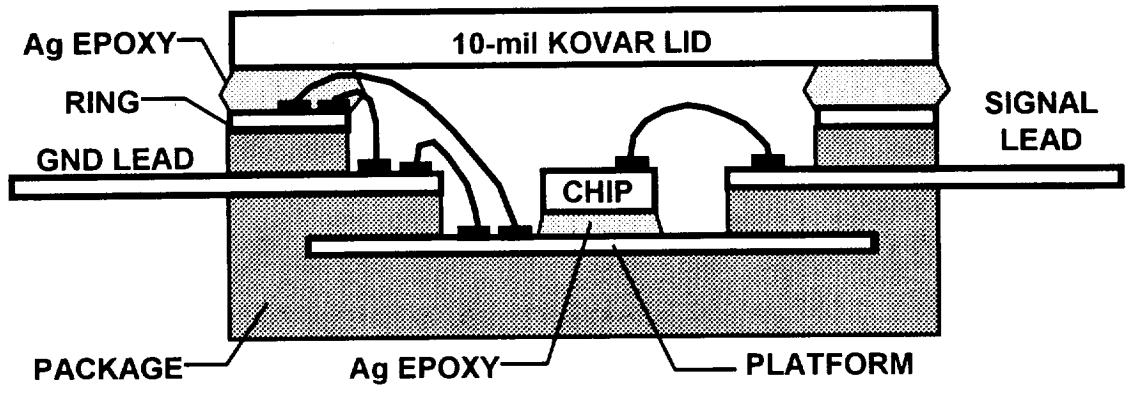

Figure 3. Cross section of the ICM2 package showing the additional wire bonds used to ground the platform and the KOVAR lid.

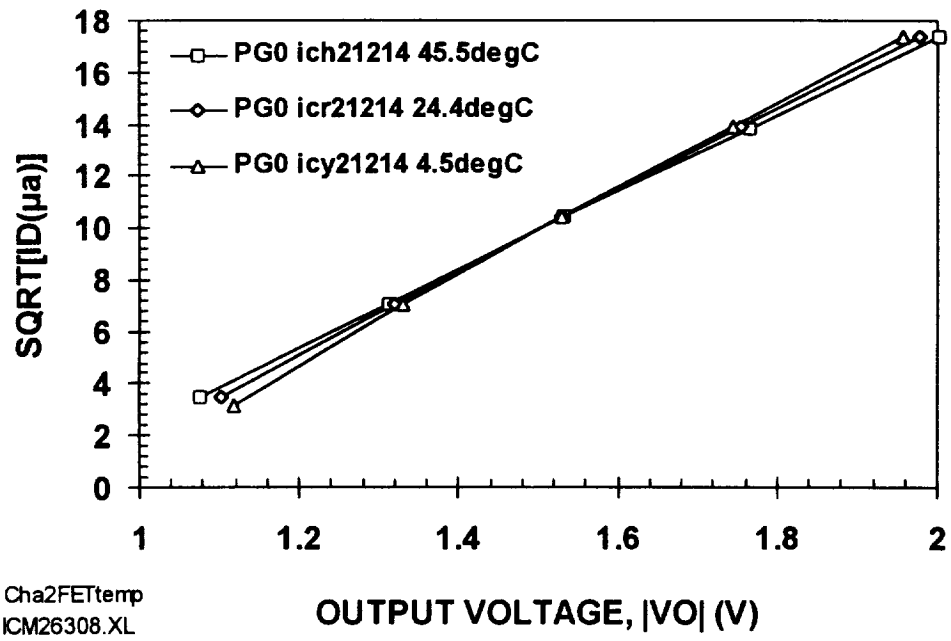

Figure 4. p-FET temperature characteristics showing the temperature independent point near 100 μA.

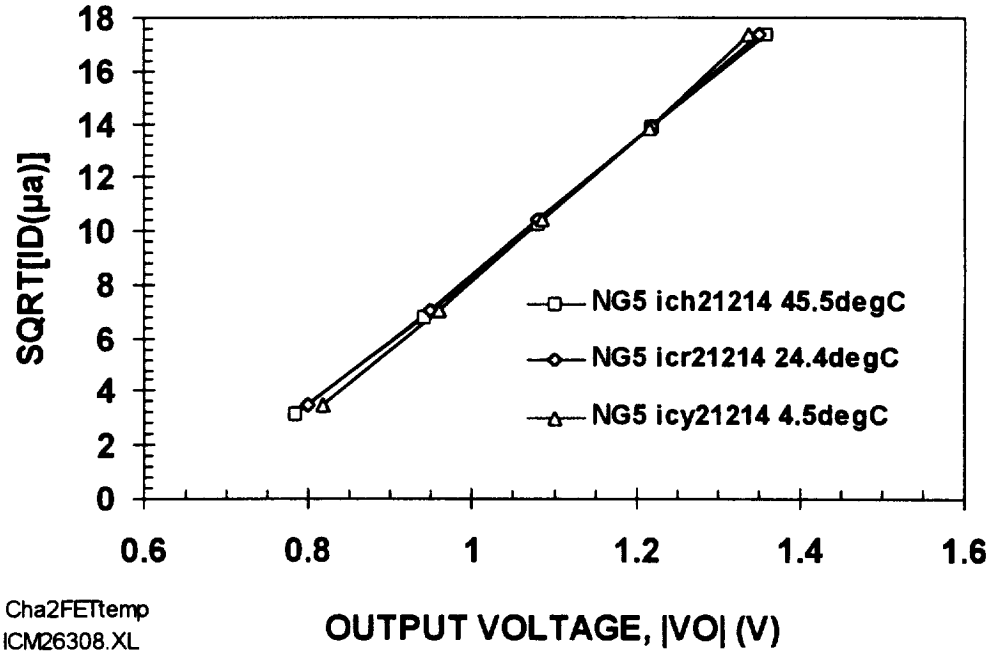

Figure 5. n-FET temperature characteristics showing the temperature independent point near 150 μA. The n-FETs are useful in assessing failures at high dose levels.

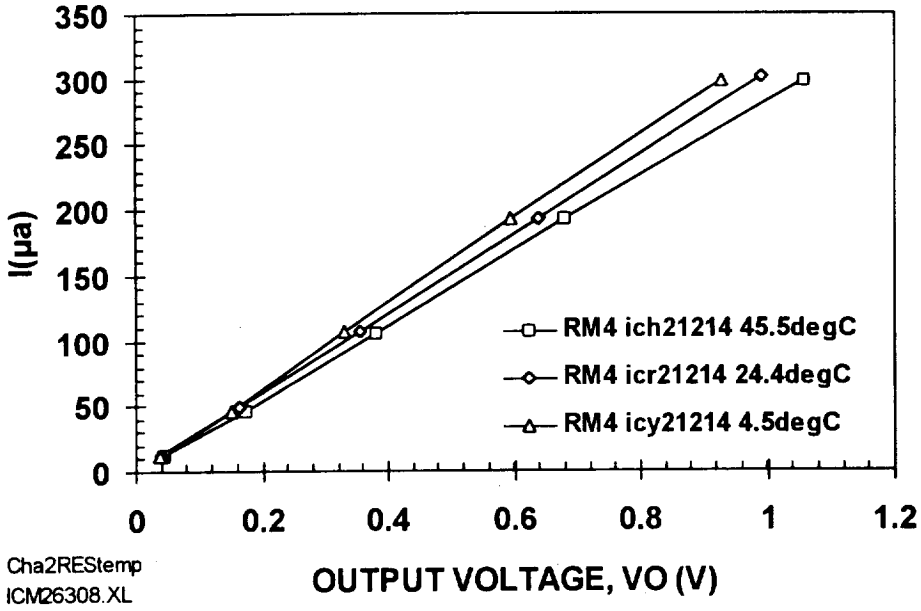

Figure 6. Metal-1 temperature characteristics showing a temperature coefficient of 3215 ppm/°C. This metal resistor serves as an on-chip reference device that is presumably independent of radiation.

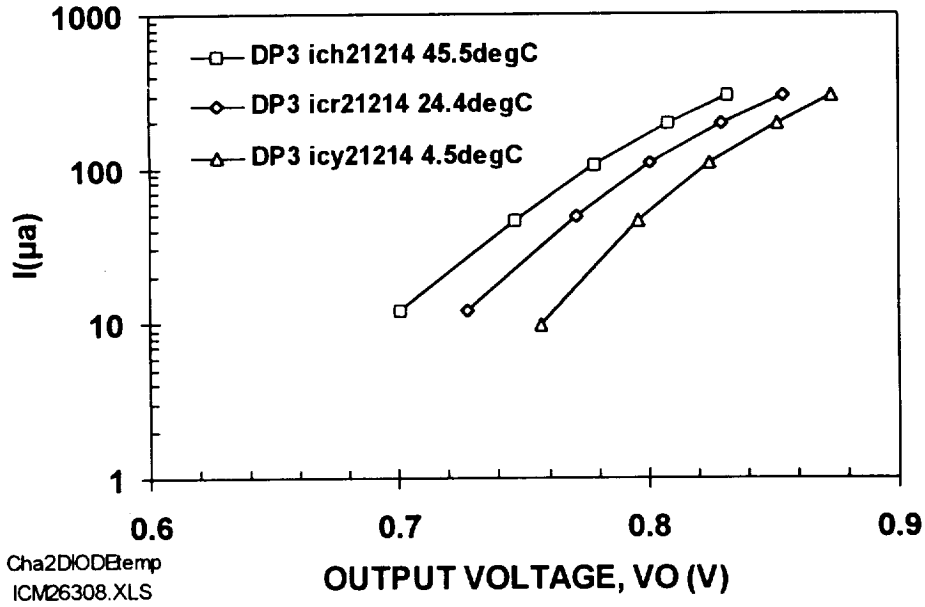

Figure 7. pn diode temperature characteristics showing a temperature sensitivity of -1.5 mV/°C at 10 μA. This diode serves as an on-chip thermometer.

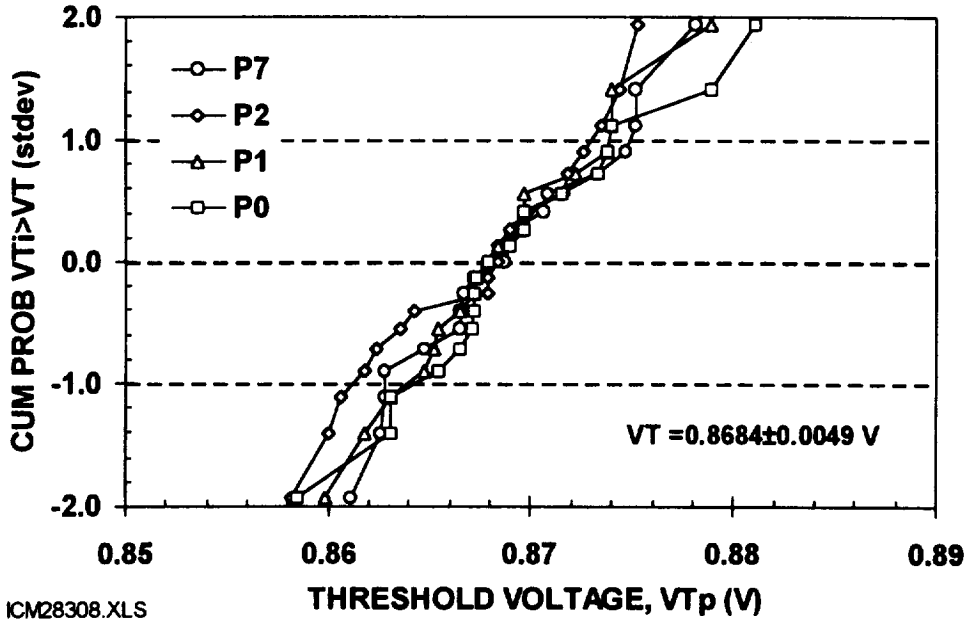

Figure 8. Room temperature (22°C) p-FET threshold voltage distributions from 19 ICM2 packages containing four p-FETs, P0, P1, P2, and P7. The average and standard deviation for the distribution is 0.868 ± 0.005 V. The standard deviation is as usual very tight at 5 mV allowing batch radiation calibration. A total of 76 p-FETs are shown on this chart.

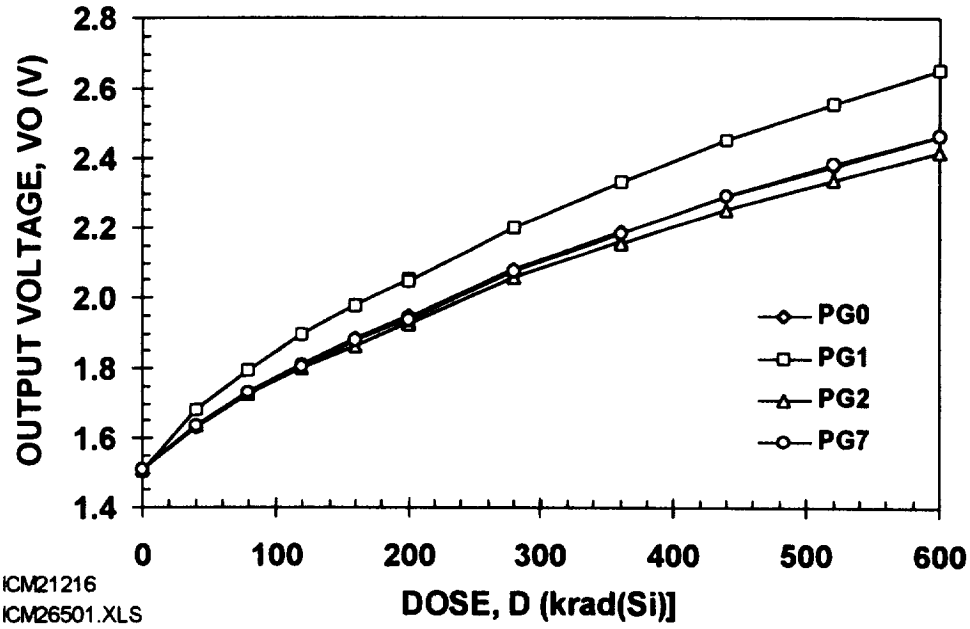

Figure 9. 1-MeV electron irradiation response of device ICM21216 measured at 100 μA, room temperature, and in a vacuum.

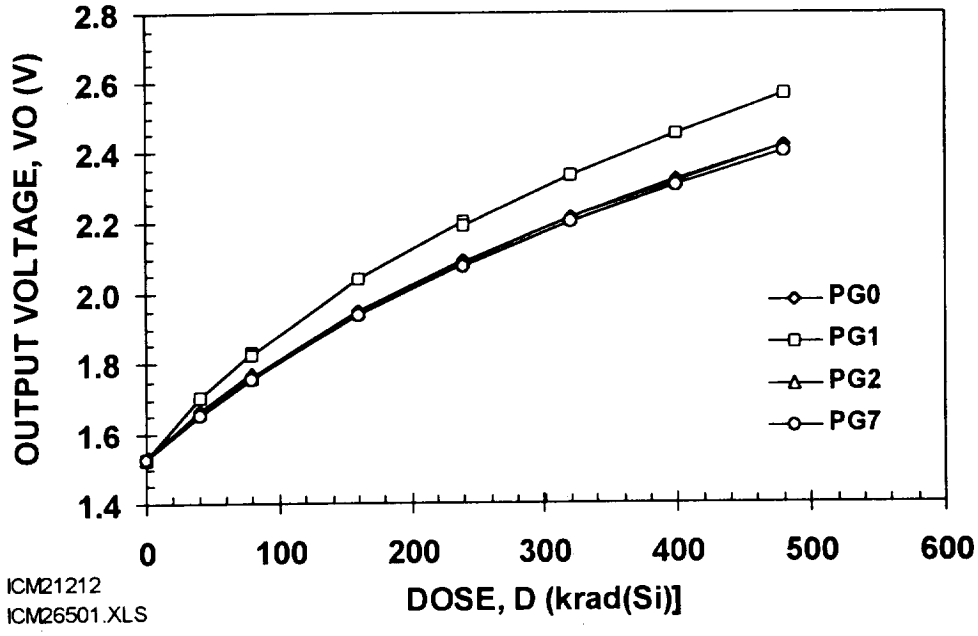

Figure 10. 1-MeV electron irradiation response of device ICM21212 measured at 100 µA, room temperature, and in a vacuum.

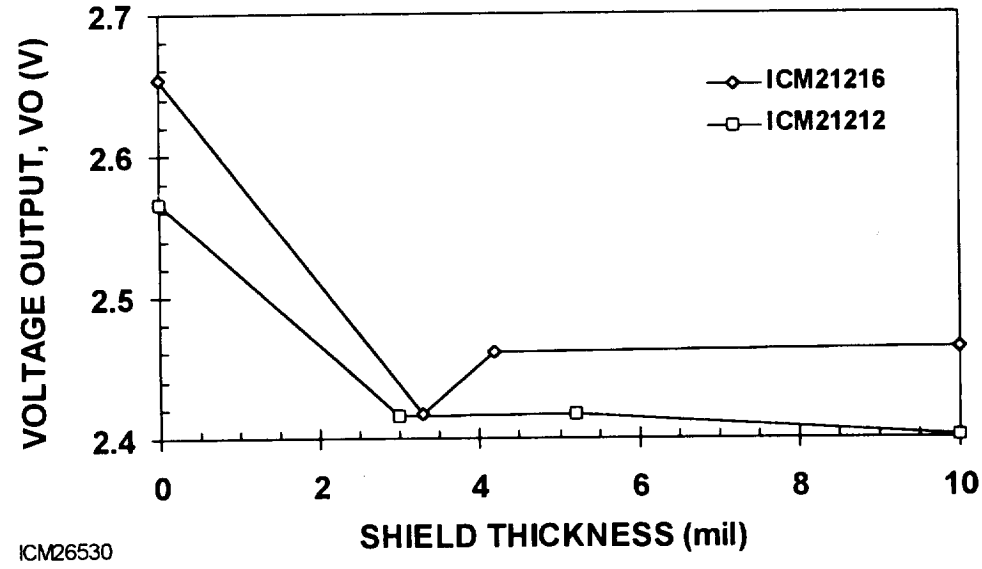

Figure 11. KOVAR shielding results for ICM21212 and ICM21216 at the maximum dose. For ICM21212, Dmax = 480 krads and for ICM21216, Dmax = 600 krad. The devices were irradiated with a 1-MeV electron beam.

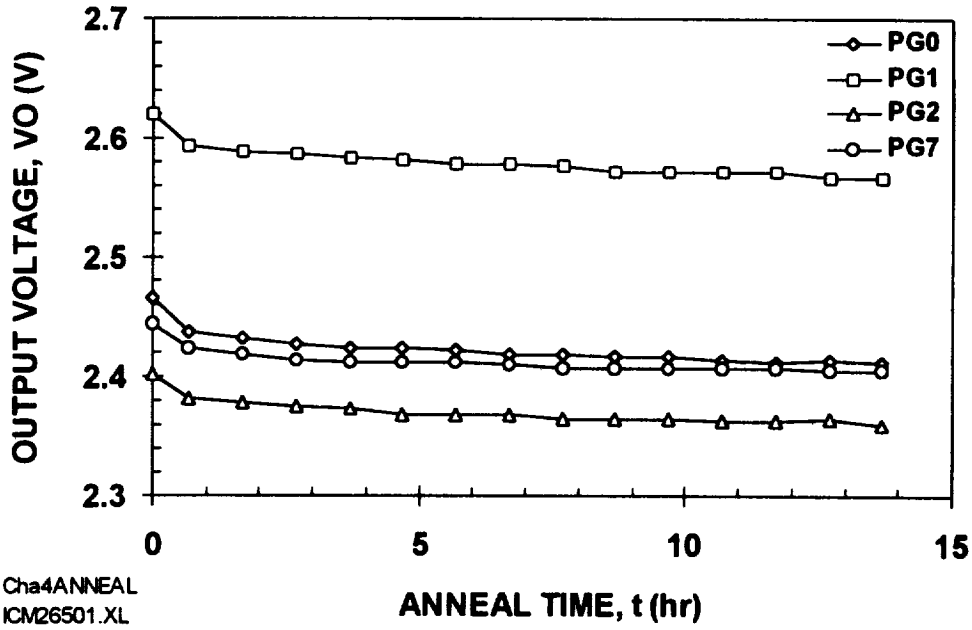

Figure 12. Annealing results for ICM216 measured at 100 µA after a 1-MeV electron irradiation at 20 rads/sec.

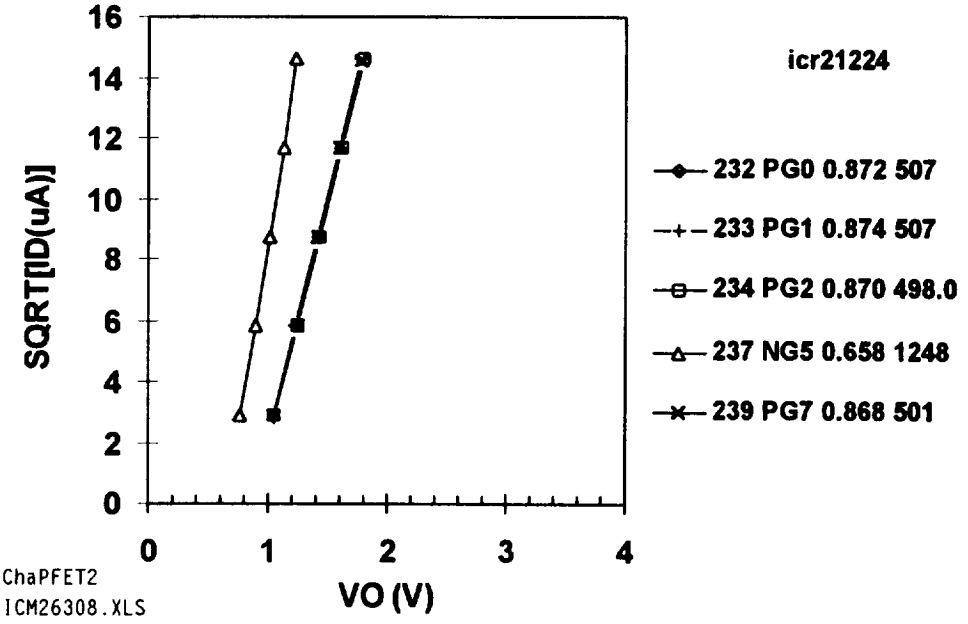

Figure 13. Typical IV characteristics for the four p-FETs and one n-FET from ICm21224. Note the p-FET characteristics overlap.

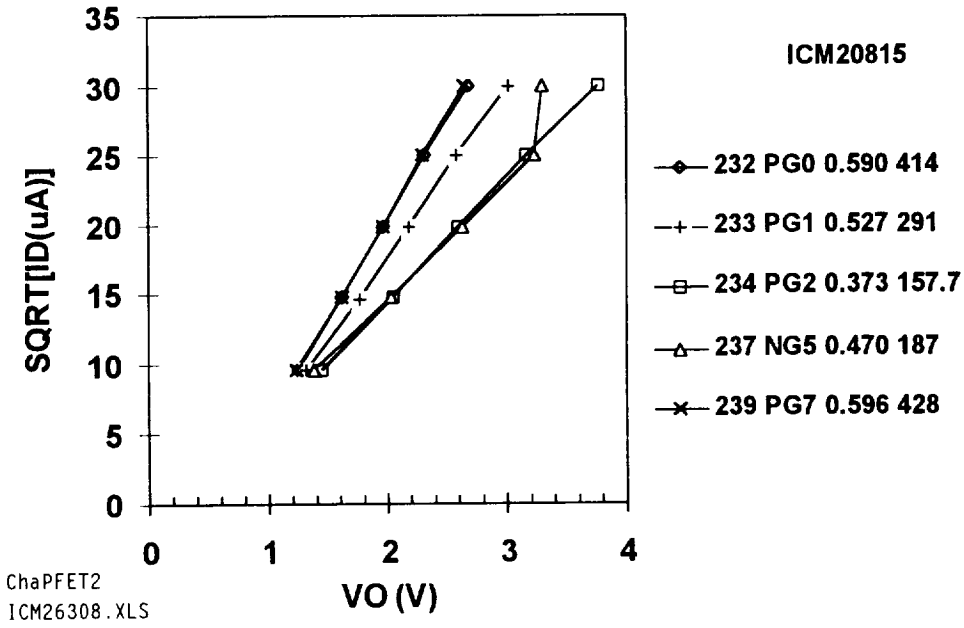

Figure 14. Typical IV characteristics for ICM208.

Presented at the Nuclear and Space Radiation Effects Conference (July 1996)

p-FET Derived Proton-Beam Dose-Depth Curves

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ABSTRACT: An array of four p-FETs was used to obtain dose-depth curves for the 100 MeV proton beam at the Loma Linda Proton Therapy Facility. The p-FET dosimetry compares extremely well with ionization chamber results and tends to resolve the peak and distal edge region more sharply.

INTRODUCTION: The use of the p-FET (p-type Field Effect Transistor) for radiation dosimetry is based primarily on the charging of the gate oxide through the capture of holes created by the passage of high energy photons or particles. The holes add positive charge to the oxide which is detected as a shift in the FET threshold voltage.

For many years p-FETs have been used for space flight dosimetry [1]. More recently, the devices were used for personal radiation dosimetry [2]. The device used here, is termed RADMON (Radiation Monitor), and consists of a multiplexed array of four p-FETs. It was developed for communication satellite dosimetry [3, 4]. This effort is directed at transferring the space radiation dosimetry to the medical community.

The dose-depth curve for protons has a unique shape as shown in Fig. 1. The uniqueness has to do with the peak that occurs near the proton's end-of-range. X-ray dose-depth curves have a monitonic decreasing dose-depth curve. The data shown in Fig. 1 was obtained using a conventional ion chamber. The ion chamber dose-depth methodology is time consuming and, as will be shown, lacks the spatial resolution of p-FET dosimetry.

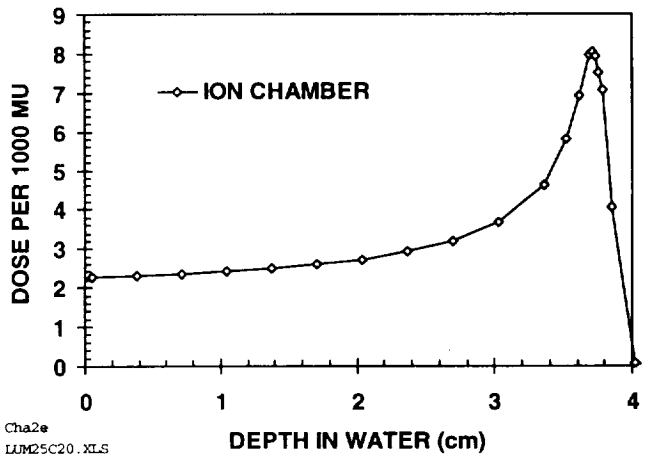

Figure 1. Ion chamber response to a 100 MeV proton beam passing through water.

The proton response of an ion chamber, shown in Fig. 1, is considered the reference response which the RADMON must match. The dose is expressed in MU, measurement units. The critical features of this curve are its shape and the characteristic number which describes the peak to zero depth ratio. This ratio is 3.5. Thus, the objective of this effort is to evaluate the use

of an array of p-FETs each with its own shield for use in proton dosimetry and compare test results with conventional ion chamber dosimetry.

RADMON measurements were taken at the Loma Linda Medical Center (LLUMC) using a 2.54-cm diameter, 100 MeV proton beam which delivered a dose of 480 rads/min. The experiment took four hours during which 49 data points were acquired.

RADMON FABRICATION: The RADMON used in this experiment was designed previously as the Integrated Charge Monitor (ICM1) [4]. The RADMON, shown in Fig. 2, was refabricated by Hewlett Packard using their 1.2-um CMOS process with a gate-oxide thickness of 21 nm. The chip consists of the devices listed in Table 1. The devices are addressed with a multiplexer (MUX) that is described later.

The important devices for this study are the four p-FETs, P0, P1, P2, and P7 which are located on 1.25-mm centers as seen in Fig. 2. The devices are closed geometry FETs with the channel width, W, and length, L, as listed in Table 1.

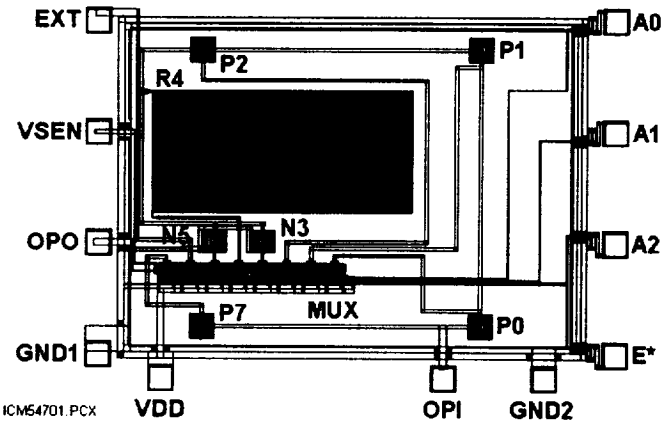

Figure 2. RADMON chip, 1.8 mm x 2.5 mm, fabricated in 1.2-µm CMOS. p-FETs located on 1.25-mm square at P0, P1, P2, and P7. The p-FET oxide is 20-nm thick.

The chip was packaged in a 16-pin flat package as seen in Fig. 3 with 1-mil (25-nm) Au wire bonds. The chip is attached to the package's Au-plated Kovar platform with conductive epoxy. Au-wire bonds are used to ground the platform. Another Au wire bond was used to ground the lid of the package. This Au wire connects an internal package pad to an external package pad. Ag epoxy is applied to the Au ring that surrounds the top of the package. The combination of the Au ring, the Ag epoxy and the Au wire bond grounds the Kovar lid. This grounding procedure prevents the buildup of charge on an electrically floating lid which could cause an electrical discharge that damages or destroys the chip.

Table 1. Device Dimensions

NO	DEVICE	DESCRIPTION	W µm	L µm
P0	p-FET	Poly Gate Oxide	193.5	9.6
P1	p-FET	Poly Gate Oxide	193.5	9.6
P2	p-FET	Poly Gate Oxide	193.5	9.6
N3	n-FET	Metal Field Oxide	193.5	9.6
R4	Resistor	Metal-1	2.4	24214
N5	n-FET	Poly Gate Oxide	193.5	9.6
E6	External	External device	NA	NA
P7	p-FET	Poly Gate Oxide	193.5	9.6

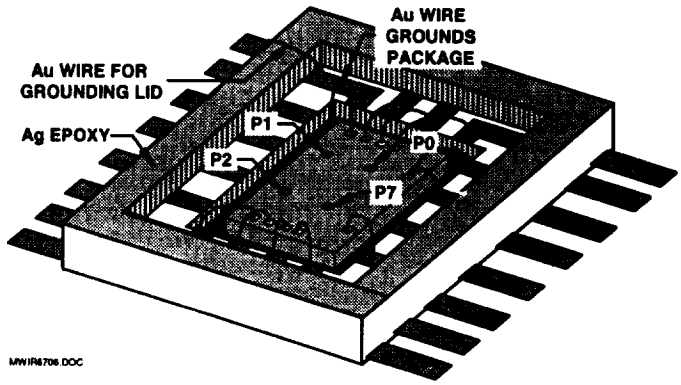

Figure 3. RADMON wire-bonded to 16-pin flat package. All portions of the package grounded to prevent charge build-up.

The lidded device is shown in Fig. 4. The p-FETs are located at the corners of a 1.25-mm square. p-FET P0 has a 125-µm Kovar shield, P1 has no shield, P2 has a 75-µm Kovar shield, and P7 has a 250-µm Kovar shield. The Kovar was chem-etched to thin the lid over P0 and P2. In the following measurements, it is assumed that the proton beam is uniform over the four p-FETs since the beam is 2.54 cm in diameter.

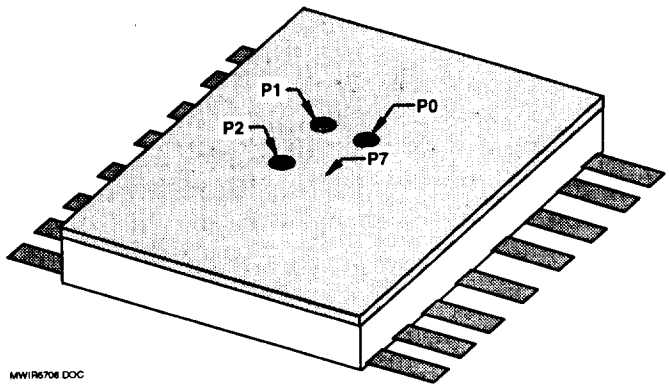

Figure 4. RADMON shielded by a KOVAR step lid.

SURROUND CIRCUITRY: The equivalent circuit used to test the RADMON is shown in Fig. 5. The p-FETs are placed in the feedback loop of an Op Amp and a 100 μA current is forced at the temperature-independent point [3]. The multiplexer is represented by two resistors, labeled by R_{mux}, in the figure. This approach is needed because solid state switches have a non-negligible resistance. Op Amp U2 senses the potential at the p-FET and thus eliminates the need to know the value of R_{mux}. In the measurement procedure, the output of U1, VO, is nulled by V_{off} and U2 amplifies VO by the ratio of R_2 to R_1 which was set to 10. The output of U2, V_{amp}, is measured by the 12-bit ADC.

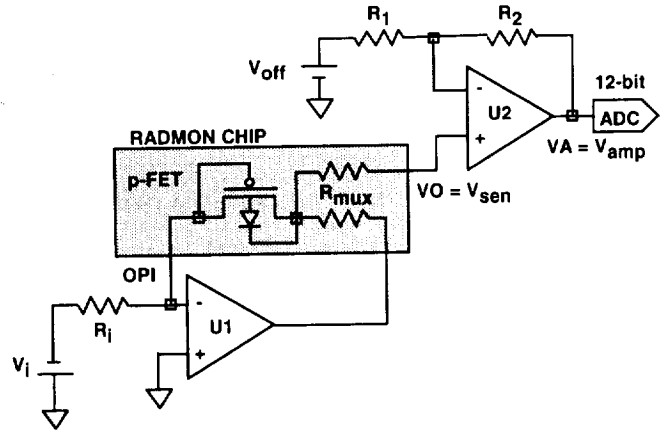

Figure 5. Simplified circuitry for measuring the p-FET where U1 provides constant current via V_i and R_i. The output of U1 is nulled via V_{off} and U2 amplifies VO via R_1 and R_2. Op Amps, U1 and U2, used in this experiment were dual SOIC LMC6042.

EXPERIMENT: The experiment was designed to emulate ion chamber test conditions as closely as possible. The beam condition was identical for the ion chamber and RADMON tests. In the ion chamber experiment, the ion detector was moved away from the proton nozzle in a water tank. In the RADMON experiment, the p-FETs were fixed relative to the proton nozzle and various polystyrene shields were placed between the nozzle and the RADMON.

The proton beam was 2.54 cm in diameter, had an energy of 100 MeV, and delivered a dose of 480 rads/minute. In this experiment a *run* was defined as the proton beam being *on* for 2.5 minutes; thus, the dose/run was 1200 rads/run. Throughout the 49 runs which comprised this experiment, the dose/run was constant. Three runs constitute a *cycle* during which one absorber was used. A cycle is illustrated in Fig. 5. Electrical measurements were taken before and after each run thus each cycle consists of four electrical measurements. The cycles were characterized by a mean run number, N. The RADMON test time/run was about 10 seconds. The total time/cycle was less than 10 minutes. After the cycle was completed the absorber was changed and a new cycle begun.

The equipment consisted of a Compaq 486/33 MHz Aero lap computer, a National Instruments DAQPad-1200, and a test box. The data acquisition program was written in Visual BASIC. During each cycle, the four electrical tests were run autonomously by the laptop with dwell times allowed for beam *on* time. Progress of the electrical tests was monitored by writing messages to the laptop screen in large letters which were visible on the control room monitor via the beam room camera. Thus, from the control room, the operator saw when the electrical tests were completed and turned the beam *on*. After completion of a cycle, the absorber was changed. Also the data, written to a floppy disk, was taken to the control room for immediate analysis. This allowed absorbers to be chosen for subsequent cycles so that gaps in the dose-depth curve could be filled.

The data for a cycle is shown in Fig. 6. These data were fitted with a line using the least squares method. For the data shown in Fig. 2,

the slope of the line, dVamp/dN, is 40.48 mV/run and the standard deviation is 1.6 mV/run.

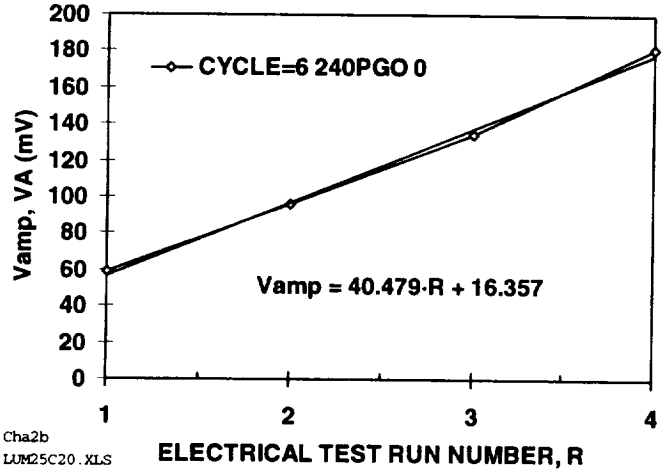

Figure 6. Measurement cycle used to determine the "dose" behind an absorber. In this case the no absorber was used. The proton beam was *on* for 2.5 minutes between each of the four RADMON measurements.

DATA ANALYSIS: The data acquired during this experiment was influenced by two factors: (a) The p-FETs were "dosed" by the proton beam during the experiment thus the p-FET output voltage is a nonlinear function of dose. (b) The thickness of the Kovar lid over each of the four p-FETs is different thus the equivalent Kovar thickness must be added to the polystyrene absorber thickness.

The FET dosing effect is modeled as follows. The FET detects radiation by absorbing radiation induced holes in oxide traps. The trap filling process is described by a rate equation for the number, n, of holes that fill oxide traps:

$$dn/dt = \sigma \cdot \varphi (N_t - n) \qquad (1)$$

where σ is the hole cross section, φ is the proton flux, N_t is the total number of holes in the oxide, and t is time.

The above equation is transformed to the following model equation:

$$dVO/dN = (\Delta VO - VO)/N0 \qquad (2)$$

where VO is the output voltage of the p-FET which is proportional to n, ΔVO is the shift in the FET output voltage which is proportional to N_t, N is the mean run number which is proportional to t or dose, and N0 is inversely proportional to $\sigma \cdot \varphi$. The solution to this equation is:

$$VO = VO_0 + \Delta VO[1 - \exp(-N/N0)] \qquad (3)$$

where VO_0 is the p-FET output voltage at N = 0 and is about 1.5 V at 100 µA for the p-FETs used in this experiment. This equation models the increase in the operating voltage of the p-FET with increasing N (or dose) and shows a decrease in the rise of VO at high dose where hole traps are filled.

The slope of Eq. 3 is:

$$dVO/dN = (\Delta VO/N0)\exp(-N/N0) \qquad (4)$$

which shows that dVO/dN decreases with increasing dose due to trap filling.

The effect of trap filling was removed by determining ΔV/N0 for each cycle by rearranging Eq. 4:

$$\Delta VO/N0 = (dVO/dN)\exp(N/N0) \qquad (5)$$

That is, the corrected slope, ΔV/N0, is determined from the measured slope dVO/dN times exp(N/N0).

The implementation of this correction requires N0. For fitting purposes, the above equation was linearized as follows:

$$\ln[dVO/dN] = \ln(\Delta VO/N0) - N/N0 \qquad (6)$$

where dVO/dN and N are the measured quantities and ΔVO/N0 and N0 are coefficients to be determined.

Multiple data points were acquired at polystyrene shield thicknesses of zero and 3.64 cm. The data, plotted in Fig. 7, clearly shows the effects of radiation dosing on the performance of the p-FET. That is the initial slope measured at the beginning of the experiment is lower toward the end of the experiment.

The data shown in Fig. 7 were fitted simultaneously using the least squares method. The result yielded N0 = 75.94. The RADMON dose-depth data were corrected using Eq. 5 and this value for N0.

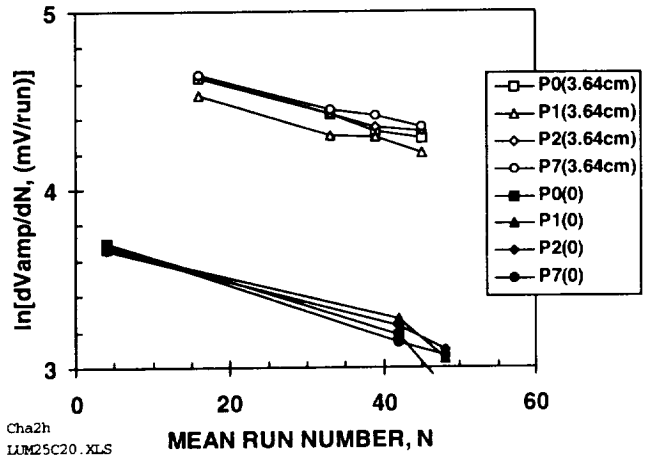

Figure 7. Determination of N0, the trap filling parameter, using the trap filling model where N0 = 75.94.

The second correction to the RADMON dose-depth curves involved determining the equivalent polystyrene thickness for the Kovar lid. This was done by shifting each of the dose depth curves until they overlapped the distal edge of the ion gage response. The factor for this adjustment was:

$$H(mm)_{polystyrene} = 50 \cdot H(mm)_{Kovar} \quad (7)$$

The results are listed in the key of Fig. 8. The maximum correction occurred for thickest Kovar lid of 0.25 mm which is equivalent to 1.25 mm of polystyrene.

The results of the data analysis are shown in Fig. 8. These data also show the ion chamber data plotted in Fig. 1 where the vertical axis of Fig. 1 was multiplied by 18 to bring the results into coincidence.

It is worth examining the RADMON dose-depth curves before the application of the step shield thickness correction. The data are shown in Fig. 9. The behavior in the distal edge region shows that the data are shifted properly with respect to the Kovar shield thickness. That is, the distal edge for P7 with a 250-μm Kovar shield falls at a smaller polystyrene thickness and the distal edge for P1 with no shield falls at a larger polystyrene thickness. This data shows the possibility that an array of p-FETs each with its own shield can be used to obtain the dose-depth curve including the shape in the distal edge region.

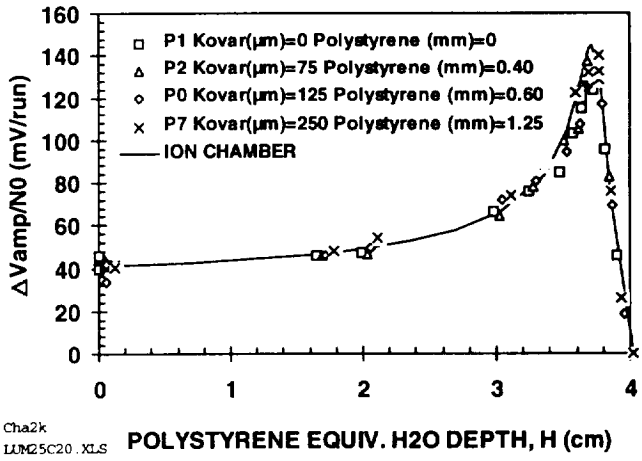

Figure 8. RADMON and ion chamber dose-depth curves for a 100 MeV proton beam. The RADMON data was corrected for gate-oxide trap filling and for step shield thicknesses. Notice that the p-FET results cluster within the ion chamber response thus showing a sharper peak response for the p-FETs.

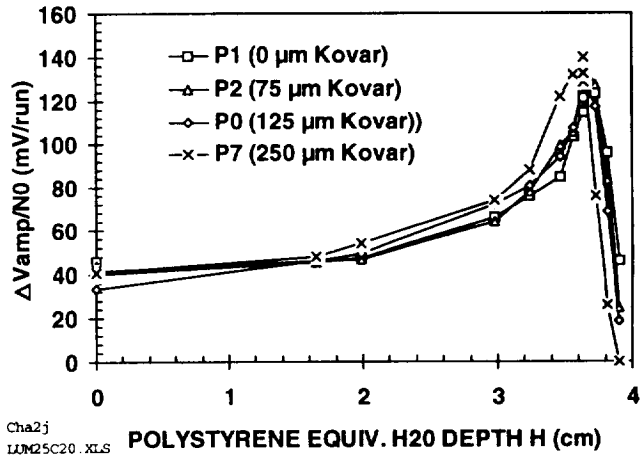

Figure 9. Data corrected for trap filling only. Effects of the Kovar step shield are clearly visible in the distal edge region. This indicates the possibility of profiling the distal edge region with a step shield and a single radiation sequence.

DISCUSSION: A comparison of the RADMON with the ion chamber, shown in Fig. 8, indicates good agreement in that there is a close correspondence between the two detectors for the 100 MeV proton beam. In fact, the RADMON appears to show that the peak region is sharper than the ion chamber data. This is expected since the ion chamber, which is 1 mm thick, is much thicker than the p-FET gate oxide, which is 20 nm thick. That is, the detecting region of the p-FET is 50,000 times thinner than the ion chamber.

CONCLUSION: This experiment showed that dose-depth curves for both the ion chamber and the RADMON are very close. The experiment also showed that the p-FET data can be corrected for the effects of proton beam dosing and Kovar absorber thickness. In addition, the data in the distal edge region as seen in Fig. 5 showed that an array of individually-shielded p-FETs can be used to characterize the proton beam with one radiation sequence.

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SAMMES RADIATION DOSIMETERS

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INTRODUCTION: This experiment is the second dosimetry experiment delivered to SAMMES (Space Active Modular Materials Experiments). The dosimeters were delivered in September 1994 and launched in June 1995 on the aborted Pegasus vehicle.

This experiment consists of p-FETs used to measure the radiation dose and capacitors used to monitor the build-up of charge in their dielectrics. These devices use the electronic circuitry designed to measure the resistance of the SAMMES actinometers. The p-FET dosimeters are custom designed p-FETs that are placed behind a number of shields with different thicknesses to verify the dose-depth curves used to design spacecraft shields. Currently, the dose-depth curves are based on computer codes that trace their roots to the NASA AP-8 and AE-8 developed in the 70's [1].

The capacitors used in this experiment are surface mount capacitors that are commonly used in the electronic circuits. As far as the experimenter knows, this is the first time that such capacitors have been flown in a test mode in space. The capacitors are being flown behind two different shields to study the effects of radiation on the capacitor's electrical properties. The understanding of deep dielectric charging is one of the major unsolved problems facing Earth orbiting spacecraft. A deep dielectric charging event is attributed to the demise of the ANIK [2] communications satellite in January 1994. It is a potential failure mechanism of the JPL experiment box flown on the STRV-1b. Deep dielectric charging was studied in the IDM (Internal Discharge Monitor) which flew on the CRRES (Combined Release and Radiation Effects Satellite) in 1990 [3]. In this experiment a number of dielectrics were placed under test and the build-up of charge was observed as pulses. The dielectrics consisted of electrical cables, printed wiring boards and Teflon and Solithane insulators. By far the largest number of discharges occurred in the PWBs composed of epoxy fiberglass.

OBJECTIVE: To measure the space radiation dose and deep dielectric charging behind different shields at six locations on SAMMES using p-FET dosimeters and surface mount capacitor arrays. It was required that these devices be measured by the same electronics used to measure the actinometers found in the other experiments included on SAMMES.

APPROACH: This experiment consists of two types of packages designated the FET variant and the CAP variant. The description of the FET variant is found in Figs. 1 to 4 and the CAP variant is described in Figs. 5 to 8. In this experiment, four FET variants and two CAP variants will be flown. The lid for the FET experiment, shown in Fig. 2, has holes over each FET. Different shields are placed over these holes as discussed later. Likewise, the lid for the CAP experiment, shown in Fig. 6, has a large square hole to allow a maximum of radiation exposure for one of the CAP experiments. The other CAP experiment has a thick shield.

PACKAGE FABRICATION: The 16-pin platform package is shown in Fig. 1 and the part number is listed in Table 1. Values for the resistors and capacitors are listed in Table 2. The package was modified by drilling two holes spaced 0.72 inch (1.8 cm) apart and tapped for a 2-56 mounting screw. The mounting screws serve two purposes: (a) to secure the devices to the spacecraft and (b) to electrically ground the package. An additional vent hole was drilled in the package to ensure that the shields experience no pressure differential during launch. THIS MEANS THAT THE PACKAGES ARE NOT HERMETICALLY SEALED AND NEED TO BE STORED IN A CLEAN DRY ENVIRONMENT. THE PACKAGES AND LIDS HAVE A BLACK MARK IN THE VACINITY OF PIN PT+ TO ENSURE CORRECT INSERTION OF THE DEVICES IN THE SOCKETS. The packages are numbered on the reverse side of the package.

SUBSTRATE FABRICATION: The ceramic substrate for this experiment, shown in Figs. 1 and 5, is 25-mil (0.62-mm) thick Al_2O_3 and was designed using AutoCAD. The substrate was designed to clear both the two screw holes and the vent hole. The substrate consists of a top side and backside Au-metal layers connected by Au-vias through the ceramic. After each layer is screen printed, it is fired at 500°C for 1 hour. The ceramic was attached to the package using non-conductive epoxy which was cured at 150°C for 1 hour. The same ceramic substrate was used for both the FET and CAP experiments.

COMPONENT ASSEMBLY: Non-conductive epoxy was used to attach the PRT to the ceramic. Conductive epoxy was used to attach the FETs, resistors, and capacitors, and PRT leads to the ceramic substrate. The

epoxy was cured at 150°C for 1 hour. The leads of the package were wire bonded to the substrate pads using 1-mil (0.02 mm) Au wire.
SHIELD ASSEMBLY: The shields used in this experiment are aluminized mylar, aluminum sheet, and tantalum sheet. The thicknesses are listed in Table 3 and the assignment to the FET and CAP variant packages is listed in Table 4. For the FET variant the shields were cut into 200 mil x 500 mil strips and attached to the outside of the lids with J. B. Weld epoxy and cured at 150°C for 1 hour. For the CAP variant the Al-mylar shield was attached to the inside of the package and the 1-mm shield was attached to the outside of the package. The clearance between the top of the FETs and the underside of the shield is about 120 mils (3.0 mm). The 0.13-mm aluminum shield has the same equivalent density thickness as a typical solar-cell cover glass.

FET PACKAGE: The FET variant package layout, shown in Fig. 1, indicates that the experiment consists of three p-FETs, F2, F1, and F3 and a positive resistance thermometer, PRT, noted as PT. The electrical schematic, shown in Fig. 2, indicates that the FET is connected in a Whetstone bridge circuit and surrounded by resistors, R1 and R2. This means that the FET is unbiased except for the short time that it is being tested. This is an important consideration for it is well known that FET radiation sensitivity is bias dependent. The measurement circuitry is shown in Fig. 4 and shows that the voltage across the bridge is connected to a log amplifier and then to a 12-bit ADC. During space measurements, Vref = 10 V so the FET current is about 100 μA which means that the FETs operate at their temperature independent point.

CAP PACKAGE: The CAP variant package layout, shown in Fig. 5, indicates that the package contains one FET, F2, two capacitors, C1 and C3, and one resistance thermometer, PT. The electrical schematic, shown in Fig. 7, indicates that the charging and discharging current through the capacitor is measured from the voltage drop across R3 when C1 is measured and R4 when C3 is measured. Notice that the capacitor experiment has a bleeder resistor, R3 = 1 MΩ, across the circuit to prevent the unbounded build-up of charge which might damage the measurement circuit. The measurement circuitry is shown in Fig. 8.

The measurement goal was to have a 1 second time constant for each capacitor circuit. Two commonly available capacitor types were chosen, X7R and NPO, and the largest available capacitor values were used. For the X7R, ten 0.1-μF capacitors are connected in parallel and this combination placed in series with a 1 MΩ resistor. For the NPO, four 1-nF capacitors are connected in parallel and placed in series with a 250 MΩ resistor. Results of measurements, discussed below, are given in Table 6.

p-FET CHIP DESIGN AND MEASUREMENT: The p-FET chip used in this experiment is shown in Fig. 9. The chip was fabricated through MOSIS at Hewlett-Packard, Corvallis, OR in 1.2-μm n-well CMOS. The six chips were arranged in a 2x3 array and separated using a diamond saw. The MOSIS run number is N61X which had a gate oxide thickness of 20.9 nm. In this FET the source is internally connected to the n-well and the drain internally connected to the gate. Two p-FETs are fabricated on chip to provide redundancy in case one FET fails. The FETs were epoxied to the ceramic substrate with conducting epoxy. Wire bonds connect SW to V+ and DG and B to IR.

Typical current-voltage characteristics for the FET's, shown in Fig. 10, indicate that the FET-to-FET variation is very small. This is important for it allows batch radiation and temperature calibration of the devices. The FET threshold voltage values, shown in Table 5, again confirms that the FET-to-FET threshold voltage variation is very small.

The meaning of the comments in Tables 5 and 6 are: TEMP is temperature measurement, E-RAD is electron irradiation, FLT is flight, FLT SPARE is flight spare, and HOLE is a device where the ceramic is covering the vent hole.

The current voltage characteristics for the FET, shown in Fig. 10, was determined using a circuit similar to the circuit shown in Fig. 4. The FET drain current is:

$$ID(\mu A) = 10 \cdot [Vref(V) - V+(V)] \quad (1)$$

where Vref and V+ are shown in Fig. 4. In this calculation the voltage drop across R5 was ignored for it introduced less than a 3 percent error. The threshold voltage, VT, was determined from a least squares fit to the FET square law relation:

$$ID = (\beta/2)(V+ - VT)^2 \quad (2)$$

where β is the FET transconductance. As seen in Fig 10, the IV points are well approximated by the square law equation.

p-FET OPERATING CURRENT: Most semiconductor sensors have a significant temperature dependence. The p-FET dosimeters are not exception to this rule. Fortunately, the temperature effects in the p-FET can be canceled by operating it at its temperature independent operating point. Temperature curves, shown in Fig. 11, indicate that the temperature effects on the IV characteristics cancel for an operating current of ID_O = 100 μA.

The measurement of ID_O follows by measuring the following parameters [4]. The temperature dependence of the threshold voltage was determined from:

$$VT = VT_O + VT_T(T - T_O) \quad (3)$$

where VT_T is the threshold temperature coefficient and T is the absolute temperature. The temperature dependence of β was determined from

$$\beta = \beta_O(T/T_O)^{-n} \quad (4)$$

where n is the channel mobility temperature coefficient. The β temperature coefficient is determined from

$$\beta_{TO} = -n\beta_O/T_O \quad (5)$$

The temperature-independent drain current was calculated from

$$ID_O = 2\beta_O^3(-VT_T/\beta_{TO})^2 \quad (6)$$

The temperature parameters and ID_O values for the three p-FETs in package SA10 are listed in Table 7. The results show that a choice of ID_O = 100 μA is a good one. This will reduce the temperature effects and allow the dosimetry effects to dominate the response. To obtain ID_O = 100 μA, R1 = 100 kΩ given that Vref = 10 V.

DIFFERENTIAL FET OPERATION: The differential characteristics for the FET, shown in Fig. 12, reveal the nonlinear behavior of the FET leg of the bridge circuit and the linear behavior of the resistor leg. In developing the bridge circuit, R2 was chosen so that V+ is slightly more positive than V-. As seen in Fig. 12, V+ - V- is about 74 mV. THE EXACT VALUES NEED TO BE DETERMINED FROM PRE-FLIGHT GROUND TESTS.

PRT MEASUREMENTS: For the resistance thermometer the current was determined from:

$$I(\mu A) = 50\cdot[Vref(V) - V+(V)] \quad (7)$$

where R5 = 20 kΩ was used. The resistance was determined from a least square fit to the slope of the IV data. A typical example is shown in Fig. 13. In the future the value of this resistor should be reduced to 5 kΩ to improve the accuracy of the current measurement.

CAP MEASUREMENTS: The capacitance circuit was measured by varying Vref as shown in Fig. 14. The voltage, Vref, was allowed a delay of about 5 sec before each transition. The voltage was measured using a National Instruments DAQPad-1200. The ADC has an input impedance of 1 MΩ but the sampling time is less than 10 μs which has a negligible effect on the measurement. The response for the capacitors C1 (X7R) and for C3 (NPO) are shown in Fig. 15. As expected the capacitors have approximately the same time response of about 1 second. The capacitor response is measured at V- as seen in Fig. 8. The rising response, V_r, across the capacitor is

$$V_r = V_{r\infty}(1-\exp(t/\tau_r) \quad (8)$$

where τ_r is rising time constant and $V_{r\infty}$ is the voltage at the end of the delay cycle. The rising time constant was calculated from a least squares fit to:

$$t = -\tau_r \ln(1 - V_r/V_{r\infty}) \quad (9)$$

where the log time response is shown in Fig. 16. For the falling response, V_f, is given by

$$V_f = V_{fo}\cdot\exp(-t/\tau_f) \quad (10)$$

where τ_f is the falling time constant and V_{fo} is the initial voltage. The falling time constant was calculated from a least squares fit to:

$$t = \tau_f\cdot\ln(V_{fo}/V_f) \quad (11)$$

where the log time response is shown in Fig. 16. The rise and fall time constants are listed in Table 6.

The temperature dependence of the ceramic surface mount capacitors is shown in Fig. 17. As expected [5] the X7R can have a +/- 15% change between -55 to 125°C; whereas, the NPO has a +/- 15 ppm/°C temperature coefficient. Thus, the X7R has a much larger temperature dependence than the NPO capacitor. The failure of the NPO to pull up to the rail is not understood. It indicates that the capacitor has started to leak. This same behavior has been observed in one other NPO capacitor so the effect appears to be real.

ELECTRON RADIATION CALIBRATION: The electron radiation test results are shown in Fig. 18. The tests were conducted at the JPL Dynamatron facility by Dr. Bruce Anspaugh. The electron irradiation was conducted using a 1-MeV electron beam that had an 8-inch (20-cm) diameter. The dose rate was 10 rads/sec. The devices were irradiated at room temperature in a vacuum of 1E-5 torr.

The results show the effect of the shields in reducing the dose received by the p-FETs. This data was fitted with an algorithm developed for the ICM1 dosimeters [6]. The algorithm is based on radiation-induced filling of p-FET gate-oxide traps and the generation of oxide-silicon interface states. The expression for the p-FET output voltage at room temperature is:

$$VO = |VT_O| + \Delta VT[1 - \exp(-D/D_V)] + (VO_O - |VT_O|)\cdot\sqrt{(1 + D/D_b)} \qquad (12)$$

where VT_O is the initial threshold voltage, ΔVT is the trap filling voltage, D_V is VT dose coefficient, β_O is the initial transconductance, and D_b is the β dose coefficient. When operated at the temperature-independent current, ID_O:

$$\sqrt{[2\cdot ID_O/\beta_O]} = VO_O - |VT_O| \qquad (13)$$

where VO_O is the preradiation value for VO. The fitting parameters are listed in Table 8.

This data was further analyzed after realizing that the FET response behind the 2-mm aluminum should have been zero for this shield is thicker than the 1.46 mm range of a 1-MeV electron beam in aluminum [7]. The range and linear energy transfer (LET) for various energies of electrons in aluminum are shown in Fig. 19. Thus, the background dose was subtracted from the p-FET shielded by the Al-mylar and the 0.25-mm Al-shield. The results are listed in Table 9. The results indicate that interface-state generation is a weak effect in that D_b is large being near 3 Mrad. The DVT is approximately the same which indicates that each FET has the same number of traps. The D_V is larger for pFET1 since it is more heavily shielded than PFET2.

The initial dose rate follows from Eq. 12 for $D_b = \infty$ and is:

$$dVO/dD|_{D=0} = \Delta VT/D_V \qquad (14)$$

The dose rate is listed in Table 9. The value for PFET2 is 4.7 mV/krad which agrees with the initial slope of 4.7 mV/krad for the Co-60 results shown in Fig. 8 of Ref. 2. The dose rate for PFET1 at 2.3 mV/krad, is too low for a 0.25-mm Al shield. It should be closer to 4.0 mV/krad according to the dose-depth curve shown in Fig. 11.3 of Ref. 8.

The capacitors did not respond to the electron irradiation. Thus, they will serve as reference circuits which should not change in space. However, the capacitors have not been irradiated with protons which may cause some change to the charging and discharging characteristics.

DISCUSSION: This experiment will develop the data to aid in developing design curves for spacecraft shielding against total dose. However, more ground tests are needed using electron irradiation to confirm the dose depth curves calculated previously [8]. The dose seen by the 0.25-mm shielded pFET is too low by almost a factor of two.

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Table 1. SAMMES Dosimeter Parts List.

ITEM	DIMENSIONS	MANUFACTURER	P/N
PRT: 0.39Ω/°C	2mm x 2.3mm	OMEGA	F3105
Package: 16-pin Au-Plated Kovar Platform	795 mil x 970 mil (20.2 x 24.6 mm)	AIRPAC Manuf: HES Intern.	ADI-16D-0006
Lid: Ni-Plated Cold Rolled Steel	795 mil x 970 mil x 10 mil (20.2 x 24.6 x 0.25mm)	AIRPAC Manuf: A. T. Wall	ADC-16D-0001
SMR: 16.9 kΩ 1% Metal Film	120 mil x 60 mil	Panasonic	ERJ 6ENF 1692
SMR: 100 kΩ 1% Metal Film	80 mil x 50 mil (2.0 x 1.3 nm)	Panasonic	ERJ 6ENF 1003
SMR: 1 MΩ 1% Metal Film	120 mil x 60 mil (3.0 x 1.5 mm)	Panasonic	ERJ 6ENF 1004
SMR: 250 MΩ 1% Metal Film	250 mil x 250 mil (6.4 x 6.4 mm)	Victoreen	MC101822506F
SMC: 0.1 µF XR7	80 mil x 50 mil (2.0 x 1.3 mm)	Panasonic	ECU-V1H102JCX
SMC: 1 nF NPO	120 mil x 60 mil (17.8 x 20.3 mm)	Panasonic	ECU-V1H104KBW
p-FET Chip: CMOS	2.2 mm x 2.2 mm	Hewlett Packard	1.2-µm CMOS
Ceramic Substrate: Al2O3	700 mil x 800 mil (17.8 x 20.3 mm)	Halcyon	custom

Table 2. R and C Values

COMPONENT	VALUE	UNITS
R1	100	kΩ
R2	16.9	kΩ
R3	1	MΩ
R4	250	MΩ
C1	0.1	µF
C1Total	1	µF
C3	1	nF
C3Total	4	nF

Table 3. SAMMES Dosimeters Radiation Shields.

Material	DENSITY g/cc	ALDRICH P/N	mm	mil	Al equiv.
Al-Mylar					1.00
Al	2.7	35,685-9	0.05	1.97	1.97
Al	2.7	32,686-0	0.13	5.12	5.12
Al	2.7	22,685-2	0.25	9.84	9.84
Al	2.7	26,657-4	0.5	19.69	19.69
Al	2.7	26,695-7	1	39.37	39.37
Al	2.7	26,659-0	2	78.74	78.74
Ta	16.6	35,724-3	0.05	1.97	12.10
Ta	16.6	26,289-7	0.25	9.84	60.51
Ta	16.6	35,725-1	0.5	19.69	121.03
Ta	16.6	26,288-9	1	39.37	242.05

Table 4. SAMMES Radiation Shield Matrix

UNIT	LOC	VARIANT	SHIELD
1	2	FET	1.00-mil Al (0.0254 mm)
	1	FET	9.84-mil Al (0.250 mm)
	3	FET	78.74-mil Al (2.000 mm)
2	2	FET	1.97-mil Al (0.0504 mm)
	1	FET	19.68-mil Al (0.5000 mm)
	3	FET	39.37-mil Ta (1.000 mm)
3	2	FET	1.97-mil Ta (0.050 mm)
	1	FET	9.84-mil Ta (0.0250 mm)
	3	FET	39.37-mil Ta (1.000 mm)
4	2	FET	5.12-mil Al (0.130 mm)
	1	FET	39.37-mil Al (1.000 mm)
	3	FET	19.68-mil Ta (0.5000 mm)
5	2	FET	1.00-mil Al (0.0254 mm)
	1	CAP(X7R)	1.00-mil Al (0.0254 mm)
	3	CAP(NPO)	1.00-mil Al (0.0254 mm)
6	2	FET	39.37-mil Al (1.000 mm)
	1	CAP(X7R)	39.37-mil Al (1.000 mm)
	3	CAP(NPO)	39.37-mil Al (1.000 mm)

Table 5. FET Variant Values

PACKAGE	UNIT	COMMENT	VT(F2) V	VT(F1) V	VT(F3) V	R(PT) Ω	
SA03	1		0.883	0.874	0.881	112.8	DAT6
SA04	1	E-RAD	0.875	0.872	0.875	109.7	
SA05	4	TEMP	0.874	0.880	0.871	112.8	DAT6
SA06	4		0.866	0.874	0.874	111.2	DAT5
SA07	4	FLT	0.880	0.878	0.878	108.8	DAT5
SA08	4		0.884	0.878	0.877	112.8	DAT5
SA09	4		0.873	0.876	0.876	293.9	DAT6
SA10	1	TEMP, FLT SPARE	0.873	0.877	0.870	106.5	DAT6
SA11		BAD	0.873	0.879	0.832	111.2	DAT6
SA12	1		0.881	0.877	0.867	108.3	DAT6
SA13	2	TEMP	0.879	0.870	0.873	106.4	DAT6
SA14		BAD	0.868	0.873	#NUM!	111.2	DAT6
SA15	1		0.879	0.867	0.873	111.2	DAT6
SA17	1		0.873	0.877	0.876	106.5	DAT6
SA18	1		0.881	0.878	0.871	110.7	DAT5
SA19	3	TEMP	0.883	0.880	0.870	112.7	DAT5
SA22	1		0.875	0.881	0.876	106.5	DAT6
SA23	1		0.871	0.870	0.869	111.2	DAT6
SA24	4		0.870	0.878	0.874	112.1	DAT5
SA25	1		0.876	0.878	0.874	108.3	DAT6
SA26		BAD	0.873	0.877	0.873	112.7	DAT5
SA27	1		0.876	0.876	0.881	133.3	DAT6
SA28	1	E-RAD	0.882	0.874	0.879	106.5	
SA29	4		0.872	0.875	0.869	106.4	DAT6
SA30	1	E-RAD	1.549	0.873	0.873	112.2	
SA32	4	HOLE	0.866	0.872	0.871	112.8	DAT6
SA34	3	FLT	0.873	0.869	0.884	112.8	DAT6
SA35	3	FLT SPARE	0.867	0.876	0.869	112.8	DAT6
SA36	2	FLT SPARE	0.878	0.873	0.871	112.8	DAT6
SA37	2	FLT	0.877	0.873	0.866	112.8	DAT6
SA38	1	HOLE	0.877	0.873	0.871	111.2	DAT6
SA39	1	FLT	0.877	0.872	0.875	112.8	DAT6
SA41	4	FLT SPARE	0.877	0.876	0.863	112.8	DAT6
SA42	1	E-RAD	0.877	0.873	0.879	108.4	

Table 6. CAP Variant Values

PACKAGE	UNIT	COMMENTS	VT(F2) V	R(PT) Ω	τ_r(C1) sec	τ_f(C1) sec	τ_r(C3) sec	τ_f(C3) sec	
SA43	6	FLT SPARE, HOLE	0.880	116.7	0.826	1.032	0.939	0.906	DAT6
SA44	5	E-RAD	----	----	----	----	-----	----	DAT6
SA45	6	FLT	0.874	111.2	0.866	1.024	0.944	0.906	DAT6
SA46	5	FLT	0.866	111.2	0.868	1.040	0.936	0.904	DAT6
SA47	5		0.874	111.2	0.842	0.987	0.953	0.922	DAT6
SA48	5	FLT SPARE	0.872	112.8	----	----	-----	----	DAT6
SA49	6	FET=?, HOLE	0.867	112.8	0.802	0.992	0.934	0.904	DAT6

Table 7. Temperature Parameters and Operating Current for SA10

SA10	UNITS	PFET2	PFET1	PFET3
W	μm	193.5	193.5	193.5
L	μm	9.6	9.6	9.6
T	K	300	300	300
VT_O	V	-0.875	-0.880	-0.870
VT_T	mV/°C	1.69	1.72	1.72
n	unitless	1.468	1.572	1.541
β_O	$\mu A/V^2$	494.6	491.9	489.7
KP_O	$\mu A/V^2$	24.5	24.4	24.3
β_{TO}	$\mu A/V^2{}^\circ C$	-2.42	-2.58	-2.52
ID_O	μA	117.9	106.2	110.0

Table 8. Electron Parameters for SA28 (with background)

PARAMETER	UNITS	PFET2	PFET1	PFET3
Al-shield	mm	0.025	0.25	2.00
VO_O	V	1.465	1.455	1.462
$\|VT_O\|$	V	0.882	0.874	0.879
$\sqrt{[2 \cdot ID_O/\beta_O]}$	V	0.583	0.581	0.583
ΔVT	mV	336	258	40
D_v	krad	60	81	67
D_b	krad	314	258	236
dVO_O/dD	mV/krad	6.6	43	1.8

Table 9. Electron Calibration Parameters for SA28 (Background removed)

PARAMETER	UNITS	PFET2	PFET1
Al-shield	mm	0.025	0.25
VO_O	V	1.465	1.455
$\|VT_O\|$	V	0.882	0.874
$\sqrt{[2 \cdot ID_O/\beta_O]}$	V	0.583	0.581
ΔVT	mV	238	176
D_v	krad	51	76
D_b	krad	2177	2840
dVO_O/dD	mV/krad	4.7	2.3

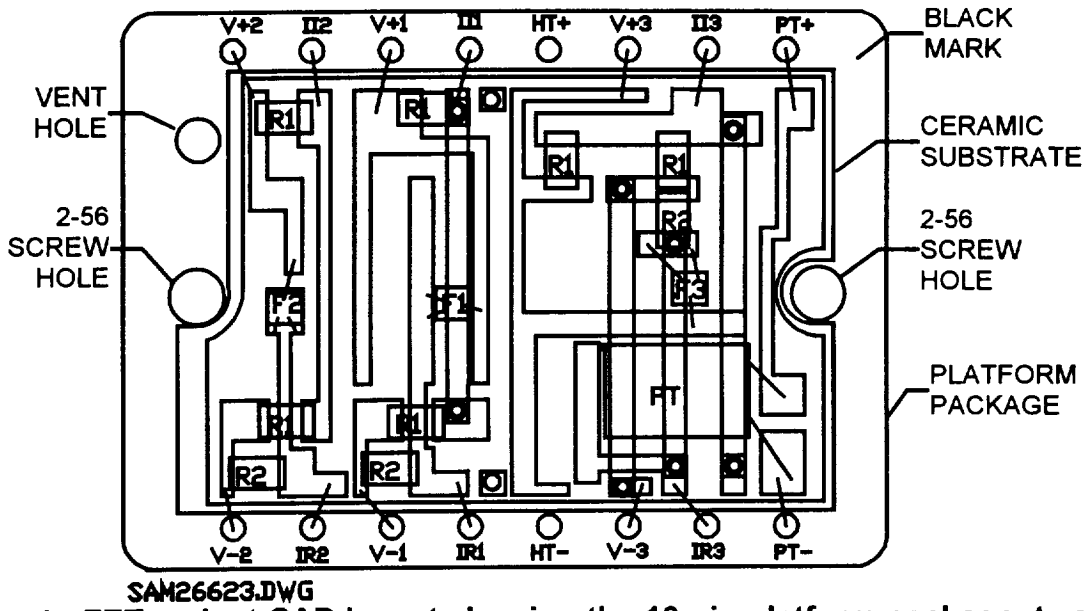

Figure 1. FET variant CAD layout showing the 16-pin platform package, two-layer co-fired ceramic substrate and components including the FETs, resistors, and PRT.

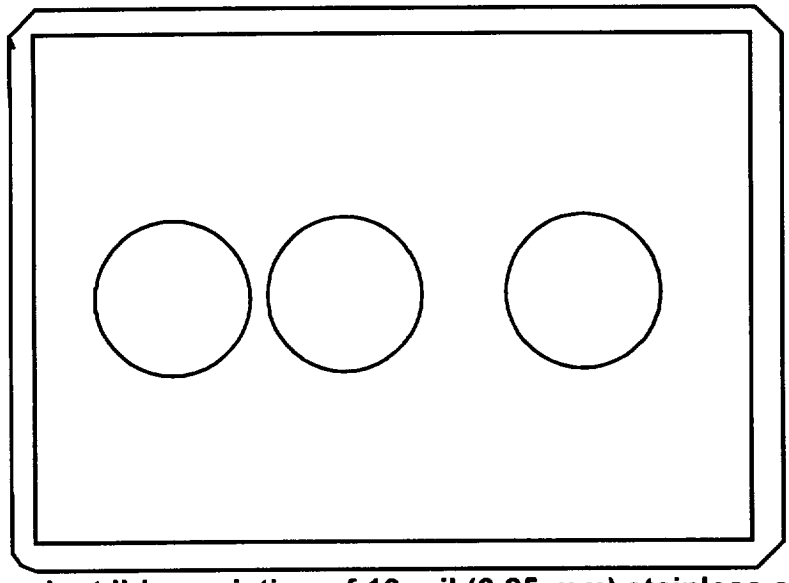

Figure 2. FET variant lid consisting of 10-mil (0.25-mm) stainless steel with 280-mil (7.1-mm) holes punched over the three FET locations.

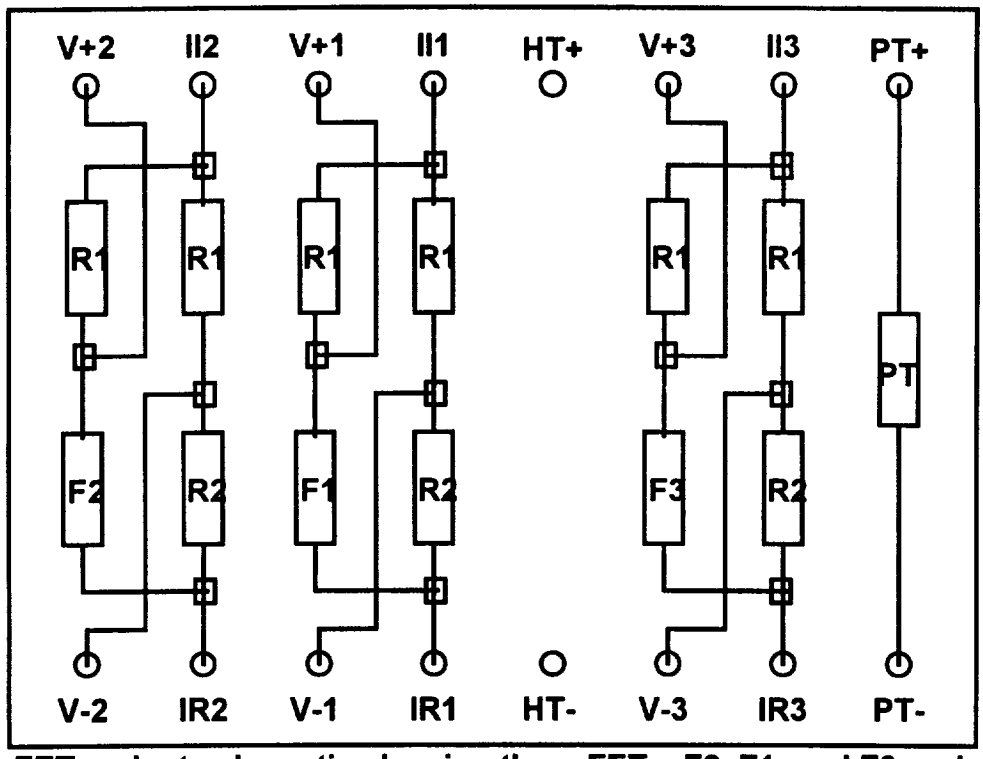

Figure 3. FET variant schematic showing three FETs, F2, F1, and F3 under test.

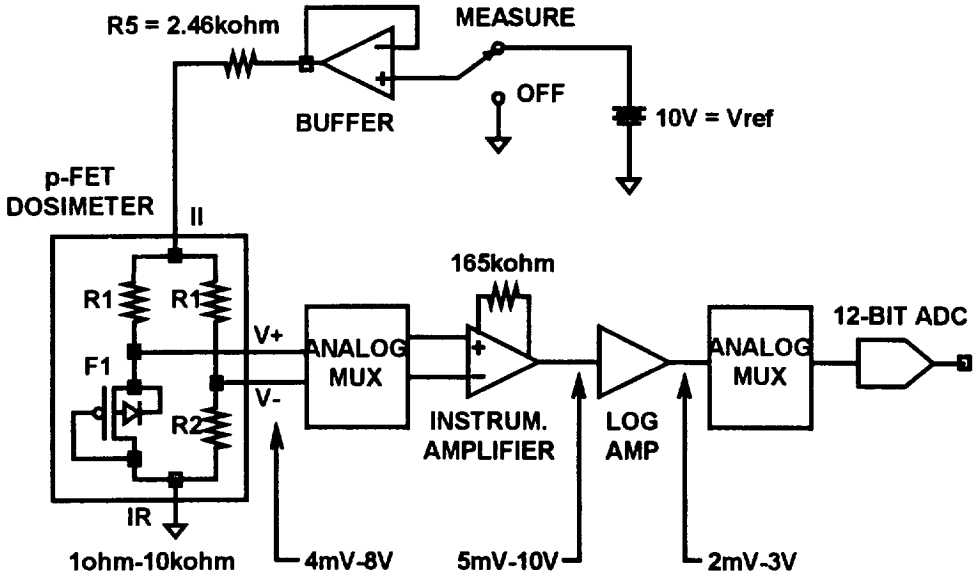

Figure 4. FET connected to the spacecraft measurement electronics showing the Whetstone bridge nature of the p-FET dosimeter.

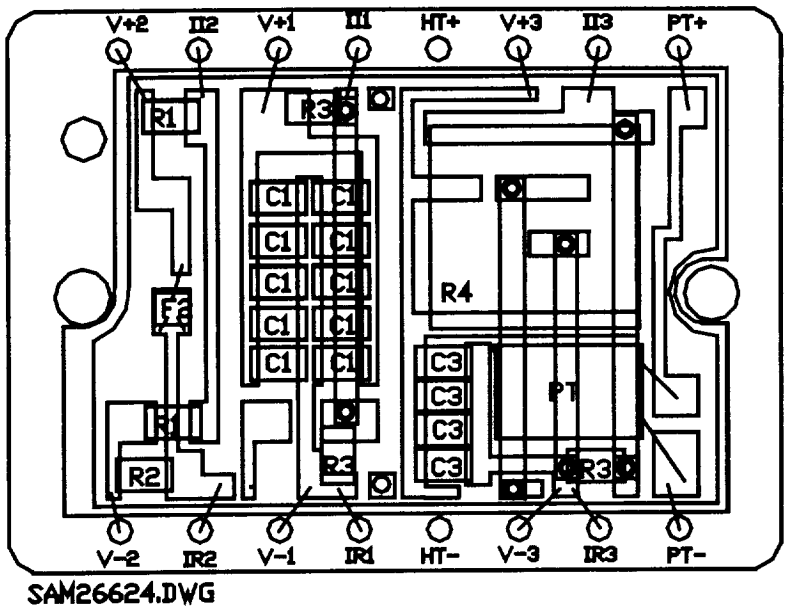

Figure 5. CAP variant CAD layout showing the platform package, the two-layer co-fired ceramic substrate, and the components including FETs, resistors, capacitors, and PRT.

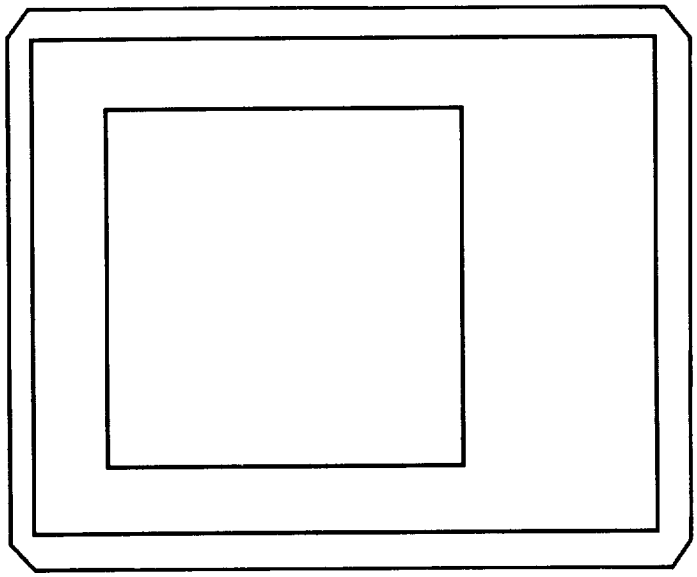

Figure 6. CAP variant lid consisting of 10-mil (0.25 mm) stainless steel with a 500-mil (125-mm) square hole.

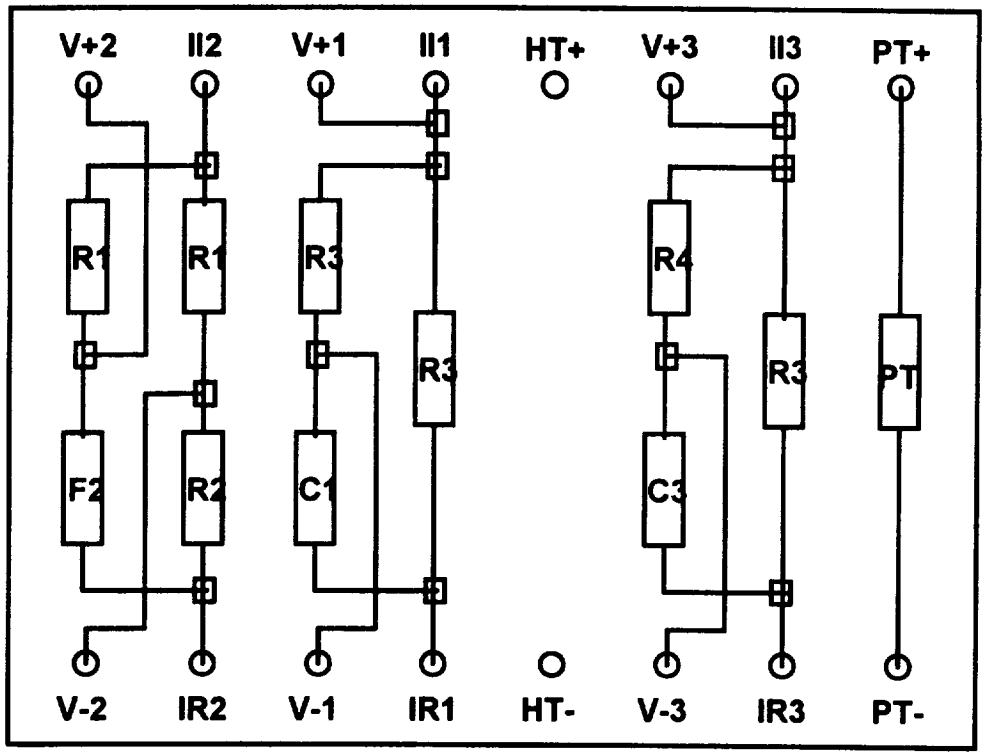

Figure 7. CAP variant schematic showing the FET and the two capacitors, C1 and C3.

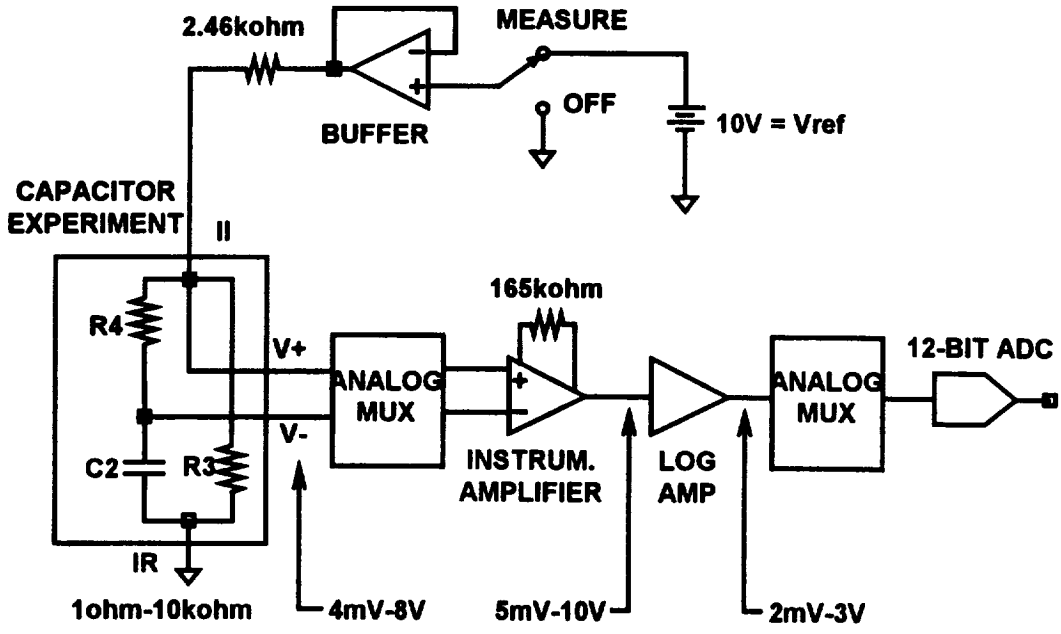

Figure 8. CAP connected to the spacecraft measurement electronics showing that the analog MUX is connected across resistor R4 which is in series with the test capacitor.

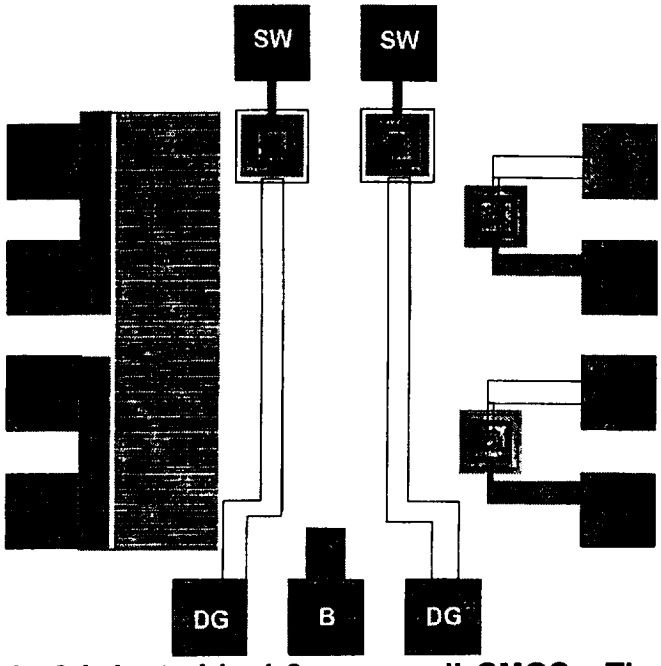

Figure 9. p-FET chip fabricated in 1.2-μm n-well CMOS. The chip contains two closed-geometry p-FETs plus a resistor and two n-FETs. Contacts to the p-FET are SW = p-Source/n-Well, DG = p-Drain/Gate, and B = Body contact to the p-substrate. The internal DG connection forces the device to operate in its saturation region and provides electrostatic discharge protection to the gate oxide.

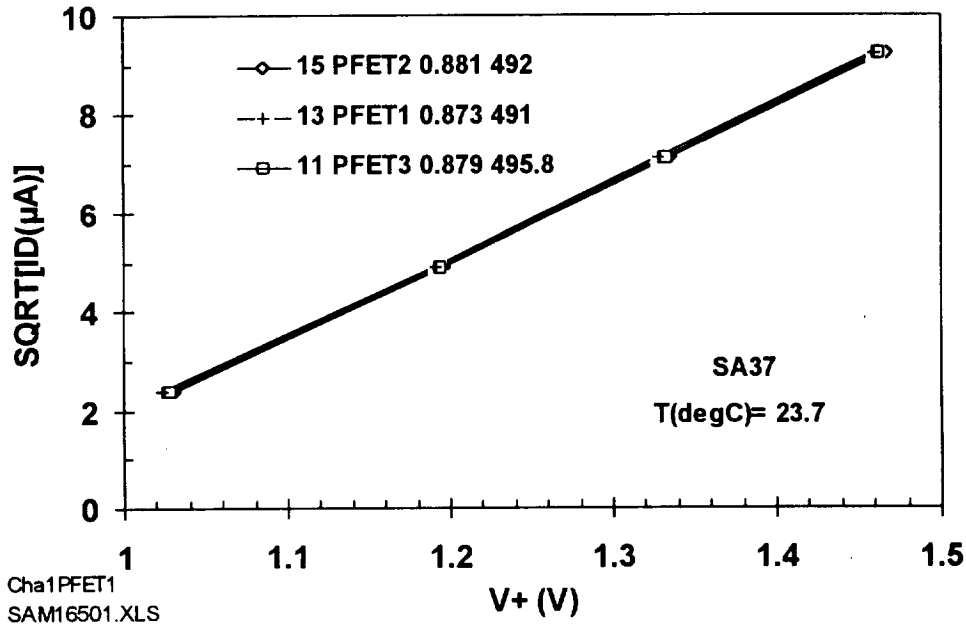

Figure 10. Typical IV characteristics for the p-FETs from FET variant showing that all three FET characteristics overlap. The key lists VT in Volts and β in $\mu A/V^2$ for three FETs.

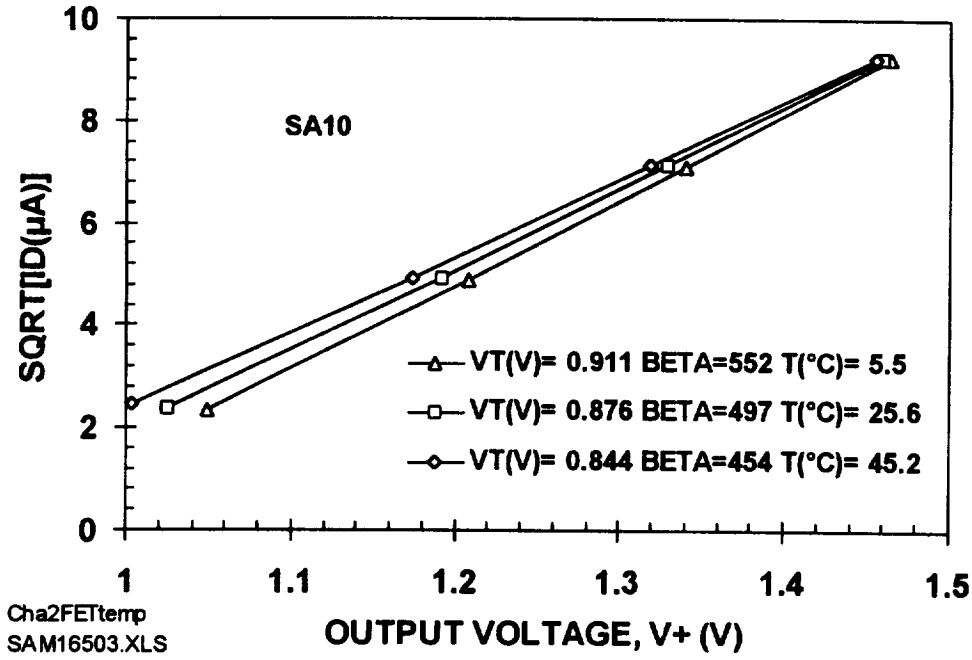

Figure 11. Temperature dependence of p-FET F2 in SA10. The key lists VT in Volts and β in μA/V^2 at three temperatures.

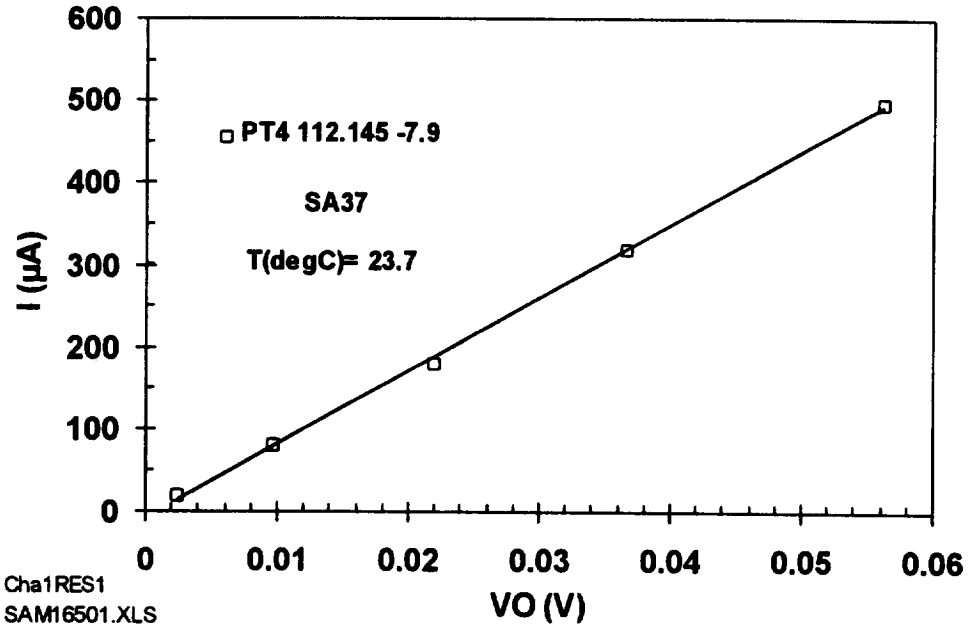

Figure 12. Typical IV characteristics for the PRT. The key lists the resistance in ohms and the offset current in μA.

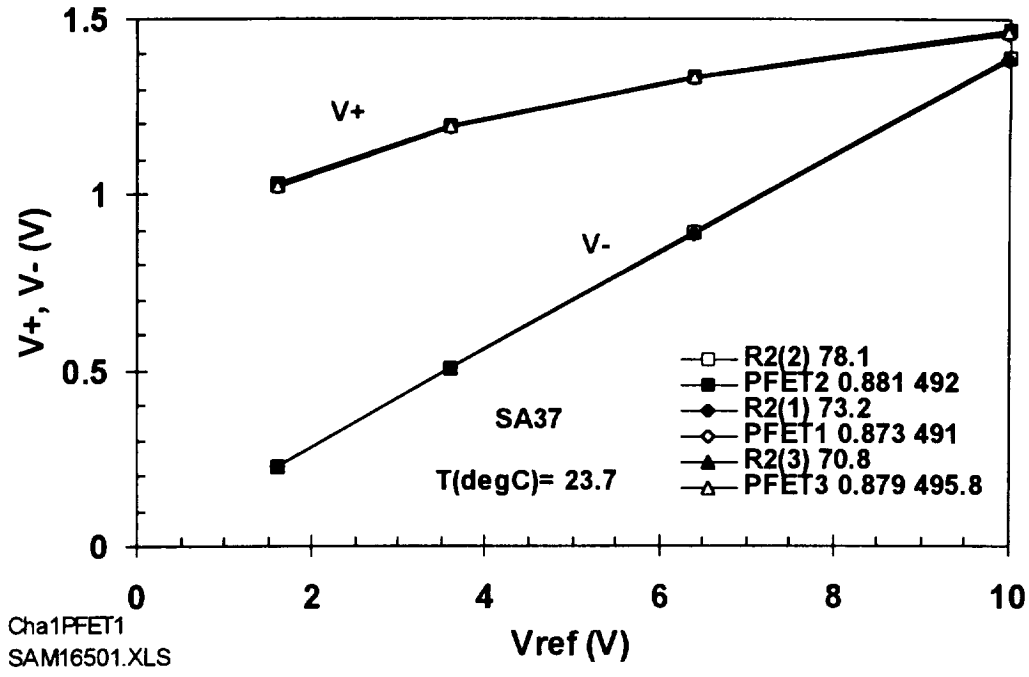

Figure 13. Operational mode for the p-FETs is at Vref = 10 V. On the PFET line VT has units of Volts and β μA/V^2 and on the R2 line V+ - V- has units of mV.

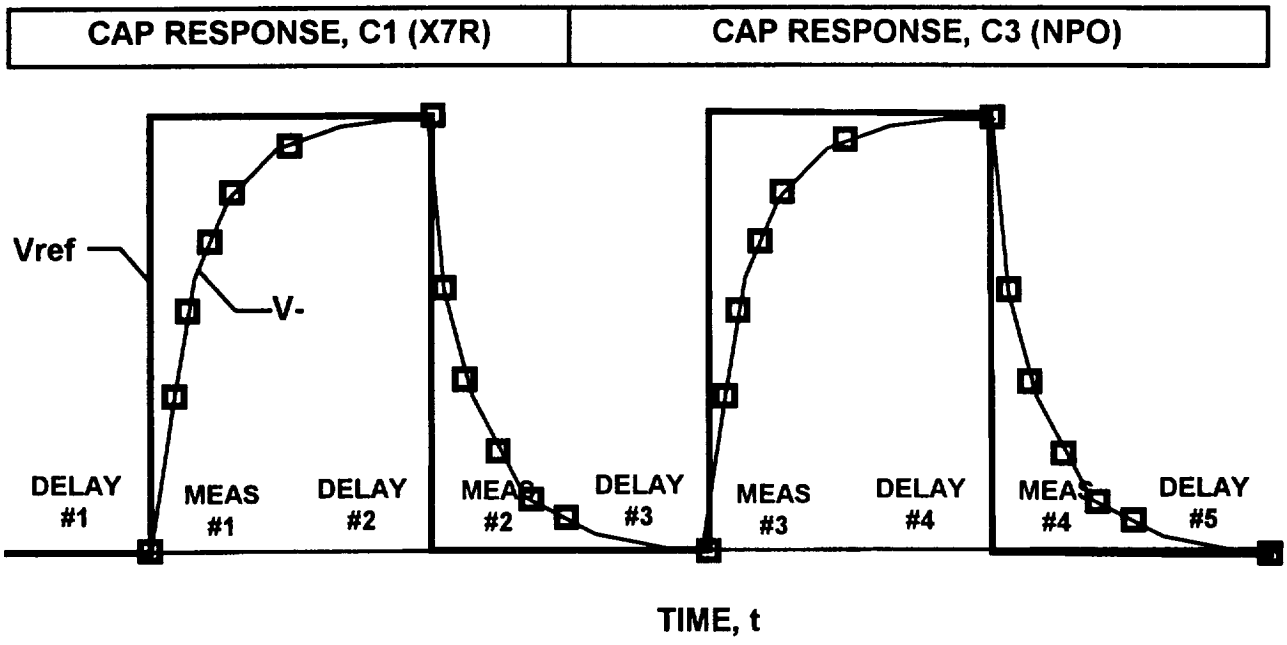

Figure 14. Capacitor experiment voltage profile for Vref and V-. The delay times are about 5 seconds and data points are acquired about every second.

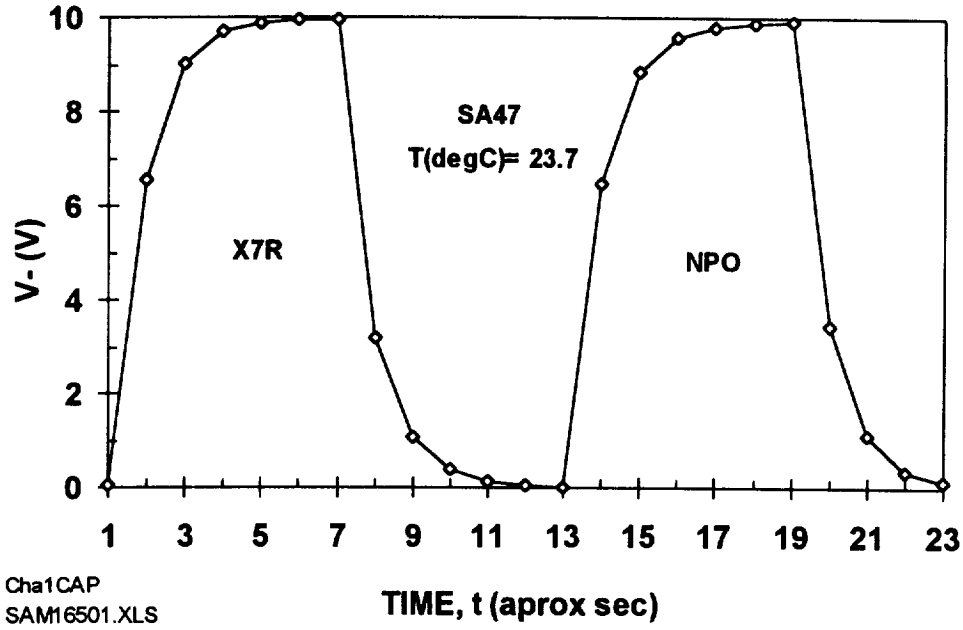

Figure 15. Typical capacitor transient characteristics for the CAP variant. Note that this is an Excel line chart where the 5-second delay times are compressed to one second.

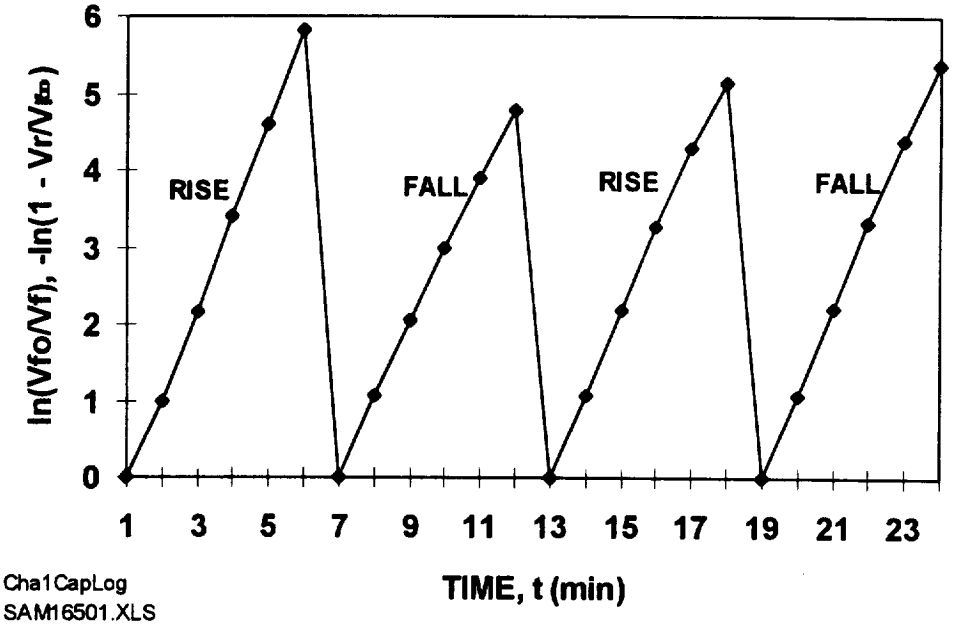

Figure 16. Logarithmic presentation of the data shown in Fig. 15

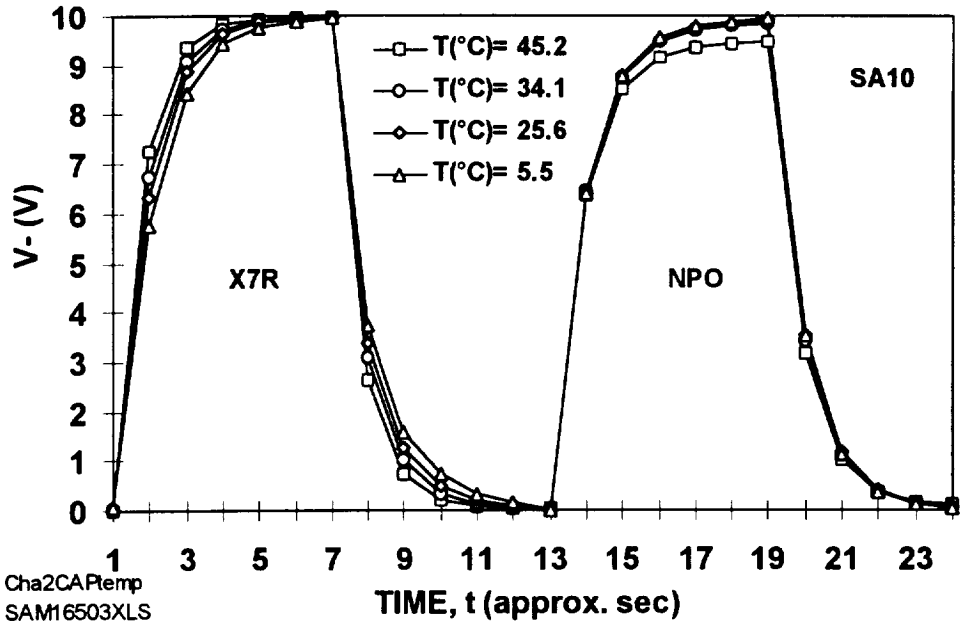

Figure 17. Temperature dependence of the two capacitors in the CAP variant. As expected the X7R showed a larger temperature dependence than the NPO. Note that the NPO failed to pull-up at the highest temperature of 45.2°C.

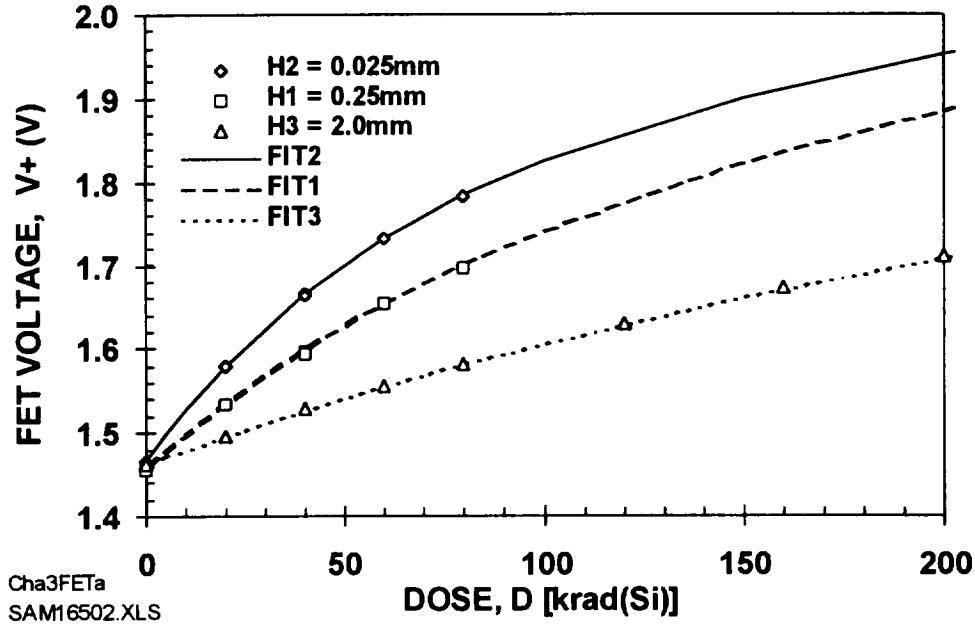

Figure 18. Radiation response from the three FETs in package SA28 with a Unit 1 type shield to 1.0 MeV electron beam at a dose rate of 10 rads/sec.

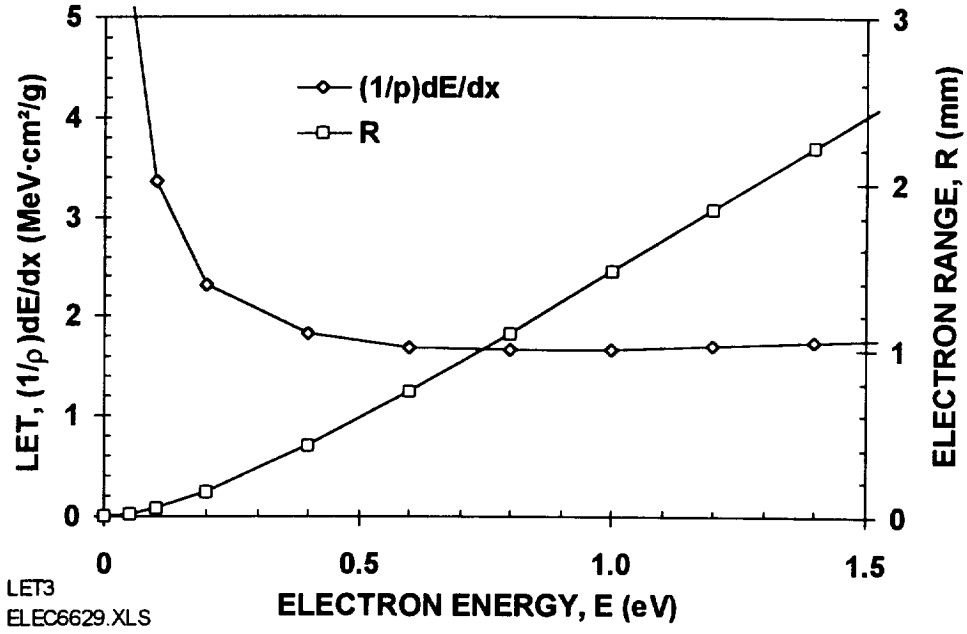

Figure 19. Electron range and LET in aluminum.

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Stacked p-FET Dosimeter for the STRV-2 MWIR Detector

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Abstract

A stacked p-FET dosimeter consisting of a RADMON mother chip with three p-FETs and multiplexer and an attached RADFET has been developed for the STRV-2/MWIR detector. Calibration of the dosimeter, using an Am-241 source, indicates that the RADFET is about 20 times more sensitive to radiation than the RADMON. This dosimeter is expected to measure radiation dose from rads to Megarads.

I. INTRODUCTION

This dosimeter has four p-FETs for monitoring the radiation dose inside the Space Technology Research Vehicle (STRV-2) Medium-Wavelength Infrared (MWIR) detector electronics box to be launched in 1998. The three year mission dose for a 450 km by 1600 km orbit behind 2.5-mm Al shield is estimated to be 10 krads. The dosimeter, seen in Fig. 1, consists of a thin-oxide RADMON mother chip [1] with three p-FETs, multiplexer, and other devices. A thick-oxide RADFET [2, 3, 4] is attached to the mother chip. The device operates on the principle that radiation passing through the gate oxide region of the p-FET creates hole-electron pairs. Since the oxides have mainly hole traps, radiation-induced positive charge is trapped in the oxide. This build-up of positive charge changes the threshold voltage of the device which is interpreted in terms of radiation dose.

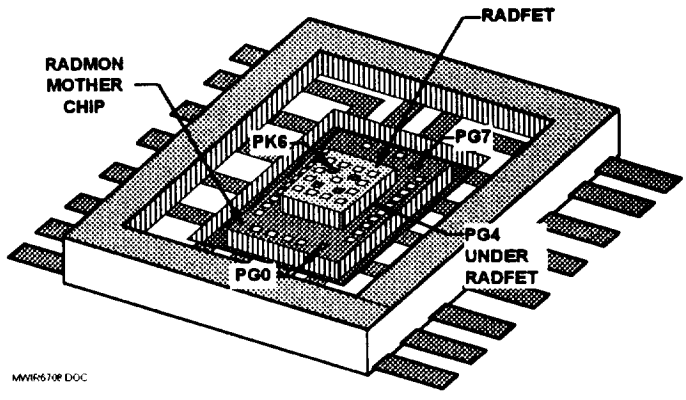

Figure 1. RADFET mounted on the RADMON mother chip in a 16-pin flat package. Three radiation sensitivities are achieved: PK6 has highest sensitivity, PG0 and PG7 have moderate sensitivity, and PG4 has lowest sensitivity being shielded by the RADFET.

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Since the RADFET is about 20 times more sensitive to radiation than the RADMON, this dosimeter can measure both low and high doses. The objective of this effort is to develop a stacked p-FET dosimeter for the STRV-2/MWIR detector and to calibrate the dosimeter using a low-cost bench-top radiation ^{241}Am source.

II. CHIP FABRICATION

The mother chip, shown in Fig. 2, was fabricated using the Hewlett-Packard 1.2-μm n-well CMOS process. The chip consists of an 8-bit multiplexer (MUX) that addresses four p-FETs (PG0, PG4, PK6, PG7), two n-FETs (NG1 and NF3), a resistor (RM2), and a user selected device (RX5) which can be the on-chip diode (DP5).

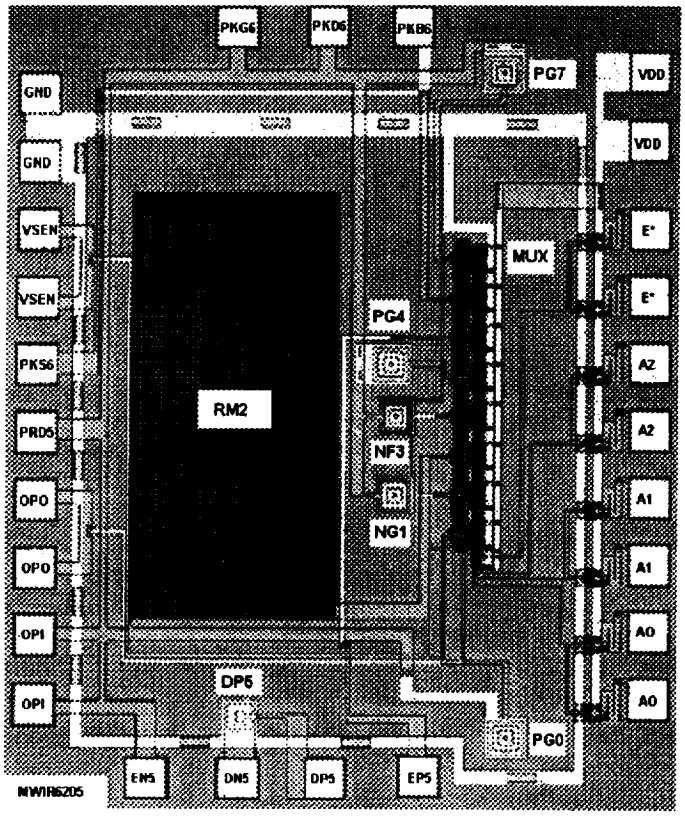

Figure 2. RADMON mother chip 1.8 mm x 2.2 mm fabricated in 1.2-μm n-well CMOS.

The RADMON p-FETs are closed geometry devices where the drain-gate is surrounded by the source-body. The FETs are covered with a metal-2 light shield. The RADFET p-FET has a comb structure. The critical dimensions of these devices are listed in Table 1.

Table 1. Critical Device Dimensions

NO.	DEVICE	LAYER	W μm	L μm	X_o nm
PG0	p-FET	Poly Gox	193.5	9.6	20
NG1	n-FET	Poly Gox	193.5	9.6	20
RM2	Resistor	Metal-1	2.4	24214	NA
NF3	n-FET	Metal Fox	193.5	9.6	500
PG4	p-FET	Poly Gox	193.5	9.5	20
RX5	Resistor	External	NA	NA	NA
PK6	p-RADFET	Metal Gox	500	10	250
PG7	p-FET	Poly Gox	193.5	9.6	20

The untested RADMON chips were mounted in the 16-pin flat pack using Ag epoxy as shown in Fig. 3. The three p-FETs on the mother chip are indicated in the figure. The RADFET was attached to the mother chip as shown in Fig. 1 with non-conductive epoxy in such a manner that PG0 and PG7 are not covered and PG4 is covered by the RADFET.

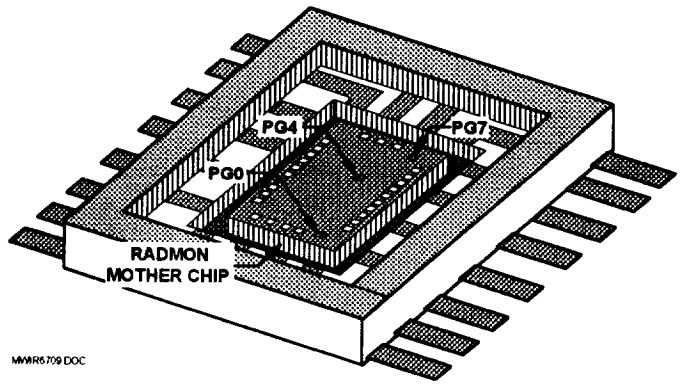

Figure 3. RADMON mother chip mounted in a 16-pin flat package. Three p-FETs are located on the RADMON.

The RADFET was fabricated using a thick oxide process at Southampton University Microelectronics Centre so it has a high radiation sensitivity [2, 3]. The RADFET is 0.5-mm thick and provides some radiation shielding for devices MUX, NG1, NF3, and PG4 found on the mother chip. The RADFET consists of four p-FETs: two are very radiation sensitive Type R and two are the less radiation sensitive Type K. For the purposes here only one Type K is used.

Because the RADFET height exceeded the package height, an Al_2O_3 spacer was epoxied to the package. Grounding of the mylar lid, the Au ring, and the Au platform is provided by the Au wire bonds as shown in Fig. 4. A cross section view, shown in Fig. 5, provides additional detail. The grounding process is extremely important for any floating electrode can charge in a radiation field and discharge damaging or destroying the dosimeter.

The package has a 25-μm thick aluminized mylar lid as seen in Fig. 6. This lid was chosen to minimize the radiation shielding since this dosimeter will be located in an electronics box and will receive about 3.3 krads/year. The packages were burned-in at 168 hrs at 125°C and centrifuged at 5000 g's.

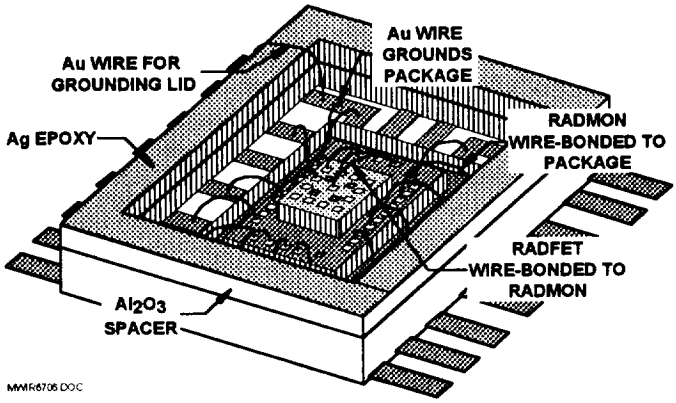

Figure 4. Au-wire bonds ground all portions of the package to prevent charge build-up.

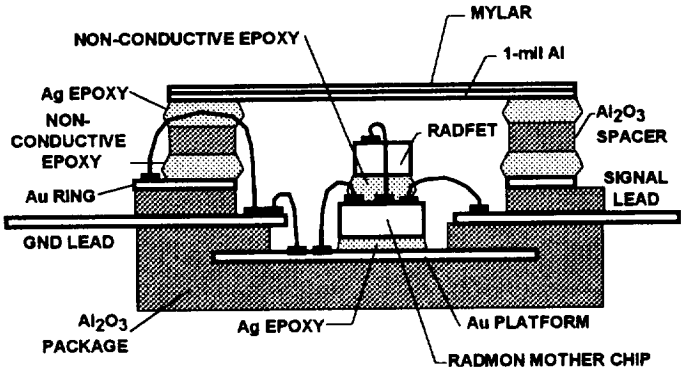

Figure 5. Cross section of the MWIR Dosimeter package showing the wire bonds that ground the Au ring and aluminum-coated mylar lid.

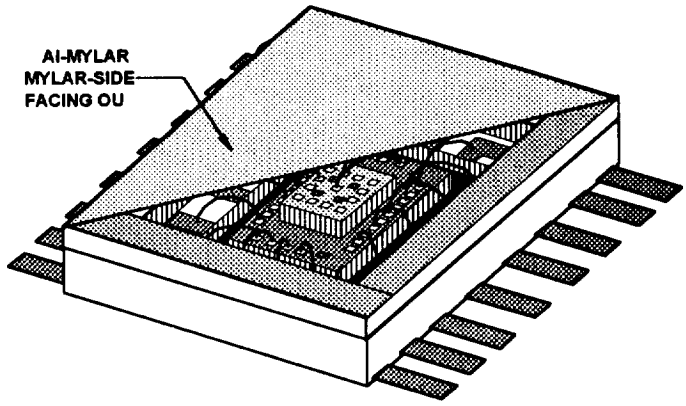

Figure 6. Cut-away view of the Al-mylar lid used to protect the chip and wire bonds from mechanical damage during board assembly. The Al side is turned toward the package so that it is grounded.

The electrical equivalent circuit for the chip is shown in Fig. 7, where the six on-chip devices are accessed through a 3-8 decoder multiplexer (MUX). The chip is connected to surround circuitry where the devices are connected between the input, OPI, and output, OPO, of an Op Amp. During measurement, current is forced through each device.

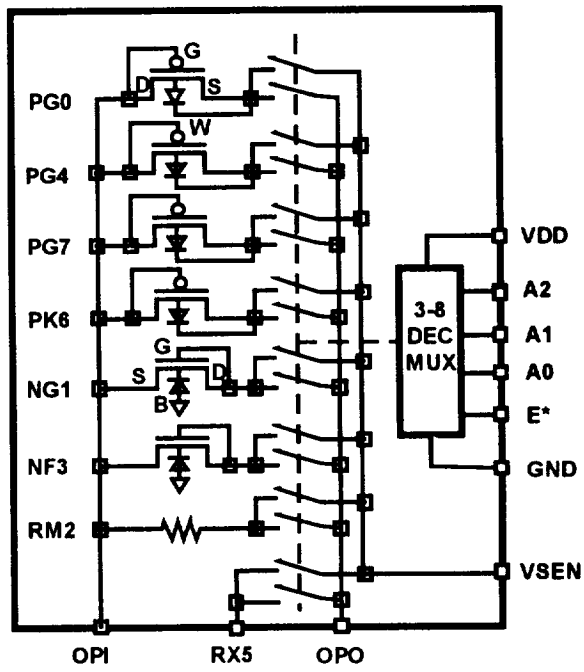

Figure 7. Chip can address eight devices which are measured by an Op Amp connected between OPI and OPO.

The switches in the MUX are operated in pairs. One switch passes the measurement current and the other switch is connected to an Op Amp that senses the potential, V_{sen}, at the device.

The bias voltage for these devices is only applied during measurement. During irradiation the device is not powered and all leads are grounded. In operation as seen in Fig. 7, the voltage on the gate in the off mode, is the voltage across the n-well at the source of the p-FET. Leakage currents through the n-well junction keep this node at zero bias.

III. THRESHOLD VOLTAGE DISTRIBUTIONS

Integral to the dosimetry process is batch calibration. That is, a few devices must be selected from a batch and destructively tested with radiation with the assurance that the resulting calibration curve is applicable to the rest of the batch. This requires fabrication of p-FETs with tight electrical parameters.

Room temperature current-voltage measurements are shown in Fig. 8 for the five FET's in this experiment. These curves were modeled using the saturation drain current expression:

$$ID = (\beta/2)(VO - |VT|)^2 \qquad (1)$$

where VO is the FET output voltage, $\beta = KP \cdot W/L$ is the transconductance, $KP = \mu C_o$, W is the channel width, L is the channel length, μ is the channel mobility, and C_o is the gate oxide capacitance per unit area.

The threshold voltage, VT, is determined from the extrapolation of the curves shown in Fig. 8 to zero drain current using a least square fitting technique. The β values were determined from the slope of the characteristics shown in Fig. 8.

VT distributions for the RADMON FET's are shown in Fig. 9 and VT distributions for the RADFET's are shown in Fig. 10. The VT for the RADMONs is 0.846 ± 0.003 V and for the RADFET's is 2.045 ± 0.010 V. The standard deviation for all FET's is considered to be acceptably small; in addition, no outliers were identified.

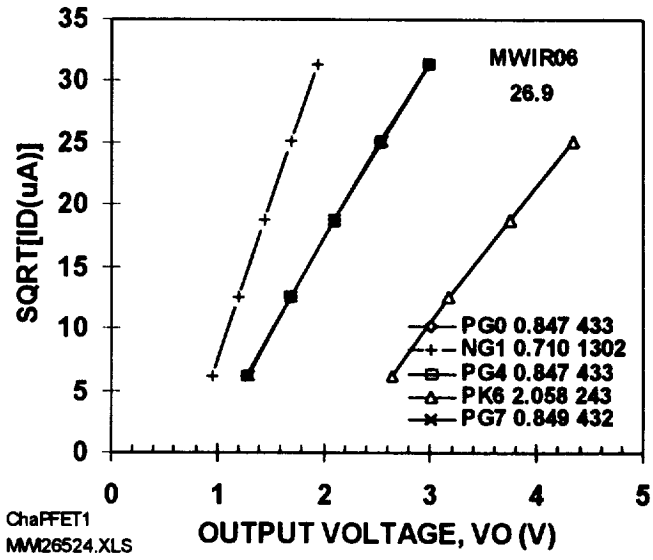

Figure 8. Typical current-voltage characteristics for the five FET's located on the MWIR. Note that the FET characteristics for PG0, PG4, and PG7 overlap. The numbers in the key are VT in volts and β in $\mu A/V^2$.

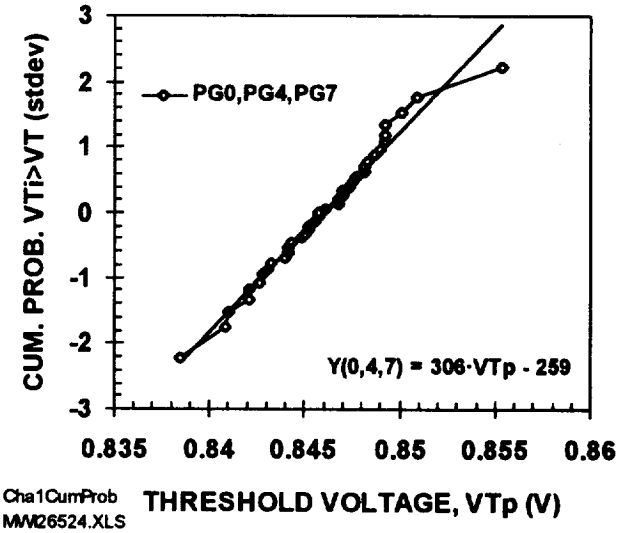

Figure 9. The cumulative probability (CUM. PROB) threshold voltage distributions for RADMONs; 39 p-FET values are shown.

Table 2. MWIR Dosimeter FET Temperature Parameters at T_O = 300K.

PARAMETER	UNITS	PG0	NG1	PG4	PK6	PG7
DEVICE NO.	---	25	25	25	25	25
VT_O	V	-0.8695	0.7122	-0.8681	-2.0500	-0.8710
VT_T	mV/°C	1.1325	-0.9154	1.2060	1.7272	1.1686
n	unitless	1.0660	1.1672	1.0863	1.3579	1.0794
β_O	$\mu A/V^2$	466.3	1343.1	465.8	249.5	464.7
KP_O	$\mu A/V^2$	23.13	66.62	23.10	5.0	23.05
β_{TO}	$\mu A/V^2°C$	-1.657	-5.226	-1.687	-1.129	-1.672
ID_O	µA	94.73	148.71	103.3	72.65	98.03
DEVICE NO.	---	13	13	13	13	13
VT_O	V	-0.8674	0.7108	-0.8689	-2.0368	-0.8680
VT_T	mV/°C	1.1094	-0.8676	1.1324	1.6448	1.1275
n	unitless	1.0266	1.1086	1.0363	1.2950	1.0321
β_O	$\mu A/V^2$	465.1	1330.5	463.6	253.7	462.3
KP_O	$\mu A/V^2$	23.07	65.99	22.99	5.07	22.93
β_{TO}	$\mu A/V^2°C$	-1.591	-4.917	-1.601	-1.095	-1.591
ID_O	µA	97.77	146.66	99.63	73.66	99.30

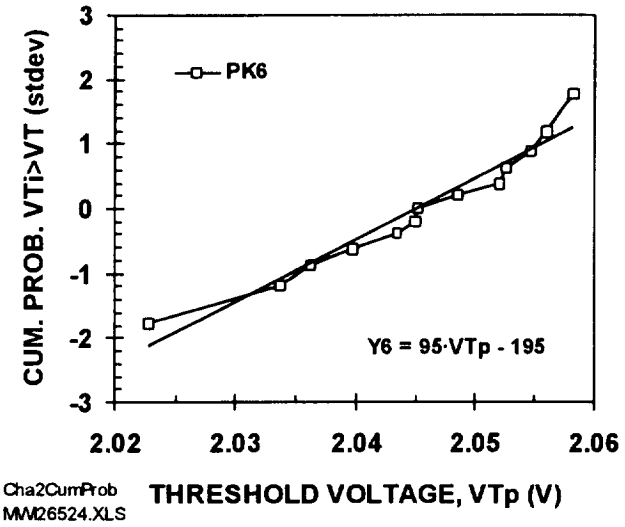

Figure 10. The cumulative probability (CUM. PROB) threshold voltage distributions for RADFETs; 13 p-FET values are shown.

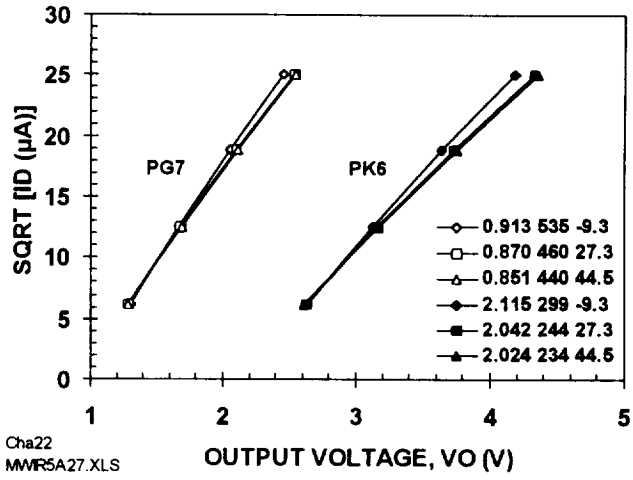

Figure 11. Temperature dependence of the p-FETs in package MWIR25 showing the temperature-independent current of 98 µA for PG7 and 73 µA for PK6. The numbers in the key are VT in volts, β in $\mu A/V^2$, and T in °C.

IV. OPERATING CONDITIONS

The operating current for these devices is determined from the temperature dependence of the IV characteristics. Data from devices PK6 and PG7 are shown in Fig. 11. A close examination of this figure indicates that the IV characteristics cross at 98 µA for PG7 and at 73 µA for PK6. The cross over point defines the temperature-independent operating point.

The temperature dependence of the threshold voltage was determined from:

$$VT = VT_O + VT_T(T - T_O) \quad (2)$$

where VT_T is the threshold temperature coefficient. The temperature dependence of β was determined from

$$\beta = \beta_O(T/T_O)^{-n} \quad (3)$$

where n is the channel mobility temperature coefficient and T is the absolute temperature. The β temperature coefficient is determined from

$$\beta_{To} = -n \cdot \beta_o / T_o \quad (4)$$

The temperature-independent drain current was calculated from

$$ID_o = 2\beta_o^3(-VT_T/\beta_{To})^2 \quad (5)$$

The ID_o values for devices 13 and 25 are listed in Table 2. In this experiment the operating drain current, ID_o is 100 μA. This will reduce the temperature effects and allow the dosimetry effects to dominate the response.

V. RADIATION CALIBRATION

A low-cost bench-top approach was used to calibrate the devices using a 1-μCi ^{241}Am source. The Am source emits alpha particles in the 5-MeV range and a number of X-rays with a maximum energy of 59 keV. The dosing mechanism is currently under study.

The p-FET voltage was measured at 100-μA. The RADFET (PK6) was determined directly from this voltage and the RADMON (PG0, PG4, and PG7) voltage was amplified 10 times. Typical results in Fig. 12 show the linear time dependence of the voltage for PK6 and PG0 measured every 30-min.

To compare RADFET and RADMON results, the differences in the device-to-radiation source distance must be determined. These two distances are illustrated in Fig. 13 as H_1 and H_2.

A FET-to-source distance model was developed using the dose rate, D_t in rad/sec expression [5]:

$$D_t = K_o \cdot \varphi \cdot L \quad (6)$$

where K_o is in rad·mg/MeV, φ is the flux in #/cm^2·sec, and L is the linear energy transfer (LET) in MeV·cm^2/mg. The flux for a point source is [5]:

$$\varphi = S/4\pi R^2 \quad (7)$$

where S is the source strength in #/sec and R is the distance in mm from the source to the p-FET.

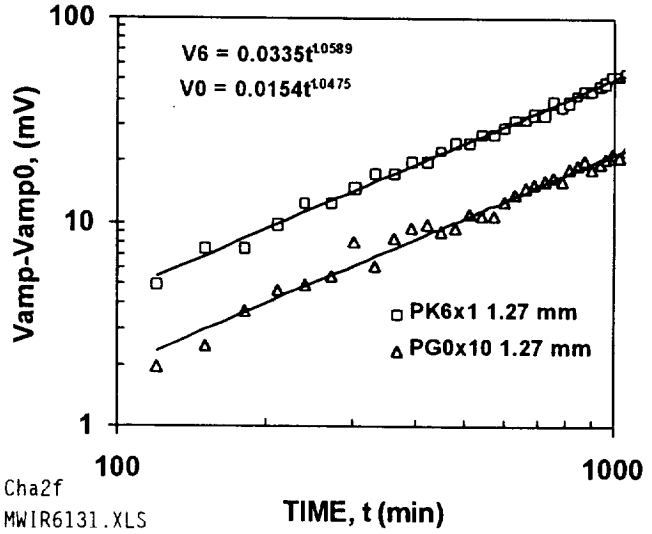

Figure 12. RADFET (PK6) and RADMON (PG0) output voltage change due to a 1-μCi ^{241}Am source where the RADMON voltage is amplified 10 times and the source is 1.27-mm above the reference plate seen in Fig.13.

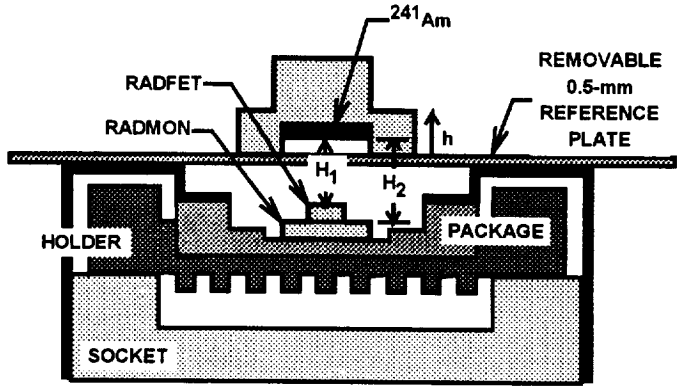

Figure 13. Cross section of the apparatus used to position the Am source above the dosimeters.

The distances, H_1 and H_2, seen in Fig. 13, cannot be determined by direct measurement. However, they can be determined by making dose measurements at different heights, h, above the reference plate. Thus, R is defined as:

$$R = H + h \quad (8)$$

where H is the FET-source distance and h is measured from the reference plate. The source is raised and lowered a distance h above the reference

plate seen in Fig. 13. Results from the RADMON are shown in Fig. 14.

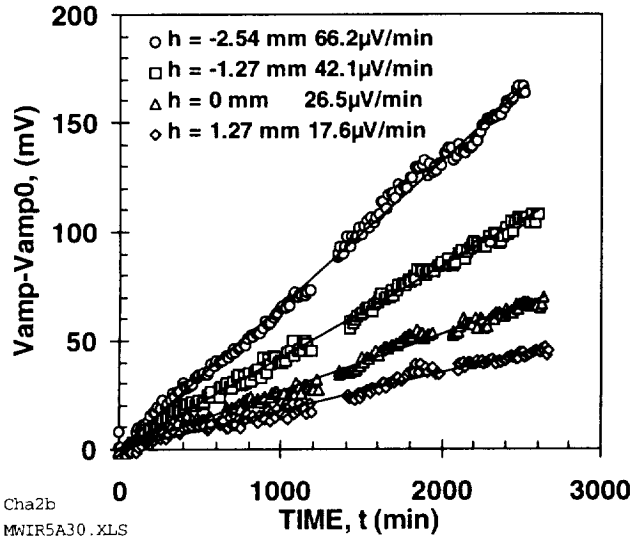

Figure 14. RADMON (PG0) voltage change due to a 1-μCi ^{241}Am source. The RADMON voltage is amplified 10 times. The source is located at h with respect to the reference plate seen in Fig. 13.

Finally, the p-FET output voltage rate, VO_t, is related to the dose rate by:

$$VO_t = V_D \cdot D_t \qquad (9)$$

where V_D is the voltage-dose sensitivity in mV/rad. Combining the above equations leads to the fitting algorithm:

$$VO_t = K/(H + h)^2 \qquad (10)$$

where

$$K = V_D \cdot K_o \cdot S \cdot L/4\pi \qquad (11)$$

The ratio of the K's for the FETs leads to:

$$\frac{V_D(\text{RADFET})}{V_D(\text{RADMON})} = \frac{K(\text{RADFET})}{K(\text{RADMON})} \qquad (12)$$

This relation allows the calculation of the dose sensitivity ratio for the two FET types found in the RADMON and RADFET where the difference in the FET-to-source distance has been removed.

The results in Fig. 15 show the voltage shift relationship between the p-FETs as a function of R. The parameters determined from the least squares fit to the data are listed in Table 3. Details of the parameter extraction are given in the Appendix.

The ratio of the dose response for the p-FETs is K_{ratio} = K(PK6)/K(PG0&PG7) = 21.0. From ^{60}Co tests, the RADMON V_D is 4.7 mV/krad [1]. Thus using the K_{ratio} = 21.0 leads to a RADFET V_D = 98.7 mV/krad. Previous response [3] of the Type K RADFET using ^{60}Co gamma rays was 200 mV/krad at zero bias and low dose. Recombination theory predicts lower response for lower photon energy. This is reflected in the LET factor initially presented in Eq. 6 and found in Eq. 11. At this time, the Am FET dosing is being compared to Co-60 dosing.

The data for each curve in Fig. 14 was acquired over a two day period. Using V_D = 4.7 mV/krad, the dose rate for the h = 1.27 mm curve is 62 millirads/sec and the dose rate for the h = -2.54 mm curve is 235 millirads/sec. These dose rates are higher than the expected space mission dose rate of 0.1 millirads/sec but smaller than the common experimental dose rate of one rad/sec.

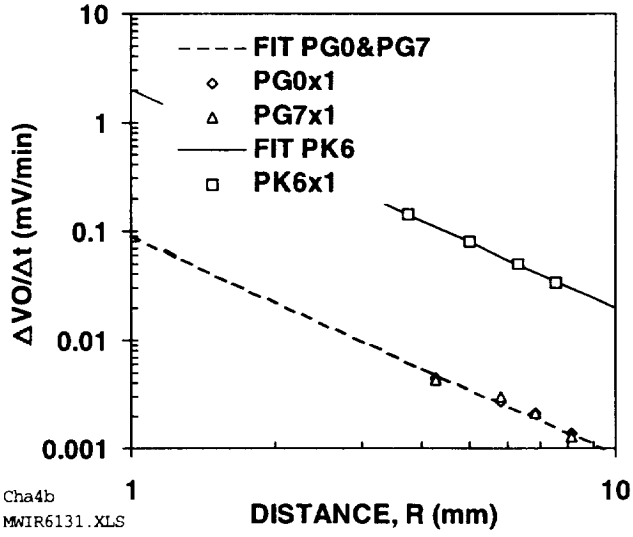

Figure 15. RADFET (PK6) and RADMON (PG0&PG7) output voltage shift rate as a function of the distance to a 1-μCi Am-241 source.

Table 3. RADFET and RADMON Parameters.

SYM	UNITS	RADMON	RADFET
H	mm	5.536	5.011
K	$mV \cdot mm^2/min$	0.091	1.994

VI. DISCUSSION

The FET response from 1-μCi ^{241}Am source radiation is easily measured. A FET-to-source distance model allows determination of relative radiation response of RADFET and RADMON even though the FETs are located at a different distance from the source. The RADFET is 21.0 times more sensitive to ^{241}Am than RADMON. Radiation doses from rads to Mrads are achievable with this detector.

VII. APPENDIX

The fitting procedure used to extract the parameter listed in Table 3 is illustrated by the graph shown in Fig. 16. The analysis is based on the 0.5-mm RADFET thickness and the 0.025-mm non-conductive epoxy thickness. Thus

$$H2 - H1 = \Delta H = 0.525 \text{ mm} \qquad (12)$$

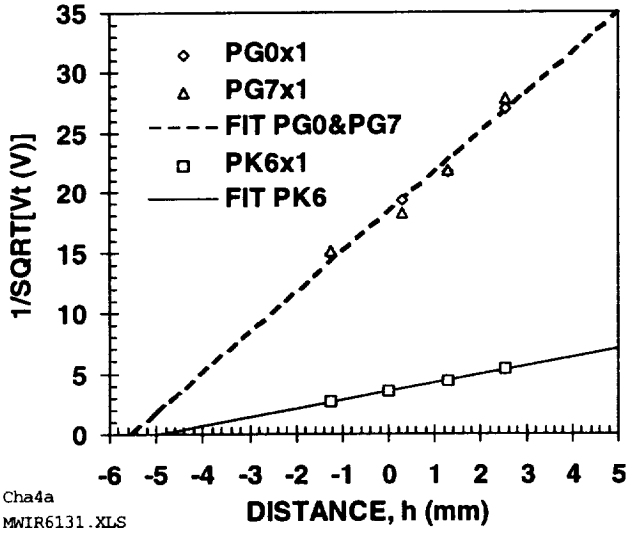

Figure 16. Graphical representation of the parameter extraction process used to extract the K and H parameter listed in Table 3.

The analysis for K and H follows from a least squares fit to the following set of equations derived from Eq. 10:

$$h_1 = -H_1 + \sqrt{K_1}/\sqrt{VO_{t1}} \qquad (13)$$

$$h_2 + \Delta H = -H_1 + \sqrt{K_2}/\sqrt{VO_{t2}} \qquad (14)$$

The result of the fitting procedure is shown in Fig. 16.

VIII. ACKNOWLEDGMENT

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