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A Thermal and Electrical Analysis of Power Semiconductor Devices

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Research Report

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ABSTRACT

The state-of-art power semiconductor devices require a thorough understanding of the thermal behavior for these devices. Traditional thermal analysis have (1) failed to account for the thermo-electrical interaction which is significant for power semiconductor devices operating at high temperature, and (2) failed to account for the thermal interactions among all the levels involved in, from the entire device to the gate micro-structure. Furthermore there is a lack of quantitative studies of the thermal breakdown phenomenon which is one of the major failure mechanisms for power electronics.

This research work is directed towards addressing. Using a coupled thermal and electrical simulation, in which the drift-diffusion equations for the semiconductor and the energy equation for temperature are solved simultaneously, the thermo-electrical interactions at the micron scale of various junction structures are thoroughly investigated. The optimization of gate structure designs and doping designs is then addressed. An iterative numerical procedure which incorporates the thermal analysis at the device, chip and junction levels of the power device is proposed for the first time and utilized in a BJT power semiconductor device. In this procedure, interactions of different levels are fully considered. The thermal stability issue is studied both analytically and numerically in this research work in order to understand the mechanism for thermal breakdown.

NOMENCLATURE

C	=heat capacitance per unit of volume
c_p	=specific heat
D	=carrier diffusivity
D^T	=thermal carrier diffusivity
$\vec{E}$	=total electrical field
E_g	=bandgap
G	carrier generation rate
H	=heat generation rate
$\vec{j}$	=electrical current density
n	=electron density
p	=hole density in semiconductor eq. or pressure in Navier-Stokes eq.
R	=carrier recombination rate
$\vec{S}_{rad}$	=Poynting vector of electromagnetic radiation field
t	=time
T	=temperature
T_i	=intrinsic temperature
u	=fluid velocity
V_{CE}	=applied collector-emitter voltage
V_{BE}	=applied base-emitter voltage
I_b	=base current
I_C	=collector current

Greek letters

ρ	=density
ε	=dielectric constant
ϕ	=electrostatic potential
κ	=thermal conductivity
μ	=carrier mobility, dynamics viscosity for fluid
γ	=kinetic viscosity

Subscripts

n	=electron
p	=hole

f	=fluid/flow

Superscripts

T	=temperature
+	=positive charged
-	=negtive charged

Acronyms

Al	Aluminum
As	Arsenide
ESD	ElectroStatic Discharge
EOS	Electrical Over Stress
FEM	Finite Element Method
Ga	Gallium
Ge	Germanium
GTO	Gate-Turn-Off Thyristor
HBM	Human Body Model
HBT	Heterojunction Bipolar Transistor
HEMT	High-Electron Mobility Transistor
IGBT	Isolated Gate Bipolar Transistor
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
NS	Navier-Stokes equations
PCB	Printed Circuit Board
SRH	Shockley-Read-Hall model of recombination
VLSI/ULSI	Very/Ultra Large Scale Integrated Circuit

SIGNIFICANCE OF THE PRESENT PROBLEM

Increasing IC integration density in power semiconductor device generates heat flux dissipation rates up to $100W/cm^2$ in some power processing applications (Mohan et al, 1995 and Lee et al, 1993). Because of this intensive heat dissipation, semiconductor devices operate at a high junction temperature. In some devices, the operation junction temperature approaches the *intrinsic* temperature. Intrinsic temperature is a threshold temperature, at which the intrinsic carrier density in semiconductor equals the majority carrier doping density, leading to the loss of functionality of transistors. This is a region where the electrical properties of semiconductors are sensitive to temperature, and devices are susceptible to thermal failure. Therefore a thorough understanding of heat transfer mechanisms and an in-depth thermal analysis are prerequisites for effective thermal management for today's power semiconductor devices.

SCOPE AND OBJECTIVES OF THE RESEARCH

Traditionally, a decoupled approach is used for thermal calculations and semiconductor device simulations (electrical). This treatment is not adequate for the state-of-art power semiconductor technology, thus requiring an in-depth understanding of thermal and electrical interactions. This research work focuses on a thorough study of thermo-electrical interactions in semiconductor devices, the significance of which is elaborated here.

From the thermodynamics point of view (Wachutka, 1990), a semiconductor micro-structure is a closed system in local thermal equilibrium, composed of electrical carrier electrons and holes and host lattices (Fig. 1). The system can be uniquely characterized by a lattice temperature $T_L(x,y,z,t)$, carrier temperature $T_e(x,y,z,t)$, and $T_h(x,y,z,t)$ (which

is considered as one local temperature $T(x,y,z,t)$ by neglecting hot carrier effects), carrier density n and p, and quasi-Fermi level $\phi_n(x,y,z,t)$ and $\phi_p(x,y,z,t)$ for electrons and holes respectively. Energy flows from carriers to lattice by lattice scattering, and between electrons and holes by carrier-carrier scattering. In addition, recombination and generation processes of carriers, such as Shockley-Read-Hall model (SRH), generate additional energy flux between carriers and lattices, and between carriers (Auger model). An inherently correct formulation must include temperature as an *independent state variable* of the semiconductor thermodynamic system.

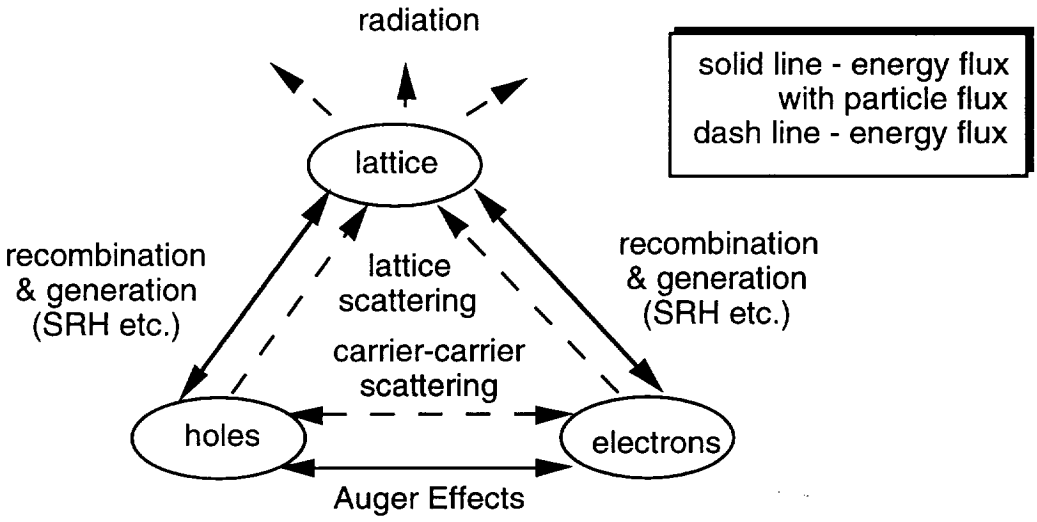

Fig. 1. Schematic of energy exchange in a semiconductor system

Carrier transportation models, such as mobility, intrinsic carrier densities and recombination/generation rates are functions of temperature. For low temperature operations, dependence on temperature can be handled by using a lumped, overall temperature of the entire device. For high temperature operations, however, both the spatial variation of temperature and the model dependence on temperature are manifested. Therefore, a coupled thermo-electrical model is required. In addition, it is necessary to include temperature diffusion terms $D_{n,p}^{T}\nabla T$ in carrier transportation equations in the drift-

diffusion model. Similarly, the heat dissipation distribution in the thermal conduction equation depends on current density, potential and carrier densities etc., which are, in turn, dependent on the temperature distribution.

An important issue in power electronics which will be studied in this research work is the prediction of thermal breakdown (secondary breakdown), which causes about 40% of IC electrostatic discharge (ESD) and electrical over stress (EOS) failures (Diaz et al, 1995). To fully understand thermal breakdown, the coupled nature of thermal and electrical mechanisms has to be understood. Thermal breakdown is usually manifested as a melted filament on a small site caused by locally high current concentration. The small site will then invariably grow in size as a result of *additional* heat generation. Once this electrical - thermal feedback loop is established, thermal failure occurs. A better understanding of the thermo-electrical interaction is necessary for the accurate prediction of the onset of such a phenomenon.

In this research work, we will also carefully investigate interactions between different levels within a power semiconductor device. The domain of thermal management for these different levels for power device expands by several orders, typically from tens of centimeters to several microns. There are essentially three different levels within power devices. They are termed as *device, chip* and *junction* levels in this report (see Table 1).

The *device* level refers to the entire power electronics device. Heat dissipates through various substrate layers within the package to the immediate environment and into the heat sink. Overall heat flux and temperature distributions within the power electronics device, optimal heat sink design and flow simulation, and thermal characterization for use of different materials and packaging technologies are topics included in modeling within this level.

Level	Scope	Governing Equation(s)	Main issues
Device level	$10 \sim 10^2 cm$	NS & Energy Eqs. incorporating the heat generation due to device	Overall Cooling Flow around heat sink Thermal package
Chip level	$0.1 \sim 1 cm$	Energy Eqs. incorporating the heat generation at the chip level	Hot spots Chip layout design
Junction level	$0.1 \sim 100 \mu m$	Drift-diffusion Eqs. & Energy Eqs. at junction level	Thermo-electrical interaction Thermal breakdown

Table 1. Three levels in semiconductor devices

The chip level refers to an individual semiconductor chip or a portion of it. Based on electrical circuit design and chip layout design, a realistic heat generation distribution is prescribed. The aim of simulation at this level is the determination of hot spot locations within a chip and localized transient response of thermal load from ESD, as well as optimization of chip layout design.

The junction level refers to the p-n junction micro-structure. Simulation domain of junction level usually includes one or several transistor structures. At this level our aim is to model the coupled semiconductor equations (drift-diffusion equations) and the thermal energy equation. This will lead to a significantly better understanding of various thermal and electrical interactions which in turn will lead to some guidelines for micro-structure layout and doping design.

Most previous works have been concentrated at only *one* level of the cited levels. When information for a lower or higher level was required, some drastic and unsystematic over-simplifying assumptions were often used. However, interactions between three levels have been literally ignored even though they have been reported to be very important (Tan et al, 1993). For example, distribution of electrical variables as well as temperature at the micro-structure level was reported to be very sensible to local thermal boundary condition, which can be accurately obtained only through a simultaneous junction and chip level modeling. However, most simulation work at the junction level used a *constant* heat transfer coefficient or a *constant* emperature condition at the boundary.

In our work, interactions between different levels are incorporated iteratively using the following procedure (see Fig. 2). As a first guess, an evenly distributed heat source term is used at the device level, and the temperature distribution, particularly that in the vicinity of the chip domain, is calculated. Using this temperature boundary condition and a presumed heat source term (a first guess) for the chip domain, a chip level temperature distribution is obtained, including the distribution on the boundary of junction domain. A thermo-electrical simulation is then carried within the junction domain, by simultaneously solving the drift-diffusion and thermal energy equations. Temperature distribution within the junction domain, as well as electrical variables are then obtained. Based on this information, a heat generation distribution within the junction level is calculated. Next, using a spatially periodical condition based on various chip layout and device configuration in each case, new heat source distributions at the chip and device level, are obtained. Utilizing these updated heat source distributions at the device level, the above described procedure is repeated and the updated temperature distributions within the three levels are calculated and then compared to the previous distributions. This iteration procedure continues until convergence at all levels is obtained.

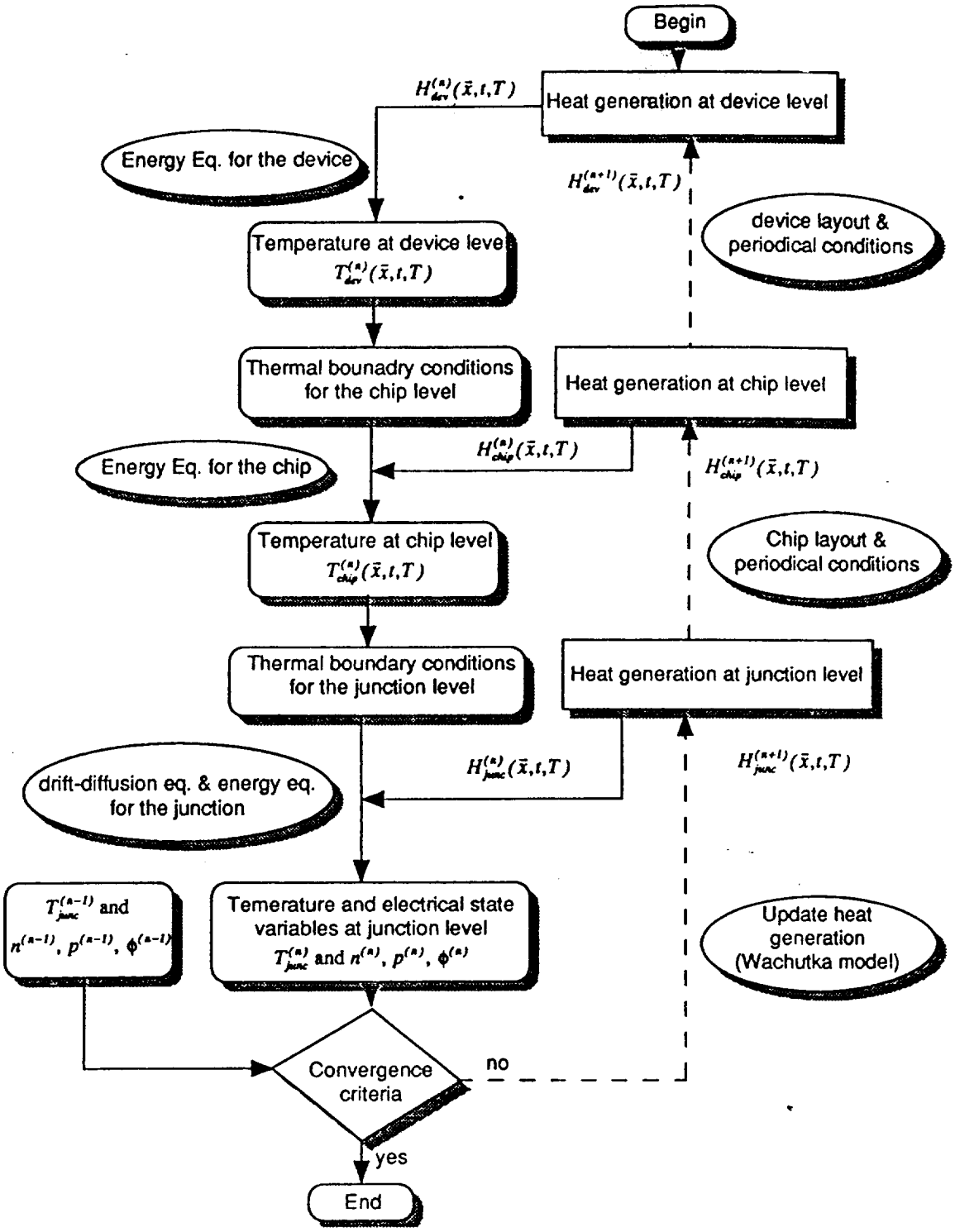

Fig. 2. Iterative procedure for 3-level simulations

LITERATURE REVIEW

Of more than 10,000 papers on semiconductors in journals and in conference reports published during 1988 to 1996, nearly 800 papers are found to be related to thermal issues. After a comprehensive review, it has be determined that about sixty of these papers are relevant to this research work. These works can be categorized as those concentrating on *Thermal Modeling, Electro-Thermal Modeling* and *Thermal Breakdown.*

Thermal Modeling

With this category, the thermal behavior of various semiconductor devices at the device, chip or the micro-structure level is considered. Within this category, there is *no* consideration of electrical coupling.

Among pertinent work in this category, Higgins (1993) studied the thermal behavior of AlGaAs/GaAs HBT power transistors. Using a 3D finite difference thermal simulator, the author carefully examined some quantitative tradeoff between power density, chip layout and junction temperatures. Several design approaches were found to be practical to lower operating temperature, including usage of substrate via, topside deposition of diamond-like layers and substrate exchange methods for reduction of thermal resistance. However, some limitations of this type of work are:

- The computation domain (Fig. 3) is related to the junction level, yet no electrical coupling is included.
- A constant temperature boundary condition is used in this work and the effects of realistic temperature distribution on this *ad hoc* treatment is not discussed.
- The phenomenon of thermal instability was found to be a major cause of sudden

failure in HBT's. A qualitative thermal instability mechanism analysis and prevention suggestions (raising the threshold power density & reduction of thermal resistance etc.) were also included in this work, but without any quantitative result. This is because Higgins (1993) did not account for the electro-thermal coupling.

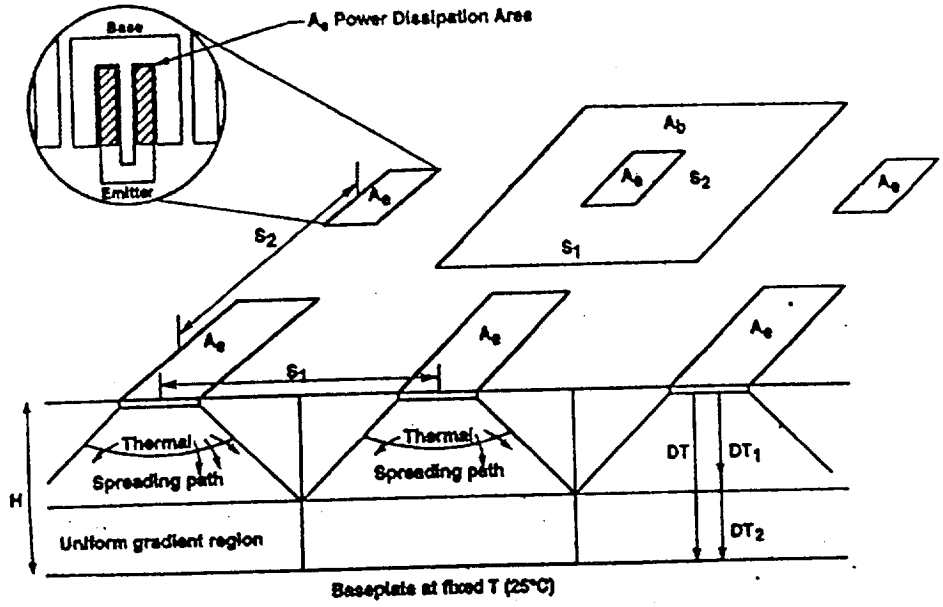

Fig. 3. Simulation domain in Higgins (1993)

Gallium-Arsenide-based MMIC (Monolithic Microwave Integrated Circuits) have been used for frequencies higher than those suitable for silicon. GaAs has high mobility desirable for high-frequency devices and large bandgap desirable for high temperature operation, but it has a poor thermal conductivity (which can be modeled as $\frac{54400}{T^{1.2}}(W/mK)$. Many thermal studies have been done on MMIC. Webb (1993) examined the thermal resistance of typical GaAs power device structures under steady-state conditions and fixed input power at the chip level. Two-dimensional simplification was

also examined and was found to be realistic only for channels of excessive width relative to the other chip dimensions, which is electrically unlikely in any device design. (see Fig. 4 for the simulation structure and 2D and 3D comparison) Ferrara et al (1995) constructed a finite-element method model which contains a "global" model with resolution to chip level and a "local" sub-model with resolution to individual gates and channels of a MMIC device. Other work on MMIC have been reported by and Fan et al (1992).

Edwards et al (1995) studied several thermal enhancement technologies for IC packages at the device level. The technologies studied included utilization of heat slugs, heat spreader, thermal via, and high thermal conductivity of mold compounds and PCB to improve the thermal performance. They found that all these technologies depend strongly upon package configuration. For example, heat slug or heat spreader is found to be effective if chip size is small relative to the size of package. Trade-off for selections of these technologies was also discussed. A more careful study of thermal via performance can be found in Handa et al (1993). The above cited works are all based on a steady state simulation. Relatively little work has been done on the transient effects, some examples of this type of work can be found in Min (1990) and Krieger (1987). Min (1990) derived a transient, three dimensional, analytical temperature solution of a two-layer semi-infinite plate structure with embedded heat source, using Green function method. It was also reported that the transient thermal response could not be represented by a conventional R-C circuit analogy.

Electro-Thermal Modeling

Electro-thermal modeling has gained increased attention in the past two decades. Many fundamental results have been established, and sophisticated semiconductor physical simulators, such as PISCES, have been well-developed.

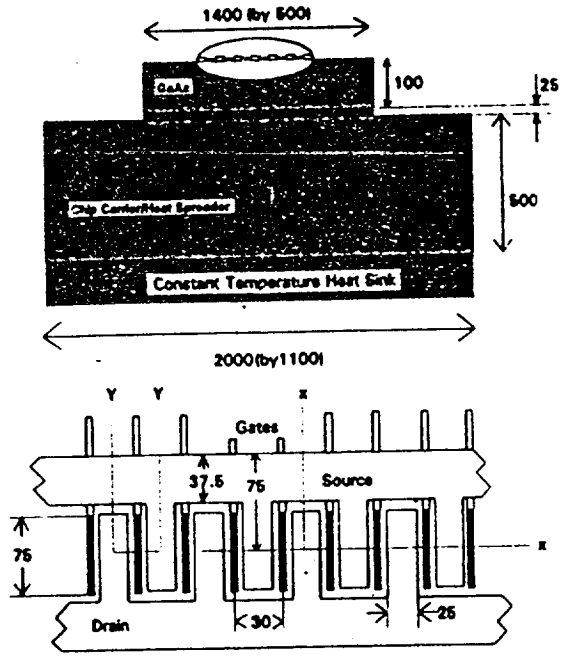

Fig. 1. Cross-sectional view of the test structure showing the GaAs chip and chip carrier. Layout of the MESFET showing the gate geometry and metallization pattern.

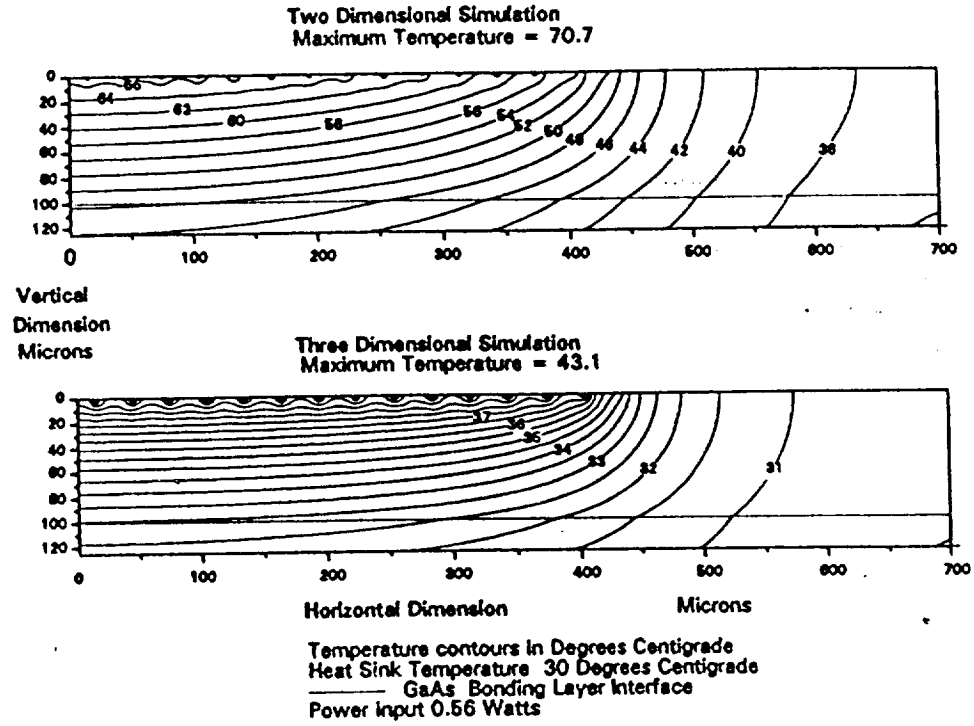

Fig. 6. Cross-sectional view of the temperature contours within the GaAs chip contrasting a two- and three-dimensional simulation.

Fig. 4. Simulation structure and 2D and 3D comparison in Webb (1993)

A correct heat generation term is crucial to thermo-electrical modeling. Several models have been introduced, e.g. Adler (1978), and Chryssafis and Love (1978), with some *ad hoc* simplifications. Wachutka proposed a heat generation model utilizing a thermodynamic treatment, without using any *ad hoc* assumptions. For a general case, the heat generation is modeled as

$$\begin{aligned} H &= \vec{j}\cdot\vec{E} + (R-G)\cdot\left(E_g + 3\kappa T\right) \\ &-\left(\vec{j}_n + \vec{j}_p\right)\cdot\left(\frac{3}{2}\kappa T + \frac{1}{2}\vec{\nabla}E_g\right) - \left\langle div\vec{S}_{rad}\right\rangle \end{aligned} \tag{1}$$

The first term in eq. (1) is the traditional Joule heat. The second term is the energy exchange between carriers and lattice in the process of recombination and generation of electrons and holes. The third term accounts for the presence of a non-constant temperature distribution and spatial variations of band edges, and the last term is associated with the electromagnetic field. Wachutka's heat generation model has been widely adopted in semiconductor device simulation works (Mawby et al, 1994, Ameraskera et al, 1993 and Hu et al, 1994) as well as in commercial device simulation packages (ATLAS/VW). This model is also adopted in our work.

Amerasekera et al (1993) investigated the effect of self-heating on the high current *I-V* characteristics of simple semiconductor structures (resistors and diodes) utilizing an electro-thermal device simulator. It was shown that when self-heating was included in the simulation, avalanche generation and thermal generation both contribute to an increase in the minority carrier density and significantly changes the *I-V* characteristics. For the structures studied, thermal breakdown occurred at temperatures higher than intrinsic temperature T_i, ranging from $1.25\ T_i$ to $3T_i$. They concluded that the intrinsic temperature is not a general condition for thermal breakdown. They proposed an improved condition for thermal breakdown based on the rate of minority carrier generation and the rate of

power dissipation. They also observed a phenomenon where the peak temperature does not coincide with the location of the maximum heat generation and suggested an analytical explanation for this phenomenon. It was shown in their simulations that the same mechanism triggers snapback, whether the origin is thermal or impact ionization. With the increase in temperature, the carrier (electron and hole) generation rate due to impact ionization decreases but that due to thermal generation increases and the net positive change of generation rate leads to onset of snapback. Thus they concluded that simulations of snapback condition (thermal or electrical breakdown) must include the temperature dependency of the generation rate of minority carriers.

More recently, Fushinobu et al (1995) developed a nonequilibrium energy transportation model for GaAs MESFET with a gate length of *0.2* micron. A strong peak of the Joule heating rate was found at the drain side of the active layer, with the maximum value of about $4 \times 10^{16} \, W/m^3$. A local hot spot was found at the drain side of the channel under the depletion region, with the maximum temperature of about 1370K. A pure electrical simulation for the same device was compared with a thermo-electrical simulation to examine heat transfer effect. The result suggested that h has considerable effect on the electrical performance of GaAs MESFET. Electrical current is reduced by lattice self-heating, due to a decrease in mobility. The thermal conductance of the package was also observed to have a strong influence on the transient response of the MESFET device. However, the heat transfer coefficient h used in their work is fixed and effects of spatial variation of h were not discussed. Tan et al (1993) simulated a AlGaAs-GaAs ridge laser diode structure utilizing both a non isothermal and an isothermal models. Similar with Fushinobu et al (1995), the results in this paper demonstrated that the thermal exchange rates at the boundaries could significantly change the performance of the laser diodes. They also discussed the use of silicon substrate in the monolithic integration of AlGaAs and GaAs devices since silicon has a higher thermal conductivity than that of GaAs (about 3

times).

Selmi and Ricco (1993) presented a simple model to account for the temperature effects influencing the dc performance of GaAs MESFET's, based on a solution of heat flow and current equations. Isothermal and non isothermal *I-V* characteristic curves of the same FET were compared and it was found that device self-heating causes a significant distortion of the curves at high gate voltages, leading to negative values of the output conductance.

Christianson and Moglestue (1995) carried out an experimental investigation of thermal-induced failure mechanism on *0.3* micron AlGaAs/GaAs HEMTs. Their experiments confirmed the existence of the temperature-heat generation, positive feed back failure mechanism, in which the high temperature in the drain region increases the drain resistance, generating more hot electrons, thus leading to more heat generation, and further increase of the drain temperature. Other electro-thermal studies can be found in Ghazavi and Ho (1995) for MESFET, Mawby (1994) for GTO thyristors and Hu (1994) for IGBT.

Thermal Breakdown

A number of works by a research group from the Wright Laboratory (J. J. Liou, 1994; Kager and J. J. Liou et al 1994 and 1995; Liou and Ortiz-Conde et al 1995; Liou and L. L. Liou et al 1994; L. L. Liou and Ebel et al 1993; L. Liou and Bayraktaroglu et al 1993) have contributed to an understanding of thermal stability analysis of AlGaAs/GaAs Heterojunction Bipolar Transistors (HBTs) with multi-finger emitter configuration. In their models, they have derived an analytical solution for the two-dimensional thermal conduction equation with multi-finger structure. The heat generation term was based on using a Joule heating term,

$$p(T) = \beta(T) J_b(T) V_{ce} \tag{2}$$

where $\beta(T)$ is the common-emitter current gain and $J_b(T)$ is the base current density. The functional forms for β and J_b were provided by a one-dimensional drift-diffusion simulator with carrier degeneracy model of heterojunction structures. The authors found current "crush" characteristics in $I_C - V_{CE}$ curves, due to the significant thermal coupling among the fingers at high I_B and V_{CE}. They showed a ballast resistance can prevent the current crush phenomenon from occurring, because a ballast resistance reduces the voltage drop across the emitter-base junction and in turn reduces the collector current and minimizes the heat generation. (This is also mentioned in Higgins 1993.) Besides, they observed an interesting self-cooling phenomenon in which emitter contact region is cooler than heat sink, due to the non equilibrium effect.

Thermal breakdown usually occurs when the local temperature in the semiconductor becomes unstable. Flik and Tien (1990) proposed an intrinsic thermal stability model for anisotropic thin film superconductors. A stability criteria was presented by assuming the existence of a normal zone that produces Joule heating and examining the condition under which the zone will grow or decay. This work demonstrated the approach of thermal stability analysis and the way to transform information on thermal disturbance spectrum into design criteria.

Olchak (1988) presented a thermal analysis of thermal breakdown for a one dimensional cylinder of silicon. The temperature dependence of conductivity (thus heat dissipation rate) was modeled as

$$\sigma(T) \propto \exp(-\theta / T)$$

Other research on thermal failure include Dwyer et al (1990), who employed an electrical de coupled model of transient thermal analysis, with use of human body model (HBM) of ESD.

METHODOLOGY

Computational programs employed in our research work are FIDAP and ATLAS. FIDAP was used to solve the proper transport equations at the device and chip levels. It was also used as the fluid dynamics simulator to numerically solve Navier-Stokes equations. ATLAS was used for simulating the electro-thermal interaction at the junction level.

A Galerkin-based finite-element method was employed to solve the system of differential in the present work. This technique is well-described by Gresho et al. The incorporation of this numerical scheme in the finite-element code used is also well-documented.

The continuum domains is first divided into simply shaped regions called elements within each of which the unknown variables are approximated by using a set of interpolation functions. Substituting these basis functions into the governing equations and boundary conditions yields a residual in each of the equations. The Galerkin method of weighted residuals reduces these error to zero by making them orthogonal to the interpolation functions of each element.

EQUATIONS AND PHYSICAL MODELS

A full scale simulation involves the use of the thermal conduction equation within the device, chip and junction domains, fluid dynamics and energy equations for the heat sink flow, and electrical carrier transportation and potential equations for semiconductors.

Basic Equations

The heat conduction equation that governs temperature distribution within the device and chip levels is

$$\rho c_p \frac{\partial T}{\partial t} = \kappa \nabla^2 T + H \tag{3}$$

where the heat generation term H can be a function of time, location and temperature in a general case.

For forced-convection cooling of the power electronic device, the governing equations for the flow field and the energy equation are mass continuity equation,

$$\frac{\partial u_j}{\partial x_j} = 0 \tag{4}$$

momentum conservation equations,

$$\frac{\partial u_j}{\partial t} + u_j \frac{\partial u_i}{\partial x_j} = -\frac{1}{\rho}\frac{\partial p}{\partial x_i} + \nu \frac{\partial^2 u_i}{\partial x_j \partial x_j} \tag{5}$$

and energy conservation equation for coolant temperature

$$\rho c_{pf}\left(\frac{\partial T}{\partial t}+u_j\frac{\partial T}{\partial x_j}\right)=\kappa_f\nabla^2 T+\frac{1}{2}\mu_f\left[\left(\frac{\partial u_i}{\partial x_j}+\frac{\partial u_j}{\partial x_i}\right)-\frac{2}{3}\left(\frac{\partial u_k}{\partial x_k}\right)\delta_{ij}\right]^2:\nabla\mathbf{u} \tag{6}$$

Currently for the semiconductor electrical simulation, we employ the drift-diffusion model. This model has been proved to be sufficiently accurate by various investigators, e.g. SILVACO (1995). This model includes Poisson's equation for electrostatic potential ϕ

$$\begin{aligned}&\nabla\cdot\vec{E}=-\frac{q}{\varepsilon}\left(N_n^+-N_p^-+p-n\right)\\&\text{where } \vec{E}=-\vec{\nabla}\phi\end{aligned} \tag{7}$$

where N_n^+, N_p^- are the local concentrations of ionized donors and acceptors, respectively, *n, p* are electron and hole density, respectively, q is the electronic charge of electron and ε is permitivity of the semiconductor material. Carrier continuity for electrons is

$$\frac{\partial n}{\partial t}=\frac{1}{q}\nabla\cdot\vec{J}_n+G_n-R_n \tag{8}$$

and carrier continuity for holes is

$$\frac{\partial p}{\partial t}=-\frac{1}{q}\nabla\cdot\vec{J}_p+G_p-R_p \tag{9}$$

where G_n, G_p, R_n, R_p are recombination and generation rates of *n* and *p,* respectively.

Constitutive equations for $\vec{J}_n, \vec{J}_p$ are required to close the drift-diffusion model. For the electron flux

$$\vec{J}_n = nq\mu_n\vec{E} + qD_n\nabla n + qD_n^T\nabla T \tag{10}$$

and for the hole flux

$$\vec{J}_p = -pq\mu_p\vec{E} + qD_p\nabla p + qD_p^T\nabla T \tag{11}$$

where μ_n, μ_p are carrier mobility, D_n, D_p are carrier diffusivity and D_n^T, D_p^T are thermal diffusivity for electrons and holes, respectively.

Heat transfer at the junction level is governed by

$$C\frac{\partial T}{\partial t} = \nabla(\kappa\nabla T) + H \tag{12}$$

where k and C are functions of thermal conductivity and heat capacitance, which are in turn functions of temperature. As mentioned before, we use Wachutka's Model (eq. (1)) for the heat generation rate H.

Physical Models

Various constitutive equations are required in order to solve for the drift-diffusion equations. Carrier mobility is perhaps the most important parameter in the model. A model utilized in this work is based on the total doping concentration N, and the lattice temperature T. This model which is suitable for the low-electrical field case, is represented by

$$\mu_{n,p} = \mu_{1n,p}\left(\frac{T}{300K}\right)^{\alpha_{n,p}} + \frac{\mu_{2n,p}\left(\frac{T}{300K}\right)^{\beta_{n,p}} - \mu_{1n,p}\left(\frac{T}{300K}\right)^{\alpha_{n,p}}}{1+\left(\frac{T}{300K}\right)^{\gamma_{n,p}}\left(\frac{N}{N_{cn,p}}\right)^{\delta_{n,p}}} \tag{13}$$

Parameters in this model are listed in Table 2.

parameter	value	unit	parameter	value	unit
μ_{1n}	55.24	$cm^2/(Vs)$	μ_{1p}	49.74	$cm^2/(Vs)$
μ_{2n}	1425	$cm^2/(Vs)$	μ_{2p}	479.4	$cm^2/(Vs)$
α_n	0.0	no unit	α_p	0.0	no unit
β_n	-2.3	no unit	β_p	-2.2	no unit
γ_n	-3.8	no unit	γ_p	-3.7	no unit
δ_n	0.73	no unit	δ_p	0.70	no unit
N_{cn}	1.072×10^{17}	cm^{-3}	N_{cp}	1.606×10^{17}	cm^{-3}

Table 2. Parameters in mobility model eq. (13)

Arora Model is another analytical model for the doping and temperature dependence of the mobility, and has the following form:

$$\mu_{n,p} = \mu_{1n,p}\left(\frac{T}{300K}\right)^{\alpha_{n,p}} + \frac{\mu_{2n,p}\left(\frac{T}{300K}\right)^{\beta_{n,p}}}{1+\frac{N}{N_{cn,p}\left(\frac{T}{300K}\right)^{\gamma_{n,p}}}} \tag{14}$$

Parameters of this model are listed in Table 3.

parameter	value	unit	parameter	value	unit
μ_{1n}	88.0	$cm^2/(Vs)$	μ_{1p}	54.3	$cm^2/(Vs)$
μ_{2n}	1252.0	$cm^2/(Vs)$	μ_{2p}	407.0	$cm^2/(Vs)$
α_n	-0.57	no unit	α_p	-0.57	no unit
β_n	-2.33	no unit	β_p	-2.33	no unit
γ_n	2.546	no unit	γ_p	2.546	no unit
δ_n	0.73	no unit	δ_p	0.70	no unit
N_{cn}	1.432×10^{17}	cm^{-3}	N_{cp}	2.67×10^{17}	cm^{-3}

Table 3. Parameters in Arora mobility model eq. (14)

Several recombination/generation models exist based on various physical mechanisms. In this work the Shackley-Read-Hall Recombination model is utilized. This model is represented by

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{\varepsilon_t - \varepsilon_j}{kT}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{\varepsilon_j - \varepsilon_t}{kT}\right)\right]} \tag{15}$$

where ε_t is the trap energy, and τ_n and τ_p are the electron and hole lifetimes

$$\tau_{n,p} = \frac{\tau_{n,p0}}{1 + \frac{N}{N_{SRH-n,p}}} \tag{16}$$

where N is the total impurity concentration. Parameters are listed in Table 4.

parameter	value	unit	parameter	value	unit
$\varepsilon_t - \varepsilon_i$	0.0	eV	τ_{n0}	10^{-7}	s
τ_{p0}	10^{-7}	s	N_{SRH-p}	5×10^{16}	cm^{-3}
N_{SRH-n}	5×10^{16}	cm^{-3}			

Table 4. Parameters in SRH model eq. (15) and (16)

Direct recombination for electrons and holes is modeled as

$$R_{opt} = C_{opt}\left(pn - n_{ie}^2\right) \tag{17}$$

where n_{ie} is the intrinsic electron density and Auger Recombination is modeled as

$$R_{Aug} = C_n\left(pn^2 - nn_{ie}^2\right) + C_p\left(np^2 - pn_{ie}^2\right) \tag{18}$$

Parameters are listed in Table 5.

parameter	value	unit	parameter	value	unit
C_n	8.3×10^{-32}	cm^6 / s	C_p	1.8×10^{-31}	cm^6 / s

Table 5. Parameters in Auger model of eq. (17) and (18)

At the interface of the insulator and the semiconductor, the following surface recombination model is used

$$J_{sn} = qv_{sn}\left(n_s - n_{eq}\right)$$
$$J_{sp} = qv_{sp}\left(p_s - p_{eq}\right) \tag{19}$$

The generation rate of impact ionization is modeled according to

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q}$$
$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp\left(-\frac{E_{n,p}^{crit}}{E}\right)^{\beta_{n,p}} \tag{20}$$

The presence of a high electric field the generation rate of band-to-band tunneling is accounted for as

$$G_{BBT} = A_{BBT} E^{\gamma} \exp\left(-\frac{B_{BBT}}{E}\right) \tag{21}$$

Diffusivity of electrons and holes is given by Einstein's relation as

$$D_{n,p} = \frac{\mu_{n,p} kT}{q} \tag{22}$$

and thermal diffusivity is given by

$$D_{n,p}^{T} \approx \frac{D_{n,p}}{2T} \tag{23}$$

Finally, the thermal conductivity is modeled as

$$\kappa(T) = \frac{1}{a + bT + cT^2} \tag{24}$$

with parameters in Table 6.

parameter	value	unit	parameter	value	unit
a	0.03	cmK / w	b	0.00156	cm / w
c	1.65×10^{-6}	$cmK / (wK)$			

Table 6. Parameters for thermal conductivity in eq. (24)

and the thermal capacitance per unit volume is modeled as a function of temperature as well

$$C = a + bT + cT^2 + \frac{d}{T^2} \tag{25}$$

Parameters are listed in Table 7.

parameter	value	unit	parameter	value	unit
a	1.97	J / cm^3	b	0.00036	$J / cm^3 / K$
c	0	$J / cm^3 / K^2$	d	-37000	$J / cm^3 / K^3$

Table 7. Parameters thermal capacitance in eq. (25)

CURRENT STATUS AND EXPECTED RESULT

Perturbation Analysis of Thermal Stability

Thermal or secondary breakdown is a major failure mode for minority carrier devices, especially for bipolar junction transistors. When thermal breakdown occurs, heat dissipates in localized regions rather than uniformly in the entire volume of the device.

This leads to a high temperature in the localized regions. In minority carrier devices, the current density is proportional to the square of intrinsic electron density, which increases drastically with temperature (see Fig. 5), leading to a negative temperature coefficient of resistance. Consequently, the high temperature spot dissipates more heat, and if this positive feedback continues, the device breaks down.

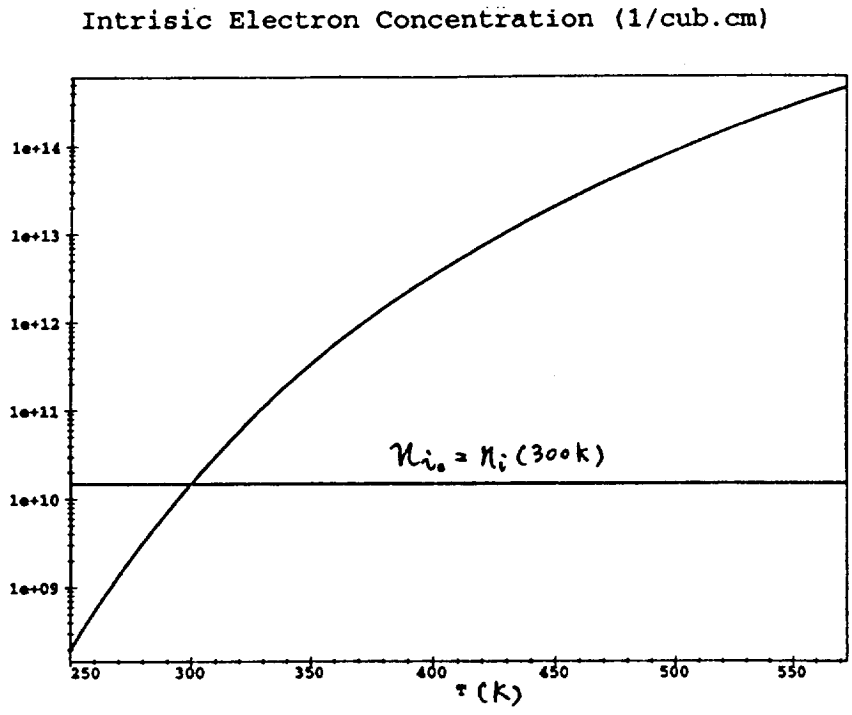

Fig. 5. Temperature dependence of intrisic concentration

To illustrate the thermal breakdown process, consider the conduction equation that governs temperature distribution

$$\rho c_p \frac{\partial T}{\partial t} = \kappa\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + H(T) \tag{26}$$

with convective boundary condition

$$-\kappa \frac{\partial T}{\partial n} = h(T - T_a) \tag{27}$$

in which the heat generation term is assumed to be temperature-dependent. Generally, $H(T)$ can be a non-linear term of temperature and it is difficult to find an analytical solution. However, we can examine the linear stability of this equation using the perturbation method. Assuming that T_0 is the steady state solution of (26), a perturbation around this solution can be expressed as

$$\rho c_p \frac{\partial(T_0+\varepsilon T')}{\partial t} = \kappa\left(\frac{\partial^2(T_0+\varepsilon T')}{\partial x^2}+\frac{\partial^2(T_0+\varepsilon T')}{\partial y^2}+\frac{\partial^2(T_0+\varepsilon T')}{\partial z^2}\right)$$
$$+H(T_0)+\varepsilon\left.\frac{\partial H}{\partial T}\right|_{T=T_0} T'+O(\varepsilon^2) \tag{28}$$

in which $|\varepsilon|<<1$. Applying eq. (26) into eq. (28) and neglecting higher order ε terms results in the small disturbance equation

$$\rho c_p \frac{\partial T'}{\partial t} = \kappa\left(\frac{\partial^2 T'}{\partial x^2}+\frac{\partial^2 T'}{\partial y^2}+\frac{\partial^2 T'}{\partial z^2}\right)+H_0 T'$$
$$\text{where } H_0 = \left.\frac{\partial H}{\partial T}\right|_{T=T_0} \text{ is a function of } T_0 \text{ only.} \tag{29}$$

with boundary condition

$$-\kappa\frac{\partial T'}{\partial n} = hT' \tag{30}$$

Note that when h approaches ∞ we obtain the constant temperature case, while when h approaches zero we obtain the adiabatic case. Here we discuss two dimensional cases (see Fig. 6), as one- and three- dimensional cases are based on very similar analysis. For two dimensional cases, eq. (26) reduces to

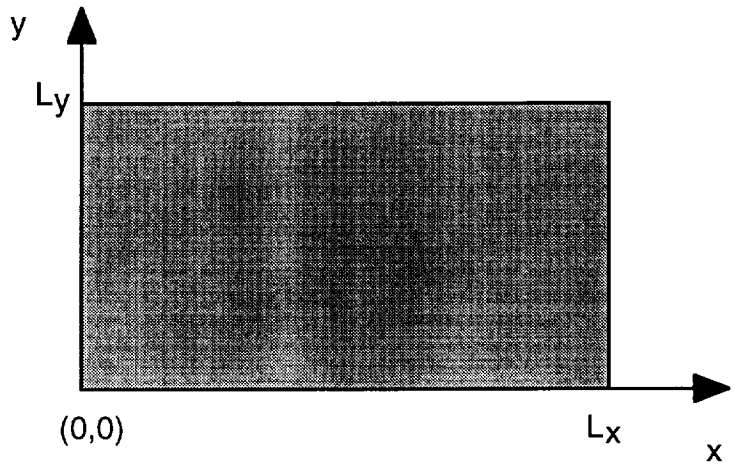

Fig. 6. Rectangular domain for the perturbation analysis

$$\rho c_p \frac{\partial T'}{\partial t} = \kappa\left(\frac{\partial^2 T'}{\partial x^2} + \frac{\partial^2 T'}{\partial y^2}\right) + H_0 T' \tag{31}$$

and boundary condition (27) becomes

$$x = 0: \quad \kappa\frac{\partial T'}{\partial x} = hT' \ , \ x = L_x: \quad -\kappa\frac{\partial T'}{\partial x} = hT' \tag{32}$$

and

$$y = 0: \quad \kappa\frac{\partial T'}{\partial y} = hT' \ , \ y = L_y: \quad -\kappa\frac{\partial T'}{\partial y} = hT' \tag{33}$$

Using separation of variables

$$T'(x,y,t) = F(x,t)\cdot G(y,t) \tag{34}$$

eq. (31) then takes the form,

$$\left(\frac{-\rho c_p F_t + \kappa F_{xx}}{F}\right) + \left(\frac{-\rho c_p G_t + \kappa G_{yy}}{G}\right) + H_0 = 0 \tag{35}$$

leading to the separation of x and y components, namely

$$\begin{aligned} \left(\frac{-\rho c_p F_t + \kappa F_{xx}}{F}\right) &= a \\ \left(\frac{-\rho c_p G_t + \kappa G_{yy}}{G}\right) &= b \\ a + b &= -H_0 \end{aligned} \tag{36}$$

For x component,

$$-\rho c_p F_t + \kappa F_{xx} = aF \tag{37}$$

Using variable separation again to eq. (37), namely let

$$F(x,t) = P(t)Q(x) \tag{38}$$

Substituting (38) into (37), the solution is obtained as

$$\begin{aligned} P(t) &= C_0 \exp\left(-\frac{a + \kappa\lambda_x^2}{\rho c_p} t\right) \\ Q(x) &= C_1 \sin(\lambda_x x) + C_2 \cos(\lambda_x x) \end{aligned} \tag{39}$$

A similar solution is obtained for $G(y,t)$ component. Hence, the small disturbance temperature takes the form

$$T'(x,y,t) = C_0 \exp\left(\frac{-\kappa\left(\lambda_x^2 + \lambda_y^2\right) + H_0}{\rho c_p} t\right) \left(\sin(\lambda_x x) + C_1 \cos(\lambda_x x)\right) \cdot \left(\sin(\lambda_y y) + C_2 \cos(\lambda_y y)\right) \tag{40}$$

Applying boundary condition (32) and (33), we obtain the eigenvalue equations for λ_x and λ_y

$$\left(\lambda_x^2 \kappa^2 - h^2\right) \sin \lambda_x L_x - 2\lambda_x \kappa h \cos \lambda_x L_x = 0 \tag{41}$$

and

$$\left(\lambda_y^2 \kappa^2 - h^2\right) \sin \lambda_y L_y - 2\lambda_y \kappa h \cos \lambda_y L_y = 0 \tag{42}$$

Note that (41) and (42) are found to be independent of the position of the coordinate system. For example, using $x = \pm\frac{L_x}{2}$ and $y = \pm\frac{L_y}{2}$ as boundary yields the same result, which is reasonable.

A stable solution is obtained when the perturbation solution does not grow with time. To ensure this condition, we need to impose

$$H_0 < \kappa\left(\lambda_x^2 + \lambda_y^2\right) \tag{43}$$

and in general

$$H_0 < \kappa \sum_{i=1}^{n} \lambda_i^2 \tag{44}$$

where n=1,2,3 for one, two and three dimensional cases respectively. Eq. (44) indicates an important fact that the derivative of heat dissipation rate with respect to temperature

$H_0 = \left.\frac{\partial H}{\partial T}\right|_{T=T_0}$ determines the thermal stability of a semiconductor chip. It should be addressed that this fact cannot be seen clearly by previous works of direct solutions of energy equation. For a more realistic configuration numerical approaches are necessary, while for a rectangular configuration eq. (44) can serve as a criteria for thermal stability and its application is under investigation. As an example, let us consider the one dimensional case, with an initial condition of

$$T'(x,0) = f_0(x) \tag{45}$$

The solution of temperature disturbance is given by

$$T'(x,t) =$$

$$\sum_{n=1}^{\infty}\left[\frac{2}{L-\kappa\sin^2(\lambda_n L)}\int_0^L f_0(\zeta)\cos(\lambda_n\zeta)d\zeta\right]\cdot\exp\left(\frac{-\kappa\lambda_n^2+\left.\frac{\partial H}{\partial T}\right|_{T_0}}{\rho c_p}t\right)\cos(\lambda_n x) \tag{46}$$

where λ_n, n = 1, 2, 3 $\cdots$ with $0 < \lambda_1 < \lambda_2 < \lambda_3$ ...are eigenvalues of equation

$$\left(\lambda_n^2\kappa^2 - h^2\right)\sin\lambda_n L - 2\lambda_n\kappa h\cos\lambda_n L = 0 \tag{47}$$

where L is the dimension in the main direction of heat transfer which is the thickness of a semiconductor chip. Eq. (45) requires that

$$\lambda_1 \geq \sqrt{\frac{1}{\kappa}\left(\frac{\partial H}{\partial T}\right)\Big|_{T_0}} \tag{48}$$

Numerical study of (47) and (48) shows that for a self-heating semiconductor chip with a

certain thickness L, there is a *threshold* temperature T_{crit}, at which a chip switches from a stable thermal state to unstable thermal state. Fig. 7 shows the *threshold* temperature as a function of thickness of a diode, with a current density of 25A/cm^2 and a forward bias of 0.5548 V. H_0 is approximated by a conventional p-n junction model. Fig. 8 shows the development with time of an unstable temperature disturbance and a stable one at the center x=0. A schematics of one dimensional structure is illustrated in Fig. 9.

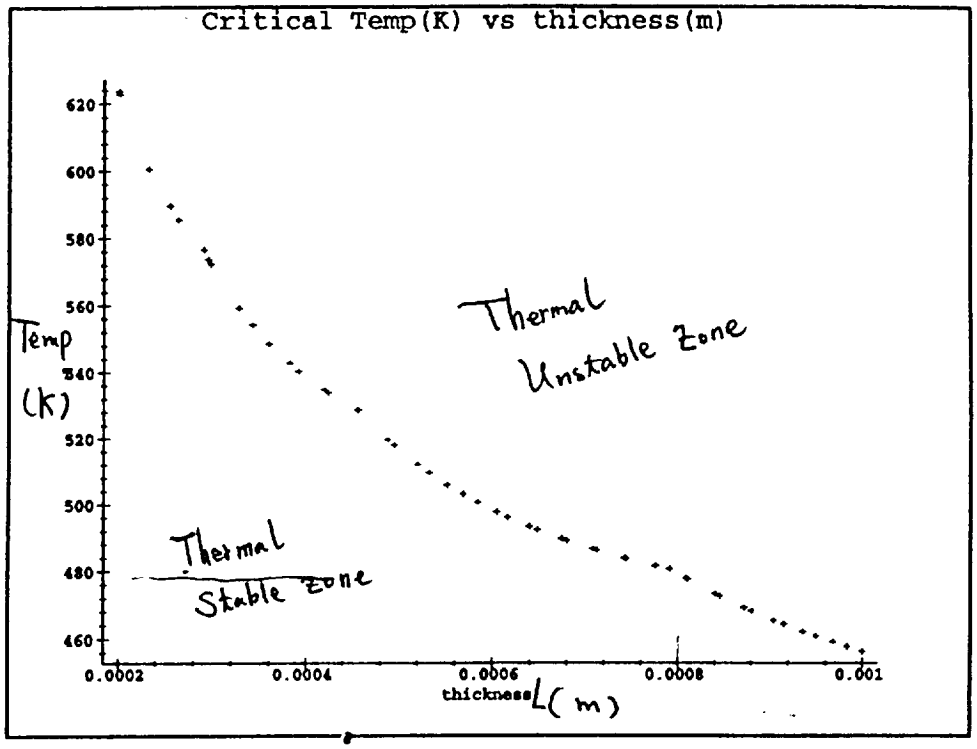

Fig. 7. Threshold temperature as a function of thickness

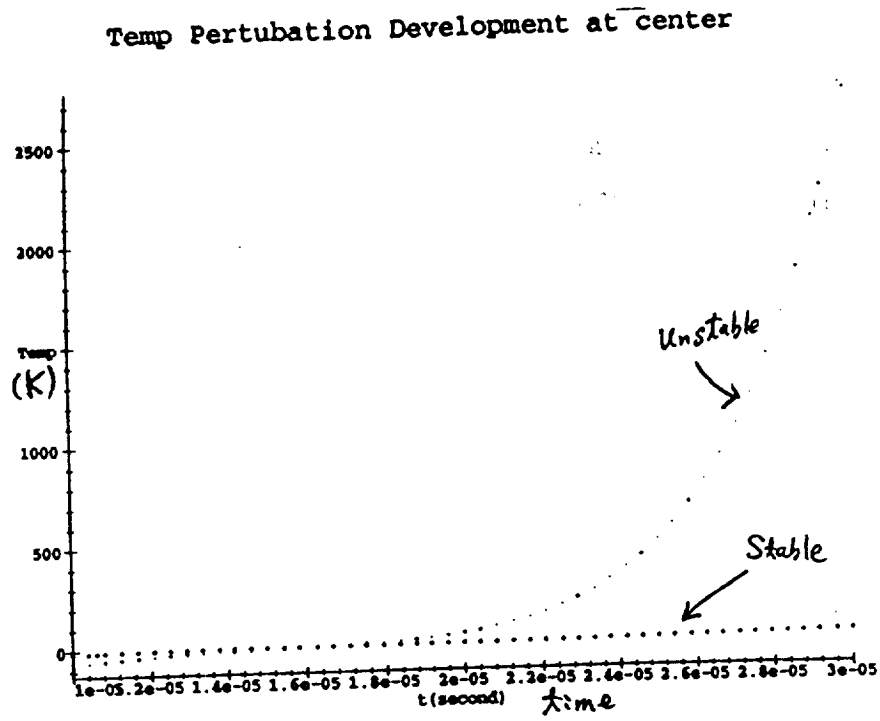

Fig. 8. Temperature disturbance development with time

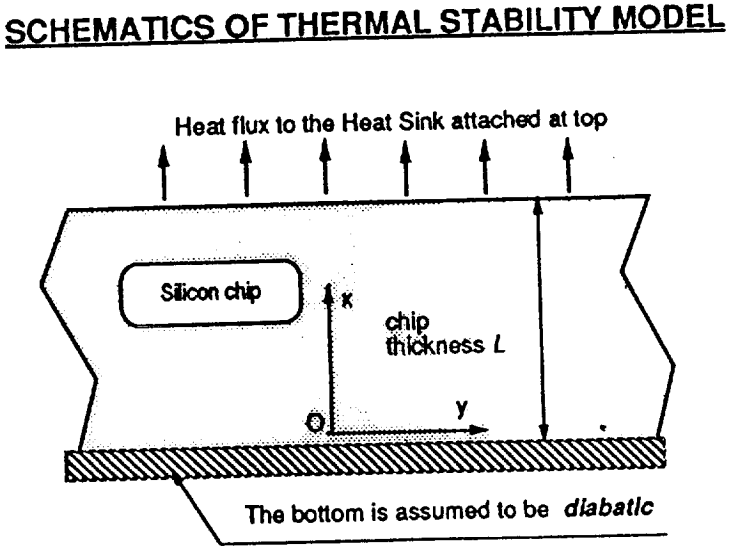

Fig. 9. Schematic of thermal stability model

Device Level Simulation Results

A power semiconductor switching device (BJT) was chosen as a representative device for device and chip level thermal simulations. Fig. 10 is a snapshot of the opened device. The multi-chip and multi-layer structure is schematically shown in Fig. 11. The dimension of the package is $63mm \times 109mm \times 15mm$.

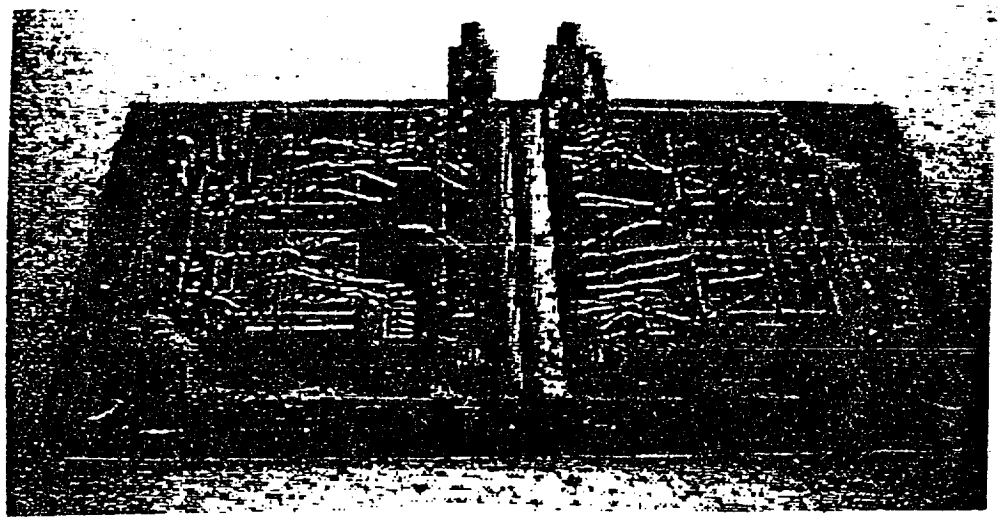

Fig. 10. Snapshot of the opened device

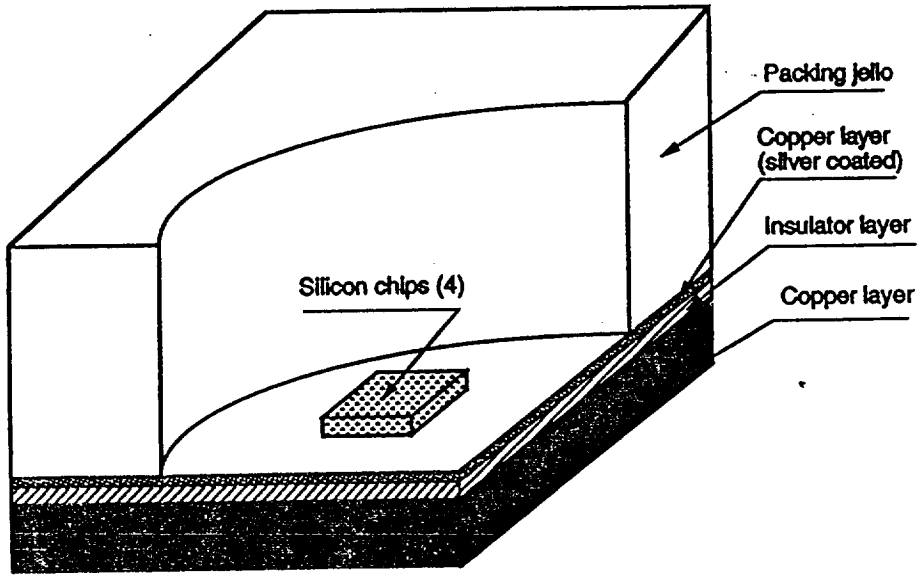

Fig. 11. Schematics of device model

Typically, at the bottom there is a pure copper layer 5 mm thick which serves as a heat spreader. In this example, calculation of the flow field around the heat sink was not included. Instead, a typical heat transfer coefficient was used. Beyond the copper layer, there is a ceramic electrical insulation layer of 2 mm thickness with thermal conductivity of *16W/mK*. Above the insulation layer, a 1.5 mm thick layer of copper, coated with silver serves as an electric connector of collectors, for the four chip modules. Four chips sit on this layer. The remaining volume is filled by protection Jello with a low thermal conductivity.

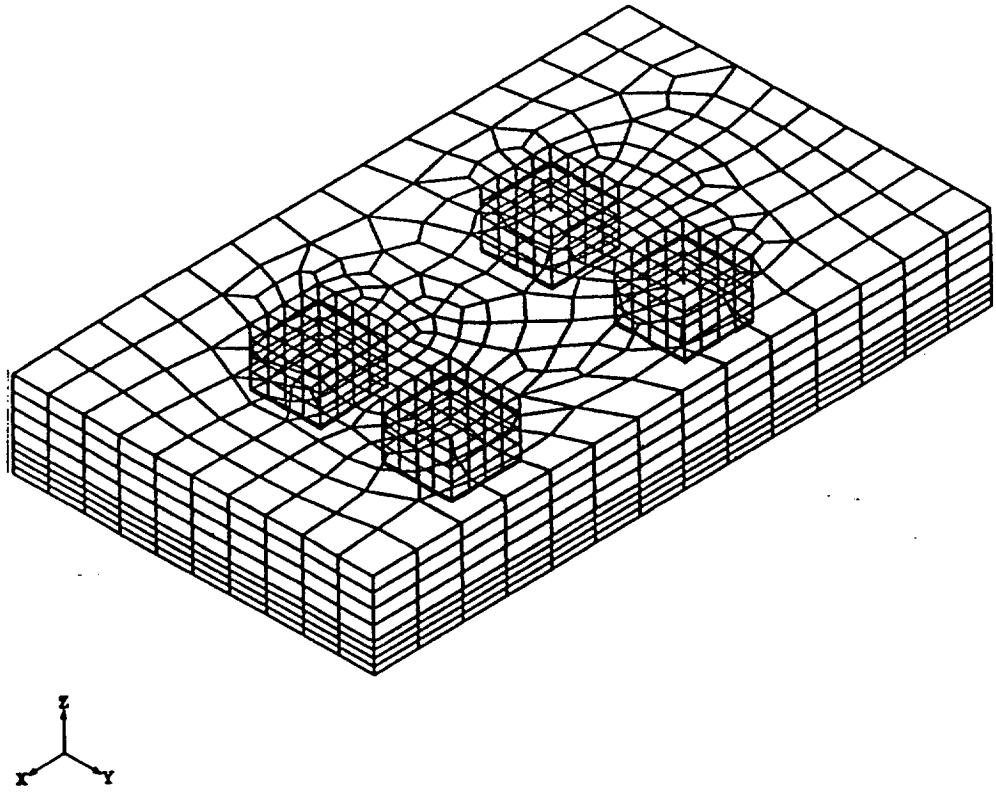

Fig. 12 (a). Meshing for device simulation

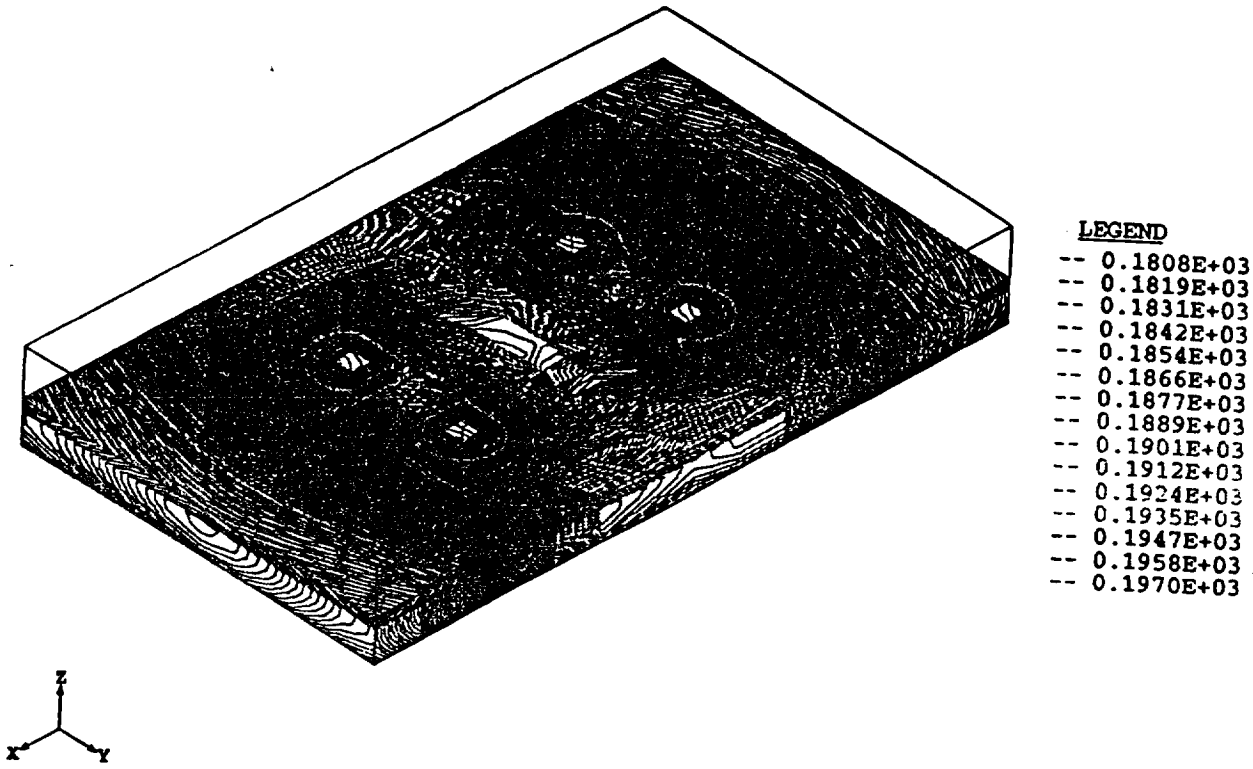

Fig. 12 (b). Device sim. -- temp. distr. through top of chips

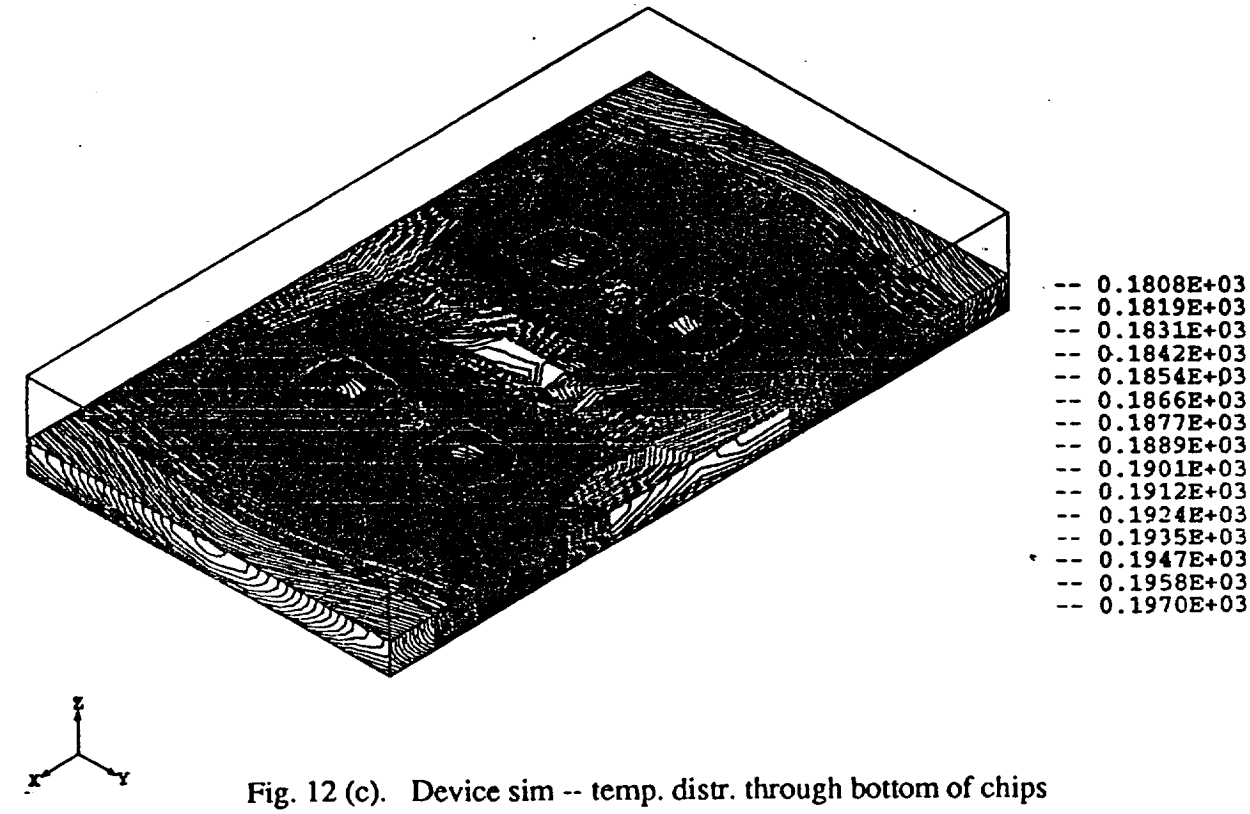

Fig. 12 (c). Device sim -- temp. distr. through bottom of chips

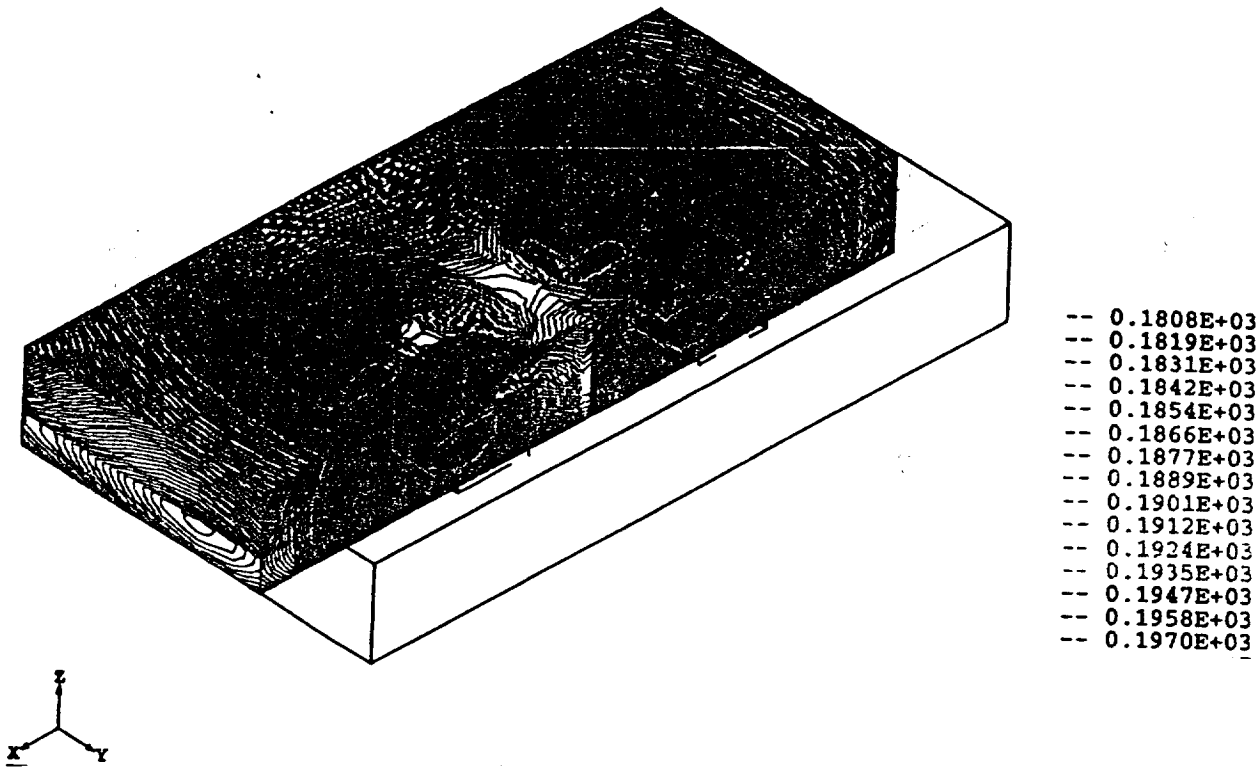

Fig. 12 (d). Device sim -- temp distr at x-z plane through center of chips

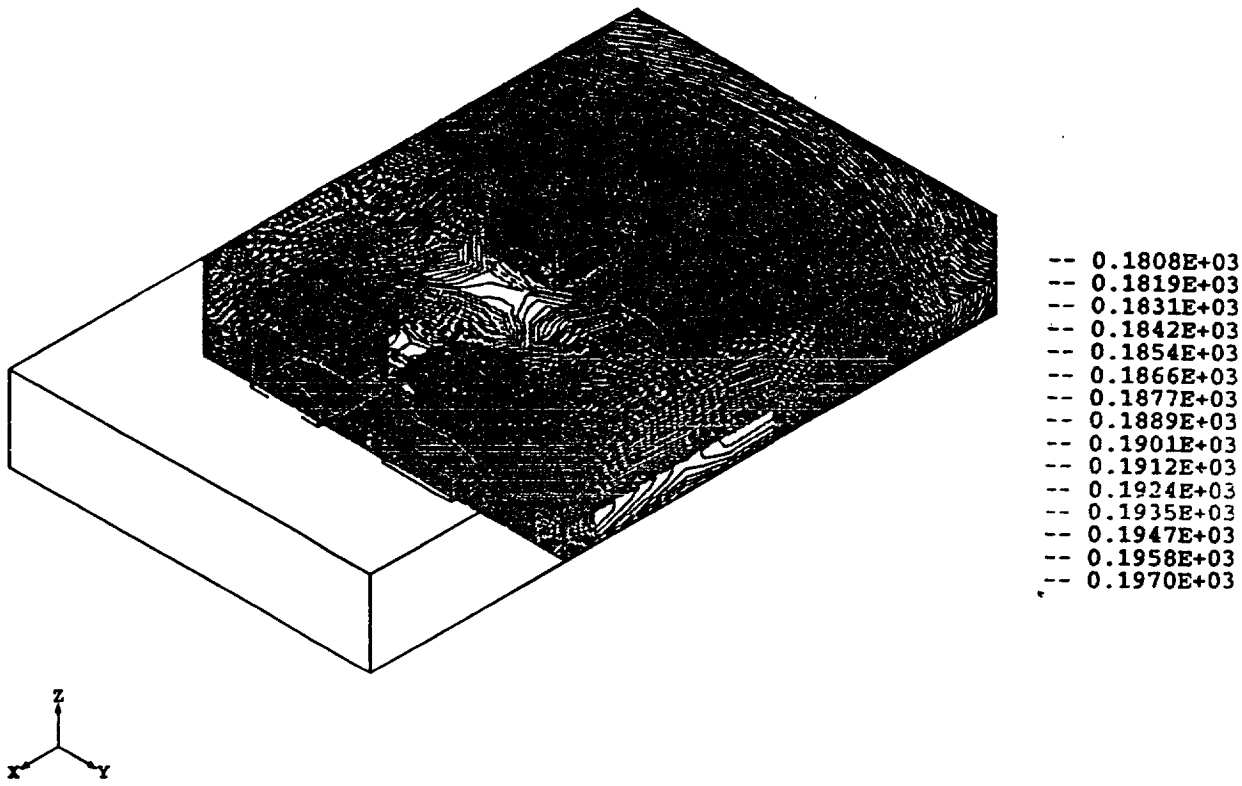

Fig. 12 (e). Device sim -- temp distr at y-z plane through center of chips

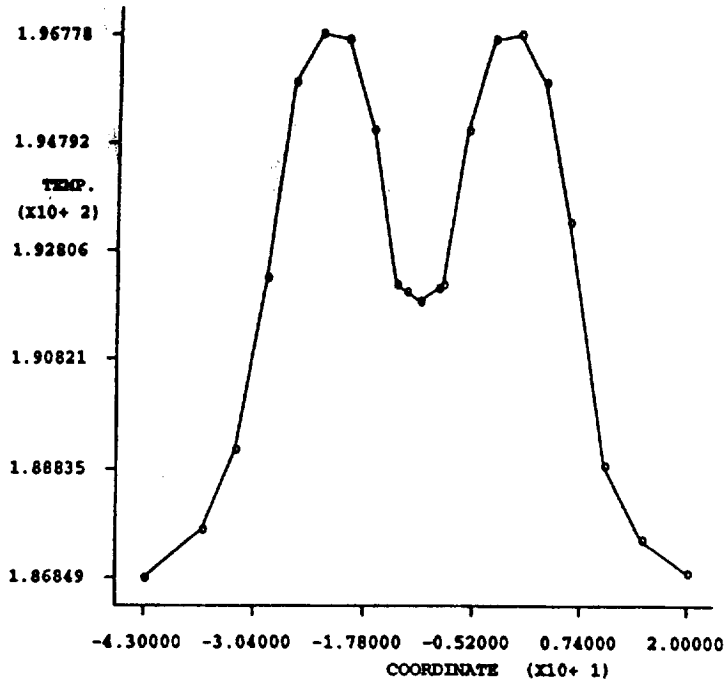

Fig. 12 (f). Device sim -- temp distr at center of chips (y dir.)

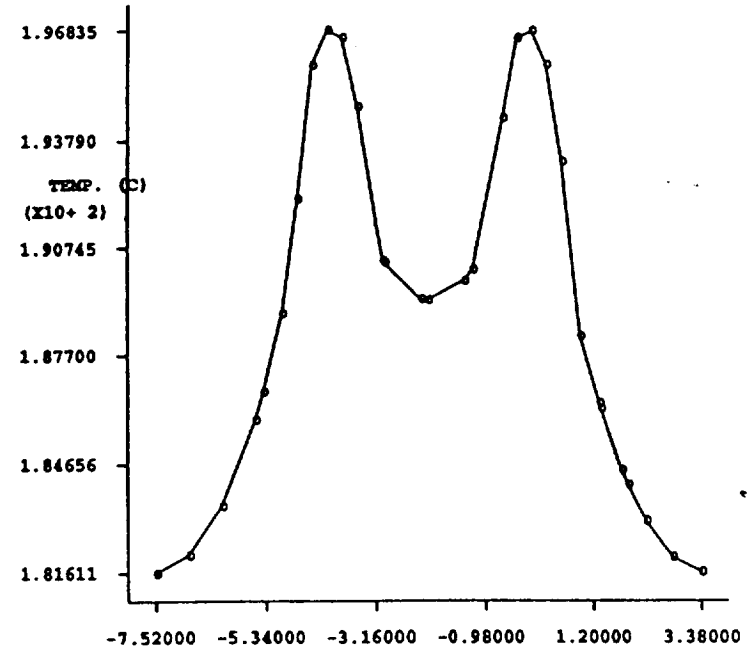

Fig. 12 (g). Device sim -- temp distr at center of chips (x dir.)

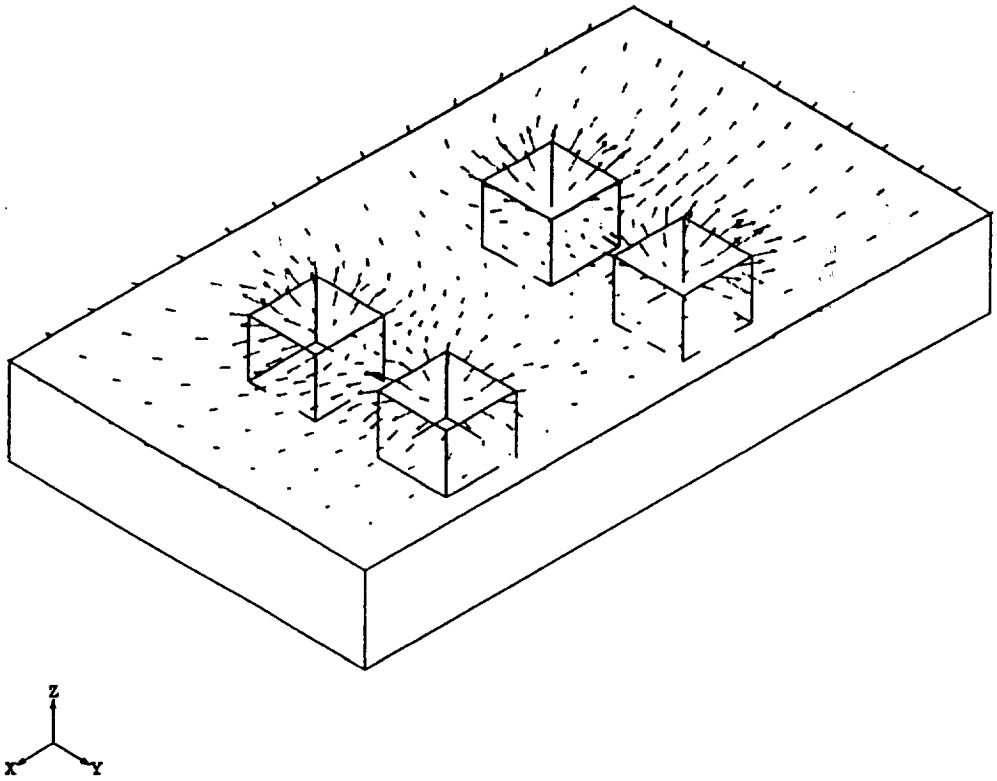

Fig. 12 (h). Device sim -- heat flux through the top surface

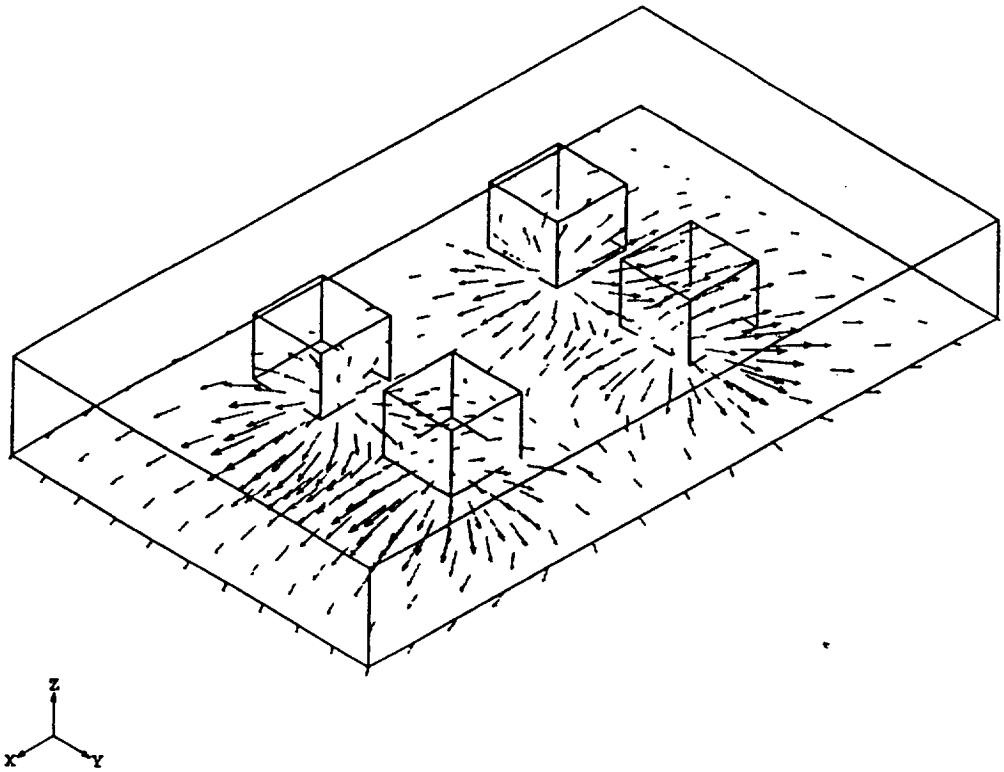

Fig. 12 (i). Device sim -- heat flux through the bottom surface

Most of the heat transfer occurs through the bottom. The top and four sides have a natural convective boundary condition, with h having a typical value of $10W/m^{2o}C$. Figures 12(b) and 12(c) show temperature contours at cross section parallel to bottom at different heights, cutting through copper, insulation layers and chips respectively. Figs. 12 (a) to (i) show some results of the device temperature distribution. As expected the highest temperature is located approximately around the center of each semiconductor chip where heat is generated. The maximum temperature difference is between the bottom of the chip and the copper plate which is 17.5 C for a h of $249.5 \, W/m^2C$ An undesirable overlapping of high temperature regions is observed in the y-direction. (Fig. 12(c,d)) Enlarging the distance in this direction might reduce this interaction. Figs. 12(f) and 12(g) show temperature contours on sections through the center of a chip in x and y directions, respectively. Heat flux vectors through the bottom, sides, and top are shown in Figs. 12(h) and 12(i), respectively.

Chip Scale Simulation Results

As shown in Fig.13, one of the four chips in this device contains monlithic, 3-level, Darlington Structure, with multi-finger shaped emitters of lower level transistor shorted to the bases of upper level transistors. The current density in the third level transistor's emitter region is about β^2 times that of the current density in the first level transistor's emitter region, where β , current gain, has a typical value from 5 to 10 (7.0 in this simulation). At about the same bias, the heat dissipation rate at the third level transistor's emitter region is about 50 times that of the first level transistor's emitter region. This example shows that heat dissipation in a semiconductor chip can be highly localized and a three dimensional chip level simulation is necessary.

SCHEMATICS OF CHIP MODEL

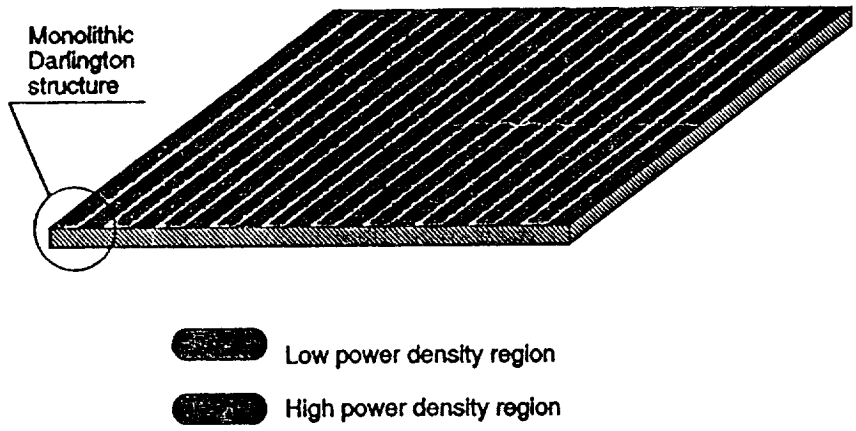

Fig. 13. Schematic of chip modeling

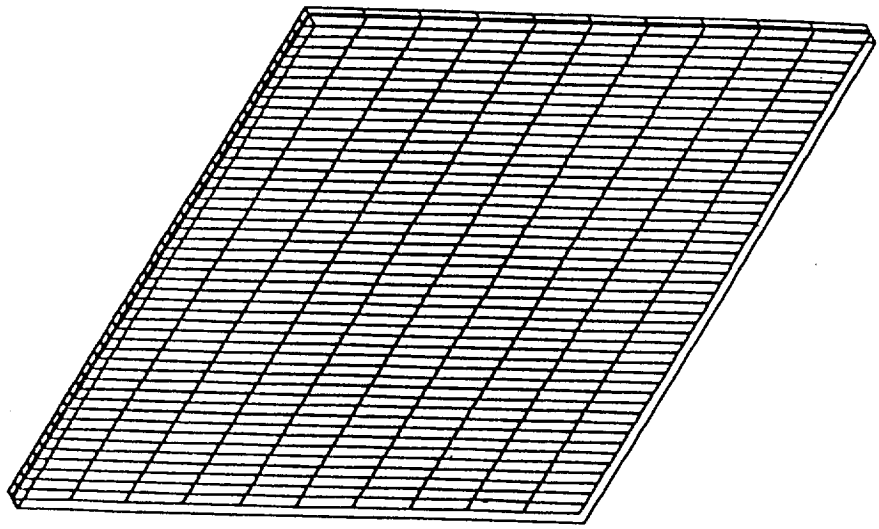

Fig. 14(a). Meshing for chip simulation

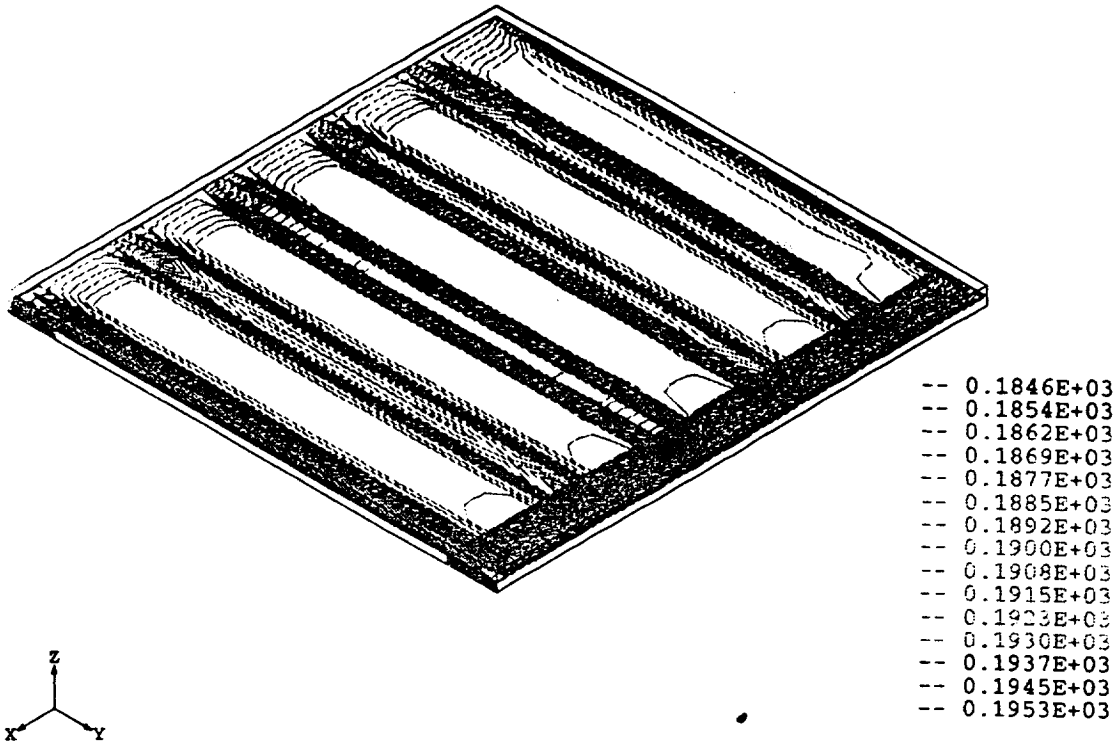

Fig. 14(b) Chip sim. -- Temp. distr. through the center of thickness

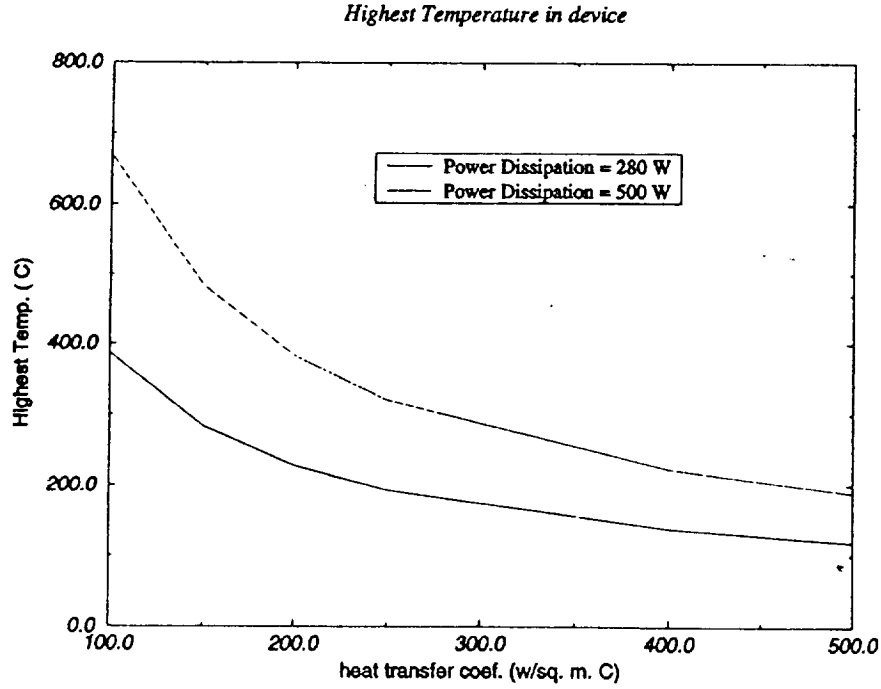

Fig. 15. Device sim. -- peak temp. as a function of heat transfer coef. *h*

Fig. 15. Device sim. -- peak temp. as a function of heat transfer coef. h

Fig. 14(b) shows the resulting temperature field within one chip area containing 5 "fingers". Periodical boundary conditions were used at the boundaries. In Fig. 14(b) long, narrow-banded, high temperature regions correspond to the multi-finger emitter regions. The maximum temperature difference is over $11^{\circ}C$ in the chip. It is noted that the contour lines are quite dense around the interface regions for low and high heat dissipation rates, implying an increased heat transfer, while around the central part of high power regions, there is a substantial decrease in heat transfer.

Junction Scale Simulation Results

A BJT structures was numerically studied in a coupled electro-thermal simulation. The schematic of the structure is in Fig. 16. Figs. 17(a).to (c).show the current density, potential and temperature distribution results respectively.

Future Works Outline

- Implement the iteration procedure suggested. Communication between the thermal and electrical simulations
- Parametric study for different layout design in each level
- Transient response
- Hot spots
- Current-induced thermal runaway (2D thermal stability)

SCHEMATICS OF POWER BJT

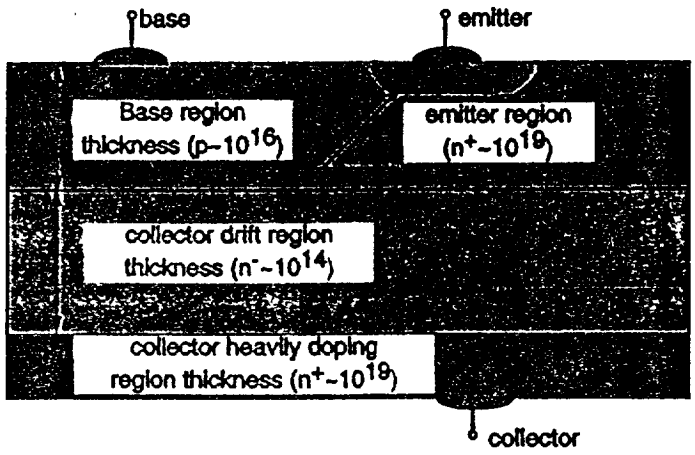

Fig. 16 Schematic of Power BJT

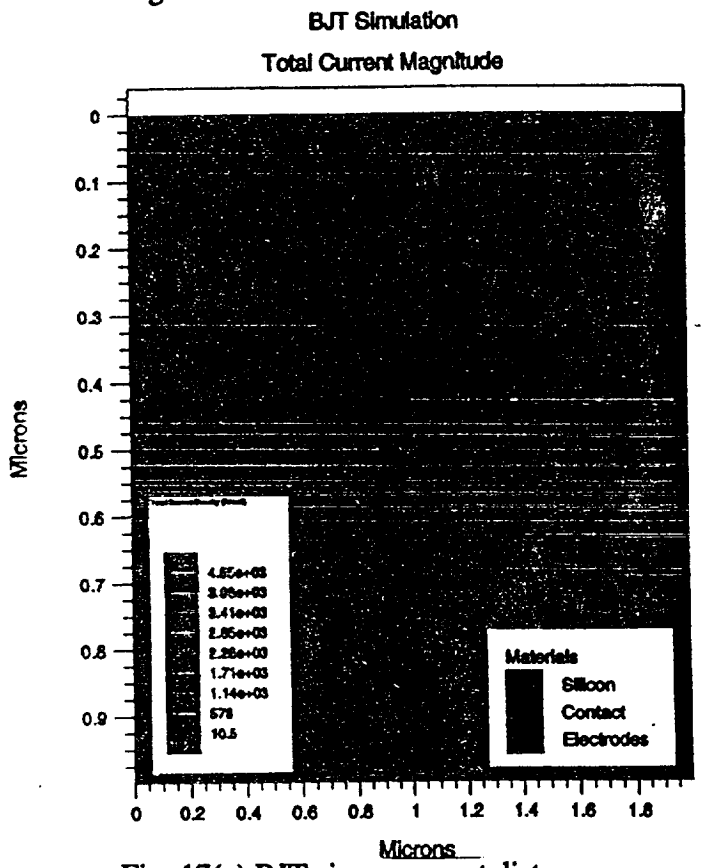

Fig. 17(a) BJT sim -- current distr.

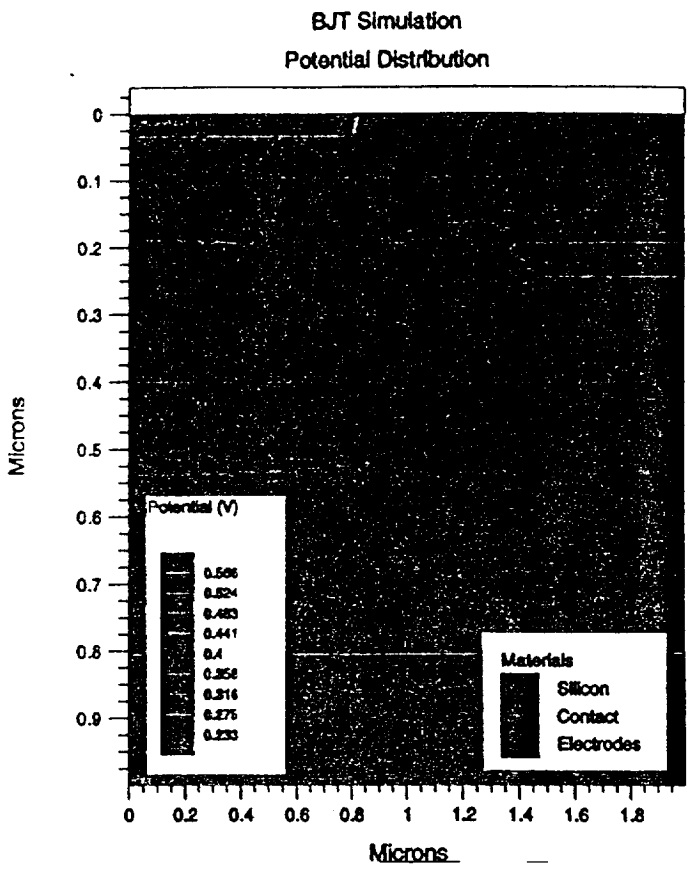

Fig. 17(b). BJT sim -- potential distr.

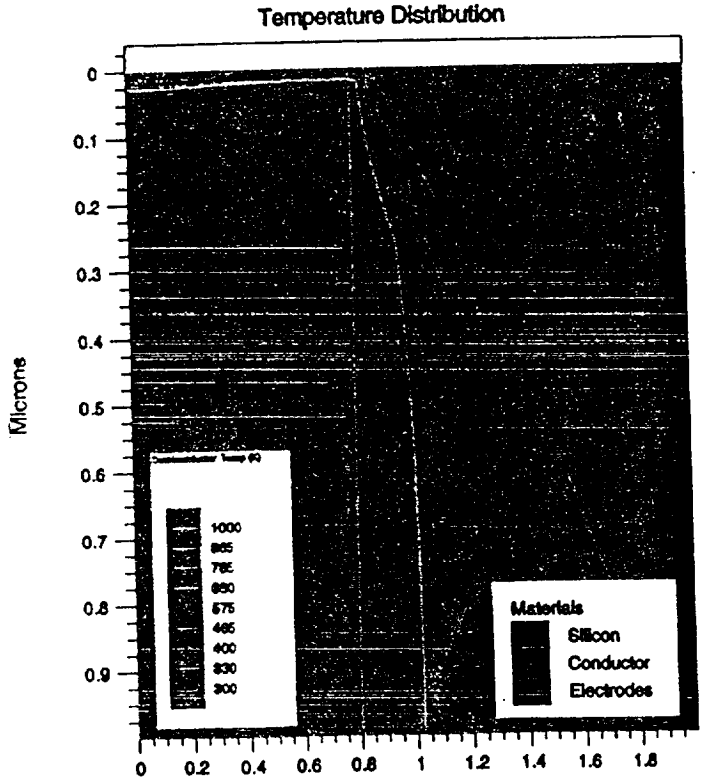

Fig. 17(c). BJT sim -- temperature distr.

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