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Final Report
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ADVANCED WATER VAPOR LIDAR DETECTION SYSTEM

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to

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1 INTRODUCTION

In the present water vapor lidar system, the detected signal is sent over long cables to a waveform digitizer in a CAMAC crate. This has the disadvantage of transmitting analog signals for a relatively long distance, which is subjected to pickup noise, leading to a decrease in the signal to noise ratio.[1][2]

Generally, errors in the measurement of water vapor with the DIAL method arise from both random and systematic sources. Systematic errors in DIAL measurements are caused by both atmospheric and instrumentation effects. The selection of the on-line alexandrite laser with a narrow linewidth, suitable intensity and high spectral purity, and its operation at the center of the water vapor lines, ensures minimum influence in the DIAL measurement that are caused by the laser spectral distribution and avoid system overloads.

Random errors are caused by noise in the detected signal. Variability of the photon statistics in the lidar return signal, noise resulting from detector dark current, and noise in the background signal are the main sources of random error. This type of error can be minimized by maximizing the signal to noise ratio. The increase in the signal to noise ratio can be achieved by several ways. One way is to increase the laser pulse energy, by increasing its amplitude or the pulse repetition rate. Another way, is to use a detector system with higher quantum efficiency and lower noise, on the other hand, the selection of a narrow band optical filter that rejects most of the day background light and retains high optical efficiency is an important issue. Following acquisition of the lidar data, we minimize random errors in the DIAL measurement by averaging the data, but this will result in the reduction of the vertical and horizontal resolutions. Thus, a trade off is necessary to achieve a balance between the spatial resolution and the measurement precision.[3]

Therefore, the main goal of this research effort is to increase the signal to noise ratio by a factor of 10 over the current system, using a newly evaluated, very low noise avalanche photo diode detector and constructing a 10 MHz waveform digitizer which will replace the current CAMAC system.[4]
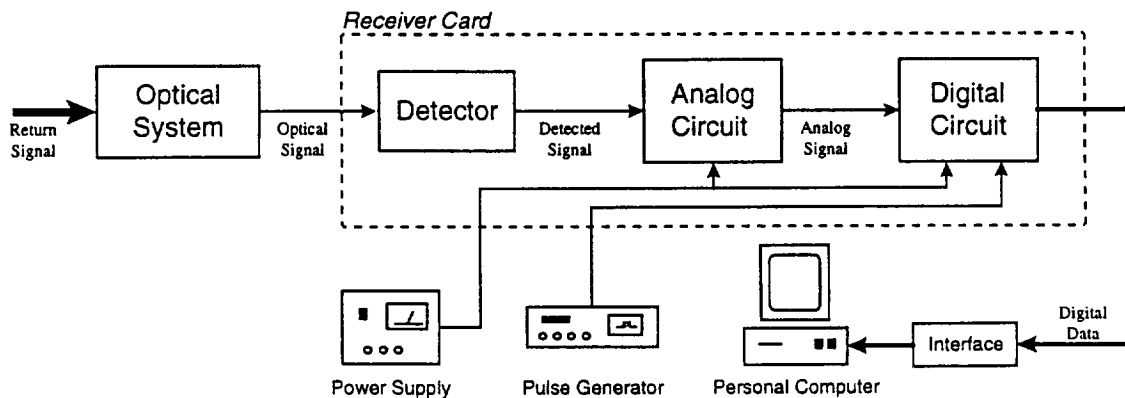

Fig.1 Developed DIAL receiver system.

The proposed DIAL receiver system is shown schematically in Fig.1. For the first time, it is planed to place the whole electronic and digital circuits on one small sized, light weight receiver card, which will include the detection and the digitization sections, to be placed directly on the receiver telescope. This scheme has the advantage of transmitting digital data, to be stored and analyzed on a personal computer.

In the optical system, a telescope is used to collect and focus the lidar return signal into a small area, compatible with the detector area. An avalanche photo diode will be used for the detection due to its ideal response for the water vapor band of interest. The detected signal will be applied to an analog circuit, which will include a signal conditioning stage. This stage is used for signal buffering and amplification and the summation of marker and dither inputs. Also it will be used for signal clipping and filtering for overload protection and noise reduction. On the other hand, this stage will provide the detector with a stable high voltage bias and control its temperature.

Finally, the analog signal will be applied to a digital circuit to be digitized, processed and temporarily stored. This circuit is compatible with a parallel input output computer interface for final data storage and display and provide monitoring for the detector high voltage bias and temperature.[2]

In the following sections, the steps carried out in the past year is discussed in more details.

2 ANALOG CUIRUCIT

The analog circuit, as shown schematically in Fig. 2, is designed to control the operation of the APD. The laser return signal will be focused into 0.5 mm diameter optical signal, and will be aligned with the APD sensitive area. The APD detected signal will be applied to a signal conditioning stage. This stage consists of three substages. The first, is a summer and buffer amplifier, designed to apply an additional gain to the detected signal in order to achieve a 2 Volt peak to peak maximum value, which is compatible with the digitizer. On the other hand, a marker and dither signals will be added to it. The marker signal is used as a mark for the beginning of the useful data, while the dither is used to add low level sinusoidal signal to dither the detected signal through the digitizer for better performance. For its ideal characteristics, an operational amplifier will be used in this stage. The operational amplifier choice was made upon characterizing a group of them in order minimize its effect on the detected signal, specially during overload recovery time and the system bandwidth.
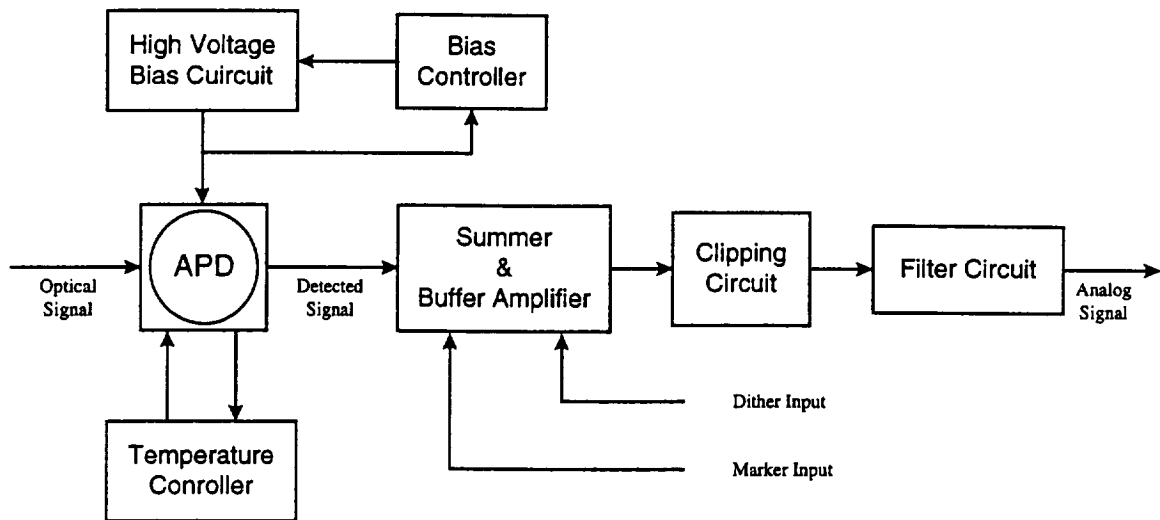
Fig. 2 Schematic diagram for the analog circuit.

In an actual DIAL application, the laser signal might hit a large amount of water vapor such as a cloud, which will lead to the system overload and saturation, producing the overload recovery time delay, which will be mainly due to the APD and the analog to digital converter. Thus, the clipping circuit will be used to clip the signal insuring it maximum peak to peak value is around 2 Volt. For non-overload signal, the clipping circuit will act as a voltage follower amplifier.

Finally, the signal will be applied to a three pole, low-pass, passive Bessell filter, with a 2.5 MHz -3dB cutoff frequency. This filter will limit the system bandwidth in order to reduce the noise, and restrict the signal frequency according to Nyquist Criterion.

The detector high voltage bias is obtained using a high voltage module. Since the APD responsivity, and consequently its output, is a strong function of its voltage bias and temperature, two proportional integral (PI)controllers had been used. The voltage controller can be adjusted manually to apply constant bias to the APD ranging from a maximum value of 10% lower than its breakdown voltage to a minimum value of 30% lower than is normal operating voltage. While the temperature controller setting point is fixed and is adjusted to operate the detector near 0 °C.

A primarily card was built to accomplish this design. The initial testing of the card showed an excellent performance of the APD with the analog circuit. The testing procedures starts with the high voltage controller by measuring its output. The value of the bias voltage is completely controllable form half the APD operating voltage up to 20% higher. The second step is to test the performance of the temperature controller. This controller is capable of cooling down the detector to 0 °C at an ambient temperature up to 40 °C provided that a sufficient heat sinking is used. Finally, the signal conditioning stage was tested to check its linearity. The gain variation along this stage was found to be less than 0.02%. On the other hand, it was concluded that switching places of the buffer and clipping amplifier is very recommended, in order to protect the buffer form overload as well.

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3 DIGITAL CUIRUCIT

The digital circuit will be designed mainly to operate as a waveform digitizer, and it can perform some simple data processing, such as averaging and housekeeping. The main function of the waveform digitizer is to convert the analog signal, representing the detector output, into a digital form that is compatible with a simple personal computer interface. Fig.3 shows a schematic diagram for the main components of the digital circuit.
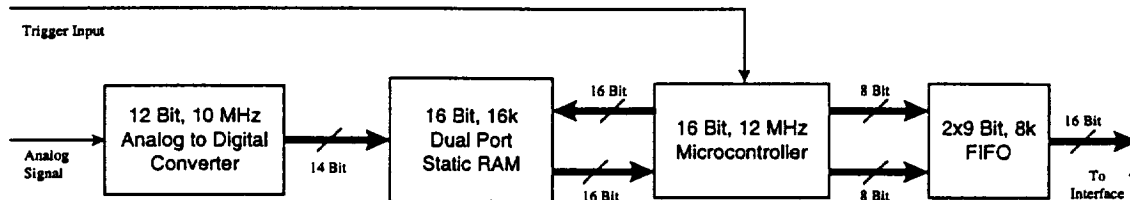

Fig.3 Schematic Diagram for the digital circuit.

The analog signal will be applied to a 14 bit, 10 MHz analog to digital converter. The digital data will be stored in the lower half of a 16k, 16 bit, dual port static RAM, equivalent to 819.2 µs time window. The static RAM is connected to a 16 bit, 12 MHz microcontroller, which will transfer the data to the upper half of the RAM for the averaging purpose. The final averaged data will be split and sent to two 8k, 9 bit FIFO to be collected by a personal computer via a discrete input output interface.

Approximately 400µs before the DIAL laser fires, it generates a trigger pulse called the precursor that informs the other subsystems that the laser is about to fire. This precursor signal is sensed by the microcontroller, by a hardware interrupt, and helps as a trigger signal in order to synchronize the system.

3-1 Data Collection and Storage Section

The first section of the digital card is the data collection and storage section, or the digitizer section. A schematic diagram of this section is shown in Fig.4. The analog signal is applied to a 14 bit, 10 MHz analog to digital converter, with lower and upper voltage limits of 0 and 2 Volt respectively. The output data is stored in a dual port, static RAM. The storage location of each word of the output data is pointed out using a 13 bit counter. A 10MHz clock signal synchronize all of these three circuits. On the other hand, the digitizer is synchronized with the hole system by control signals connected directly to the microcontroller.

The analog to digital converter is continuously converting the input analog signal into a digital form. But only the useful data will be stored in the RAM. At the beginning of the each cycle, the microcontroller sends a clear signal to the counter, addressing the first memory location in the RAM. When the microcontroller sense the trigger signal, it sends a start signal to the counter,

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addressing successively the other memory locations. When the counter finishes scanning half the RAM, it sends a feedback signal to the microcontroller indicating the end of the digitization.
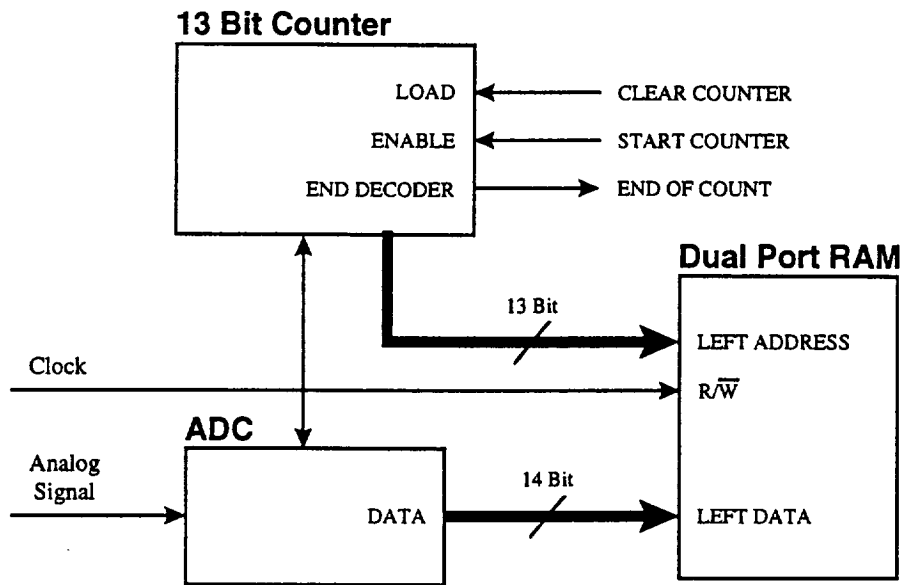
13 Bit Counter

Fig. 4 Schematic diagram of the data collect and store section.

3-2 RAM - Microcontroller Section

When the digitizer sets the end of count signal, the microcontroller starts to transfer the data from the lower portion of the RAM to its upper portion. Fig.5 shows a schematic for the microcontroller RAM connection. This data transfer data is allowed for the averaging purpose, with a maximum of four average waveforms.
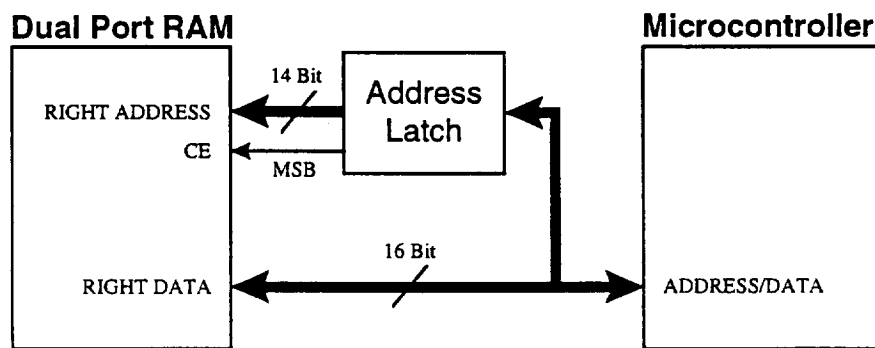

Fig. 5 Schematic diagram of the RAM - microcontroller section.

The significant advantage of the dual port RAM is its separation of the digitizer section, on its left port, from the microcontroller on its right port, which allows the microcontroller to operate at a higher 12 MHz frequency using a local crystal

oscillator, for faster data handling. Consequently, the on chip 8 bit, four channel analog to digital converter will be used for sensing the APD temperature and bias voltage. Fig.6 shows the memory map of the system. The memory section, starting with the nibble 7, is used to address the FIFO as it will be discussed in the output section. While the memory section starting with the nibble 6 is reserved for the control word, set by an on board dip switches, used to define the averaging and record lengths.

3FFFH		FFFFH
	ADC Output Data Storage	
2000H		C000H
1FFFH		BFFFH
	Data Averaging	
0000H		8000H
	FIFO	7FFFH
		7000H
	Control Word	6FFFH
		6000H
	NOT USED	5FFFH
		4000H
	Internal Program Storage EPROM	3FFFH
		2080H
	NOT USED	
	Register File	00FFH
		0000H

Fig.6 System memory map.

3-3 Output Section

Fig.7 shows the output section of the digital card. After finishing the averaging, the averaged data will be sent by the microcontroller from the lower half of the RAM to the FIFO, ready to be transferred to a personal computer. Once again, the FIFO has the advantage of the separation between the 12 MHz microcontroller circuit from the computer interface card, which can be operated at a frequency as low as 300 kHz.
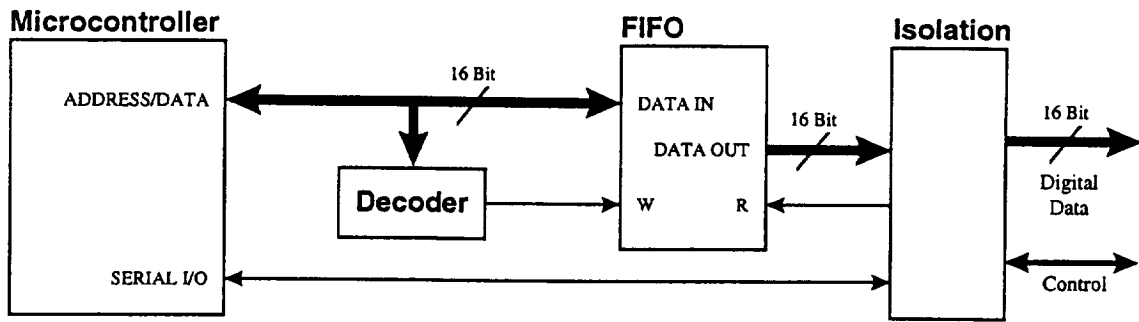
Fig.7 Schematic diagram of the output stage.

The FIFO read operation is fully controlled by the computer interface via a read command. On the other hand, serial communication, directly between the microcontroller and the interface, allows to collect the housekeeping data indicating the actual APD temperature and voltage bias. Finally, optocouplers are used for the purpose of ground isolation between the digital card and the computer interface.

A 12 bit test digital circuit was constructed and operated and the initial testing indicates an acceptable performance. The computer interface used for reading the parallel data was a 24 bit discrete input output card. The final digital board will have a 14 bit digitizer. The digital circuit primary testing were performed as follows.

• First, the communication between the different memory locations and the microcontroller was performed successfully for both read and write operations.

• Second, the counter operation was tested in order to scan half the static RAM. Its operation is fully controlled by the microcontroller.

• Next, the digitizer operation was successfully tested at a digitization rate of 10 MHz. The output data was stored in the successive memory locations of the RAM.

• Finally, the communication between the FIFOs and a personal computer was performed.

Although the testing of each individual section of the digital circuit was performed successfully, additional performance testing for the whole system is needed, including the design of an operational code for the final card.

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This report summarizes work done by Tamer Refaat as an ODU graduate student conducting experiments at NASA Langley in collaboration with the Atmospheric Science Division.