

GSFC Cutting Edge Avionics Technologies for Spacecraft

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Abstract— With the launch of NASA's first fiber optic bus on SAMPEX in 1992, GSFC has ushered in an era of new technology development and insertion into flight programs. Predating such programs the Lewis and Clark missions and the New Millennium Program, GSFC has spearheaded the drive to use cutting edge technologies on spacecraft for three reasons: to enable next generation Space and Earth Science, to shorten spacecraft development schedules, and to reduce the cost of NASA missions.

The technologies developed have addressed three focus areas: standard interface components, high performance processing, and high-density packaging techniques enabling lower cost systems. To realize the benefits of standard interface components GSFC has developed and utilized radiation hardened/tolerant devices such as PCI target ASICs, Parallel Fiber Optic Data Bus terminals, MIL-STD-1773 and AS1773 transceivers, and Essential Services Node. High performance processing has been the focus of the Mongoose I and Mongoose V rad-hard 32-bit processor programs as well as the SMEX-Lite Computation Hub. High-density packaging techniques have resulted in 3-D stack DRAM packages and Chip-On-Board processes. Lower cost systems have been demonstrated by judiciously using all of our technology developments to enable "plug and play" scalable architectures.

The paper will present a survey of development and insertion experiences for the above technologies, as well as future plans to enable more "better, faster, cheaper" spacecraft. Details of ongoing GSFC programs such as Ultra-Low Power electronics, Rad-Hard FPGAs, PCI master ASICs, and Next Generation Mongoose processors.

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1. INTRODUCTION

The advanced technology components developed by GSFC have all in some way increased the capability of the spacecraft and enabled cutting edge science missions. Moreover, each technology has contributed to lowering the cost of the mission, enabling more missions within budget constraints.

Some of the GSFC technologies described herein are to address a specific need, such as higher processing performance, expressed in MIPS which is directly traceable to mission requirements. Many others have been developed using overall program goals such as lower weight and lower power avionics. This type of development actually predates flight project requirements and enables projects not yet started.

In some cases the cost reduction has been easy to demonstrate such as electronics size and weight reductions and dollar per pound measures. In many others the cost reductions are very difficult to measure such as shorter integration and test times, or problems avoided.

Technology transfer to industry has been a very large focus

in the development of avionics for spacecraft. The technologies described have not been "transferred" to industry, they were developed by industry, under contract to GSFC, to meet NASA requirements for "better, faster, cheaper" spacecraft. In this way there is no learning curve for the commercial entity, as they were part of the development from the beginning. Therefore, GSFC maintains their focus on the next cutting edge technology, and the industry member is available to focus on offering the product and services developed.

2. FIBER OPTIC BUSES

GSFC has used fiber optic busses on several spacecraft including SAMPEX, XTE, TRMM, HST, MAP, and EO-1. Fiber optic busses have several advantages over their electrical equivalents such as lower weight, safer integration, simpler grounding, and fewer EMI/EMC concerns. Fiber optics at GSFC has been an evolving science, and a learning experience. Several different devices have been developed for GSFC, others have been developed independently and have been integrated onto GSFC spacecraft.

GSFC's involvement in the use of fiber optic busses began with SAMPEX, the first flight of NASA's Small Explorer Program, which implemented a MIL-STD-1773 command and control bus using 850 nm wavelength light to communicate between the spacecraft computers and subsystems. The MIL-STD-1773 bus is a fiber optic implementation of the MIL-STD-1553 bus, using the same protocols at the same 1 MHz bit rate on a different physical medium. The fiber optic transceiver, known as the Small Explorer Data System (SEDS) Terminal was developed by SCI of Huntsville, AL. The SEDS terminal (or SEDS I terminal as it was later called) incorporates the fiber optic receivers and transmitters as well as a custom ASIC that converts the bi-level light levels to the tri-level electrical levels allowing the use of available MIL-STD-1553 protocol chips from UTMC and DDC.

The MIL-STD-1773 bus uses a passive star topology, with the star coupler housed separately. SAMPEX nominal bus data rate is 20 kbits/s, well under the 200-400 kbit/s capability. SAMPEX launched in 1992 and continues to operate nominally. [1]

Three separate MIL-STD-1773 busses were implemented for the XTE mission, one for instrument traffic, one for attitude control traffic and the third for the remainder of the spacecraft subsystem communication. In certain subsystems, those using the UTMC UT1553 BCRTM protocol chip, the SEDS terminal was replaced with a smaller subset of the terminal, namely the Honeywell fiber optic transmitters and receivers themselves, eliminating the custom ASIC and greatly reducing board space used by the

fiber optic interface. The second major change to the bus was the reduction in size of the star coupler by approximately one-third. This was accomplished by using a MIL-C-38999-type connector, with 16 fiber optic termini per connector. The TRMM bus implementation was roughly equivalent to the XTE system, the only notable change being the incorporation of a newer generation SEDS II terminal into several subsystems. The SEDS II terminal was developed for GSFC by SCI to occupy the same footprint and pinout as a MIL-STD-1553 transceiver, in order to reduce the impact of fiber optic bus incorporation into existing designs. XTE was launched in December 1995 and continues to operate nominally. TRMM was launched in November 1997 and continues to operate nominally. [2]

An ongoing development at GSFC to support many different programs in need of a slightly higher bandwidth bus while retaining the advantages of standard communications is in the area of components and techniques using the AS1773 bus. The AS1773 bus implements both 1 and 20 MHz bit rate communications using the same protocols at MIL-STD-1773, while dynamically switching between the two rates. GSFC joined the UNM Microelectronics Research Center, SCI and Teledyne in developing a 1300 nm "dual rate" transceiver for use on spacecraft. GSFC has designed and developed an in-situ bit error rate test for the Boeing DR1773A for the Microelectronics Photonic Test Bed (MPTB). The Boeing transceivers will be used (at the 1 MHz bit rate) on the Medium Explorers Microwave Anisotropy Probe (MAP) mission, to be launched in the Fall 2000. [3]

Another development at GSFC to support the very high data rate of upcoming missions is the development and qualification of components and techniques to implement a 1 GHz bit rate IEEE P1393 or Serial Fiber Optic Data Bus (SFODB). Combining an earlier effort with an ongoing NASA Small Business Initiative in Research (SBIR) contract with Optical Networks Inc (ONI) has resulted in an implementation that uses parallel fiber optic receivers, transmitters and ribbon cable to implement the bus. This development is ongoing under the New Millennium Program and will demonstrate flight quality components in Fall 1998. [4]

The major advantages of using fiber optic busses vs. conventional electrical equivalents include ease of integration, fewer electromagnetic interference and compatibility (EMI/EMC) concerns and less weight. Ease of integration is enabled by the nature of "safe" integration of fiber optics. Where conventional electrical systems must undergo many safe-to-mate checks to ensure that no box is damaged during integration, fiber optics allow plug and play with no risk of damage due to short circuits, ground loops, and incorrect pinouts. Fewer EMI/EMC concerns is

primarily due to the nature of the fiber optic cable, negating the need for shielding, grounding and attention to cable routing to avoid interference. Lower weight can be realized by using almost any standard bus, however the weight of fiber optic cable compared to it's shielded twisted pair equivalent is dramatic. Fiber optics systems used on several GSFC spacecraft and have been credited with lowering overall system costs, mostly due to shortening and simplifying integration. [3]

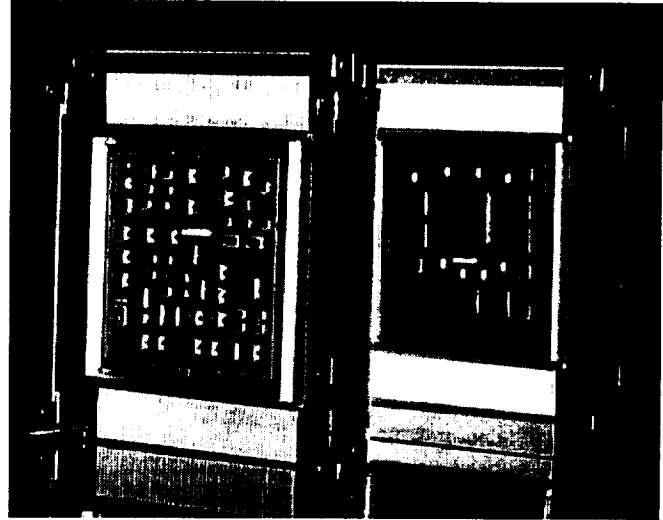
3. ESSENTIAL SERVICES NODE

The Essential Services Node (ESN) was developed by GSFC to reduce cost, size and schedule for the development of remote terminals on spacecraft. The ESN integrates many common functions into a single 2.6" x 2.6" x 0.1" package such as:

- 16-bit UT69R000 RISC Processor
- BCRTM protocol chip for MIL-STD-1553/1773
- Parallel and Serial interfaces
- A/D converter, Analog MUX and current sources
- UARTs, Timers, Watchdog

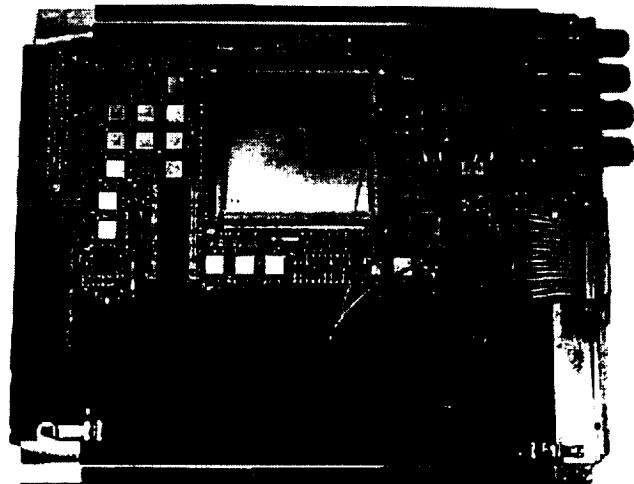
The ESN was designed to be embedded into a spacecraft subsystem or instrument to provide a standard software and hardware interface to the spacecraft bus. The ESN reads status and other data from a subsystem, formats it for the bus, and provides a platform for processing the data and reacting to out-of-limit conditions. The ESN also receives commands and other data over the bus, and translates that to physical commands to the user's subsystem.

The ESN, in order to decrease size and weight, was implemented as a Multi-Chip-Module (MCM) by Honeywell Central Technical Operations (CTO) of Phoenix, AZ with all of the digital logic implemented in a single ASIC by FirstPass, Inc. of Castle Rock, CO. The double sided MCM (with lids removed) is shown in front of a mirror to view both sides in the figure below. [5]



Essential Services Node (in front of a mirror to show both sides)

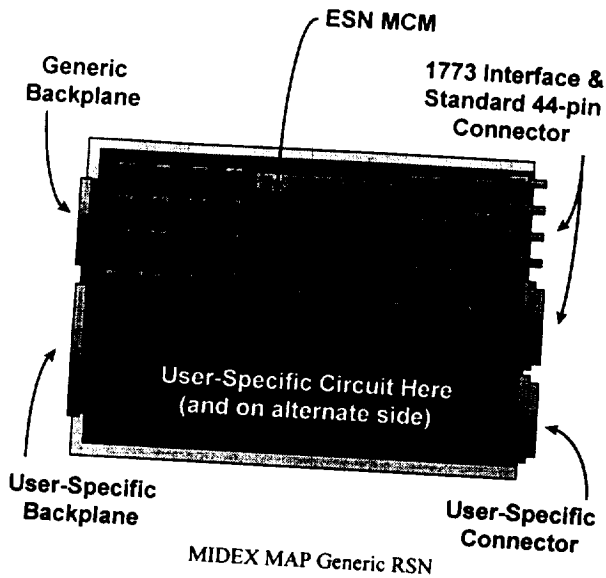
The ESN was designed to be a single part solution for embedding a computer into an instrument or subsystem. However, certain parts such as PROMs, oscillators, data bus transceivers have to be added outside of an ESN to make it a completely operational computer. To maintain the standard hardware and software interface goals, designers on the MIDEX MAP program extended the level of standardization to include this generic peripheral hardware outside the ESN, and created a standard circuit that would be used by all MIDEX MAP subsystems. The total circuit, known as the Generic Remote Services Node (RSN), was laid out and fixed, allowing each of the subsystem engineers to concentrate on their particular application and not duplicating efforts. The actual Generic RSN hardware implementation occupies one half of one side of a MIDEX standard 9.7" x 8.4" flight card size and is shown in the figure below.



MIDEX MAP Generic Remote Services Node (RSN)

In this way, each individual subsystem was left three quarters of the board to implement circuits for their particular subsystem. This is demonstrated in the figure

below.



The ESN, using the Generic RSN approach, has been successfully integrated into the MIDEX MAP design in five different subsystems including the MAP Instrument, Housekeeping, Attitude Control, Power, and Transponder Interface electronics. [6]

The ESN has been successfully integrated into several other GSFC developments such as the TDRSS Generation IV Transponder being developed by Motorola, the X-Band Phased Array Antenna being developed by Boeing, the Ka-Band Phased Array Antenna being developed by Harris and the Total Ozone Mapping Spectrometer (TOMS) FM-5 Instrument electronics under development by Orbital.

The main advantage of implementing a system using the ESN is reduced cost and weight. The ESN is approximately one fourth the cost of its discrete equivalent. This is due in part to the use of an ASIC to integrate the major digital functions on to one chip. This in turn means one chip is tested, one chip is stocked, and one chip is handled in the assembly of each ESN. Another cost advantage is in the inherent increase in software reuse in the implementation of a system wherein five identical processors are used. The use of the double sided MCM package has reduced the weight of an ESN system, the ESN weighing approximately one tenth of its discrete equivalent.

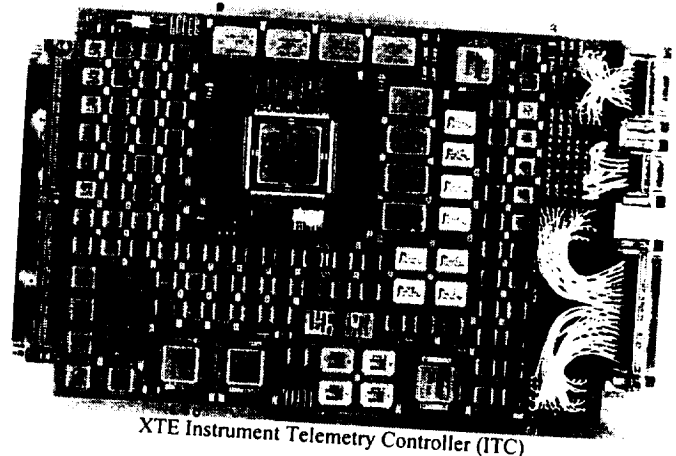
4. MONGOOSE PROCESSORS

Developing and integrating processing platforms for data handling and attitude control has long been a focus of GSFC. In the past this development was accomplished at the board level, purchasing existing processors from Intel or Harris or others, and designing a board around them. Following the successful integration of SAMPEX in 1991,

GSFC identified the need for a truly radiation hardened 32-bit microprocessor. The MIPS architecture was chosen for the first of these, the Mongoose I processor, developed by GSFC, designed by Harris Government Services Division of Melbourne, FL and fabricated on the LSI Logic (now defunct) LRH20000 radiation hardened gate array line.

The Mongoose I was developed by converting the LSI Logic Cobra core processor to a gate array design. The caches were moved off chip, and the processor ran in a cache-only mode to reduce gate count of implementing a more complete cache controller. In order to reduce overall board chip count, peripherals were added to the Mongoose I core such as general purpose timers, expanded interrupts and dual UARTs.

The Mongoose I was first used in the XTE spacecraft in the Instrument Telemetry Controller, shown below. It was subsequently used in the TRMM Power Subsystem, in the SSTI/Lewis Goddard Electronics Module and in the Hubble Space Telescope Coprocessor installed during the 2nd Servicing Mission.

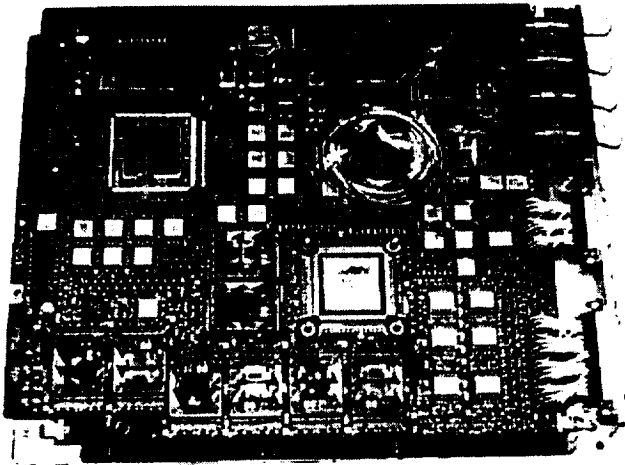


XTE Instrument Telemetry Controller (ITC)

The Mongoose V began development soon after the Instrument Telemetry Terminal was completed, and addressed several of the shortcomings of the Mongoose I design. In order to increase performance, an IEEE Floating Point Unit was added. In order to reduce overall system cost, which was mostly driven by radiation hardened SRAM external cache costs, several items were integrated onto the processor chip including a the Level 1 instruction and data caches, DRAM controller, and an Error Detection and Correction Unit. [7]

For the MAP mission, the Mongoose V processor board, shown below, acts as the spacecraft central processor and recorder for all instrument and spacecraft data. The Mongoose V processor board has 256 Mbytes of DRAM with EDAC for data storage, 4 Mbytes of EEPROM for program storage, several timers including a watchdog and a

Medium Speed Serial Port (MSSP) for direct transfer of data to the spacecraft downlink.



MIDEX MAP Mongoose V Processor Board

The Mongoose V has several advantages over other processors. The choice of an industry standard R3000 core has been advantageous because of the availability of development tools and real-time operating systems. The integration of the caches and the FPU onto the chip has reduced the chip count of the processor, thereby decreasing board size and cost. The addition of EDAC and a DRAM controller has allowed the use of very high density inexpensive DRAM stacks for recorder memory. The integration of various peripherals such as UARTs and timers has also dramatically reduced board complexity. The Mongoose V is available as a chip, and therefore can be designed into systems of any size and shape, which is advantageous for future nano-satellites and other smaller spacecraft where novel packaging will be the key to success.

5. SMEX-LITE COMPUTATION HUB

For the SMEX-Lite program, GSFC has developed a plug-and-play architecture that considers all mission elements that contribute to mission costs. This architecture allows components to be added, deleted, or upgraded to meet specific mission needs. The SMEX-Lite main computer, the Computation Hub, communicates with other spacecraft subsystem via a MIL-STD-1553 bus. For instrument data, four EIA RS422 Direct Memory Access (DMA) channels provide high speed access direct to the computer memory. A RAD-6000 32-bit processor board, jointly developed by GSFC, Lockheed Martin and the U. S. Airforce performs data processing and storage in the Computation Hub. The RAD-6000 processor board includes 200 Mbytes of DRAM with EDAC, 1 Mbyte of EEPROM for program storage, and 4 Mbytes of SRAM for program execution.

Communications on the backplane of the Computation Hub

are via an industry standard PCI bus running at 33 MHz. The master protocol chip, on the RAD-6000 processor board is implemented within the LIO chip, part of the RAD-6000 chipset. For specific spacecraft functions, GSFC designed custom boards that were PCI bus slaves. In order to implement the PCI slaves, GSFC purchased a VHDL model for the PCI slave, and implemented the slave protocol chip in an Actel FPGA.

The SMEX-Lite spacecraft has also served as a tested bed for demonstrating many weight savings devices. The use of cast aluminum electronics enclosures reduces weight of the chassis as well as dramatically reducing the cost of reproduction. The base plate of many electronics boxes serves as the outer structural member of the spacecraft. Rather than fabricate the outer structure as a door to a bay on which a box is mounted, the structural member is integrated with the box, and the unit is integrated to the spacecraft bus simultaneously. The SMEX-Lite spacecraft design has focused on all aspects of spacecraft design that reduce cost, the weight of the spacecraft, the widespread use of standard interfaces and the plug-and-play architecture to accommodate many different future missions.

6. ULTRA-LOW POWER

Currently GSFC is developing a nano-satellite class of satellites. This class of satellites will weigh 10 kg or less and will have a total power budget of approximately 5 watts. Developing the Command and Data Handling (C&DH) subsystem for a nano-satellite presents some unique challenges. The major challenges placed on the C&DH subsystem are meeting the requirements of a mass budget of 0.25 kg and a power budget of 0.5 watts.

With its partners GSFC is developing CMOS Ultra-Low Power Radiation Tolerant (CULPRiT) technology, which while meeting the low power challenge of nano-satellites will also reduce weight, size, and cost to produce optimal electronics. CULPRiT, in conjunction with System on a chip and C&DH in your Palm are the technologies that will enable the power reduction required for nano-satellites. The goals of these technologies are a 20:1 power reduction over current 5 Volt technology, foundry independence of die production, and radiation tolerance.

The CULPRiT development is being undertaken by a partnership between NASA/GSFC, DoD, the University of New Mexico, Sun Microsystems, Stanford University, and American Microsystems Inc. These partners have expertise in a variety of areas. NASA/GSFC with its expertise in space flight electronics and radiation testing will be handling the radiation testing and technology insertion. The University of New Mexico with expertise in radiation tolerant electronics in commercial CMOS processes will be

developing the radiation tolerant libraries and American Microsystems Inc. with expertise in running a modern commercial IC foundry for the Government/Aerospace industry will be manufacturing the chips.

CULPRiT will utilize two technologies in order to achieve its goals. The first is ultra low voltage CMOS technology that enables CMOS to operate at 0.25 volts. The second is radiation tolerant CMOS that utilizes only changes in the design of the circuits and not the IC process. This will allow for the fabrication of CULTRiT VLSI on commercial foundries reducing the cost of developing radiation tolerant parts.

The first chip off the CULPRiT line will be the Reed-Solomon Encoder to be used for CCSDS Encoding of data. This chip should be available for radiation testing by the end of 1999.

7. RHRFPGA

Another technology enabling a decrease volume of spacecraft is the Radiation Hardened reconfigurable FPGA (RHRFPGA). The RHRFPGA reduces volume by replacing many logic functions/circuits with one die. The RHRFPGA also allows concurrent design by de-coupling the logic design from the module which saves time and cost by shortening the design schedule and lowering the part count. An additional benefit to RHRFPGAs is the ease of rework, where the hardware can be redesigned as easily as software is currently re-written.

In addition, the RHRFPGA can be configured into a Reconfigurable Processing Array (RPA) merging speed and flexibility. Currently there are two approaches used for data processing. The first is a dedicated hardware approach that is designed for a specific function giving the best functional performance and highest functional efficiency. Unfortunately, this method typically takes a relatively long time and it is difficult to make design changes. The other approach is a software approach, which utilizes a general purpose processor allowing for flexible programmability and reuse of existing applications. The down side of this approach is that there is a reduced performance and lower efficiency compared to the hardware solution.

Configuring the RHRFPGA into a RPAs provides a single design, which enhances performance, programmability, efficiency, and reuse. RPA cards can be reconfigured on the fly at the silicon level to perform different tasks on orbit. Applications that will benefit from the computational speed and re-programmability of PRA's in the areas of band aggregation, radiometric/geometric processing, automated cloud cover assessment, thumbnail imaging, digital signal processing, compression/decompression of data, sequence analysis and pattern matching.

There are two types of FPGAs, volatile and non-volatile. The volatile FPGAs utilize RAM based technology and are multi programmable allowing a single FPGA to be used for an infinite number of designing iterations. The non-volatile FPGAs use anti fuse technology which limit the device to being a one time programmable part only with one chip only holding one design.

Commercial FPGAs are available today, however, there are no radiation hardened FPGAs.

Currently GSFC is working with Sandia National Lab, Honeywell, and Atmel to design, develop, and fabricate a Radiation Hard reconfigurable FPGA. This development will take the ATMEL AT6010 FPGA and re-fabricate it on a Honeywell radiation hard fabrication line. The scheduled date for developing an end product is mid-FY2000.

8. ADVANCED PACKAGING

To meet the mechanical geometry and power requirement of a nano-satellite, fundamental changes must be made in the way electronics are packaged. To reduce power and increase signal speed, electrical paths between circuit elements must be as small as possible. The trend toward wafer scale integration will certainly enable very complex electrical, thermal and mechanical devices to reside within microns of each other as opposed to centimeters or even meters. This technology, though maturing rapidly in the theoretical regime, is still not available commercially with the exception of wafer scale electronics and application specific chips.

The most dense packaging available today is being accomplished with a variety of interconnect technologies including multi-chip modules (MCM), the use of flip-chip die attach and the use of chip-scale packaging with ball grid array solder attach. These packaging techniques allow selection of circuitry at the die level (including user designed circuitry) and high integration density either within a package or at the pc-board level. The industry is thereby providing users paths for customizing their systems through device selection (which is critical for space flight circuitry where radiation tolerance is often a critical parameter) while still being able to benefit from commercial packaging technologies developed for high volume production. Though these technologies are available on a commercial basis, they must be proven for use in flight hardware. Evaluations and implementations of these processes have been ongoing for a couple of years and will continued to be studied, so it is advantageous to consider them in the near term for advanced packaging solutions for nanosatellites.

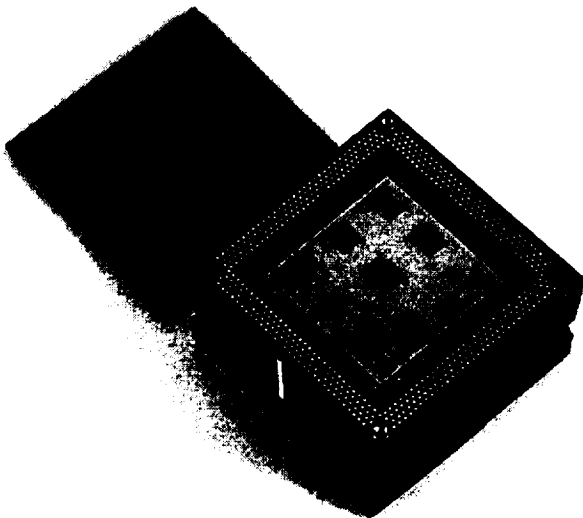
NASA's need for lightweight, highly dense electronics

parallels commercial industry's trend toward compact, handheld, battery powered computers. Spacecraft busses are becoming standardized and Principle Investigators are turning to smarter, more autonomous instruments. System designers are being asked to mix heritage designs and software with newly emerging systems. The structure, the thermal bus and the electronics must allow plug-and-play modularity, occupy as little space as possible and minimize power consumption to maximize the projects' ability to provide resources to the collection of science data. The stacked MCM approach is seen as a first generation electronics box for nanosatellites that attempt to address these needs.

The key design challenges for making a stacked MCM are:

- integration of the electronic device at the die level
- design of a electrically, thermally and mechanically optimized substrate
- module organization to allow plug and play of sub-assembly level circuitry
- module-to-module interconnects which allow high speed, low noise data transfer
- design of an assembly level package or rack which allows module replacement and a module-to-board level interface.
- integration, test, troubleshooting a part which has a three dimensional form factor

Several cube computers and stacked memory devices are on the market and in development, which show the interest and trend toward three-dimensional electronic module integration. None are on the scale of the goals set for nanosatellites (216 cm³). Pico Systems Inc. and NASA GSFC have been looking at combining a variety of emerging packaging technologies to create a three-dimensional multichip module on a nanosat scale. One such concept is shown in the figure below.



Pico Systems Inc. is the sole provider of programmable substrates. Substrates that are normally used in multichip modules are multi-layer ceramic components with a user defined circuit interconnection grid. Each ceramic substrate is custom and can take eight to twenty weeks to procure depending on the complexity and backlog at the manufacturer. The cost of designing and fabricating ceramic substrates do not lend themselves to prototyping so design errors can have major cost ripple effects. The programmable substrate is an amorphous silicon device, fabricated using standard semiconductor processes, and can be "burned" with a interconnection design, like is done with field programmable gate arrays, on a piece part basis. The turn-around time is on the order of days and design changes have little to no cost impact. Circuit density using Pico Systems' programmable substrates is similar to that of MCM's, which use ceramic substrates. Advances in the programmable substrate technology promise to lend even more flexibility to the designer with respect to substrate sizes and bond pad arrangement.

A NASA contract is currently in place with Pico Systems to design and fabricate a prototype four layer stacked MCM using their programmable substrates and fuzz button interconnects between the layers. Fuzz buttons are fine, gold wire, columns, which are embedded in FR4 pc-board material. They are compliant interconnects which allow a zero insertion force, tightly spaced, repeatable connection. A pin grid array is planned for the board interface, however a ball grid array is also an option. SRAM and EEPROM will be used to demonstrate the electrical performance of the interconnections on each layer, between layers and between the board and the stack over frequency, with temperature and in vibration. Evaluation at GSFC will also determine the theoretical stress concentrations over temperature, with temperature cycling and in vibration due to the geometry of the design and the materials selected. Theoretical limits will be determined for the number of layers a stack can have while maintaining mechanical reliability. Other approaches to the Pico Systems stack are being investigated and considered including technologies being explored by JPL's X.2000 program. As the electronics move closer together, thermal issues must also be seriously investigated. This will be critical as more electronic circuitry shares wafer space with micro-electro-mechanical systems (MEMS) which experience performance degradation when thermal gradients exist across a wafer. Integrated heat pipe technology and the use of super-heat diffusing materials, such as chemical vapor deposited diamond, should be studied and developed in preparation for future advances in electronics packaging.

9. CONCLUSION

The advanced technology components developed by GSFC have all in some way increased the capability of the spacecraft and enabled cutting edge science missions. Moreover, each technology has contributed to lowering the cost of the mission, enabling more missions within budget constraints.

The usage of MIL-STD-1773 fiber optic busses have simplified and shortened spacecraft integration and test activities for the SAMPEX, XTE and TRMM projects. Our current Parallel FODB developments will enable data transfer rates three orders of magnitude higher than MIL-STD-1773, enabling science instruments to produce more data than ever before.

The development of the Essential Services Node was focused mainly on reducing the size and weight of processor boards by implementing equivalent electronics in ASICs and MCMs. This reduction allowed each subsystem to integrate increased capabilities onto their processor board. Each subsystem implementing the ESN also reduced software integration time and cost, by implementing a standard hardware base.

The Mongoose I processors were developed to address the need for 32-bit processing in spacecraft. The Mongoose V processor addressed the need for reducing chip count, board real estate and increased functionality.

The SMEX-Lite computation hub demonstrates several cost and weight savings innovations that will enable future spacecraft to be smaller and lighter. The computation hub offers a industry standard processor, backplane and box-level interface allowing the user the maximum flexibility for reuse.

The Ultra Low Power development taking place will reduce the power consumption of avionics by 20:1. The positive impacts of this will ripple throughout the spacecraft, reducing overall system costs by at least an order of magnitude. Ultra Low Power will allow reduction in size of solar panels, batteries, power systems. Reduced power dissipation will allow even the housing of the avionics to reduce in size.

The Radiation Hardened FPGA development taking place will not only reduce the size of electronics by integrating boards onto chips, it will usher in a new era in reconfigurable spacecraft. Science data processing algorithms currently implemented on the ground could be migrated to the spacecraft. This would allow data reduction to take place on the spacecraft reducing downlink requirements. The reconfigurable nature of Rad-Hard

FPGA would allow the algorithms to be implemented in hardware at higher speed, and allow them to be changed routinely to meet the needs of the science team.

The Advanced Packaging developments are essential to meet the mechanical geometry and power requirement of future nano-satellites. GSFC has addressed these needs in point solutions such as ASICs, MCMs, 3-D stack memories. In order to meet the needs of future program the focus must be on reducing non-recurring costs, and reuse of mechanical enclosures. The Advanced Packaging effort at GSFC will allow a great reduction in size and volume while maintaining structural integrity and thermal capability.

This paper has presented a survey of development and insertion experiences for the above technologies, as well as future plans for technologies that enable more "better, faster, cheaper" spacecraft. It by no means represents the whole of development within GSFC in support of cutting edge Earth and Space Science. For more information on these or other technologies under development at GSFC, contact the authors at the email addresses given above.

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