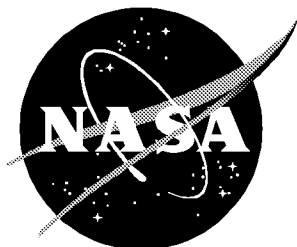


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Design of Advanced Atmospheric Water Vapor Differential Absorption Lidar (DIAL) Detection System

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July 1999

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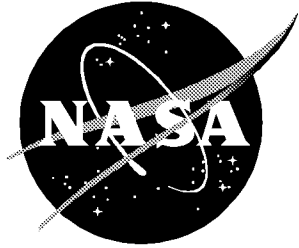
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Abstract

The measurement of atmospheric water vapor is very important for understanding the Earth's climate and water cycle. The lidar atmospheric sensing experiment (LASE) is an instrument designed and operated by the Langley Research Center for high precision water vapor measurements. The design details of a new water vapor lidar detection system that improves the measurement sensitivity of the LASE instrument by a factor of 10 are discussed. The new system consists of an advanced, very low noise, avalanche photodiode (APD) and a state-of-the-art signal processing circuit. The new low-power system is also compact and lightweight so that it would be suitable for space flight and unpiloted atmospheric vehicles (UAV) applications. The whole system is contained on one small printed circuit board ($9 \times 15 \text{ cm}^2$). The detection system is mounted at the focal plane of a lidar receiver telescope, and the digital output is read by a personal computer with a digital data acquisition card.

1. Introduction

Water vapor is a very important molecular species in the atmosphere. Although it is located primarily in the troposphere, its distribution is highly variable in both time and position. Its measurement is important for the following three main reasons (ref. 1):

1. The knowledge of the atmospheric water vapor distribution is essential for achieving a full understanding of the Earth's water cycle
2. Water vapor is the predominant greenhouse gas and plays a major role in the global climate system
3. Water vapor distribution has a direct impact on some natural disasters, such as hurricanes; water vapor has been found to be the main energy source for hurricanes and water vapor measurement can aid in estimating hurricane strength and direction (ref. 2)

Aircraft-based lidar systems are increasingly being used to measure troposphere water vapor profiles. Aircraft lidars using the differential absorption lidar (DIAL) technique can accurately measure water vapor densities throughout the troposphere (ref. 3). Future lidar systems are being proposed to be deployed from space platforms where continuous global profiles of water vapor can be obtained across the lower atmosphere on a daily basis for several years. Such an accumulation of water vapor data will allow for these issues to be addressed in a manner not available before.

The lidar atmospheric sensing experiment (LASE) is an instrument, designed and operated by the Langley Research Center, for remote water vapor profile measurements in the troposphere from the NASA ER-2 aircraft, which is based at the Ames Research Center (ref. 4). The LASE instrument measures with an accuracy of better than 6 percent or 0.01 g/kg, whichever is greater (ref. 5). Although LASE is the most capable water vapor DIAL system in the world, its detection system uses a CAMAC (computer automated measurement and control) crate which is massive and consumes much power.

This type of detection system is unsuitable for space applications, which require small size, low mass, and low power. (See refs. 4, 5, and 6.)

In this paper, a new advanced water vapor DIAL detection system is described. This system is placed on one card which contains an advanced very low noise avalanche photodiode (APD) detector. State-of-the-art electronics are considered and include saturation protection amplifiers, a 14-bit digitizer, and a microcontroller for on-line data processing. The new system is interfaced to a remote computer to store the data (ref. 7).

1.1. DIAL Technique

Light detection and ranging (lidar) is an active remote sensing technique which uses a pulsed laser and a colocated receiver to measure the density of atmospheric gases and aerosols as a function of range. In the DIAL technique, two laser pulses at slightly different wavelengths are transmitted into the atmosphere. The transmitted laser pulse is subjected to scattering, absorption, and reflection because of the molecules and particles in the atmosphere; therefore, the light backscattered to a telescope receiver contains some information about this medium which can be evaluated with the lidar equation. By looking at the lidar signals in terms of the received power $P(r)$ when the transmitted laser pulse has an initial optical power P_o , the backscattered received power from a range r is given by (ref. 3)

$$P(r) = P_o \frac{c\tau A\eta \beta(r)}{2r^2} \exp \left\{ -2 \int_0^r [\sigma n(r) + k(r)] dr \right\} \quad (1)$$

where c is the speed of light, τ is the laser pulse duration, A is the receiver area, η is the receiver efficiency, $\beta(r)$ is the atmospheric volume backscatter coefficient, σ is the absorption cross section of the molecular species of interest, $n(r)$ is the number density profile of the gas, and $k(r)$ is the atmospheric extinction coefficient resulting from all other attenuation processes.

Generally, the absorption profile of a gas is a unique function of the wavelength. According to this principle, the DIAL technique is used to distinguish and monitor different atmospheric gases including water vapor. In a water vapor DIAL system, two laser pulses are transmitted to the atmosphere. The wavelength of the first pulse is adjusted to the peak of a water vapor absorption line and is called the on-line pulse, whereas the other pulse wavelength is adjusted to a wavelength which corresponds to no absorption and is called the off-line pulse as shown conceptually in figure 1. Because the two wavelengths are so close, the scattering by atmospheric molecules and particles is essentially equal for both wavelengths, and the difference in the attenuation with range of return signals is entirely caused by the absorption by the water vapor molecules. Thus the ratio of the backscatter signal at the two wavelengths as a function of range can be used to calculate the water vapor concentration profile. (See refs. 3, 8, and 9.)

If the wavelength difference between the on-line and the off-line signals is less than or equal to 0.1 nm, it can be assumed that $\beta_{\text{on}}(r) = \beta_{\text{off}}(r)$ and $k_{\text{on}}(r) = k_{\text{off}}(r)$, and we can solve equation (1) for the number density profile of water vapor to obtain

$$n(r) = \frac{1}{2(r_2 - r_1)(\sigma_{\text{on}} - \sigma_{\text{off}})} \ln \left[\frac{P_{\text{off}}(r_2) P_{\text{on}}(r_1)}{P_{\text{off}}(r_1) P_{\text{on}}(r_2)} \right] \quad (2)$$

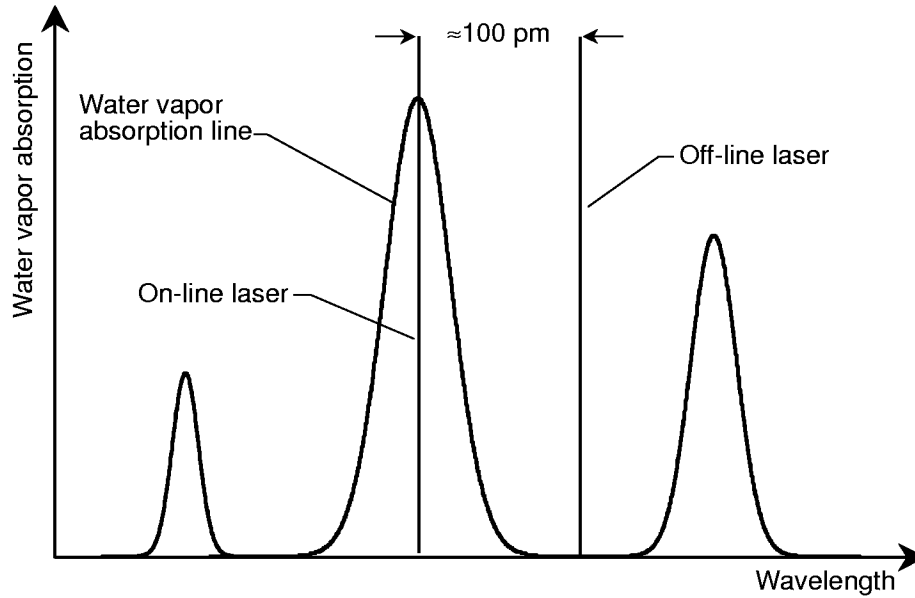


Figure 1. DIAL on-line and off-line wavelengths relative to water vapor absorption line.

where $(r_2 - r_1)$ is the range cell for the average concentration, $(\sigma_{\text{on}} - \sigma_{\text{off}})$ is the differential absorption cross section for the two wavelengths, P_{on} is the power received from range r for the on-line wavelength, and P_{off} is the power received from range r for the off-line wavelength. One can then convert the number density profile to a mass mixing ratio by dividing the gas number density by the ambient atmospheric number density. (See refs. 3, 8, and 9.)

Based on this information, the DIAL detection system must be capable of measuring the backscattered on- and off-line lidar returns accurately; this drives the DIAL receiver design considerations and specifications which include the following:

1. The system must have a wide dynamic range to handle the different intensities of the backscattered radiation
2. It must have low noise to reduce the minimum detectable signal level to extend the measurement range
3. It must have a sufficient bandwidth to resolve the return pulses
4. For accurate measurements, it must be very linear with minimum phase shift in the operating bandwidth
5. It must be capable of capturing both the on- and off-line signals sequentially with high resolution
6. It must be capable of operating at 10 to 30 Hz repetition rate
7. It must be compact and have low mass and low power consumption

1.2. DIAL Detection System Development

The main goal of this research effort is to increase the signal to noise ratio of the water vapor DIAL detection system by a factor of 10 compared with the LASE instrument (ref. 4). Also designing it to a compact size suitable for mounting directly on the receiver telescope is required. On the other hand, the output data must be compatible with a simple computer interface. These goals are achievable by using state-of-the-art electronic components and a newly evaluated very low noise APD detector and by constructing a 10-MHz waveform digitizer which will be placed as close as possible to this detector on the same card.

The new DIAL receiver system is shown schematically in figure 2. The design allows the placement of both analog and digital circuits on one small size, lightweight electronic card which includes detection and digitization sections. This scheme has the advantage of transmitting digital data, which will be stored and analyzed by a personal computer. Therefore, analog signals do not have to be transmitted for long distances, which will reduce the system noise pickup. (See ref. 7.)

The system design is optimized for wavelengths of 820 and 940 nm. In the optical system, a telescope is used to collect and focus the lidar return signal into a small area that is compatible with the detector sensitive area. An APD package is used for the light detection. The APD output signal then goes to an analog circuit for signal conditioning, which includes signal clipping, amplification, and filtering. In addition, this stage provides the detector with a stable bias voltage and temperature control.

The analog signal then goes to a digital circuit to be digitized, processed, and temporarily stored. This circuit is compatible with a parallel input/output computer interface for final data storage and display, and it provides monitoring for the detector high-voltage bias and temperature. The card is supplied with ± 5 V and ± 12 V power and a 10-MHz clock signal for the digitization. Each part of the new DIAL detection system is discussed in detail in the following sections.

2. Avalanche Photodiode Detector

Generally, APD detectors are an ideal choice for water vapor DIAL detection systems because of their high quantum efficiency of close to 90 percent over the wavelength operating range, which is

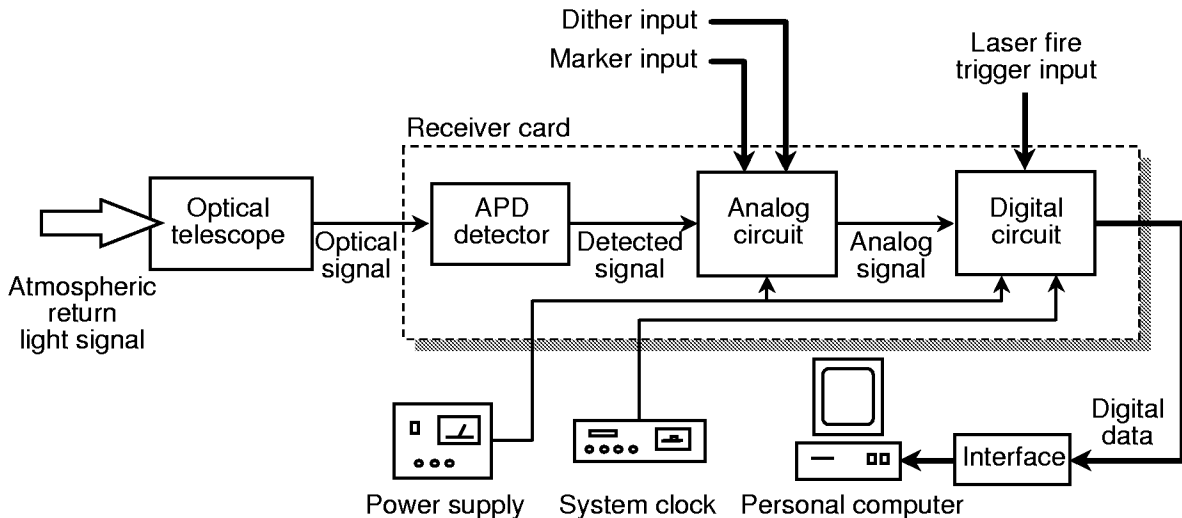


Figure 2. Schematic diagram of new DIAL receiver system.

unmatched by other detectors such as photomultiplier tubes. Also, it is a very fast device with internal gain, unmatched by silicon p-i-n detectors; it has low noise in the range of a few fW/Hz^{1/2}; it has excellent linearity with respect to incident light intensity, which is desirable for instrument calibration and data processing. The APD has a relatively low bias voltage (in the range of hundreds of volts) and is compact, lightweight, mechanically rugged, and reliable, which makes it suitable for an aircraft or space-flight detection system. (See refs. 10, 11, and 12.)

Several experiments were carried out to characterize and test a group of APD detectors representative of different manufacturers and with different structures to choose one of them for the new water vapor DIAL detection system (ref. 10). As a result of these measurements, the EG&G C30649E SLIK (super low ionization factor κ (with κ being defined as ratio of ionization probability of holes to that of electrons)) APD was chosen as the system optical detector. Table 1 summarizes the characterization results for both the EG&G C30955E RTS (reach through structure), currently used in LASE, and the SLIK APD's, both at their rated bias voltage and 23°C. The noise equivalent power (NEP) of the new detector is 8.6 percent of the current detector. This NEP improvement might be because of the smaller area of the new detector; therefore, the figure of merit (D^*) of both detectors is given. The results show that with the new detector, D^* has improved by a factor of 5 over the current detector; this indicates that the SLIK structure has a lower noise content than the RTS structure irrespective of its area. (See ref. 10.)

Table 1. Characterization Results for SLIK and RTS Detectors at 820 nm and Room Temperature (23°C)

[From ref. 7]

Model	Active area, mm ²	Rated bias, V	Responsivity, A/W	NEP, fW/Hz ^{1/2}	D^* , cm-Hz ^{1/2} /W
EG&G C30955E RTS	1.69	317	75.6	22.2	5.99×10^{12}
EG&G C30649E SLIK	0.24	336	43.8	1.9	3.05×10^{13}

The RTS APD is a device designed to have two separate field regions. The first is a wide region (about 30 μ m) with a relatively low field (20 kV/cm) in which the incident photons are absorbed and the charge carriers are drifted. The second region is a narrow, high field region in which the electron multiplication takes place resulting in internal gain. The relatively new SLIK or super low κ structure resembles, to some extent, the RTS structure. The electric field profile is shown in figure 3 for both devices. For the SLIK structure, the field profile is designed to achieve the lowest possible value of effective κ for a given device thickness. This is obtained by ensuring that the electric field is high enough to give some multiplication everywhere in the device, with the field gradually increasing to reach a maximum near the deepest point of the device, where practically no hole current exists. This design results in an effective κ of 0.002, which indicates low noise content, and a breakdown voltage of 400 V for about 25 μ m device depth. (See ref. 11.)

Other advantages of this APD package are its own built-in transimpedance amplifier (TIA), which enables it to directly generate a voltage signal proportional to the detected light intensity. Figure 4 shows a block diagram of the SLIK APD package. On the other hand, the APD active surface is placed on a thermoelectric cooler (TEC), with a thermistor located as close as possible to control and stabilize its temperature for constant responsivity operation. The feedback resistor of the TIA is also placed on the TEC to reduce the Johnson noise which reduces the amplifier total noise. The APD package spectral response is shown in figure 5 for the device rated bias voltage at room temperature (25°C) and 0°C. Appendix A gives the complete information for this detector package.

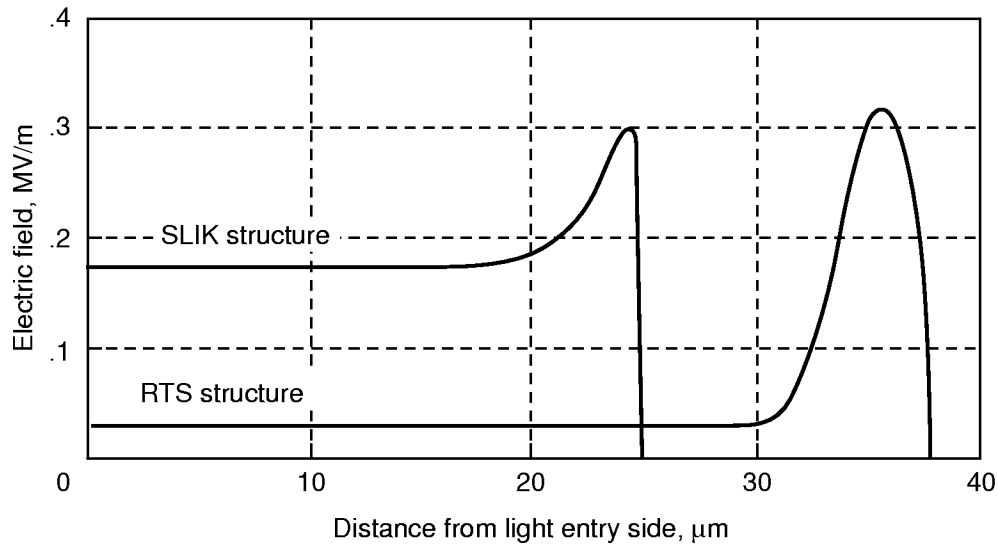


Figure 3. Approximate electric field profile along device depth for RTS and SLIK APD's. (Data from Henri Dautet of EG&G Optoelectronics Canada.)

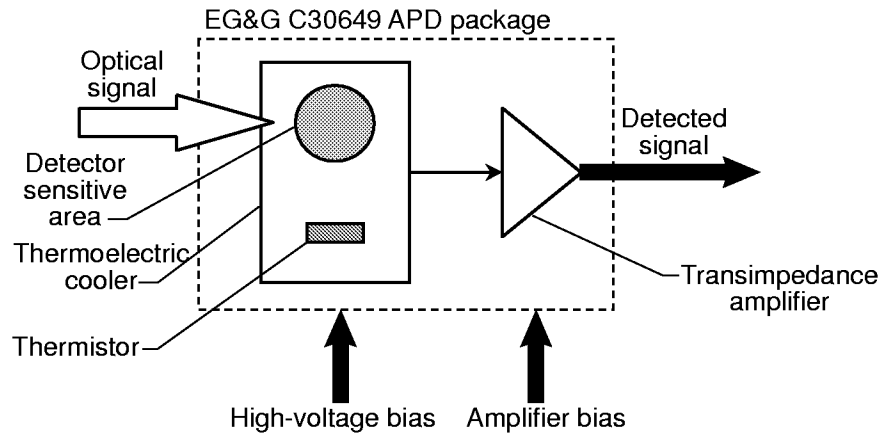


Figure 4. Schematic diagram of SLIK APD. (From ref. 7.)

3. Analog Circuit

In the text, the various parts of the system are referred to by their letter designations (e.g., L1, U1, R21); for the particular component used for the part, see appendix B. The analog circuit, shown in figure 6, is designed to control the operation of the APD package and to condition its output signal. The laser return signal is focused onto the 0.5-mm-diameter spot, which is compatible with the APD sensitive area.

The APD output signal is applied to the signal conditioning stage, which consists of three substages. In an actual DIAL application, the transmitted laser pulses might hit a large amount of water vapor or aerosol layer, such as clouds; this would result in high levels of backscattered light which overloads the system. These overload signals are a major problem since they saturate the detector and cause

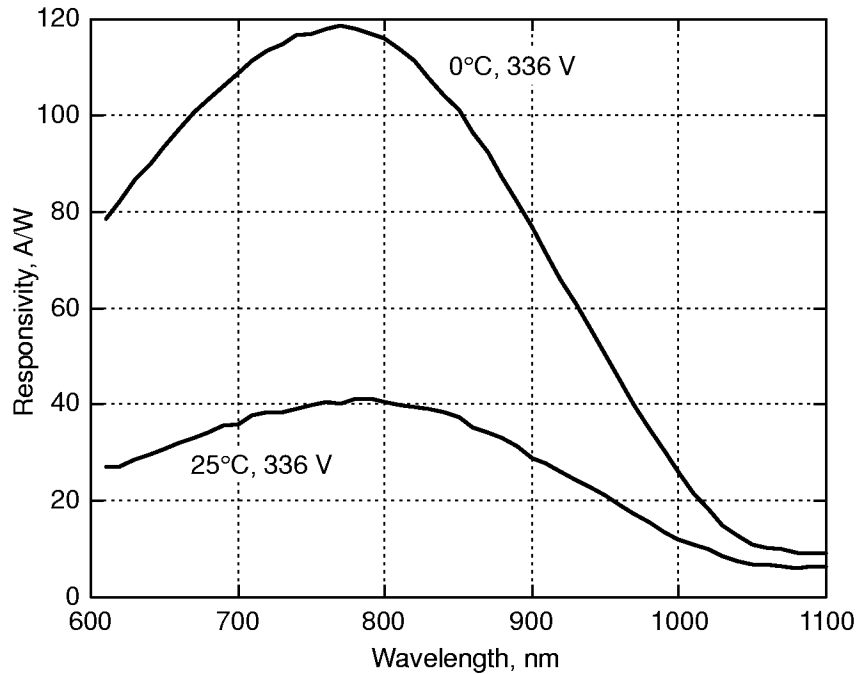


Figure 5. SLIK APD package spectral response.

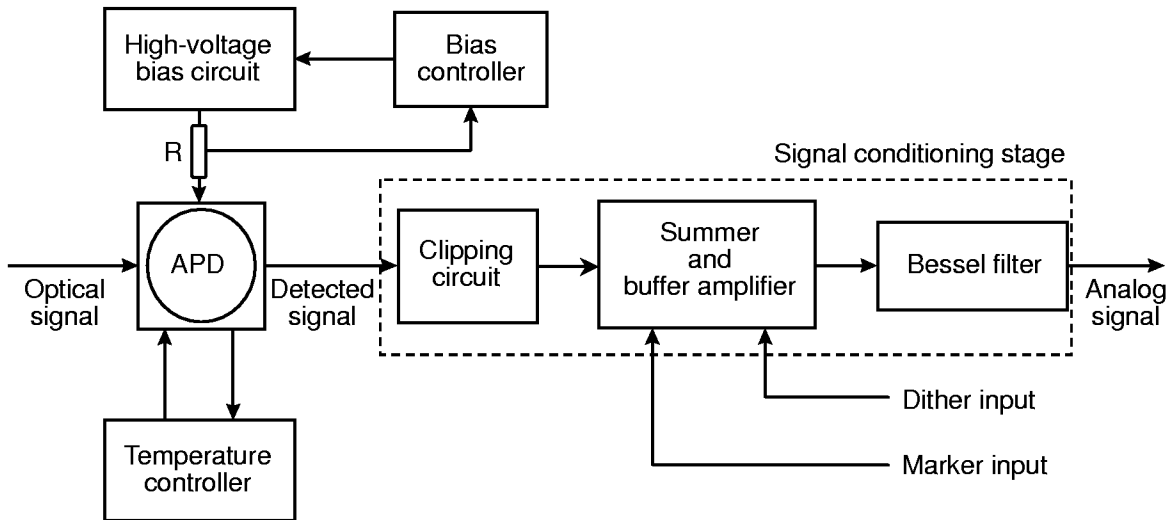


Figure 6. Block diagram of analog circuit.

“hanging” of the digitizer, which leads to loss of some data words. The clipping circuit is used to protect the digitizer by clipping these overload signals to a predefined level. For normal signals, the clipping circuit acts as a voltage follower amplifier. The APD overload is prevented by using a current limiting resistor R in figure 6.

Following this stage is a summer and buffer amplifier, designed to apply an additional gain to the detected signal to achieve a 2-V maximum peak-to-peak value, which is compatible with the digitizer. Also it adds a marker and dither signals to the detected signal. The marker signal is used to mark the beginning of the useful data, whereas the dither is used to add a low level sinusoidal signal for better

digitization performance (ref. 7). On the other hand, these inputs can apply a dc signal to eliminate high background signals. Because of its near ideal characteristics, an operational amplifier (op amp) was used in these stages. The op amp choice was made after characterizing a group of them to minimize their effect on the detected signal in terms of noise, linearity, and offset voltage. Finally, the signal was applied to a Bessel filter with a 2.5-MHz cutoff frequency. This filter will limit the system bandwidth in order to reduce the high-frequency noise and restrict the signal frequency with respect to the digitizing frequency according to Nyquist criterion.

Since the APD responsivity is a strong function of its voltage bias and temperature, two proportional integral (PI) controllers were used. The first is a voltage controller which can be adjusted manually to apply a constant bias to the APD ranging from a maximum value of 2.5 percent under the breakdown voltage to a minimum value of 13.1 percent lower than its rated bias which is measured with an open circuit. The second is a temperature controller with a fixed set point. This controller is used to cool the detector with respect to the ambient temperature. (See ref. 7.)

3.1. Power and Reference Voltages

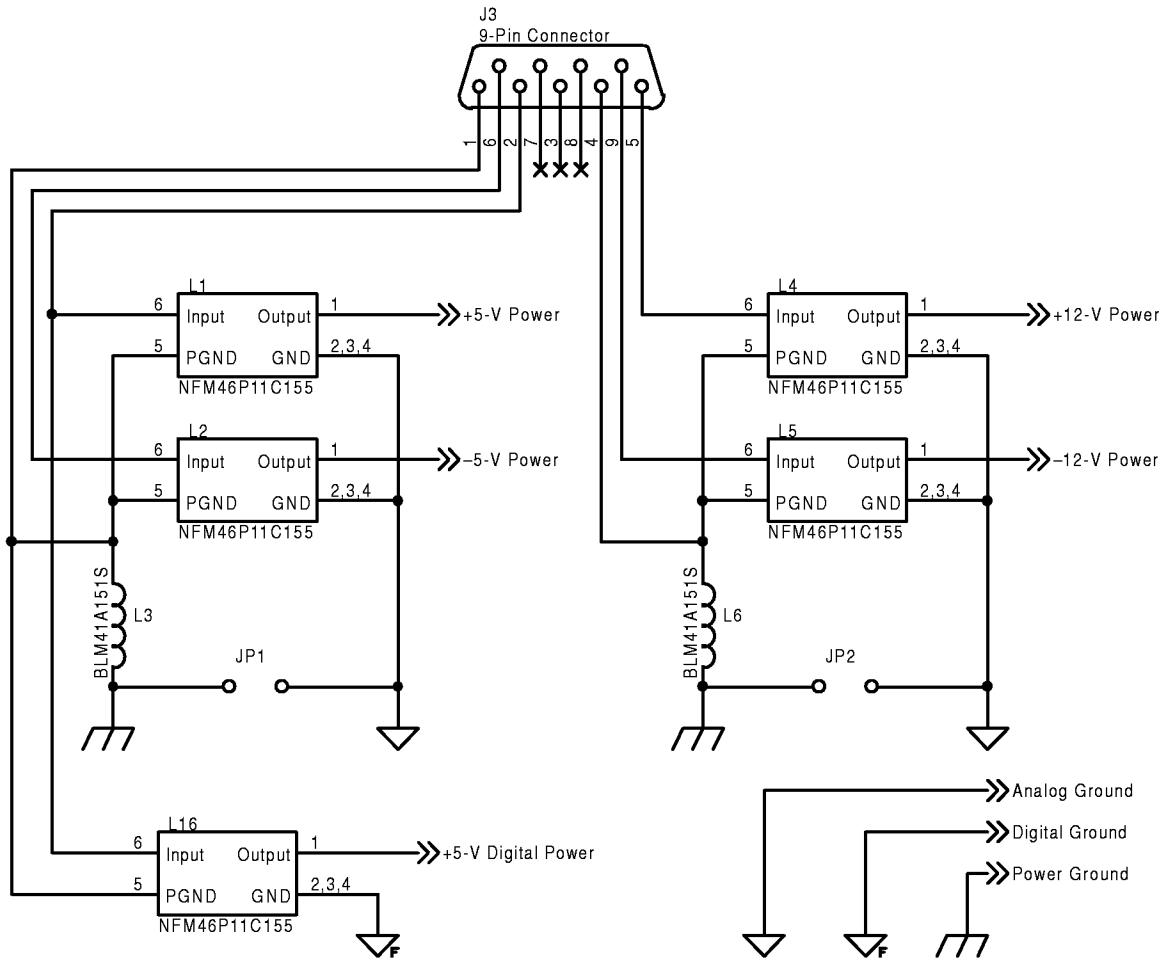
The detection card uses ± 5 and ± 12 V power applied by using J3, a 9-pin D connector, as shown in the circuit diagram in figure 7(a). Each supply is filtered separately by using noise suppression line filters L1, L2, L4, and L5, with the power ground separated from the circuit ground by using jumpers JP1 and JP2 to prevent ground loops. The +5 V is filtered once again by using L16 to ensure a proper separation between the analog and the digital circuits. L3 and L6 are chip ferrite bead inductors for ground noise reduction. The filtering of the power lines was done to ensure power voltage stability by reducing any voltage ripples. (See ref. 13.)

As discussed later, the detection card also uses +5- and -1.5-V reference voltages. As shown in figure 7(b), the +5-V reference is obtained from U1, the reference generator, whereas a dual op amp is used in the inverting configuration in U2 with a gain of 0.3 to obtain the -1.5-V reference. The 1- μ F capacitor C2 is used to eliminate high-frequency noise at its output by limiting the inverter bandwidth. (See refs. 14 and 15.)

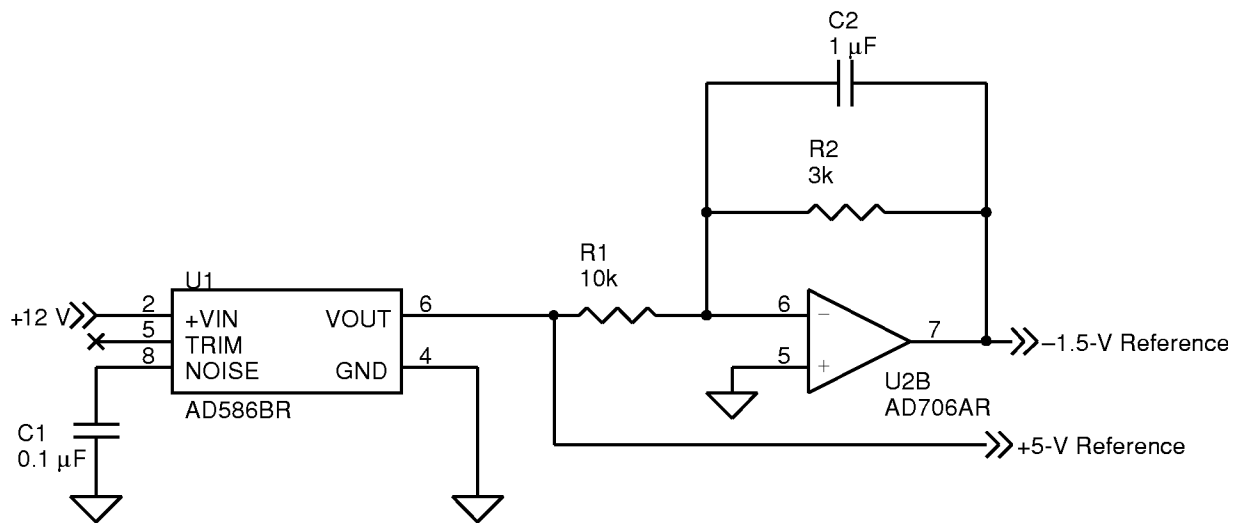
3.2. Signal Conditioning

Signal conditioning is the most critical stage in the whole detection system since any noise contribution from this stage to the detected signal directly affects the useful data. Figure 8 shows the circuit diagram of this stage. Op amp U7 is a clipping op amp which has been carefully chosen to solve the hanging problem. U7 operates as a voltage follower for the detected signal provided that the signal lies within the clipping limits. The upper clipping limit is set to 2.5 V with R24 and R25. This limit is chosen only for the op amp stability and has no influence on the output because the detected signal coming from the APD package is always negative with a maximum theoretical value of zero. The lower clipping limit is set by the -1.5-V reference voltage. R26 acts as the load resistance for the op amp as recommended by the manufacturer. The output of the clipping op amp is then applied to U8, which is a gain and summer amplifier. Using this op amp, the signal gain is set to 3 by using R27 and R26. The summation of the marker and the dither inputs to the detected signal is obtained by using R28 and R29, respectively. (See refs. 16 and 17.)

The final output is then filtered by using U9 which is a 3-pole, 2.5-MHz, low pass Bessel filter. The Bessel filter was selected because of its excellent performance regarding the phase shift for real-time data. R30 and R31 act as a terminating resistance for maximum power transfer condition. To check the output signal from this stage, the voltage across R31 can be accessed by an external connector. Also,



(a) Power supply.



(b) Reference voltage.

Figure 7. Power and reference voltage circuit diagrams.

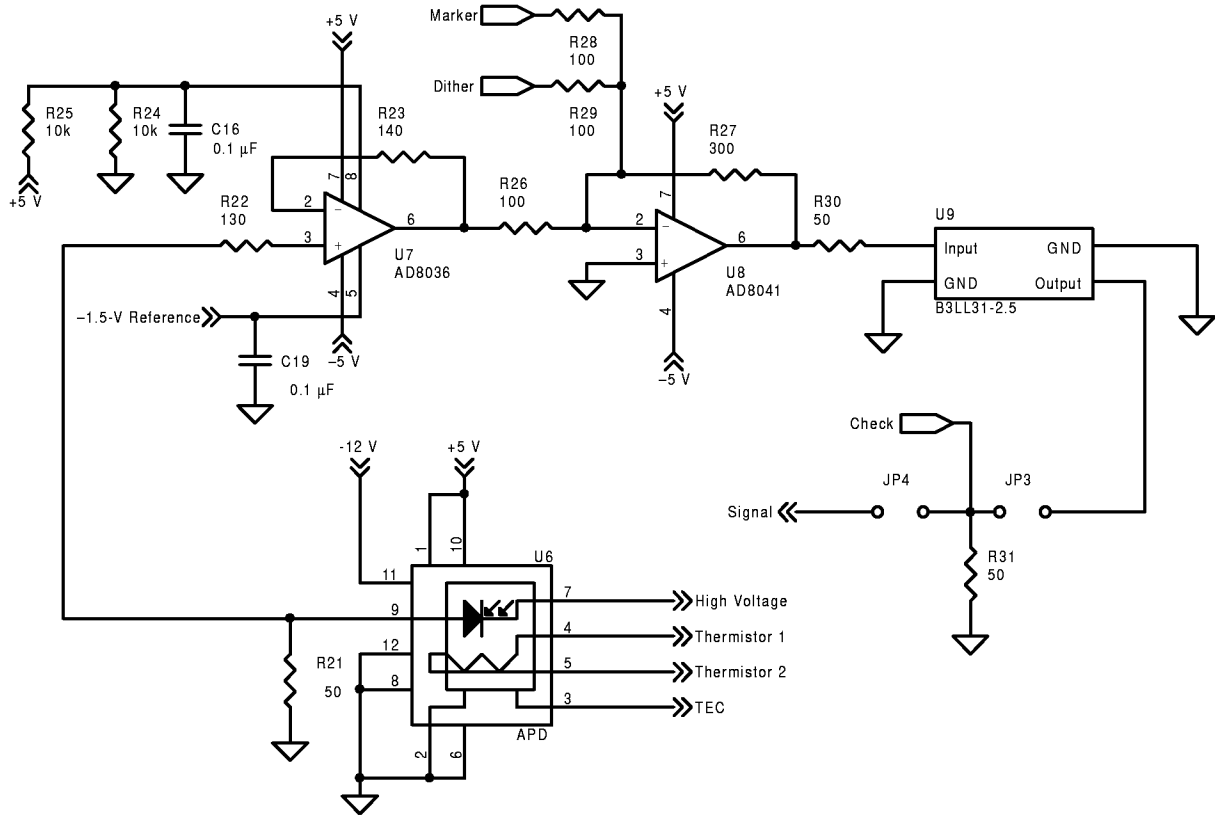


Figure 8. Circuit diagram of signal conditioning stage.

this connector can be used to inject an external voltage to the digitizer according to the JP3 and JP4 jumpers settings. (See ref. 18.)

3.3. APD Voltage Controller

As shown in figure 9, the APD voltage bias is supplied from U4, the high-voltage module. The control of the high voltage was obtained with U3, a dual op amp, with one acting as the proportional controller set to a gain of 4 by using R3 and R4 and the other as the integral controller set to an RC time constant of 0.04 s by using R5 and C5. D1 is used to ensure positive control voltage to U4. R7 is a potentiometer used to set the APD high voltage between 292 and 365 V. The output high voltage is applied to a low pass filter formed by R8 and C8 to eliminate any bias ripples. In addition, R8 limits the APD current as a secondary overload protection, and C9 supplies it with instantaneous in-rush current. A potential divider formed by R9 through R13 is used as the voltage feedback to the controller. Voltage monitoring is obtained after the proportional controller with a voltage reading V_{BM} is related to the high-voltage bias V_{bias} by

$$V_{BM} = \frac{V_{bias}}{14.91} - 20 \quad (3)$$

The bias monitor reading can be obtained directly from an external connector or digitally by the micro-controller. (See refs. 14 and 19.)

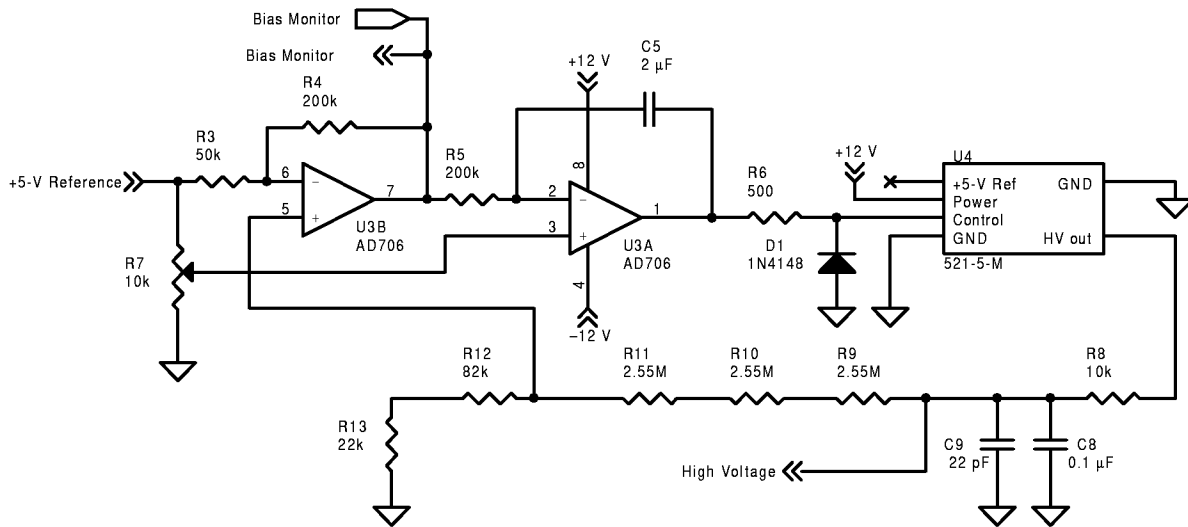


Figure 9. APD voltage bias controller circuit diagram.

3.4. APD Temperature Controller

As mentioned earlier, the APD package was supplied with a built-in TEC cooler and a thermistor. The temperature status of the detector is sensed by the thermistor by placing it in an arm of a Wheatstone bridge formed by R15, R16, R17, and R18 as shown in the circuit diagram of figure 10. The value of R18 will determine the balance condition of the bridge and therefore set the detector temperature. Because the thermistor resistance R_T is given by

$$R_T = 10^4 \exp \left[3940 \left(\frac{1}{T} - \frac{1}{298} \right) \right] \quad (4)$$

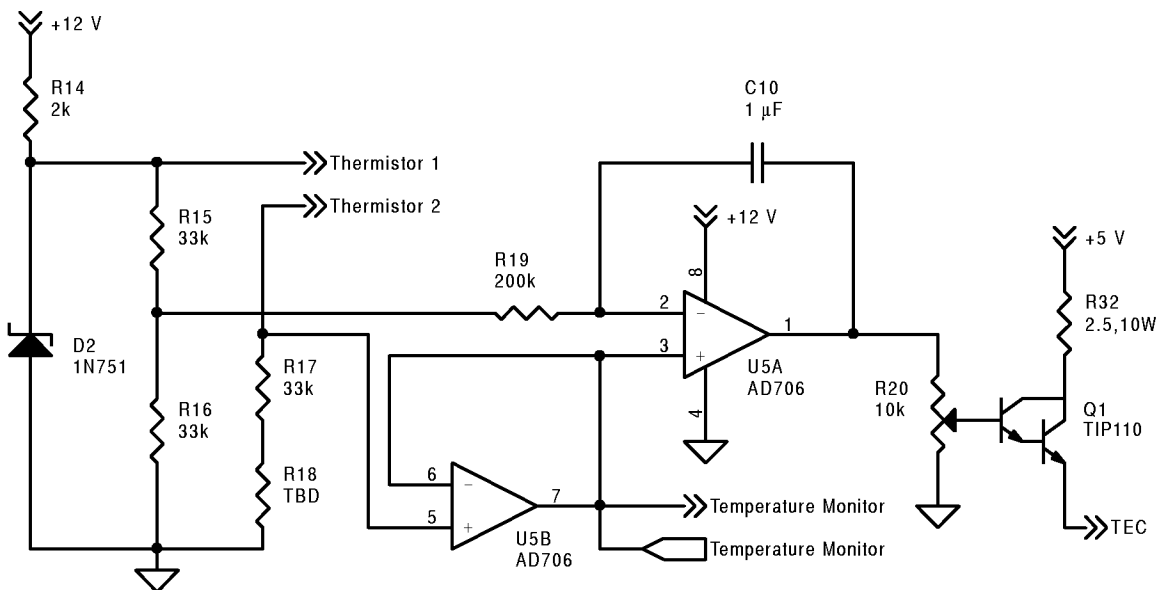


Figure 10. APD temperature controller circuit diagram.

and the bridge balance condition is

$$\frac{R_{15}}{R_{16}} = \frac{R_T}{R_{17} + R_{18}} = 1 \quad (5)$$

therefore, the temperature setting, in Kelvin, is given by

$$T = \left\{ \frac{\ln \left(\frac{R_{18} + 33 \times 10^3}{10^4} \right)}{3940} + \frac{1}{298} \right\}^{-1} \quad (6)$$

Equation (6) indicates that the minimum temperature setting is selected by R17 and is equal to 0.3°C with R18 short-circuited. Temperatures lower than this value usually cause problems due to freezing of water vapor on the detector window. Zener diode D2 is used to supply the bridge by its zener voltage V_Z which is equal to 5.1 V. The zener current limit is set by R14.

The bridge balance is sensed by an instrumentation amplifier formed by U5, with one op amp acting as a voltage follower for the temperature monitor and the other acting as both the proportional integral controller with RC time constant of 0.02 s set by R19 and C10. The controller output is applied to a potentiometer R20 to set the TEC current by controlling the collector emitter current of the Darlington transistor Q1. R32 is a 10-W resistor used to set the maximum TEC current to 2 A according to its specification (appendix A). The temperature monitor voltage reading V_{TM} will be given in terms of the zener voltage by

$$V_{TM} = \frac{R_{17} + R_{18}}{R_{17} + R_{18} + R_T} V_Z \quad (7)$$

After starting the circuit when the detector temperature reaches its steady state value the monitor voltage will be simply given by

$$V_{TM} = \frac{1}{2} V_Z \quad (8)$$

Similarly, this voltage can be read directly by using an output connector or digitally by the microcontroller. (See refs. 14 and 20.)

4. Digital Circuit

The digital circuit was designed mainly to operate as a waveform digitizer and also to perform some simple data processing such as averaging DIAL lidar return signals and monitoring the detection system performance. Figure 11 shows a schematic diagram of the main components of the digital circuit. The waveform digitizer is used to convert the analog lidar signal from the detector to a digital format. The dual port RAM is used for temporary data storage and also isolates the 10-MHz digitizer frequency from the 16-MHz microcontroller frequency.

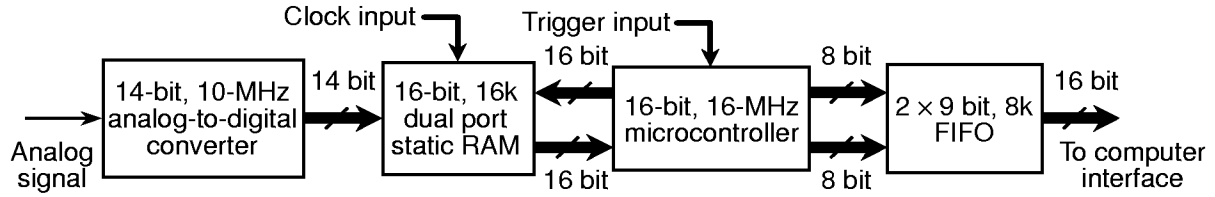


Figure 11. Schematic diagram for digital circuit.

Approximately 400 μ s before the DIAL laser fires, a trigger pulse is generated and is used as a precursor that informs other systems that the laser is about to fire. This pulse is sensed by the microcontroller, and this acts to synchronize the detection system with the laser transmitter. A 10-Hz maximum laser firing frequency is assumed in this design, although a higher repetition rate could be accommodated. Also, the microcontroller is used for on-line signal processing, which includes data averaging and housekeeping.

Finally, the first-in-first-out (FIFO) memory is used to output the final data to the recording system. Again, the FIFO separates the 16-MHz microcontroller operating frequency from the output reading frequency which could be any value up to 20 MHz. The output digital data are compatible with a simple input-output personal computer interface. (See ref. 7.)

4.1. Data Sampling and Storage Circuit

The conditioned analog signal was applied to U16, a 14-bit, 10-MHz analog-to-digital converter (ADC), as shown in figure 12. (See appendix C.) The input digitizer range was set to be from 0 to 2 V. Note that the maximum allowable output signal from the detector is given by

$$2 \frac{\text{ADC upper limit}}{\text{Signal conditioning gain}} = 2 \times \frac{2}{-3} = -1.33 \text{ V} \quad (9)$$

and the clipping op amp U7 lower limit was set to -1.5 V ; this limit ensures the linearity of the signal conditioning stage by avoiding the nonlinear knee between the linear and clip regions in the op amp input-output characteristics.

As shown in the circuit diagram of figure 12, a 10-MHz clock (CLK) was externally applied to the ADC. Therefore, it continuously digitizes the analog signal during each clock cycle. The digitized data was buffered using U17 and U18 and stored in a certain memory location in U19, a 16-bit, 16k, dual port RAM. The data storage location or address was set by a 13-bit counter formed by cascading three 4-bit binary counters U10, U11, and U12 and U13, a JK flip flop. The counter and the RAM share the same 10-MHz clock in order to synchronize them with the ADC. Connecting the most significant bit (MSB) of the left RAM address to the supply enables the counter only to access its upper half while the lower half of the RAM is kept for data averaging purposes. Thus the maximum real-time window for the digitized data can be obtained by

$$\text{Data time window} = \frac{\text{Storage space}}{\text{Clock frequency}} = \frac{16 \times 1024/2}{10 \times 10^6} = 819.2 \mu\text{s} \quad (10)$$

which is enough to record both the on- and off-line signal returns.

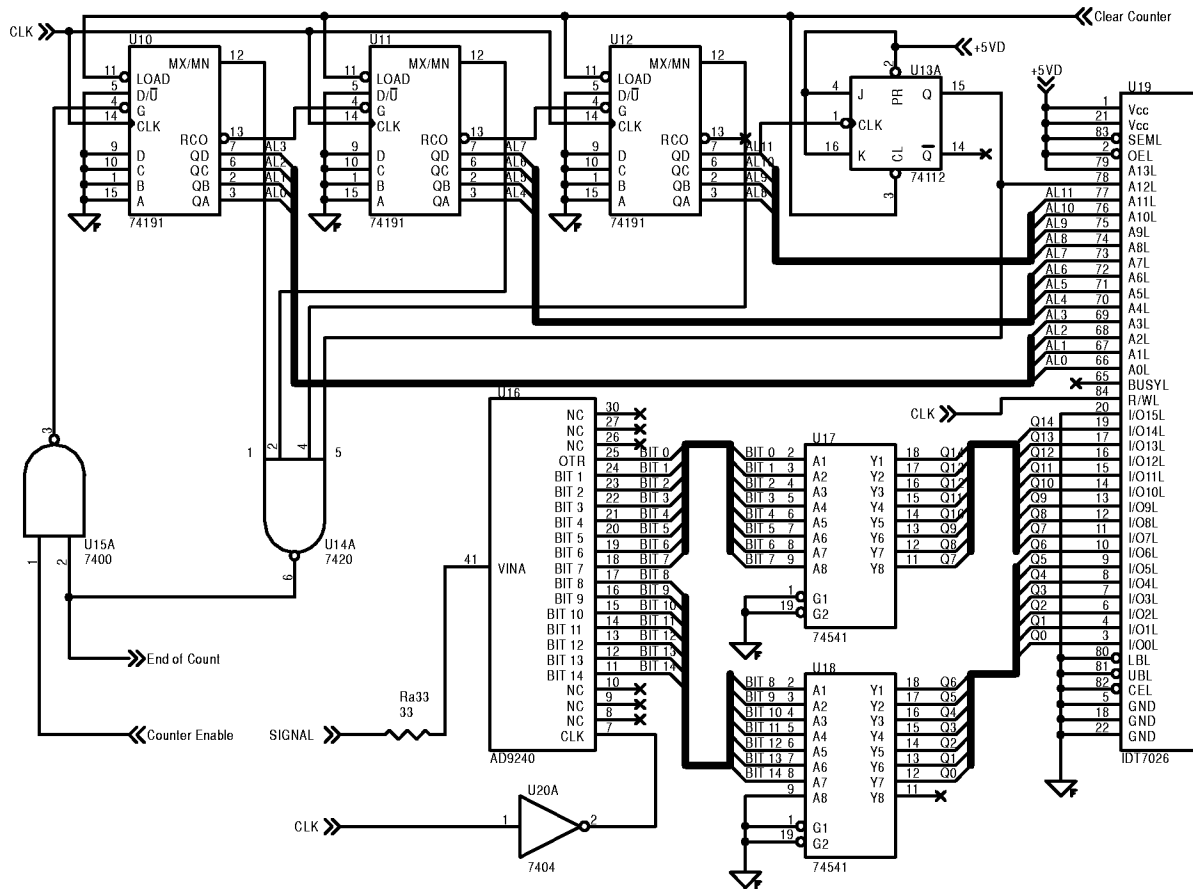


Figure 12. Circuit diagram of data collect and store section.

The counter operation is fully controlled by the microcontroller. At the beginning of the circuit operation, the microcontroller sends a clear signal to the counter resetting its output to the left address 2000H equivalent to the right address C000H which is the first storage location in the RAM. The ADC output is continuously stored in this location until the trigger signal is received.

When the microcontroller senses the trigger signal, it sends a start count or “counter enable” signal to the counter causing it to address successive memory locations in the RAM in order to store the useful data. After scanning half the memory, when the counter reaches its maximum count of 1FFFH, which is equivalent to memory in the address of 3FFFH, an “end-of-count” signal is sent back to the microcontroller indicating the end of the time window record. Therefore, the useful data are available to the microcontroller in the address range from C000H to FFFFH as shown in the memory map in figure 13. (See refs. 21, 22, and 23.)

4.2. Microcontroller

The 16-MHz microcontroller, U23, is shown in figure 14. The memory map of the microcontroller and the RAM is shown in figure 13. The microcontroller address and data are shared on the same bus. Therefore, U21 and U22 are used for address latching. The microcontroller address is decoded by using U20B to access the right address of the RAM, U26A to access the FIFO, and U26B to access the dip switch. The memory section, starting with the nibble 7, is reserved to access the FIFO as discussed in section 4.3. The memory section, starting with the nibble 6, was reserved for the control word, set by

3FFFH	ADC output data storage	FFFFH
2000H		C000H
1FFFH	Data averaging	BFFFH
0000H		8000H
	FIFO	7FFFH 7000H
	Control word	6FFFH 6000H
	NOT USED	5FFFH 4000H
	Internal program storage EPROM	3FFFH
		2080H
	NOT USED	
	Register file	00FFH 0000H

Figure 13. System memory map.

onboard 8-bit dip switches S1. The “not used” address range from 4000H to 5FFFH can be used for system upgrades to the microcontroller.

After the counter end-of-count signal is detected by the microcontroller, it starts to transfer and add the data from the upper half of the RAM to the lower half for averaging. By the end of each averaging cycle, the data are transferred to the FIFO waiting to be transferred another time to the reading device. The dip switch output is buffered using U24, and this was used to give the microcontroller a control word to indicate the averaging times required, with a maximum of 4 averages, and the record length which could be 1, 2, 4, or 8k corresponding to 102.4, 204.8, 409.6, or 819.2 μ s, respectively. For record length less than 8k, the ADC data still are stored in 8k and the first 4k, 2k, or 1k are considered and the rest of the data are neglected.

One advantage of the selected microcontroller is its built-in 8-channel 10-bit ADC. Two of these channels are reserved for the detector bias voltage and temperature monitor readings. Finally, serial communication is allowed between the microcontroller and the computer via J2, a 9-pin D-connector for further simple commands or checking transfers. (See refs. 23, 24, and 25.)

4.3. Output Stage

Figure 15 shows the circuit diagram of the output stage of the digital card. The FIFO is formed by a parallel connection of U27 and U28 which are 8k, 9-bit FIFO's to form an 18-bit word to handle the 16-bit data. The output data were buffered by using U29 and U30 and then applied to U31, U32, U33,

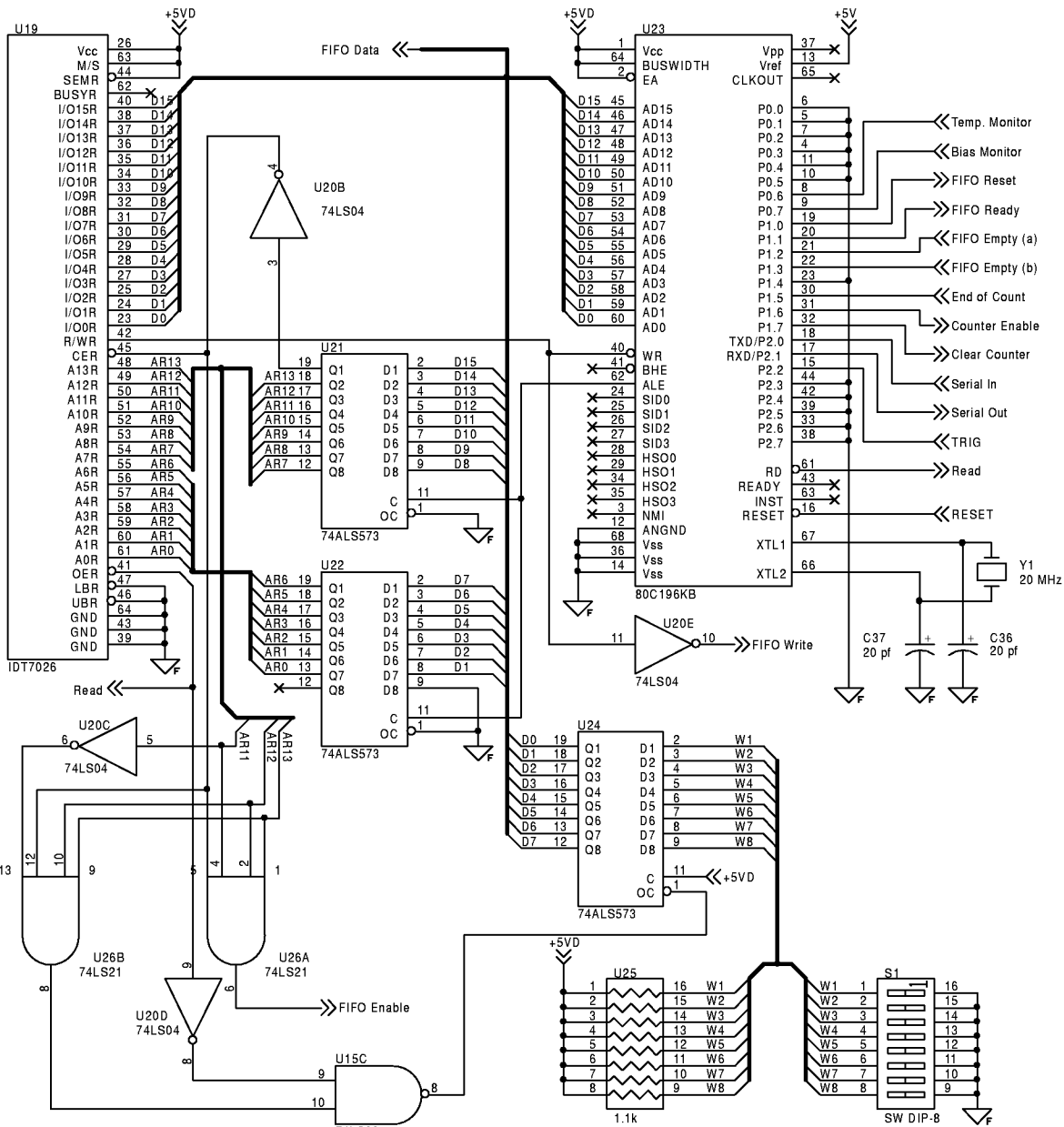


Figure 14. Microcontroller connection circuit.

and U34 which are 4-channel, TTL compatible optical isolators. These isolators are used to isolate the circuit and the reading device grounds. Finally, the data were read with J1, a SCXI connector. The FIFO operations are controlled by the microcontroller, whereas the FIFO read is controlled by the reading device. In order to check the correct sequence of data handling, the empty flags of both FIFO's are read by the microcontroller. Any unequal state of these flags indicates a FIFO failure or data crash.

After the microcontroller sends the complete data set to the FIFO, it sends a "FIFO ready" signal to the reading device to synchronize it with the system. Both the FIFO ready and FIFO read signals are also optically isolated by U37, which are dual separate channel optocouplers, once again to separate the grounds. Finally, the microcontroller controls the FIFO reset signal in order to reset the FIFO before the first writing operation. (See refs. 26, 27, and 28.)

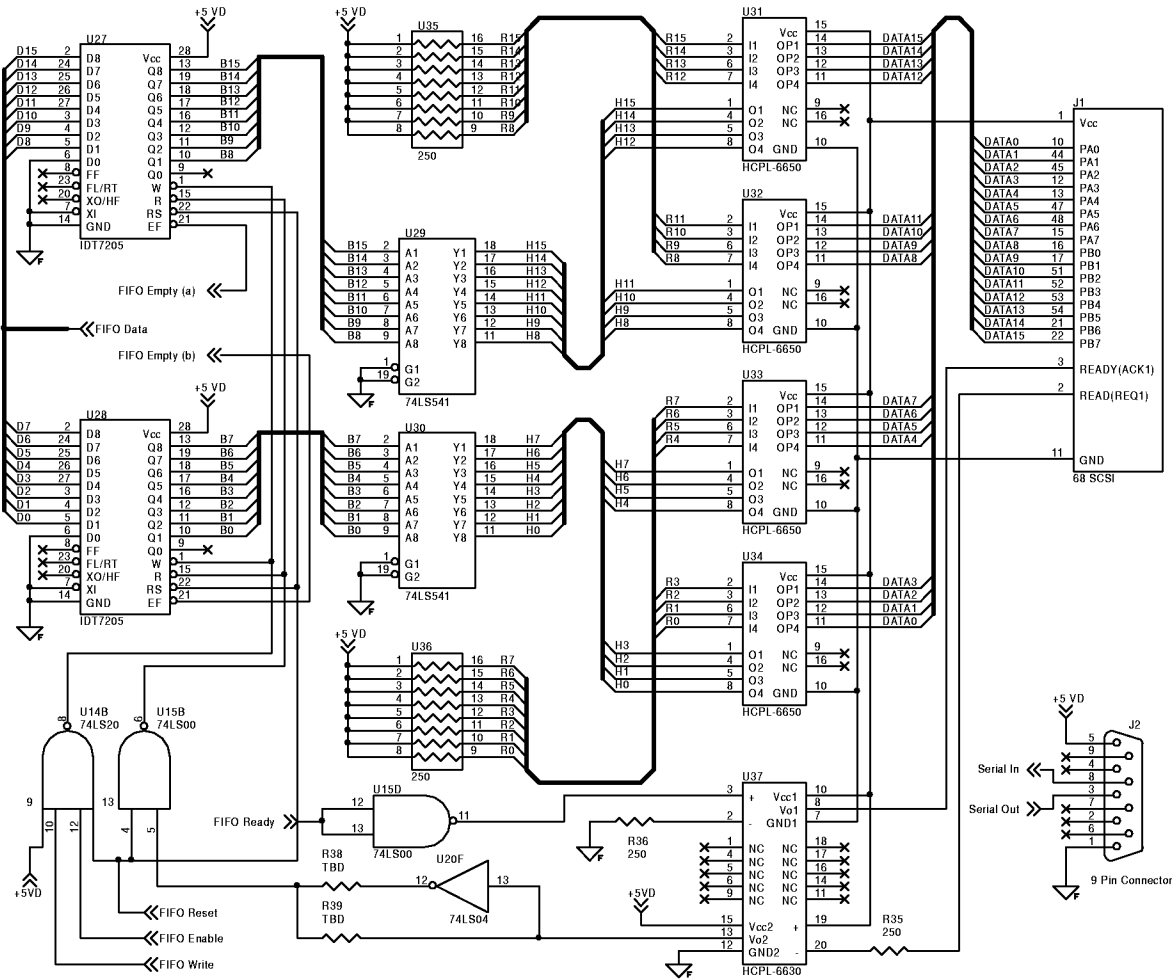


Figure 15. Schematic diagram of output stage.

5. Design Operational Testing

The described system was built on one 312-gm, $15 \times 9 \text{ cm}^2$ printed circuit board by using surface mount technology. This was very challenging because of the sensitivity of the different elements to the board layout because accurate analog signals were subjected to different pick-up noise sources from the high switching frequency digital signals. Therefore, the board layout was carefully designed to separate the analog and digital circuits on the two board sides with complete ground isolation between them. Furthermore, the whole detection system is optically isolated from any external instrument such as the clock generator, trigger input, and computer. The only electrical connection between the detection system and any external device is through the power supplies. That connection was taken care of by proper filtering and isolating the power grounds from the circuit grounds. The estimated power consumption of the card is 21.1 W (appendix D). In this section, we discuss the operational testing of the final board.

5.1. Analog Circuit Testing

The testing of the analog circuit started by checking the operation of the APD voltage controller. The output high voltage was observed to be very stable, with about a 2-ms settling time. After checking the temperature controller at a room temperature of 22°C , it was observed that setting the APD

temperature to a low value of 0.6°C required forced cooling to stabilize its operation. This points out the design requirement of an APD heat sink to stabilize its operation. The controller settling time in this case was about 30 sec with a steady state TEC current of 0.5 A.

Testing of the signal conditioning stage indicates its linearity with input signals in the digitizer range. Above this range, clipping starts and the stage becomes nonlinear as shown in figure 16. The noise equivalent power contribution of this stage to the detected signal was estimated to be 4.8 fW/Hz^{1/2} which is added to the detector NEP of 1.9 fW/Hz^{1/2}. With a system bandwidth of 2.5 MHz, this gives a total NEP of 10.6 pW, which is equivalent to the minimum detectable signal level as shown in figure 17. Setting this NEP to be equivalent to two digitizer counts defines the total gain of the signal conditioning stage and the maximum detectable signal level. This gives a total dynamic range for the detection system of about 8000. For wider dynamic range a multichannel detection system needs to be used.

5.2. Digital Circuit Testing

The digital circuit was built by using the same design discussed previously. A 12-bit digitizer was used instead of the 14-bit digitizer and an Intel VLSiCE-96 emulator was used to simulate the microcontroller chip as shown in figure 18. An advantage of using the emulator was to check several operating programs by using a personal computer to test the different system parts without burning a new microcontroller chip each time.

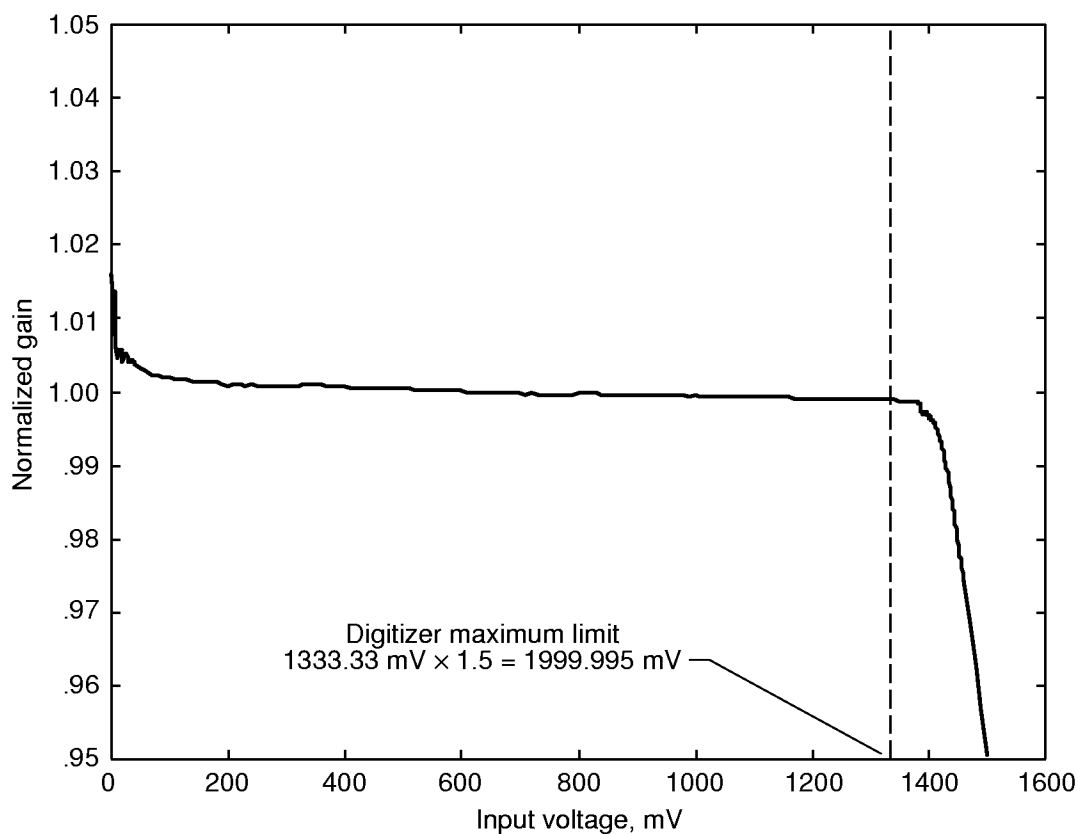


Figure 16. Linearity check of signal conditioning stage. Normalized gain = $(V_{out}/V_{in})/(\text{Mean gain})$; Mean gain = 1.5; Gain nonlinearity = 1.5 percent.

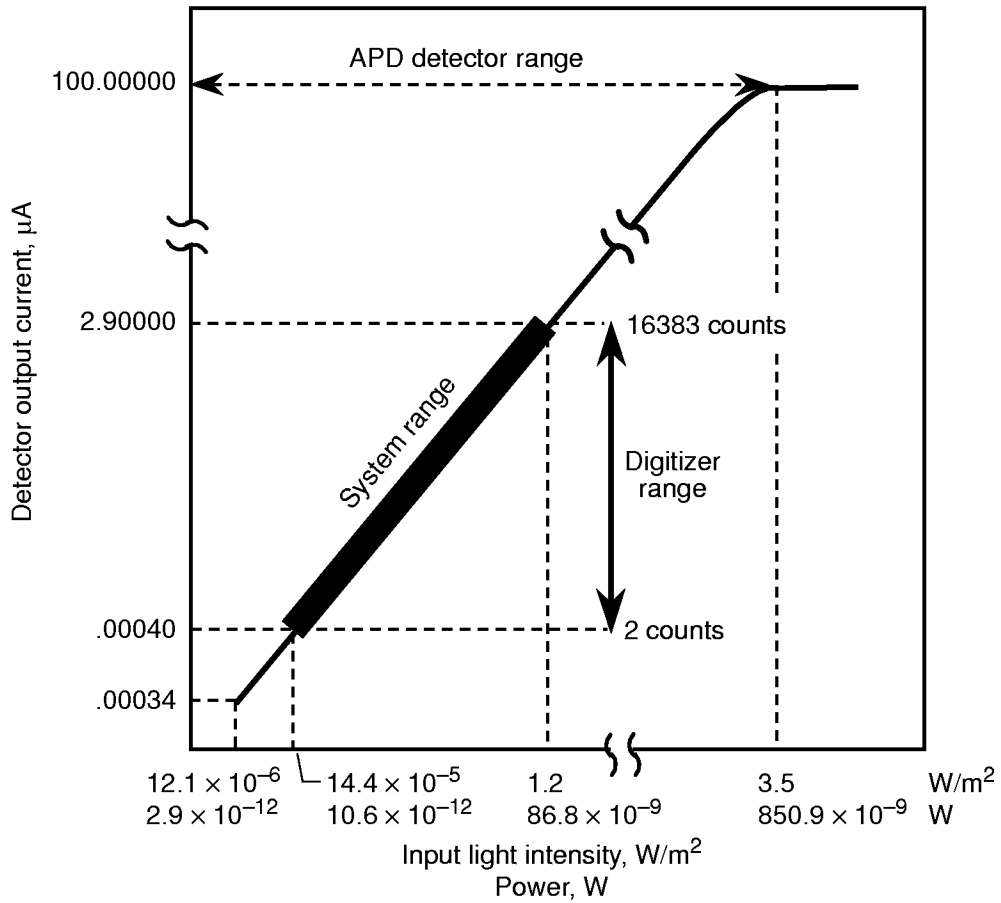


Figure 17. System and APD dynamic ranges obtained at APD operating conditions of 336 V, 0.6°C, 788 nm, and 117.5 A/W.

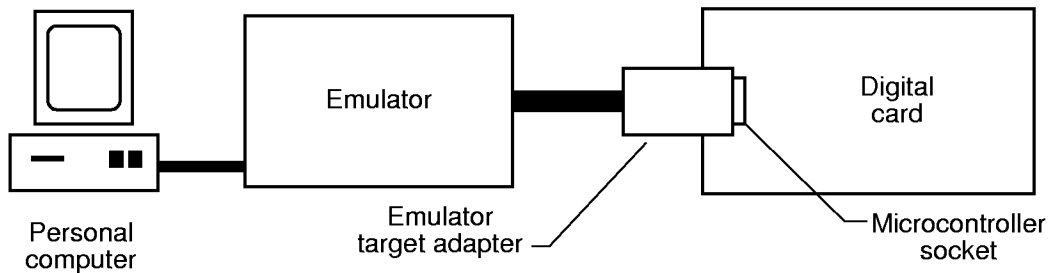


Figure 18. Emulator setting.

The operational testing of the digital circuit proceeded as follows:

1. Checking microcontroller ability to read the 8-bit dip switches with different switches settings
2. Checking microcontroller communication with serial ports for both read and write operations
3. Checking microcontroller communication with RAM for both read and write operations
4. Checking microcontroller write operation to the FIFO
5. Checking the digitizer operation
6. Checking the 13-bit counter operation and the digitizer data storage in the RAM
7. Checking the FIFO data read operation

Figure 19 shows the experimental setup for checking the operation of the whole detection system. The final data are read and stored in a personal computer by using a National Instruments PCI-DIO-32HS digital input-output interface card. The lidar return signal was simulated by a laser diode output, at a 788-nm wavelength. Figure 20 shows the plot of a simulated lidar return impulse with no averaging.

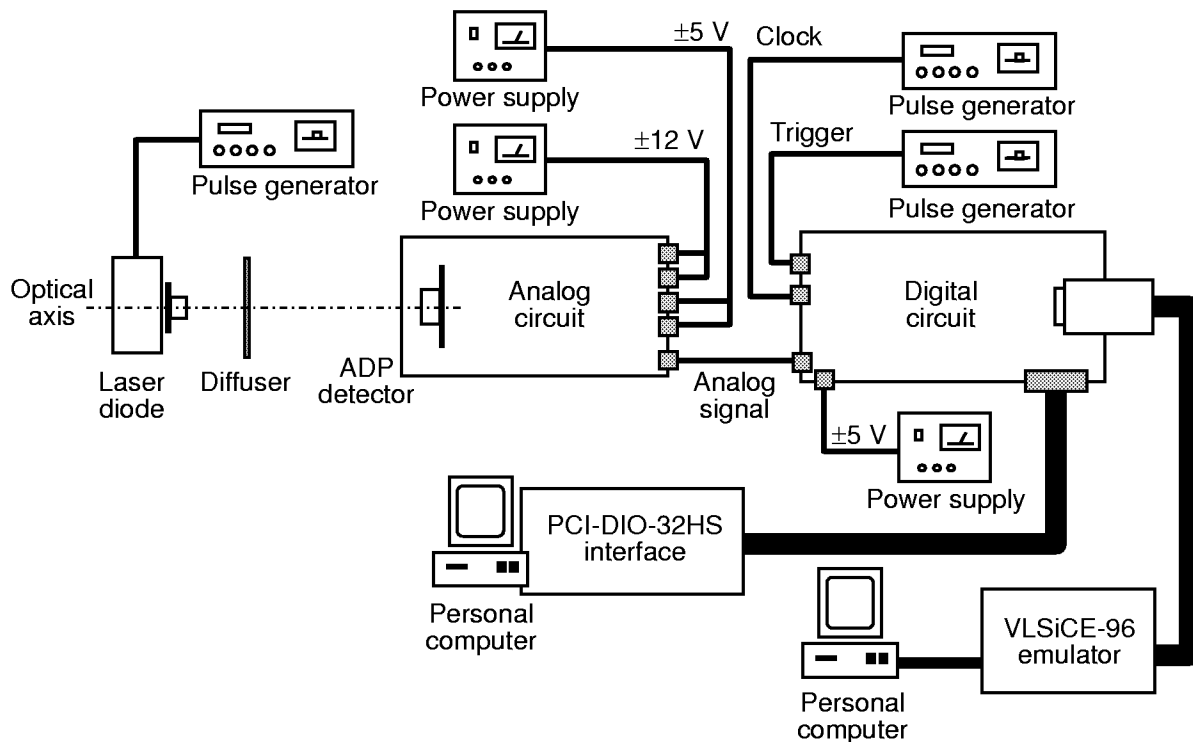


Figure 19. Experimental setup for detection system operational testing.

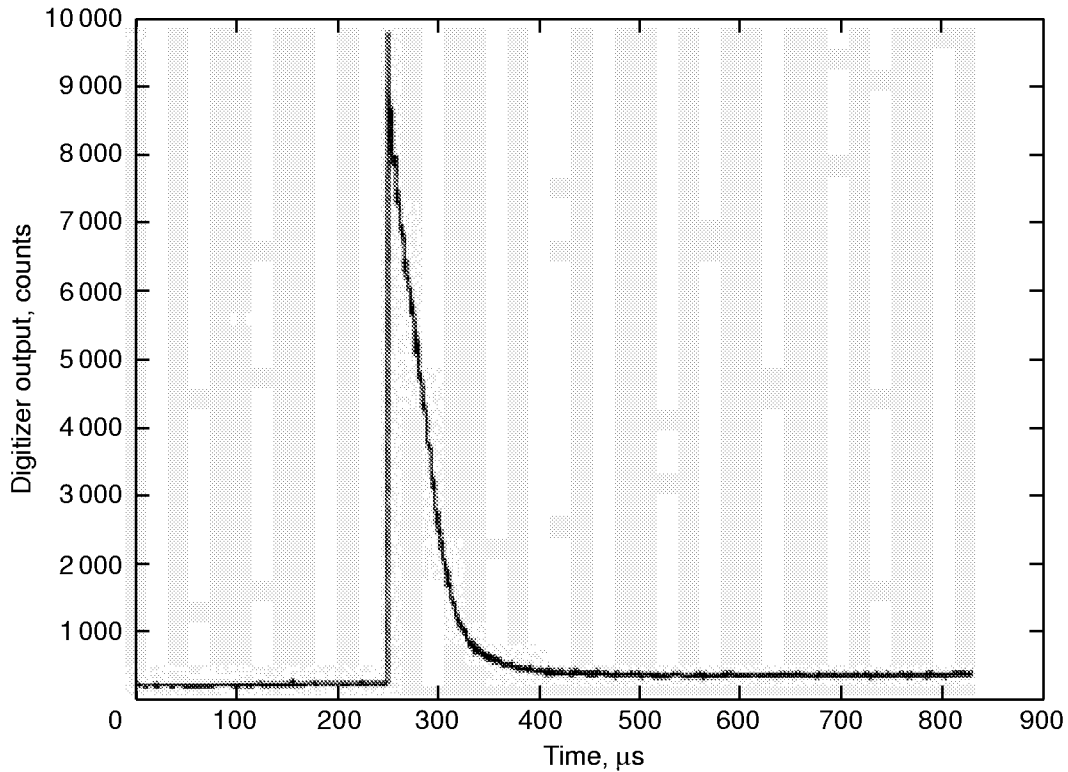


Figure 20. Detection system output for simulated lidar return signal.

6. Concluding Remarks

The complete design of a water vapor DIAL detection system with an advanced avalanche photodiode (APD) detector and state-of-the-art electronics was discussed. The system design mainly consists of an analog circuit and a digital circuit. The analog circuit consists of an APD detector package, including a built-in thermoelectric cooler and a transimpedance amplifier, and a signal conditioning stage. Also it contains bias voltage and temperature controllers for stabilizing the APD operation. The digital circuit consists of a 14-bit, analog-to-digital converter for converting the detected analog signal into a digital format and a microcontroller for signal processing. The main goals of the design were to minimize the system noise, power consumption, mass, and volume to make it small enough to be placed on the receiver telescope and to make it compatible with a personal computer for future unpiloted atmospheric vehicle or space applications. The operation of the detection system was tested by a simulated lidar return signal and results show good system performance regarding the 8333 dynamic range, 21.1 W power consumption, and 250k words/s data transfer rate.

This design can be generalized for measuring atmospheric species other than water vapor by using the DIAL technique. Because of its compactness and low power consumption, it can also be used in space-based systems for continuous global atmospheric monitoring of water vapor and other species such as aerosols, CH_3 , CF_x , NO , NO_2 .

Appendix A

EG&G C30649E Detector Package

The manufacturer's test data sheet is shown in the following table:

Description	Condition	Minimum	Data	Maximum	Units
Positive bias current	V_r , dark, 25°C	11	18	22	mA
Negative bias current	V_r , dark, 25°C	5	7.1	15	mA
Output offset voltage	V_r , dark, 25°C	-1.5	0.19	0.5	V
APD breakdown voltage	$I_{hv} = 2 \mu A$, dark, 25°C	325	356	500	V
APD operating voltage	Resp = 50 MV/W, 25°C	300	349	480	V
APD dark current	V_r , dark, 25°C		7	35	nA
Spectral noise peak	V_r , dark, 25°C		150	150	nV/\sqrt{Hz}
Noise equivalent power	V_r , dark, 25°C		0.003	0.006	pW/\sqrt{Hz}
APD operating voltage	Resp = 50 MV/W, 0°C	290	336	470	V
APD dark current	V_r , dark, 0°C		4	15	nA
Spectral noise peak	V_r , dark, 0°C		140	150	nV/\sqrt{Hz}
Noise equivalent power	V_r , dark, 0°C		0.003	0.006	pW/\sqrt{Hz}
Bandwidth	$I_{hv} = 2 \mu A$, dark, 25°C	10	11		MHz

Tests were done at ± 5 V on amplifier with 50- Ω AC coupled.
 Test wavelength = 820 nm.
 Serial number 147.

The pin layout is shown in figure A1.

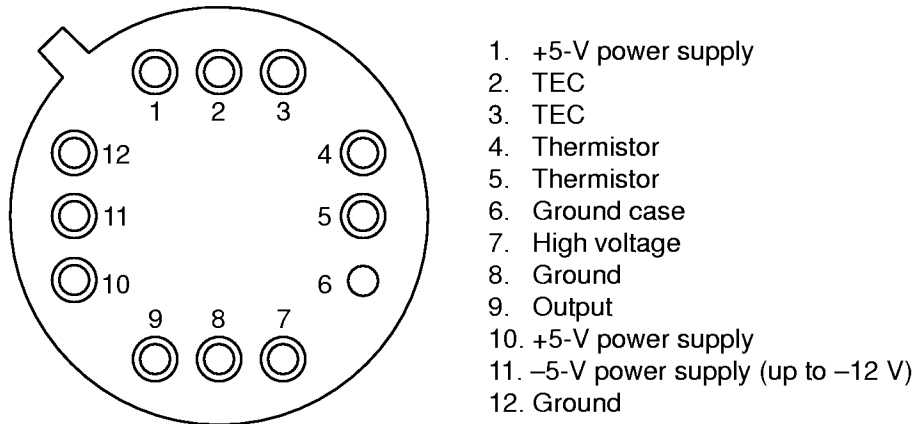


Figure A1. Pin layout.

The detector package circuit is shown in figure A2.

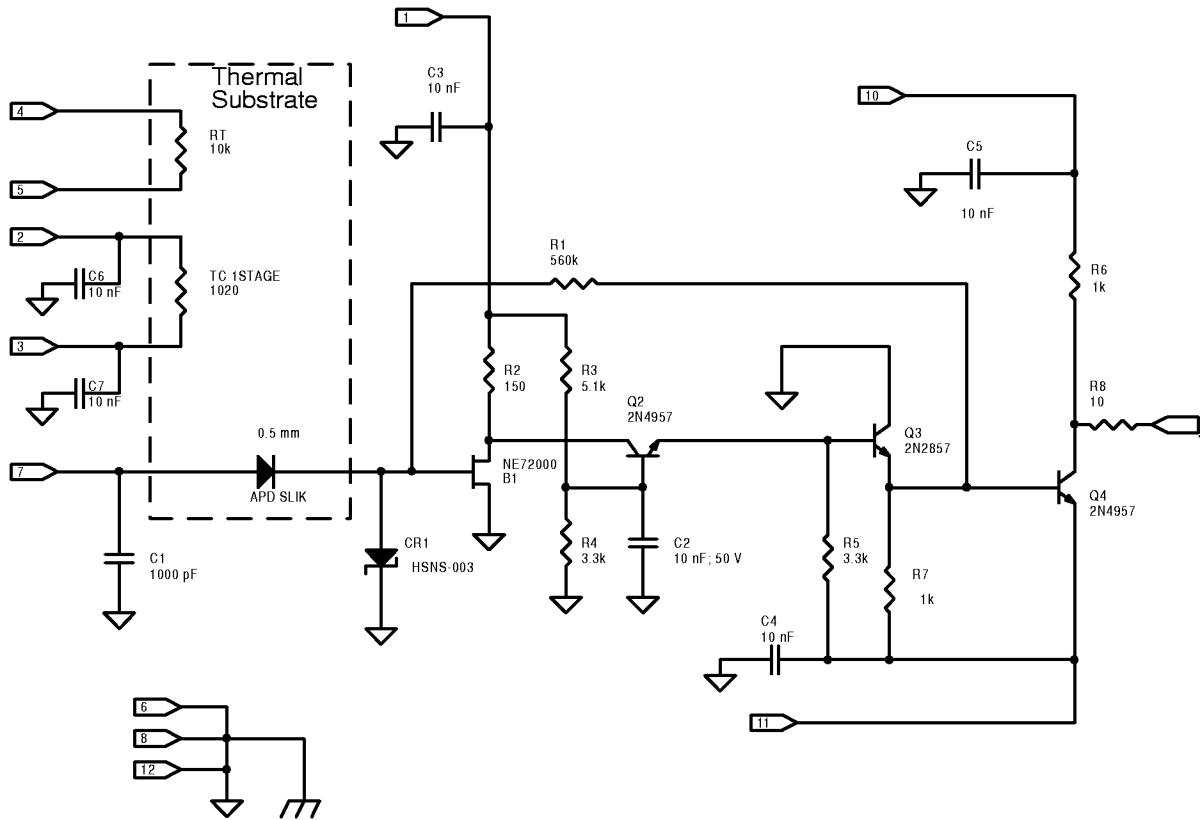


Figure A2. Detector package circuit.

Characteristics of the detector package are given as follows:

Detector sensitive area (measured), mm ²	0.24
Transimpedance amplifier feedback resistance, kΩ560
Detector maximum power loss, MW50
TEC maximum current, A	1.8
TEC rated current at 0°C, A	0.5
TEC area, mm ²3.96 × 3.96
Thermistor resistance R_T	$10^4 \exp \left[3940 \left(\frac{1}{T} - \frac{1}{298} \right) \right]$

Appendix B

Detection Card Components

The detection card components are given in the following table:

Part	Component	Number of parts per board	Description	Manufacturer
U1	AD586BR	1	+5-V reference voltage	Analog Devices, Inc.
U2,U3,U5	AD706AR	3	Dual operational amplifiers	Analog Devices, Inc.
U4	521-5-M	1	High-voltage power supply	Analog Modules, Inc.
U6	C30649E	1	Avalanche Photodiode	EG&G, Inc.
U7	AD8036AR	1	Clipping amplifier	Analog Devices, Inc.
U8	AD8041AR	1	Buffer and summer amplifier	Analog Devices, Inc.
U9	B3LL31-25-P/P	1	Output filter	K&L Microwave, Inc.
U10,U11,U12	74F191SC	3	4 bit counter	Fairchild Semiconductor Corp.
U13	TC74AC112FN	1	Dual JK flip flop	Toshiba Corp.
U14	TC74VHC20FT	1	Dual, 4 input NAND gates	Toshiba Corp.
U26	TC74VHC21FT	1	Dual, 4 input AND gates	Toshiba Corp.
U15	TC74VHCT00AFT	1	Quad, 2 input NAND gates	Toshiba Corp.
U16	AD9240AS	1	14 bit, 10 MHz ADC	Analog Devices, Inc.
U17,U18,U29,U30	TC74VHCT541AFT	4	Octal buffers, 3 state output	Toshiba Corp.
U19	IDT7026L20J	1	16k, 16 bit dual port RAM	Integrated Device Technology
U20	TC74VHC04FT	1	Hex inverters	Toshiba Corp.
U21,U22,U24	TC74VHC573FT	3	8 bit, address latch	Toshiba Corp.
U23	N87C196KB-16	1	Microcontroller	Intel Corp.
U27,U28	IDT7205L15J	2	8k, 9 bit, FIFO	Integrated Device Technology
U31,U32,U33,U34	HCPL-6650	4	4 channel optocoupler	Hewlett-Packard Co.
U37	HCPL-6630	1	2 channel optocoupler	Hewlett-Packard Co.
U38	HCPL-2430#300	1	2 channel optocoupler	Hewlett-Packard Co.
U25	766-163-R(1k)	1	1k, 2%, 160 mW, resistor network	CTS Corp.
U35,U36	766-163-R(270)	2	270, 2%, 160 mW, resistor network	CTS Corp.
D1,D3,D4,D5,D6, D7	LL4148DICT	6	Diode, 1N4148	Vishay Intertechnology, Inc.
D2	BZX84C5V1DICT	1	5.1 V, zener diode, 1N751	Vishay Intertechnology, Inc.
Q1	TIP110	1	Darlington transistor	Texas Instruments, Inc.
L1,L2,L4,L5,L16	NFM46P11C155	5	Noise suppression line filter	Murata Electronics

Part	Component	Number of parts per board	Description	Manufacturer
L3,L6,L7,L8,L9, L10,L11,L12,L13, L14,L15	BLM41A151S	11	Chip ferrite bead inductors	Murata Electronics
C8	1812Y104JXE	1	0.1 μ F, 500 V, 5% ceramic capacitor	Vishay Intertechnology, Inc.
C2,C10,C5,C5a	VJ1812Y105JXXMB	4	1 μ F, 25 V, 5% ceramic capacitor	Vishay Intertechnology, Inc.
C39,C40	PCC472BCT	2	5 nF, 50 V, 10% ceramic capacitor	Panasonic
C38	PCS1226CT	1	22 μ F, 6.3 V tantalum capacitor	Panasonic
C36,C37	PCC200CCT	2	20 pF, 50 V, 5% ceramic capacitor	Panasonic
C9	PCC220JCT	1	22 pF, 3 kV, 5% ceramic capacitor	Panasonic
C14,C17,C21,C23, C25,C29,C3u23	PCS3106CT	1	10 μ F, 16 V tantalum capacitor	Panasonic
Cu31,Cu32,Cu33, CU34,C1u37, C2u37,C1u19, C2u19,C3u19, C1u23	PCC1034BCT	6	0.01 μ F, 50 V, 10% ceramic bypass, coupling capacitor	Panasonic
C1,C3,C4,C6,C7, C11,C12,C13,C15, C16,C18,C19,C20, C22,C24,C26,C27, C28,C30,C31,C32, C33,C34,C35, Cu10,Ca35,Cu11, Cu12,Cu13,Cu14, Cu15,Cu17,Cu18, Cu20,Cu21,Cu22, Cu24,Cu26,Cu27, Cu28,Cu29,Cu30, C2u23	PCC104BCT	42	0.1 μ F, 50 V, 10% ceramic bypass, coupling capacitor	Panasonic
R32	895-0205	2	5 Ω , 10 W, 1% resistor	Vishay Intertechnology, Inc., Dale
R33,Ra33	P33ECT	2	33 Ω , 5% resistor	Panasonic
R21,R30,R31,R41, R42	P50FCT	5	50 Ω (49.9), 1%, 1206	Panasonic
R26	TNPW1206100B	2	100 Ω , 1%, 1206	Vishay Intertechnology, Inc.
R22	P130FCT	1	130 Ω , 1% resistor	Panasonic
R23	P140FCT	1	140 Ω , 1% resistor	Panasonic
R35,R36,R44,R45	P270ECT	4	270 Ω , 5% resistor	Panasonic
R27,R28,R29	TNPW1206301B	3	300 Ω (301), 1%, 1206	Vishay Intertechnology, Inc.

Part	Component	Number of parts per board	Description	Manufacturer
R6	P499FCT	1	500 Ω (499), 1% resistor	Panasonic
R40,R43	P620ECT	2	620 Ω , 5% resistor	Panasonic
R14,R34	P2KZCT	2	2 k Ω , 0.1%, 0850	Panasonic
R2	P3KZCT	1	3 k Ω , 0.1%, 0850	Panasonic
R1,R8,R24,R23	P10KZCT	4	10 k Ω , 0.1%, 0850	Panasonic
R13	P22KZCT	1	22 k Ω , 0.1%, 0850	Panasonic
R17,R15,R16,R37	P33KZCT	4	33 k Ω , 0.1%, 0850	Panasonic
R3	P49.9KFCT	1	50 k Ω (49.9k), 1%, 1206	Panasonic
R12	P82KZCT	1	82 k Ω , 0.1%, 0850	Panasonic
R4,R5,R19	P200KFCT	3	200 k Ω , 1% resistor	Panasonic
R9,R10,R11		3	2.55 M Ω	
R18,R38,R39			TBD	
R7,R20	SM4W103	2	10 k Ω , POT, 10%	Philips Electronics
JP1,JP2,JP3,JP4	SPE1211	2	Jumpers	Specialty Electronics, Inc.
J1	777600-01	1	68 pin, SCSI connector	AMP
J2	AFR09G	1	9 pin D connector (Female)	AMP
J3	AMR09G	1	9 pin D connector (Male)	AMP
S1	CT2198MST	1	8 pin, dip switches	CTS Corp.
S2	P8087SCT	1	Push button switch	Panasonic
Y1	XC550CT	1	16 MHz crystal oscillator	ECS, Inc.
	SK-PLCC68-S01	1	68 pin, PLCC socket	Ironwood Electronics, Inc.

Appendix C

Auxiliary Circuits

C1. Analog-to-Digital Converter Setting

The AD9240 is a 10M sample per second, 14-bit ADC. It has an on chip low noise sample, and hold amplifier and a programmable voltage reference. Figure C1 shows the associated programming circuit in our application. C32, C33, C34, C35, and Ca35 are 0.1 bypass capacitors between each supply and its corresponding ground pin. The AD9240 maximum conversion rate can be controlled by R34. VINA and VINB are two analog inputs for either a differential input mode or single ended mode. By connecting VINB to VREF and SENSE via R33, the second mode is selected, with a common mode at 1 V with a 2-V input range. The chip internal reference, which appears on CAPT and CAPB, is used in this connection. C28, C29, C30, and C31 form the recommended decoupling network to ensure a stable reference. This device provides the only connection between the analog and the digital grounds.

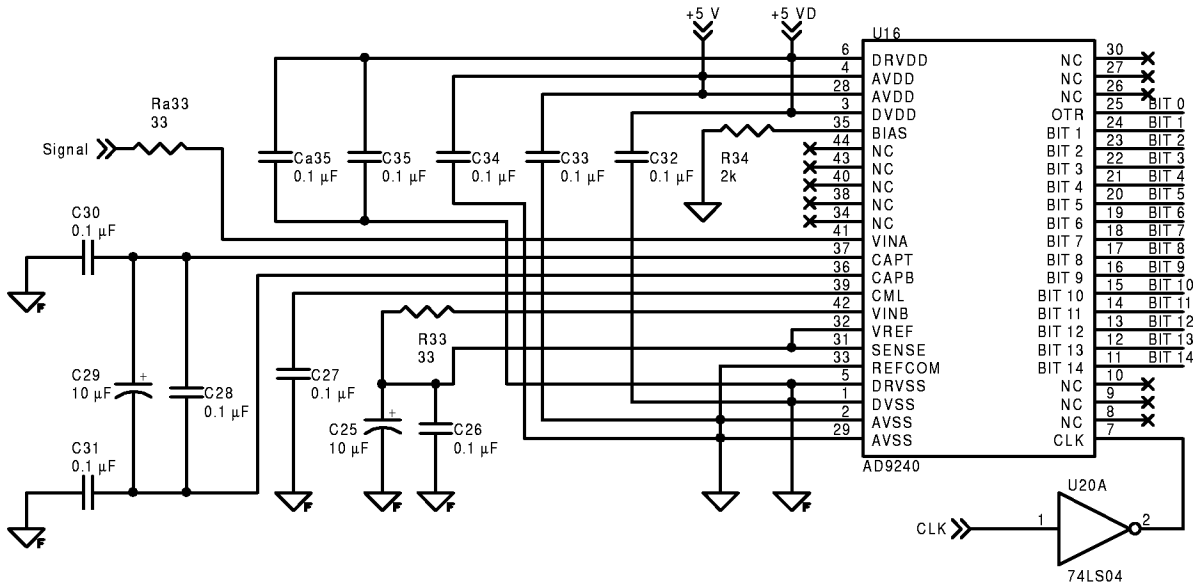


Figure C1. Analog-to-digital converter circuit.

C2. Microcontroller Analog-to-Digital Converter

The 16-MHz, 87C196KB microcontroller has an internal, 8-channel, 10-bit ADC. Two of these channels are used for APD bias and temperature monitoring. Figure C2 shows the interface circuit between the monitor signal and the microcontroller input pin. Diodes D4 and D5 provide a voltage overload protection to the device. R44 and C39 are low pass filter for high-frequency noise elimination.

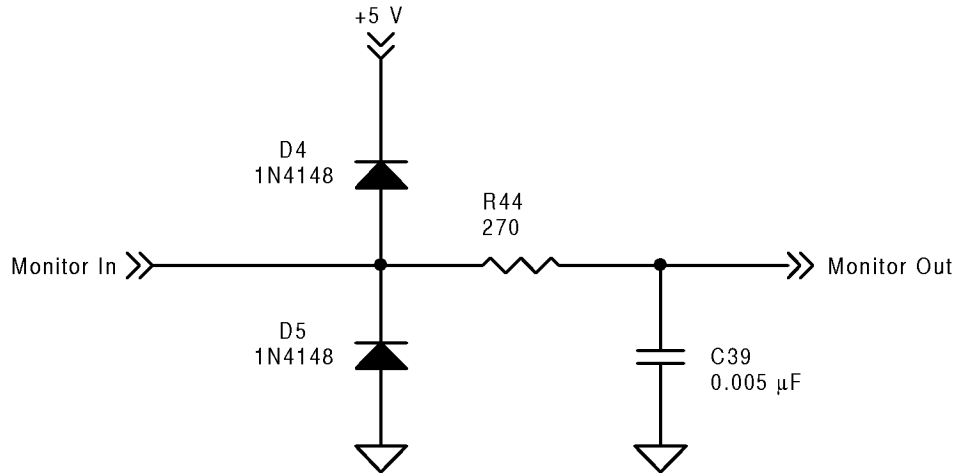


Figure C2. Microcontroller ADC interface per channel.

C3. Microcontroller Reset

At the beginning of the circuit operation, the microcontroller must be reset, before it can perform any function. This is done by applying a low input to the RESET pin of the microcontroller chip. Figure C3 shows the reset circuit to perform this operation. S2 is a push button switch, with normally open state. At steady state, the capacitor C38 will charge to a voltage equal to the supply voltage and the RESET pin will be high. Closing S2 will discharge the capacitor, leading to apply the required low pulse to reset the device. Diode D3 is used to ensure that the capacitor voltage is less than the supply.

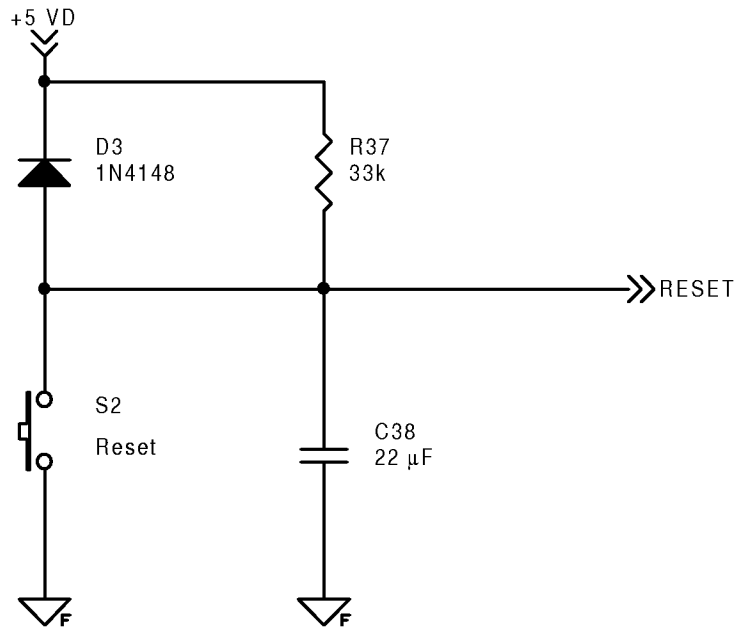


Figure C3. Microcontroller reset circuit.

C4. Chip Power Supply Bypassing

Generally, bypass or coupling capacitors are used with every supply pin of any device. It is used to supply the device with inrush currents required at switching instants. Figure C4 shows the used power supply bypassing for an op amp for both the positive and the negative supplies. Inductors Lx1 and Lx2 are used for smoothing the device bias current. Cx3 and Cx1 are 0.1- μF ceramic capacitors. As a layout restriction, these capacitors must be located less than 0.3 cm away from the supply pin. Cx2 and Cx4 are 10- μF electrolyte capacitors. For all devices other than op amps, 0.1- μF capacitors are only in use to couple every supply pin to the ground.

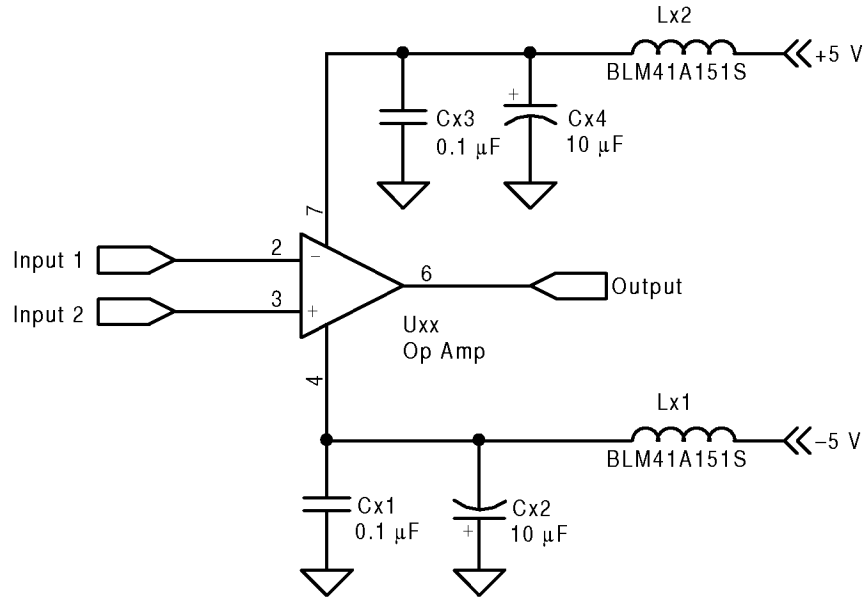


Figure C4. Op amp connection to bias power supplies.

C5. Clock and Trigger Isolation

U38, HCPL-2430, is a dual channel, TTL compatible optocoupler. It is used to optically isolate the clock and the trigger inputs as shown in figure C5. Resistors R41 and R42 are 50- Ω termination resistors. R40 and R43 are used to limit light emitting diode current.

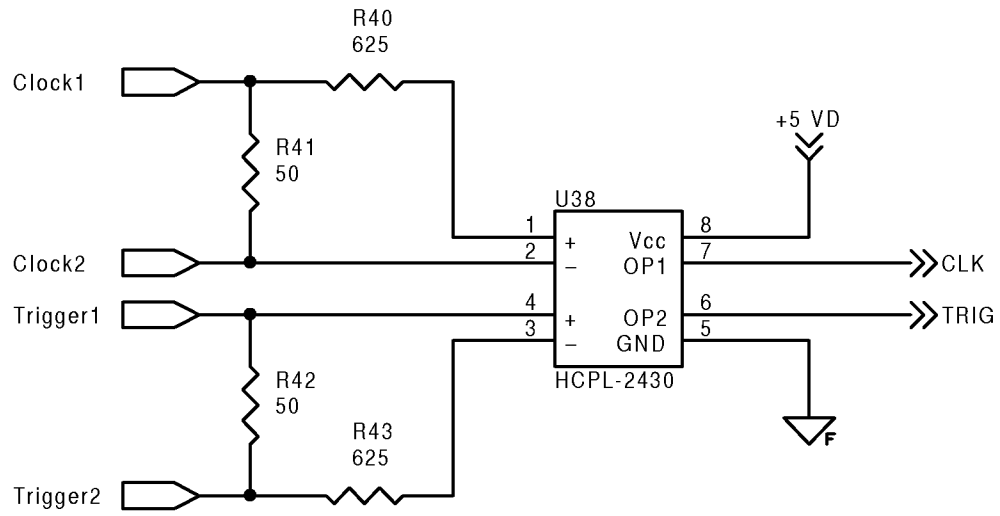


Figure C5. External clock and trigger isolation circuit.

Appendix D

Detection Card Power Consumption

The steady state maximum power consumption of the individual components of the detection system is as follows:

Reference voltage	P U1	500.00	mW	
	P U2	650.00	mW	
	P R1	2.50	mW	
	P R2	0.75	mW	
	Total power P1	<u>1153.25</u>	mW	
Signal conditioning	P U6	250.00	mW	
	P U7	900.00	mW	
	P U8	900.00	mW	
	P R21	45.00	mW	
	P R24	0.70	mW	
	P R25	0.70	mW	
	P R26	22.50	mW	
	P R27	67.50	mW	
	P R28	67.50	mW	
	P R29	67.50	mW	
	P R30	101.30	mW	
	P R31	101.30	mW	
	Total power P2	<u>2524.00</u>	mW	
Voltage controller	P U3	650.00	mW	
	P U4	480.00	mW	
	P R3	0.50	mW	
	P R4	2.00	mW	
	P R5	2.00	mW	
	P R6	50.00	mW	
	P R7	2.50	mW	
	P R8	0.10	mW	
	P R9-11	20.70	mW	
	P R12	0.20	mW	
	P R13	0.10	mW	
	Total power P3	<u>1208.10</u>	mW	
	Temperature controller	P U5	650.00	mW
P R14		24.50	mW	
P D2		16.70	mW	
P R15		0.40	mW	
P R16		0.40	mW	
P R17		0.40	mW	
P R19		0.20	mW	
P R20		14.40	mW	
P RT		0.40	mW	
Total power P4		<u>707.40</u>	mW	
		P R32	625.00	mW
		P Q1	1875.00	mW
		P TEC	124.00	mW
Total power P5	<u>2625.00</u>	mW		

Data collect and store			
	P U10	100.00	mW
	P U11	100.00	mW
	P U12	100.00	mW
	P U13	180.00	mW
	P U14	180.00	mW
	P U15	180.00	mW
	P U16	285.00	mW
	P U17	180.00	mW
	P U18	180.00	mW
	<u>Total power P6</u>	<u>1485.00</u>	<u>mW</u>
Microcontroller circuit			
	P U19	750.00	mW
	P U20	180.00	mW
	P U21	180.00	mW
	P U22	180.00	mW
	P U23	1500.00	mW
	P U24	180.00	mW
	P U25	181.80	mW
	P U26	180.00	mW
	<u>Total power P7</u>	<u>3331.80</u>	<u>mW</u>
Output stage			
	P U27	770.00	mW
	P U28	770.00	mW
	P U29	180.00	mW
	P U30	180.00	mW
	P U31	800.00	mW
	P U32	800.00	mW
	P U33	800.00	mW
	P U34	800.00	mW
	P U35	800.00	mW
	P U36	800.00	mW
	P U37	400.00	mW
	P U38	700.00	mW
	P R40	10.00	mW
	P R41	125.00	mW
	P R42	125.00	mW
	P R43	10.00	mW
	<u>Total power P8</u>	<u>8070.00</u>	<u>mW</u>

Total power for analog circuit from ± 5 -V supply = P2 + P5

$$= 2524.00 + 2625.00 = 5149.00 \text{ mW}$$

Total power for analog circuit from ± 12 -V supply = P1 + P3 + P4

$$= 1153.25 + 1208.10 + 707.40 = 3068.75 \text{ mW}$$

Total power for analog circuit = P1 + P2 + P3 + P4 + P5

$$= 5149.00 + 3068.75 = 8217.75 \text{ mW}$$

$$\begin{aligned}\text{Total power for digital circuit from +5-V supply} &= P_6 + P_7 + P_8 \\ &= 1485.00 + 3331.80 + 8070.00 = 12886.80 \text{ mW}\end{aligned}$$

$$\begin{aligned}\text{Total power for the card} &= P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 + P_8 \\ &= 8217.75 + 12886.80 = 21104.55 \text{ mW}\end{aligned}$$

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13. ABSTRACT (Maximum 200 words) The measurement of atmospheric water vapor is very important for understanding the Earth's climate and water cycle. The lidar atmospheric sensing experiment (LASE) is an instrument designed and operated by the Langley Research Center for high precision water vapor measurements. The design details of a new water vapor lidar detection system that improves the measurement sensitivity of the LASE instrument by a factor of 10 are discussed. The new system consists of an advanced, very low noise, avalanche photodiode (APD) and a state-of-the-art signal processing circuit. The new low-power system is also compact and lightweight so that it would be suitable for space flight and unpiloted atmospheric vehicles (UAV) applications. The whole system is contained on one small printed circuit board (9 x 15 cm ²). The detection system is mounted at the focal plane of a lidar receiver telescope, and the digital output is read by a personal computer with a digital data acquisition card.			
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