DESIGN OF THE TRANSCONDUCTANCE AMPLIFIER FOR FREQUENCY DOMAIN SAMPLING RECEIVER

A Thesis

by

XI CHEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2009

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Sebastian Hoyos
Committee Members,	Jose Silva-Martinez
	Peng Li
	Rainer Fink
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ABSTRACT

Design of the Transconductance Amplifier for Frequency Domain Sampling Receiver. (May 2009)

Xi Chen, B.S., Fudan University, Shanghai, China

Chair of Advisory Committee: Dr. Sebastian Hoyos

In this work, the circuit implementation of the front-end for Frequency Domain (FD) Sampling Receiver is presented. Shooting for two different applications, two transconductance amplifiers are designed.

A high linear transconductance amplifier with 25 dBm IIP3 is proposed to form the high resolution and high sampling rate FD receiver. The whole system achieves an overall sampling rate of 2 Gs/s and resolution of 10 bits.

Another low noise transconductance amplifier exploiting noise cancelling is designed to build up the FD wireless communication receiver, which is an excellent candidate for Software Define Radio (SDR) and Cognitve Radio (CR). The proposed noise cancelling scheme can suppress both thermal noise and flicker noise at the front-end. The system Noise Figure (NF) is improved by 3.28 dB.

The two transconductance amplifiers are simulated and fabricated with TI 45nm CMOS technology.

ACKNOWLEDGEMENTS

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CHAPTER I

INTRODUCTION

In recent years, wireless communication standards are progressing very fast. Those standards lead to various modulation types, carrier frequencies and bandwidths. The prototype RF receivers and transmitters are only applicable to one particular standard. The concept of software defined radio (SDR) has been proposed to build up flexible and reconfigurable radio platform so that the receiver and transmitter can be programmed to accommodate multiple standards. The Frequency Domain (FD) receiver is an excellent candidate for SDR receiver [1]. The front-end design of the FD receiver is quite different from the traditional wireless communication receiver. The analog front-end of the FD receiver makes use of current integration so that a low noise transconductance amplifier (LNTA) is required instead of a voltage low noise amplifier (LNA). In some cases the LNTA is the only active circuit block in the whole front-end, so it is the most important part in the front-end that determines both the linearity and the noise performance of the whole receiver. As the first stage of the front-end, the amplifier should be able to provide good input matching, low output thermal noise current and large bandwidth to include multiple communication standards. Furthermore, good linearity is required to suppress intermodulation between different carriers. On the other hand, The CMOS technology continues to scale and the impact of flicker noise is more

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prominent. Simulation shows that the corner frequency could be up to several GHz with smallest size of transistors in 45 nm CMOS process, so that low NF is more difficult to access. New techniques are required to mitigate the effect of flicker noise.

Different types of LNTA need to be designed to fit various applications. In this thesis, systematic trade-offs in the FD receiver front-end are discussed and for different applications how to determine the specifications of the circuit block, especially the LNTA, is presented. To realize a high resolution and high sampling rate ADC system with the FD receiver front-end, a low gain and high linear LNTA is designed. To build up a small signal wireless SDR, a high gain LNTA exploiting noise cancellation is proposed.

The organization of the thesis is as follows. Chapter II gives a brief introduction to the FD receiver. Systematic simulations explore the impact of all key parameters. Base on those conclusions, chapter III explains how to design a LNTA that provides maximum achievable system Signal to Noise and Distortion Ratio (SNDR) to realize a high resolution and sampling rate ADC system. In chapter IV, another LNTA fits small signal wireless SDR is presented. The noise cancelling scheme is employed to cancel both thermal noise and flicker noise. The conclusions are provided in chapter V.

CHAPTER II

THE MULTI-PATH FREQUENCY-DOMAIN (FD) RECEIVERS

2-1. Basic structure of the multi-path FD receivers

The Multi-Path FD Receivers are composed of many parallel paths as shown in Fig.2-1. The wideband input signal is mixed with different local oscillator frequencies, which are normally distributed in the signal bandwidth. The mixers are followed by current integrators, which behave as low pass anti-aliasing filters. After mixing, the signal is shaped by the anti-aliasing filter, whose -3 dB bandwidth is BW/N, where BW is the bandwidth of the signal and N is the number of paths. Thus the signal bandwidth is

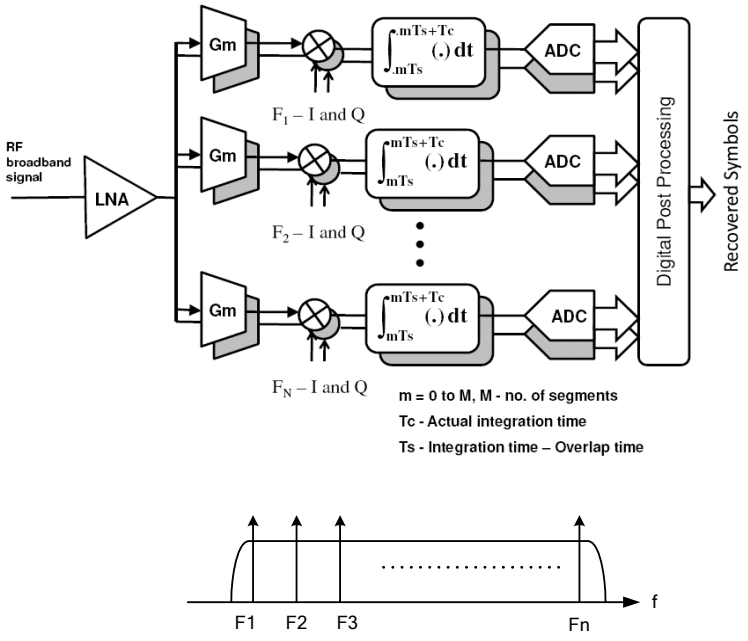


Fig.2-1 The basic structure of a FD receiver

separated into N parts, each of which is sampled by a following ADC. In other words, the input signal is expanded over a set of basis frequencies and sampled in frequency domain. The hardware requirements in each path are significantly relaxed. The required sampling rate for each path ADC is only 2BW/N, where 2BW is the Nyquist Rate. By combining all path ADCs together with the front-end, the whole receiver is able to accommodate large input signal bandwidth. The overall sampling frequency depends on the integration window in each path and the number of paths, while the resolution depends on those path ADCs. Both resolutions and sampling rates are scalable and flexible.

2-2. Basic circuit blocks in the FD receiver front-end

The front-end circuits include a LNA, Gm stage, Mixers and integrators.

1) LNA and transconductance amplifiers:

The anti-aliasing filter in each single path is provided by current integration so transconductance amplifiers (Gm stages) are required at the front-end to translate the input voltage signal into current. All the blocks after the Gm stages could be passive and will not introduce too much noise and distortions, so the LNA and the Gm stage dominate the noise performance and the linearity of the whole front-end.

The LNA and the Gm stage generate output thermal noise current whose density is $4kTgm$, where gm is the transconductance in their blocks. Besides, they generate flicker noise with density of K/f, where K is a constant that depends on the process,

size of transistors and the biasing current. The noise current is going to limit the Signal to Noise Ratio (SNR).

They also produce distortions which degrades the Signal to Distortion Ratio (SDR). Assuming the second and third order harmonics fall out of bandwidth of interest, the third order intermodulations (IM3) between different carriers that fall in band play important roles. That's why usually the non-linearity of a circuit block is dominated by IM3, so the third order input intercept point (IIP3) is the key parameter to evaluate the linearity of the block. The output power of the fundamental signal and the IM3 versus the input signal power is plotted in Fig.2-2.

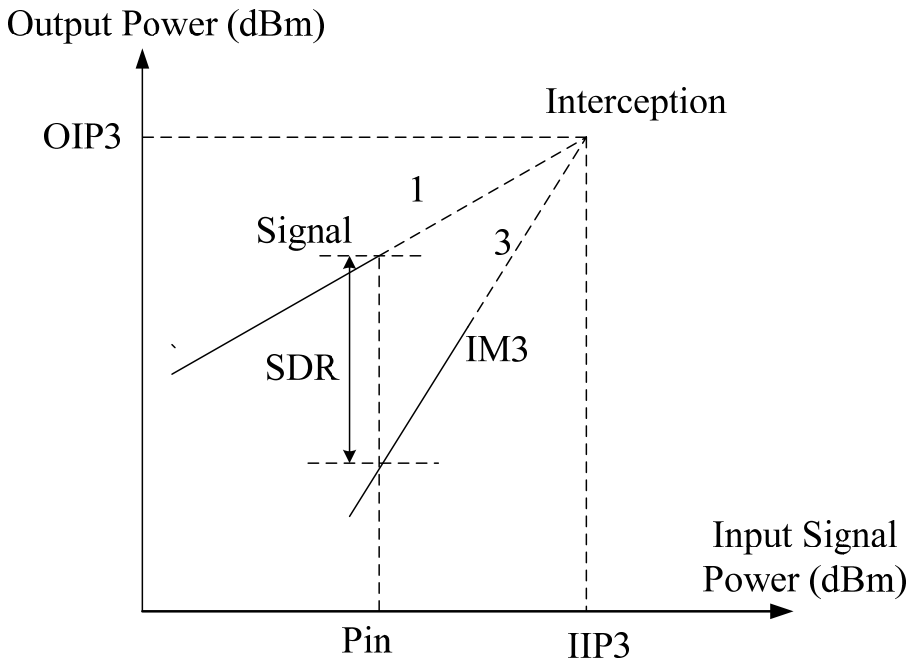


Fig.2-2 Definition of the IIP3

The slope of the signal line is 1 while the slope of the IM3 line is 3. The IIP3 is defined as the intercept point of the fundamental component with the third order intermodulation component. In real circuits this interception never happens because both signal and IM3 gets saturated before they hit the interception point. However, the IIP3 can still indicate the output SDR in the circuit in case the input signal power is given.

$$SDR_{output} = 2\left(IIP3 - P_{input,signal}\right)$$

Given the output noise current and the IIP3 of the LNA and the Gm stage, the noise performance and linearity of the whole system can be predicted. The specific circuit structures for LNA and Gm stage are discussed in chapter III and chapter IV.

2) Passive mixers:

The transconductance amplifiers are followed by passive mixers which will not introduce significant noise and distortion.

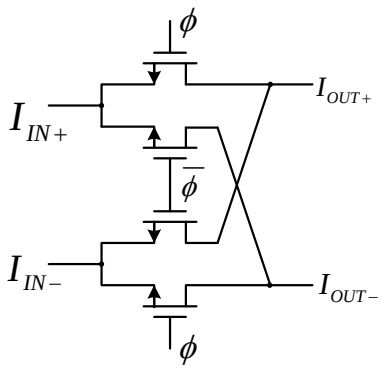


Fig.2-3 An example of the double balanced passive mixer

Double balanced passive mixer (Fig.2-3), which is composed of only four switches, is preferred due to low clock feed-through and signal feed-through. Transmission gates can be employed to reduce charge injection when the clock signal switches, but it doubles the area and the complexity of the clock wiring on chip.

3) Integrators, anti-aliasing filters and the sampling circuits:

The anti-aliasing filter and the sampling circuits are embedded in the integrator (Fig.2-4). After the mixer the signal current is directly integrated into the sampling capacitor and read out. The sampling capacitors are reset at the end of the integration window, providing a sinc type low pass anti-aliasing filter in frequency domain (Fig.2-5). The sinc type filter provides better attenuate at the nodes compared with the non-reset continuous integrator. The sampled data are read out before the reset. The sampling circuit has two interleaved branches so when one of the branches is being reset the other one can continue to sample the data. The simplified sampling circuit and the frequency response are shown below. The -3 dB bandwidth of the anti-aliasing filter is 1/2Tc so it is programmable with different controlling clocks.

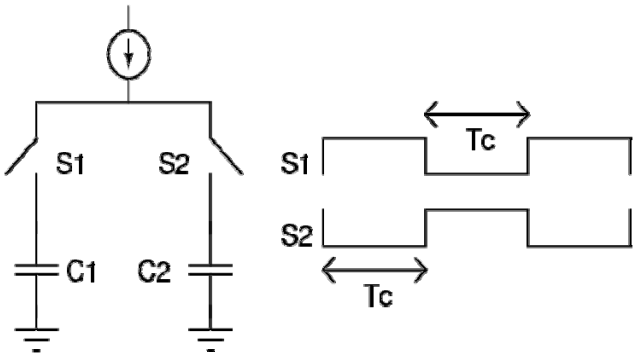


Fig.2-4 The two-branch current integrator/sampler and the integration windows

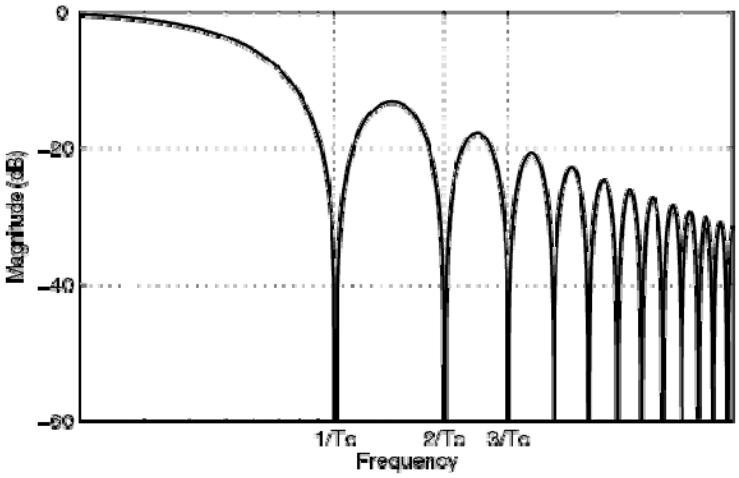


Fig.2-5 Frequency response of the windowed integration

A overall schematic including all the components in a single path of the front-end is shown in Fig.2-6. The circuit is differential.

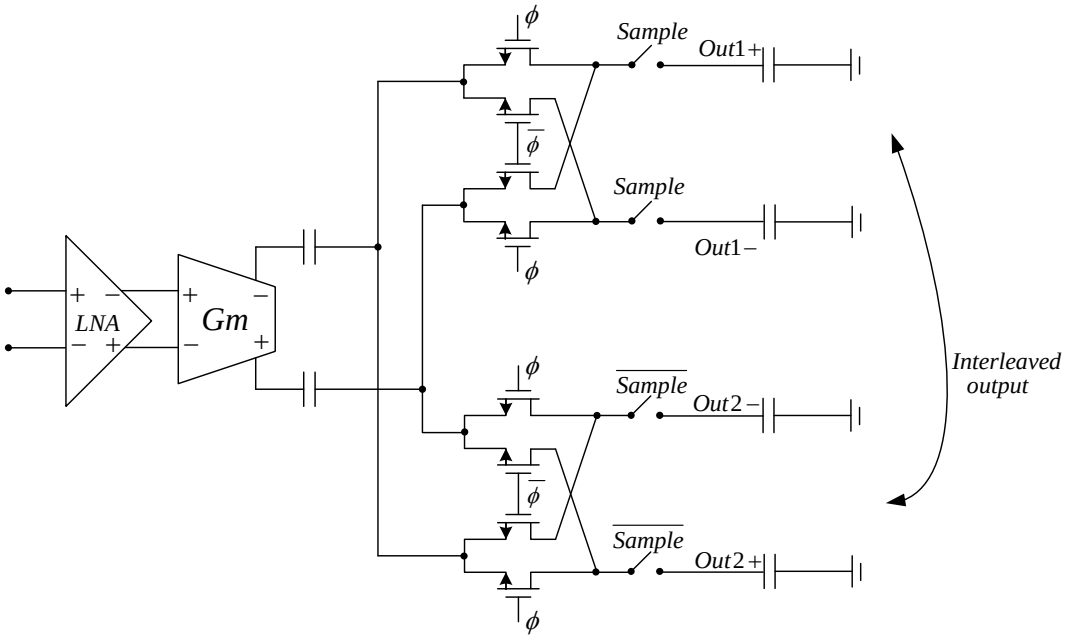


Fig.2-6 The schematic of a single path

2-3. Noise and distortions

The linearity and noise performance of the front-end circuits limit the maximum achievable system SNDR.

Key parameters that affect the system SNDR:

- The transconductance of the Gm stage, determining both the system gain and the output thermal noise current density of the Gm stage.
- IIP3 of the Gm stage, determining the linearity of the Gm stage and the whole system.
- P_{Gm}, the power consumption of the Gm stage, which gives a boundary for the IIP3 and the Gm.
- Ti, the length of the integration window, determining the sampling rate of the single path. It also determines how much gain is required to hit the full scale output amplitude.
- Cs, the size of the sampling capacitor.
- $V_{out,MAX}$, the maximum output signal amplitude at the sampling capacitor. Usually it is limited by the full scale input voltage range of the following ADC. In the following analysis assume $V_{out,MAX}$ =4 dBm.
- $V_{in,MAX}$, the maximum input signal amplitude. Assume $V_{in,MAX}$ =0 dBm.
- $\overline{V_{N,in}^2}$, the thermal noise density at the input of the front-end.

Let's consider a simplified diagram for a single path shown in Fig.2-7.

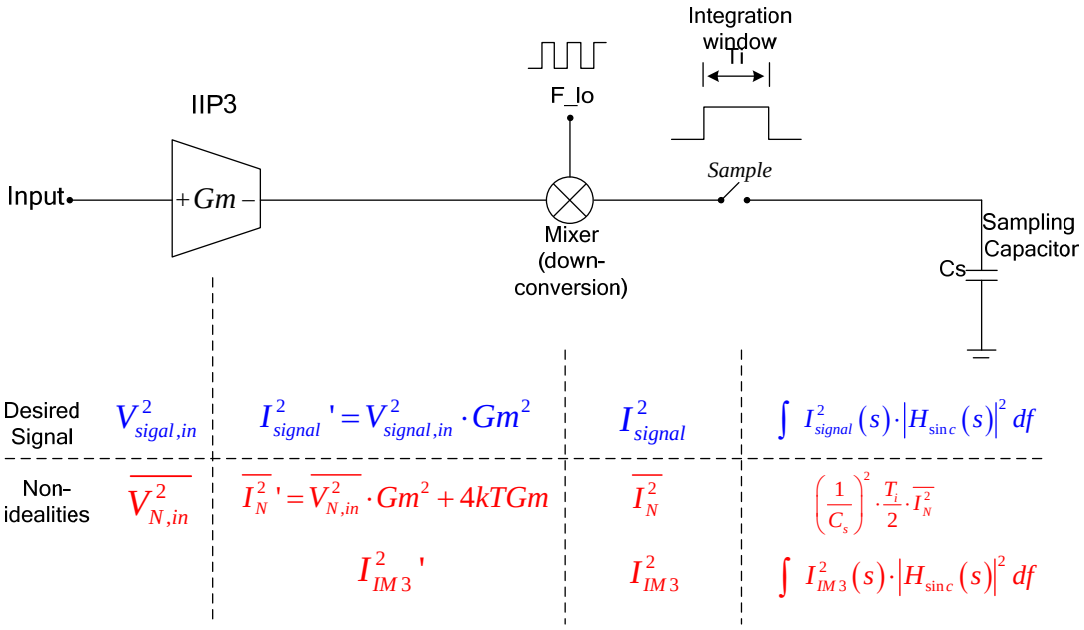


Fig.2-7 The simplified diagram of one path

The LNA is removed for simplification. Only thermal noise is considered in the following analysis. Two different units, which are Vrms and dBm, are used to present the power. Equations shown below are useful for transformation between Vrms and dBm.

$$P_{dBm} = 10 \cdot \log \frac{V_{rms}^2}{50} \cdot \frac{1}{1mW} = 10 \cdot \log\left(20 \cdot V_{rms}^2\right) \qquad (2\text{-}1)$$

$$V_{rms}^2 = 0.05 \times 10^{\frac{V_{dBm}^2}{10}} \qquad (2\text{-}2)$$

The input signal $V_{sigal,in}^2$ is translated into signal current by the Gm stage. At the output of the Gm stage,

$$I_{signal}^2 ' = V_{signal,in}^2 \cdot Gm^2 \qquad (2\text{-}3)$$

The current signal is mixed with the local oscillator signal. Given that the double-balanced hard switch passive current mixer is employed, the mixer provides $2/\pi$ of gain. After down-conversion,

$$I_{signal}^2 = \left(\frac{2}{\pi}\right)^2 \cdot I_{signal}^2{}' \qquad (2\text{-}4)$$

Finally the signal current is integrated into the sampling capacitor and shaped by the sinc type anti-aliasing filter. The sampled signal power is determined by the expression shown below,

$$V_{sig,out}^2 = \int I_{signal}^2(s) \cdot \left|H_{\sin c}(s)\right|^2 df \qquad (2\text{-}5)$$

The maximum output signal amplitude is achieved given that all input signal power focuses at F_lo then after down-conversion all signal power is at base band, getting the maximum gain from the anti-aliasing filter.

$$\left|H_{\sin c}(s)\right|_{MAX} = \left|H_{\sin c}(s)\right|_{s=0} = \frac{Ti}{Cs} \qquad (2\text{-}6)$$

in this case,

$$V_{sig,out,MAX}^2 = I_{signal}^2 \cdot \left(\frac{Ti}{Cs}\right)^2 \qquad (2\text{-}7)$$

where Ti is the length of the integration window.

The thermal noise comes from the input and the Gm stage. At the input, thermal noise with minimum noise density of -174 dBm/Hz is generated when the input impedance is matched to 50 ohms. This input noise is translated into noise current

through the Gm stage. The Gm stage also generates thermal noise current whose density is $4kTGm$. At the output of the Gm stage,

$$\overline{I_N^2}' = \overline{V_{N,in}^2} \cdot Gm^2 + 4kTGm \qquad (2\text{-}8)$$

$$\text{where } \overline{V_{N,in}^2} = -174dBm/Hz \qquad (2\text{-}9)$$

In the Sample & Hold circuit for voltage sampling, the on-resistance of the sampling switch generates thermal noise, whose sampled amplitude is kT/Cs in the sampling capacitor (Fig.2-8).

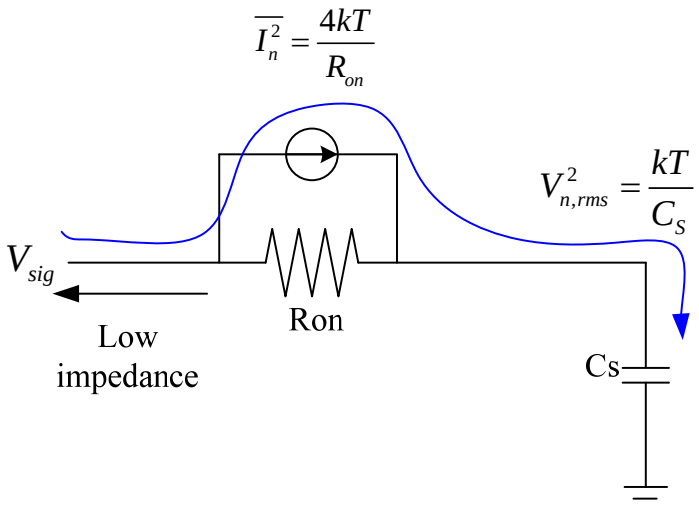


Fig.2-8 Sampled thermal noise in the S&H circuits

However, in the current sampling circuits (Fig.2-9), all the switches don't generate too much thermal noise because one of the terminals of the switch is connected to high impedance, which is the output resistance of the transconductance amplifier, thus the noise current generated by the on-resistance of the switch is circulating inside it and doesn't affect the sampling capacitor.

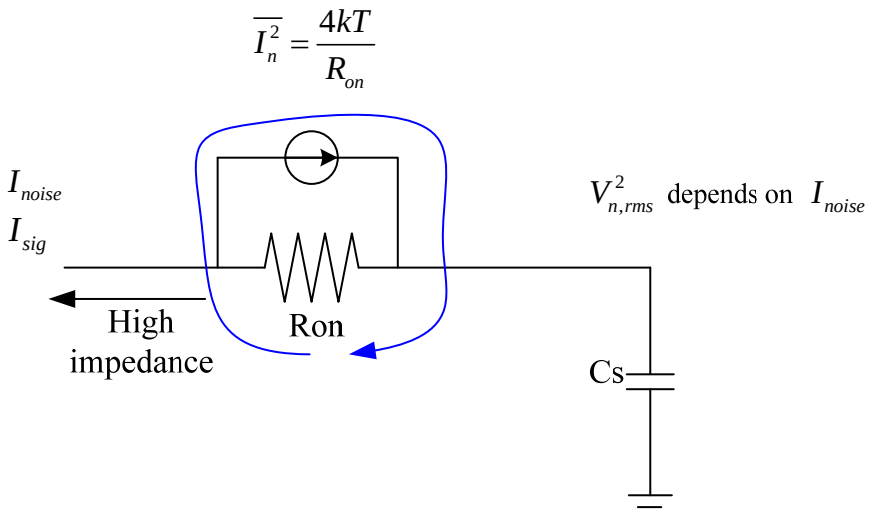


Fig.2-9 Thermal noise of Ron in the current sampling circuits

For the same reason, the passive mixer, which is simply a group of switches, doesn't generate significant noise. Assume I-Q modulation is employed, at the output of the mixer, the thermal noise doesn't get overlapped.

$$\overline{I_N^2} = \left(\frac{2}{\pi}\right)^2 \cdot \overline{I_N^2}' \qquad (2\text{-}10)$$

This noise current is integrated into the sampling capacitor, limiting the SNDR. The integrated thermal noise power in the sampling capacitor is determined by the expression shown below,

$$V_{output\_noise,rms}^2 = \int_0^\infty \overline{I_N^2} \cdot \left|H_{\sin c}(s)\right|^2 df \approx \left(\frac{1}{C_s}\right)^2 \cdot \frac{T_i}{2} \cdot \overline{I_N^2} \quad [2] \qquad (2\text{-}11)$$

Another thing that kills the SNDR is the distortion generated at the Gm stage. Finally the whole system will be built up differentially, so the dominant distortion is the third-order inter-modulation, which will fall in the signal band. At the output of the Gm stage,

$$I_{IM3,dBm}^2{}' = I_{signal,dBm}^2{}' - 2\cdot\left(IIP3_{Gm,dBm} - V_{signal,in,dBm}^2\right) \tag{2-12}$$

The passive mixer doesn't generate considerable distortion. After the down-conversion,

$$\overline{I_{IM3}^2} = \left(\frac{2}{\pi}\right)^2 \cdot \overline{I_{IM3}^2}' \tag{2-13}$$

The sampled distortion at the sampling capacitor is shown below,

$$V_{IM3,out}^2 = \int I_{IM3}^2(s)\cdot\left|H_{\sin c}(s)\right|^2 df \tag{2-14}$$

Actually the distortion power can be calculated by the input power and the IIP3 of the Gm stage

$$V_{IM3,out,dBm}^2 = V_{signal,out,dBm}^2 - 2\cdot\left(IIP3_{Gm,dBm} - V_{signal,in,dBm}^2\right) \tag{2-15}$$

The total SNDR at the sampling capacitor is determined by the expression shown below,

$$SNDR = \frac{V_{signal,out}^2}{V_{IM3,out}^2 + V_{output\_noise}^2} \tag{2-16}$$

For the whole receiver, quantization noise of the ADC should also be included. The resolution of the whole receiver is limited by the expression shown below.

$$SNDR_{Receiver} = \frac{V_{signal,out}^2}{V_{IM3,out}^2 + V_{output\_noise}^2 + Nq} \tag{2-17}$$

Additionally, based on some approximations, relationships between Gm, $IIP3_{Gm}$, and P_{Gm} can be represented by simple equations to explore the design trade-offs. In the

technology we are using, the Gm stage can provide 5 mS of transconductance per 1 mW of power consumption with IIP3 of 5 dBm.

$$\frac{Gm}{P_{Gm}} = 5mS / mW \Big|_{IIP3=5dBm} \qquad (2\text{-}18)$$

Assume there is no special technology to boost the IIP3, there is trade-off between *Gm* and IIP3 when the power consumption is fixed. Approximately,

$$k1 \cdot Gm_{dB} + k2 \cdot IIP3_{dBm} = \mathrm{K} \qquad (2\text{-}19)$$

where K is a constant determined by the power consumption and k1, k2 are coefficients that represents different weights of Gm and IIP3 in the expression. When the IIP3 is fixed, usually the Gm is roughly proportional to the power consumption so k1 is equal to one. However, when the Gm is fixed, it is more difficult to boost the IIP3 with additional power, so k2 is bigger than 1. In the following analysis, assume k is equal to 1.5. Based on equation (2-18), we get:

$$Gm_{dB} + 1.5 \cdot IIP3 = 20\log 5 + 20\log P_{Gm} + 5 \cdot 1.5dB \qquad (2\text{-}20)$$

Given that: $V^2_{out,rms,MAX,dBm}$ =4dBm, Gm =1mS, $IIP3_{Gm}$ =5dBm, Ti=5ns,

$\overline{V^2_{N,in}}$ =-174dBm/Hz, and the following ADC has resolution of 10 bits. The SNDR is plotted in the fig shown in Fig.2-10 when *Cs* is sweeping from 0.1pF to 1pF and the input signal power is sweeping from -80 dBm to 0 dBm.

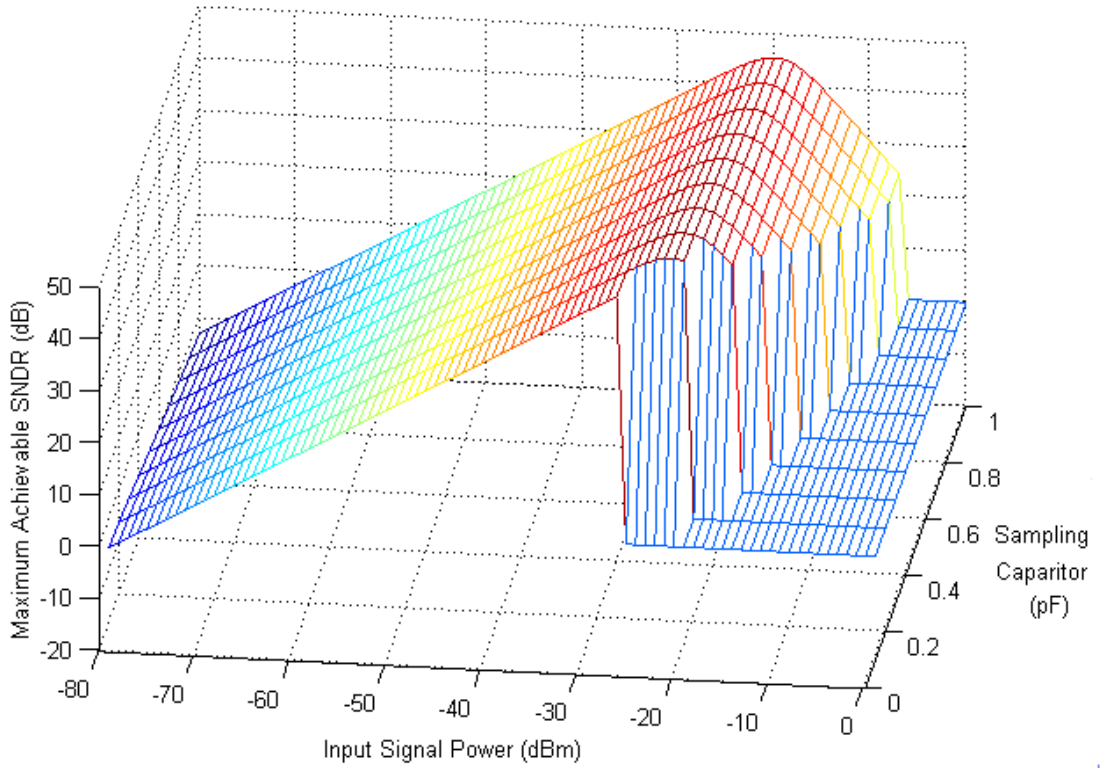


Fig.2-10 System output SNDR with Pin and Cs sweeping

With low power input signal, the SNDR is limited by the noise while with high power input signal the SNDR is limited by distortions. The SNDR hits the peak value when the input signal power is around an optimum point. The peak SNDR defines the Dynamic Range (DR) of the system. The value of Cs determines the output signal amplitude which is proportional to 1/Cs. When Cs is too small, the surface in the fig is cut off at the edge because the output exceeds the maximum allowed output amplitude so that the SNDR is not able to hit the peak value. On the other hand, when Cs is too big, the amplitude of the output signal is reduced and the quantization noise of the following

ADC starts to dominate. There is an optimum value of Cs that maximizes the Dynamic Range. The simplified plot for peak SNDR (DR) versus Cs is shown in Fig.2-11.

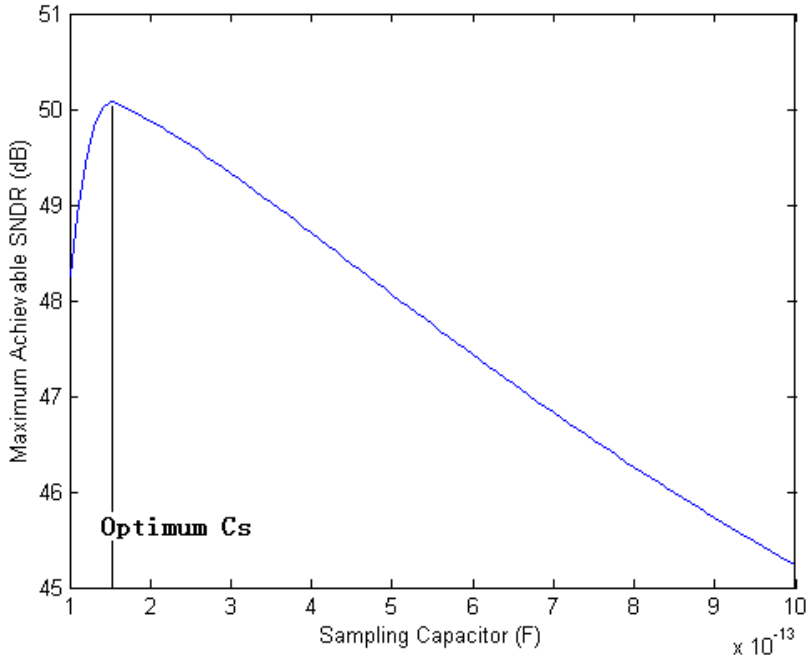


Fig.2-11 Maximum system output SNDR vs. sampling capacitor

Given that: $V^2_{out,rms,MAX,dBm}$ =4dBm, Ti=5ns, $\overline{V^2_{N,in}}$ =-174dBm/Hz, Cs=0.5p, P_{Gm} =1mW, and the following ADC has resolution of 10 bits. The SNDR is plotted in the fig shown in Fig.2-12 when the input signal power is sweeping from -80 dBm to 0 dBm and Gm is sweeping from 0.1mS to 10mS. The $IIP3_{Gm}$ is automatically calculated and swept based on the equation (2-20).

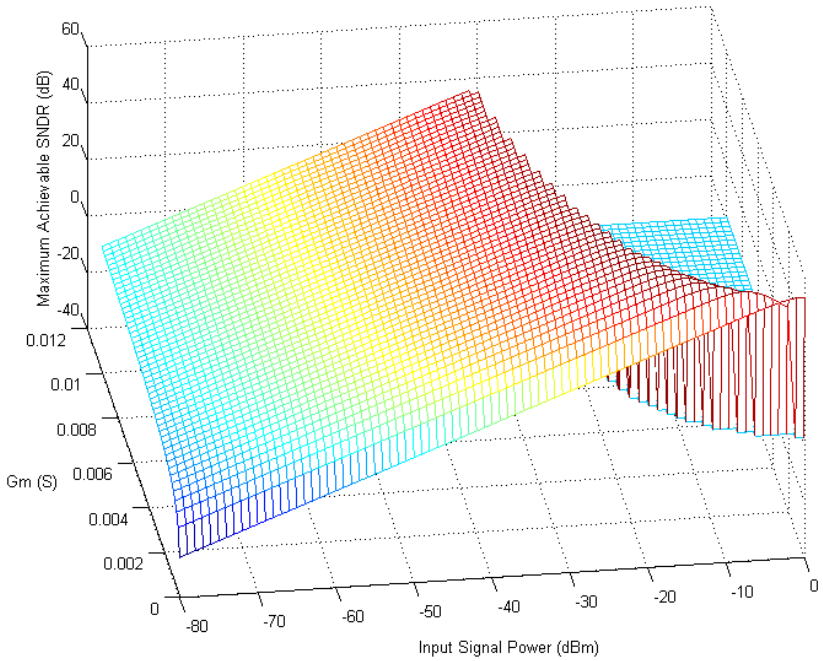


Fig.2-12 System output SNDR with Pin and Gm sweeping

The simplified plot of the maximum SNDR versus Gm is show below.

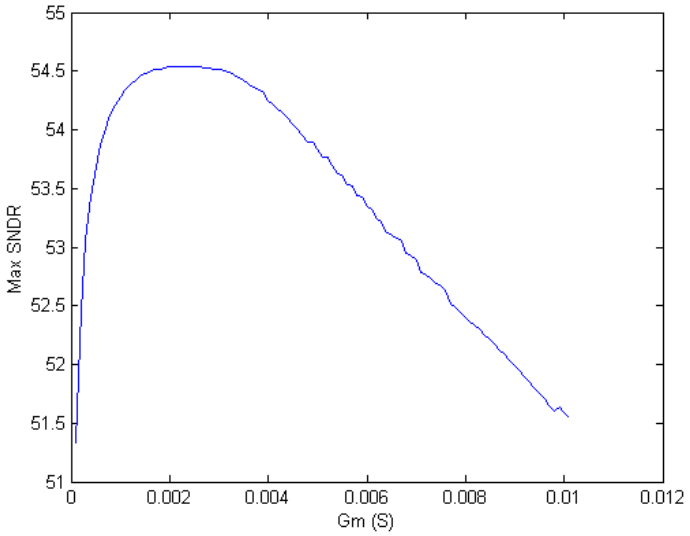


Fig.2-13 Maximum system output SNDR vs. Gm

As shown in Fig 2-13, to get high SNDR the front-end has to be a low-gain design. When the front-end is designed to be high-gain, only low input signal power is allowed, otherwise the output signal will exceed the maximum allowed output amplitude. Since the input noise floor -174 dBm/Hz is fixed, low input signal power makes the input SNR quite small, thus the output SNR is limited by the noise floor at the input. The gain can't be designed too small either because enough gain is required for the output signal to hit the full scale output amplitude otherwise the quantization noise of the ADC plays a role. The optimum Gain is roughly equivalent to $V_{out,\,fulscale} / V_{in,\,fulscale}$. Making full use of both the maximum input range and the maximum output range is necessary to maximize the SNDR. In order to accommodate the full scale input signal, IIP3 needs to be extremely good so that the SNDR is not limited by distortions.

Given that: $V^2_{out,rms,MAX,dBm}$ =4dBm, Ti=5ns, $\overline{V^2_{N,in}}$ =-174dBm/Hz, and the following ADC has resolution of 10 bits. The maximum SNDR versus power consumption and Cs is plotted in Fig.2-14. The optimum Gm and IIP3 are automatically calculated based on previous conclusions.

Increasing the power consumption and the size of the sampling capacitor can not further improve the SNDR. The maximum achievable SNDR in the FD receiver is less than 60 dB. The SNDR is actually limited by Ti, which determines the path sampling rate. When Ti is equivalent to 5ns, the path sampling rate is 200 MS/s. Thus, all the noise expanding over 200MHz of bandwidth is sampled and the total integrated noise power is significant. Theoretically, by increasing Ti, the sampling rate as well as the bandwidth of the noise can be reduced. However, finite output impedance of the

transconductance amplifier leads to current leaking and Ti needs to be short enough so that the sampled signal is not leaked out before being read out. Due to the difficulty of realizing low sampling rate, usually noise of large bandwidth is integrated and sampled, limiting the maximum achievable SNDR. The current leaking problem will be addressed in details in the next section.

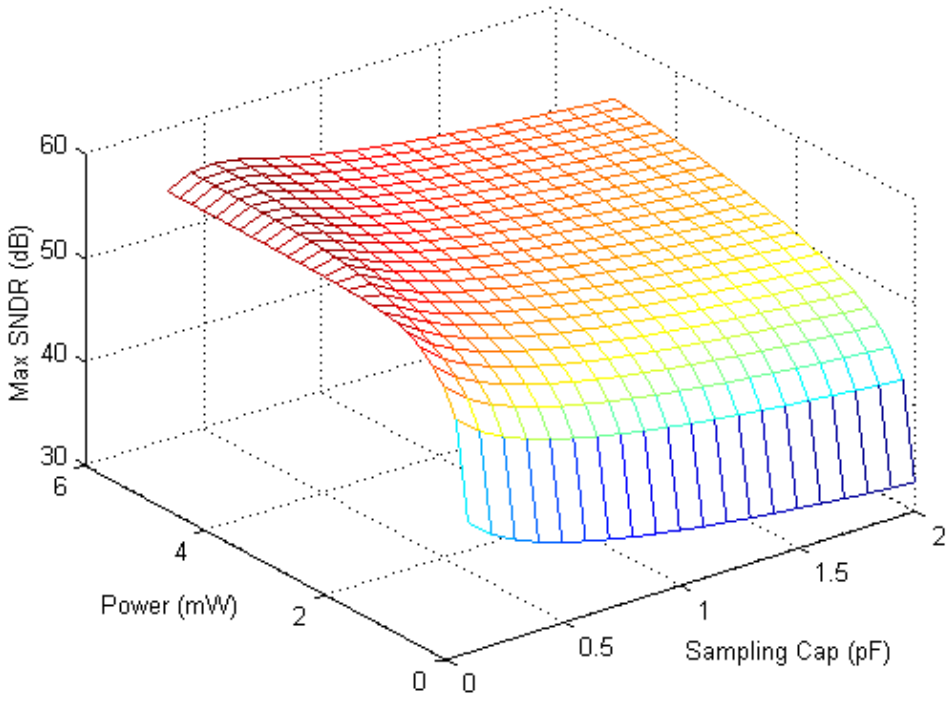


Fig.2-14 Maximum SNDR vs. power consumption & sampling capacitor

Faster sampling rate means shorter Ti, which requires more gain and more power to access the full scale output amplitude. There are trade-offs between the resolution and the sampling rate. Given that: $V^2_{out,rms,MAX,dBm}$ =4dBm, $\overline{V^2_{N,in}}$ =-174dBm/Hz, Cs=0.5p and

the following ADC has resolution of 10 bits. The Maximum achievable SNDR with sampling rate and power consumption sweeping is plotted in the Fig shown in Fig.2-15.

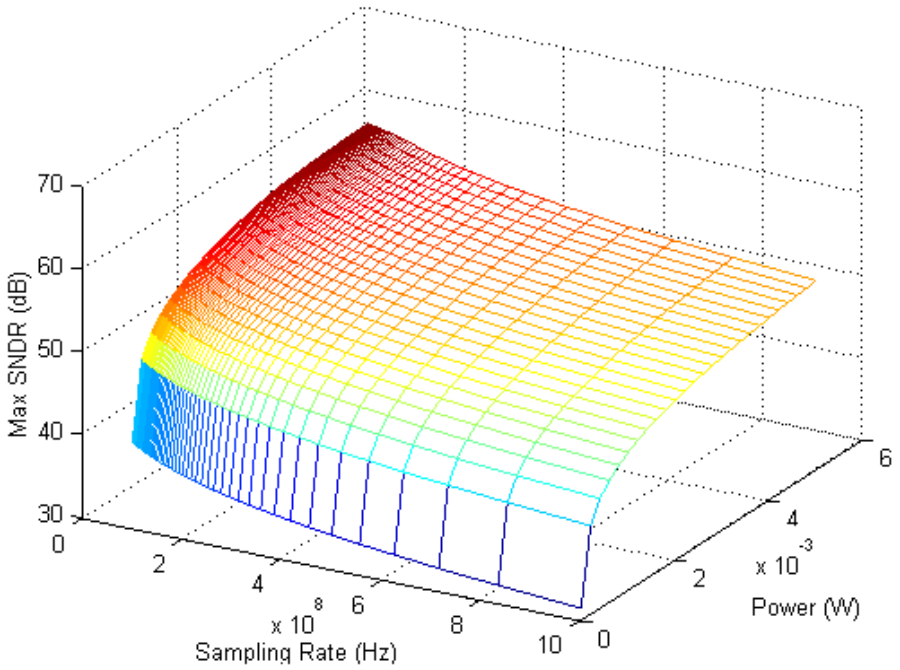


Fig.2-15 Maximum SNDR vs. power consumption & sampling rate

Conclusions:

- To maximize the SNDR, low gain and high linear front-end is required. Making use of full scale input and output range is necessary.
- The maximum SNDR is potentially limited by the characteristic of the FD front-end. Increasing the power and the chip area doesn't help to boost the SNDR. The best achievable resolution is between 9 bits ~ 10 bits, which corresponds to 56dB ~ 62 dB SNDR.

- Fixing the power consumption, there is trade-off between the resolution and the sampling rate. Increasing the sampling rate sacrifices the resolution.

2-4. Other circuits limitations

1) Finite output resistance of the Gm stage.

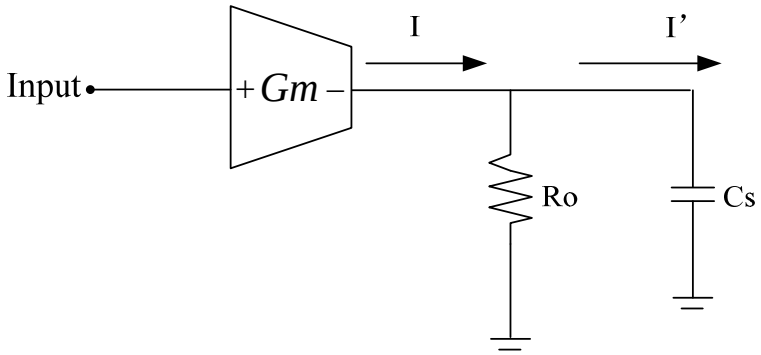


Fig.2-16 Effect of finite Ro

In Fig.2-16, the on-resistance of the passive mixer is ignored. Finite output resistance introduces a high pass type filter.

$$I' = I \cdot \frac{s \cdot C \cdot Ro}{s \cdot Cs \cdot Ro + 1}$$

Ro should be big enough so that the corner frequency 1/CsRo is below the lower edge of the signal bandwidth.

Furthermore, finite Ro leads to charge leakage. Those charge that already gets integrated in the sampling capacitor keeps leaking (Fig.2-17).

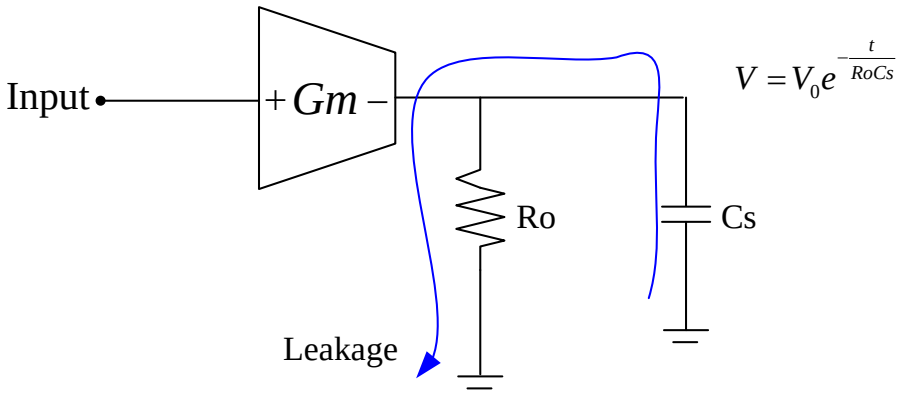


Fig.2-17 Effect of charge leaking due to finite Ro

It is better to set the time constant RoCs bigger than five times Ti in order to prevent the integrated signal from dropping, where Ti is the integration window.

It is difficult to design with either very fast sampling rate or very low sampling rate. It requires more power to get fast sampling rate while high Ro is required to get low sampling rate. Without any cascade structure, the maximum achievable Ro is around 1K ohm in the 45nm CMOS technology.

2) Limited bandwidth of the Gm stage.

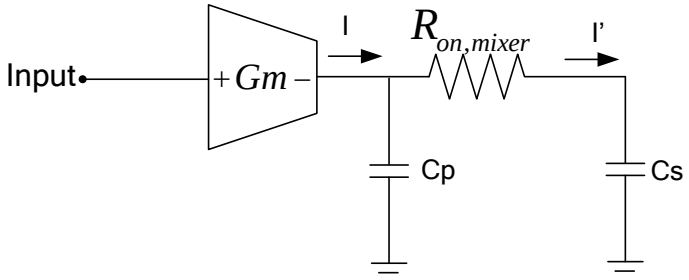


Fig.2-18 Effect of parasitic capacitor at the output of the Gm stage

Assuming Cs is much large than Cp, at high frequencies, the corner frequency $1/C_p \cdot R_{on,mixer}$ limits the bandwidth of the signal (Fig.2-18).

$$I' = I \cdot \frac{\frac{1}{C_p}}{R_{on,mixer} + \frac{1}{Cs} + \frac{1}{C_p}} \approx I \cdot \frac{1}{1 + s \cdot C_p \cdot R_{on,mixer}}$$

The Cp comes from the transistors in Gm stage and the blocking capacitor between the Gm stage and the mixer. Usually a blocking capacitor is employed between the Gm stage and the mixer to stop the DC current. The blocking capacitor has large size so there is pretty huge parasitic capacitance between it and the ground.

3) Limitations on equation (2-20)

Equation (2-20) assumes that we can infinitely boost the gm and the IIP3 by increasing the power consumption, which is not true in real circuit. The maximum chip power dissipation, the transistor break-down voltage and the finite supply voltage limit the maximum achievable Gm and IIP3.

Additionally, in equation (2-20), only non-linearity of gm is considered. In real circuit, signal swing at the output of the Gm stage also introduces distortions due to non-linear gds of the transistors.

Active integrators (Fig.2-19) can be employed to suppress the signal amplitude at the output of the Gm stage in order to mitigate the effect of the non-linear gds.

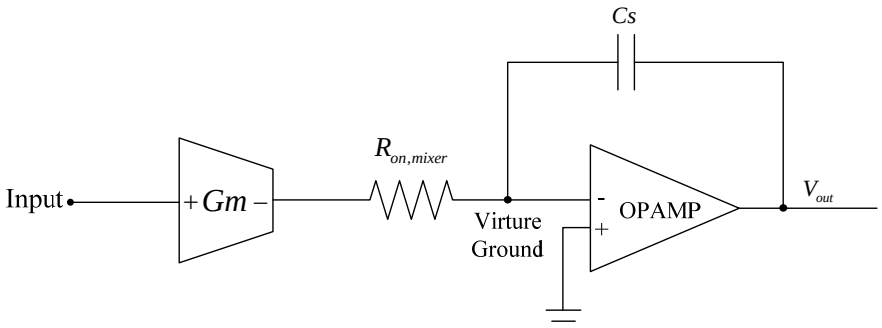


Fig.2-19 Basic active integrator

Looking into the input of the active integrator, the equivalent capacitance is ACs, where A is the gain of the OPAMP, so the time constant that determines the charge leakage is amplified to $A \cdot C_S \cdot R_{O,Gm}$, relaxing the requirement on Ro of the Gm stage. The OPAMP introduces additional noise and distortions so it needs to be carefully designed not to limit the output SNDR of the system.

There are also some other techniques to suppress the signal amplitude at the output of the Gm stage, which are not stated here.

4) Flicker noise

The effect of flicker noise is not considered in chapter II. As stated in the introduction, flicker noise is not ignorable anymore in the sub-micron CMOS technology. In many cases the flicker noise could be more dominant than the thermal noise. If the flicker noise is not properly mitigated, the achievable SNDR will be much worse than our prediction.

In chapter III, the proposed transconductance amplifier suppresses the flicker noise by using the source degeneration resistor. In chapter IV, the proposed cross-

coupling noise cancelling low noise transconductance amplifier removes both thermal noise and flicker noise from the first stage. The simulations show that the corner frequencies of the flicker noise in those two circuits are below the lower edge of the signal bandwidth, so the conclusions in chapter II still hold.

5) Additional thermal noise

In chapter II, the transconductance amplifier introduces thermal noise of 4kTgm, where gm is the signal transconductance gain. However, the biasing circuit will surely introduce additional noise. For example, in chapter III, resistors are employed to bias the drains of the main transistors and the overall output noise current is roughly as twice as 4kTgm. The maximum achievable SNDR is 3 dB less than predicted in chapter II.

6) Jitters

Jitters at all the gates of switches are limiting the SNDR. In our group, the effect of jitter in FD receiver is simulated with Matlab. It is not discussed in this thesis.

CHAPTER III

HIGH LINEAR TRANSCONDUCTANCE AMPLIFIER FOR HIGH RESOLUTION & HIGH SAMPLING RATE FD ADC SYSTEM

3-1. Introduction and motivation of the high resolution & high sampling rate ADC

The performance of the state-of-art Nyquist Rate ADCs (Fig.3-1) are limited by power consumption. With fixed power consumption, there are trade-offs between the sampling rate and the resolution. For a single ADC, it is quite difficult to get both high sampling rate and high resolution, otherwise the power consumption would be unacceptable. For example the Flash ADC has fast sampling rate but low resolution.

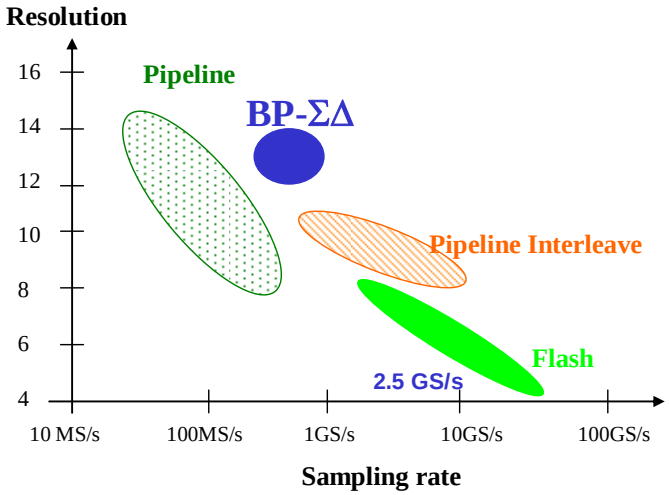


Fig.3-1 Performance of the state-of-art Nyquist rate ADCs

The FD receiver separates the input signal bandwidth so the hardware requirements for each path are significantly relaxed. Assuming N path is implemented,

the required sampling rate for each path ADC is only Nyquist Rate/ N. ADCs with high resolution and moderate sampling rate can be employed to sample the data at each single path. By combining all path ADCs together with the front-end, it is possible to build up an ADC system that provides very high effective sampling rate. With optimized power consumption, the whole system can achieve both high sampling rate and high resolution.

3-2. Specifications of the Gm stage

The proposed high resolution and high sampling rate ADC system is shooting for 2GS/s sampling rate and 9~10 bits resolution. The system is composed of 10 paths. The sampling rate of each path is 200MS/s. The sampling capacitor is 1pF and the maximum output voltage at the sampling capacitor is 0.8V. The maximum input signal amplitude is 0.4V. The input signal bandwidth is 1~2 GHz. The ADC in each path has resolution of 10 bits. The analog-front end is shooting for output SNDR higher than 55 dB to get the required system resolution.

Based on conclusions in chapter II, the Gm stage needs to have low gain and high linearity. Full scale input signal needs to be used in order to maximize the input SNR, thus the LNA is removed. The front-end is composed of Gm stages, passive current mixers and integrators. The single path circuit is the same with shown in Fig.2-7.

The Gm stage needs to have 0.6mS of transconductance for the full scale input signal to hit full scale output amplitude. IIP3 of the Gm stage needs to be as high as 25 dBm so that the SNDR is not limited by distortions.

The SNRs stage by stage are shown in the Fig.3-2. At the output of the front-end, maximum SNR of 59 dB is achievable when the input is a single tone signal. When the input is multi-tone signal, with the same full scale input range, the allowed input signal power is less than the single tone signal, leading to lower input SNR, thus the achievable SNR at the output for multi-tone signal is less than that for the single tone input. The worst SDR at the output is 61 dB.

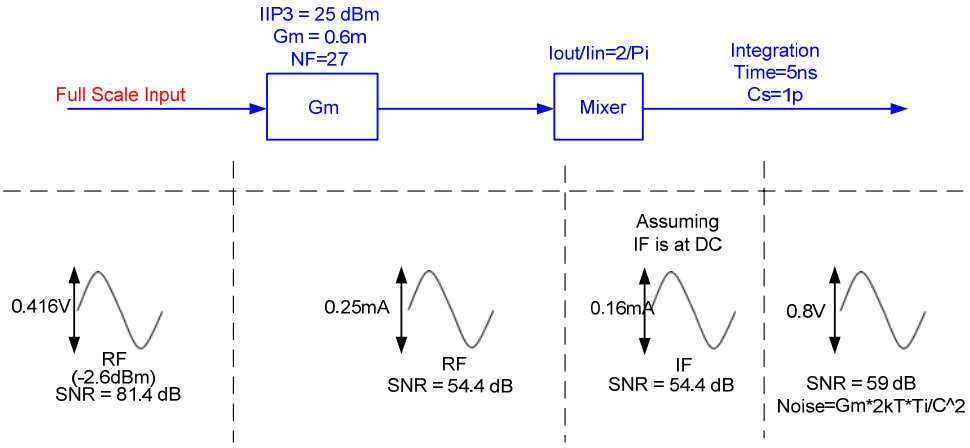


Fig.3-2 Stage by stage SNRs in the proposed FD front-end

3-3. Circuit design of the Gm stage

The Gm stage should be able to provide 0.6mS of transconductance and 25 dBm of IIP3. It is very challenging to get such a high IIP3 in a traditional transconductance amplifier. By simply increasing the Vdsat of the transistor, only 5~10 dBm of IIP3 is achievable. Special techniques are required to improve the linearity.

Many fancy techniques for boosting the IIP3 have been published. However, usually those special techniques are too sensitive to the environment and the process

variation. Reliability is the main consideration when this block serves a whole receiver. The most popular and most reliable technique to boost the IIP3 is the basic source degeneration (Fig.3-3).

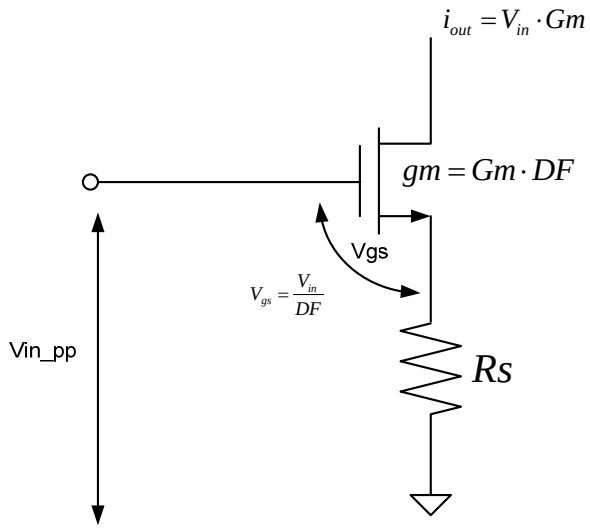


Fig.3-3 Basic source degeneration structure

The linearity of this circuit depends on the voltage amplitude that is applied to Vgs, which drives the non-linear gm. The source degeneration resistor degrades the amplitude of the input signal and only part of the input amplitude falls on Vgs.

$$V_{gs} \approx \frac{V_{in}}{DF}$$

Where the Degeneration Factor (DF) is equivalent to $1 + gm \cdot Rs$.

Assume that the transistor can achieve 5 dBm of IIP3, which means the interception happens when the voltage amplitude that is applied to Vgs is equivalent to 5dBm. To boost the system IIP3 to 25 dBm, the DF needs to be at least 10. When DF is equal to 10,

the amplitude of Vgs is 20 dB less than Vin, which means the interception happens when the input voltage power is 25 dBm. When gm is equivalent to 7 mS and Rs is 1.3 Kohm, IIP3 of 25 dBm might be achieved. This is just a simple analysis in terms of signal amplitude. Actually the theoretical IM3 is suppressed even more if it is accurately calculated in the negative feedback loop.

Another main concern in this circuit is the flicker noise. As presented in chapter I, the corner frequency of the flicker noise can be easily up to several GHz when small size of transistor is used. The flicker noise will fall in bandwidth of 1~2GHz and dominate the output SNR. In chapter II equation (2-8) assumes that the flicker noise is ignorable, but this assumption is totally wrong if the flicker noise is not properly suppressed. The degeneration resistor mitigates the flicker noise and defenses the assumption made by equation (2-8). When DF is big, which is true in the proposed circuit, the main part of the noise from the transistor is eliminated and the degeneration resistor becomes the main noise contributor.

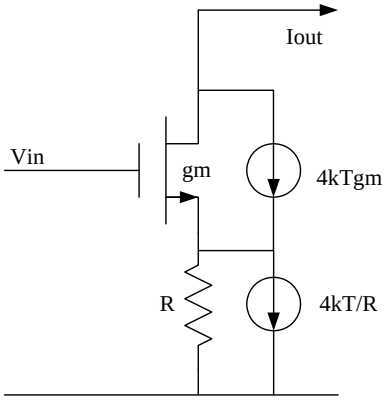


Fig.3-4 Noise current source in a basic source degeneration circuit

In Fig.3-4, the output noise current introduced by the transistor can be represented as,

$$\overline{I_{n,out(gm)}^2} = i_{mosfet}^2 \cdot \left(\frac{1}{gm} // R \cdot gm - 1 \right)^2 = \frac{i_{mosfet}^2}{(1+gm \cdot R)^2}$$

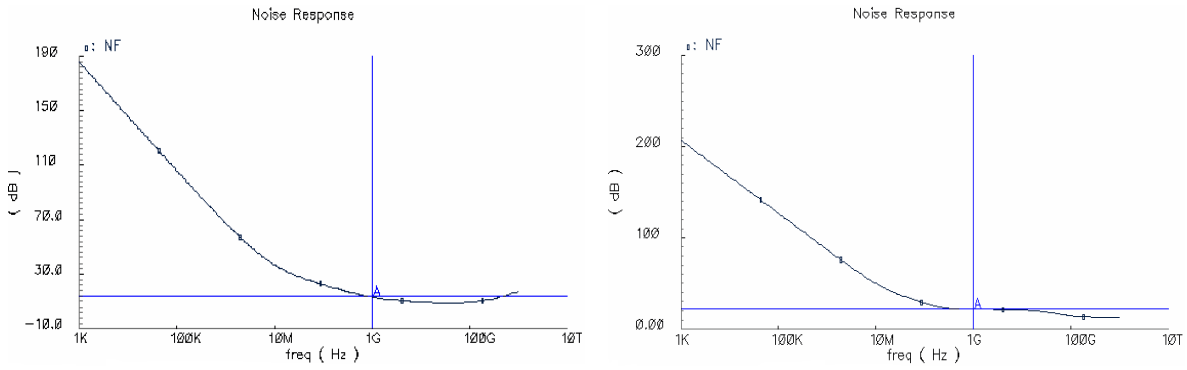
The output noise current generated by the degeneration resistor is written as,

$$\overline{I_{n,out(R)}^2} = \frac{4kT}{R} \cdot \left(\frac{1}{gm} // R \cdot gm \right)^2 = \frac{4kT}{R} \cdot \left(\frac{gm \cdot R}{1+gm \cdot R} \right)^2$$

The overall output noise current is shown below,

$$\overline{I_{n,out}^2} = \frac{i_{mosfet}^2}{(1+gm \cdot R)^2} + \frac{4kT}{R} \cdot \left(\frac{gm \cdot R}{1+gm \cdot R} \right)^2 \approx \frac{4kTgm}{1+gmR} = 4kTGm$$

When the degeneration factor $1+gm \cdot R$ is huge, the noise generated by the transistor is ignorable and the degeneration resistor, which doesn't produce any flicker noise, provides the output noise current that is approximately equal to 4kTGm. This result agrees on the assumption made by equation (2-8).



(a) (b)

Fig.3-5 (a) Simulated noise performance before source degeneration,

(b) Simulated noise performance after source degeneration

Before the source degeneration, the flicker noise falls in band and the noise spectrum is not flat. After the source degeneration the flicker noise in band is ignorable (Fig.3-5).

The load of this circuit needs to provide high impedance which is required by a transconductance amplifier. The most popular wide band high impedance load is a PMOS transistor. However, the flicker noise and thermal noise from the PMOS transistor would be overwhelming. A load resistor is used for biasing this circuit. The schematic is show in Fig.3-6.

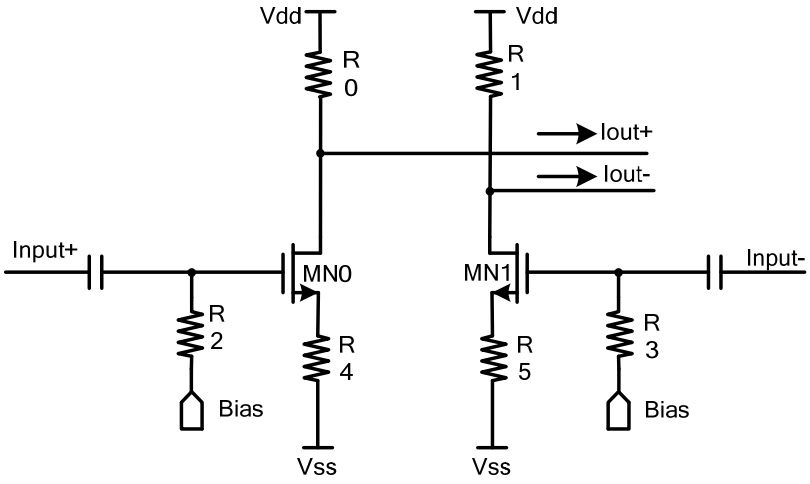


Fig.3-6 Schematic of the high linear Gm stage

R0 and R1 generates comparable amount of noise with R4 and R5. So the noise current coming from the Gm stage is a few dB worse than predicted by equation (2-8). R2 and R3 are 25 ohms for input impedance match. In a traditional high gain amplifier,

resistors at the input, such as R2 and R3 will introduce huge amount of noise. However, this transconductance amplifier is designed to be low-gain so the impact of the noise at the input is trivial. For this reason, the main consideration of this design is the output noise current, instead of the Noise Figure.

Due to the existence of source degeneration resistors, the DC biasing voltages at the source terminals of the NMOS transistors, as well as ones at gate terminals, are pretty high. The bulks of the NMOS transistors are always connected to VSS, so Vgb of those NMOS transistors might exceed the breakdown voltage. The solution is to use PMOS transistors, instead of NMOS transistors (Fig.3-7). The bulk and the source of the PMOS transistor can be connected together, so voltages across any two terminals of the transistor are not exceeding the breakdown voltage, even though very high supply voltage is used.

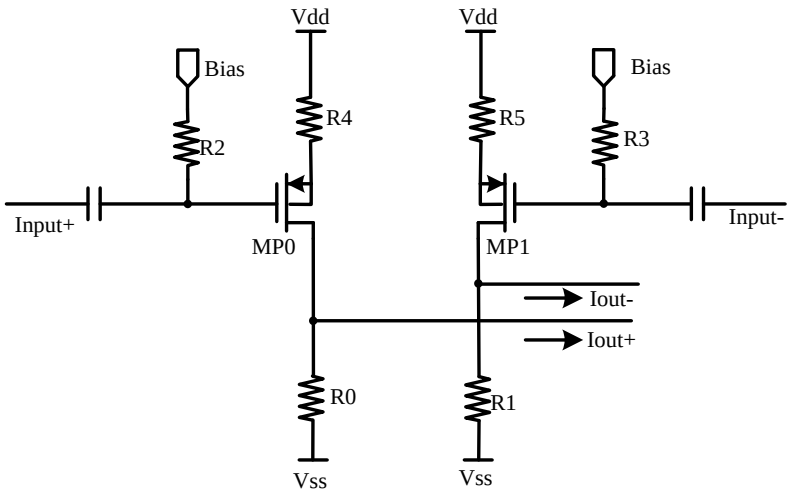


Fig.3-7 Schematic of the high linear Gm stage using PMOS transistors

The key parameters are shown in the table 3-1.

Table 3-1 Key parameters of the high linear transconductance amplifier

W/L of the PMOS	20.24um/0.08um
R0,R1	1.2Kohm
R4,R5	1.3Kohm
Vss	0V
Vdd	3.5V
Vbias	1.4V

The simulated IIP3 and NF are shown below;

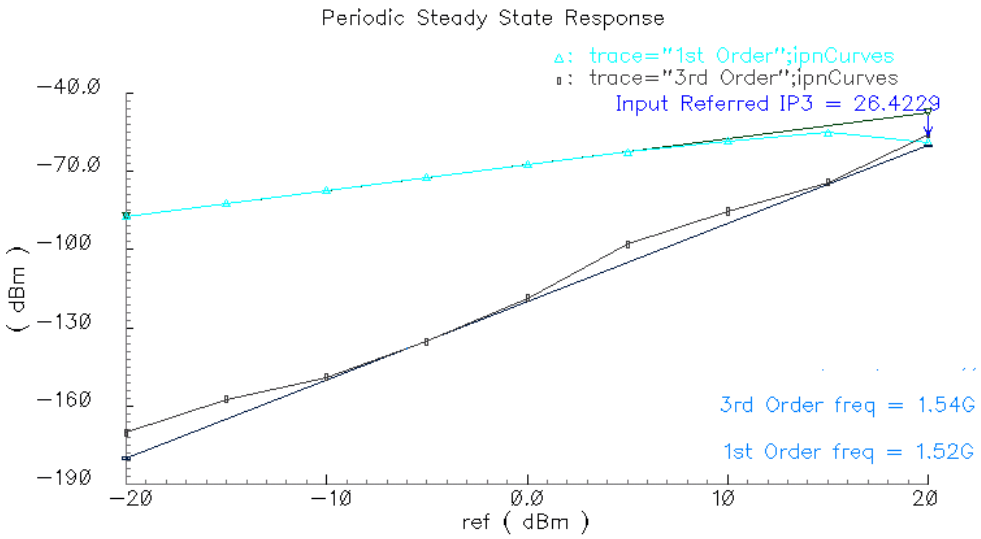


Fig.3-8 Simulated IIP3 of the proposed high linear transconductance amplifier

Linearity of the output current is measured (Fig.3-8). Power of the signal and distortions are plotted as $10 \cdot \log\left(20 \cdot I_{rms,output}^2\right)$. The testing tones are at 1.54 GHz and 1.52 GHz. The IIP3 is 26.4 dBm. Other simulations show that the output voltage amplitude needs to be less than 100 mV, otherwise the IIP3 will be degraded by the non-linear gds. Active integrators in Fig.2-19 is one of the solution to limite the output signal amplitude.

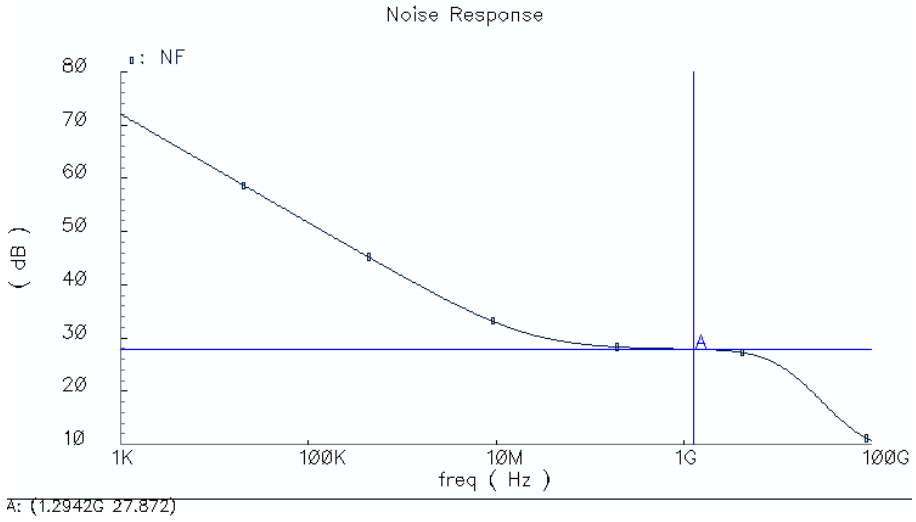


Fig.3-9 Simulated NF of the proposed high linear transconductance amplifier

The Noise Figure of this transconductance amplifier is about 28 dB (Fig.3-9), but the output noise current is still low enough for a 9.5 bits resolution. The overall performance is shown in table 3-2.

Table 3-2 Performance of the high linear transconductance amplifier

Power Consumption	3.5V*1.2mA
NF	27.9 dB
IIP3	26.4 dBm
Gm	0.7 mS

In the whole proposed FD front-end, ten proposed transconductance amplifiers are driving ten paths. The layout of the whole system is shown in Fig.3-10.

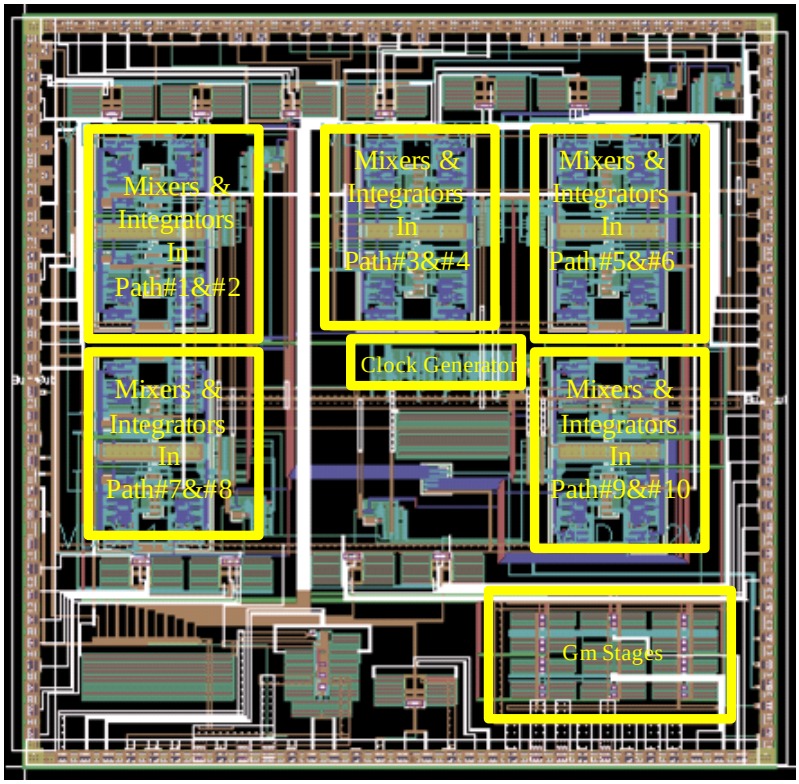


Fig.3-10 Layout of a 10 path FD receiver front-end

CHAPTER IV

A DIFFERENTIAL NOISE CANCELLING LOW NOISE TRANSCONDUCTANCE AMPLIFIER FOR DRIVING THE FD RF COMMUNICATION RECEIVER

4-1. Introduction

In chapter III a high linear transconductance amplifier is proposed to realize the high resolution and high sampling rate ADC system. To get enough output SNDR the transconductance amplifier is designed to be high linear and low-gain. The maximum achievable SNDR is 59 dB. However, in the RF communication receiver very high SNDR is not necessary. The desired signal can be processed and recovered with 20 dB SNDR or even less. Furthermore, to handle weak input signal from the antenna, the front-end should be able to provide enough gain. Above all, the transconductance amplifier which is suitable for the RF communications receiver is different from the high linear transconductance amplifier discussed in chapter III. Another transconductance amplifier, which is shooting for low NF, high Gain, moderate IIP3, is required.

As stated in chapter I, in the 45nm CMOS technology the corner frequency of the flicker noise could be up to several GHz. Due to the impact of flicker noise, low NF is more difficult to access. In this paper, a differential cross-coupling two stage low noise transconductance amplifier (LNTA) implementing noise-cancelling is proposed to mitigate both thermal and flicker noise at the first stage.

4-2. Circuit design

The proposed LNTA is composed of two stages. The first stage is a LNA which provides input matching in bandwidth of interest and the second stage translates the voltage signal into current.

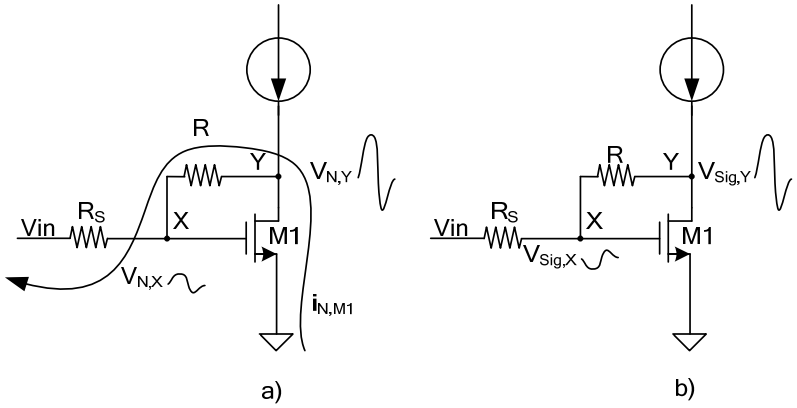


Fig. 4-1 (a) Noise and (b) signal voltage at nodes X and Y in the basic shunt resistance feedback matching low noise amplifier

The basic shunt resistance feedback input matching LNA in Fig.4-1 [3] has the potential to implement noise-cancelling so it is a good choice as a first stage. Very good input impedance matching is achieved given that impedance due to the LNA and R at node X is equal to R_S. The feedback resistor R is usually much larger than R_S so that noise current generated by R is negligible. The main noise contributor is M1. The drain noise current of M1 will flow through R and R_S generating noise voltages at both nodes X and Y. Noise voltages at nodes X and Y are in-phase but have different amplitudes which depend on the voltage divider composed of R and R_S. Approximately the noise voltage $V_{N,Y}$ will be A times $V_{N,X}$, where A is the gain of the LNA,

$$A \approx R / R_S \approx V_{N,Y} / V_{N,X} \qquad (4\text{-}1)$$

Therefore, if $V_{N,X}$ is amplified by A and subtracted from $V_{N,Y}$, it is possible to cancel them out as depicted in Fig.4-2.

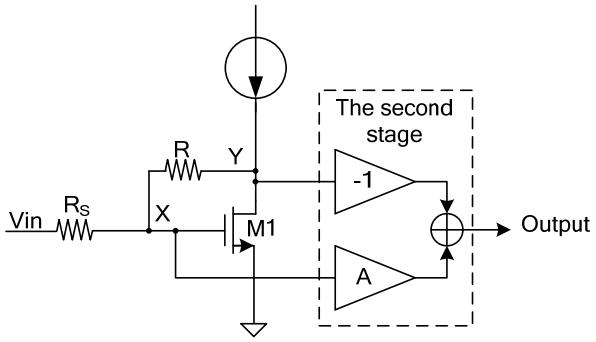


Fig. 4-2 The noise cancellation mechanism

A remarkable benefit of this approach is that main signal components at nodes X and Y have opposite signs and then will add coherently at the output.

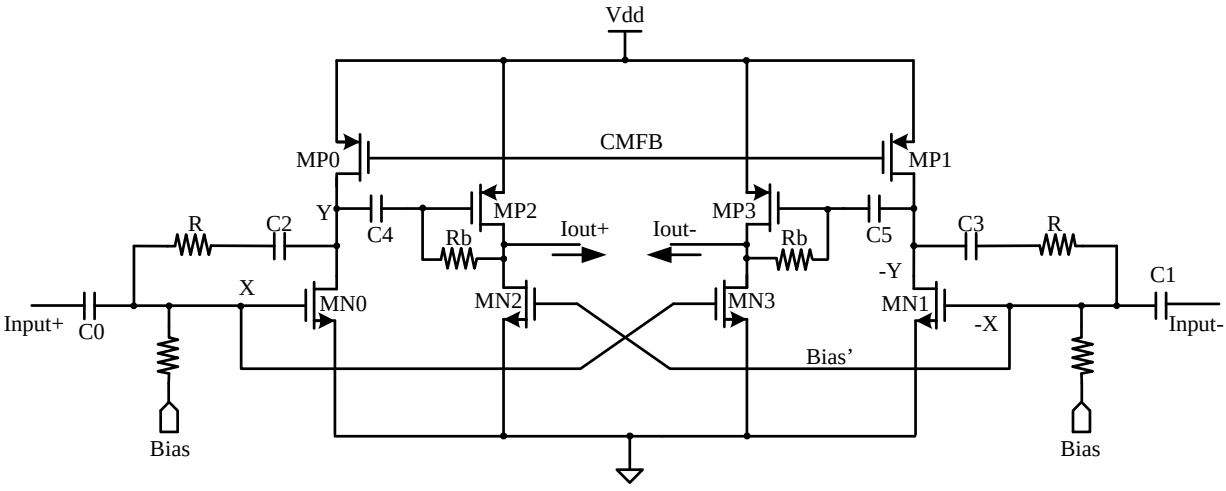


Fig. 4-3 Schematic of the proposed cross couple noise cancelling LNTA

A second stage is required to process the voltages at nodes X and Y. This additional stage should be able to provide an inverting gain and a non-inverting gain to implement the noise subtraction operation. The proposed cross-coupled noise cancelling LNTA is shown in Fig.4-3 [1]. $V_{N,Y}$ is driven into the gate of MP2 through C4 which leads to an inverting transconductance. MN3 implements a non-inverting transconductance for $V_{N,X}$. The noise cancellation is realized in a natural way when the differential output is further processed (Fig.4-4).

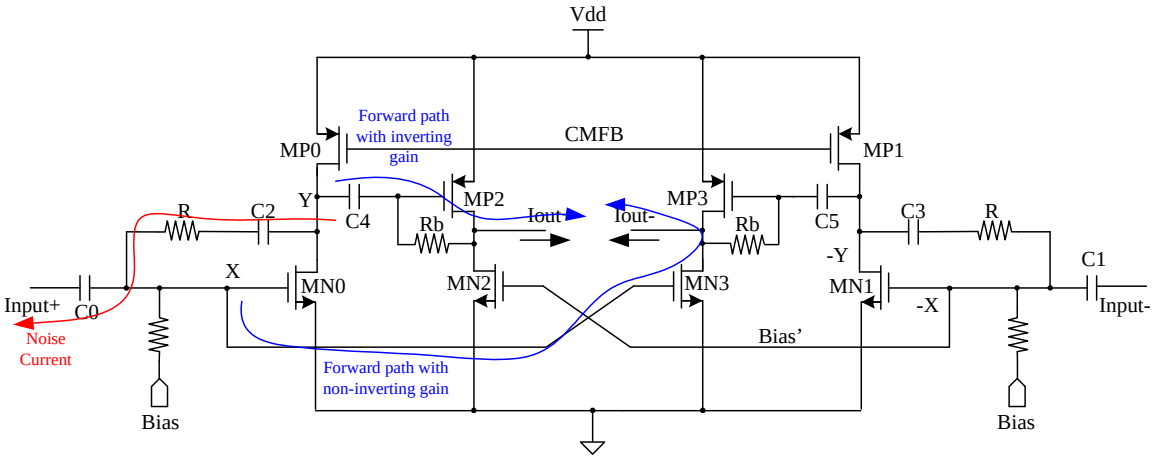


Fig. 4-4 Noise cancelling in the proposed LNTA

To perfectly cancel out the noise generated at the first stage it is required to satisfy the following condition,

$$gm_{MN2} / gm_{MP2} = A \qquad (4\text{-}2)$$

In fact this noise cancelling scheme is quite robust to mismatches in the second stage. Even though equation (4-2) is not perfectly satisfied significant part of the noise in

the first stage still gets cancelled. After noise cancelling the second stage will be the main noise contributor.

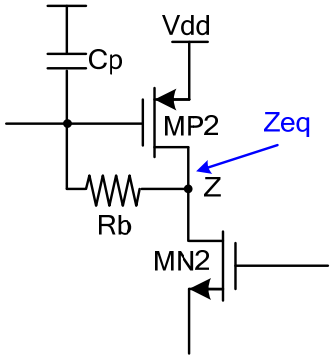


Fig. 4-5 Self-biasing circuit

For this prototype, MN0 and MN1 are biased off-chip. MP0 and MP1 are biased through the common mode feedback network. MP2 and MP3 are self-biased using the circuit shown in Fig.4-5. MP2 and MP3 are connected as active inductors [4]. A large resistor Rb is used for the biasing.

$$Z_{EQ} = \frac{1 + sR_bC_p}{gm + sC_p} // Ro_{MP2} // Ro_{MN2}$$

$$Z_{EQ}\,|_{s\to\infty} = R_b // Ro_{MP2} // Ro_{MN2}$$
$$Z_{EQ}\,|_{s\to 0} = 1/gm_{MP2}$$

At DC, the equivalent load resistance at node Z is 1/ gm_{MP2}, which is low impedance, so the DC voltage at Z can be stabilized. At high frequency we get high output impedance, which is $ro_P//ro_n$, given that Rb is huge.

The proposed noise cancelling LNTA presents better NF than single stage transconductance amplifier when they are shooting for the same transconductance gain

Gm. To show this advantage, consider the thermal noise first in a simple one stage amplifier.

$$V^2_{N,input\_reference} = 4kT / Gm \qquad (4\text{-}3)$$

In the two stage noise cancelling amplifier, both two stages contribute to the signal Gm but after noise cancellation, only the second stage contributes to the noise. In other words, the noisy gain is less than the signal gain.

$$V^2_{N,input\_reference} = 4kTgm_2 / Gm^2 \qquad (4\text{-}4)$$

where gm_2 is the transconductance of the second stage. Therefore, the input reference noise is decreased by gm_2/Gm. Evidently, first stage 1/f noise is also suppressed and only the second stage contributes to the noise.

The frequency dependent mismatches reduce the effectiveness of the noise cancellation technique, hence parasitic poles in the architecture must be placed at high frequencies so that the noise is well cancelled over the entire bandwidth.

4-3. Limitations of the proposed structure

The driving capability and the -3 dB bandwidth are limited by the parasitic poles at nodes X and Y.

$$\omega_{p,Y} = 1/\left(R_{eq} \cdot C_{g,MP2}\right)$$

$$R_{eq} = \left(R + R_S\right) // \frac{1}{gm_{MN0} \cdot \dfrac{R_S}{R_S + R}}$$

Assuming gm_{MN0} is equal to 1/Rs and Rs<<R,

$$R_{eq} \approx R/2 \Rightarrow \omega_{p,Y} = 1/\left(\frac{R}{2}\cdot C_{g,MP2}\right) \tag{4-5}$$

$$\omega_{p,X} = 1/\left[\frac{R_S}{2}\cdot\left(C_{g,MN2}+C_{g,MN0}\right)\right] \tag{4-6}$$

In equation (4-5), only parasitic capacitance introduced by MP2 is considered. This assumption is not accurate. Parasitic capacitance introduced by the first stage and the blocking capacitor could be dominant. However, this simplification makes it convenient for exploring design trade-offs and circuit limitations. Compare these two poles:

$$\frac{\omega_{p,X}}{\omega_{p,Y}} = \frac{\frac{R}{2}\cdot C_{g,MP2}}{\frac{R_S}{2}\cdot\left(C_{g,MN2}+C_{g,MN0}\right)} \approx A\cdot\frac{W_{MP2}}{W_{MN2}+W_{MN1}} \tag{4-7}$$

To cancel the noise of the first stage, (4-2) must be satisfied:

$$I_{D,MP2} = I_{D,MN2} \Rightarrow \sqrt{\frac{K_N\cdot W_{MN2}}{K_P\cdot W_{MP2}}} = A$$

$$\Rightarrow \frac{W_{MP2}}{W_{MN2}} = \frac{1}{A^2}\cdot\frac{K_N}{K_P} \tag{4-8}$$

Substitute (4-8) into (4-7),

$$\frac{\omega_{p,X}}{\omega_{p,Y}} = k\cdot\frac{K_N}{K_P}\cdot\frac{1}{A} \tag{4-9}$$

$$k = \frac{W_{MN2}}{W_{MN2}+W_{MN1}}$$

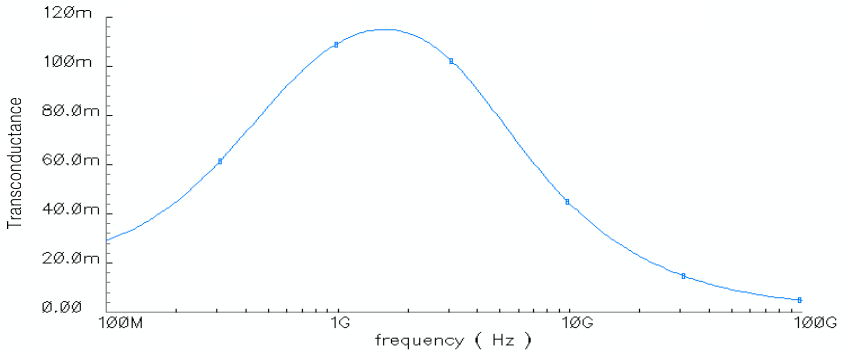
When $A < kK_N/K_P$, the pole at Y is dominant However, when $A > kK_N/K_P$ the bandwidth is limited by node X and the input matching is degraded. The gain of the first

stage needs to be carefully designed so that the bandwidth is not degraded by node X. In the proposed circuit, the bandwidth is still limited by node Y.

The linearity is limited by MP2 and MP3 because they have A times bigger input amplitude than other transistors. They should be well biased to get as good linearity as possible. Fortunately, MP2 and MN2 are biased by the same DC current but the size of MN2 is much larger than the size of MP2, so the overdrive voltage for MP2 is usually set very high then the linearity of MP2, as well as MP3, is not seriously bad.

4-4. Simulation results

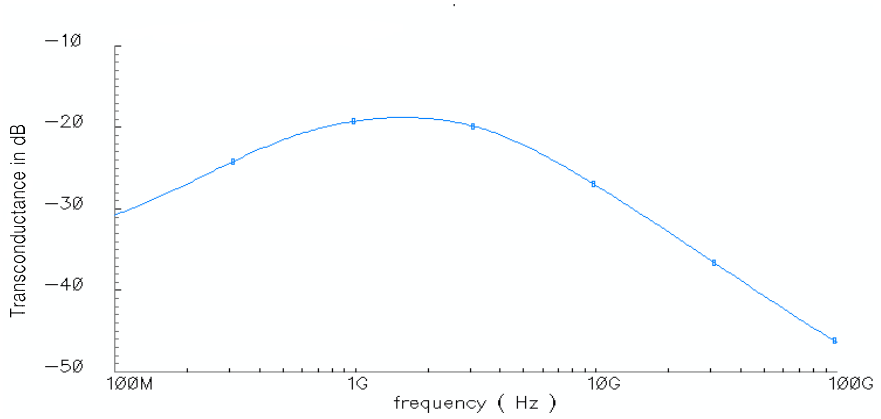
The proposed LNTA is simulated using Cadence Spectre. The TI 45 nm CMOS device models are used in the simulation. The gm_{M1} is set to match 50 ohms differentially. R is 200 ohms to get proper gain of the first stage. The simulated transconductance is shown in Fig.4-6.



(a)

Fig. 4-6 (a). The simulated transconductance of the LNTA

(b). The simulated transconductance of the LNTA in dB



(b)

Fig. 4-6 Continued

The peak small signal transconductance is 115 mS at 1.5GHz. The -3 dB bandwidth measured with respect to the peak value is 4.5 GHz.

The linearity of the output current is simulated. The IIP3 is shown in Fig.4-7.

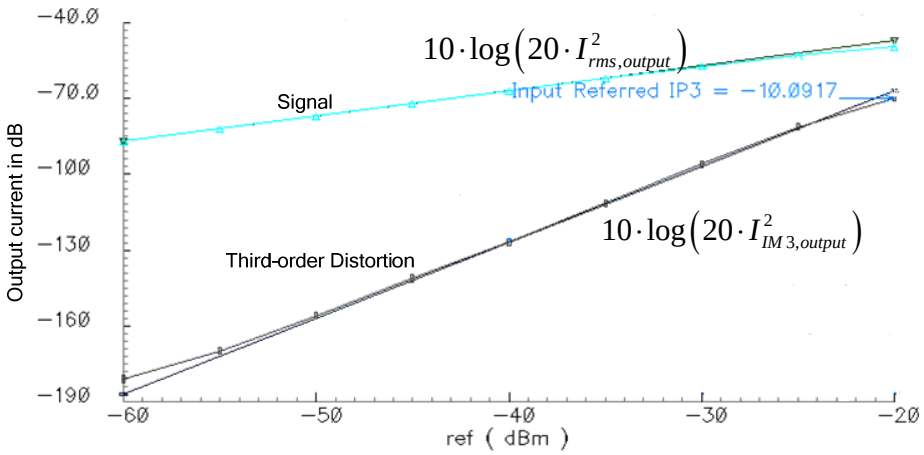


Fig. 4-7 The simulated IIP3 of the LNTA

The IIP3 is -10 dBm at 1.5 GHz. The frequency spacing of the two tone test is 20 MHz. The linearity of the LNTA is limited since the first stage amplifies the signal, hence the second stage, mainly MP2 and MP3 process large signal degrading system linearity.

The simulated Noise Figure is shown in Fig.4-8.

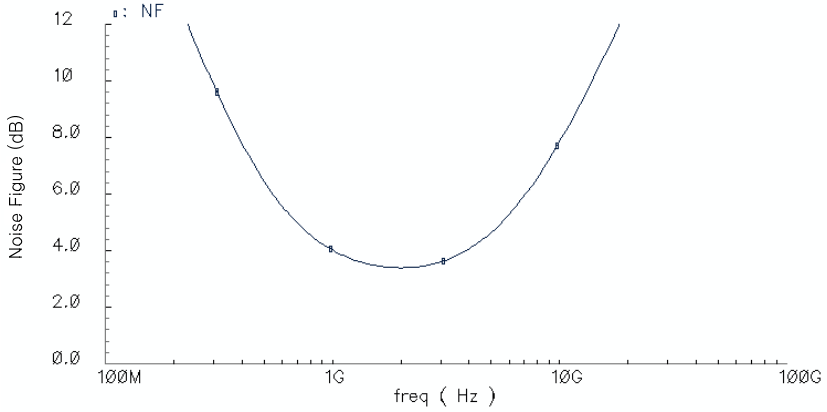


Fig. 4-8 The simulated NF of the LNTA

The minimum Noise Figure is 3.4 dB at 2 GHz. The average Noise Figure in the frequency range 1~ 4.5 GHz is 3.62 dB.

For comparison, a single stage transconductance amplifier shooting for the same Gm has been designed. Its Noise Figure is shown in Fig.4-9.

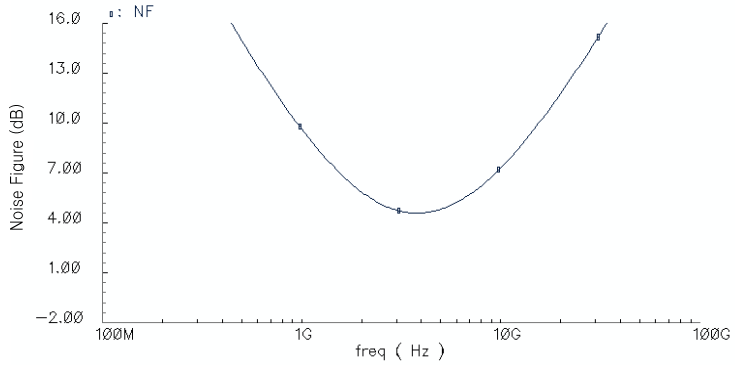


Fig.4-9 The simulated NF of the Gm stage of single stage

The minimum Noise Figure is 4.5 dB and the average Noise Figure between 1~4.5 GHz is 6.9 dB. The comparison is shown in the Fig.4-10.

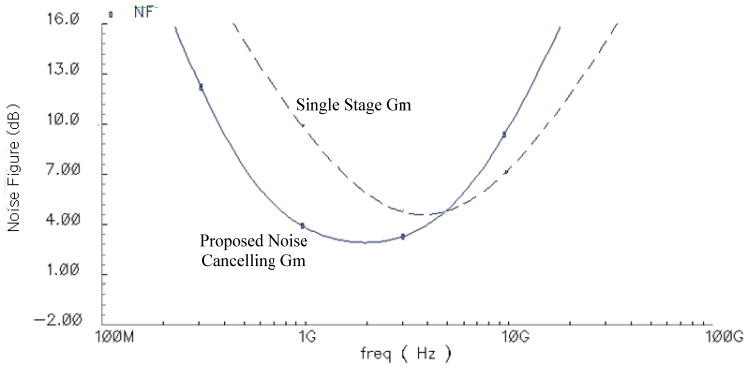


Fig.4-10 The improvement of the NF

Both thermal noise and flicker noise are suppressed.

The power consumption of the LNTA is 40 mW. Reducing Vdsat of the transistors can save power but the linearity will be sacrificed.

The overall performance is shown in table 4-1.

Table 4-1 Simulated performance of the noise cancelling LNTA

NF_{min} / $NF_{in\ band}$	3.393 dB / 3.62 dB
In band NF improvement	3.28 dB
IIP3	-10 dBm
Gm (Stage 1 + Stage 2)	115 mS
Gain (Stage 1)	14 dB
-3 dB Bandwidth	4.5 GHz
Maximum in band S11	-13 dB
Power consumption	40 mW

For testing purpose, the two stage LNTA is followed by a testing buffer. The load of the second stage is approximately equivalent to a 0.5 pF capacitor. The Layout of the LNTA is shown in Fig.4-11. The area is 300um*270um including all the blocking capacitors.

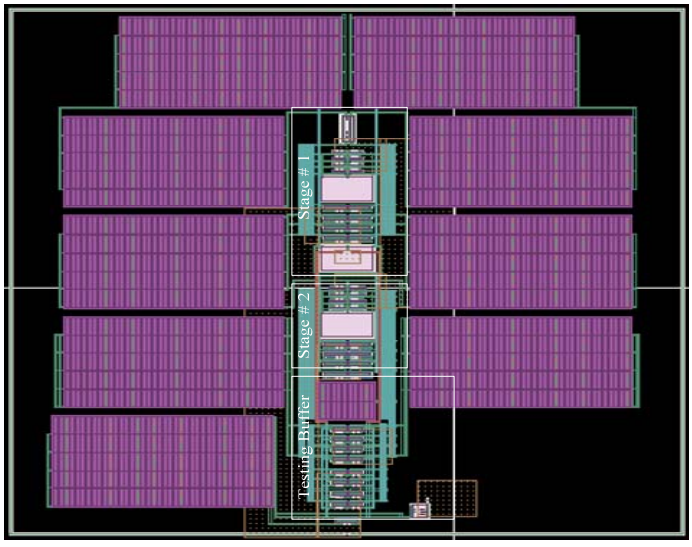


Fig. 4-11 The layout of the LNTA

4-5. Multi-path implementation

In the FD receiver, this noise cancelling LNTA is employed to drive the multi-channel front-end. The first stage is shared by the transconductance stages of all the channels. The simplified schematic of the multi-channel driver is shown in Fig.4-12. Blocking capacitors and biasing circuits are not shown for simplification.

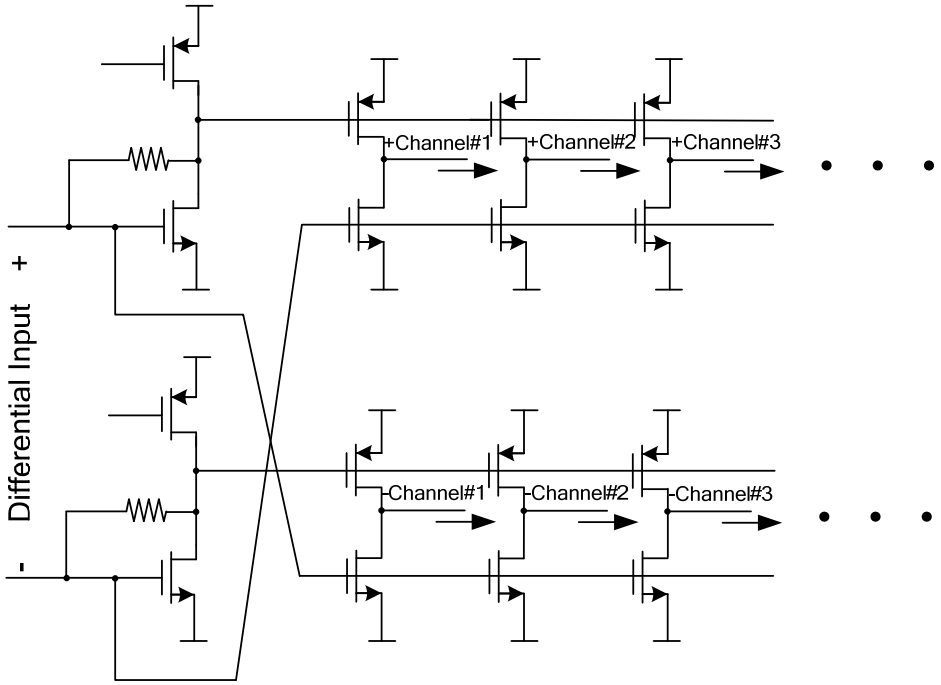


Fig. 4-12 The circuit structure of the noise cancelling multi-channel driver

When lots of paths are driven, parasitic capacitance introduced in the second stage is more significant than that in the first stage. The assumption made by equation (5) becomes more accurate. The k in equation (4-9) is approximately equal to one in these cases.

CHAPTER V

CONCLUSIONS

Development of the FD sampling receiver calls for high performance transconductance amplifiers. The FD sampling receiver is capable of realizing many different types of applications, including a high sampling rate & high resolution ADC system and a SDR platform. Shooting for these applications, different kinds of transconductance amplifiers are designed to fit various requirements.

The high linear and low gain transconductance amplifier is proposed to build up the high sampling rate & high resolution system. At the output of the front-end, the maximum achievable SNDR is around 59 dB. The whole system has 2GS/s of sampling rate and 9.5 bits of resolution. Another transconductance amplifier shooting for low NF and high gain is suitable for the SDR receiver. By cross-coupling the second stage, the noise cancelling scheme is exploited to suppress both thermal noise and flicker noise.

REFERENCES

[1] P. K. Prakasam, M. Kulkarni, X. Chen, Z. Yu, S. Hoyos, J., Silva-Martinez and E. Sanchez-Sinencio, "Applications of multi-path transform-domain charge-sampling wideband receivers," *IEEE Transactions on Circuits and Systems II*, vol. 55, pp.309-313 , April 2008.

[2] S. Karvonen, "Charge-domain sampling of high-frequency signals with embedded filtering," academic dissertation, Department of Electrical and Information Engineering, University of Oulu, Acta Universitatis Ouluensis, C 233, Oulu University Press, 2006.

[3] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol.39, no.2, pp.275-282, February 2004.

[4] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits:* New York: Cambridge University Press, 1998.

VITA

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