

GaAs Photovoltaics on Polycrystalline Ge Substrates

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Abstract

High efficiency III-V multijunction solar cells deposited on metal foil or even polymer substrates can provide tremendous advantages in mass and stowage, particularly for planetary missions. As a first step towards that goal, poly-crystalline p/i/n GaAs solar cells are under development on polycrystalline Ge substrates. Organo Metallic Vapor Phase Epitaxy (OMVPE) parameters for pre-growth bake, nucleation and deposition have been examined. Single junction p/i/n GaAs photovoltaic devices, incorporating InGaP front and back window layers, have been grown and processed. Device performance has shown a dependence upon the thickness of a GaAs buffer layer deposited between the Ge substrate and the active device structure. A thick (2 μ m) GaAs buffer provides for both increased average device performance as well as reduced sensitivity to variations in grain size and orientation. Illumination under IR light ($\lambda > 1$ micron), the cells showed a Voc, demonstrating the presence of an unintended photoactive junction at the GaAs/Ge interface. The presence of this junction limited the efficiency to ~13% (estimated with an anti-reflection coating) due to the current mismatch and lack of tunnel junction interconnect.

Introduction

High efficiency III-V photovoltaics, demonstrating AM0 efficiencies approaching 30%, are in wide spread use for space power applications. For near Earth applications, absolute conversion efficiency has become the dominate metric driving solar cell development. As missions move beyond low Earth orbit, specific mass and stowage volume (W/kg and W/m³) become ever more important, given the tremendous costs for moving mass out of Earths gravity well and safely landing it in another well (Mars for example). Figure 1 shows a comparison of cell mass specific powers for III-V multijunction solar cells deposited on various substrates.

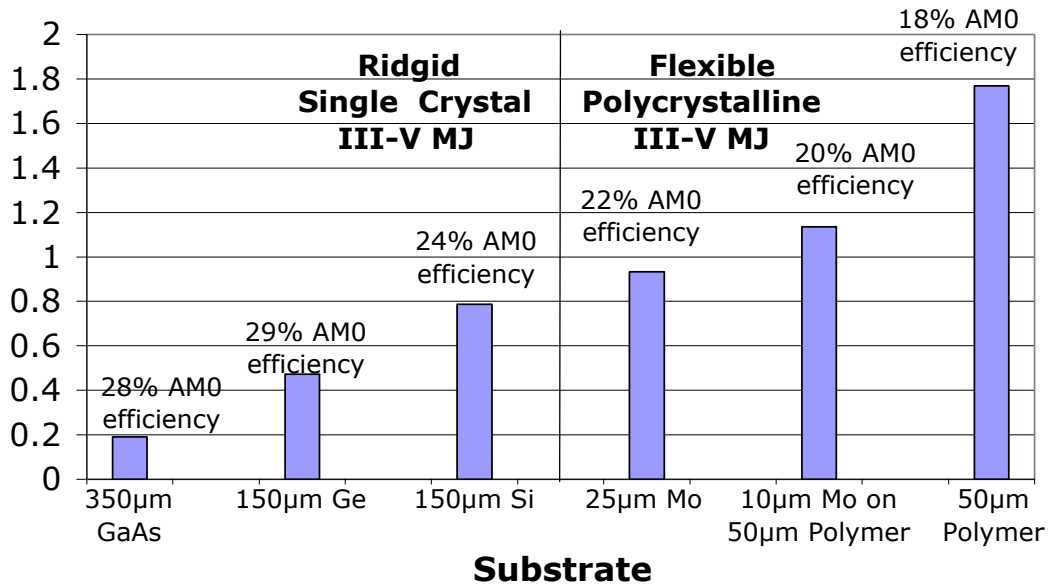


Figure 1 – Comparison of cell level mass specific power for III-V multijunction devices on various substrate materials.

Current SOA technology is shown by the 29% AMO efficiency on 150 micron Ge substrates (~ 450 W/kg). If silicon is substituted for Ge, the specific power nearly doubles despite a drop in overall efficiency. Transitioning to a metal foil provides the potential for an additional increase in specific power, plus the added feature of flexibility. The impact of the high density of molybdenum (Mo) can be moderated by the possible addition of a polymer (Kapton) backing layer following device fabrication. Finally, if a high temperature polymer substrate is developed, very high mass specific powers may be achievable.

The first steps down this path have been taken with the recent demonstration of III-V single and multi-junction devices on Si substrates [1,2]. These devices are now being tested in space aboard the MISSE5 spacecraft [3]. Moving to the next step, polycrystalline III-V devices on Mo foil, builds upon component technologies demonstrated previously. As shown in figure 2, the proposed process for integrating III-V devices on metal foil utilizes a thin film of Ge which is thermally recrystallized. This recrystallization process has been demonstrated by several researchers [4, 5], with grain sizes exceeding 1 mm². Traditionally, tungsten wetting and capping layers are used to promote large area grains and smooth surface morphologies. In addition, aluminum is occasionally incorporated to promote grain growth via the formation of a low temperature liquid eutectic.

Growth of polycrystalline III-V devices has also been explored in the past.[6] High efficiency (20% AM1.5) polycrystalline gallium arsenide (GaAs) solar cells have been reportedly produced on polycrystalline Ge wafers with average grain sizes < 1 mm². For high efficiency, the transition from single crystal to polycrystalline required the use of a

p/i/n device architecture. It was postulated that n-type dopants (Se) accumulated at the grain boundaries in the base region, forming n/n++ or high-low junctions. The presence of this junction, along with the resultant electric field, was conjectured to inhibit minority carriers from recombining at the grain boundaries. The need for an i region is also linked to dopant accumulation at the grain boundaries. For structures without the i region (p/n), a high dark current was noted. The dark current was attributed to tunneling currents near the depletion layer which appears to be aided by the dopant accumulation at the grain boundaries. The addition of a spacer layer (i) resulted in a 40x reduction in dark current, with a commensurate increase in Voc and FF.

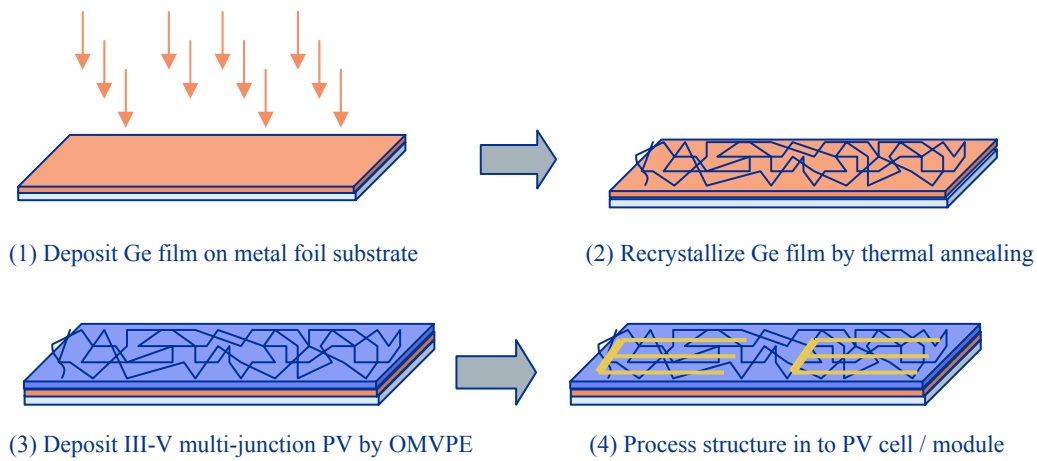


Figure 2 – Conceptual fabrication process for producing III-V materials on Mo foil. (1) Deposit Ge film (~2 microns) on Mo foil, (2) thermally recrystallize Ge film producing mm sized grains, (3) transfer structure to OMVPE system for III-V material deposition and (4) process structure into active devices.

Experiment

In order to develop the proposed technology, the activities were split into two parallel paths: (1) development of recrystallized Ge films on Mo foils (steps 1 and 2 from figure 2) and (2) OMVPE growth of polycrystalline III-V materials and devices (steps 3 and 4). At some point of development of the individual technologies, the paths would be merged into a single effort. The remainder of this paper will describe our efforts in the OMVPE growth of polycrystalline III-V materials and devices.

Polycrystalline Ge substrates with grain sizes on the order of mm^2 were obtained from Umicore. These wafers were polished and prepared using their standard process for generating epi-ready single crystal Ge wafers. The wafers were loaded into a horizontal low-pressure OMVPE system using conventional precursor materials (AsH_3 , PH_3 , TMGa , TMIIn , DEZn and Si_2H_6). A variety of nucleation and growth conditions were examined (table 1) by depositing a 250\AA nucleation layer of GaAs, followed by a $5,000\text{\AA}$ layer of GaAs. The resultant epitaxial structures were examined by Nomarski optical microscopy

and the impact of each deposition parameter judged by the range of morphologies noted on the various grain surfaces. Three primary morphology types were identified (figure 3), mound defected, cat-eye defected and smooth. A bias toward low temperature was included in the selection of the optimum nucleation and growth parameters in order to minimize the total thermal budget. This was done in hopes of one day transitioning this technology to a high temperature polymer, should one become available.

Parameter Varied	Values	Results
Bake temperature	600, 650, 700°C	Increasing temp (600 to 650°C) reduced mound defect density somewhat, but with no effect on cat-eye defects. At 700°C, observed an overall degradation in morphology. Optimum bake temp was 600°C.
Nucleation temperature	450, 500, 550°C	Increasing nucleation temp had no effect on mound density. At high temp, cat-eye defects emerged. Optimum nucleation temperature was 450°C
Growth temperature	620, 675, 725°C	Increasing temperature to 675°C eliminated cat-eye defects (mounds unaffected). At 725°C, overall morphology degraded. Optimum growth temperature 675°C.
V/III Ratio	100, 500	No effect observed over this range

Table 1 – Matrix of nucleation and growth variables tested in the deposition of GaAs on polycrystalline Ge substrates by OMVPE.

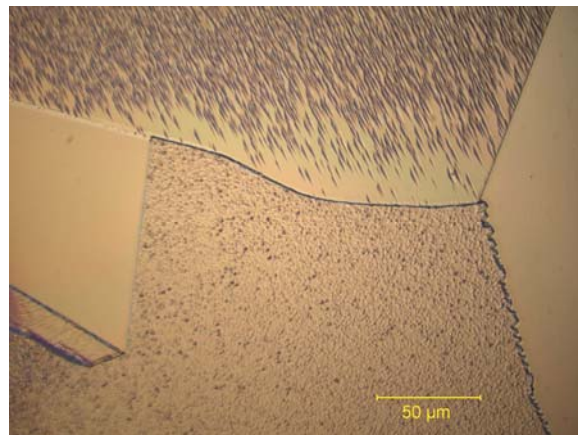


Figure 3 – Optical Nomarski image of 0.5µm thick polycrystalline GaAs deposited on Ge under non-ideal conditions. Visible are the three types of morphologies noted, cat-eye (top), mound (bottom) and smooth (sides).

Using the set of “optimized” nucleation and growth conditions, several single junction GaAs cell structures were fabricated (figure 4). The device design consists of a p/i/n GaAs cell structure with InGaP front and rear window layers. Two different GaAs buffer layer thicknesses were examined, 0.2 μm and 2 μm . The morphology of the cell structure is shown in figure 5. Twelve (12) 1 cm^2 , mesa isolated devices were fabricated on each 2” diameter wafer using conventional photolithography and metallization techniques. Mesa isolation was performed only on the GaAs cell layers (i.e. the mesa etch was not carried through to the Ge substrate).

500Å GaAs:Zn 5e18/cm ³
500Å InGaP:Zn 1e18/cm ³
0.3 μm GaAs:Zn 3e18/cm ³
1000Å GaAs:nid e14/cm ³
2.5 μm GaAs:Si 2e17/cm ³
500Å InGaP:Si 1e18/cm ³
2000Å / 2μm GaAs:Si 2e18/cm³
250Å GaAs:Si 2e18/cm ³
Poly Ge:Sb

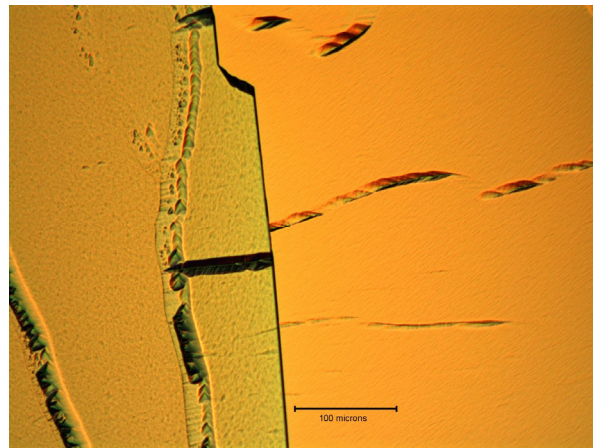


Figure 4 – p/i/n poly GaAs cell structure.

Figure 5 – Nomarski micrograph of cell epitaxy.

I-V characterization of the as-processed devices showed excessive Voc values (1050 mV), indicative of a voltage boost from a Ge sub-junction. Quantum efficiency (QE) measurements as well as Voc testing under 1 μm illumination confirmed the presence of an unintentional Ge junction. QE measurements showed the average QE to be ~10%, thus the Ge sub-junction is current limiting the tandem stack. The devices were re-mesa etched to ensure the Ge junction was mesa isolated as well. The resultant I-V curves (shown in figure 6) demonstrate the classic double knee for a current mismatched tandem device. In addition, the data shows a high series resistance which is not surprising given the lack of a tunnel junction interconnect between the subcells. Calculations suggest that for a current matched GaAs/Ge tandem, one would need an average Ge QE of ~ 0.8. This performance from a polycrystalline Ge film may be very difficult to achieve. Future efforts will look to deactivate the Ge sub-junction.

QE measurements of the devices (figure 7), suggests that a thick buffer layer slightly improves the blue end of the QE curve for devices with the worst performance and

morphology (yellow and purple lines). The primary difference between the single crystal control and the polycrystalline device are in the bandedge portion of the curve. At this time, it is unclear whether recombination within the base or at the base/window interface is controlling the reduced response. It should be noted that Si was used as the base dopant in this study as compared to Se for the previous work [6], in addition to the use of an InGaP rear window instead of a BSF (n+ GaAs). Additional work is required to optimize the dopant species and/or rear surface passivation approach to maximize the bandedge photoresponse.

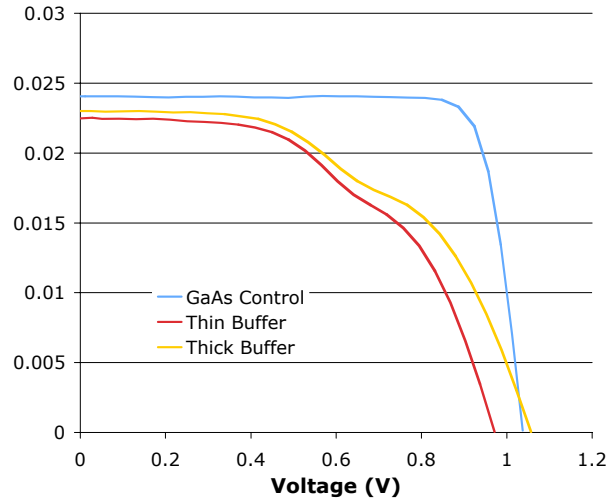


Figure 6 – AM0 I-V data for a single crystal GaAs p/i/n cell (control) and for polycrystalline GaAs p/i/n cells with thin (0.2µm) and thick (2µm) buffers.

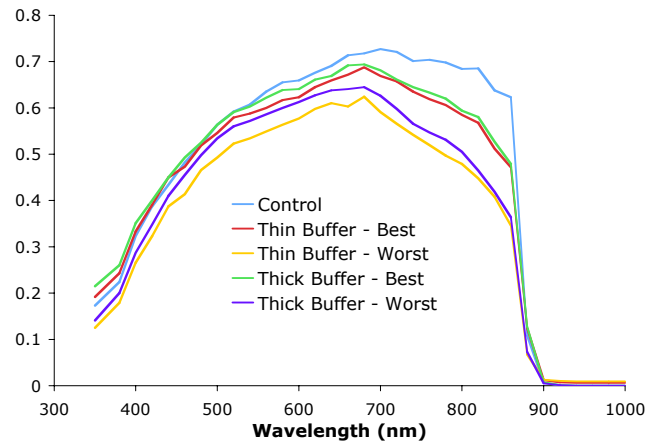


Figure 7 – External QE data (without ARC) for a single crystal GaAs p/i/n cell (control) and for polycrystalline GaAs p/i/n cells with thin (0.2µm) and thick (2µm) buffers. For the polycrystalline devices, the best and worst performing device from each wafer is plotted.

Finally, the Voc and Isc of each cell from both the thick and thin buffer samples were characterized and statistics (average and std. dev.) were tabulated (table 2). The data suggests that the use of a thick GaAs buffer provides two benefits, namely increasing the average device performance as well as reducing the variability in device performance. This latter benefit should be particularly beneficial when attempting to transition to large area devices in which there exists a large and uncontrolled range of crystalline orientations, grain sizes and interfaces.

	Thin Buffer		Thick Buffer	
	<i>Average</i>	<i>Std. Dev</i>	<i>Average</i>	<i>Std. Dev</i>
Jsc (mA)	21.95	1.12	23.09	0.366
Voc (mV)	790	229	889	42

Table 2 – Comparison of average performance and distribution for polycrystalline GaAs cells with thick and thin buffers.

Conclusions

The OMVPE growth of polycrystalline p/i/n GaAs solar cells on polycrystalline Ge substrates has been demonstrated. This development is a stepping stone in an effort to eventually develop high efficiency III-V multijunction solar cells on metal foil substrates. Organo Metallic Vapor Phase Epitaxy (OMVPE) parameters for pre-growth bake, nucleation and deposition have been examined. Single junction p/i/n GaAs photovoltaic devices, incorporating InGaP front and back window layers, have been grown and processed. Device performance has shown a dependence upon the thickness of a GaAs buffer layer deposited between the Ge substrate and the active device structure. A thick (2 μ m) GaAs buffer provides for both increased average device performance as well as reduced sensitivity to variations in grain size and orientation. Illumination under IR light ($\lambda > 1$ micron), the cells showed a Voc, demonstrating the presence of an unintended photoactive junction at the GaAs/Ge interface. The presence of this junction limited the efficiency to ~13% (estimated with an anti-reflection coating) due to the current mismatch and lack of tunnel junction interconnect.

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