SPACE SOLAR CELL RESEARCH AND DEVELOPMENT PROJECTS AT EMCORE PHOTOVOLTAICS

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INTRODUCTION

The $GaInP_2$/InGaAs/Ge triple junction device lattice matched to germanium has achieved the highest power conversion efficiency and the most commercial success for space applications [1]. What are the practical performance limits of this technology? In this paper we will describe what we consider to be the practical performance limits of the lattice matched $GaInP_2$/InGaAs/Ge triple junction cell. In addition, we discuss the options for next generation space cell performance.

CURRENT TECHNOLOGY

An "advanced triple junction" (ATJ) lattice matched $GaInP_2$/InGaAs/Ge device was commercially introduced in 2001 by Emcore Photovoltaics. Figure 1 is a histogram for over 100,000 large area (≥26 cm^2) devices that have been manufactured since that time. The efficiency was calculated using 135.3 mW/cm^2 solar constant. The histogram is skewed, in that the average efficiency for all of the cells, 27.6%, is not the same as the peak of the distribution, 28.0%. The upper limit of the ATJ technology, as seen in the histogram, is 29.0%. The skewed distribution is consistent with an upper limit in the efficiency.

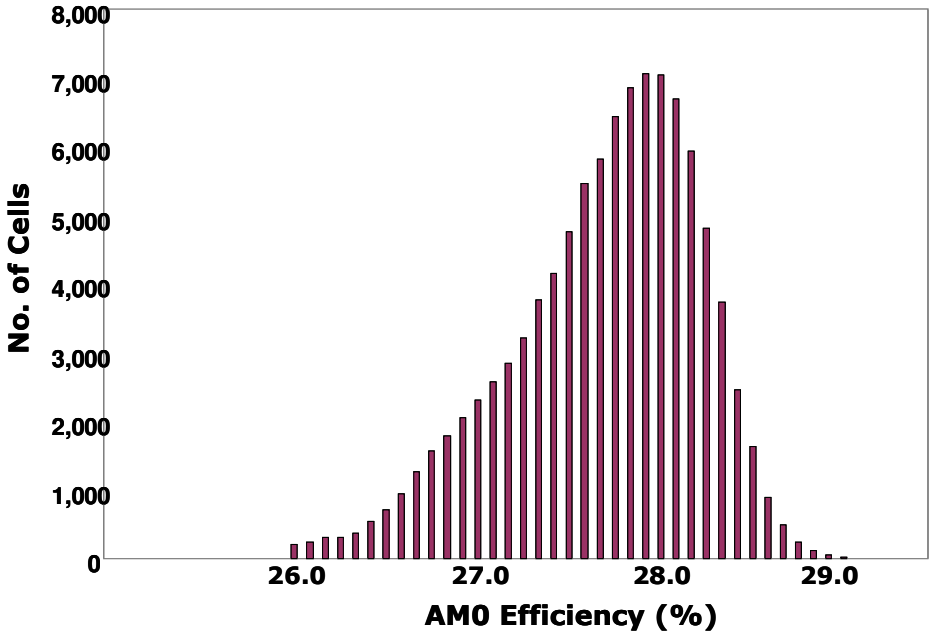

Figure 1. Histogram of cell efficiency for over 100,000 ATJ cells. The efficiency is calculated using 135.3 mW/cm^2.

In late 2002, an ATJ cell with a monolithic bypass diode (ATJM) was introduced as a commercial product. The monolithic bypass diode was included to reduce subsequent packaging complexity, i.e., the coverglass-interconnect (CIC) operation, and improve product reliability. Figure 2 is a cross section schematic of the ATJM cell. The schematic is not to scale, as the area of the diode is typically 4 mm^2, compared to approximately 2,750 mm^2 for the total cell area.

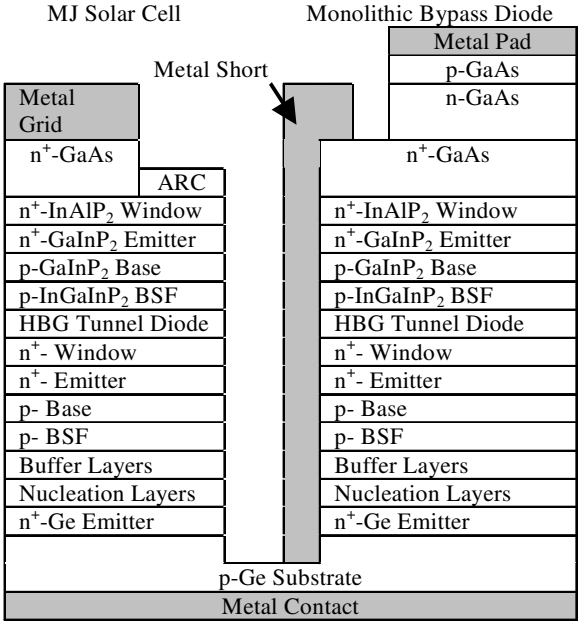

Figure 2. Cross section schematic of the advanced triple junction solar cell. The relative areas of the diode and the cell are not to scale.

MODELING OF THE $GaInP_2$/InGaAs/Ge CELL

Performance modeling of the lattice matched $GaInP_2$/InGaAs/Ge device was done to determine an upper theoretical limit to the AM0 efficiency. The desire was to determine a practical efficiency target for the BTJ device design. Care must be taken in any performance modeling, to understand the basic assumptions of the model. For the current modeling, the following assumptions were made:

1. The ideal diode equation, with a diode ideality factor of 1, to construct IV curves,
2. A value for J_o using the semi-empirical model of Green [2],
3. The fill factor was also calculated using Green's semi-empirical formula [2],
4. Absorption limited photocurrent collection (100% internal quantum efficiency {IQE}), and
5. The maximum power point of the series interconnected junctions was calculated numerically.

Different assumptions, particularly for the value of J_o, will lead to different efficiencies. In addition, other aspects of the model are idealized, such as 100% IQE across the spectrum, an anti-reflection coating (ARC) that has zero reflectance, and no grid/busbar losses.

Table 1 is a summary of the modeling data for the individual junctions in the complete device. Using the individual junction data, current limiting the complete device according to the top junction, and doing the numerical calculation to determine the maximum power point, the theoretical efficiency for a complete triple junction device is 35.6%, for the 135.3 mW/cm^2 solar constant.

Junction	$GaInP_2$	InGaAs	Ge
Bandgap, eV	1.92	1.40	0.664
Jsc, mA/cm_2	19.07	19.42	41.34
Voc, mV	1,510	990	274
ff, %	91.4	88.1	70.4
η, %, 135.3 mW/cm^2	19.26	12.52	5.89

Table 1. Summary of individual junctions theoretically modeled data for the BTJ cell. See text for a discussion of the complete triple junction cell efficiency.

While providing an upper limit for a particular device design, the achievable, practical efficiency is always lower than the theoretical. As a general "rule of thumb", 80% of a theoretical calculation is taken as an achievable, practical efficiency in our state of the art manufacturing production line. The 80% factor takes into account the non-idealities that the modeling does not account for, as mentioned previously. Using the 80% rule and the theoretical modeling done above, a practical efficiency for the BTJ cell was determined to be about 28.5%. This was the target average lot efficiency for the device, which included the monolithic bypass diode.

BTJ CELL DEVELOPMENT

In developing the BTJ cell, the ATJ and ATJM cells were taken as the starting points. The device design and OMVPE growth of each of the $GaInP_2$, InGaAs, and Ge junctions were considered, as were the processing steps for transforming the epitaxial growth into a finished device. There have been improvements in the voltage, current, and fill factor above that of the ATJ, but the largest area for improvement was in the voltage. This was largely due to improved growth conditions. The bulk of the improvements in the current and the fill factor were due to process improvements.

Figure 3 shows the IV curve for one of the better large area (27.5 cm^2) devices produced to date, and Table 2 has the cell performance data. The challenge is not so much to produce a world record efficient cell, but rather to be able to produce thousands of cells consistently. Figure 4 shows a performance histogram for one of the development cell builds. The average efficiency of this histogram is 29.2%, for the 135.3% mW/cm^2 solar constant. As can be seen in Figure 4, there is a lower performing tail going all of the way down to 27.5%. Effort spent in "tightening" the performance distribution is well worthwhile. While the minimum average performance results from the development lots have been greater than 29%, we believe that the 28.5% value is more realistic of what a minimum average lot efficiency would be as the BTJ product is transitioned into high volume manufacturing.

One additional modification to the BTJ cell is an increase in the monolithic bypass diode area to nearly 8 mm^2. The motivation for this was to include weld and interconnect redundancy to the diode. Two separate interconnects would be welded to the diode pad, a picture of which is shown in Figure 5. The redundancy is included for the diode interconnects and welds, as the monolithic diode design is sufficiently robust in and of itself.

Because the BTJ cell is not a radical departure from the ATJM cell, the space qualification of the device is expected to be straightforward and yield similar results to the ATJM cell. We have already completed preliminary radiation testing, and the degradation results for exposure of the cell to 1 MeV electrons are shown in Table 3. These results are consistent with the radiation results for the ATJM cell. A more complete space qualification is underway, both at the bare cell and CIC level.

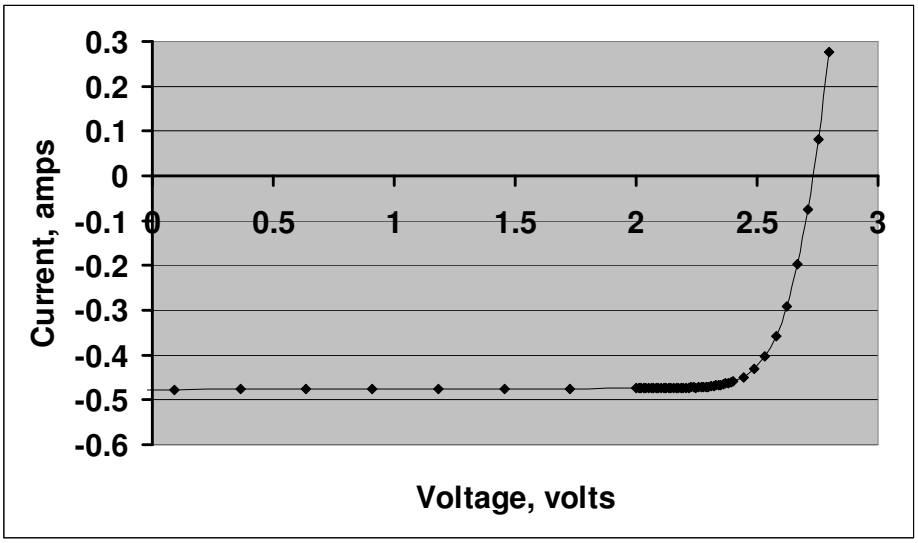

Figure 3. Current-voltage curve for one of the best BTJ cells produced to date. See Table 2 for performance details.

Isc, mA	477
Voc, mV	2732
Fill factor, %	84.5
η, %, 135.3 mW/cm^2	29.6
Cell area	27.5 cm^2

Table 2. Performance data for the cell shown in Figure 3.

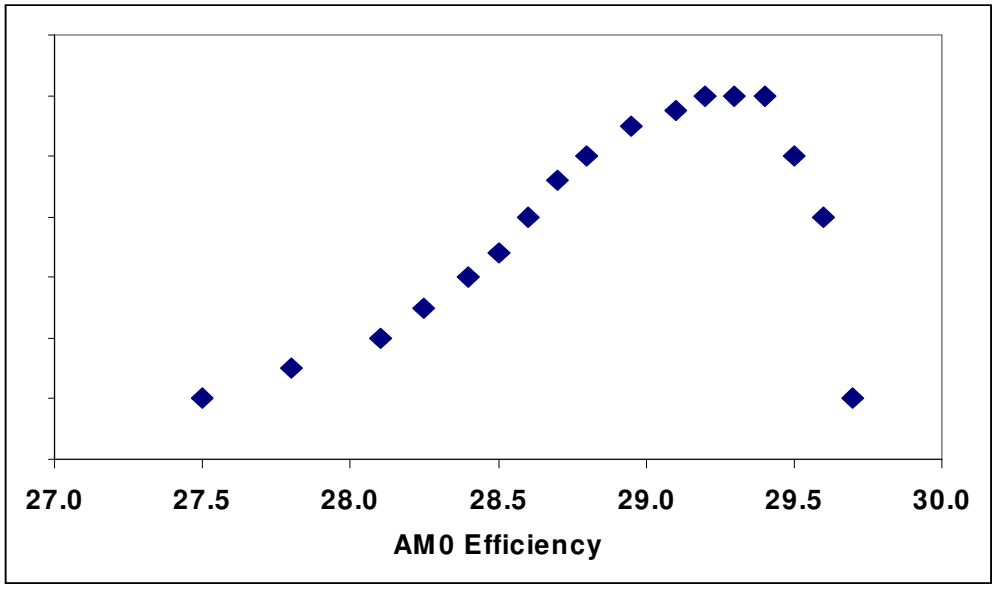

Figure 4. Efficiency histogram for one development build of the BTJ solar cell.

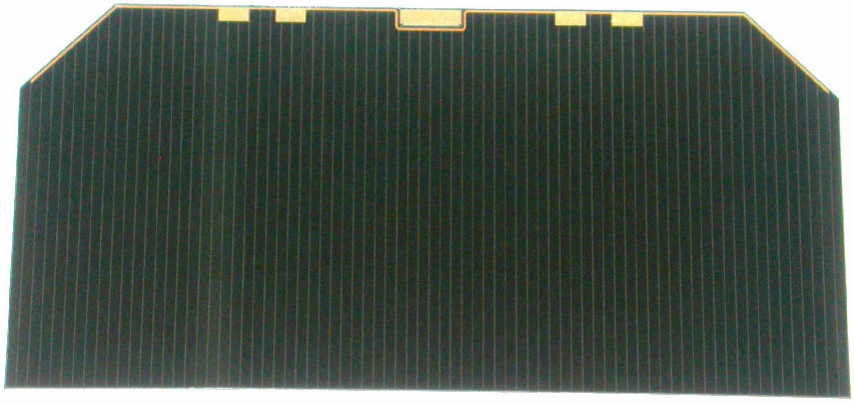

Figure 5. Picture of a BTJ cell, with the monolithic bypass diode pad at the center top of the cell. The total cell area is 27.5 cm^2. There are 4 cell bus pads, two on each side of the diode.

Fluence	Voc	Isc	VPmax	Eff
5e14	0.93	0.97	0.94	0.90
1e15	0.91	0.95	0.92	0.86

Table 3. Performance degradation factors for the BTJ solar cell after exposure to 1 MeV electrons, for two fluences.

FUTURE GENERATION DEVICES

A question naturally arises as to what the next generation device will be after the BTJ. At Emcore Photovoltaics, we have been working on three "traditional" approaches, as well as several other approaches. The three "traditional" approaches to device configurations with higher efficiencies are:

1. New materials development, in particular developing a 1-eV material lattice matched to GaAs to make a quad junction $GaInP_2$/InGaAs/1 eV junction/Ge device,
2. Mechanically stacking junctions together, and
3. Lattice mismatching to known materials, i.e., growing InGaAs with larger amounts of In, and incorporating these junctions into devices.

Each one of these approaches is not without challenges. At one time 1-eV InGaAsN lattice matched to GaAs was thought to be the ideal way to get to a quad junction cell. Reality turned out to be quite different, as InGaAsN has serious materials issues [3]. In particular, the short minority carrier diffusion length resulted in InGaAsN junctions with less than expected voltage and current. For a series interconnected device, the limited current generated by the InGaAsN severely limited the overall performance of a multijunction device using such a junction. In addition, the growth costs for InGaAsN layers are about an order of magnitude higher than those for growth of As and P based layers.

Mechanically stacking cells has the advantage that materials with different lattice constants can be combined into a single device. The removal of the lattice matching constraint opens up a number of possibilities for combining suitable band gaps. However, there are a number of challenges. First, a mechanical means of connecting the junctions has to be developed. The method of mechanical stacking has to be mechanically robust, optically transparent, and electrically conductive. Meeting all three of these criteria is quite a challenge. One method of interest is to use wafer bonding. Our own experience has indicated issues with the robustness of the adhesion, as well as having large area devices (>4 cm^2) without voids at the mechanical stack. There are additional issues with mechanically stacked devices for space applications. The first of these is cost. The substrate cost of the current $GaInP_2$/InGaAs/Ge is that largest part of the total cell cost. Using multiple substrates will substantially increase the cost of the completed device. There are also additional costs for the processing of each separate device that is incorporated into the final mechanical stack. In addition to cost, weight can be an issue. Multiple substrates add weight to the final device. Thinning substrates removes this consideration, but also adds process complexity and cost. Overall, we do not see mechanical stacking as a way to get to higher efficiency devices.

The lattice mismatch, or metamorphic approach, has achieved the most recent attention in the attempt to achieve higher efficiencies. The $GaInP_2$/InGaAs/Ge triple junction device is taken as the starting point. The standard approach is to grow from 3 to 5 lattice mismatched junctions on the germanium substrate. By lattice mismatching, the band gaps of the epitaxial layers are made more optimal for conversion of the AM0 spectrum.

We have modeled the 4, 5, and 6 junction lattice mismatched approach using germanium as the starting point. Our results indicate several difficulties with this approach. The modeling was done using the same assumptions mentioned above for the modeling of the lattice matched triple junction device. The germanium junction was the starting point, and epitaxial junctions were added. The band gaps of the epitaxial junctions were chosen such that they were current matched, and any band gap was allowable. Degradation of lattice mismatched layers due to threading dislocations (leading to reduced minority carrier lifetime and reduced voltage and current) was not taken into account. The first epitaxial junction was taken as a parametric, and the maximum achievable efficiency was calculated for that first epitaxial junction. Figure 6 is a summary of the results, showing how the efficiencies of 3, 4, 5, and 6 junction cells change with the first epitaxial band gap.

From Figure 6 it is seen that for a given first epitaxial band gap, increasing the number of junctions increases the device efficiency. However, the marginal increase in efficiency decreases as more band gaps are added. In addition, for a given efficiency, added junctions means that the first epitaxial junction does not have to be as low a band gap, i.e, less mismatching is required.

Figure 7 shows what the various band gaps should be for the 4, 5, and 6 junction cells, in order to achieve the efficiencies shown in Figure 6. For all of the devices, in order to achieve the optimum efficiency, a top junction of 2.0 eV or greater is required. However, this raises a serious issue. The proposed top junction for the lattice mismatched approach is InGaAlP.

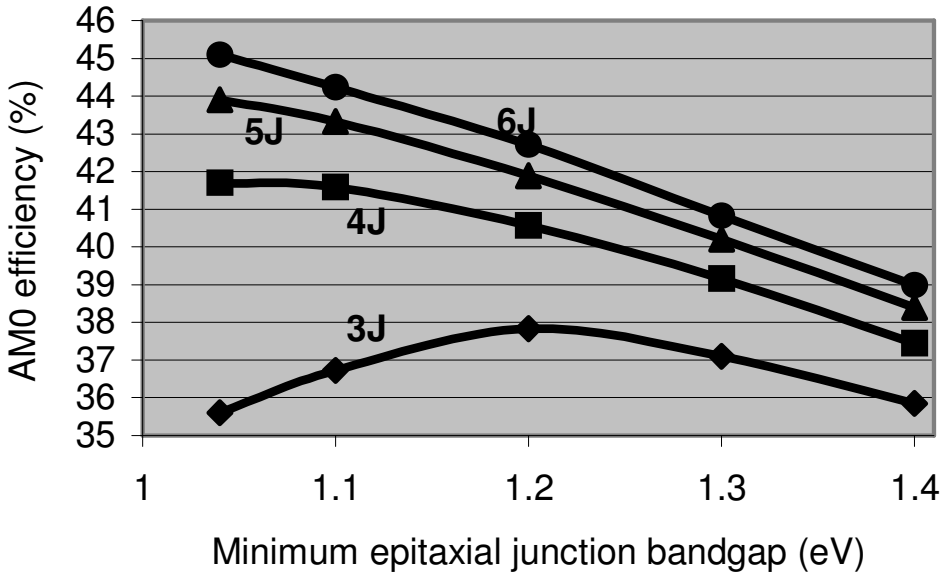

Figure 6. Maximum possible efficiency for 3, 4, 5, and 6 junction cells as a function of the first epitaxial junction.

Growth of high quality InGaAlP junctions is quite a challenge, because of the aluminum content. Aluminum and oxygen form a very strong bond, and so any residual oxygen in the growth reactor or the precursors tends to be incorporated into the junction. The oxygen in the material is a lifetime killer, i.e., it degrades the electrical performance of the junction. As such the InGaAlP junction limits the performance of the rest of the device. Our experience with the growth of InGaAlP junctions is that it is extremely difficult to consistently grow a high quality junction that will not limit the performance of the remainder of the device. The aluminum-oxygen issue is exactly why the AlGaAs/GaAs dual junction cell was never commercially successful [1]. Not only is the oxygen an issue for InGaAlP, but above about 2.2 eV InGaAlP becomes an indirect semiconductor material, meaning that very thick layers are required to absorb all of the incoming light. Incorporation of a junction with a bandgap greater than 2.0 eV is unlikely unless these issues are solved.

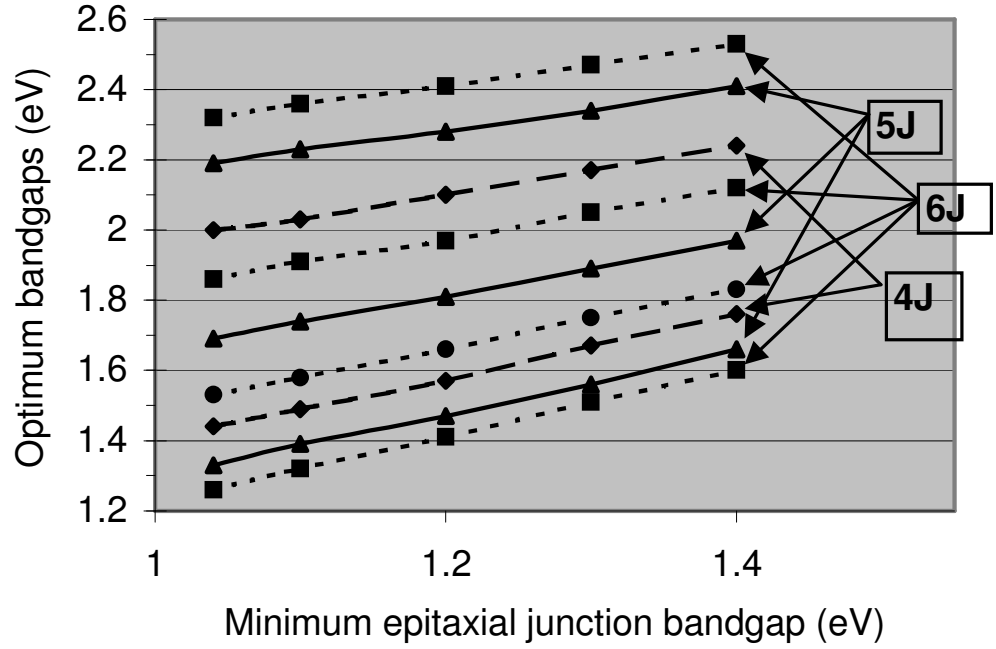

Figure 7. Optimum sets of band gaps for the 4, 5, and 6 junction devices. The important thing to note is that all of the devices require a top junction greater than 2.0 eV in order to maximize the conversion efficiency.

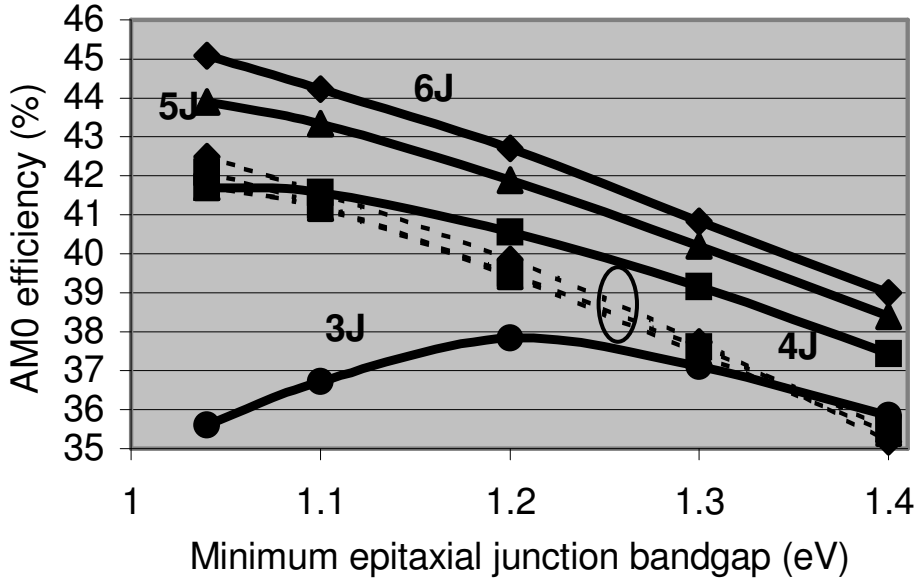

Figure 8. If the top junction band gap is constrained to 2.0 eV, the maximum efficiency of the 4, 5, and 6 junction cells collapse to the dashed lines (marked by the oval).

Figure 8 shows what happens to the 4, 5, and 6 junction modeled efficiencies when the top junction is constrained to 2.0 eV. The efficiencies "collapse" onto one another. There is minimal advantage in going to a 5 and 6 junction cell unless the top junction band gap can be made larger than 2.0 eV. Going to more junctions requires that the band gaps of the junctions be "spread out" in order to achieve the higher efficiencies. Unless this issue can be solved, the added complexity of the 5 and 6 junction approach outweigh any practical improvement in efficiency. To date there have not been any lattice mismatched devices made, starting with germanium and growing lattice mismatched epitaxial layers, that have achieved higher efficiencies than the lattice matched $GaInP_2$/InGaAs/Ge triple junction device.

The effects of the lattice mismatching on material quality have been previously mentioned. Lattice mismatching degrades material due to threading dislocations. For the previously described lattice mismatched approach this is a huge issue because all of the epitaxially grown junctions are lattice mismatched. Approximately 90% of the power from the device is coming from the lattice mismatched layers.

Recently, an inverted metamorphic (IMM) device has been proposed that keeps the majority of the epitaxial layers lattice mismatched, and only utilizes lattice mismatched layers for the smaller band gap junctions [4]. The $GaInP_2$ and InGaAs junctions are grown lattice matched but inverted on the germanium substrate. Any smaller band gaps are grown lattice mismatched on top of these layers, again in an inverted manner. The most likely material for the lattice mismatched junction is again InGaAs, but in this case there is only one lattice mismatched junction in the final device. Post growth the layers are attached to a "handle", the substrate removed, and the processing finished. For a triple junction device, with a 1.0 eV metamorphic third junction, approximately 80% of the device power is coming from the lattice matched junctions, and the remainder from the lattice mismatched junction. While using germanium for growth, there is no longer any constraints from the germanium junction. The IMM triple junction device looks promising for achieving a >30% device.

CONCLUSIONS

The following conclusions are drawn:

1. High volume manufacturing of a lattice matched $GaInP_2$/InGaAs/Ge cells with monolithic bypass diodes with average lot efficiencies of 28.5% are starting,
2. The lattice matched $GaInP_2$/InGaAs/Ge architecture is approaching the maximum practical efficiency in manufacturing,
3. Adding junctions to current 3J cells, without also extending the range of bandgaps available is not effective for

increasing conversion efficiency, and

4. Achievement of a high quality, high bandgap (>2.0 eV) top junction is critical to the success of 4, 5, and 6 junction cell architectures.
5. A new, inverted metamorphic (IMM) triple junction device is a possible way to achieving >30% AM0 efficiency.

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