Fabrication of a Silicon Backshort Assembly for Waveguide-Coupled Superconducting Detectors

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***Abstract*— The Cosmology Large Angular Scale Surveyor (CLASS) is a ground-based instrument that will measure the polarization of the cosmic microwave background to search for evidence for gravitational waves from a posited epoch of inflation early in the Universe's history. This measurement will require integration of superconducting transition-edge sensors with microwave waveguide inputs with excellent control of systematic errors, such as unwanted coupling to stray signals at frequencies outside of a precisely defined microwave band. To address these needs we present work on the fabrication of micromachined silicon, producing conductive quarter-wave backshort assemblies for the CLASS 40 GHz focal plane. Each 40 GHz backshort assembly consists of three degeneratively doped silicon wafers. Two spacer wafers are micromachined with through-wafer vias to provide a 2.04 mm long square waveguide delay section. The third wafer terminates the waveguide delay in a short. The three wafers are bonded at the wafer level by Au-Au thermal compression bonding then aligned and flip chip bonded to the CLASS detector at the chip level. The micromachining techniques used have been optimized to create high aspect ratio waveguides, silicon pillars, and relief trenches with the goal of providing improved out of band signal rejection. We will discuss the fabrication of integrated CLASS superconducting detector chips with the quarter-wave backshort assemblies.**

***Index Terms*—Superconducting microstrip, transition edge sensors, deep reactive ion etching, wafer bonding, surface roughness**

I. Introduction

Gravitational waves produced during inflation are expected to create a unique polarization pattern on the cosmic microwave background (CMB). This signature offers an important tool with which to investigate the high-energy physics of the inflationary epoch of the early Universe. The discovery of this signature will provide direct evidence for inflation and rule out most competing explanations for the initial conditions of the Universe. Characterization of this signal offers a way to explore the first 10^{-32} seconds of the Universe. The polarized signal from inflation is anticipated to be 10^{-9} of the 2.725 K isotropic CMB. Thus for an instrument to be successful in measuring this signal it must have (1) the requisite sensitivity, (2) excellent control over systematic errors in measurement, and (3) multiple spectral bands for foreground removal. We are developing the Cosmology Large Angular Scale Surveyor (CLASS) [1], a ground based telescope designed to search for the polarized divergence free "B-mode" signal in the CMB [2], [3], [4].

The CLASS instrument takes an innovative approach to address the scientific requirements for measuring the B-mode signal at large angular scales ($\theta > 2°$). CLASS will operate at three spectral bands (40, 90 and 150 GHz) to aid in foreground removal. Excellent beam control enabled by feedhorns [5] is combined with the sensitivity provided by transition-edge-sensing (TES) bolometers. The sensor integration is enabled via the use of a broadband planar orthomode transducer (OMT) that symmetrically couples the independent polarizations in the waveguides into separate microstrip lines [6]. The microstrip line for each polarization terminates in a resistor that is thermally coupled to a bolometer. This architecture enables incorporation of the band-defining filters into the microstrip circuitry, definition of the detector's radiation environment, and refined control over the sensor's thermal-mechanical interfaces.

A critical enabling component for the CLASS instrument is the detector technology. The CLASS 40 GHz detector architecture was described in [7]. A description of the electromagnetic design is reported in [5]. The full assembly is composed of three parts, a detector chip, a silicon quarter-wave backshort, and a silicon interface chip. The detector chip, which contains planar superconducting microwave antennas, magic-T power combiners [8], crossovers [9], band defining filters, and transition edge sensors for each polarization channel, is flip-chip bonded to the backshort. The stack is then bonded to the interface chip that mates the detector assembly to the focal plane. These fabrication processes are reviewed in section II. In section III we describe the fabrication of the quarter-wave backshort.

II. Fabrication

A. Detector chip fabrication

Fabrication of the CLASS 40 GHz detectors has been described previously in [10]. Here we give a brief overview of the process. A diagram of the CLASS 40 GHz detector fabrication process is shown in Fig. 1. Fabrication begins with a silicon-on-insulator (SOI) wafer with a high resistivity 5 µm thick device layer and a 375 µm thick handle wafer separated

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by a buried thermal oxide. The device layer will serve as the microstrip dielectric as well as the thermal link between the leg-isolated silicon membranes and the thermal bath. Using single crystal silicon for the device layer offers the advantage of a low dielectric loss material with repeatable material parameters improving performance of on-chip filters and superconducting microstrip components [6]. After patterning and etching a niobium ground plane, the wafer is bonded to a degeneratively doped silicon wafer with a polymer adhesive. Subsequently, the handle wafer is removed from the wafer stack by a plasma dry etching step. This naturally stops on the SOI buried oxide, which is removed in buffered HF solution. At this point the wafer resembles a modified SOI wafer where the buried silicon oxide is replaced by the polymer adhesive, the handle wafer is degeneratively doped silicon, and the silicon device layer has a buried Nb ground plane layer. Subsequent processing follows standard device fabrication since the polymer adhesive, when properly cured, is inert in standard micromachining chemicals. Additionally, after the silicon oxide is removed, the silicon layer is clean and provides an excellent surface for microfabrication of the transition edge sensors.

The next step is deposition and characterization of the transition edge sensors (TES). We use Mo/Au TES consisting of 500 Å of Mo and 2700 Å of gold. The deposition is done in a two stage process where the first stage is a sputter deposition of Mo with a flash of Au to create the seed layer and the second stage is an electron beam deposition of Au to the thickness required to suppress the Mo transition temperature (Tc) from a typical 900 mK to our target of 150 mK. The sputtered Au in the seed layer is thick enough to prevent subsequent Mo oxidation while not so thick as to suppress bilayer Tc significantly. The seed layers have typical Tc=700 mK. We batch process a number of product wafers along with witness wafers, so the seed films can be processed at the same time and have similar transmission coupling between the Mo and Au. Also, the Mo transition temperatures have minimal variation for films deposited in the same vacuum cycle. Au electron beam depositions are done subsequently after an *in-situ* surface cleaning on the witness wafers to bracket the bilayer transition as a function of Au thickness prior to committing the product wafers. Electron beam deposited Au gives a higher residual resistivity ratio than room temperature sputtered Au and this can help suppress bilayer Tc for minimal additional gold [5], [11]. We anneal the Mo/Au bilayers at 150° C after deposition to stabilize them against subsequent high temperature processes [12].

The TES Au is patterned and ion-mill etched, stopping on the Mo. Next the Nb microstrip is deposited by sputter deposition. The Nb is then reactive-ion etched in a fluorine-based plasma in two steps. In the first step that is used for the majority of the microstrip geometry, the plasma chemistry is adjusted for a vertical Nb sidewall slope profile. This is to minimize microwave loss due to sloped sidewalls. A second lithography step patterns the Nb in areas where it must make contact to other metal layers and this requires a sloped sidewall for good step coverage. The plasma chemistry is adjusted by adding oxygen to the chamber. The Nb etching is done in a bench top reactive ion etching tool using fluorine and oxygen plasma chemistry.

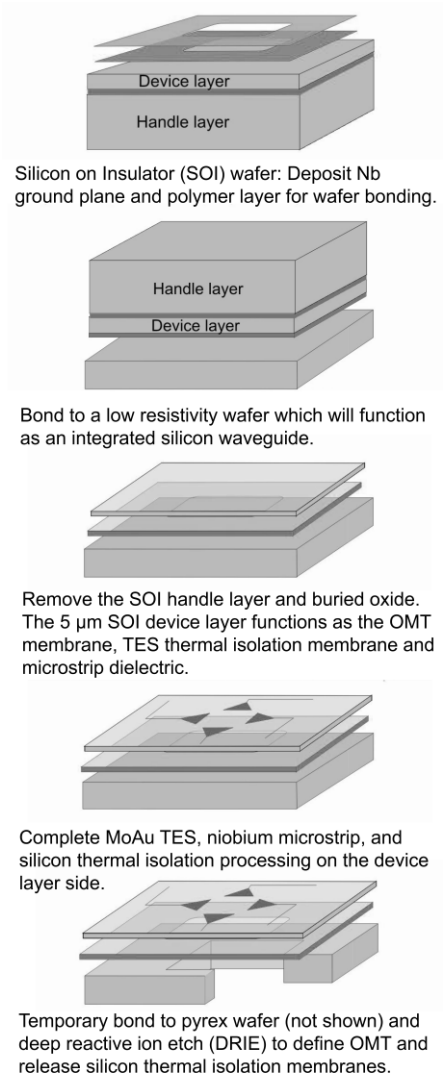

Fig. 1 Detector Fabrication Process.

Following the second Nb etch, the Au broadband load is deposited and patterned by liftoff. The broadband load is used as a termination for the magic-T and crossover components [8], [9]. It is also used as a contact between the Nb microstrip and the PdAu termination resistor. The PdAu deposition is targeted for 5 Ω/square resistance. The final metal deposition step is electron beam deposition of Pd, which provides the necessary heat capacity on the TES membrane for the required response time and to thermalize the TES membrane. Following the Pd deposition and liftoff, the silicon legs and the TES membrane are defined and etched. This is done in SF_6 plasma using a capacitively coupled reactive-ion etching (RIE).

A typical profile of the silicon legs and the TES membrane is shown in Figs. 2b and 2c. The silicon is etched isotropically with 2 µm of lateral etching for 5 µm of vertical etching. The

leg cut etch continues through the buried Nb ground plane and stops on the polymer bonding material. Next, the wafer is temporarily bonded to a handle wafer and the backside is patterned for deep reactive ion etching (DRIE). The DRIE defines the leg-isolated thermal membranes as well as the membranes for the antennas, crossovers and magic-Ts. Next the polymer layer is removed in an O_2 plasma stopping on the Nb ground plane and the silicon. The wafer is then soaked in solvent to remove the handle wafer and the individual chips are released. An image of the final detector chip is shown in Fig. 2a.

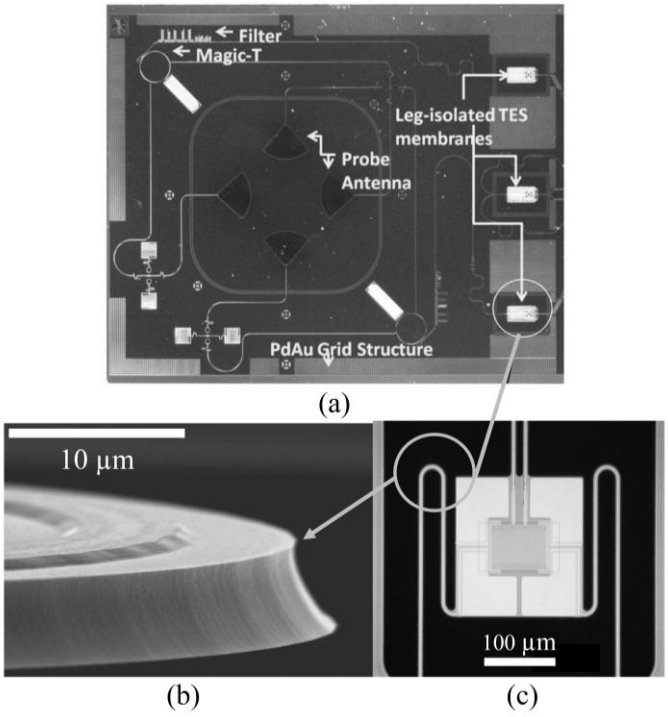

Fig. 2 (a) Image of CLASS 40 GHz detector chip. (b) Sloped sidewall of silicon leg with Nb microstrip. (c) Silicon membrane for thermal conductance control.

For the 40 GHz CLASS detector, the backshort must be placed 2.04 mm from the OMT. We chose to integrate the backshort into silicon using micromaching techniques. For CLASS, the silicon backshort assembly not only provides a quarter-wave backshort but also mitigates high frequency leakage that can couple to the TES or other unshielded circuit components [5]. An additional component called the silicon interface chip is bonded to the detector chip. This component is used to shield the backside of the TES from high frequency leakage as well as to extend the ground plane of the detector chip improving the efficiency of a photonic choke joint [13] which is machined into the focal plane [9].

B. Silicon backshort

In this section we will discuss the fabrication of the silicon backshort assembly as well as the silicon interface chip. The silicon backshort assembly for the 40 GHz detector is made up of three silicon wafers. The 0.875 mm thick "interface" wafer, and the 1.16 mm thick "spacer" wafer define the quarter-wave delay, which is terminated by an RF short by the metalized surface of the 0.325 mm thick "cap" wafer. All of the wafers are fabricated from degeneratively doped silicon with room temperature resistance between 1 to 3 mΩ·cm and residual resistivity ratio (RRR) of 1.7. Each of the 3 wafers is processed separately and subsequently bonded at the wafer level by gold thermo-compression bonding [14]. A schematic diagram of the backshort is shown in Fig. 3.

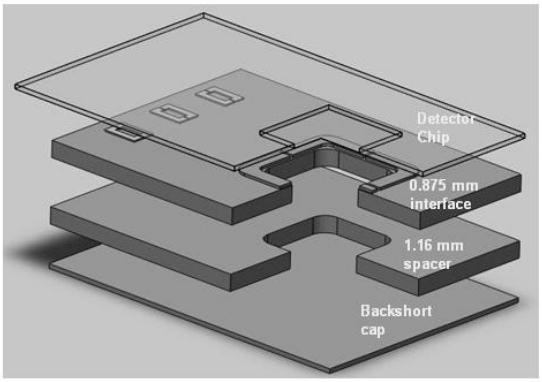

Fig. 3 Schematic Diagram of the Backshort integrated with CLASS 40 GHz detector chip.

We split up the backshort assembly into a stack of three wafers to improve the sidewall profile of the waveguide, which is etched by deep reactive ion etching using the well-known Bosch process [15]. The Bosch process consists of alternating a plasma passivation step with C_4F_8 and an etching step using SF_6. By adjusting the ratio between the etch time and the passivation time the etch rate and sidewall slope can be controlled. For very thick wafers however, it is difficult to maintain a high aspect slope without the buildup of silicon grass that forms due to unetched fluorocarbon passivation.

The grass can ultimately limit silicon etching. To simplify the requirements, we split the through wafer etching into two steps where we etch halfway through the wafer from either side. This requires a front to back alignment and results in an hourglass waveguide profile with a 2° reentrant slope off of the horizontal. A representative profile of the 1.16 mm thick spacer is shown in Fig. 4a.

The 0.87 mm thick wafer is processed similarly to the 1.16 mm wafer where the through-wafer DRIE is etched from both sides. Since this wafer forms the interface to the detector chip, there is an additional 50 µm deep relief etch completed on the surface of the backshort wafer that mates to the detector chip to accommodate the Nb microstrip. The backshort interface wafer contacts the detector wafer around the OMT and around the TES membranes with a 150 µm wide mousehole to accommodate the Nb microstrip lines. The sizes of the cavities around the TES are designed such that they do not support in-band resonances. An SEM image of the relief etch is shown in Fig. 4b.

We additionally micromachine silicon bumps at the contact interface. When the bonding epoxy is applied to the silicon bumps, capillary action forces it to flow between the bumps only in the contact area while maintaining it only in areas where bonding should occur.

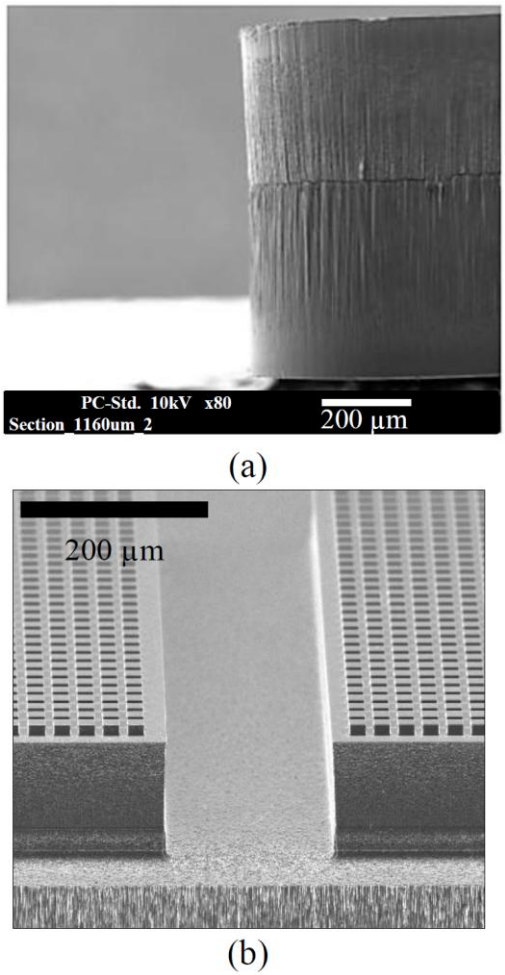

Fig. 4 (a) Silicon sidewall profile of 1.16 mm wafer etched by DRIE. (b) SEM image of the relief etch.

Once the three backshort wafers are complete, they are cleaned and coated with 0.5 µm of Au by electron beam evaporation. The Au coats both the sidewalls of the waveguide and the surface of the silicon. The Au coated wafers are bonded in a Karl Suss SB6e substrate bonder at 360° C and 4 bar pressure following standard Au-Au thermo-compression bonding procedures [14]. The bonding sequence consists of first bonding the cap wafer to the 1.16 mm spacer wafer, then bonding the cap/spacer stack to the backshort interface wafer. The surface that interfaces with the detector chip is then coated with Nb to reduce microwave loss. The final step in the backshort fabrication process is to dice the 2 mm thick stack into individual backshorts. An image of the backshort assembly is shown in Fig. 5.

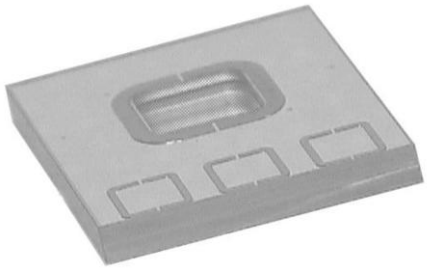

Fig. 5 Image of a completed Backshort Assembly.

C. Silicon Interface Chip

The last component in the detector assembly is a silicon interface chip that mates the detector chip with the CLASS focal plane. We elected to incorporate the interface chip to reduce the required size of the detector chips, which are the most complicated and time consuming fabrication process. This allowed an increase of the number of chips per four inch wafer from 4 to 13. The interface chip increases the effective size of the detector chip ground plane thus improving the efficiency of a photonic choke that is machined into the focal plane [9], [13]. It also terminates the back of the cavities under the TES membranes, magic-T and microstrip crossovers. It is etched such that it can be clamped against metal posts on the focal plane simplifying mounting to the focal plane. The interface chip is 0.32 mm thick low resistance silicon that is coated with Al to reduce microwave loss. The backshort assembly, detector chip and interface chip are hybridized by flip-chip bonding. First, the backshort assembly is bonded with epoxy to the detector chip followed by bonding the interface chip to the back of the detector chip. The photo in Fig. 6 shows a detector, which has completed hybridization.

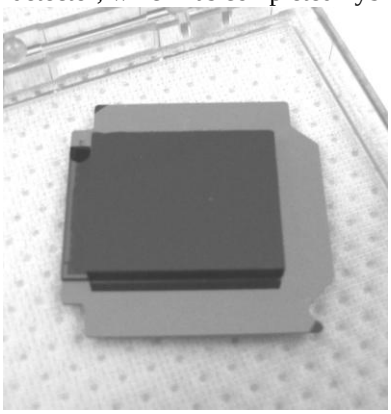

Fig. 6 Hybridized CLASS 40 GHz micromachined TES detector.

III. CONCLUSIONS

We have described a fabrication method for integrating silicon backshorts to TES based superconducting detectors for cosmic microwave background polarimetry. The backshort design had the goal of minimizing out of band leakage of stray radiation to the TESs or to other microwave components such as filters, magic-T and crossover structures. Fabrication of the backshorts uses deep reactive ion etching micromachining techniques and gold-gold thermo-compression bonding at the wafer level. The backshorts are epoxy bonded to the detectors at the chip level. We have recently completed fabrication of our new smaller form factor 40 GHz detectors with thermal and microwave measurements currently in progress. The first prototype of the 90 GHz CLASS detectors has also been completed.

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