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# Impact of Total Ionizing Dose Radiation Testing and Long-Term Thermal Cycling on the Operation of CMF20120D Silicon Carbide Power MOSFET

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## Background

Power systems designed for use in NASA space missions are required to work reliably under harsh environment conditions. Radiation, thermal cycling, and extreme temperature exposures, which are typically encountered in almost all of the space exploration missions, are a major concern for the operation and reliability of on-board electronics of the spacecraft power system. Besides reliability, efficiency constitutes another critical requirement in space applications where size and weight are of utmost importance. This, in turn, would require the use of high power, low-loss devices and circuits capable of operation in space-borne radiation and other environmental stresses.

Today's electronics based on silicon technology would not be able to meet the stringent requirements of space systems without the use of the present-day conventional radiation-shielding structures and thermal control elements for proper operation. Semiconductor devices based on wide bandgap materials, especially silicon carbide (SiC), are becoming more readily available as the enabling technologies begin to mature. The wide bandgap structure of SiC-based power devices offers great benefits when compared with those made of silicon (Si). Some of these advantages include high breakdown voltage, higher power and current densities, low on-resistance, higher switching frequency, and high operating temperatures. Table I lists a comparison of properties of silicon and silicon carbide semiconductor materials [1]. By being able to withstand large voltages with small leakage currents and fast switching speeds, SiC devices show great promise and become good candidates for use in future power electronic systems. The low on-resistance of wide band-gap materials allows the development of a new generation of transistor devices that switch faster and with greatly reduced losses. The combined higher switching speed and efficiency of these transistors, for example, allows the operation of DC/DC converters at very high frequencies, thereby reducing weight, saving board space, and conserving power.

Information pertaining to performance of these new wide bandgap devices in the space environment is very scarce. Such data is very critical so that proper design is implemented in order to ensure mission success and to mitigate risks associated with exposure of on-board systems to the space operational environment. In this work, samples of an N-channel enhancement-mode metal-oxide-semiconductor field effect transistor (MOSFET) based on SiC technology were exposed to radiation followed by long-term thermal cycling over a wide temperature range to determine their susceptibility and to address their reliability for use in space applications. The results of this experimental work are presented and discussed. This report must be viewed in COLOR.

Table I. Properties of silicon and silicon carbide semiconductor materials [1].

| Property | Si | 3C-SiC | 6H-SiC | 4H-SiC |
|---|---|---|---|---|
| Bandgap, $E_g$ (eV at 300K) | 1.12 | 2.4 | 3 | 3.2 |
| Critical electric field, $E_c$ (V/cm) | $2.5x10^5$ | $2x10^6$ | $2.5x10^6$ | $2.2x10^6$ |
| Thermal conductivity, (W/cm.K at 300K) | 1.5 | 3-4 | 3-4 | 3-4 |
| Saturated electron drift velocity, $v_{sat}$ (cm/s) | $1x10^7$ | $2.5x10^7$ | $2x10^7$ | $2x10^7$ |
| Electron mobility, $\mu_e$ ($cm^2$/Vs) | 1350 | 1000 | 500 | 950 |
| Hole mobility, $\mu_h$ ($cm^2$/Vs) | 480 | 40 | 80 | 120 |
| Dielectric constant | 11.9 | 9.7 | 10 | 10 |

**Scope of Work**

Five samples of COTS (commercial-off-the-shelf) SiC power MOSFETs were used in this investigation. The devices, part # CMF20120D, are produced by Cree Inc. using their patented Z-FET$^{TM}$ technology [2]. These parts exhibit low drain-source on-resistance ($R_{DS(ON)}$), low capacitance, are easy to parallel, and are suited for high voltage DC/DC converters, solar inverters, and motor drives. Some of the manufacturer's specifications of this power MOSFET are listed in Table II.

Table II. Manufacturer's specifications of CMF20120D [2].

| Part # | CMF20120D |
|---|---|
| Drain-source breakdown voltage, $V_{(VBR)DSS}$, (V) | 1200 |
| Gate threshold voltage, $V_{TH}$ (V) | 2.5 |
| Drain Current, $I_D$ (A) | 33 |
| Drain-source on-resistance, $R_{DS(ON)}$ (mΩ) | 80 |
| Operating temperature, $T_C$ (ºC) | -55 to +125 |
| Package | Plastic TO-247-3 |

The experimental work involved performing total ionizing dose radiation testing on only three of the five samples, while the other two were un-irradiated (labeled as control). The three devices that underwent radiation exposure had various bias conditions while being irradiated as described in Table III. Following the radiation exposure, all five samples were exposed to long-term thermal cycling.

Table III. Condition of test articles.

| Device Label | Sample Condition |
|---|---|
| 2 | Control |
| 5 | Control |
| 4 | Irradiated, Biased ON: Vgs = 20V, Vds = 0V |
| 7 | Irradiated, Biased OFF: Vgs = 0V, Vds = 900V |
| 9 | Irradiated, Grounded: Vgs = 0V, Vds = 0V |

### *Radiation Exposure*

Total ionizing dose testing of the parts was performed at GSFC. The samples in this test were surface-mounted on copper boards having pins designed to plug into wire wrap sockets. The parts were irradiated using a $^{60}$Co source, at varying dose rates of 500-1000 rad(Si)/min during the day, and 5-25 rad(Si)/min overnight, to a total dose of 400 krad(Si). The parts were tested until the threshold voltage dropped below 1 V (there is no minimum threshold voltage specified for these parts so this was arbitrarily chosen as the failure threshold).

After 400 krad(Si), the MOSFETs underwent a one-week room-temperature anneal under bias, with measurements at 24 hours post-anneal, and following the full 168-hour anneal. Parts were then irradiated for an additional 200 krad(Si). They were then subjected to a 168-hour anneal at 100 °C, with measurements only after the full time period. A total of ten MOSFETs were used for this test, seven of which were biased either in an on-state (three devices), off-state (two devices), or grounded state (two devices), with the remaining three devices used as a controls. Specifically, the on-state bias conditions were 20 V on the gate and grounded source and drain; the off-state bias conditions were grounded gate and source and 900 V on the drain; and the grounded bias conditions shorted all pins to ground. Unfortunately, several parts died during the execution of the test, so only five parts were available for thermal cycling – two controls and one from each irradiated test condition.

### *Thermal Cycling*

The thermal cycling activity on the samples was performed using a Sun Systems Environmental Chamber, Model EC12, that employs liquid nitrogen as the coolant. The chamber has a built-in controller that allows setting and controlling of the temperature rate of change, dwell times, and extreme set points. The thermal cycling profile implemented in this investigation, which is depicted in Figure 1, comprised:

- Total # of Cycles 1000
- Temperature rate of change: 10 ºC/min
- Temperature range: -55 ºC to +125 ºC
- Soak time at extreme temperatures: 10 min

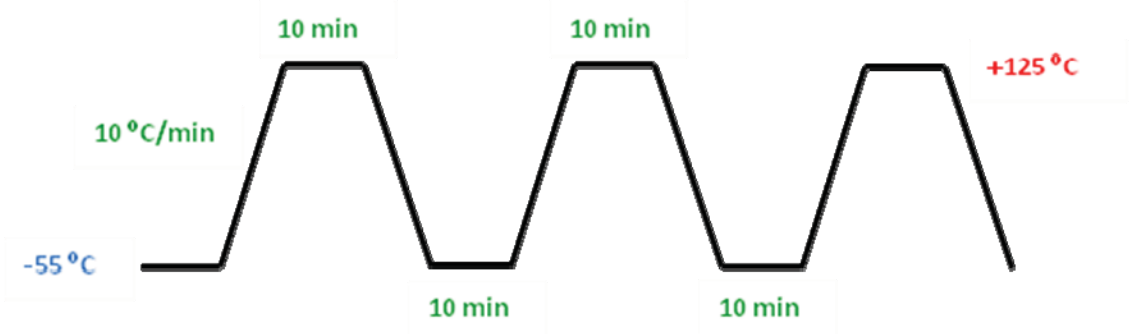



Figure 1. Profile of thermal cycling.

### *Device Characterization*

Parametric evaluation of the power MOSFETs was performed following the radiation exposure in terms of drain current ($I_D$) versus drain-to-source voltage ($V_{DS}$) family curves at various gate voltages ($V_{GS}$), voltage threshold level ($V_{th}$)), and drain-to-source on-state resistance ($R_{DS(on)}$). These measurements were made using a Sony/Tektronix 370A programmable curve tracer and Keithley 238 Source-Measure Units. The device properties' characterization was performed at the test temperatures of 20 °C, -55 °C, and +125 °C before, during, and after the thermal cycling exposure.

## Results

### *TID Testing*

Like most SiC-based power devices, the CMF20120D showed a high tolerance to total ionizing dose. The parameters most affected by dose were threshold voltage, breakdown voltage, turn-on delay time, and turn-off delay time. The parts biased in the on-state showed the greatest degradation across the parameters measured. For this set of experiments, failure was defined as occurring when the threshold voltage degraded to less than 1 V, which occurred at 400 krad(Si) for the parts biased in the on-state, as shown in Figure 2. A change in the breakdown voltage was also observed, as seen in Figure 3, only for the case of the biased-on parts, and dropped as low as 1 V at 400 krad(Si) for one of the parts. The other radiation-induced changes in the on-state biased devices comprised of a decrease in the turn-on delay time and an increase in the turn-off delay time as a function of dose as shown in Figure 4 and 5, respectively. The amount of degradation observed would have to be evaluated by designers to determine at what point the changes would become unacceptable, and the parts would not actually be appropriate for use in spaceflight applications. Overall, the parts appear robust to TID levels well beyond what is typically seen in NASA missions.

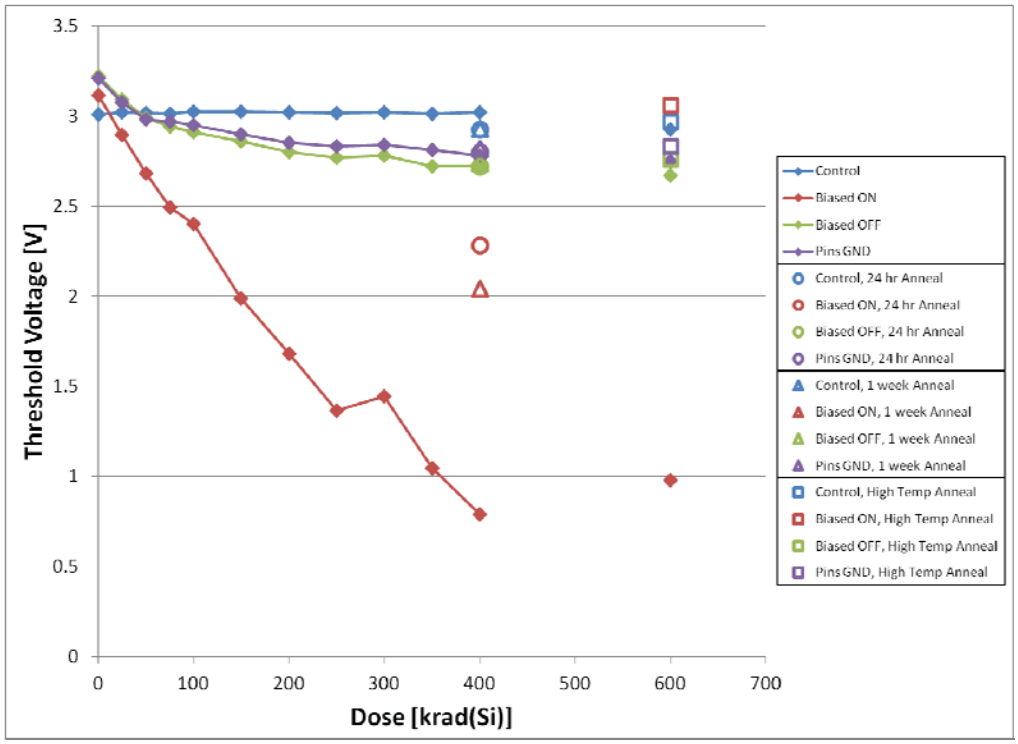



Figure 2. Variation in threshold voltage with dose level.

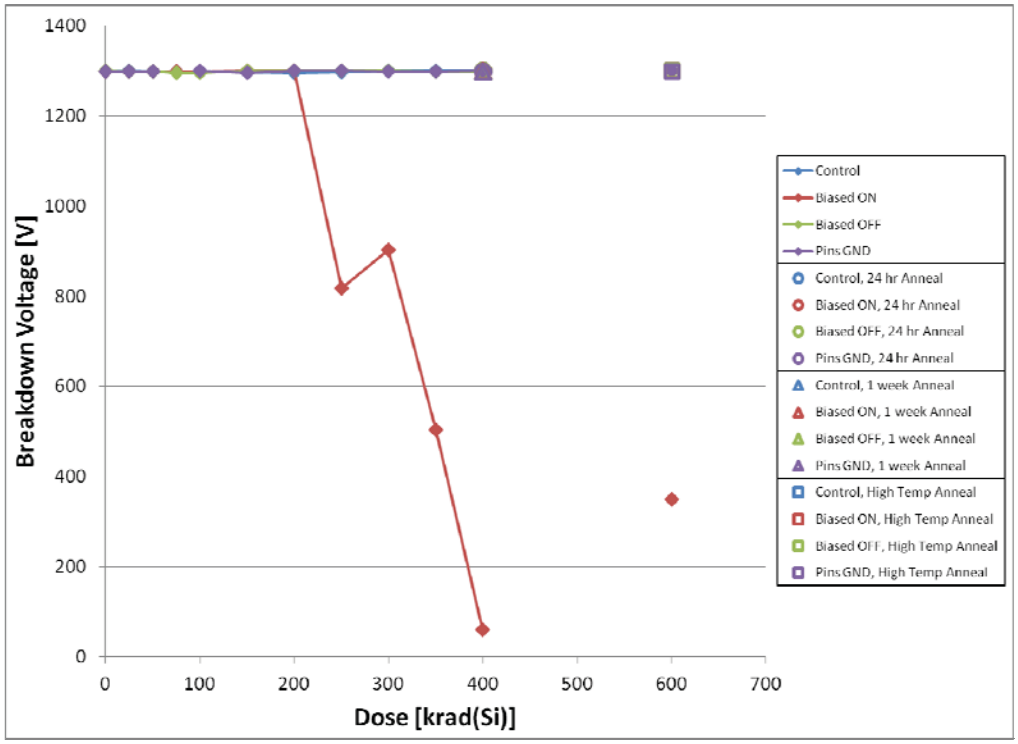



Figure 3. Breakdown voltage as a function of total dose.

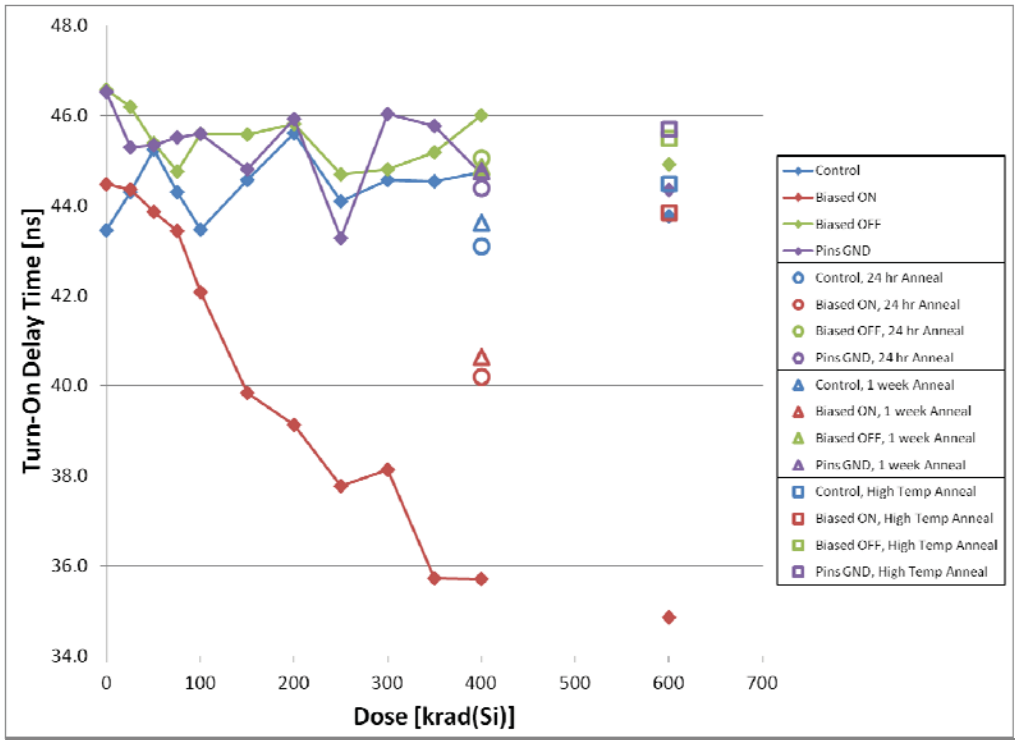



Figure 4. Turn-on delay time versus dose.

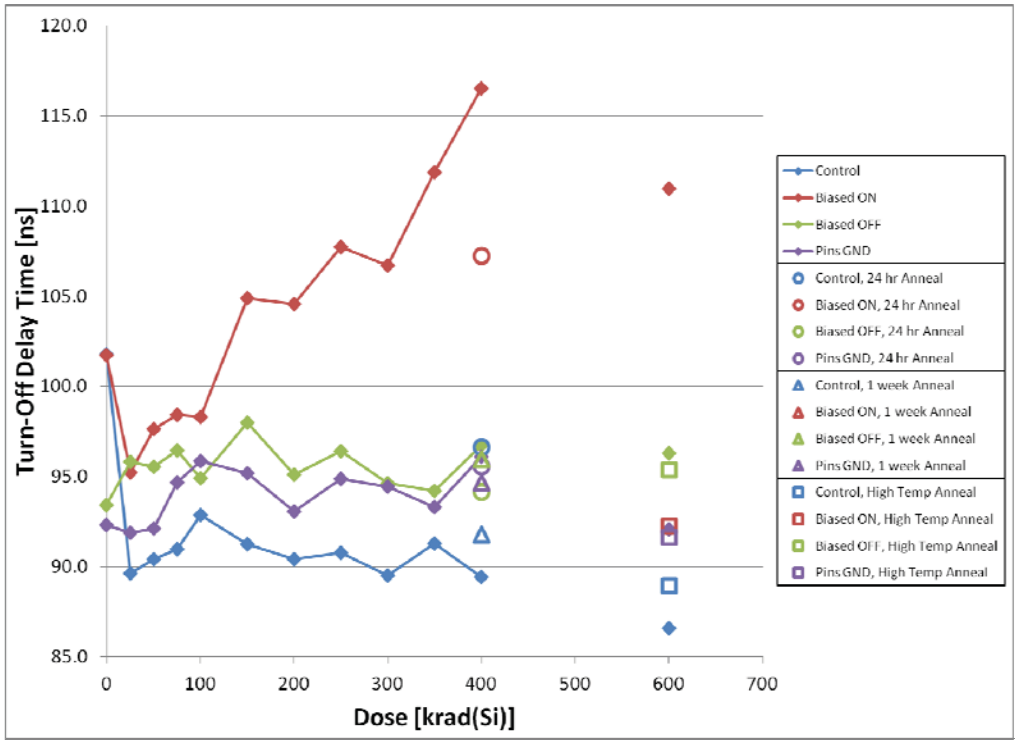



Figure 5. Turn-off delay time versus dose.

### *Temperature Effects*

Figure 6 shows the pre-cycling output characteristics of the controlled and irradiated MOSFET devices at the selected test temperatures of 20, -55, and +125 °C. The output characteristics are defined as the drain current ($I_D$) versus drain-to-source voltage ($V_{DS}$) family curves at various gate voltages ($V_{GS}$). The test temperature seemed to influence the output I/V curves of the MOSFET devices in similar fashion regardless of their conditioning. In other words, both the control and the irradiated samples underwent changes in their characteristics with change in test temperature. The first change is reflected in the downward shift of the I/V curves as the temperature is decreased from room temperature to -55 °C. This trend is reversed upon increasing the temperature to +125 °C. These changes can be attributed to the increase in the gate threshold voltage at low temperatures, while it decreases as the temperature is increased. The second deviation observed in the output characteristics of all devices is the decrease in the slope of the I/V curves in the switching region, while the opposite is true. This phenomenon is primarily caused by the increase in the on-state resistance with decreasing temperature. Such effects of test temperature on the $V_{th}$ and $R_{DS(on)}$ of the device, for all samples, are shown in Figures 7 and 8, respectively.

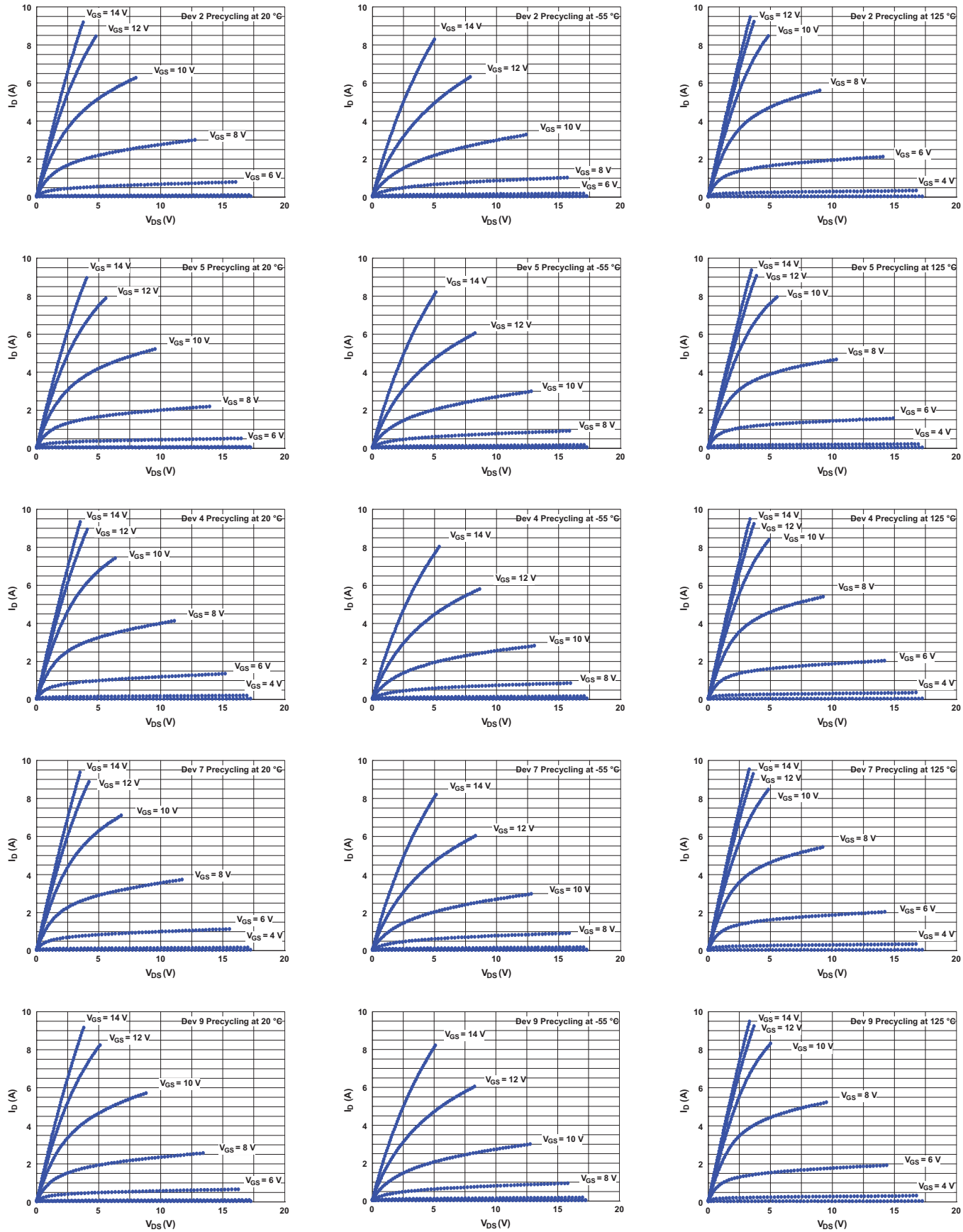



Figure 6. Pre-cycling I/V characteristics of MOSFETs at 20 °C, -55 °C, and +125 °C for control devices #2 & #5 (first two rows) and irradiated devices #4, #7, & #9 (bottom rows).

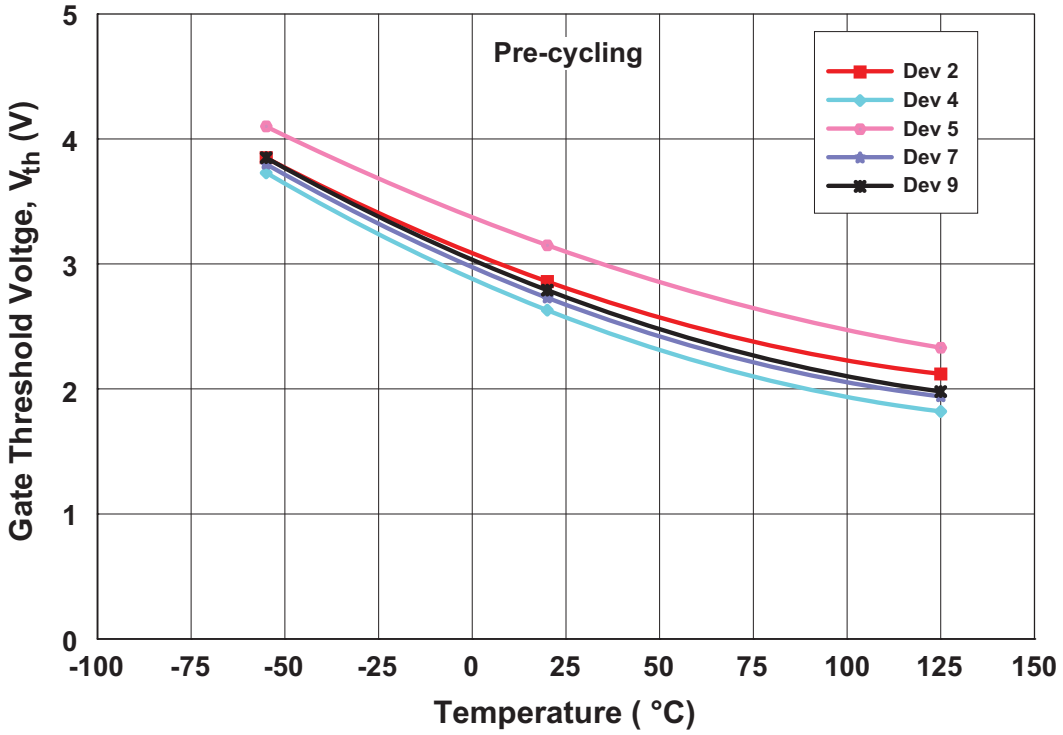



Figure 7. Variation in threshold voltage with temperature prior to cycling.

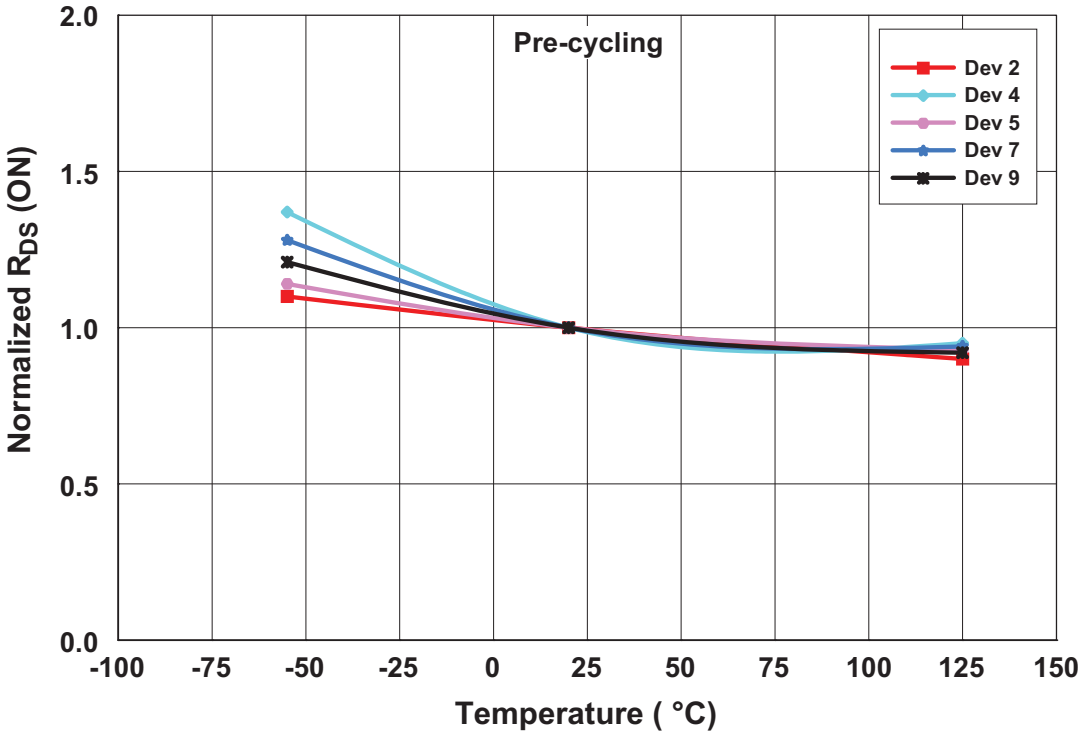



Figure 8. MOSFET's on-state resistance (normalized) versus temperature prior to cycling.

***Thermal Cycling***

As was mentioned earlier, the MOSFET devices were exposed to a total of 1000 cycles between -55 °C and +125°C and parametric measurements were performed during, as well as, after conclusion of the cycling activity. These characterizations were done after the completion of 500 cycles, 750 cycles, and 1000 cycles. The following two points need to be noted in presenting data pertaining to the thermal cycling:

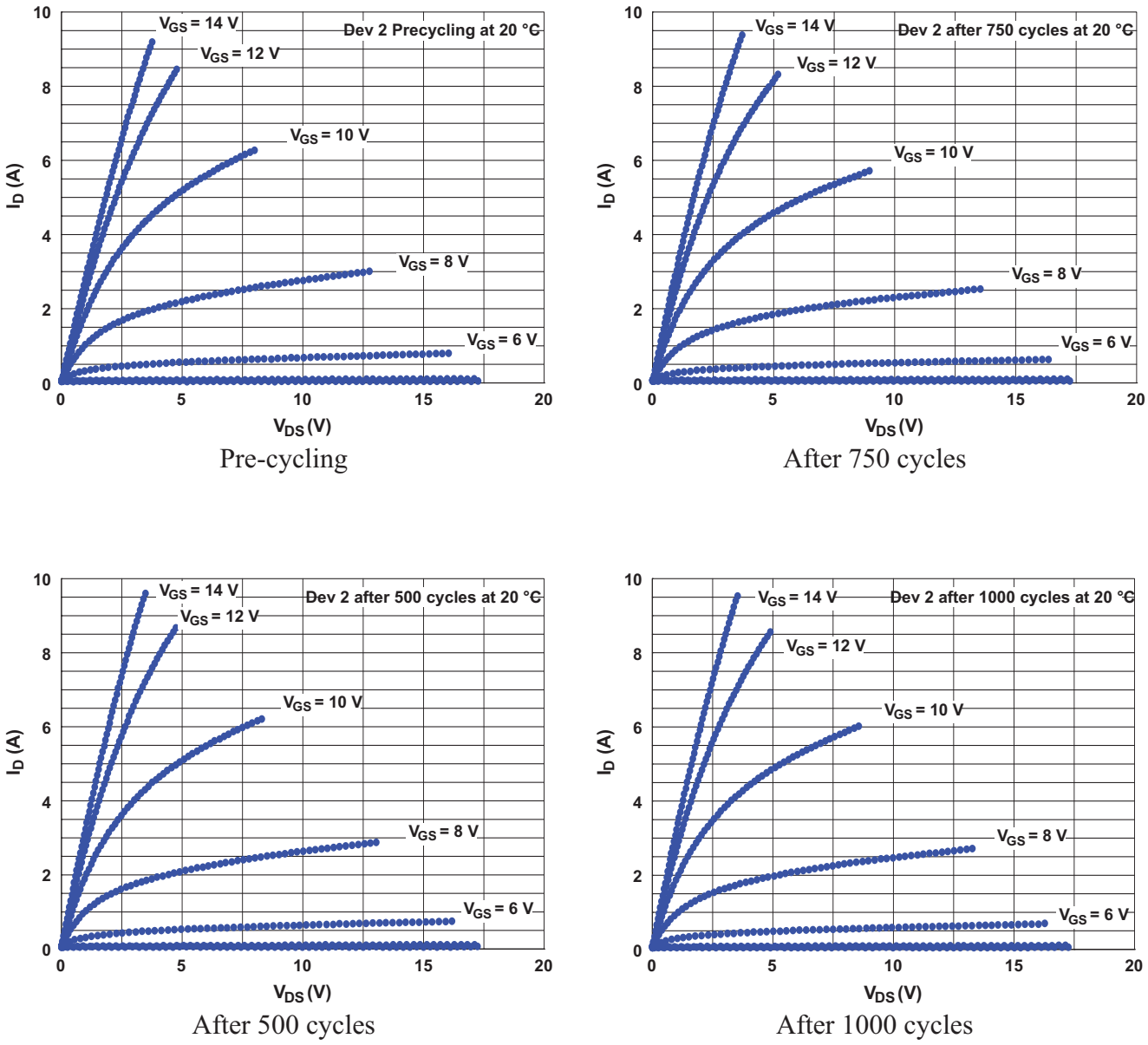
- Both control samples, i.e. devices #2 and #5, exhibited the same behavior in their characteristics with regard to cycling, therefore, only the data pertaining to device #2 is presented here while that of device #5 is given in the Appendix.

- During the thermal cycling, data specific to each one of the device tested obtained at a given test temperature, i.e. 20 °C, -55 °C, or +125 °C, showed the same trend with cycling. Thus, results obtained at 20 °C only, for all parts, are reported in this section; while those taken at -55 °C and +125 °C are shown in the Appendix.

The room temperature I/V output curves of control device #2 obtained at various stages of the cycling activity are shown in Figure 9. It is evident that the cycling activity has not caused any major changes in the characteristics of these curves. The only apparent variation is a slight decrease in the slant of the I/V curves as the device underwent cycling. This effect, which was experienced by the control device #2, was found to apply for the irradiated samples as well regardless of the bias applied during the radiation exposure. The output characteristics for these devices, parts #4, #7, and #9, are shown in Figures 10, 11, and 12, respectively.

Figure 13 shows the dependence of the gate threshold voltage ($V_{th}$) of all devices on temperature taking into account the thermal cycling applied to the test specimen. As was mentioned earlier, a decrease in test temperature causes an increase in the threshold voltage of the power MOSFET. While this phenomenon seemed to be more profound in the low temperature region and is experienced by all devices, control as well as irradiated, the thermal cycling seemed not to influence the gate threshold voltage property of any of the tested devices, as depicted in Figure 9.

Although the drain-to-source on-state resistance ($R_{DS(on)}$) showed similar dependency on test temperature as that of the gate threshold voltage, albeit more severity is exhibited at cryogenic temperatures, application of the thermal cycling seemed to exacerbate this effect on all of the devices tested. This impact of thermal cycling can be seen in Figure 14, and is an indicative of the decrease in the steepness of the I/V curves for control as well as irradiated devices in their linear region as stated earlier.



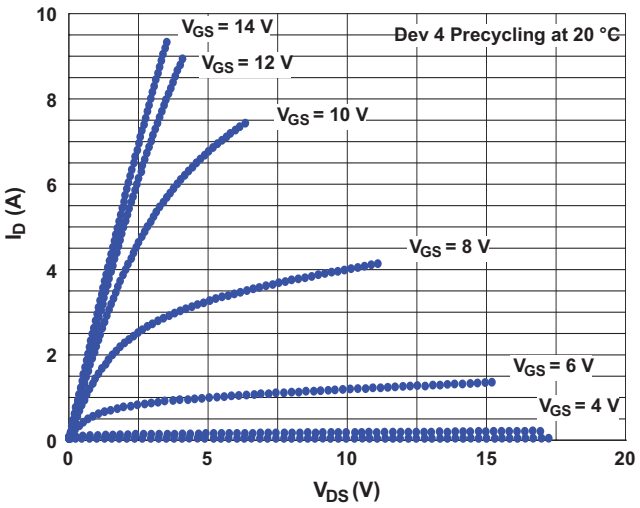

Pre-cycling

After 750 cycles

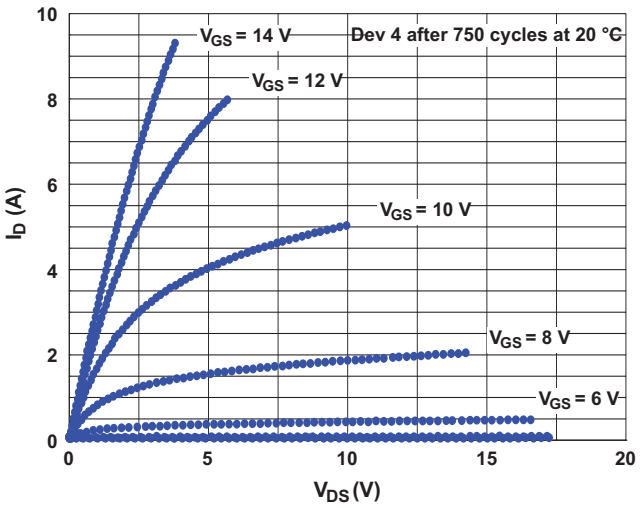
After 500 cycles

After 1000 cycles

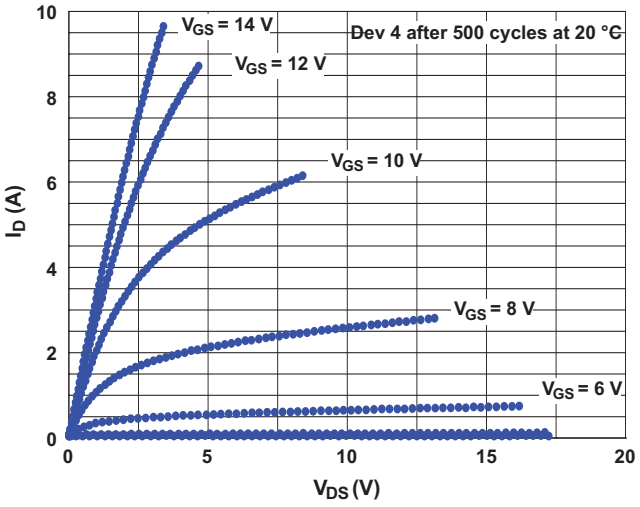
Figure 9. I/V curves of un-irradiated device #2 at various stages of thermal cycling.



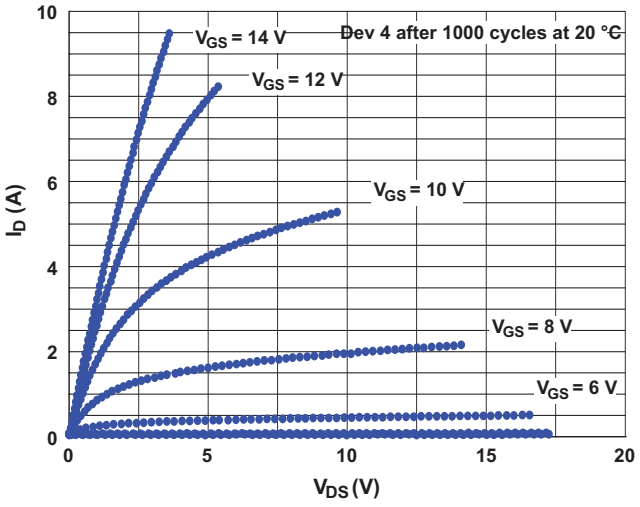

Pre-cycling




After 750 cycles

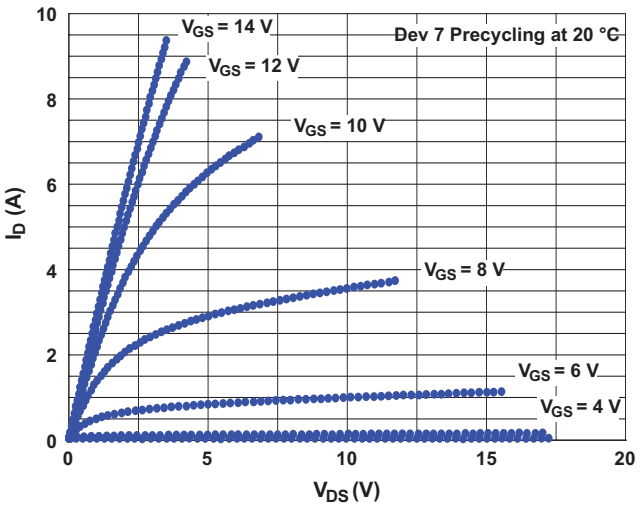



After 500 cycles

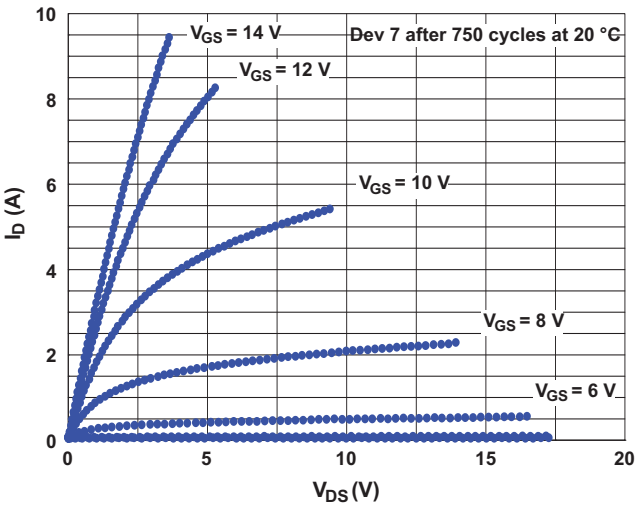



After 1000 cycles

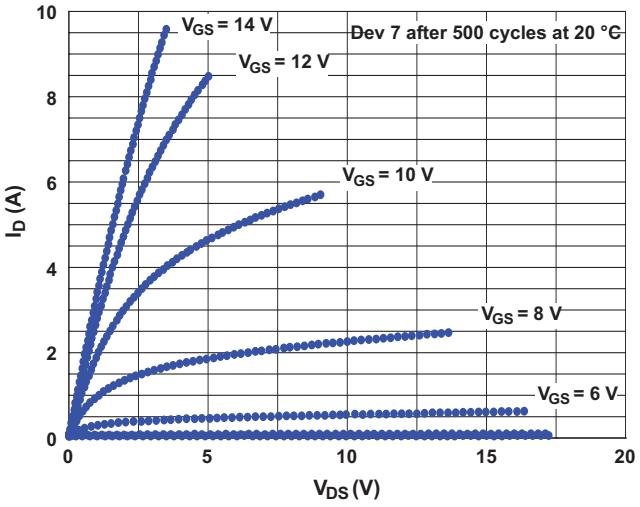
Figure 10. I/V curves of device #4 (that had been irradiated in the Biased-ON condition) at various stages of thermal cycling.



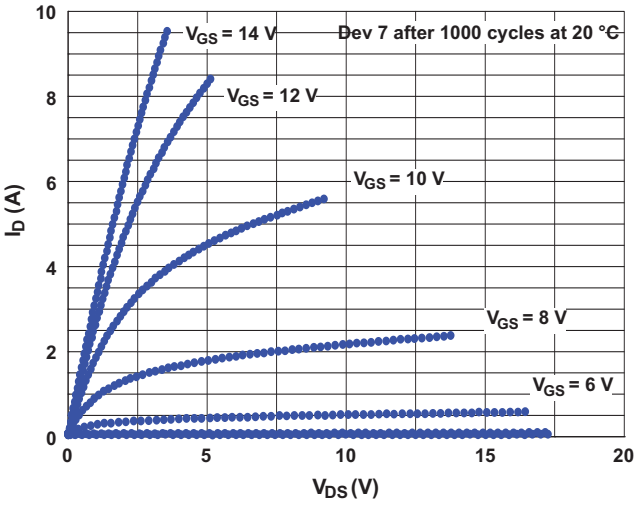

Pre-cycling




After 750 cycles

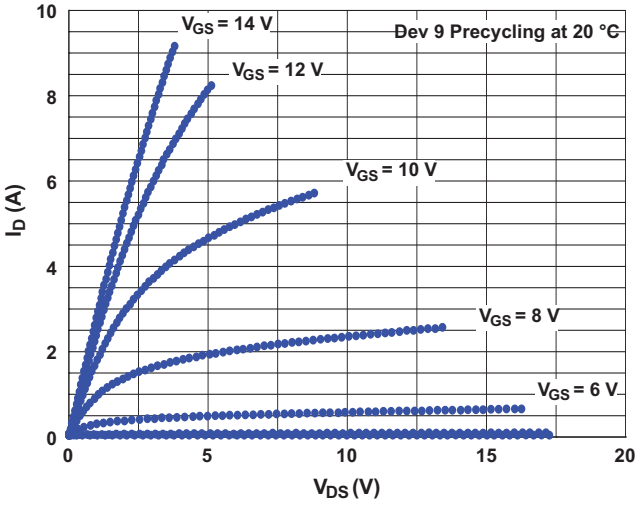



After 500 cycles

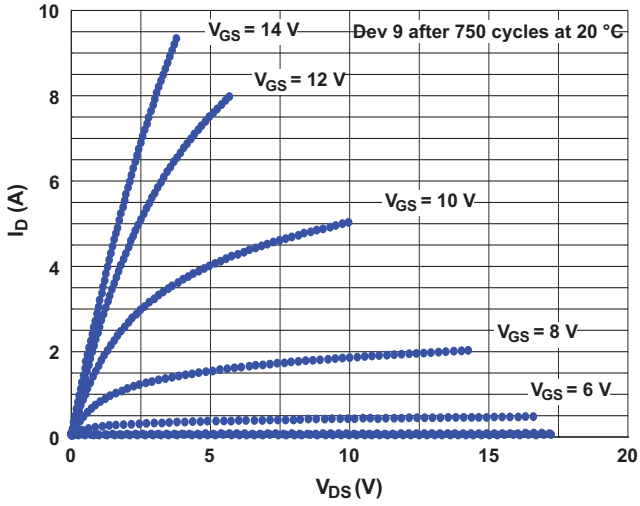



After 1000 cycles

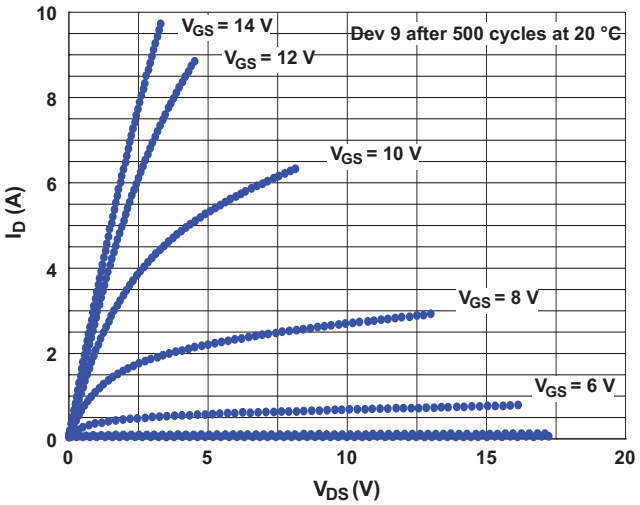
Figure 11. I/V curves of device #7 (that had been irradiated in the Biased-OFF condition) at various stages of thermal cycling.



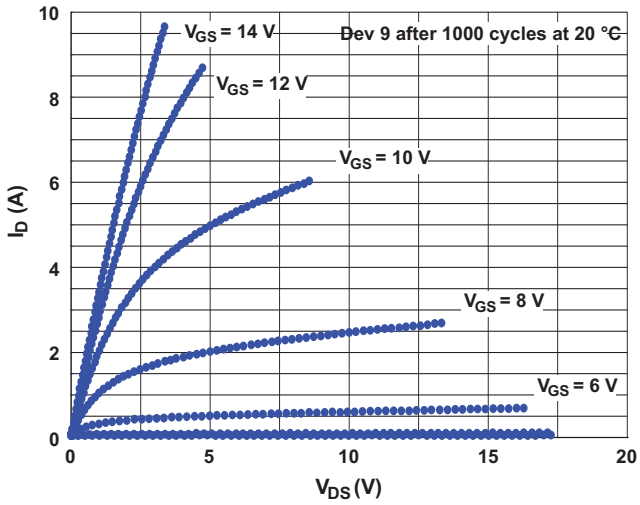

Pre-cycling




After 750 cycles

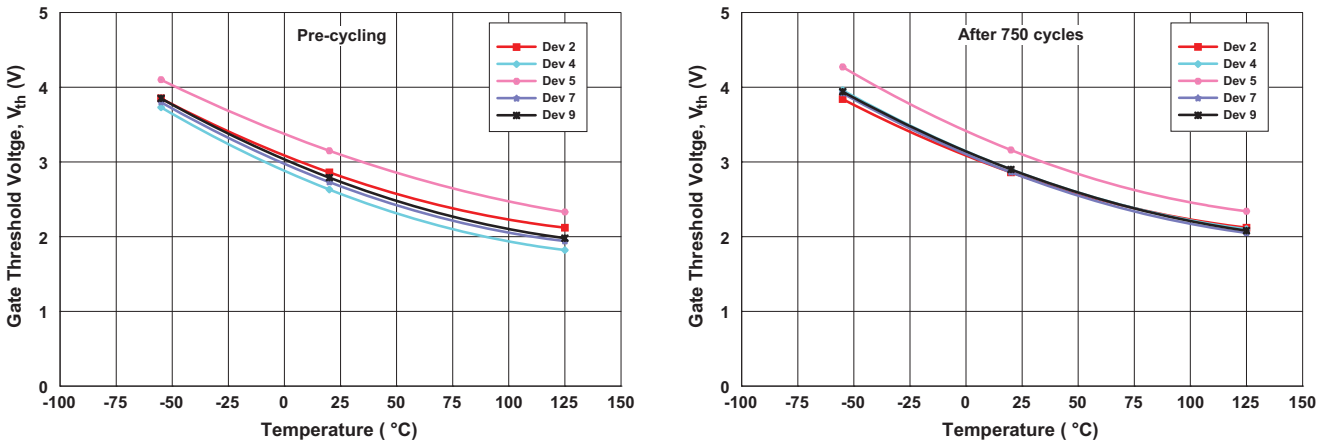



After 500 cycles




After 1000 cycles

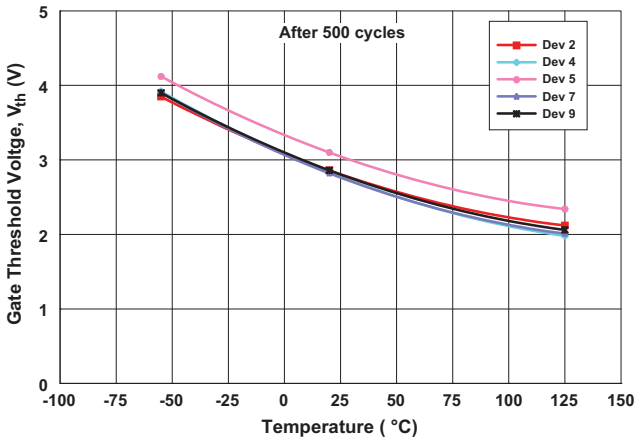
Figure 12. I/V curves of device #9 (that had been irradiated with all pins GROUNDED) at various stages of thermal cycling.



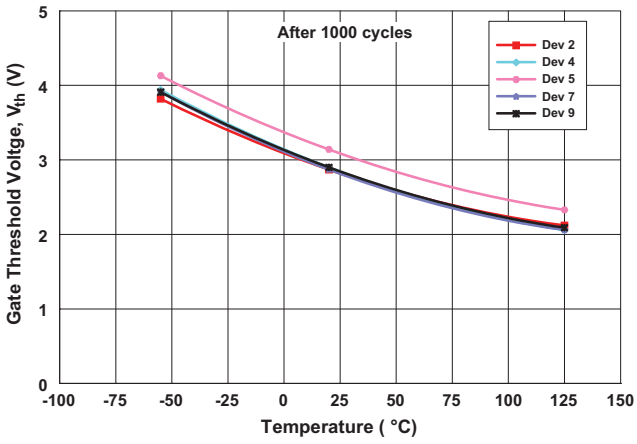

Pre-cycling




After 750 cycles




After 500 cycles




After 1000 cycles

Figure 13. Gate threshold voltage versus temperature at various stages of thermal cycling.

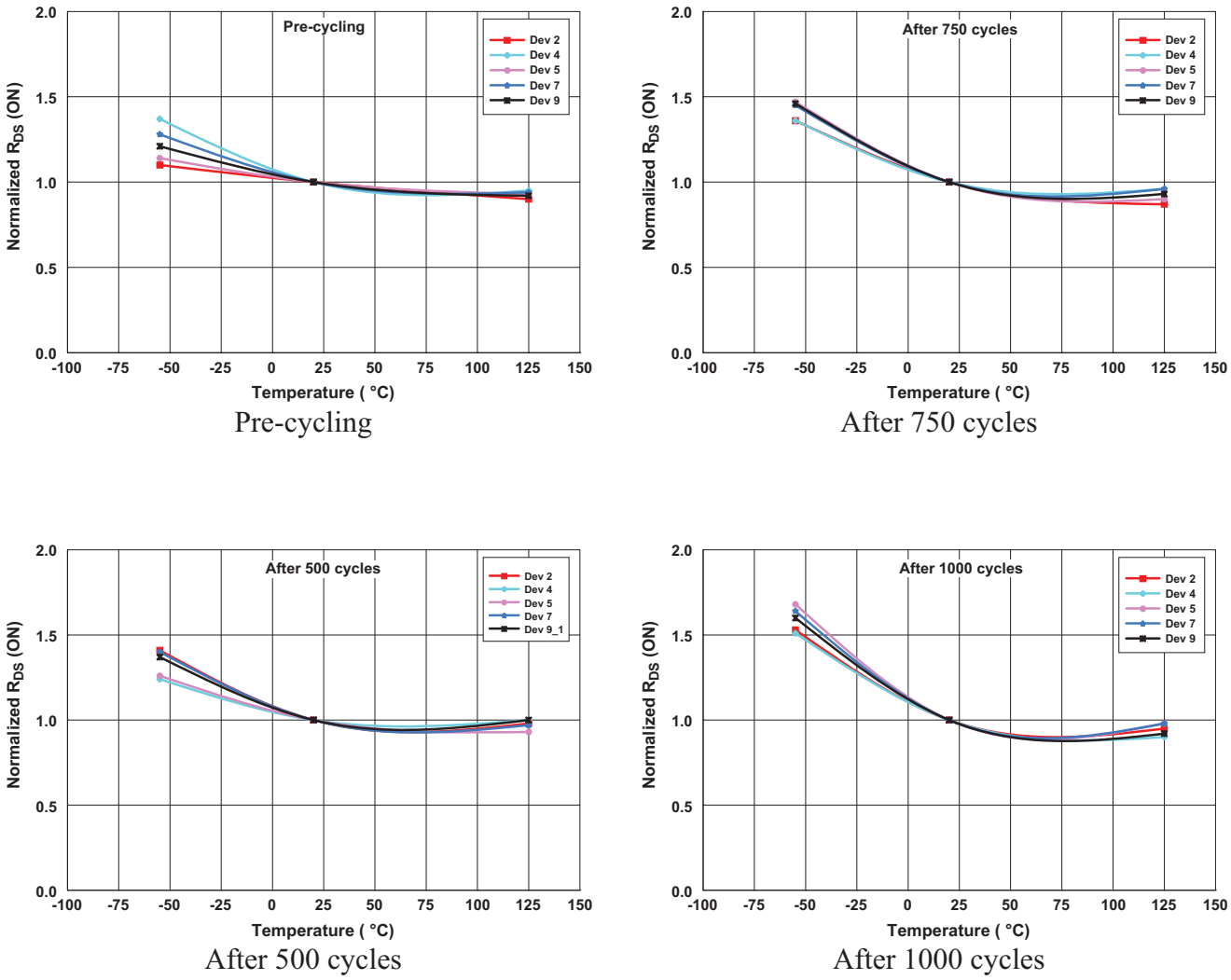



Figure 14. On-state resistance versus temperature at various stages of thermal cycling.

### *Extreme Temperature Re-Start*

After 1000 cycles of thermal cycling, re-start capability of the five SiC power MOSFETs at extreme temperatures was investigated by allowing each device to soak at the cryogenic temperature of -55 °C and at the hot temperature of +125 °C for at least 20 minutes without the application any electrical bias. Power was then applied to the device under test, and measurements were taken on the output characteristics. All devices were able to successfully re-start at either temperature, and the results obtained were similar to those obtained under the same test temperature condition while under bias.

## Conclusion

Power systems designed for use on many of NASA space missions are required to be efficient, reliable, and capable of operation under exposure to radiation, thermal cycling, and extreme temperatures. In this work, the effects of total ionizing dose radiation testing and wide-temperature thermal cycling on the performance of silicon carbide power MOSFET transistors was investigated under different bias conditions. Results of the radiation testing indicate that the parts are very robust to TID and would survive at dose levels well above most NASA missions.

The long-term thermal cycling of these power MOSFETs didn't seem to cause any catastrophic damage to these parts. While the gate threshold voltage property of any of the tested devices was found to maintain its value throughout the cycling activity, the drain-to-source on-state resistance ($R_{DS(on)}$) experienced an increase in its value with cycling, most notably in the low temperature region. Such a trend was similar for all of the tested devices, control as well as irradiated, regardless of the bias conditions.

## References


[1]. L. Scheick, "Rad Effects in Emerging GaN FETs," 3rd NASA NEPP Electronic Technology Workshop, June 2012.

[2]. Cree Inc., CMF20120D-Silicon Carbide Power MOSFET" Data Sheet, #CMF20120D Rev. A, http://www.cree.com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