

An Airborne Onboard Parallel Processing Testbed

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Objectives for Intelligent Payload Module Testbed

- Low power/high performance benchmarking
 - Test various typical onboard science processing requirements with parallel processing via multicore processors and field programmable gate array circuits
 - Target processors that can be radiation tolerant or radiation hardened
- Airborne Intelligent Payload Module(IPM) box used as proxy for satellite version of IPM
- Research being conducted under AIST-11 effort, “A High Performance Onboard Multicore Intelligent Payload Module for Orbital and Suborbital Decadal Missions”

Potential Users of IPM

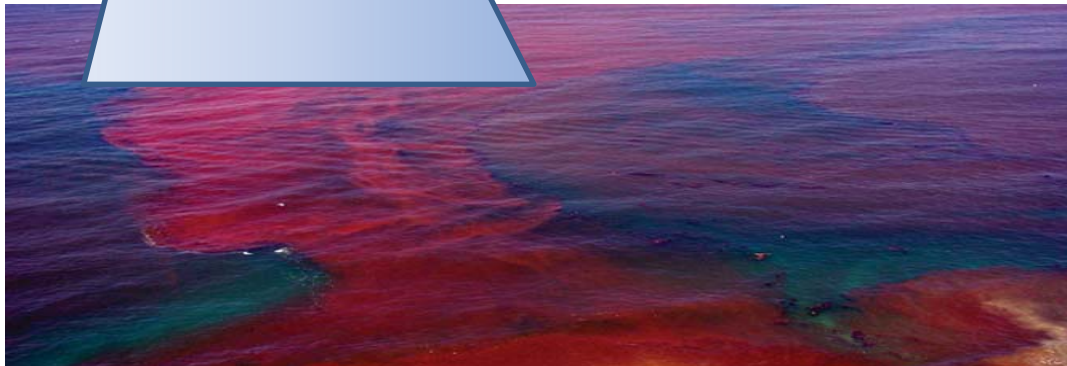
- HypsIRI Smallsat mission
 - Visible ShortWave InfraRed (VSWIR) Imaging Spectrometer
 - Multispectral Thermal InfraRed (TIR) Scanner
- HypsIRI Space Station mission
 - Visible ShortWave InfraRed (VSWIR) Imaging Spectrometer
 - Multispectral Thermal InfraRed (TIR) Scanner
- Geocape

Sample Operational Scenario: Detection of Harmful Algal Blooms with Rapid Map Downlinked to Validation Team on Ground



- Realtime map with following processing steps:
- ✓ Radiance to reflectance conversion
 - ✓ Atmospheric Correction
 - ✓ Geocorrection/Co-registration
 - ✓ Classification (Web Coverage Processing Service)
 - ✓ Vectorization and data reduction

Downlink to Ipad



Harmful Algal Bloom

Processors Used in Conjunction With The Testbed

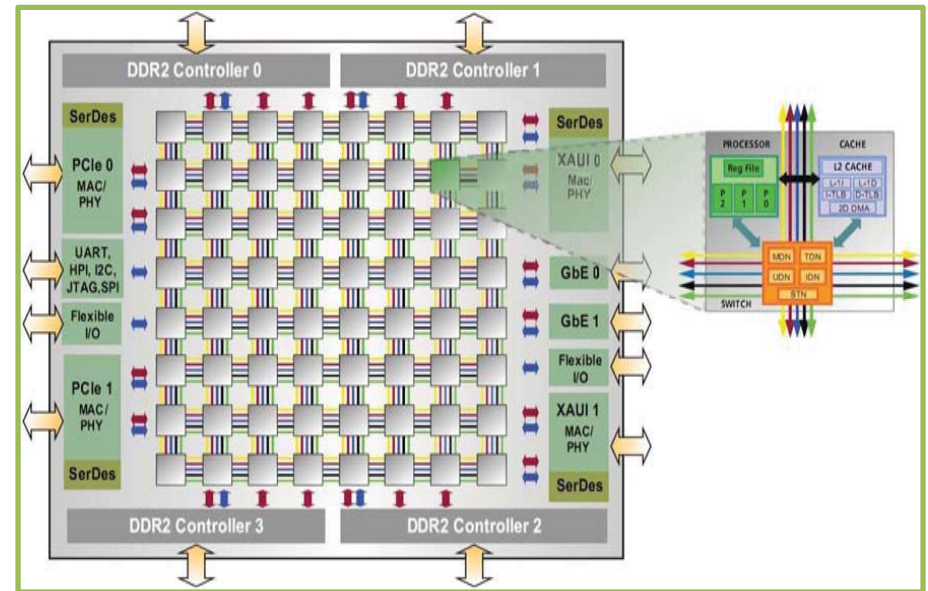
Tilera Tile64 as Proxy for Maesto

Specifications

- Launched on August 20, 2007
- **8 x 8 tile array (64 cores)**
- Each tile on chip is an independent processor capable of running an entire operating system
- 700MHz - 866MHz (No FPU)
- 15 - 22W @ 700MHz all 64 cores running
- Idle tiles can be put into low-power sleep mode
- ANSI standard C / C++ compiler
- Supports SMP Linux with 2.6 kernel

Issues

- Special data homing considerations required when programming/compiling for the TILE64
 - Uses a crude coherence strategy; each shared memory location may only be cached in one tile – its “home” tile. A location’s home tile is fixed at runtime
 - Accessing remotely-cached data is correct, but performance is low
 - Prevents TILE64 from efficiently running existing generic multithreaded code
 - Careful “homing” of data is crucial to good scalability
- TILE64’s compiler does not use the now-standard C++ ABI popularized by GCC 3.2+
 - This compiler is closed-source, based on SGI’s “MIPSPro”
 - Prevents linkage with and preprocessing by other C++ compilers, such as AESOP



Maestro as Proxy for Maestro-lite

- Origin - DARPA Polymorphic Computer Architecture (PCA Program)
- DARPA/DTRA Radiation Hardened By Design (RHBD) 90 nm IBM CMOS process
- Government purchased Tiler Corp's (commercial 64 core processor) software intellectual property (IP) for government space-based applications
- Program managed by National Reconnaissance Office (NRO)
- Maestro Chip developed by Boeing Solid-State Electronics Development (SSED)
- Government customers: NASA, NRO, Air Force Research Laboratory
- Maestro basic specifications
 - 7 x 7 tile array (49 cores)
 - 300 MHz, 45 GOPs, 22 GFLOPS (FPU on each tile)
 - 18 Watts typical
 - RHBD Total Ionizing Dose (TID) >500krad

Tilera TilePro64 as Proxy for Maestro

Specifications

- Launched on September 22, 2008
- **8 x 8 tile array (64 cores)**
- Each tile on chip is an independent processor capable of running an entire operating system
- 700MHz - 866MHz (No FPU)
- 19 - 23W @ 700MHz all 64 cores running
- Idle tiles can be put into low-power sleep mode
- ANSI standard C / C++ compiler
- Supports SMP Linux with 2.6 kernel

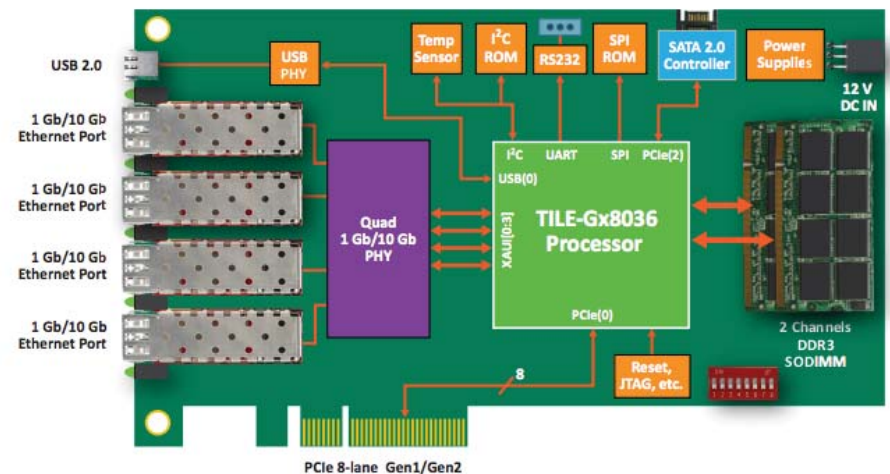
Addressed issues exhibit in TILE64

- Uses a better cache coherence protocol allowing many tiles to cache the same data
- The native compiler is now an open-source port of GCC 4.4, using standard C++ ABI
 - Compiler and toolchain is actively supported
 - October 14 2011 - Tilera contributed its port back to the GCC project
- First-class Linux kernel architecture
- **Presently in IPM used during recent flights**

Tilera Tile-Gx8036 / Tile-Gx8009 as Proxy for Maestro

Specifications

- Launched on January 30, 2012
- 6 x 6 tile array (36 cores) / 3 x 3 tile array (9 cores)
- Each tile on chip is an independent processor
- capable of running an entire operating system
- 1GHz – 1.5GHz (FPU)
- 27 - 30W @ 1.2GHz all 36 cores running
- 9 – 10W @ 1.0GHz all 9 cores running
- Idle tiles can be put into low-power sleep mode
- ANSI standard C / C++ compiler
- Supports SMP Linux with 2.6 kernel



SpaceCube 1.5

| Unit | Mission | Notes | Specs | Stats | Status |
|-----------------------|---|---|--|---|--|
| SpaceCube 1.0a | Hubble SM 4 | RNS Experiment STS-125 May 2009 | 4"x4" card (2) Virtex4 | Size: 5"x5"x7" Wt: 7.5 lbs Pwr: 16W x 2 | 2009 Flight |
| SpaceCube 1.0b | MISSE-7/8 | added RS-485, RHBS, STS-129 Nov 2009 | 4"x4" card (2) Virtex4 | Size: 5"x5"x7" Wt: 7.5 lbs Pwr: 16W x 2 | Operating on ISS Since Nov 2009 |
| SpaceCube 1.5 | SMART | added GigE & SATA SubTec-5 Jun 2011 | 4"x4" card (1) Virtex5 | Size: 5"x5"x4" Wt: 4 lbs Pwr: 10W | 2011 Flight |
| SpaceCube 1.0c | Argon Demo | added 1553 & Ethernet | 4"x4" card (2) Virtex4 | Size: 5"x5"x7" Wt: 7.5 lbs Pwr: 18W x 2 | Demonstration Testbed |
| SpaceCube 1.0 d, e, f | STP-H4, future STP-H5 & RRM3 | added 1553 & Ethernet | 4"x4" card (2) Virtex4 | Size: 5"x5"x7" Wt: 7.5 lbs Pwr: 15W | On ISS Since Aug 2013 |
| SpaceCube 2.0 | Earth/Space Science, SSCO, GPS Nav | Std 3U form factor, GigE, SATA, Spacewire, cPCI | 4"x7" card (2) Virtex 5 + (1) Aeroflex | Size: 5"x5"x7" Wt: < 10 lbs Pwr: 15-20W | EM On ISS Since Aug 2013 (Flight Unit In Development) |
| SpaceCube 2.0 Mini | CubeSats, Sounding Rocket, UAV | "Mini" version of SpaceCube 2.0 | 3.5"x3.5" card (1) Virtex 5 + (1) Aeroflex | Size: 4"x4"x4" Wt: < 3 lbs Pwr: 8W | Flight Unit in Development (2016 launch) |

SpaceCube Family Overview

v1.0



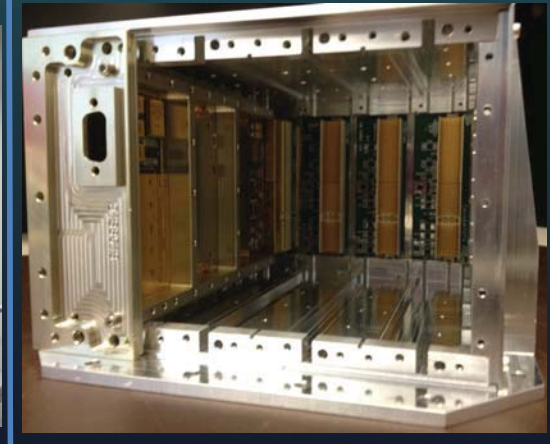
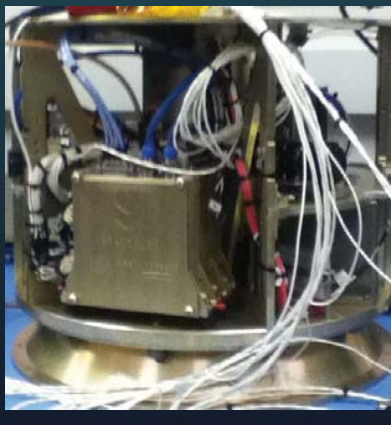
v1.5



v2.0-EM



v2.0-FLT



2009 STS-125
 2009 MISSE-7
 2013 STP-H4
 2016 STP-H5

2012 SMART

2013 STP-H4
 2016 STP-H5

2015 GPS Demo
 - Robotic Servicing
 - Numerous proposals
 for Earth/Space/Helio

Processor Comparison

| Processor | MIPS | Power | MIPS/W |
|-------------------|------|-------|--------|
| MIL-STD-1750A | 3 | 15W | 0.2 |
| RAD6000 | 35 | 15W | 2.33 |
| RAD750 | 300 | 15W | 20 |
| LEON 3FT | 75 | 5W | 15 |
| LEON3FT Dual-Core | 250 | 10W | 25 |
| BRE440 (PPC) | 230 | 5W | 46 |
| Maxwell SCS750 | 1200 | 25W | 48 |
| SpaceCube 1.0 | 3000 | 7.5W | 400 |
| SpaceCube 2.0 | 6000 | 10W | 600 |
| SpaceCube Mini | 3000 | 5W | 600 |



ZC702 – Zynq (ARM/FPGA Processor) Proxy for COTS+RH+FTC CHREC Space Processor (CSP)

COTS

- Zynq-7020 hybrid SoC
 - Dual ARM A9/NEON cores
 - Artix-7 FPGA fabric + hard IP
- DDR3 memory

RadHard

- NAND flash
- Power circuit
- Reset circuit
- Watchdog unit

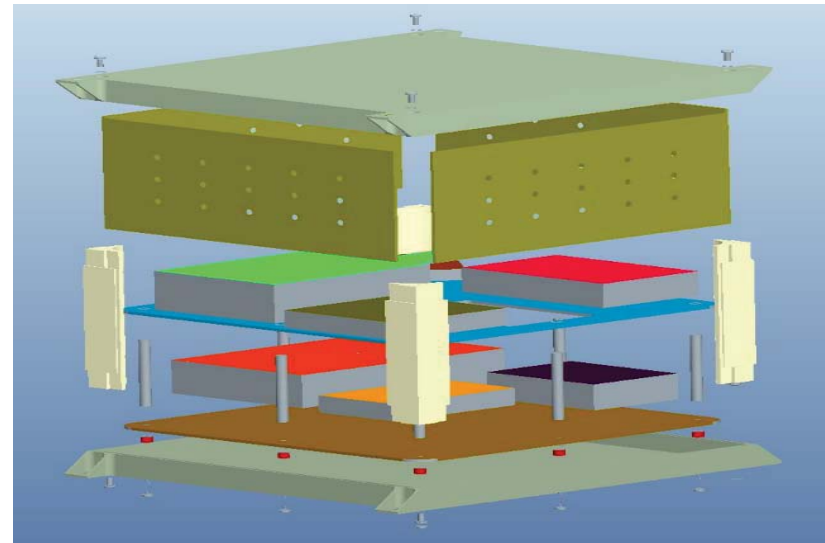


FTC = Fault-Tolerant Computing

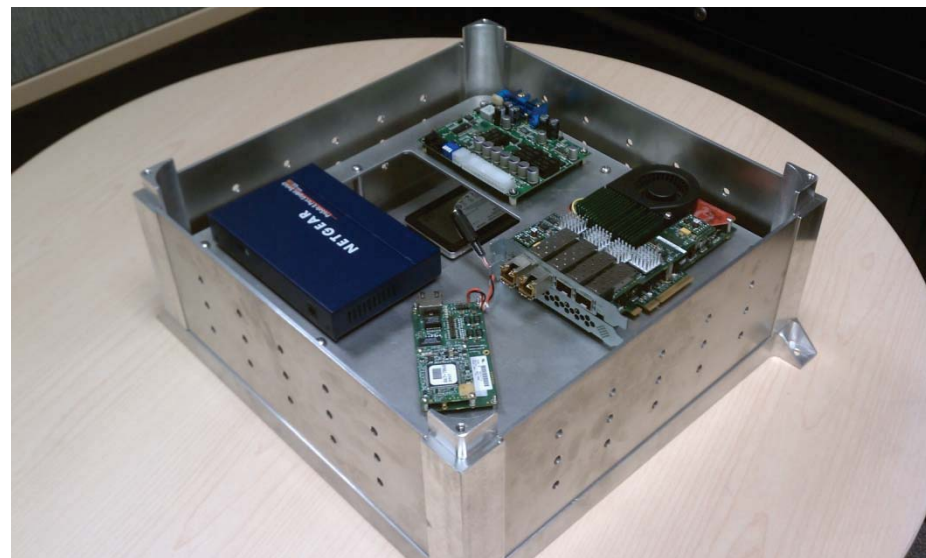
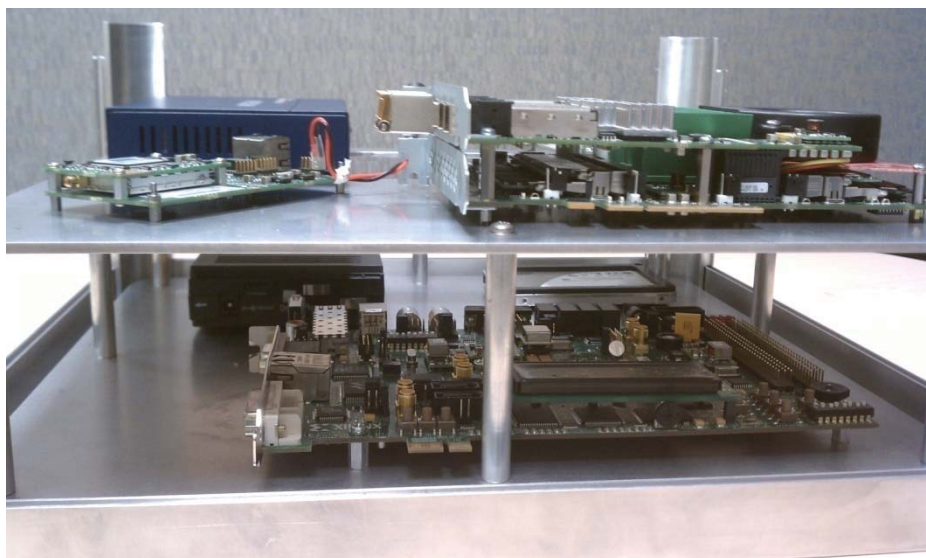
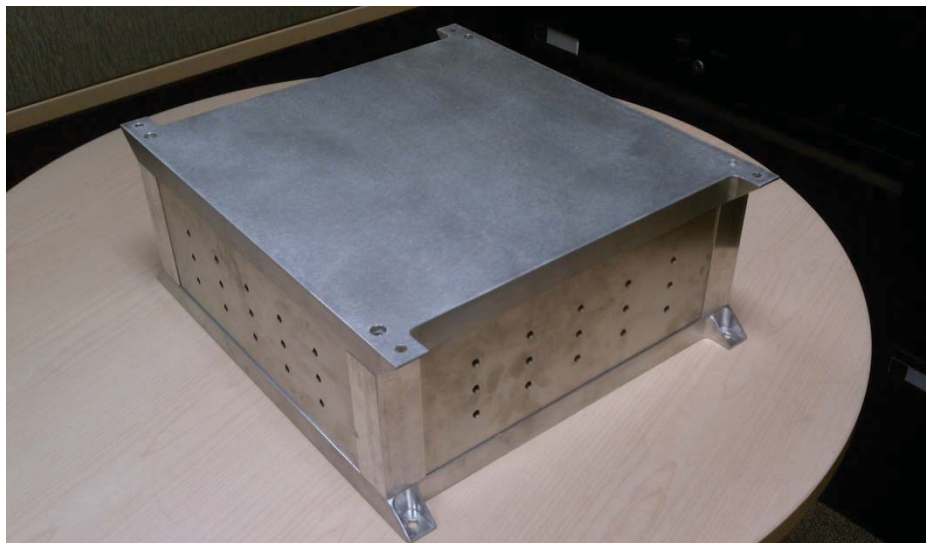
- Variety of mechanisms
 - External watchdog unit to monitor Zynq health and reset as needed
 - RSA-authenticated bootstrap (primary, secondary) on NAND flash
 - ECC memory controller for DDR3 within Zynq
 - ADDAM middleware with message, health, and job services
 - FPGA configuration scrubber with multiple modes
 - Internal watchdogs within Zynq to monitor behavior
 - Optional hardware, information, network, software, and time redundancy

IPM Hardware

- 14 x 14 x 6 inches
- Wide-Input-Range DC voltage (6V-30V)
- Made of strong durable aluminum alloy
- Dual mounting brackets
- Flush design
- Removable side panels
- Mounting racks are electrically isolated from the box
- Appropriate space allocation for interchangeable Tileria
 - and SpaceCube boards
- Electronic components
 - Tileria development board
 - SpaceCube development board
 - Single board computer
 - 600GB SSD
 - Gigabit Ethernet switch
 - Transceiver radio
 - Power board



IPM Hardware



Compact Hyperspectral Advanced Imager (CHAI V640)



SPECIFICATIONS

| MECHANICALS | ESTIMATE |
|-------------------------------------|-------------------|
| Size (with lens) | 125 x 101 x 75 mm |
| Size (with telescope) | 200 x 101 x 75 mm |
| Weight | .48 kg [.99 lbs] |
| Power | 20 watts |
| Temperature Range | -20 to +50 C |
| <i>Size does not include NS/GPS</i> | |

| OPTICS | SPECIFICATION |
|-------------------------|--|
| Spectrometer Type | Dyson |
| Telescope | All-reflective telescope |
| Field of View | 40 degrees |
| Cross Track Pixels | 640 |
| F-Number | f/2 |
| Spectral Range | 350-1080 nm (Reflective) 400-1000 nm (Refractive) |
| Smile Distortion | < 0.1 pixels |
| Keystone Distortion | < 0.1 pixels |
| Stray Light | < 1e-4 Point Source Transmission |
| Spectral Bands | 256 |
| Spectral Sampling | 2.5, 5, 10 nm |
| Peak Grating Efficiency | 88% |
| Slit Size | 9.6 x .015 mm |

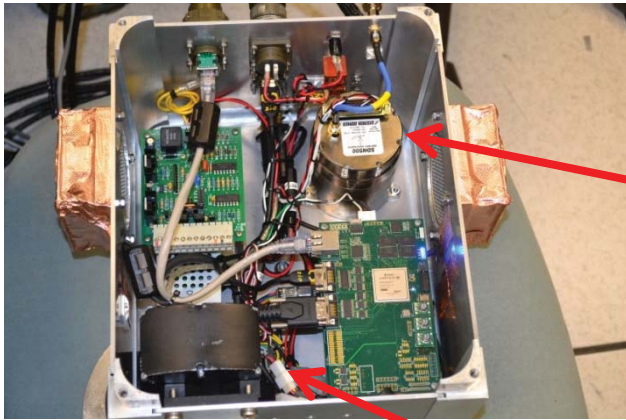
| IMAGE SENSOR | |
|--------------------|--|
| Image Sensor | 640 x 512, with 15 μ m pixels |
| Full Well Capacity | Gain 0: 500,000 Gain 1: 60,000 Gain 2: 10,000 |
| Read Noise | Gain 0: < 63 electrons Gain 1: < 42 electrons Gain 2: < 10 electrons |
| Maximum Frame Rate | 1000 frames/second |
| Quantum Efficiency | > 50% @ 380 nm 80% @ 400-900 nm > 30% @ 1000 nm |
| Camera Interface | USB-3 |
| Data Acquisition | 500 MB Solid State Recorder Serial Interface for GPS/INS |

| CHAI SOFTWARE | |
|---------------|---|
| Trigger Modes | Pilot, GUI, electronic, and Lat/Long triggered acquisition |
| Visualization | 3-band RGB waterfall display of real-time and recorded data |
| Metadata | Temperature, pressure, and humidity |
| Data Format | RAW, ENVI BIL, or Processed |
| Processing | EXPRESSO™ |



from Brandywine
Electronics
Contact: John Fisher

ChaiV640 Box and IPM (Tilera Multicore Proxy for Maestro)

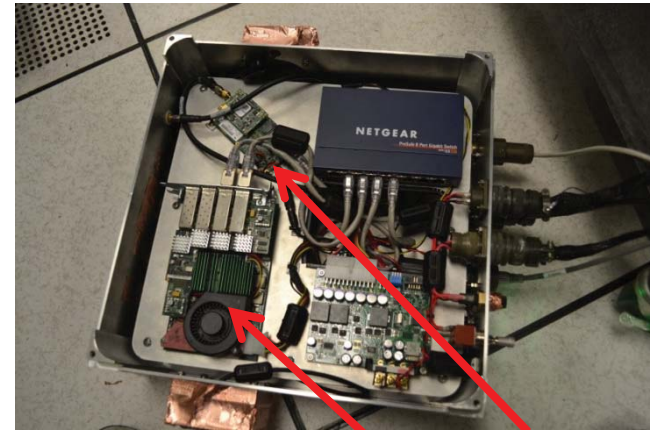


SDN500
IMU

ChaiV640 Box

Brandywine
ChaiV640

ChaiV640 Box Mounted on Helo



IPM

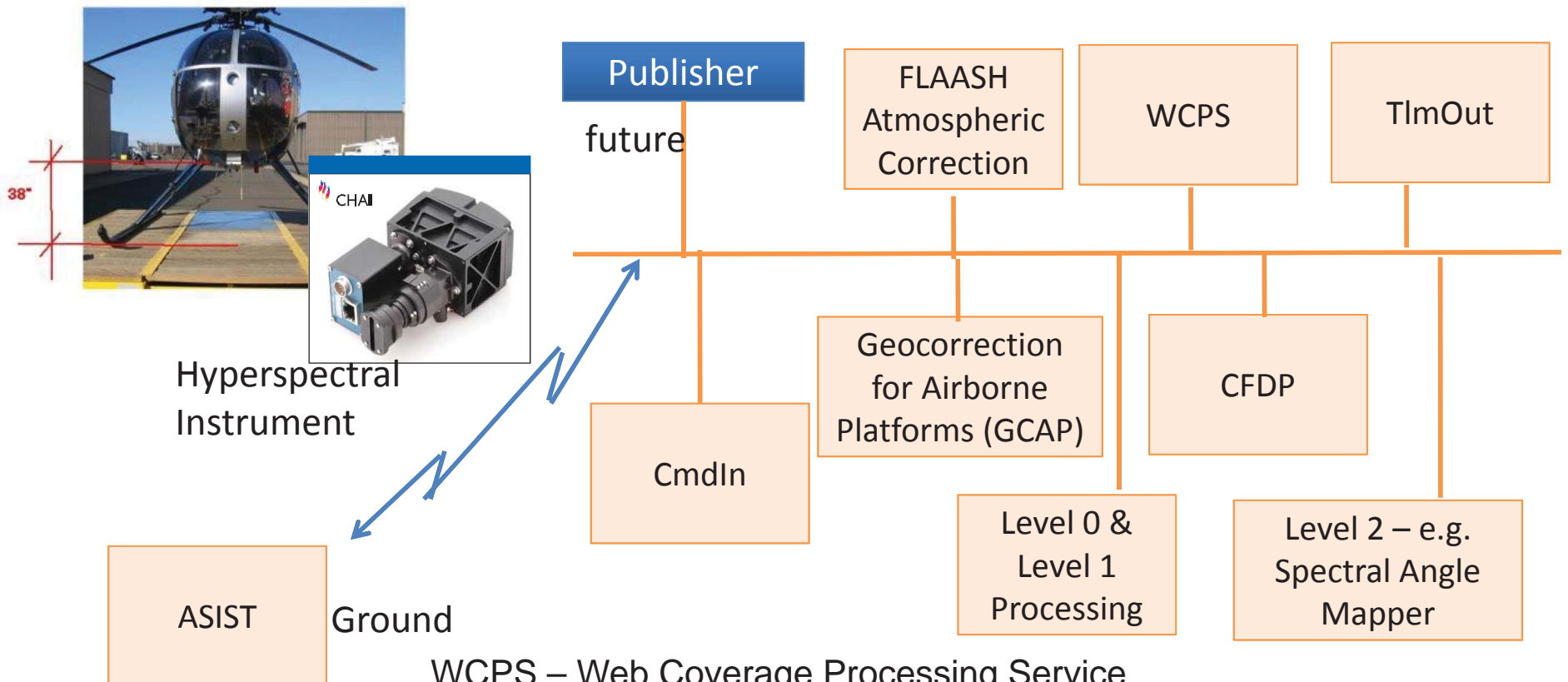
Freewave
Transceiver

Tilera TilePro

ChaiV640/IPM on Bussmann Helo Takeoff



Software with Addition of Publisher Node Onboard IPM



WCPS – Web Coverage Processing Service

CmdIn – Command Ingest

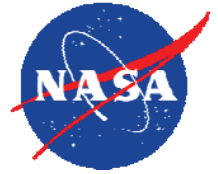
TImOut – Telemetry Output

CASPER - Continuous Activity Scheduling Planning Execution and Replanning system

CFDP - CCSDS File Delivery Protocol

ASIST - Advanced Spacecraft Integration and System Testing Software

Data Processing Chain for Benchmarking



Main Data Source

CHAI v640
on Bussmann
Helicopter

170
Mbps

Ingest/
Level 0

Level
1R

FLAASH
AC

Level
1G

WCPS

Level
2
SAM

Level
2
Vector
izer

Alternative Data Sources

AMS
on Citation
Forest Service

GLiHT on UC-12
Langley

CHAI v640
on UC-12
Langley

EO1 ALI and
Hyperion Data

Radiometric
Correction

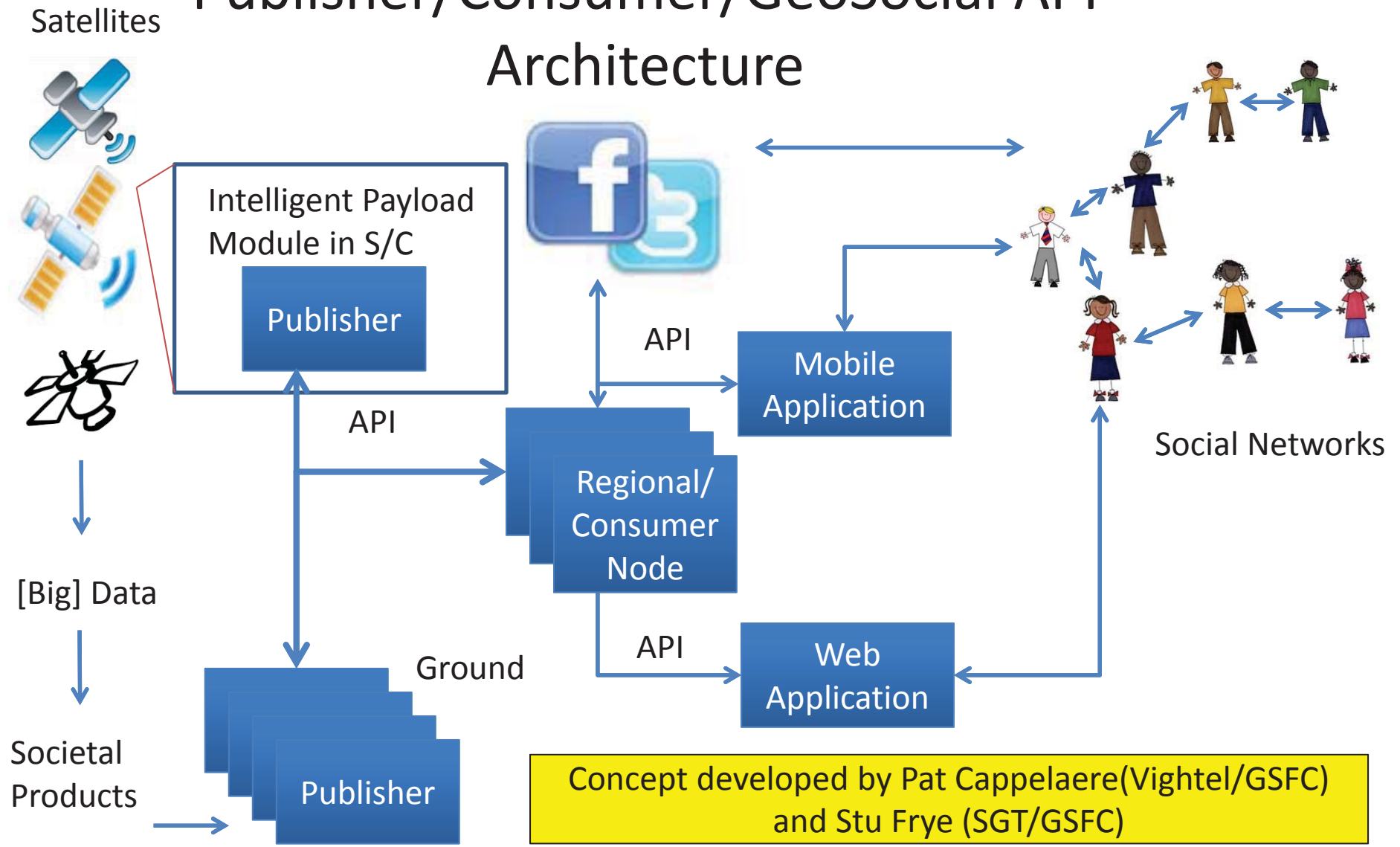
Atmospheric
Correction

Geometric
Correction

Classifiers
& Other
Algorithms

Downlink high level
data products to
ground at 200 kbps

Publisher/Consumer/GeoSocial API Architecture



A methodology to rapidly discover, obtain and distribute satellite data products via social network and open source software

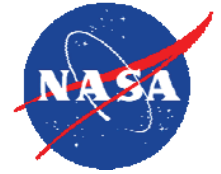
Initial Hyperspectral Image Processing Benchmark

| | Radiometric Correction | *Atmospheric Correction (FLAASH) | Geometric Correction (GCAP) | *WCPS (vis_composite) |
|------------------------------------|------------------------|----------------------------------|-----------------------------|-----------------------|
| 864 MHz TILEPro64 (1 core) | 121.95 | 2477.74 | 183.42 | 72.39 |
| 864 MHz TILEPro64 (49 cores) | 23.83 | TBD | 4.59 | 21.63 |
| 1.2 GHz TILE-Gx36 (1 core) | 57.22 | 897.71 | 28.51 | 19.93 |
| 1.2GHz TILE-Gx36 (36 cores) | 9.21 | TBD | 1.41 | 8.72 |
| 2.2GHz Intel Core I7 | 2.09 | 58.29 | 0.169 | 2.26 |
| Virtex 5 FPGA | TBD | TBD | TBD | TBD |

Image data: GLiHT 1004 x 1028 x 402 (829,818,048 bytes)
 Hyperion 256 x 6702 x 242 (830,404,608 bytes)
 Chai640 696 x 2103 x 283 (828,447,408 bytes)

Notes: Unit is in seconds
 TILEPro64 – No floating point support
 TILE-GX36 – Partial floating point support
 * Indicates time includes file I/O

Detail on Benchmarking of Atmospheric Correction



- Worked with Spectral Sciences to modify FLAASH GLUT version to support airborne atmospheric correction.
- Optimized FLAASH to run on the multicore Tiler processor.
- Processed CHAI v640 data with FLAASH to create reflectance values

FLAASH Parallelization Effort

| | wall | system | user | notes | Parallelized? | Original Walltime | Parallel Speedup |
|----------------------|-------------|------------|-------------|--------------------------------|---------------|-------------------|------------------|
| Surf reflectance | 32.7962 | 5.1398 | 27.6554 | Reflect: RadtoRef | YES | 197.317 | 6.016642679 |
| Cube smoothing | 145.741 | 18.1373 | 127.6037 | mini_cube- >Smooth; FFT | | | |
| Cube reduction | 112.363 | 13.9834 | 98.3796 | >Condense | | | |
| Cube load & distrib | 89.0128 | 11.0775 | 77.9353 | | | | |
| Cube gather & write | 83.2988 | 10.3664 | 72.9324 | | | | |
| Aerosol Retrieval | 52.6236 | 6.54892 | 46.07468 | | | | |
| Water col retrieval | 34.7984 | 4.3306 | 30.4678 | | | | |
| Spectral Polishing | 33.5795 | 4.17891 | 29.40059 | | | | |
| Sensor calibration | 28.5097 | 3.54799 | 24.96171 | | | | |
| Images and Masks | 17.1781 | 2.13779 | 15.04031 | | | | |
| Spectral Resampling | 8.72743 | 1.08611 | 7.64132 | Smile_Resampl er::Cube_Copy | YES | 241.669 | 27.69074057 |
| Cloud Masking | 5.93287 | 0.738336 | 5.194534 | | | | |
| Sensor slit function | 0.764612 | 0.0951547 | 0.6694573 | | | | |
| Modtran Tables | 0.416416 | 0.0518223 | 0.3645937 | | | | |
| un-categorized | 0.0397966 | 0.00495262 | 0.03484398 | | | | |
| Flaash setup | 0.000163794 | 2.04E-05 | 1.43E-04 | | | | |
| total time | 645.7813884 | 81.425006 | 564.3563824 | | | | 1.641422344 |
| total time (h:m:s) | 0:10:46 | 0:01:21 | 0:09:24 | | | | |
| Original Wall time: | 1060 | | | | | | 36 |
| | 0:17:40 | | | | | | |

Using this subroutine which takes about 20% of processing time and is a Fast Fourier Transform to benchmark FPGA acceleration.

FFT Benchmark Tests with Various CPU Processors and FPGA

| Processor | Cores | FFTW 1 band 128 x 256 time (Msec) | Clock rate (Mhz) | Power Consumption (watts) |
|-----------|-------|-----------------------------------|------------------|---------------------------|
| TileGX | 1 | 21.3 | | |
| TileGX | 4 | 10.0 | | |
| Maestro | 1 | 187 | 200 | 14 watts |
| Maestro | 8 | 55 | 200 | 14 watts |
| ZynqARM | 1 | 8.7 | 667 | 3 watts |
| ZynqARM | 2 | 6.9 | 667 | 3 watts |
| XeonPhi | 1 | 9.0 | | |
| XeonPhi | 171 | 0.221 | | 225 watts |
| FPGA | NA | 1.5 | 100 | <3 watts |

Goal

- Experimenting with putting almost all of the data processing chain in FPGA using the Zynq based ZC702 (proxy for CSP) to do the benchmark
- Install ZC702 in IPM and fly on helicopter as part of our flight tests
- Issues
 - Moving data between programmable logic, processor system and memory
 - Design of data processing chain buffering scheme
- Based on DMA access, throughput speed of as much as 10 Gbps might be possible
- Would like to demonstrate producing high level data products while keeping up with an input instrument data rate of between 500 – 1000 Mbps

CHREC Space Processor (CSP) Missions

- CSP Tech Demo ISIM (Space Station)
 - 2 CSP's
 - Targeted to be on Space Station Summer 2015
 - Gary Crum/587
- Compact Radiation BElt Explorer (CeREs) is part of NASA's Low-Cost Access to Space program
 - 3U Cubesat
 - 1 CSP
 - Launch May 2015

Conclusion

- Working towards IPM and GeoSocial API integrated architecture
- Working towards radiation tolerant IPM
- Prototype how much of the flight software and data processing software can be hosted
- Measure relative throughput performance of representative data processing chain
- Present AIST-11 effort is working mostly in multicore processor environment and only begins to explore FPGA performance