Real-Time On-Board Airborne Demonstration of High-Speed On-Board Data Processing for Science Instruments (HOPS)

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ABSTRACT

The project called High-Speed On-Board Data Processing for Science Instruments (HOPS) has been funded by NASA Earth Science Technology Office (ESTO) Advanced Information Systems Technology (AIST) program since April, 2012. The HOPS team recently completed two flight campaigns during the summer of 2014 on two different aircrafts with two different science instruments. The first flight campaign was in July, 2014 based at NASA Langley Research Center (LaRC) in Hampton, VA on the NASA's HU-25 aircraft. The science instrument that flew with HOPS was Active Sensing of CO2 Emissions over Nights, Days, and Seasons (ASCENDS) CarbonHawk Experiment Simulator (ACES) funded by NASA's Instrument Incubator Program (IIP). The second campaign was in August, 2014 based at NASA Armstrong Flight Research Center (AFRC) in Palmdale, CA on the NASA's DC-8 aircraft. HOPS flew with the Multifunctional Fiber Laser Lidar (MFLL) instrument developed by Excelis Inc. The goal of the campaigns was to perform an end-to-end demonstration of the capabilities of the HOPS prototype system (HOPS COTS) while running the most computationally intensive part of the ASCENDS algorithm real-time on-board. The comparison of the two flight campaigns and the results of the functionality tests of the HOPS COTS are presented in this paper.

Keywords: onboard, high speed, HOPS, FPGA, ACES, ASCENDS

1. INTRODUCTION

HOPS is funded by NASA's ESTO AIST program for three years starting April in 2012. The goals of the project are to develop a high-speed on-board reconfigurable and scalable data processing platform for the select National Research Council's decadal survey science missions [1] such as ASCENDS [2-9] and 3-D Winds [10-12]. The HOPS maturation is scheduled for April, 2015, and this paper presents the results of two flight campaigns conducted in 2014. The entry and the exit Technology Readiness Level (TRL) of HOPS are two and five, respectively. All the components of HOPS are space-borne flight-ready equivalent (path-to-flight) and the board layout likewise seeks to minimize the risk associated with transitioning to a space-borne platform. HOPS is an enabler for science missions to perform real-time data processing by offering extremely high data processing rate [13-15]. The FPGA and memory bandwidth of HOPS is approaching 16 GB/sec and the inter-board communication bandwidth is approaching 4 GB/sec. The plug-N-play VHDL IP cores of HOPS provide the easy and efficient implementation of data processing algorithms with a quick turn-around time. The basic requirements to support high-speed on-board data processing are: (1) high speed computation element(s), (2) sufficient memory to hold intermediate computed values, and (3) sufficient bandwidth between the computation element and memory. Current space grade general purpose processors (GPPs) [16] and digital signal processors (DSPs) [17] do not meet all three requirements. There are multi-core general purpose and DSP processors [18] in the works which could meet requirement (1), but requirements (2) and (3) have not been met. With the

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availability of rad-hardened reprogrammable FPGAs, however, it is now feasible to develop a high-speed on-board data processing system for science instruments that meets all three requirements, and high speed computation element(s) can be implemented in reconfigurable FPGAs [19-21]. FPGAs can be augmented with a high-speed on-board memory to address requirement (2) [22-24]. Furthermore, requirement (3) can be addressed with high-rate memories and a wide data bus architecture between the FPGA and the on-board memories. Lastly, FPGAs support high-speed serialized input/output allowing scalability. Section 2 discusses the design of HOPS from concept to flight, and Section 3 reports the outcome of the two flight campaigns. The current status of HOPS is presented in Section 4, followed by the conclusion.

2. CONCEPT TO FLIGHT

HOPS employs space-borne flight-equivalent parts in its design, allowing risk reduction in advancement to TRL 6. Several iterations of computing architecture supporting ASCENDS data processing were prototyped in SystemC during the first year of development. Preliminary HOPS hardware requirements were defined and the performance of ASCENDS data processing on HOPS was estimated during that period. Based on the analysis results in SystemC, a prototype (HOPS COTS) was built using commercial-off-the-shelf (COTS) components during the second project year. The system flew twice during the summer of 2014 to test its end-to-end capabilities. All the lessons learned from the campaigns are applied to the design and the demonstration of the final custom board called HOPS hardware (HOPS HW). HOPS is a three-year project and the future work post HOPS is called radiation-tolerant (RT) HOPS for space flights. HOPS seeks to minimize the risk associated with transitioning to RT-HOPS and therefore HOPS HW mimics the functional capabilities and layout of the anticipated RT-HOPS board through informed component selection and floor-planning. Since all the components of HOPS HW are path-to-flight, the construction of RT-HOPS will be at minimal risk and cost effective. Figure 1 illustrates the evolution of HOPS and its concept to flight path to RT-HOPS.
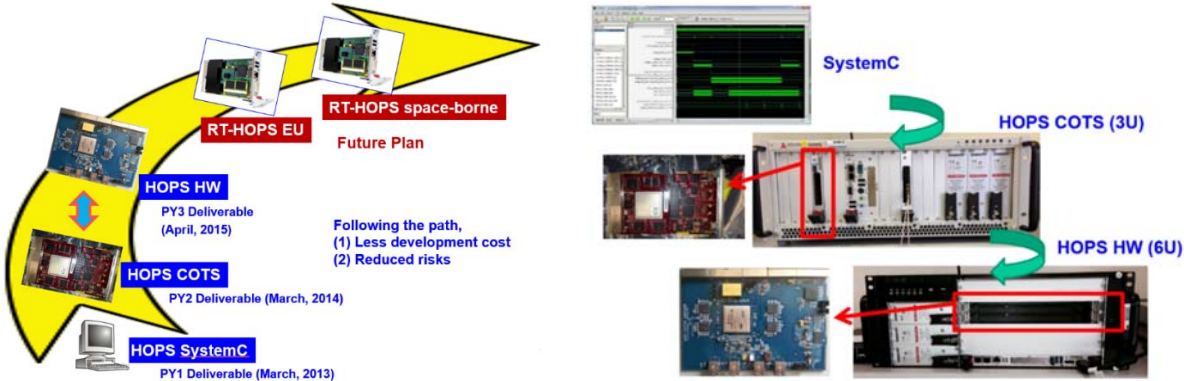

Figure 1   Concept-to-flight of HOPS and RT-HOPS.

3. FLIGHT CAMPAIGN WITH ACES AND ASCENDS

Figure 2   HOPS team during the Integration and Testing (IT) at AFRC

Figure 2 shows the photos of HOPS engineers at AFRC during the flight campaign in Palmdale, CA. The HOPS system that flew in 2014 is 3U-based, and consists of HOPS COTS and a COTS 14-bit digitizer. In order to demonstrate the end-to-end capabilities of HOPS, a sample C/C++ code was written to perform real-time data acquisition and processing running the ASCENDS algorithm. The system is quasi-autonomous and the majority of the data was acquired without an operator aboard.

HOPS Flight Campaigns	Campaign 1	Campaign 2
Location	LaRC in Hampton, VA	AFRC in Palmdale, CA
Aircraft	HU-25	DC-8
Period	July 1st – 16th, 2014	July 27th – August 22nd, 2014
Real-Time On-Board Data Rate	4 million samples per second. 14-bit fixed point per sample.	
Algorithm	ASCENDS	
Flight Hours	11.7 hours	11 hours
Data Hours	20:43:34	14:58:34
Science Team	ACES (ESTO IIP)	Exelis Inc. (ESTO ACT)

Table 1   Logistics of HOPS flight campaigns in 2014.

Table 1 compares the logistics of the two flight campaigns. The first campaign was held during the first half of July based at LaRC and the HOPS system flew with the LIDAR instruments for ACES. The second campaign was based at AFRC in Palmdale, CA on the larger aircraft DC-8. The HOPS system tapped off of the LIDAR's raw data stream and preformed real-time data processing independently of the science instruments during the flight. The two campaigns serve as an end-to-end demonstration of the final deliverable HOPS HW since the operations and the functionalities of HOPS COTS are a subset of HOPS HW. The performance of HOPS HW will be far better than the HOPS COTS prototype, which will be demonstrated as part of the final deliverables.

Campaign 1 Goals	Campaign 2 Goals
1. Learn from a small aircraft campaign to prepare for the DC-8 campaign. 2. Check the integration of HOPS COTS in a 3U cPCI system with a COTS digitizer. 3. Check HOPS COTS functionality. 4. Check the integration of HOPS into a project and identify any issues such as cabling, boot-up sequence, power management, data archive, and HOPS system monitoring. 5. Test the sample code that utilizes HOPS COTS with a digitizer. 6. End-to-end demonstration.	Goals in campaign 1 plus 1. Apply lessons from Campaign 1 to the larger platform DC-8. 2. Check the heat dissipation of FPGA on the DC-8 during the campaign. 3. Check integration issues with a larger platform in general. 4. End-to-end demonstration.

Table 2   Goals of the two 2014 HOPS flight campaigns

Table 2 shows the list of goals in each campaign. The end-to-end airborne demonstration allows the HOPS team to be able to prepare HOPS HW for its seamless integration into the target science missions. Based on the lessons learned from the two campaigns, an integration plan has been devised so that the HOPS HW can be incorporated into the science mission data acquisition and processing system easily. Also, by-products from the campaigns such as a sample C/C++ program for real-time data distribution and archive and the know-hows in cabling and interface design will be valuable resources for science missions to adopt the HOPS HW into their system. At the end of each flight campaign, the accuracy of the algorithm was analyzed and the validation of the functionalities of the IP Core was performed. All the science data products met the required accuracy tolerance in those analyses, and the goals of each campaign were

accomplished.

4. STATUS QUO

The first bare-board of HOPS HW was built and tested for its basic electrical functionalities in August, 2014. It was populated upon the completion of basic electrical testing, and the major electrical and functional testing was performed on the resulting assembly board. A few issues were identified such as the difficulty of rewiring cabling used with the board and opportunities to further increase memory operating speed, and proper modifications were made to address these on the revised design and more bare-boards were ordered in December, 2014. After the basic electrical testing on the second bare-board, the second assembly board was made in January, 2015. A bit error problem was identified with a single data line on the DDR2 memory. The source of the problem was discovered to be damage to the DDR2 memory incurred during assembly due to solder lodged in a vertical trace which runs outside the component package. Testing revealed that a short circuit was not present between vertical traces and therefore it is currently believed that the solder transferred thermal energy inside the package damaging this single data line's connection with the vertical trace. Mitigations were discussed with both the component manufacturer and the assembly vendor and it was decided that a protective cap would be used to cover the vertical traces on the component during future assemblies. No electrical modification was necessary with the revised design. The third bare-board was ordered and received in February, 2015. After conducting a basic electrical testing on it, the third assembly board will be ordered in March, 2015. Upon its delivery in early March, 2015, the main electrical and functional testing will be performed to verify the correct operation of the board and the HOPS team will confirm the successful mitigation of the assembly problem previously encountered. Once this is confirmed, three additional assembly boards will be ordered and a total of four final HOPS custom boards will be delivered as final deliverables. Figure 3 shows an HOPS custom board (HOPS HW) during the electrical and functional testing.
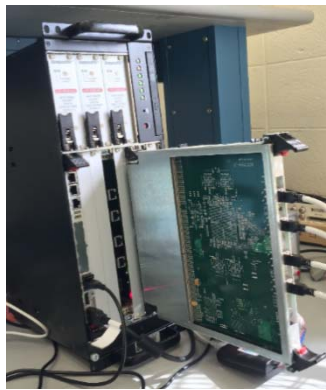

Figure 3   HOPS custom board (HOPS HW) in testing.

5. CONCLUSION

The three design phases of HOPS have been successful and the final HOPS HW is evolving to its maturity without any significant schedule delays. The seamless and user-friendly integration of HOPS HW into ASCENDS is the top priority of the project at the end of the project year, and an integration plan has been devised accordingly. The design principle of HOPS is to enable science missions that require extremely high data rate in general, and the final deliverable packages will contain documentations and resources that meet such a goal. The proof of re-configurability and scalability of HOPS HW is also part of the final deliverables, which are one of the unique features of HOPS HW. The two flight campaigns during the summer of 2014 were completed successfully in every aspect. The science data products met the required accuracy tolerance and the functionalities of the FPGA IP Core were verified and validated. The integration of the HOPS system using HOPS COTS into the science instruments for ACES and ASCENDS was successful, and all the integration and testing plans were executed without any issue. The HOPS system was quasi-autonomous and it operated without an operator once the system had started on the ground. All the lessons learned from the two flight campaigns will be incorporated into the completion of HOPS HW and the future planning of a space-borne version RT-HOPS. The

HOPS project is scheduled to complete in early 2015.

ACKNOWLEDGMENT

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