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Architecture, Voltage, and Components for a Turboelectric Distributed Propulsion Electric Grid

Final Report

Michael J. Armstrong and Mark Blackwelder
Rolls-Royce North American Technologies, Inc. (LibertyWorks), Indianapolis, Indiana

Andrew Bollman and Christine Ross
Rolls-Royce Corporation, Indianapolis, Indiana

Angela Campbell
Georgia Institute of Technology, Atlanta, Georgia

Catherine Jones and Patrick Norman
University of Strathclyde, Glasgow, Scotland, United Kingdom

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University of Strathclyde, Glasgow, Scotland, United Kingdom

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Michael J. Armstrong and Mark Blackwelder
Rolls-Royce North American Technologies, Inc. (LibertyWorks)
Indianapolis, Indiana 46207

Andrew Bollman and Christine Ross
Rolls-Royce Corporation
Indianapolis, Indiana 46206

Angela Campbell
Georgia Institute of Technology
Atlanta, Georgia 30332

Catherine Jones and Patrick Norman
University of Strathclyde
Glasgow, Scotland, G1 1XQ, United Kingdom

1.0 Introduction

1.1 TeDP Electrical System

The development of a wholly superconducting turboelectric distributed propulsion system presents unique opportunities for the aerospace industry. However, this transition from normally conducting systems to superconducting systems significantly increases the equipment complexity necessary to manage the electrical power systems. Due to the low technology readiness level (TRL) nature of all components and systems, current Turboelectric Distributed Propulsion (TeDP) technology developments are driven by an ambiguous set of system-level electrical integration standards for an airborne microgrid system (Figure 1).

While multiple decades' worth of advancements are still required for concept realization, current system-level studies are necessary to focus the technology development, target specific technological shortcomings, and enable accurate prediction of concept feasibility and viability. An understanding of the performance sensitivity to operating voltages and an early definition of advantageous voltage regulation standards for unconventional airborne microgrids will allow for more accurate targeting of technology development.

Propulsive power-rated microgrid systems necessitate the introduction of new aircraft distribution system voltage standards. All protection, distribution, control, power conversion, generation, and cryocooling equipment are affected by voltage regulation standards. Information on the desired operating voltage and voltage regulation is required to determine nominal and maximum currents for sizing distribution and fault isolation equipment, developing machine topologies and machine controls, and the physical attributes of all component shielding and insulation. Voltage impacts many components and system performance.

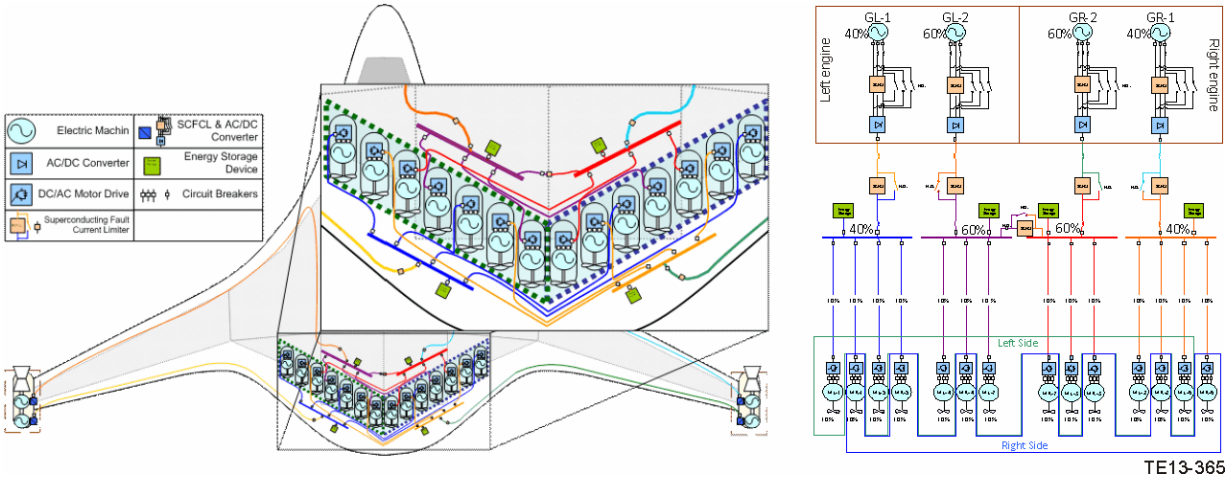

Figure 1.—Rolls-Royce TeDP System Architecture Concept.

Issues that must be considered for higher voltage operation are the following:

- Maximum and steady-state current ratings
- Fault current interruption for fault isolation and protection
- Partial discharge and corona protection
- Dielectric insulation life
- Safety procedures for testing, manufacturing, and maintenance

To assess the feasibility of unconventional airborne N+2/3 microgrid concepts more accurately, tools and processes are necessary to estimate and govern the development of appropriate voltage regulation standards for these unconventional concepts. An integrated system-level process for identifying the desired voltage standards would allow for more accurate prediction of electrical system weight and volumes, overall system reliability, and safety of technology concept. This influences the vehicle-level feasibilities assessments, highlighting technology gaps where increased development is needed (protection equipment). Once advantageous sets of standards are identified, these standards can be used to assist in informing electrical technology development relating to expected systems interactions and operational constraints.

A holistic approach to defining the appropriate standards is necessary to guide future technology developments. Most current superconducting technology developments are subject to constraints imposed by interfacing with normally conducting terrestrial systems. However, because the NASA N3-X microgrid is wholly superconducting, many of the driving connection constraints are removed, and the operating standards for a wholly superconducting system can be tailored to capture maximum benefit to the entire system. Additionally, because this system must be airworthy and flight critical, operating standards must be defined that lend specifically to aircraft environmental, safety, and performance objectives.

1.2 A Review of Current Voltage Standards

Terrestrial systems have adopted multi-kilovolt (kV) standards for electrical power distribution. However, the aerospace community typically operates well under the kV level. The highest accepted power distribution voltage for conventional transport aircraft is ±270 Vdc. These common voltage practices reflect the current aircraft electrical power systems paradigm. While increased voltages would

act to reduce conductor weight and volume, insufficiently understood risks associated with insulation and protection equipment prohibit the introduction of higher voltage standards.

Voltage levels on existing electrical systems for aircraft are relatively low. As power demands increases on a conventional system, it is necessary to increase voltage levels so that conductor weight can be reduced. Increasing the voltage level allows the conductor current to decrease for the same power requirement. Reduced conductor current rating also reduces conductor weight. However, higher voltage levels require thicker insulation, which contributes to an increase in cable weight.

The primary motivation for current limitation on voltage for airborne power system is derived from Paschen's Law (Figure 2) (Ref. 1). This law considers parallel metal plated in air under a uniform electric field. Figure 2 charts the voltage breakdown of an airgap in terms of the product of the distance between conductors and pressure. The approximate minimum breakdown voltage for any product of pressure and distance is 327 Vdc. This means an arc will not occur between two parallel metal plates at voltage levels below this value at low or high altitude. For this reason, existing aircraft dc voltages remain below the 327-Vdc threshold.

The superconducting cables and physical layout of the electrical system must consider Paschen's Law to avoid breakdown and discharge especially at high altitude by designing cable insulation and distance between conducting elements appropriately. In addition to the composition of the airgap, pressure, and conductor distance, the breakdown threshold voltage is also a function of temperature. For lower temperatures, which increase the air density, the strength of the gap is increased since increase in air density translates to a larger pressure-distance product. Since this electrical system is cryogenic, the breakdown voltage may be less sensitive to pressure and conductor distance than the room-temperature curve for which Paschen's Law is characterized. Other factors that should be considered when determining system voltage levels are contamination in the air gap, impact of vibration, abnormal system events, and transient events (Ref. 2).

Conventional wisdom indicates that increased power levels demand higher voltages to reduce operating current and thus reduce the conductor size and weight. However, in the context of a wholly superconducting microgrid system, overall system weight becomes largely insensitive to increases in conductor cross-sectional area. Superconducting components have acceptable power density with lower-voltage higher-current levels. An additional challenge arises, however, for large current systems at lower voltages. In this case, large operating currents require larger interruption devices for protection and control purposes.

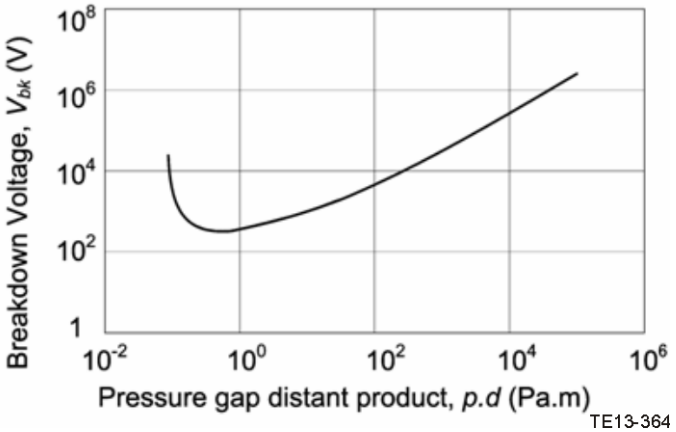

Figure 2.—Illustration of Paschen's Law (Ref. 1).

Extrapolations from terrestrial superconducting standards provide a limited basis for comparison due to typical fundamental assumptions applied. Current implementations of superconducting equipment are developed and integrated in a piecemeal fashion. Sections of superconducting cabling or machine equipment are coupled with normally conductive systems for specific targeted benefits. In these cases, the weight, size, or cost of a normally conductive component becomes prohibitive and benefits to the insertion of the superconducting component warrants insertion into the more conventional system. As such, the operating requirements for the superconducting component are fixed by the bounding systems elements or defined by considering the single component's performance sensitivity in isolation.

1.2.1 Grid Codes

Voltage standards that apply to the utilities industry vary according to country and region. Two areas reviewed here are the North American market and the European market. The North American grid is stiff but is starting to develop standards for the connection of small, distributed generation to the larger power system. The European market is more dynamic and the standards take into account the integration of disruptive power sources such as photovoltaic (PV) systems. The utilities' standards normally assume that the power on the grid is shared by multiple generators. While this sharing of power on a common grid is dissimilar to the TeDP project, some trends are worth noting.

1.2.1.1 European Standards

The British Standards Institute (BSI) released requirements for voltage regulation and parallel operation of AC machines (Ref. 3). BS 4999-140 covers generators running in parallel and running singly. This standard is unique as it uses a percent of rated current to define load changes rather than rated power and faulted conditions are not covered in the standard. The standard defines nine regulation grades that a generator can be specified to depending on the application and agreement between manufacturer and purchaser. Permissible steady-state voltage regulation, transient voltage droop, and recovery times are given for each regulation grade. The amount of load acceptance can vary from 35 to 100 percent of rated current, at rated voltage, and at a power factor between 0.4 and 0 lagging. For load shed events, the amount of allowable for voltage droop is given for 100 percent load shed events assuming a 0.8 power factor.

The bulk European energy market is not an open market between countries, so while the International Electrotechnical Commission (IEC) provides some overarching regulations, such as standard voltages (Ref. 4), individual countries impose additional regulations on their utility companies. It is also worth noting that because of this fragmentation, the European electric grid is not as "stiff" as the North American grid, so it may provide better insight on how disruptive technologies (wind, photovoltaic penetration) impact system regulation. In the Finnish specifications for power plant performance (Ref. 5), the nominal voltage in the main grid can drop to as low as 0.85 pu and up to 1.05 pu during disturbances, while the nominal voltage is within 0.95 and 1.05 pu. Unlike aircraft standards, the voltage and frequency regulations are dependent on each other as Figure 3 indicates. Generators may remain synchronized to the grid as long as they do not suffer damage if the frequency is below 47.5 Hz or above 53 Hz. Generators must be disconnected if the frequency is above 55 Hz.

For disturbances and exceptional conditions, the generating units are designed to withstand the suggested grid voltage variations shown in Figure 4 without disconnection from the grid and only a small power reduction is accepted.

The Finnish grid code further states the preference to have generators with low reactances and also specifies the amount of forcing the exciter is expected to have so that generator can ride through transient conditions. Each generator is capable of operating at the rated active power continuously with a power factor down to at least 0.95 underexcited and 0.9 overexcited, throughout the voltage rant of 100 to 105 percent on

the underexcited condition and 90 to 105 percent on the overexcited condition. The voltage control system includes a power system stabilizer (PSS), protective limiters and reactive current statics equipment.

A second example of voltage control is the new German grid codes for connecting photovoltaic systems to medium voltage power grids in accordance with DIN EN 50160 – "Voltage Characteristics of electricity supplied by public distribution networks" (Refs. 6 and 7). This is relevant as the grid considers power connected to the grid through converters.

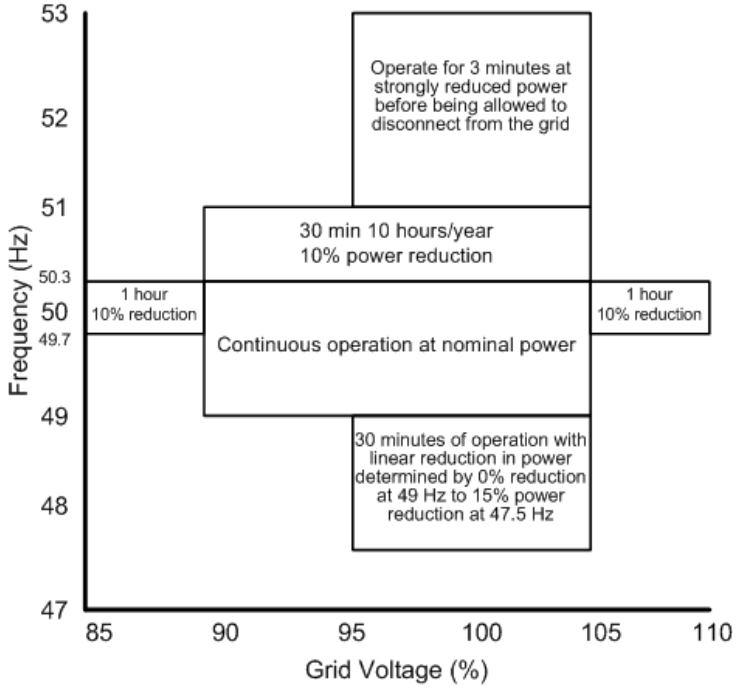

Figure 3.—Finnish Grid Requirements concerning Power Production When the Grid Frequency and Voltage Vary.

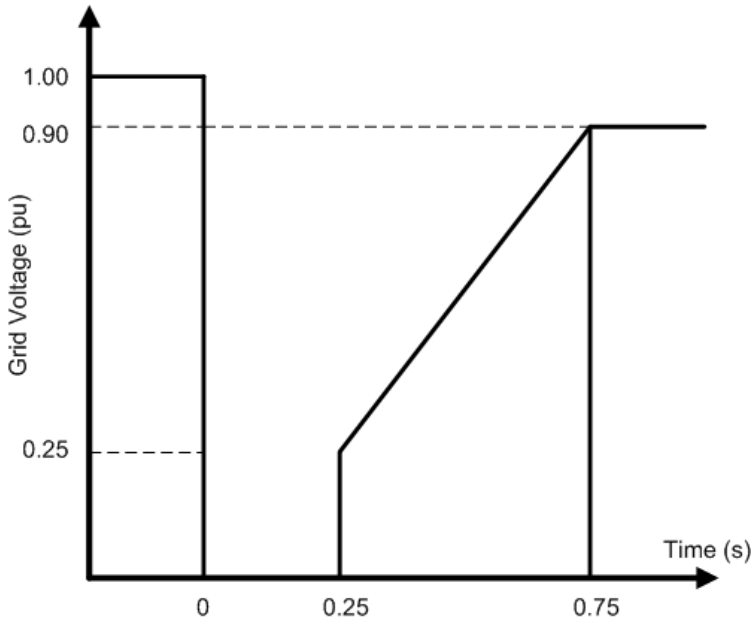

Figure 4.—Grid Voltage Transient Caused by a Fault.

Figure 5 shows the limiting curves during a fault for plants connected to the grid that do not use a synchronous generator. It can be seen that the power plant must remain tied to the grid during a voltage drop down to 0 V for up to 150 ms. If voltage is above boundary line 1, then the unit has to remain connected to the grid. If the voltage is between boundary line 1 and boundary two, the behavior of the system can vary based upon agreement between network operator and plant operations. Between boundary line 2 and the blue line, disconnect times greater than 2 s are allowed to protect generation equipment subject to agreement with the network operator.

In the event of a network symmetrical fault that results in weakened voltage, the power facility must manage the import and export of reactive power to prevent a full voltage collapse. Figure 6 shows the voltage response during a symmetrical fault so that the generator injects reactive current onto the network. The generating units must be capable of feeding the required reactive current into the grid within 20 ms of the fault, up to 100 percent of the rated current. The German standard also contains a power reduction formula similar to the Finnish grid study above that helps to protect the equipment from unsafe system operation.

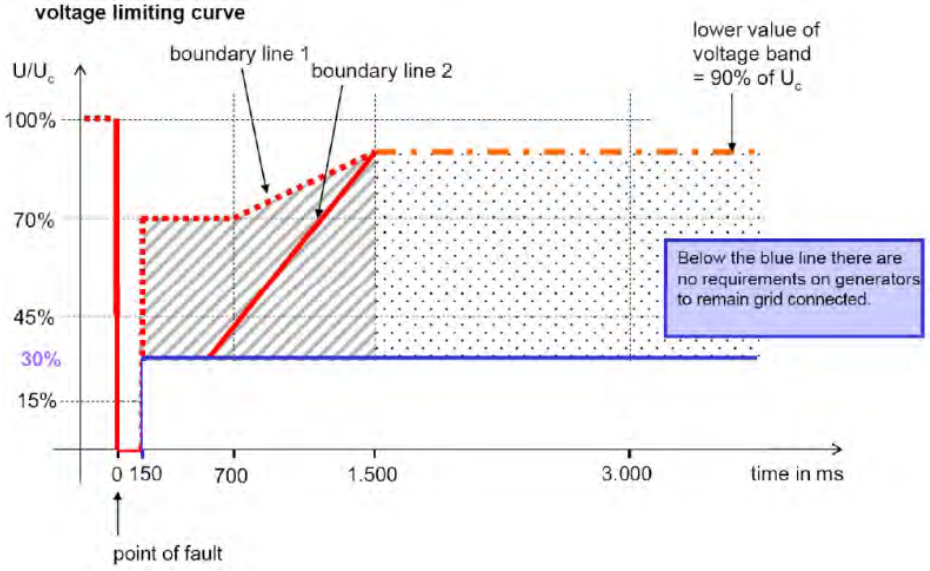

Figure 5.—Limiting Voltage Curves at the Grid Connection Point in the Event of a Network Fault.

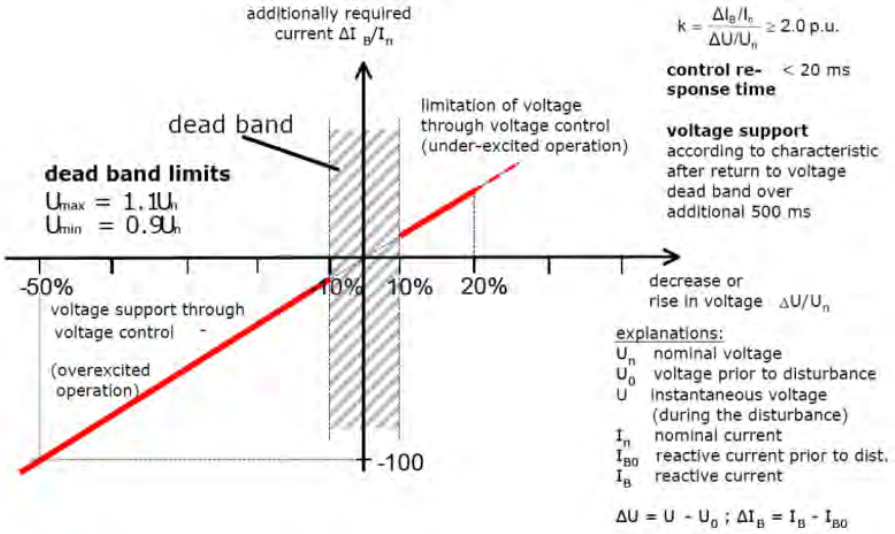

Figure 6.—Principle of Voltage Support in the Event of a Symmetrical Network Fault.

1.2.1.2 North American Standards

There are numerous standards that cover the electric grid in the United States, from the federal regulations of the North American Electric Reliability Corporation (NERC) to the regional Independent Service Operators (ISO) to the industry standards of IEEE 1547 and ANSI C84. There are standards that cover the generation, transmission, distribution and consumption of electrical energy based on a generator's size, its location and if it is participating in the wholesale energy market. This review only covers a very small section of the standards.

The NERC ensures the reliability of the bulk power system in North America. The standard NERC-PRC-024 relates to the frequency and voltage protective settings of generators and ensures that generators remain connected during defined frequency and voltage excursions. PRC-024 defines the voltage during a fault at the Point of Interconnection (POI). Transmission connection systems (large utilities) have a set of different requirements than DER including voltage tolerance in accordance with NERC PRC-024 and allow the voltage at the source to be controlled on voltage, power factor or reactive power.

IEEE 1547 is the standard for interconnecting Distributed Energy Resources (DERs) with electric power systems. Table 1 shows the voltage and frequency variations allowed by IEEE 1547. The standards cover the interconnection of DER by imposing requirements on certain voltage characteristics (Ref. 8). Voltage regulation is to be within ±5 percent per ANSI C84, voltage control of DER is not permitted per IEEE 1547, the distortion of the waveform is controlled by individual harmonics, and the IEEE 1547 requires that the direct current injection in the grid be less than 0.5 percent of the full rated RMS output current.

Figure 7 superimposes the transient voltage curves of both the transmission system (NERC PRC-024) and the distributed system (IEEE 1547). The curves look similar to the European fault voltage curves as well as the voltage envelopes of MIL-STND-704. This does not dictate the voltages of the system or the voltage at the load but regulates voltage at the point of connecting an electrical source to the grid.

TABLE 1.—STANDARDS FOR INTERCONNECTING DISTRIBUTED RESOURCES WITH ELECTRICAL POWER

Voltage range, % nominal	[a] Maximum clearing time, s
V < 50%	0.16
50% ≤ V < 88%	2.0
110% < V < 120%	1.0
V ≥ 120%	0.16

[a] Maximum clearing times for DER ≤ 20 kW; Default clearing times for DER > 30 kW

Frequency range, Hz	Maximum clearing time, s
f > 60.5	0.16
[b] f < 57.0	0.16
[c] 59.8 < f < 57.0	Adjustable (0.16 and 300)

[b] 59.3 Hz if DER ≤ 30 kW

[c] For DER > 30 kW

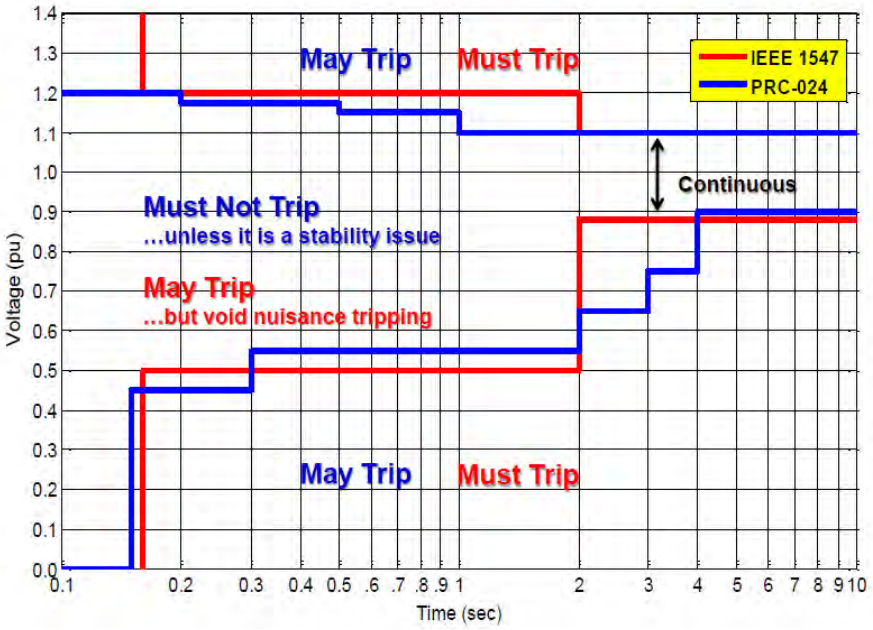

Figure 7.—IEEE 1547 versus NERC PRC-024 (Ref. 9).

1.2.2 Maritime Power Systems

1.2.2.1 Current Regulations

Modern maritime vessels are advancing power management systems in several areas that are of interest to TeDP architecture. Both the shipping industry and TeDP are looking at taking advantages of electric propulsion to save energy while investigating different energy storage techniques to power critical loads. Some shipping applications resemble a power grid made up of isolated power generators driving primarily inductive loads such as the pumping motors on a Floating Production Storage and Offloading ship. The shipping industry can provide some insight in isolated microgrids and is already regulated by several societies, including the American Bureau of Shipping (ABS), Det Norske Veritas (DNV), and Lloyd's Register. The regulatory bodies have not created standards for a maritime DC power system for reasons that will be covered in a later section, though progress is being made in that area.

While MIL-STND-704 guarantees the power quality at the input of utilization equipment, the ABS rules for Steel Vessels and for Mobile Offshore Drilling Units (MODU) govern every aspect of the power system. The ABS rules govern the response of generators for a given load change with the worst case specified or agreed upon by purchaser and manufacturer. As fault scenarios and power flow (load flow) solutions depend on the transmission and distribution networks as well as the generators and loads, the power system designer must gather and analyze the entire system to ensure that the ABS regulations will be met. A significant difference between the military standard and the maritime standards is that the shipping standards assume generators share a common bus.

The voltage level on shipping vessels typically varies between 460 V and 15 kV, depending on the load application. The lower voltage is used for auxiliary loads such as lighting, communication equipment and similar equipment. The higher voltages are used for winches, pumping motors and other large inductive loads, connected either directly on-line or through large motor controllers. The ABS specifies that the generator voltage is to be within ±2.5 percent of rated voltage for all loads between zero and the load at rated power factor. For emergency generators, that limit is increased to ±3.5 percent. Generator

transient voltage variations are required to be within the range of –15 to 20 percent of the rated voltage given the following load change events:

- A load equal to the starting current of the largest motor or a group of motors, but in any case, at least 60 percent of the rated current of the generator, and power factor of 0.4 lagging or less, is suddenly thrown on with the generator running at no load
- A load equal to the above is suddenly thrown off

The voltage must be restored within ±3 percent of the rated voltage in less than 1.5 s for both load acceptance and load shed scenarios. From the above conditions, the ABS considers the maximum load change, the load inductance, recovery time and recovery limits during transients when regulating voltage.

The ABS does state what voltage fluctuations will be at the electrical equipment supplied by the generators. The electrical loads should operate with a permanent voltage variation of 6 and –10 percent with a transient variation of ±20 percent with a recovery time of 1.5 s. The difference between allowable voltage variations between the generator and distribution system illustrates that the ABS considers how much voltage drop and dynamic response the connecting equipment can have the electrical system. The voltage continuous variation in DC distribution systems can be ±10 percent. The DC system can have a voltage cyclic variation deviation of 5 percent and a voltage ripple of 10 percent. The DC variations include systems supplied by rectifiers. As the rectifier output is ±10 percent but the AC generator can be –15 to 20 percent, it can be assumed that the ABS expects the rectifier to provide dampening to DC system transients.

The ABS also defines the power sharing between generators since the generators are on a single bus. The reactive power requirements are of interest as reactive power sharing is typically driven by voltage control. The ABS defines the amount of allowable difference in reactive power generation between sources and this may need to be considered in the TeDP architecture as the SMES and a generator may both inject power into the same bus during a disturbance or fault.

Energy storage that is used as emergency power on ships is typically provided with batteries. The ABS directs that where energy storage is the sole means of supplying DC power equipment for essential services, failure of the charging equipment cannot result in the total loss of the energy storage services. The energy storage should be capable of automatically connecting to the emergency switchboard in the event of a failure to the main source of electrical power while immediately supplying power to critical services and carrying the emergency electrical load without recharging while maintaining the voltage of the energy storage within 12 percent of nominal voltage throughout the discharge cycle.

The ABS rules also cover frequency, earthing, and protection requirements that may be of interest to the TeDP architecture but not directly related to the voltage study. The ABS provides the required voltage level for insulation testing on electric machines that are similar to some tests in MIL-HDBK-704. The TeDP standard development may want to develop new standards for superconducting machines and cables as the superconducting TeDP system will provide novel fault and degradation conditions.

The Institute of Electrical and Electronic Engineer (IEEE) has developed a recommended practice for 1 to 35 kV Medium-Voltage DC (MVDC) power systems on ships (IEEE Std 1709) and a recommended practice for electrical installations on shipboard (IEEE Std 45). The IEEE states that the common ratings of the MVDC power systems, including their operating devices and auxiliary equipment, should be selected from the following:

- Rated maximum voltage
- Rated withstand voltages
- Rated continuous current
- Rated short-time withstand current
- Rated duration of short circuit

The IEEE goes on to state that the voltage should be determined by the desired generator voltage, propulsion motor voltage, converter design, load considerations, standard cable ratings, efficiency, and arc fault energy. The continuous DC voltage tolerances should be selected considering the normal loads and insulation breakdown. The rated withstand voltage is different for the system than for the power electronics (the power electronics are detailed in IEEE Std 1662). The choice of withstand voltage allows for different voltage performance criteria or overvoltage patters and should be made considering the degree of exposure to lightning and switching surge overvoltages, the neutral grounding of the system, and the overvoltage limiting devices. Grounding is essential for the MVDC system as the lack of a reference point will allow for the presence of leakage currents that may cause an unpredictable DC offset.

IEEE Std 1709 also addresses the stability of the MVDC system by making it clear that the designer is required to describe what is meant by stability. To assist, the IEEE defines the following criteria:

1) Time domain criteria exist
    a) Transient recovery time
    b) Bounded transients (percent of maximum variation)
    c) Absence of limit cycle behavior
2) Frequency domain criteria exist
    a) For example, 6 dB per 30° margins
    b) Frequency domain techniques using a time domain model

A description of possible stability studies is also provided, some of which have been started by developing the dynamic models of the system. In addition to the time-domain analysis of the dynamic models, frequency domain analysis and impedance characterization will be crucial in developing a stable MVDC power system. The Quality of Service (QoS) is another factor considered in the MVDC power system of ships. The QoS is the metric of how reliably the power system provides power to the loads. To do this, the loads must be categorized as un-interruptible, short-term interrupt, long-term interrupt, and exempt.

The power quality may be described in part by the voltage waveform. IEEE Std 45 specifies the harmonic distortion allowed on the system and on the electric propulsion system, setting limits for both total and individual harmonics. IEEE Std 1709 addresses the quality of power on the MVDC bus through voltage ripple and voltage tolerance. It sets the limit on the acceptable RMS value of ripple and noise to be less than 5 percent per unit. Also, the following parameters should be defined:

- Maximum non-repetitive peak
- Maximum repetitive peak
- Maximum repetitive peak-to-peak

Finally, it is prudent to note that safety is critical when designing the MVDC power system. There are no known international guidelines for safety of operation of MVDC power systems above 3 kV. However, IEEE Std 1628 and MIL-HDBK-1025/10 include safety recommendations that can be applied to a MVDC system. DC arc fault currents will be significant and models that identify the location and severity of arc flash hazard should be developed. The risk of corona discharge is increased with higher voltage and higher current levels, and prevention methods will be necessary. The IEEE recommends the disconnection and discharge of all power storage devices, in part to reduce the risk of electric shock to personnel and equipment.

1.2.3 Current Aircraft Voltage Standards

The standard that establishes and governs the power interface between military aircraft and aircraft utilization equipment is MIL-STD-704. The standard regulates voltage levels, frequency, phase, power factor, ripple, electrical noise and abnormal conditions for both AC and DC systems that will be available at the input terminals of utilization equipment. Electromagnetic Interference (EMI) is not covered by this standard and the document does not go into the quality of power generated, transmitted or distributed; it is up to the aircraft manufacturer to determine the requirements of the power system to guarantee the power levels set forth in MIL-STD-704. MIL-HDBK-704 defines test methods and procedures for determining airborne utilization equipment compliance with the electric power characteristics requirements.

AC power is required to be single-phase or three-phase with a wire-connected grounded neutral system. While a 400 Hz, fixed-voltage scheme is typical, the standard allows variable frequency and double voltage equipment. Variable frequency systems may have frequencies between 360 to 800 Hz with a nominal voltage of 115/200 V while double-voltage systems may have nominal voltages of 240/400 V with a nominal frequency of 400 Hz. It is noted that the system is not allowed to be variable frequency and dual voltage. The phase sequence and markings are specified in the standard as well. The AC system is regulated using the following characteristics and are defined for both normal and abnormal conditions:

- Steady-state voltage
- Voltage unbalance
- Voltage modulation
- Voltage phase difference
- Distortion factor
- Distortion spectrum
- Crest factor
- DC component
- Steady-state frequency
- Frequency modulation
- Transient peak voltage
- Voltage transient envelope
- Frequency transient envelope
- Voltage and frequency recovery times
- Power factor

The MIL-STND allows for a two-wire or negative ground return DC system having a nominal voltage of 28 or 270 V. The RTAPS TeDP system assumes a three-wire, bipolar system with negative return. The following characteristics are defined to govern the operation of a DC system:

- Steady-state voltage
- Distortion factor
- Distortion spectrum
- Ripple amplitude
- Transient voltage
- Voltage and frequency recovery times

In both AC and DC systems, it is assumed the protection equipment will keep the voltage within the operating limits.

MIL-STND-704 contains several requirements that are paramount to the reliability and safety of an airborne electrical system. One requirement is that protective devices operate independently of control and regulation. While prudent in a traditional system, this requirement may not be feasible in a DC electrical propulsion system as the power electronics in the converters may be used to regulate voltage as well as for protection. Indeed a novel DC electrical system may upend the traditional protection scheme, removing traditional circuit breakers and relying on fault current limiters and converters for both power regulation and protection. The protection and regulation circuits could still use independent instrumentation.

The military standard does highlight several areas that should be considered when developing a TeDP electrical system. The bonding of all AC devices should be carefully considered to allow for any system unbalance.

1.3 Challenging in Creating DC Propulsion Standards

The marine industry is in the process of exploring DC propulsion systems with several navies funding research into the dc power system architecture, protection and energy storage. At this time, these regulatory societies have not released standards for a maritime DC power system. The ABS society includes some rules on DC propulsion (Ref. 10) and the IEC has several standards (Ref. 11) that include requirements for DC systems but there currently is no path in getting a full DC electrical system on a maritime vessel approved by any regulatory body The lack of standards has not stopped research into the areas and in fact may allow companies to explore the entire design space of DC systems by not constraining solutions by over-burdensome regulation. ABB delivered the Dina Star in 2013 that utilizes an onboard DC grid that creates a flexible marine power and propulsion system (Ref. 12). Perhaps by being the first to market and having the opportunity to prove their design, ABB was granted approval in principle for the Onboard DC Grid concept by ABS in January 2014 (Ref. 13). This will allow ABS to review the innovative and novel concept of onboard DC systems and provides a path for approval of DC systems into the traditional classification rules.

Outside of commercial applications, the US Navy is trying develop a Medium Voltage DC (MVDC) demo that de-risks shared energy storage and advanced MVDC circuit protection, operating above 4 kV (Ref. 14). The British Royal Navy has recently published several papers on the challenges in maturing DC designs to the point of acceptance in naval vessels (Refs. 15 and 16).

DC systems provide a stability challenge different to AC systems as the presence of reactive power in an AC system provides a stabilizing effect. The type of loads are important in a DC systems as constant power loads may cause instability in DC systems; as more current is drawn, then voltage has to drop to maintain a constant product of voltage and current. The ratio of load and source impedances has to be well understood in determining system stability (Ref. 15), a problem bidirectional loads and converters exacerbate as the source and loads are interchangeable and the relationship in impedances must also reverse which will probably require active control compensations for bi-directional loads. The use of capacitance in the network for stability is a common practice but the trade is providing enough capacitance to maintain stability while not oversizing capacitors and increasing the cost and size of converters. Finally, a low inductance busbar is important in creating an electrically stiff network; possible appropriate busbars are in different stages of development.

Fault protection and clearance is another well-known issue in DC networks. The lack of a zero-crossing requires that the switchgear to be large and expensive, especially in converter based systems which can have a very high inductance to resistance ratio on short circuit events. Current shipping applications are considering using the power electronic devices in the network to provide power regulation and system protection. Fold back control strategy allows the source impedance to be dynamically controlled so that it

follows the load impedance under faulted condition and thereby limiting and eventually eliminating the fault current. If the converters are to be used for system protection, they can do so accurately enough to limit the currents to a point where traditional over-current and differential circuit breaker discrimination strategies do not work making it difficult to isolate the fault (Refs. 16 and 17).

Finally, the role of energy storage on DC maritime systems is not well defined. Commercial applications often assume that redundancy in generation will alleviate the need for large energy storage systems. Whether the energy storage is located centrally or distributed next to critical loads will impact the behavior and control of energy storage and current regulations have taken the approach to define the power quality at the critical load's interface to the power system and have left it up to the designer to determine the size, type and control of the uninterruptible power supply based on the duration and duty cycle of the load.

1.4 TeDP Electrical System Voltage Standards

Flight-weight propulsive power rated microgrid systems necessitate the introduction of new aircraft distribution system voltage standards. Voltage impacts much of component and system performance. All protection, distribution, control, power conversion, generation, energy storage, and cryocooling equipment are affected by voltage regulation requirements. Information on the desired operating voltage and voltage regulation is required to determine nominal and maximum currents for sizing distribution and fault isolation equipment, developing machine topologies and machine controls, and the physical attributes of all component shielding and insulation.

Voltage standards provide assurance that electrical equipment will be operate and integrate effectively by applying generally accepted operating limits. These limits impose requirements on system components. Existing voltage standards express steady-state and transient limits in order to provide a common framework for component manufacturers. Adherence to the standard ensures that the equipment will operate effectively within the context of a conventional system. Additionally, the implementation of these requirements imposes generally accepted implications on the system. However, the introduction of new standards within the context of mature systems is challenging due to implications on the electrical systems supply chain. On the other hand, existing standards are insufficient to address the unique needs of revolutionary TeDP electrical systems.

The development of a voltage standard requires addressing a system in multiple perspectives. Therefore, the standard development activity manages stakeholder expectations and visions and results in a common set of bounds which guide the achievement of the goals. These bounds may encompass operational envelope, personnel safety, performance objectives, governance authority, or system stability. In order to capture expectations and requirements of different stakeholders, it is important to perform stakeholder analysis. Figure 8 starts to illustrate the major groups that will have input to the voltage standard and what a voltage standard will impact. This study focuses on framing the objectives and sensitivities from a design/engineering perspective.

1.4.1 Regulation, Protection, and Recovery: A Design/Engineering Perspective

Many of the requirements on regulation, protection, and recovery systems are derived from the systems transient performance. Therefore, as the challenges associated with custom voltage regulation and protection are addressed and matured for TeDP systems, new standards must evolve to meet the needs of the industrial base. Fundamentally, for a TeDP system, voltage limits ensure the provision of uninterrupted thrust to the aircraft during all flight conditions and operations in a manner which does not put operators at risk. For a TeDP system architecture, three areas of voltage management are required. These include voltage regulation, fault isolation and protection, and recovery and reconfiguration.

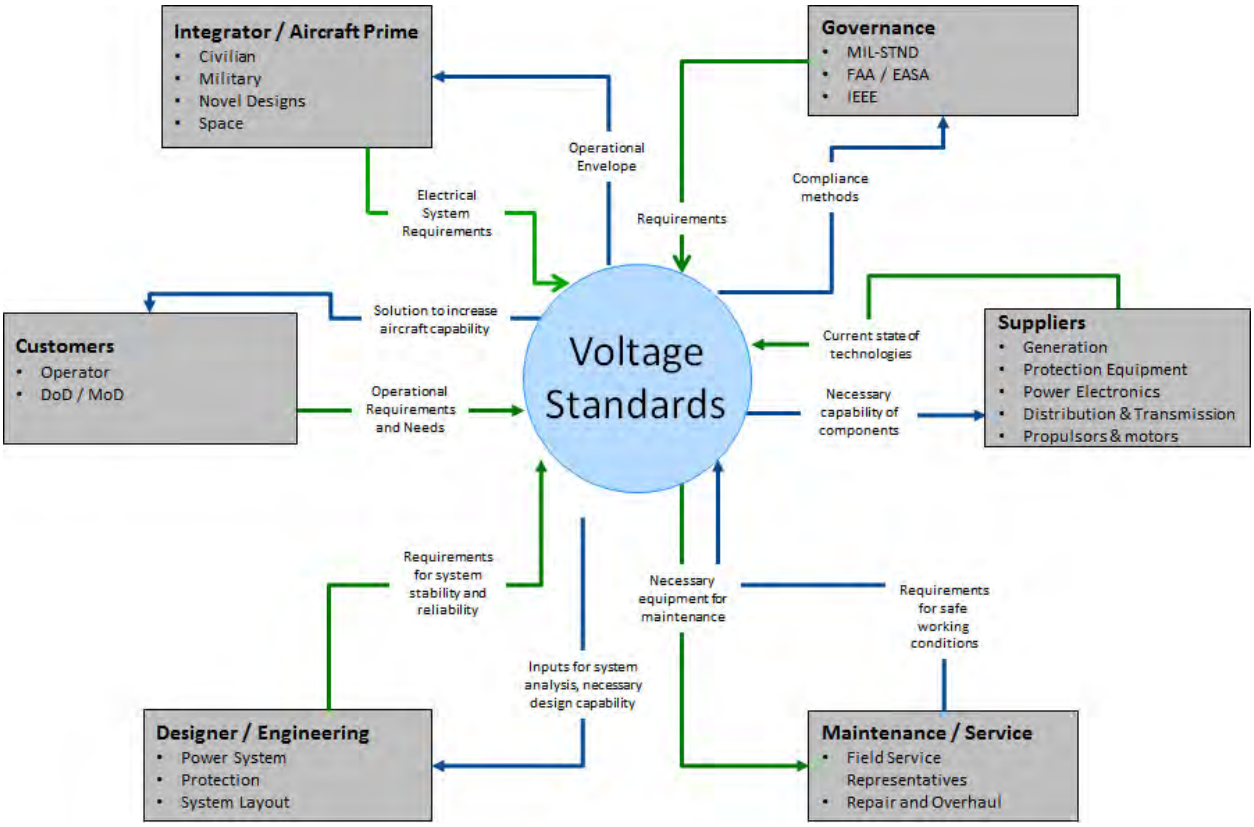

Figure 8.—Voltage Standard Development Stakeholder Map.

Recovery solutions were introduced via segregation and symmetry during system architecting to ensure that no single-point failure in the TeDP system would lead to a steady state loss in thrust power below minimum take-off power requirements. Additionally, the configuration is such that no adverse yawing moments are generated during a TeDP system fault.

During normal operation the system is operating with an "absence of any fault or malfunction that degrades performance beyond established requirements" (Ref. 18). Under these conditions, power conversion equipment manages voltage variations. When a fault or degradation occurs, protection devices operate to remove the malfunction within a broader set of abnormal operation limits. A notional voltage limit plot is illustrated in Figure 9.

Manipulation of these normal and abnormal voltage limits determines the requirements for each device within the electrical system. Normal limits define the required operation from the power sources and conversion/regulation equipment. Abnormal limits determine the impact of the maximum current and voltage ratings for all devices, as well as the current interruption capability for protection devices. Identifying the preferred voltage range for systems with low TRL components has its own challenges. In the absence of data, estimates of component attributes and sensitivity to requirements are based on projections of current technologies and first principle estimates regarding future technology capabilities.

1.4.2 Operational Voltage Limits Category Definitions

Considering the unique attributes of the loads and redundancy available on a TeDP electrical system, the definitions typically applied for aircraft power systems deserve revisiting. The definitions presented here are augmented from MIL STD 704F (Ref. 19).

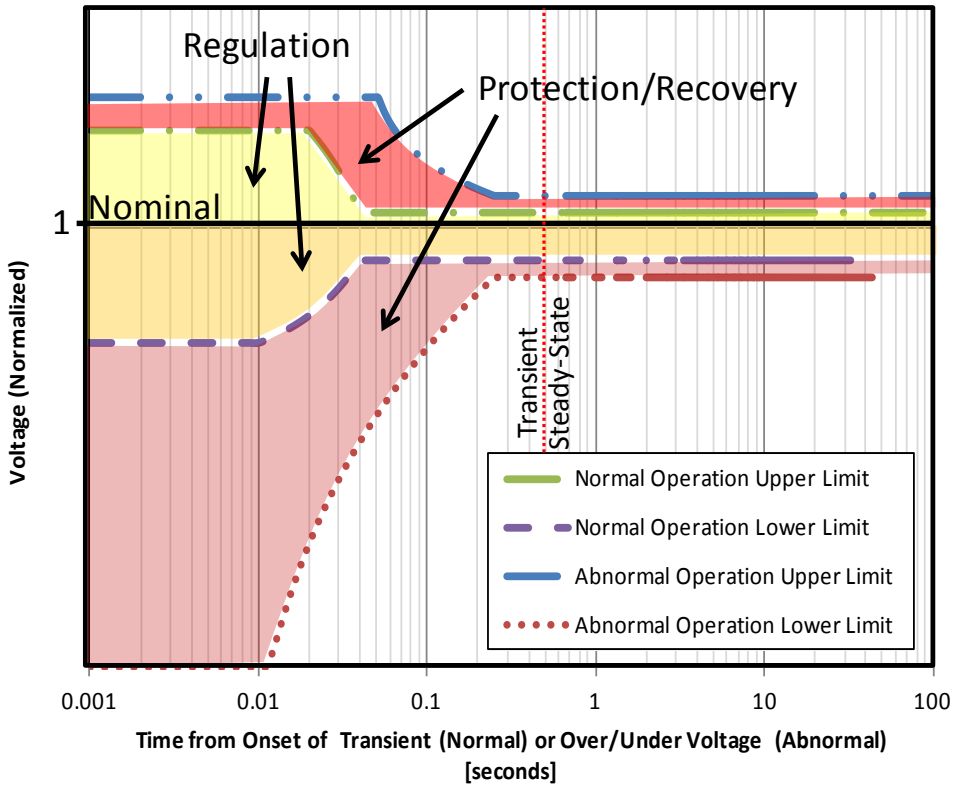

Figure 9.—Steady-state and Transient Voltage Limits for Normal and Abnormal Operations.

1.4.2.1 Normal Operation

Normal operation occurs when the system is operating as intended in the absence of any fault or malfunction that degrades performance beyond established requirements.

The major adaptation to this definition is the removal of transfer operation as a subset of normal operations. As is illustrated in Figure 9, voltage variability for normal operations can be very narrow. Nominal loads on a TeDP system are highly regulated and coordinated. Other types of microgrid networks must interface with loads which are unscheduled and unpredictable. Under normal conditions, the only transients experienced by the system are from the acceleration and deceleration of propulsor fans. Even in the presence dynamic loading requirements from stability augmentation for flight controls or from torque loads imposed by inlet distortions, the transients are relatively slow and can be coordinated at the system level.

1.4.2.2 Abnormal Operation

Under fault conductions a subset of the propulsors shall be permitted a degradation or loss of function as specified by aircraft propulsion and control requirements. Electrical system equipment shall not suffer damage or cause an unsafe condition.

Limits on the abnormal operations enforce the magnitude of the disturbance allowable. When normal operation limits are exceeded, protection and controls equipment act to isolate the failure and return to a normal operating state by initiating recovery and transfer operations.

1.4.2.3 Recovery Operation

After experiencing and abnormal operation, equipment undergoes recovery. Requisite propulsors shall automatically resume specified performance when normal operating characteristics are resumed. The requisite propulsors are determined by airframe by propulsion and control requirements.

Recovery operations occur on the faulted branches of the TeDP system after an abnormal operation occurs. Temporary loss of power to the propulsors will result during fault isolation and potential deployment of uninterrupted power supply (UPS) energy storage (depending on the location of the fault and fault zonal protection). After fault clearance, attempts may be made to re-engage the previously fault equipment. However, with fail-safe redundancy requirements for OEI scenarios, faulted sources may be forfeit for the remainder of the aircraft mission after a fault. Power for the propulsors allocated originally to the faulted source branch can receive power from healthy branches via transfer operations.

Following isolation and clearance of a load side fault, recovery may then include the removal of thrust requirements from propulsors with faulted electrical equipment or damaged mechanical equipment.

1.4.2.4 Transfer Operation

Normally operating equipment undergoes a transfer operation following abnormal operation of other equipment to facilitate a recovery operation.

Recovery operations occur on the faulted branches of the TeDP system. This operation occurs when power is routed from a healthy branch in response to an abnormal event on an adjacent branch. A transfer operation introduces the largest non-fault-related step loads on the systems. However, the timing of these loads may be coordinated with energy storage charge/discharge operation.

1.4.3 Selection of the Optimal Operating Voltage

With the bulk of the system components being superconducting, the requirements for an airborne TeDP system may not be driven by interface to normally conductive systems. Therefore, additional freedom is available to more intelligently define operational attributes of this wholly superconducting system. In the absence of applicable design standards, this requires a fundamentally different approach in defining optimal configuration. Due to the integrated nature of this system, the definition of the optimal voltage standards must be performed holistically. The sensitivities of all system components must be considered simultaneously.

Figure 10 illustrates the process and framework developed for identifying the optimal operating voltage standards for non-conventional aerospace microgrid systems. This process and framework is applied to the Rolls-Royce N3-X TeDP architectures to identify the trend for the optimal voltage levels based on predictions of component voltage mass and efficiency sensitivity, integrated system-level effects of voltage levels, and future technology development factors. With this information in hand, more accurate assessment of electrical system weight, volume, and reliability may be generated and drive component development requirements. The scope of the 2012 RTAPS study (RTAPS TEDP I) and the scope of the current RTAPS study (RTAPS TEDP II) are indicated in this figure.

This process for selecting the preferred operating voltage follows the traditional top-down, bottom-up engineering V-process (Ref. 20). This process is defined in four phases: architecture definition, nominal voltage selection, transient limit selection, and recovery scenario analysis. The tasks and activities for each of these phases. Each phase of this process requires additional levels of fidelity to evaluate the impact of voltage limits on the architecture weight and efficiency. The method and results discussed in this paper focus on the second phase of this voltage standard definition process. The architecture definition portion of this process has been documented in Reference 21.

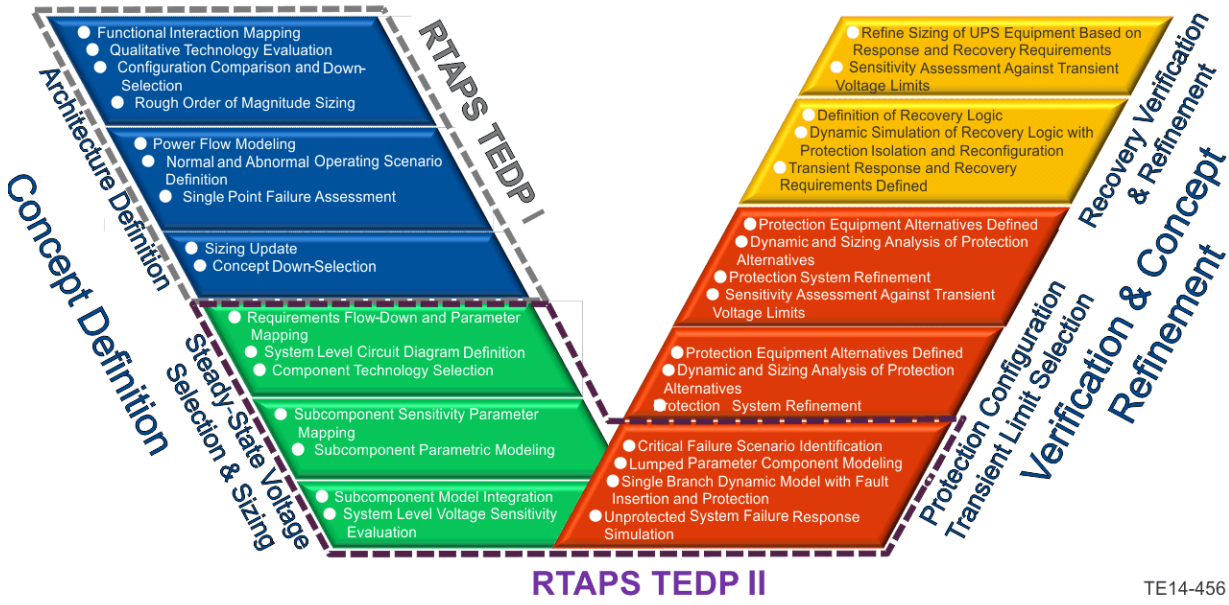

Figure 10.—TeDP Architecture Design Approach.

1.4.3.1 Phase 1

Phase 1 of this process (Architecture Definition) focuses primarily on defining the context and content to be considered when defining the transient and steady state voltage limits. This requires that the architecture be defined in terms of its general structure, functional interfaces, and technologies. Conceptual level modeling of power flow and sizing are used to justify the concept selection. The sizing of these systems requires that general contingency response concepts be defined for all pertinent operating scenarios.

The Phase I tasks were performed for this the N3-X architecture during previous studies. In 2012, the Rolls-Royce Electrical Power and Control Systems (EPACS) group delivered a Research and Technology for Aerospace Propulsion Systems (RTAPS) study to NASA that considered the stability, transient response, control, and safety of a high-power electric grid for the NASA N3-X TeDP system (Ref. 22). Under this research contract, promising electrical system architecture concepts were identified and compared. Weight and complexity comparisons were made between systems concepts based on estimated future component weight trends (Refs. 23 and 24).

This effort was successful in detailing the impact of safety, reliability, redundancy, protection, and integrated flight control requirements on TeDP system design. However, the holistic perspective applied by Rolls-Royce in this study identified significant gaps that must be addressed for this nonconventional electrical system development. The operating voltage level for this aircraft was discussed identified as an area interest for further evaluation.

1.4.3.2 Phase 2

Identifying the optimal voltage for the N3-X TeDP architecture is the primary objective of this study. During Phase 2 (Steady-State Voltage Selection and Sizing), additional scrutiny is applied to the architecture selected in Phase 1. The Phase 2 tasks are: component decomposition, subcomponent sensitivity assessment, system sizing and steady-state voltage selection. The activities in this phase map the effect of system level operating parameters on the individual subcomponents of the system. The sensitivities of these subcomponents are then evaluated against variations in the operating parameters.

These sensitivities are expressed in the form of first principle subcomponent models of or data where available. Once the subcomponent sensitivities are defined, an integrated system model that assembles these components for overall system evaluation is constructed. This evaluation determines the expected mass, efficiency, and operating parameters as a function of voltage and other system level operating parameters (temperatures, shaft speeds, etc.). This phase applies assumptions regarding the impact of protection and recovery on component size

One major challenge in identifying the optimal operating voltage will be the identification of component and system sensitivity to voltage regulation parameters. The process for performing this analysis will follow the basic framework for selecting the optimal dc system voltage used by Christou et al. and Cotton et al. (Refs. 25 and 26). Within the constraints of a fixed duct area size, minimum clearance required between wires and ground, and standard wire gauge sizes and their associated diameters, ac and dc system current rating, and insulation thickness, cases were considered for distribution systems for the configurations. The results of these system options was compared for peak voltage rating versus conductor diameter, power rating versus single-wire voltage rating, and power-to-weight ratio versus single-wire peak voltage rating. The wire voltage rating varies nonlinearly with power rating and power-to-weight ratio. Such trends allow the system to be optimized for the operating voltage based on maximum power rating or power-to-weight ratio. Alternatively, an operating voltage can be selected that is a compromise between these and other identified objectives.

A similar approach to voltage selection was applied in this study. However, the principles of this study are expanded to consider each piece of equipment in the electrical system. Therefore, reasonable estimates of the effect of voltage on power densities for superconducting generators and motors, cable, fault-current limiters, circuit breakers, and cryogenic converters are required. Where available, cryogenically operating component data was used for sensitivity models (IGBTs, diodes, superconducting cables). However, in most cases parametric models based on first principle and published analytical estimates were developed to identify the mass, efficiency, and voltage sensitivity of system components.

1.4.3.3 Phase 3

Many of the requirements on protection and recovery systems are derived by the transient performance of the system. Therefore, Phases 3 and 4 require dynamic system models and simulations. The activities in Phase 3 (Protection Configuration and Transient Limit Selection) focus on refining the requirements on the protection devices. The magnitude of the transient overcurrent and overvoltage requirements are assessed with respect to the performance of the protection devices (e.g., interruption time for solid-state circuit breakers (SSCBs) and resistivity transition for SFCLs). At the conclusion of this phase, the sizing sensitivity is revisited with updated transient protection equipment requirements.

Parallel to the voltage sensitivity modeling activities in support of Phase 2 objectives, dynamic models were developed for all grid components to enable trade studies around voltage regulation, fault protection and isolation, and thrust power recovery. The development of these models is presented in this report. However, addition work is necessary to exercise the models against fault conditions to update protection and conversion component sizing requirements.

1.4.3.4 Phase 4

The final phase of this process (Recovery Verification and Refinement) is intended to confirm and refine the contingency strategies defined in Phase 1. Assuming that the TeDP system must operate as an UPS, dynamic simulations of system recovery are performed to update energy storage and generation requirements for these recovery scenarios. Upon completion of this analysis, the sizing and sensitivity is performed with these additional requirements updates.

1.5 Introduction Summary

Establishing the feasibility and viability of a DC, superconducting, DC, microgrid TeDP system requires detailed understanding the integrated performance of electrical components, as well as the implications of system level requirements. In the absence of refined standards regarding voltage regulation, fault protection and isolation, and system recovery for this revolutionary system concept, one must rely on model representations of the system to guide technology development. This study supports a holistic TeDP electrical system architecture design approach through the development of parametric and dynamic models for the entire N3-X TeDP system. The parametric sizing models are used to determine the system level impact of performance requirements in terms of overall system mass and efficiency. Following preliminary sizing, the dynamic models are used to determine the transient operation requirements for the equipment. This information refines the assumptions used during parametric sizing trades to refine the architecture performance estimates.

This document reviews the development of these models and their implementation for nominal operating voltage optimization and dynamic analysis of fault accommodation strategies. It is hoped that this process and continued development of these tools will assist in establishing limits on normal and abnormal electrical system operations. This information will provide useful in providing requirements for individual technology development and provide continued support for the definition of TeDP system voltage standards.

2.0 Architecture Selection

2.1 Architecture Candidates

Candidate architecture concepts were adapted from deliverables provided under the previous RTAPS task order. These architectures are described. All architecture concepts here were sized considering fail-safe and single point failure requirements. No single point failure will lead to, or yield a catastrophic loss in thrust.

2.1.1 Concept 1: Baseline Architecture

A baseline architecture concept is illustrated in Figure 11. The baseline consists of four independent electrical systems. Each electrical system consists of 1 generator, 1 AC/DC converter, 1 bus with an associated energy storage device, and 4 propulsors. The initial concept included a total of 14 propulsors which required two buses supporting 3 propulsors and two buses supporting 4 propulsors. In order to mitigate asymmetric thrust with bus and generator faults, an even number of propulsors is desirable for each bus. Therefore, the number of propulsors was increased to 16, with four assigned to each power bus. This alteration is consistent for all architecture concepts.

The engine out scenario produces the sizing case for this architecture. In this scenario a group of 8 propulsors must provide 100 percent of the required thrust, supported by 2 buses. Therefore, each propulsor much account for roughly 12.5 percent of the minimum power and each bus must be able to support 50 percent of the power.

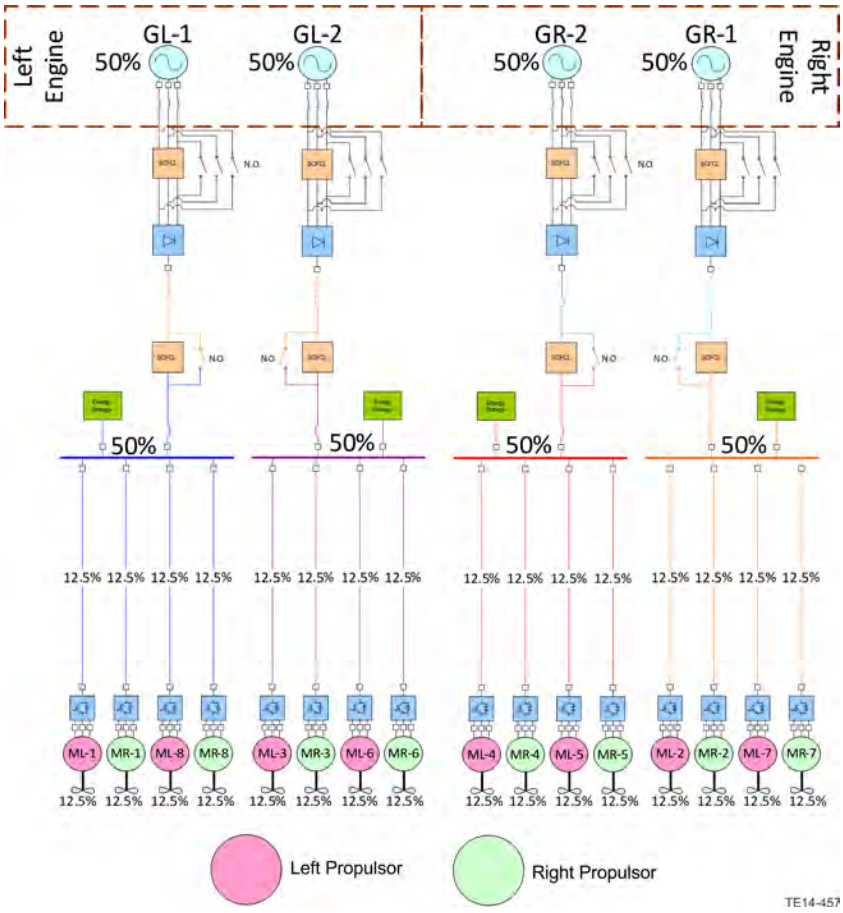

Figure 11.—Baseline Architecture Diagram.

This simple radial architecture concept acts as the baseline architecture for architecture comparisons. While this architecture is attractive in terms of simplicity, it is evident that the components are oversized.

2.1.2 Concept 2: Inner Bus Tie Concept

The second architecture concept allows for a reduction in propulsor oversizing by including a single point of reconfigurability in the system.

While the engine out scenario remains sizing critical, closing the bus tie engages more propulsors to provide thrust. Each set of 4 propulsors must provide a 1/3 of the total propulsive power. Therefore, the inner and outer buses and generators are sized differently to reflect the required interconnectivity (Figure 12).

2.1.3 Concept 3: 3-Bus Multifeeder Concept

A further reduction in propulsor oversizing can be achieved by allowing power to be rerouted through secondary feeders from other alternative bus sources. The engine out scenario no longer produces sizing critical requirements for the propulsor system. For this concept, the propulsors are sized to mitigate two propulsor fault conditions (Figure 13).

2.1.4 Concept 4: Cross-Redundant Multifeeder Concept

The final concept evaluated under the previous task order includes multiple layers of interconnectivity to reduce distribution systems oversizing. This comes at the cost to complexity and increases to the number of components in the system.

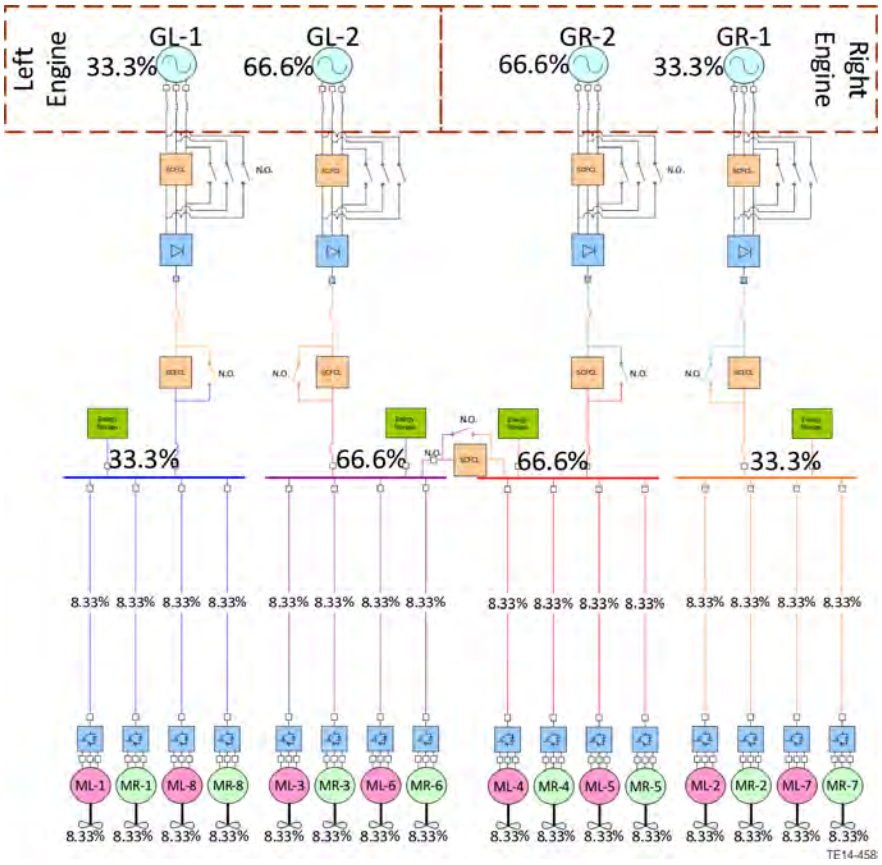

Figure 12.—Inner Bus Tie Architecture Diagram.

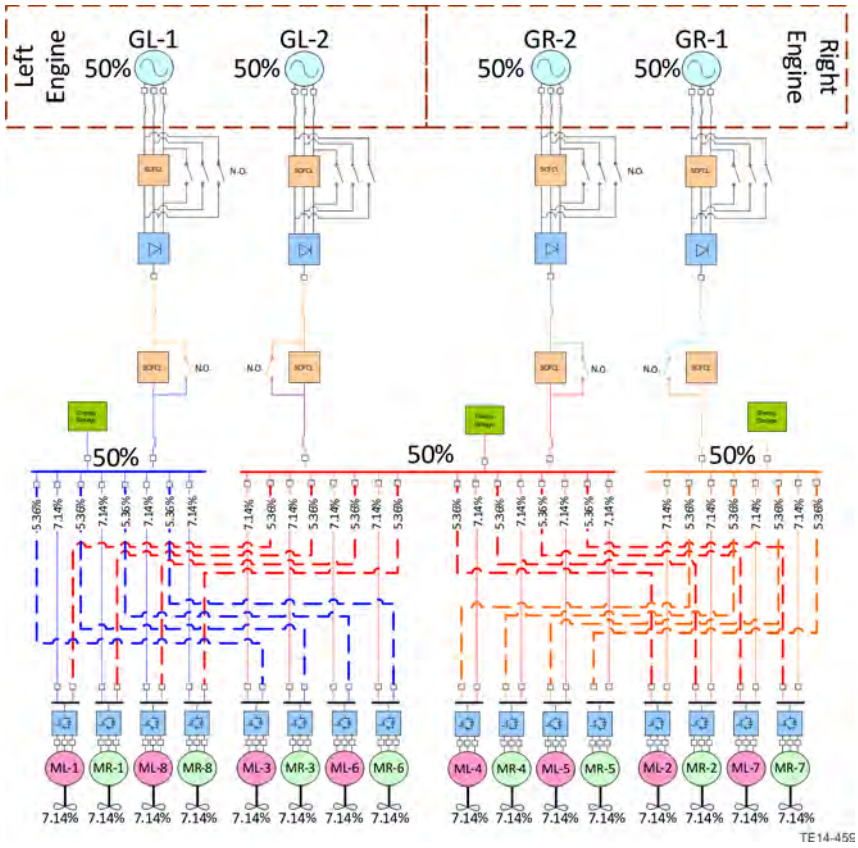

Figure 13.—Three-Bus Multifeeder Architecture Diagram.

This concept benefits from having an equal number of propulsors for each bus (Figure 14 and Figure 15). This allows for consistent sizing of all primary and secondary feeders, as well as the transmission and distribution components.

2.1.5 Concept 5: 4-Bus Inner Bus Tie Multifeeder Concept

An additional concept architecture was generated by combining the reconfigurability employed by the inner bus tie and multifeeder concepts.

This architecture was introduced because of its ability to represent three or the four candidate architecture in its modeling. The baseline architecture is represented by disconnecting the secondary feeders and opening the bus tie. Additionally, the inner bus tie concept is represented by disconnecting the secondary feeders. Finally, the multifeeder concept is represented by closing the bus tie and connecting the secondary feeders. Scaling of component capability limits is also required to represent these concepts.

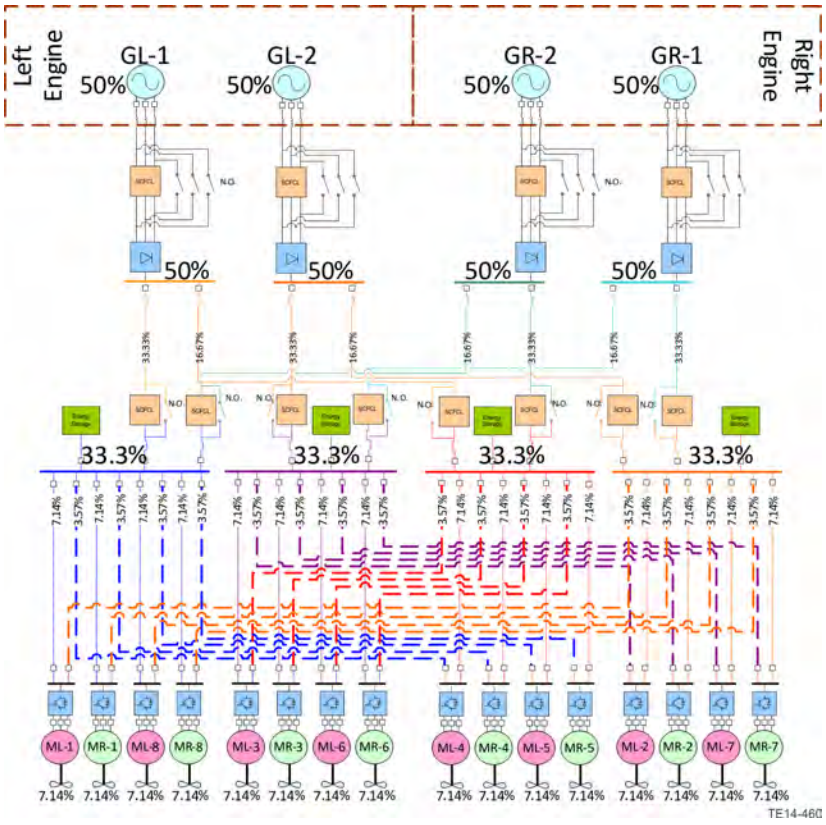

Figure 14.—Cross-Redundant Multifeeder.

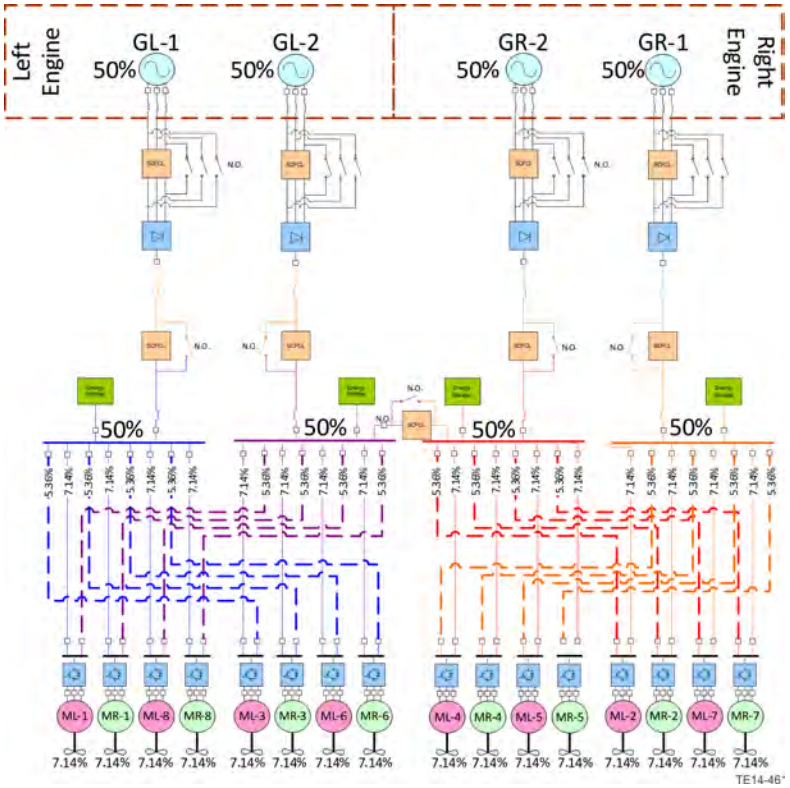

Figure 15.—Four-Bus Inner Bus Tie Multifeeder.

2.2 Architecture Evaluation and Selection

Table 2 shows the evaluation criteria used for evaluation and selection of the architecture concepts. The criteria in yellow were used in comparing and selecting the architecture of interest during the previous RTAPS task order. These criteria consider the architectures weight, complexity and performance. The weight approximations were made in the previous study on a specific weight basis and without consideration to voltage sensitivities. The weights and complexities of the various architectures will change on the voltage range for the system. As such, the analysis performed on the selected architecture evaluation remains valid for the other candidates. This evaluation has been performed without consideration of voltage sensitivity.

In addition, the current task order required a broadened evaluation of the architectures. With added deliverables to develop a process for architecture evaluation, the criteria in green were introduced. These new evaluation criteria consider the adaptability/scalability of a process developed by considering this single architecture concept (Table 3). Additionally, the difficulty involved in modeling the architecture was also considered.

Weightings were applied to the evaluation criteria to determine the preferential architecture going forward in for this project. A 1, 3, 9 scaling was applied for low, medium, and high weightings, respectively.

Application of these weighting and architecture assessments are illustrated in Table 3. The colors in this table indicate the criteria based assessment relative to the baseline concept. The darker the red the cell, the worse the concept performs relative to the baseline. The darker the green, the better the concept performs.

TABLE 2.—ARCHITECTURE COMPARISON MATRIX

	Architecture Evaluation Criteria	Weighting	Baseline	Inner Bus Tie	3-bus Multi-feeder	4-bus Inner Bus Tie, Multi-feeder	Cross-redundant multi-feeder
Previous Metrics	Weight, kg	High	5086	4227	4144	4176	4010
	Complexity						
	Failure Response (rerouting complexity)	Low	+	+			-
	Component count	High	116	118	158	160	174
	Excess Power, hp	Med	100%	33.33%	14.28%	14.28%	14.28%
New Metrics	Scalability of Process						
	Breadth of Protection Scheme	Med	0	+	+	++	+++
	Switching Functionality represented	Med	0	+	+	+	+
	Load interruption represented	High	0	0	0	0	0
	Model Complexity						
	Dynamic model (with protection)	High	0	-	-	-	---
	Multiple sources on common bus	Med	0	+	++	++	+

TABLE 3.—ASSESSMENT MATRIX

	Importance	Baseline	Inner Bus Tie	3-bus Multi-feeder	4-bus Inner Bus Tie, Multi-feeder	Cross-redundant multi-feeder	
Weight (kg)	9	1.00	1.17	1.19	1.18	1.21	
Failure Response (re-routing complexity)	1	1.00	1.00	1.00	1.00	0.75	
Component count	3	1.00	0.98	0.64	0.62	0.50	
Excess Power (hp)	1	1.00	0.33	0.14	0.14	0.14	
Breadth of Protection Scheme	9	1.00	1.20	1.20	1.75	1.75	
Switching Functionality represented	3	1.00	1.20	1.20	1.20	1.20	
Load interruption represented	9	1.00	1.00	1.00	1.00	1.00	
Dynamic model (w/ protection)	9	1.00	0.80	0.50	0.50	0.25	
Multiple sources on common bus	3	1.00	1.20	1.50	1.50	1.50	
		47.00	49.00	46.12	50.97	48.40	Absolute Rating
		0.00	2.00	-0.88	3.97	1.40	Relative Rating

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The weighted sum for each concept and the weighted sum relative to the baseline are given below in the assessment matrix.

Two architecture concepts are evaluated to be preferential to the baseline architecture and two concepts are evaluated to be worse than the baseline (Figure 16).

The 4-bus, inner bus tie, multifeeder concept is narrowly the preferential architecture according to this assessment. This is particularly due to the breadth of the protection schemes that it represents (the baseline, inner bus tie, and 3 bus multifeeder concepts can all be represented with the same model structure as this concept). Additionally, for some protection schemes and failure scenarios, this architecture requires that a load receive power from both the primary and secondary feeders simultaneously. The 4-bus, inner bus tie, multifeeder architecture also exhibits comparable weight and complexity scores to the preferential architecture which was selected previously (inner bus tie concept).

2.3 Weight Sensitivity and Deliverable Objectives

The design of superconducting transmission equipment current is predominately driven by objective to minimize the cost and volume of distribution cables with increased efficiency. However, for an airborne superconducting microgrid, overall system weight becomes more critical.

Considering the weight breakdown for this TeDP microgrid performed in the previous Rolls-Royce RTAPS study (Ref. 27) with the indicated assumptions of power, current, and torque density in Figure 17. For these architectures, cable weight is not of primary concern due to their relatively small overall weight contribution (4.1 percent of the system weight on average for all architectures considered). Looking at these weight evaluations, the voltage sensitivity of power electronics is preeminent (Table 4). This is followed by machine and protection sensitivity. Understanding the impact of voltage on these components is required to determine the optimal operating voltage for this TeDP architecture.

This deliverable does not explore these voltage sensitivities. However, it reviews typical and projected voltage levels demonstrated and studied for these architecture components. Additionally, the deliverable also presents an architecture down selection for our future sensitivity, sizing, and dynamic modeling.

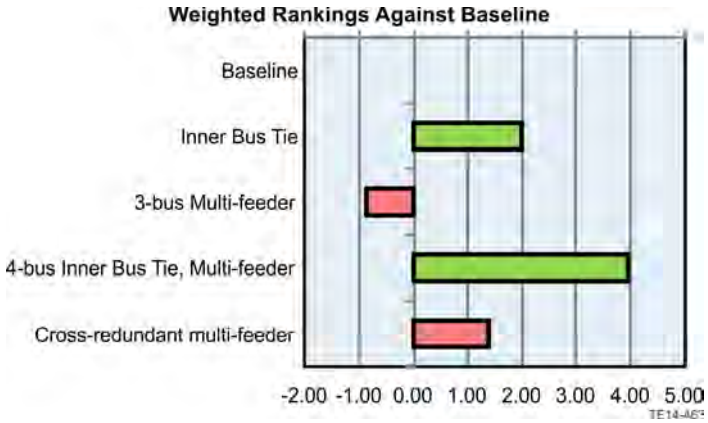
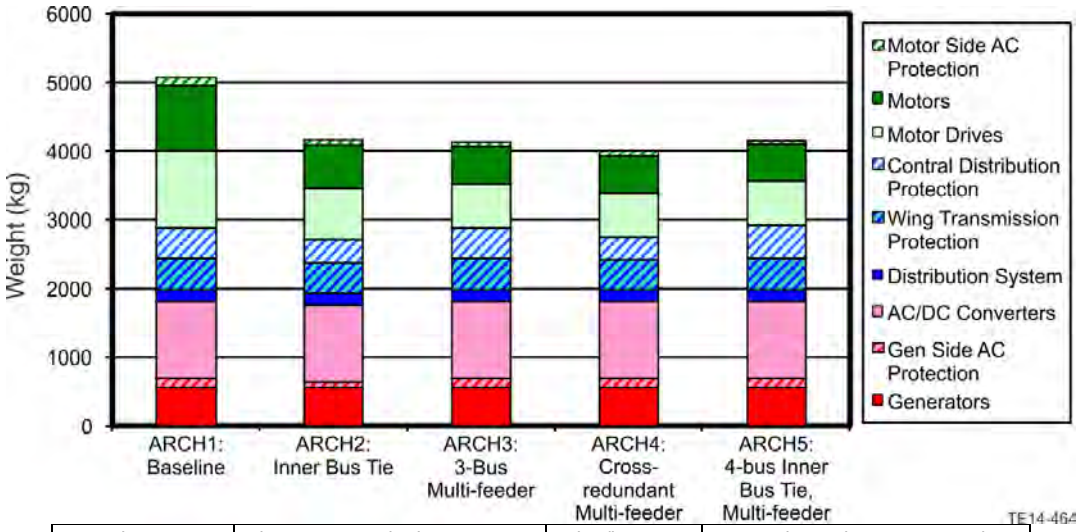


Figure 16.—Relative Weighting of the Architectures.



30,000 hp	Min Power Required	40 kW/kg	Power Electronics Power Density
4500 rpm	Prop. Speed	100 Nm/kg	Motor/Generator Torque Density
7500 rpm	Turbine Speed	200 kW/kg	DC Breaker Power Density
±10 kV	Voltage	350 kW/kg	AC Breaker Power Density
500 A/kg/m	Feeder Linear Current Density	0 lb/ft	Yaw Trimming Moment

Figure 17.—Weight Breakdowns.

TABLE 4.—ARCHITECTURE WEIGHT BREAKDOWN
[Results do not include energy storage weight estimates or fault current limiter weight.]

	Arch1: Baseline, %	Arch2: Inner bus tie, %	Arch3: 3-bus multifeeder, %	Arch4: Cross-redundant multifeeder, %	Arch5: 4-bus inner bus tie, multifeeder, %	Arch5: 4-bus inner bus tie, multifeeder, %	Average, %
Generators	11.2	13.5	13.7	14.2	13.6	13.6	13.3
Converters	22.0	26.5	27.0	27.9	26.8	26.8	26.2
Distribution system	3.5	3.9	4.3	4.3	4.3	4.3	4.1
Motor drives	22.0	17.6	15.4	15.9	15.3	15.3	16.9
Motors	18.7	15.0	13.1	13.5	13.0	13.0	14.4
Protection equipment	20.1	19.7	23.4	20.9	23.2	23.2	21.7

2.4 Overview and Naming Convention for Selected TeDP Architecture

The four-bus, inner bus tie, multifeeder architecture employs multiple layers of redundancy to provide uninterrupted thrust power the aircraft during electrical system failures. Source redundancy is provided by two engines, each driving redundant electric machines. Each engine is sized to provide the overall minimum thrust power required. Therefore, each electric machine is sized to provide half of the required thrust power. Under this arrangement, the transients experienced by the gas turbine will be a sudden increase in torque from 50 to 100 percent in the event of a one engine inoperable (OEI) condition or a torque loss from 50 to 25 percent for a single point electrical system failure.

During nominal operation, each generator supports a single distribution bus. Each radial connection between the generator source and the bus is termed a branch. Each branch is sized to generate and distribute a quarter of the required thrust power nominal and half of the thrust power required during a faulted condition. Power is delivered to the propulsors by means of primary and secondary feeders. Secondary feeders are used during branch and OEI fault scenarios. Additionally, the bus tie allows a single engine to provide power to all of the propulsors. Further discussion on the rerouting of power in response to failures is provided in Section 7.6.

Figure 18 shows a more detailed diagram of the architecture selected for this study. This figure also indicates the naming convention for each of the components in the system.

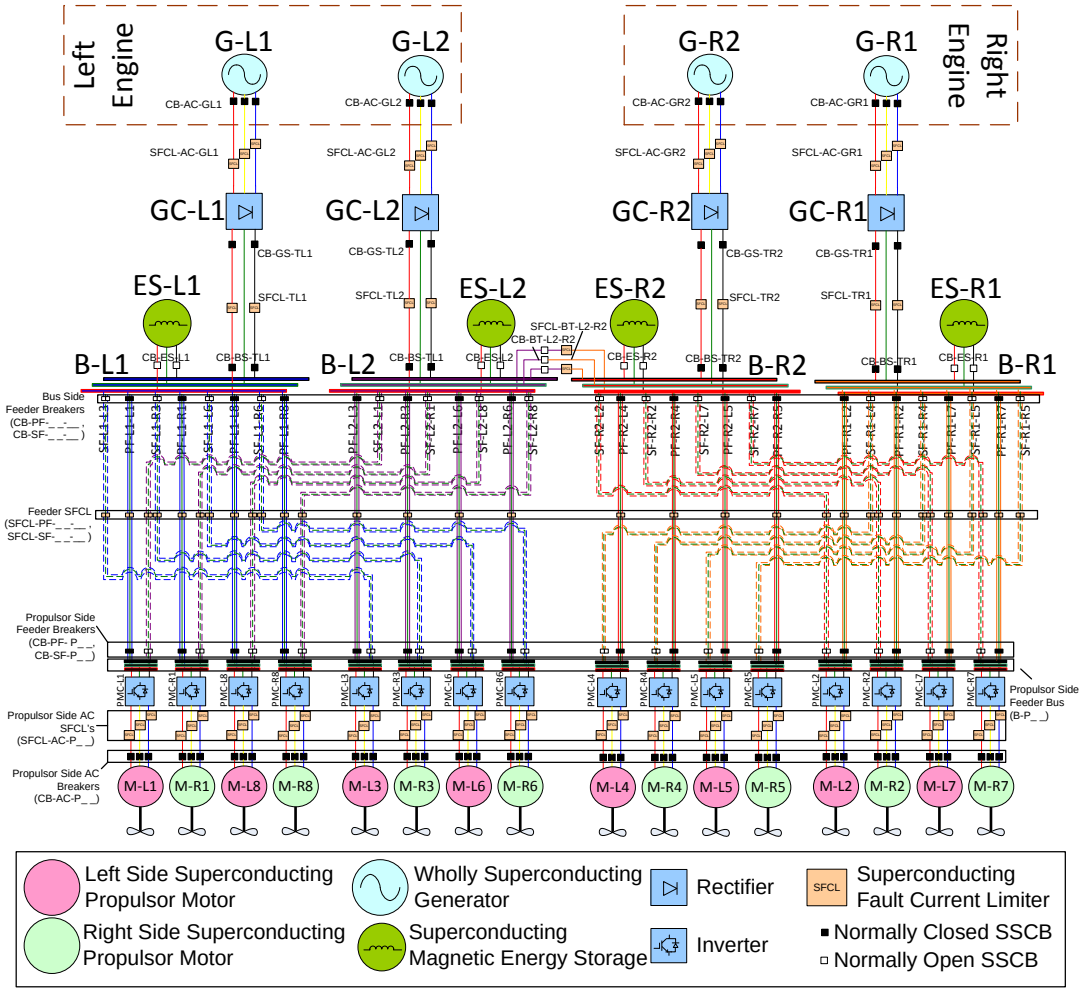


Figure 18.—4-Bus, Inner Bus Tie, Multifeeder Architecture Diagram with Component Naming Convention.

Not all components included in this diagram will be necessary in the final architecture. A protection system for this architecture may be provided by a combination of circuit breakers, fault current limiters, and the converter switches. However, following a dynamic evaluation of system faults, the final architecture may only require a subset of the protection devices illustrated in this diagram. Further discussion on potential configuration of the protection is provided in Section 6.3.

The naming convention illustrated in Figure 18 assigns nomenclature based on the relationship of the device to its related branch and/or proposal motor. The branches are labeled based on which turbogenerators provide them power. This nomenclature is given in Table 5.

TABLE 5.—NAMING CONVENTION FOR TEDP ARCHITECTURE COMPONENTS

Device	Label
Generator	G - <Branch Index>
Rectifier	GC - <Branch Index>
Bus	B - <Branch Index>
Transmission Line	T - <Branch Index>
Energy Storage	ES - <Branch Index>
Primary Feeder	PF - <Branch Index> - <Propulsor Index>
Secondary Feeder	SF - <Branch Index> - < Propulsor Index>
Propulsor Bus	B - P<Propulsor Index>
Inverter	PMC - <Propulsor Index>
Propulsor Motor	M - <Propulsor Index>
Turbogenerator AC Circuit Breaker	CB - AC - G<Branch Index>
Source Side Transmission Line Circuit Breaker	CB - GS - T<Branch Index>
Bus Side Transmission Line Circuit Breaker	CB - BS - T<Branch Index>
Primary Feeder Bus Side Circuit Breaker	CB - PF - <Branch Index> - <Propulsor Index>
Secondary Feeder Bus Side Circuit Breaker	CB - SF - <Branch Index> - <Propulsor Index>
Primary Feeder Propulsor Side Circuit Breaker	CB - PF - P<Propulsor Index>
Secondary Feeder Propulsor Side Circuit Breaker	CB - SF - P<Propulsor Index>
Propulsor AC Circuit Breaker	CB - AC - P<Propulsor Index>
Energy Storage Circuit Breaker	CB - ES - <Branch Index>
Bus Tie Circuit Breaker	CB - BT - <Branch Index1> - <Branch Index2>
Turbogenerator AC Superconducting Fault Current Limiter	SFCL - AC - G<Branch Index>
Transmission Line Superconducting Fault Current Limiter	SFCL - T<Branch Index>
Primary Feeder Superconducting Fault Current Limiter	SFCL - PF - <Branch Index> - <Propulsor Index>
Secondary Feeder Superconducting Fault Current Limiter	SFCL - SF - <Branch Index> - <Propulsor Index>
Propulsor AC Superconducting Fault Current Limiter	SFCL - AC - P<Propulsor Index>
Bus Tie Superconducting Fault Current Limiter	SFCL - BT - <Branch Index1> - <Branch Index2>

3.0 Terrestrial Systems Benchmarking

3.1 Power Transmission Superconducting Cable Installations

The voltage, current, and power ratings for current ground based power transmission installations using superconducting cabling were reviewed. The primary sources for these overviews were Electric Power Research Institute's (EPRI) "Superconducting Power Equipment Technology Watch 2012," (Ref. 28) and two reports from Sumitomo Electric Industries (SEI): "Present Status of International Standardization Activities for Superconductivity" (Ref. 29) and "Present Status and Future Perspective of High-Temperature Superconductors" (Ref. 30). The information from these reviews is plotted in the Figure 19, Figure 20, and Figure 21. The rated current for all of these systems ranges from 0.8 to 10 kA and the operating voltage ranges from 1.3 to 275 kV.

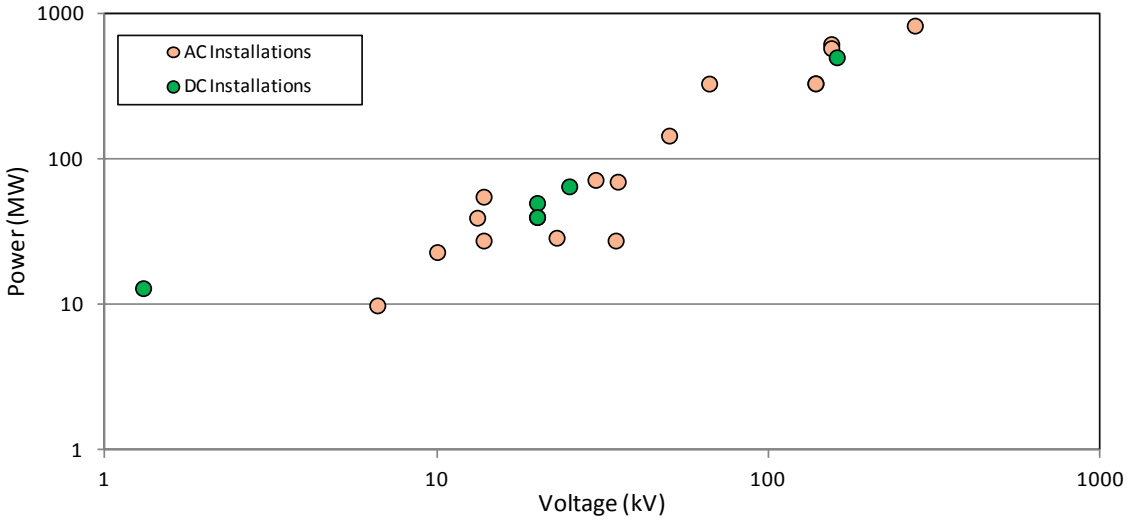


Figure 19.—Voltage, Current, and Power for Existing Terrestrial Cable Installations.

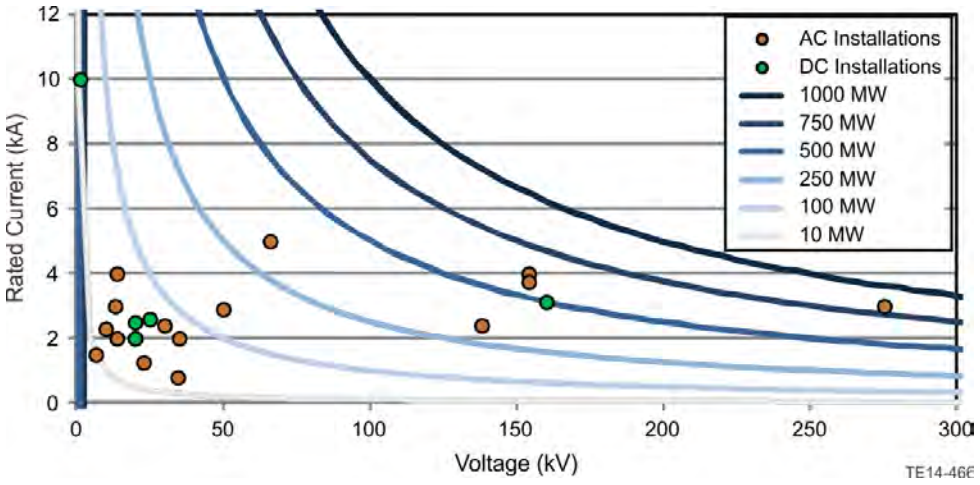


Figure 20.—Power versus Voltage Trends for Existing Terrestrial Installations.

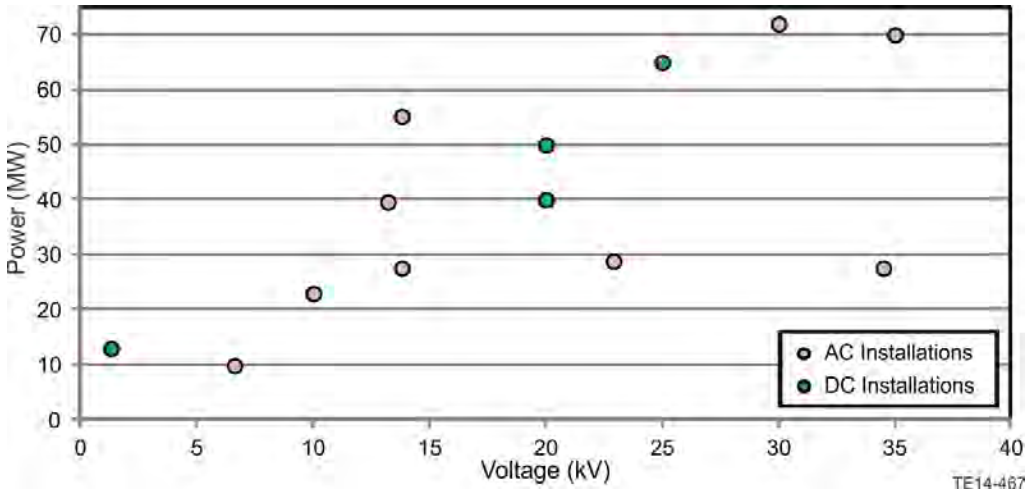


Figure 21.—Narrowed Range for Power versus Voltage Trends for Existing Terrestrial Installations.

The majority of superconducting installations interface to the electrical grid and are configured to operate with three-phase alternating current. These installations are labeled in orange in Figure 21. There are several DC transmission systems installed in Russia, China, Japan, and South Korea which are labeled indicated in green.

All of the transmission systems compared in these figures utilize LN_2 cooled YBCO or BSCCO with one exception. This exception is Russia's Hybrid Energy Transfer Line (ETL), which consists of a 12 m MgB_2 system cooled by LH_2.

From Figure 22 it is clear that the sizing of the superconducting transmission systems have a definite correlation with the rated power of the system. Generally, higher power systems implement higher voltage levels. However, focusing on the power levels applicable to TeDP (Figure 21), this trend is not as clear as voltages typically range between 1.3 and 35 kV. While this range will act as a baseline for future work in this study, all observed trends for the systems considered in this section are exclusively applicable to terrestrial systems. In contrast, weight metrics are of more significant interest for an airborne TeDP electric grid system.

3.2 Future DC Power Transmission Installations

In addition to its ability to provide a bulk power transfer with a significantly smaller footprint, superconducting DC power transmission systems promise to improve safety, reliability, and efficiency relative to existing AC power grid (Ref. 31). In advance of potential future applications, major superconducting cable manufacturers are beginning to enhance their high voltage DC capabilities.

Current work toward Korea's JeJu Island's ±80 kVdc substation interconnect and future concept plans toward New Mexico's Tres Amigas 200 kVdc energy hub are two examples of the future superconducting state of the art. While the risk and cost associated with current superconducting protection and conversion technology prohibited the implementation of a HTS solution for the Tres Amigas Project (Ref. 32), superconducting technology advances can have dramatic impacts on terrestrial transmission systems in the very near future.

In their report on Superconducting DC Cable, EPRI describes there baseline future concept for power transmission. This concept is described as "an interregional, superconducting dc cable system that is intended to achieve 10 GW power capacity with a nominal current and voltage of 100 kA and 100 kV" (Ref. 33). While the voltage level is certainly achievable with today's technology, technology

improvements are required to allow for increasing the standard operating currents by an order of magnitude. According to EPRI:

> *"The insulation level of 100 kA is easily achieved with currently available insulation schemes. In fact, the voltage level is so low that insulation thickness is determined by structural capabilities and ruggedness rather than by voltage standoff capabilities. A higher voltage could be readily achieved and would help meet the challenges posed by the high current. However, the advantages of keeping the voltage as low as possible are not to be ignored... High-power transmission at relatively low voltage is a hallmark of superconducting power transmission systems, both ac and dc, and is a key component of their economic viability."* (Ref. 33)

While the superconducting cable of the future requires multiple layers of conductor, insulator, formers, and coolant passages, the largest contributor to cable weight and size is the quench conductor. Additionally, the cable size is just a small portion of the overall vacuum sealed conduit used to thermally isolate the cryogenic system (Ref. 34).

With limited benefits achieved with increased voltage in terms of conductor and insulation impact, the main determining factor for voltage decisions is managing quench conditions.

A lower end limit of the operating voltage may be defined considering the power level of the TeDP electric grid and the maximum operating current. The maximum conventional terrestrial distribution system current identified was for a Chinese alumina electrolyzer plant. This system's operating current is greater than 10 kA. A cable transmission system providing 25 MW of power with a maximum current of 10 kA would require a minimum operating voltage of 2.5 kV (or ±1.25 kV).

Applying EPRI's future superconducting power transmission target of 100 kA, the operating voltage could drop to as low as 250 V (or ±125 V).

3.3 Superconducting Fault-Current Limiter Installations and Prototypes

There are many installations of transmission and distribution voltage-level superconducting fault-current limiters (SFCLs). In addition to these high power installations, there are a few lower power research projects involving the design and development of SFCLs at the University of Manchester, a Rolls-Royce University Technology Center (UTC). Key facts about each project are listed in Table 2. The Ph.D. dissertation from a student at the University of Manchester describes in detail the design, development, and test of a SFCL with an integrated vacuum interrupter (Ref. 35). This thesis also describes and tabulates the data in Table 2. The references for those sources are individually cited in this report.

From Table 2, it is notable that the projects using the superconductor MgB_2 operate at much lower voltage, current, and power levels than the installations using BSCCO and YBCO. This is due in part to the more recent discovery of MgB_2 as a superconductor (2001 compared to mid-1980s for BSCCO and YBCO) and the need for development to scale its production for higher current and power applications. All of these applications are for AC terrestrial grid fault-current limiting where the SFCL is the only dedicated superconducting device and interfaces to a normally conducting distribution line.

3.4 High Power Normally Conducting Solid-State Switchgear

While solid-state circuit breakers and switch gear for superconducting or cryogenic systems are only in the early research stage, there are initiatives to drive the design and development of normally conducting hybrid solid-state circuit breakers for power distribution voltages. Some advantages of high power solid-state circuit breakers over mechanical circuit breakers that also apply to aircraft power systems are the potential to eliminate momentary interruptions, provide instantaneous current limiting,

clear faults more quickly, and limit inrush currents for capacitive loads. In Reference 36, EPRI outlines requirements and specifications for a 15 kV, 600 A steady-state current rating design. Other relevant requirements are a short-circuit current rating of 12.5 kA (symmetrical, for 1 s), less than 10 kW of losses, and fault clearing within half a cycle (8.3 ms).

3.5 Cryogenic Semiconductors

Semiconductor performance is directly related to temperature across several aspects. Mainly, carrier density decreases, carrier lifetime decreases, and carrier mobility increases with decreasing temperature. First, a doped semiconductor typically decreases in resistance with decreasing temperature due to the reduction of lattice scattering of carriers (Ref. 37). Yet, at a specific dopant concentration and material temperature, impurity scattering causes a decrease in carrier mobility, increasing resistance, with a decrease in temperature. This change in resistance gradient with respect to temperature occurs at approximately 50 K for silicon as seen by the relative invariance of electron mobility in the 30 to 50 K range in Figure 22 and several orders of magnitude decrease in dopant concentration in the 30 to 50 K range in Figure 23.

Second, a PN junction voltage tends to increase with decreasing temperature due to the increased band gap energy (Refs. 37). Furthermore, the saturation current exponentially decreases with decreasing temperature.

The solid state device overall performance at cryogenic temperatures is a complex combination of the carrier concentration, carrier mobility, band gap energy, and the device structure. For instance, as the temperature decreases from room temperature to 70 K, the threshold voltage of non-punch through insulated gate bipolar transistors (NPT-IGBT) increases and the “on” resistance decreases due to the increase in band gap and the increase in carrier mobility, respectively. When cooled further, there is a two stage resistivity and increasing threshold voltage. Yet in general several groups of scientists and engineers have shown that with decreasing temperature, device resistance decreases, device switching speed increases and device threshold voltage increases (Refs. 38, 39, and 40).

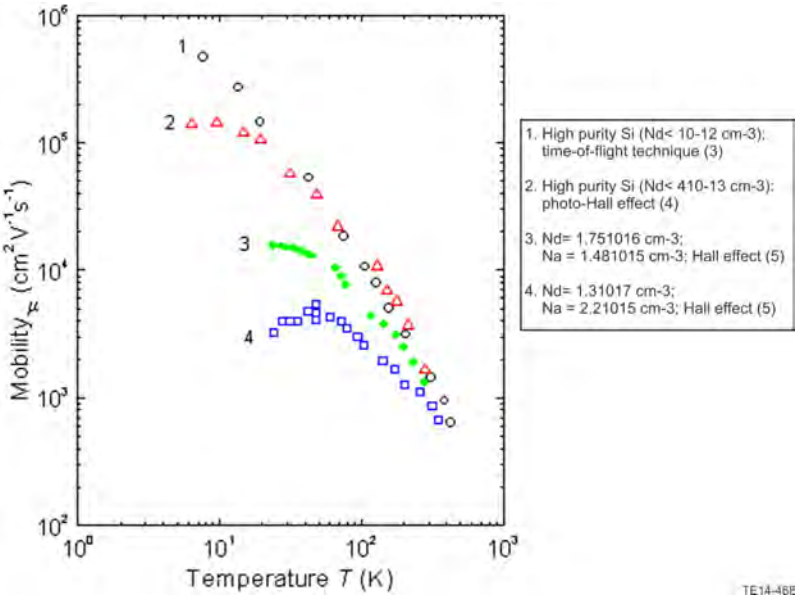


Figure 22.—Electron Mobility versus Temperature for Different Doping Levels.

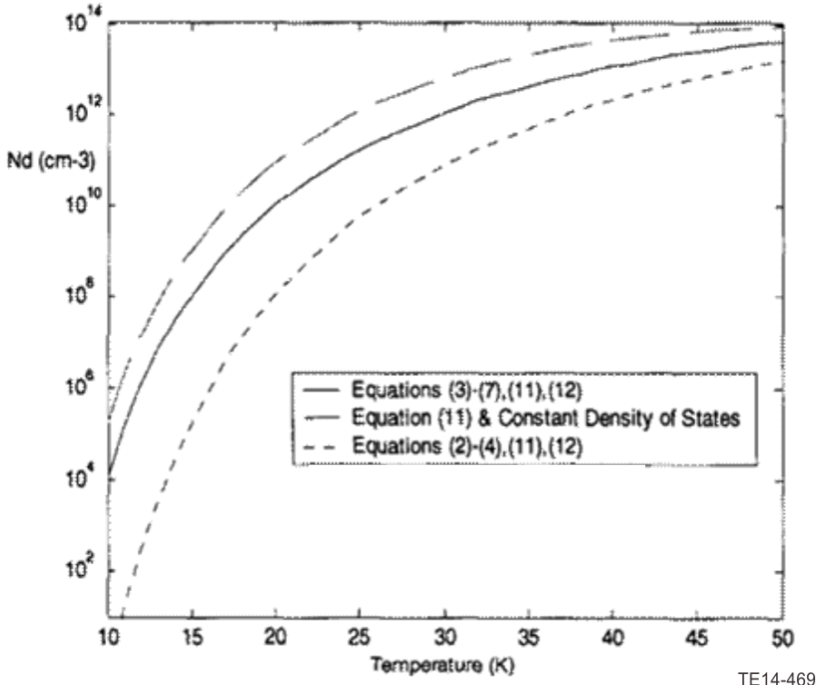


Figure 23.—Various Estimations of Ionized Donor Concentration as a Function of Temperature. The Background Doping Density Is Assumed To Be 10^{14} cm^{-3} and Phosphorous as the Dopant Species.

From literature review, as a generalization for all devices, switching time, thus switching losses, decrease by tenfold and the hold-off or reverse break down voltage decreased by ~30 percent, while the resistance and threshold voltage combined to give negligible change in conduction losses. The reduction in switching time may not provide any benefit due to packaging parasitic inductances and capacitances. Due to the high power nature of this application we shall use IGBTs as the example device topology. As such, the reduction in switching times may provide benefit due to the "current tail" or delayed turn-off characteristic limiting switching speeds rather than packaging parasitics. Modern trench gate IGBTs have shown more detriment to breakdown voltage at lower cryogenic temperatures. This reduction in breakdown voltage is as high as 70 percent in trench gate IGBTs at approximately 50 K. Although other semiconductor devices are available for higher power densities, such as the gate turn-off thyristors (GTOs), MOS gated thyristor (MGT), MOS controlled thyristor (MCT), Integrated Gate-Commutated Thyristor (IGCT), etc., no research was found that quantified the cryogenic performance of these devices. A scaling of device parameters for a selection of IGBTs is shown in Table 6.

Typical passive components require careful consideration at cryogenic temperatures. Yet, polymer film, solid tantalum, and mica capacitors have relatively small changes in capacitance and equivalent series resistance and decreased dissipation factors (Refs. 41 and 42). Similarly, high permeability alloy cores show little variation over temperature. However, ferrite cores decreased in permeability drastically with temperature (Ref. 43).

Recent technical and market progression for hybrid and electrical vehicles has resulted in an overall inverter specific power reaching ~17 kW/kg (Ref. 44). A typical mass percentage of equipment is shown in Table 7 (Ref. 45). By applying the variation in ratings to the mass percentages of typical lightweight inverters for cryogenic operation, one may estimate the mass for generator active rectifiers, generator field drives, and motor inverters. Similarly, the component room temperature parameters may be scaled for cryogenic temperatures for use in a mechanical and semiconductor hybrid circuit breaker.

TABLE 6.—PUNCH THROUGH (PT), NON-PUNCH THROUGH (NPT), AND TRENCH GATE (TG) DEVICE PARAMETER VARIATION AT 30 K RELATIVE TO ROOM TEMPERATUR (REFS. 46 AND 47)

Device	PT (600 V 250 A)	NPT (1700 V 200 A)	TG (1700 V 150 A)
Resistance	100% (30 mΩ)	100% (50 mΩ)	100% (50 mΩ)
"Knee" voltage	110% (0.7 V)	200% (0.5 V)	170% (0.7 V)
Turn-off time	50% (400 ns)	15% (2800 ns)	5% (600 ns)
Breakdown voltage	75% (900 V)	60% (2000 V)	35% (1800 V)
Gate capacitance	100%	100%	100%
Switching losses	33% (5.8 mJ)	20% (25 mJ)	20% (33 mJ)

TABLE 7.—AUTOMOTIVE INVERTER COMPONENT MASS PERCENTAGES (REF. 48)

Component	Mass percentage
Heat exchanger	37
Power modules, gate drivers, PWBs	23
Housing	15
Capacitors	12
Bus bars	7
Current sensors	6

3.6 Cryogenic Power Converter Prototypes

Both high and low power cryogenic power converters are in the early stages of research. One example of a low power DC-DC converter was designed, developed, and tested at the University of Manchester (Ref. 49). The converter was designed as the field controller for a superconducting machine in 2012. The machine's field was superconducting. Basic specifications for the cryogenic DC-DC converter are: 50 V output, tested up to 40 A (2 kW), MOSFETs used as switching devices, operated at 77 K, a closed-cycle cooler was used, and liquid nitrogen was the cooling medium.

Higher power converters were prototyped for naval propulsion by MTECH under funding from the Missile Defense Agency. The two prototypes, one low voltage at 600 V and one high voltage at 1200 V, showed increased efficiency, from 97.3 to 99.7 percent, at liquid nitrogen temperature ranges (Ref. 50). Yet, the cryogenic efficiency was admittedly difficult to quantify due to the dynamics of the pulse waveform and the precision of the test equipment. For the high voltage bridge the increase in efficiency was attributed to the greatly reduced turn-off times, thus switching losses.

Due to carrier "freeze out," or inability of carriers to reach the conduction band below approximately 40 K for highly doped silicon, large band gap semiconductors must be used if MgB_2 is the superconductor of choice. Ironically, research into high temperature semiconductor power devices and provides the technology for lower cryogenic temperatures (Refs. 51 and 52). Since the highest HVDC conversion system is 275 kV, the relative size and cost of the conversion equipment will influence the overall design optimization without a hard constraint with respect to voltage (Ref. 53). To derive the weight of the conversion equipment, the present strategy is to scale state-of-the-art converters designed for weight and cost in the automotive market with respect to each component. The semiconductors will assume IGBTs at a maximum of 10X room temperature switching speeds, and a hold off voltage reduction of 30 percent from room temperature. The passive components will then be a per unit scale of modern mobile inverters

as a function of state (current for inductors and voltage for capacitors) and frequency. The resulting mass will be used for overall system sensitivity analysis.

3.7 Superconducting Electric Machine Prototypes

While superconducting electric machines are not the focus of this voltage sensitivity study, it is beneficial to understand the operating voltages of superconducting machine prototypes. The power converters must rectify the generator voltage and invert the DC distribution voltage to control the motors. Because of this interface, the power converter voltage sensitivity should also consider electric machine voltage operation.

Several prototypes of partially superconducting electric machines have been developed and tested (Table 8). Key metrics of these designs are tabulated in Table 9. Additionally, a fully superconducting electric machine prototype is being built in 2013 at the University of Manchester. For these prototypes, the phase voltages are rated to 2 to 4.5 k.

3.8 Study Voltage Range Conclusion

Current installations and prototypes of superconducting cables, SFCLs, electric machines, and cryogenic power converters all involve connections to normally conducting and higher temperature environments. As a result, the operating voltage of the component is constrained by this connection and the surrounding electrical system architecture. These systems range from research prototypes to full-scale transmission operation. Based on these installations, the DC distribution voltage range for this TeDP superconducting architecture study will be 2.5 to 40 kV with potential extended targets. The lower limit is set by the maximum current carrying capacity of existing installations. The upper limit is based on current installations of superconducting cables in the power range of the distribution cables for this TeDP architecture (≈50 MW).

An extended range of interest may also be evaluated which would include 250 V at the lower end and 270 kV on the upper end. These reflect potential future current carrying capacities for DC superconducting cables. The upper limit represents the limit for current terrestrial installations. The practical final voltage range for the TeDP architecture will be determined by the critical current density of the superconductor in the N+3/N+4 time frame in order to generate, convert, and distribute the necessary propulsion power.

System weight will be highly sensitive to the operating voltage selected. Therefore, this deliverable was intended to pose a voltage range of interest for in support of future.

TABLE 8.—CURRENT SFCL INSTALLATIONS AND RESEARCH PROJECTS

Installation company	Date	Operating voltage, kV rms	Rated operating current, kA rms	Expected max fault current, kA	Superconductor material	Operating temperature, K	Rated power, MW	Cooler	Size	Type	Recovery time, s	Ref.
University of Manchester, Hyper Tech Research	2013	5.5	1.25	2.8	MgB_2	20-34	6.875	Gifford McMahon	8- by 10-ft skid	Resistive	180	54
University of Manchester, Hyper Tech Research	2012	0.00779	0.283	0.7	MgB_2	20-34	0.220457	Scientific Magnetics, Gifford-McMahon, Helium		Resistive	50	55,35
ACCEL/Nexans	2004	12	0.6		BSCCO 2212 bulk		7.2			Resistive		56
Nexans/ASL	2009	12	0.1		BSCCO 2212 bulk		1.2			Resistive		57
Nexans	2009	12	0.8		BSCCO 2212 bulk		9.6			Resistive		57
Nexans/ASL	2011	12	0.4		BSCCO 2212 bulk		4.8			Resistive		57
Nexans	2011	12	0.560	63	YBCO tape	77	6.72	Nexans Open Loop, LN_2	2.5- by 1- by 13-m, 2.5 tons	Resistive	10	28
Nexans	2013	24	1.005	25.6	YBCO tape		24.12	Gifford McMahon, LN_2	10- by 1- by 3-m	Hybrid		28
Siemens/AMSC	2007	7.5	0.3		YBCO tape		2.25			Resistive		58
Siemens/AMSC	2011	138	1.2	63	YBCO tape	< 75 K	165.6	Cryomech, LN_2	8-m long by 3-m diameter 40,000 kg per phase	Hybrid Resistive	15	59
CESI Ricerca	2005	3.2	0.22		BSCCO 2223 tape		0.704			Resistive		60
CESI Ricerca	2006	0.397	0.096		MgB_2 tape		0.038112			Resistive		61
ERSE, Sumitomo	2010	9	0.25	30	BSCCO 2223 tape	65	2.25	Stirling BV, LN_2	3/5- by 2- by 4-m, 3.8 tons	Resistive	10	62, 28
ERSE	2012	9	1		YBCO tape		9			Resistive		62
SuperPower	2004	8.6	0.8		BSCCO 2212 bulk		6.88			Resistive		63
Zenergy	2009	12	1.2		BSCCO 2223 tape		14.4			DC biased iron core		64
Zenergy	2011	12	1.2		BSCCO 2223 tape		14.4			DC biased iron core		65
CAS	2005	10.5	1.5		BSCCO 2223 tape		15.75			Diode bridge		66
Innopower	2007	35	1.5	41	BSCCO 2223 tape	77	90	Open loop, LN_2	4.2- by 4-m diameter, 27 tons	DC biased iron core	0.8	67, 28
Innopower	2010	220	1.36		BSCCO 2223 tape		300			DC biased iron core		68
Hyundai	2007	13.2	0.63		YBCO tape		8.316			Resistive		69
KEPRI/LSIS	2007	22.9	0.63	25	YBCO thin film	71	14.427	Closed Loop, LN_2	2.5- by 1.2- by 2.4-m, 1 ton	Hybrid resistive		70
Toshiba	2008	6.6	0.072		YBCO tape		0.4752			Resistive		71

TABLE 9.—CURRENT SUPERCONDUCTING ELECTRIC MACHINE PROTOTYPES

Installation company	Date	Machine description	Rated phase voltage, kV	Rated operating current, kA	Rated power, MW	Super-conductor material	Rated speed, rpm	Cooler	Operating temperature, K	Ref.
University of Manchester	2010	Superconducting field winding (rotor)	2.71	1.73	7	MgB_2	156		20-30	72
AMSC, CAPS, ONR	2004	HTS field winding on rotor, conventional copper air-core winding on stator	2.4	0.715	5		230			73
GE, NREL/DoE	2004	HTS field	4.16	0.255	1.5	BSCCO-2223	3600	Closed-cycle Gifford-McMahon, helium		74

4.0 DC Protection Devices

4.1 Introduction

There are several ways to protect superconducting DC electrical systems—dedicated DC protection devices, control of rectifiers and inverters, and quench control. Candidates for dedicated DC protection devices are the primary focus for this document. An understanding of the characteristics and limitations of these devices is required in order to design the electrical system protection and control. However, before designing the protection and control, a transient electrical and thermal fault analysis of the complete electrical system architecture is necessary in order to determine the protection requirements and decide which protection technologies should be used to implement the protection and control design. The protection requirements will be defined to meet one or more objectives such as minimizing the protection equipment weight or maximizing the efficiency of the protection system.

The dedicated DC protection devices discussed are electromechanical circuit breakers (EMCBs), hybrid circuit breakers (HCBs), and SSCBs. Superconducting fault-current limiters (SFCLs) can also be used in conjunction with a circuit breaker in order to further limit the fault current required to be conducted and interrupted by the circuit breaker. A detailed discussion of circuit breaker use with SFCL is not included in this document but should be studied when determining implementation of the protection system. A notable difference between the types of circuit breakers is their operating time as discussed in Reference 75 (see Figure 24). For a conventional DC electrical system as well as a superconducting system before quenching, the fault energy required to be dissipated by the circuit breaker is reduced when the circuit breaker can interrupt the fault current more quickly. Generally, the size and mass of the circuit breakers is reduced for lower fault energy dissipation requirements. In the case of a quenched superconducting system, the fault current is significantly reduced, so the increased circuit breaker operation time may not be as advantageous. However, the energy lost to heat due to the increased resistance during quench may have a significant impact on the cooling system size. Additional differences discussed for the different circuit breaker technologies include weight and conduction resistance.

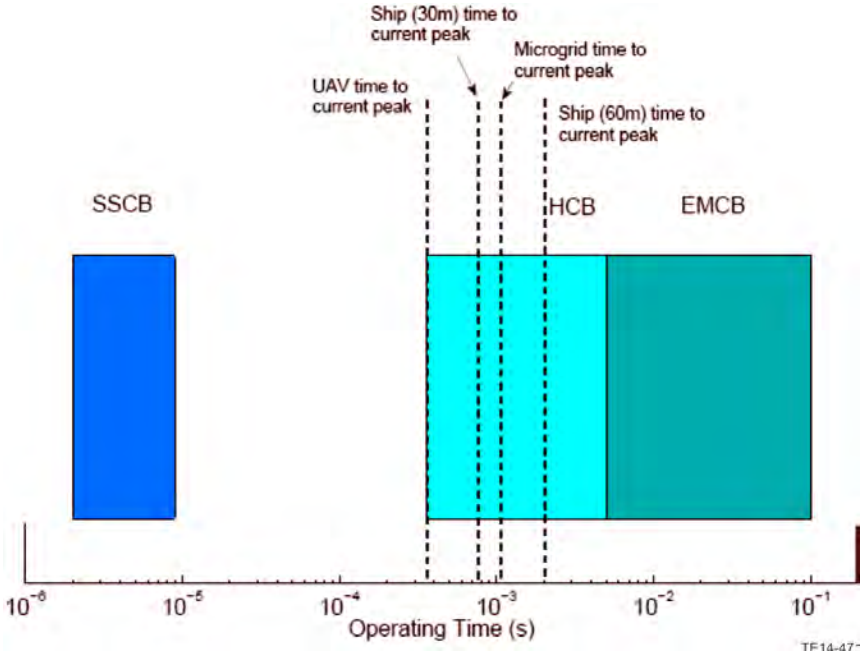


Figure 24.—Comparison of Circuit Breaker Operating Time with Time to Peak Current for Different Electrical System Architectures (Ref. 75).

4.2 DC Electromechanical Circuit Breakers

4.2.1 Conventional DC EMCBs

DC mechanical circuit breakers rated for interruption of thousands of amperes have been developed for industries such as traction. They employ a mechanical switch and a means to absorb and dissipate the fault energy, such as a cold cathode arch chute (Ref. 76). As part of the mechanical circuit breaker, applying a magnetic field orthogonal to the arc (by means of permanent magnets, secondary coils, or magnetic field due to current) can be used to move the arc from the contact gap into the splitter plates. Examples of DC mechanical circuit breakers rated for large DC current interruption are predominately developed for traction applications, such as those developed by Hawker Siddeley Switchgear Ltd, Sécheron, and GE (Refs. 77, 78, and 79). Figure 25 illustrates the components in an example EMCB. These DC circuit breakers are developed with different ratings for the rectifier and feeder of a traction power substation. Most of these are air circuit breakers with electromagnetic blowout. The electrical contact material is silver tungsten carbide. Note that these devices are typically designed to operate from –25 to 40 °C and up to 2000 m altitude. These existing designs can be operated at higher ambient temperatures up to 55 °C or at higher altitudes, but their operation is then derated. They are traditionally not designed to withstand vibrations beyond 0.5 g per 30 s nor for high humidity. Table 10 shows characteristics of several EMCBs including weight, conduction resistance, approximate operating time, and electrical specifications.

A potential advantage of the mechanical circuit breaker over the hybrid or solid-state circuit breakers is lower conduction losses during normal operation, which becomes more significant for higher nominal current operation. More information about hybrid circuit breakers is presented in Section 4.3. Additionally, the mechanical and hybrid circuit breaker provides a physical separation of conductors while the solid-state circuit breaker relies on semiconductor dielectric strength. However, DC mechanical circuit breakers take significantly longer to interrupt the fault compared to solid-state energy dissipation. Assuming that faults can reliably be detected, discriminated, and the electrical system has not quenched, then it is advantageous to interrupt the fault faster in order to reduce the fault energy.

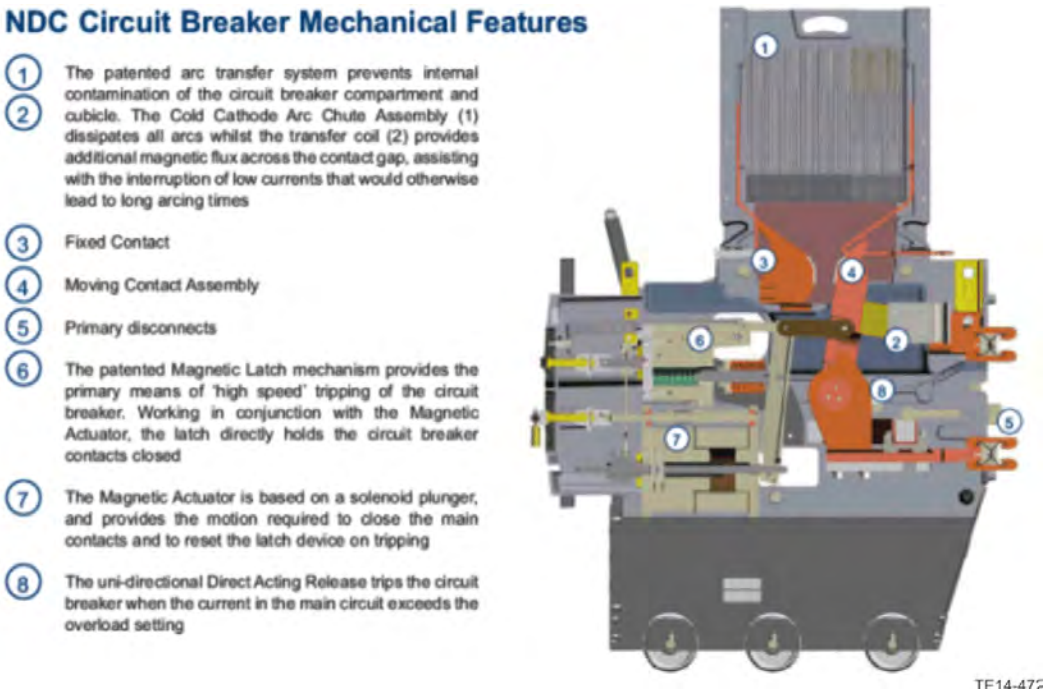


Figure 25.—Hawker Siddeley Switchgear Ltd Lightning DC Circuit Breaker Mechanical Diagram (Ref. 77).

TABLE 10.—EMCB DEVICE CHARACTERISTICS

Device Name	Developed by	Weight, kg	Normal conduction resistance, mω	Approx. operating time, ms	Rated voltage, kV	Normal operational current rating, kA	Fault current rating, kA	Ref.
Lightning NDC Circuit Breaker	Hawker Siddeley Switchgear	580	0.005	100	0.75	4	125	77
Lightning NDC Circuit Breaker	Hawker Siddeley Switchgear	600	0.005	100	0.75	6	125	77
Lightning NDC Circuit Breaker	Hawker Siddeley Switchgear	600	0.005	100	0.75	8	125	77
Lightning NDC Circuit Breaker	Hawker Siddeley Switchgear	620	0.005	100	1.5	4	100	77
Lightning NDC Circuit Breaker	Hawker Siddeley Switchgear	640	0.005	20	1.5	6	100	77
Arc Chute 81, HPB45	Secheron	108	Not available	20	0.9	4.5	125	78
Arc Chute 81, HPB60	Secheron	126	Not available	20	0.8	6	125	78
Arc Chute 82, HPB45	Secheron	119	Not available	15	1.8	4.5	80	78
Arc Chute 82, HPB60	Secheron	137	Not available	15	1.8	6	80	78
Gerapid 2607, Arch chute 1x2	GE	120	Not available	20	1	2.6	50	79
Gerapid 2607, Arch chute 1x4	GE	120	Not available	20	2	2.6	35	79
Gerapid 2607, Arch chute 2x2	GE	160	Not available	20	2	2.6	71	79
Gerapid 2607, Arch chute 2x3	GE	160	Not available	20	3	2.6	35	79
Gerapid 2607, Arch chute 2x4	GE	160	Not available	20	3.6	2.6	30	79
Gerapid 4207, Arch chute 1x2	GE	120	Not available	20	1	4.15	50	79
Gerapid 4207, Arch chute 1x4	GE	120	Not available	20	2	4.15	35	79
Gerapid 4207, Arch chute 2x2	GE	160	Not available	20	2	4.15	71	79
Gerapid 4207, Arch chute 2x3	GE	160	Not available	20	3	4.15	35	79
Gerapid 4207, Arch chute 2x4	GE	160	Not available	20	3.6	4.15	30	79
Gerapid 6007, Arch chute 1x2	GE	150	Not available	20	1	6	50	79
Gerapid 6007, Arch chute 1x4	GE	150	Not available	20	2	6	35	79
Gerapid 6007, Arch chute 2x2	GE	165	Not available	20	2	6	56	79
Gerapid 6007, Arch chute 2x3	GE	165	Not available	20	3	6	35	79
Gerapid 6007, Arch chute 2x4	GE	165	Not available	20	3.6	6	Not available	79
Gerapid 8007, Arch chute 1x2	GE	190	Not available	20	1	8	50	79
Gerapid 8007, Arch chute 2x2	GE	210	Not available	20	2	8	50	79

4.2.2 EMCBs Applied to Superconducting Systems

Several instances of superconducting circuit breakers or switches are available in the literature. Engineers at the Tokyo Electric Power Company have designed and developed a DC current-limiting circuit breaker with a superconducting fault-current limiter (Ref. 80). Their project involved a SFCL with a puffer-type DC circuit breaker in liquid nitrogen. They tested the DC circuit breaker design at varying voltages and fault currents to determine the mechanical limitations of the circuit breaker with and without the puffer operation. Figure 26 and Figure 27 show that the puffer increases the operating voltage, reduces the fault interruption time, and increases the fault current that can be interrupted successfully. The fault interruption time of approximately 10 to 20 ms is similar to other DC circuit breakers that use air only as a dielectric. This study shows that it is feasible to use LN_2 as a dielectric for a mechanical circuit breaker.

The theory for scaling a superconducting switch has been developed by researchers at CERN (Ref. 81). Researchers there have a need to extract the energy from a superconducting magnet when it quenches to limit the heat generated by the event. For their application, the switch connected in series with the superconducting magnet can be superconducting or normally conducting. The switch is in parallel with a dump resistor. An illustration of an example superconducting switch for this application is

shown in Figure 28. A superconducting switch may reduce the heat lost due to removal of the interface of the superconductor to a higher temperature environment during nominal operation. If the switch operated at a higher temperature, the large currents in the circuit would flow from the superconducting to conventionally conducting environments. For a superconducting switch, the leads to the higher temperature environment only need to conduct during discharge of the superconducting magnet energy. The RTAPS architecture has the objective to eliminate conductor leads between superconducting and normally conducting environments. Such a superconducting switch could be used as a mechanical circuit breaker or a hybrid circuit breaker. As a hybrid circuit breaker, the superconducting switch would be used to commutate the fault current to the solid-state circuit which dissipates the fault energy.

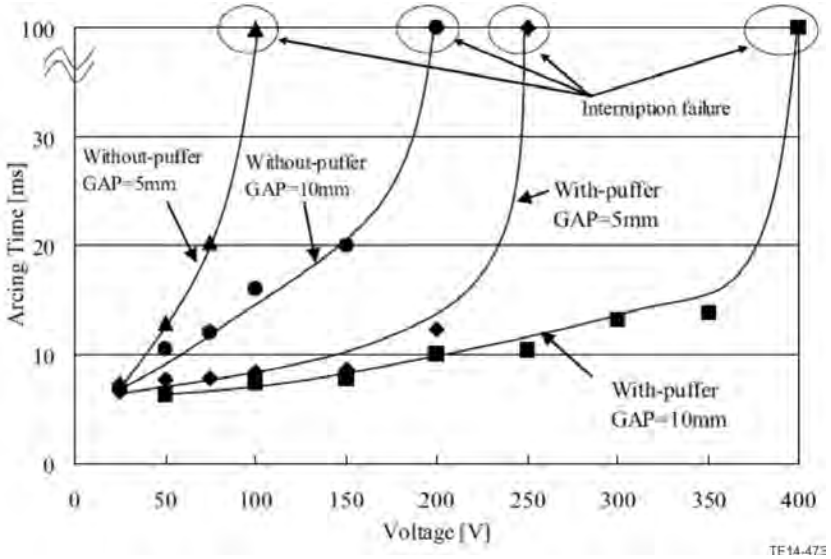


Figure 26.—Fault Interruption Time versus Voltage for LN_2 DC Circuit Breaker (Ref. 80).

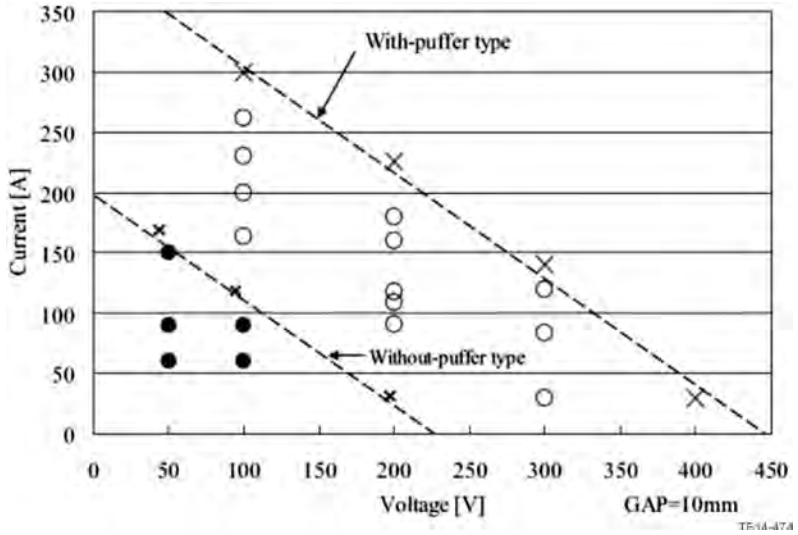


Figure 27.—Fault Interruption Current versus Voltage for LN_2 DC Circuit Breaker (Ref. 80).

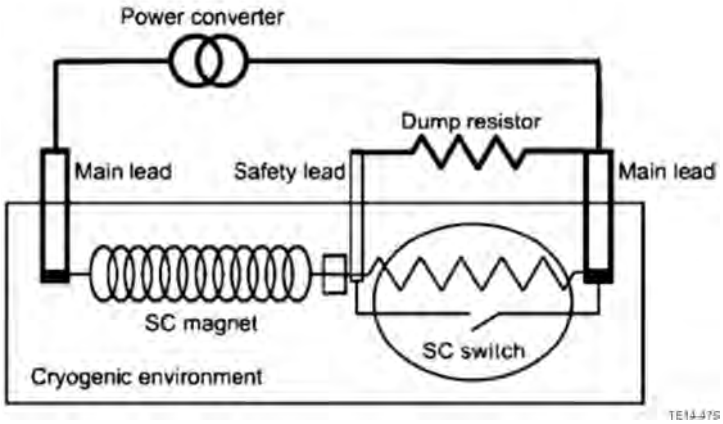


Figure 28.—Basic Circuit for Superconducting Switch to Divert Superconducting Magnet Discharge Current to a Dump Resistor.

The superconducting switch would be a metal matrix or on a metallic substrate. The study in Reference 81 discusses switch scaling based on superconducting material, rated nominal voltage and current, fault current, and energy dissipation requirements. The minimum mass required for the superconducting switch is determined by the energy that must be absorbed by the switch.

The switch is triggered from a superconducting state to a resistive state by raising the temperature, current density, or magnetic field. To maximize efficiency, the temperature is likely to be held as constant as possible within the ratings of the cryocooler, and there may not be a means of pulsing a magnetic field by the switch. For this scenario, the switch can be designed to transition to a resistive state due to increased current density in a similar fashion as a resistive SFCL. The CERN study discusses using discharge capacitors to create a large current pulse.

The study outlines an approximate mass estimate for the switch based on energy, current, voltage, superconductor density, engineering current density, resistivity, and energy absorption capability. (Ref. 81) This mass estimate is characterized as

$$M_s \geq \sqrt{\frac{E_o I_0 V_o \upsilon \sigma^2}{J_{eng}^2 \rho C_T}}$$

where

M_s mass of switch wire and cable (kg)

E_o energy stored in circuit (J)

I_0 maximum current in main circuit (A)

V_o maximum voltage to discharge into resistor (or other energy dissipation device) (V)

υ density of switch cable (kg/m^3)

σ safety factor to ensure sufficient margin for cable cross section $A = \frac{\sigma I_0}{J_{eng}}$

J_{eng} engineering current density limit in switch (A/m^2)

ρ resistivity of materials in switch conductor (Ω·m)

C_T specific energy of switch for energy that can safely be absorbed (J/kg)

For an MgB_2 superconductor (critical current at 39 K), the study proposes a Cu-Ni conductor for the switch matrix. Considering the conductor properties of this switch, one can use the following estimates for the parameters (Ref. 81):

$\upsilon = 8\times10^3$ kg/m^3
$\sigma = 1.5$
$J_{eng} = 10^9$ A/m^2 (for 2035 time frame)
$\rho = 50\times10^{-8}\,\Omega\cdot$m (stainless steel and copper-nickel matrix)
$CT = 40\times10^3$ J/kg (for operation up to 250 K)

Given these assumptions, the mass of the superconducting switch can be estimated based on the energy dissipation requirement, current, and voltage. To size a superconducting switch on one of the four main TeDP distribution lines connecting each generator to a feeder bus (rated for 50 percent of minimum takeoff power = 12.5 MW), and assuming an interruption time of 1 ms (for a hybrid circuit breaker response time), the energy that must be dissipated by the switch is 12.5 kJ. This is merely an approximation of the energy for this example. A transient analysis of the fault current and inductance for faults at various locations on the architecture is required to determine the energy dissipation requirement and the appropriate protection system fault detection and response time in order to minimize the mass of the protection equipment or meet some other objective. Given this assumption, the mass of the switch can be estimated as:

$$M_s \geq \sqrt{\frac{E_o I_0 V_o \upsilon \sigma^2}{J_{eng}^2 \rho C_T}}$$

$$M_s \geq \sqrt{\frac{11.2\times10^3 \times I_0 V_o \times 8\times10^3 \times 1.5^2}{(10^9)^2 \times 50\times10^{-8} \times 40\times10^3}}$$

$$M_s \geq 1.004\times10^{-4}\sqrt{I_0 V_0}$$

For the fixed power of 12.5 MW, the switch mass is estimated as 0.34 kg. However, the maximum current and voltage will differ from the steady-state power requirement. Figure 29 shows the switch mass estimate for a voltage range of 2.5 to 40 kV and current range of 280 to 4480 A. The switch mass ranges from 0.084 to 1.344 kg.

If the fault interruption time is longer as is typical for electromechanical circuit breakers (10 ms), then the fault energy increases proportionally (125 kJ). For the fixed power of 12.5 MW, the switch mass for this increase in fault energy increases more than three times to 1.06 kg.

4.3 Hybrid Circuit Breakers

There are many different topologies of HCBs. In essence, each includes a mechanical switch to commutate the current into the solid-state device that is in parallel with the switch. The solid-state device is used to dissipate or store the energy in the arc. The mechanical switch must be rated to carry the nominal and fault current and should be designed to have a low on-state resistance. The solid-state devices are used for current conduction for a short time and can be rated to just the interrupted fault current. Some topologies are depicted in Figure 30, Figure 31, and Figure 32.

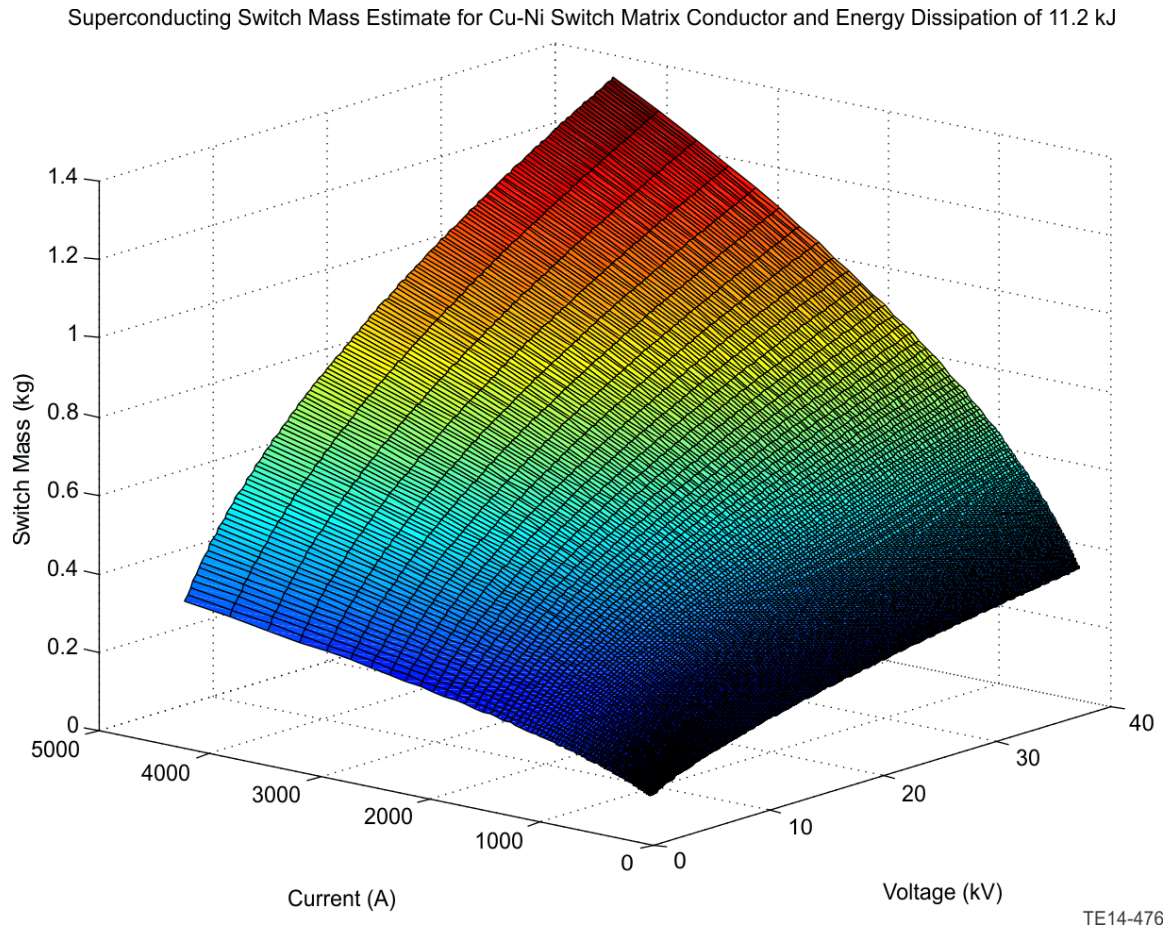


Figure 29.—Superconducting Switch Mass Estimate for Fixed Energy Dissipation Requirement.

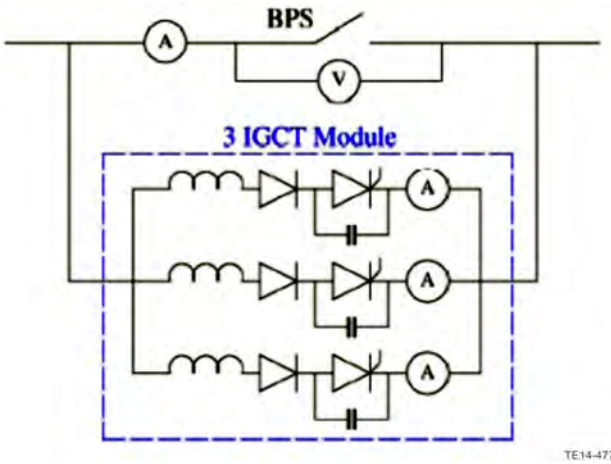


Figure 30.—Simplified Schematic of HCB with IGCTs Prototype (Ref. 82).

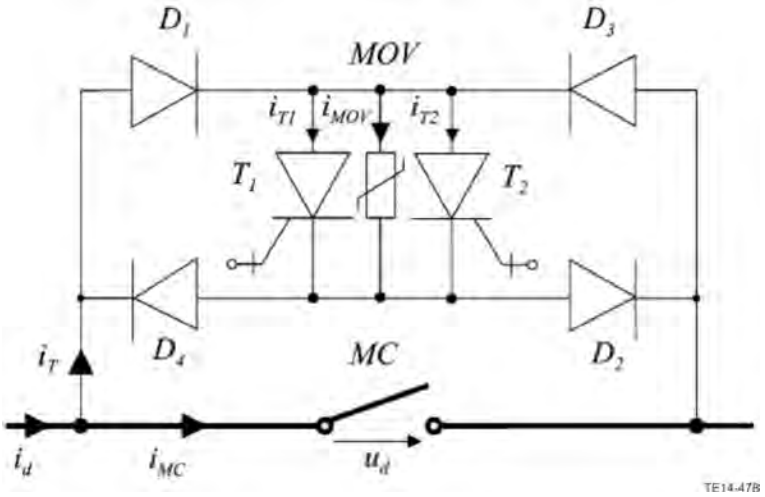


Figure 31.—Simplified Schematic of HCB using IGCTs and Metal-Oxide Varistor (Ref. 83).

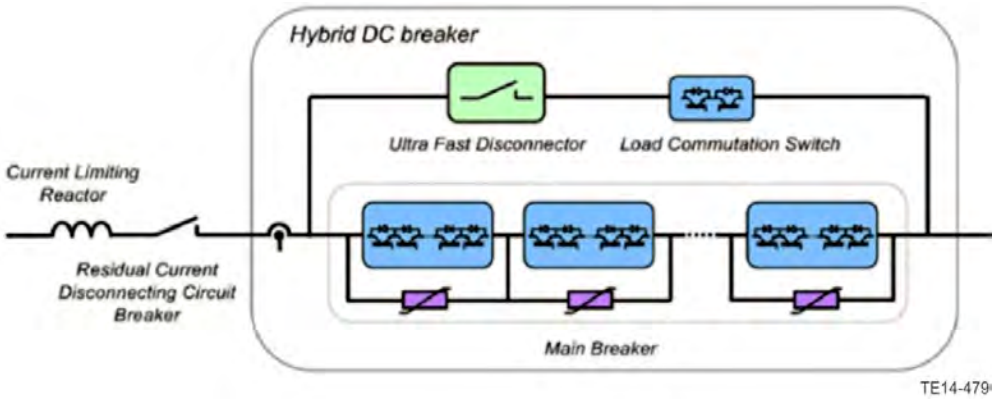


Figure 32.—Schematic of HCB for HVDC using IGBTs (Ref. 84).

The circuit breaker in Reference 82 consists of several conducting paths in parallel and a bypass switch (BPS). The BPS was rated for 70 kA nominal current and 17.5 kV nominal voltage and is opened by a pneumatic actuator. The BPS arc voltage is low for the paper's application in a superconducting magnet system. This posed problems for the current commutation from the bypass switch to the circuit breaker. Three paralleled IGCTs with snubbers and voltage clamps were used to form the circuit breaker due to their controllability at turn-on and turn-off and ability to interrupt large currents. Each conduction path of this circuit breaker is composed of an inductor (required for IGCT turn-on protection to limit the rate of current rise), diode, IGCT, and current measurement device. Both studies in References 83 and 84 investigate and use Thomson drives for fast opening times of the mechanical switch.

While mass data is not published for these HCBs, the existing IGCT and IGBT component mass as well as other characteristics, such as conduction resistance, are available. Approximations of the mass for the other components in the hybrid circuit breaker can be made in order to estimate the hybrid circuit breaker weight. Available data for several hybrid circuit breaker implementations and IGBT and IGCT components is tabulated in Table 11. Additionally, the table includes a solid-state circuit breaker prototype for comparison with the HCBs. This data is developed for IGBT or IGCT operation at 25 to 125 °C. An understanding of the semiconductor at cryogenic temperatures (4 to 70 K) is required in order to estimate conduction resistance, blocking voltage, and turn-on and turn-off times for cryogenic electrical system protection. This discussion is included in Section 3.5.

TABLE 11.—HCB, SSCB, AND IGBT AND IGCT COMPONENT DATA

Device name	Developed by	Use	Weight, kg	Conduction resistance at rated current, mΩ	Peak off-state current, mA	On-state voltage, V	CB turn-off (component turn-on) operating time, ms	Rated blocking voltage rating, kV	Normal operational current rating, kA	Fault current rating, kA	Ref.
Hybrid DC CB	European Atomic Energy Community (EUATOM)	Quench protection of superconducting magnets	Not available	75.00	Not available	24	8	2.8	4	10	82
DC hybrid CB with ultra-fast contact opening and IGCTs	ABB	Railway electrical system	Not available	1.00	Not available	5	0.3	2.5	4	5.7	83
Hybrid HVDC CB	ABB	HVDC VSC Protection	Not available	Not available	Not available	Not available	0.2	80	2	8.5	84
Solid-State CB with Six Series-Connected IGBTs	Diversified Technologies	Naval power system	27.2	11.25	10	9	0.0045	10	0.8	1	85, 86
ABB HiPak IGBT Module 5SNA 1200G450300	ABB	Hybrid DC circuit breakers	1.76	2.17	0.0005	2.6	0.00098	4.5	1.2	2.4	87
IGCT module - 5SHX 26L4520 (Reverse Conducting IGCT)	ABB	Hybrid DC circuit breakers	2.9	1.27	50	2.6	0.007	2.8	1.01	2.2	88

From Table 11, there are several differences among the technologies to note. The conduction resistance for IGBTs is higher than for IGCTs. This may become significant at higher fault current levels but is dependent on the component operation at cryogenic temperatures. The IGBT component weight is less than the IGCT weight, where the IGBT has comparable fault current interruption capability but higher blocking voltage rating. This may be beneficial to reduce the solid-state component weight when using several components in series or parallel. The IGBT turn-on time is faster than the IGCT time, but at cryogenic temperatures the times may differ.

4.4 Solid-State Circuit Breakers

There are several solid-state circuit breaker designs, but few with published mass and efficiency data and testing data for higher voltage and current operation. One example with mass estimate and transient opening and closing data was developed by Diversified Technologies for naval power systems (Ref. 85). They developed and tested a solid-state circuit breaking using six 4.5 kV IGBTs (CM900HB-66H) connected in series. Figure 33 and Figure 34 illustrate the physical layout and the simplified SSCB diagram. The published mass estimate for the solid-state circuit breaker was 27.2 kg (60 lb). Looking up the Mitsubishi Electric high-voltage IGBT data sheets, each IGBT weighs 1.5 kg. For six IGBTs, the IGBTs account for approximately 9 kg (33 percent of total weight). That leaves an additional 18.2 kg (67 percent) for the additional structural components as well as snubbers and other circuit components. Additional discussion about cryogenic operation of IGBTs and characteristics of IGBTs is included in Section 3.5.

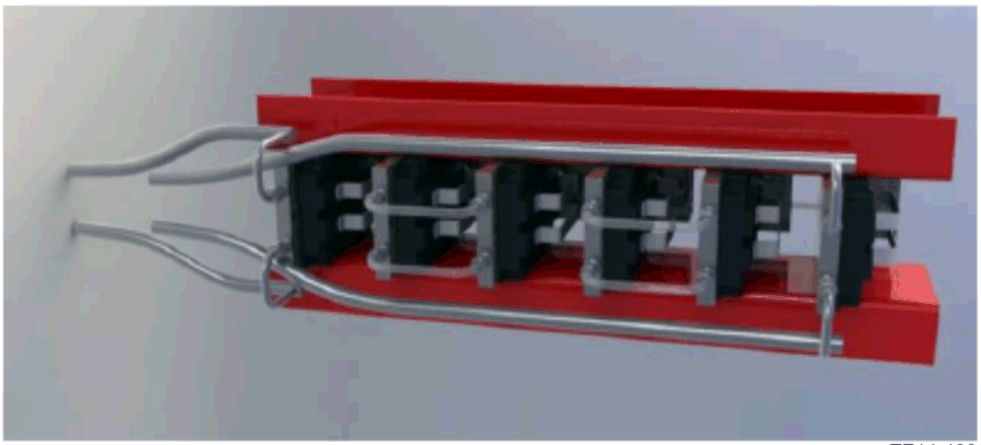


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Figure 33.—A 10 kV, 800 A IGBT Solid-State Circuit Breaker Mechanical Layout (Ref. 85).

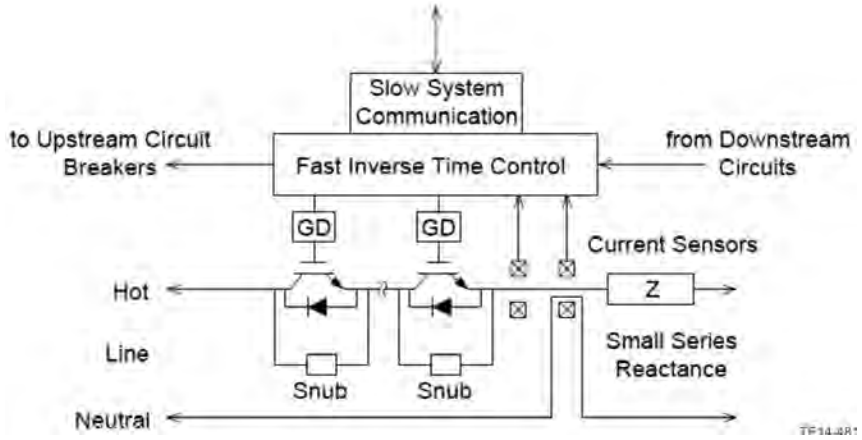

Figure 34.—Simplified Diagram of Example Solid-State Circuit Breaker (Ref. 85).

Referring to Table 11, there are several notable differences between HCBs and SSCBs. The conduction resistance of SSCBs is generally higher than that for HCBs due to the lower resistance of the mechanical switch for HCBs. As mentioned previously, the turn-on (current interruption) time for the SSCBs is significantly faster than for HCBs in large part due to the operation of the mechanical switch for the HCBs. Practical implementation of the protection and control system that enables fault detection and discrimination fast enough to utilize the fast interruption time of SSCBs is difficult. The transient fault response for the electrical system architecture will determine whether or not the protection system weight can be significantly reduced by using SSCBs and their associated faster fault interruption time.

TABLE 12.—DC PROTECTION DEVICE SUMMARY

Characteristic/Device	EMCB	HCB	SSCB
Operating time	–	o	+
Weight	–	o	+
Conduction resistance	+	o	–
Cryogenic operation	o	+	+

4.5 Summary

The major properties of DC protection devices including weight, conduction resistance, fault current interruption capability, and fault interruption time were presented based on available data. Further assessment can be done to estimate EMCB, HCB, and SSCB weight for varying fault current interruption and blocking voltages based on IGBT or IGCT component weights and estimating additional CB component weights such as inductors, contactors, and arresters. The summary of the discussion in this section is shown in Table 12. The + symbol indicates a benefit, o indicates a neutral or minor benefit, and – indicates a negative attribute for application to a superconducting TeDP protection system.

For the sensitivity and dynamic modeling, SSCB were used to eliminate fault conditions quickly and had a compact package. If the devices operate early or late in the fault condition the amount of fault current that it is required to interrupt is decreased significantly which will reduce the size of the circuit breaker. The longer a fault persists on the network increases the amount of energy that the cryocooler will have to absorb increasing the size and mass of the system. These two reasons imply that interrupting a fault early in the cycle is the preferred option to reduce size and weight. The coordination between the superconducting fault current limiter and circuit breakers can be explored using the dynamic model. If the superconducting fault current limiter can restrict the peak of the fault current to non-damaging levels than slower circuit breakers may be used but the prolonged fault condition will result in a larger cooling system.

5.0 Component Sensitivities and Sensitivity Modeling

5.1 Component Sensitivity Overview

The impact of operating voltage at the system level is dependent on its integrated effects on all system components. In order to determine the sensitivity of the TeDP architecture to operating voltage, mass and efficiency sensitivities of each system component must be characterized. Parametric sensitivity models were developed for TeDP components.

This section outlines the methods employed for determining component voltage sensitivity. Important assumptions are highlighted and the driving factors behind sensitivity trends are discussed. Component sensitivity models reviewed in this section are:

- Converters
  - Unidirectional current source converter
  - Bidirectional current source inverter
- Superconducting cables
- Superconducting magnetic energy storage
- Solid-state circuit breaker
- Superconducting fault current limiter

The component I/O was determined considering the overall system requirements, system sensitivity variable, component design parameters and interactions between components and systems. The relationships are indicated via the colored arrows in Figure 35. The weight and efficiency for each component is determined as a function of the input variables and internal assumptions. Additionally, the component losses and temperature at which the heat is removed determines the heat quality factor illustrated in Figure 35.

Component specific parameter diagram will be given with the discussion of each TeDP component model to illustrate the parameters used in its model.

The power requirement and component count for each architecture discussed in Section 2.0 is provided in Table 13. This component breakdown is modified from the breakdowns presented in the August 2012 Rolls-Royce RTAPS final report (Ref. 89). The architectures considered here have 16 propulsors instead of 14. The nominal power requirements for the components are scaled accordingly. The nominal current rating for the each grid component is determined by the power rating and the operating voltage for each component.

The max operating current for each device requires more information regarding the manner in which the protection equipment is configured to mitigate overcurrents during electrical system failures. The identification of the sizing current requirements will be discussed in the subsequent sections.

Table 13 gives a high level decomposition of the architecture. However, component sizing requires a decomposition of the architecture to lower levels of abstraction. Each component is an assembly of subcomponents which contribute to the overall weight and component efficiency.

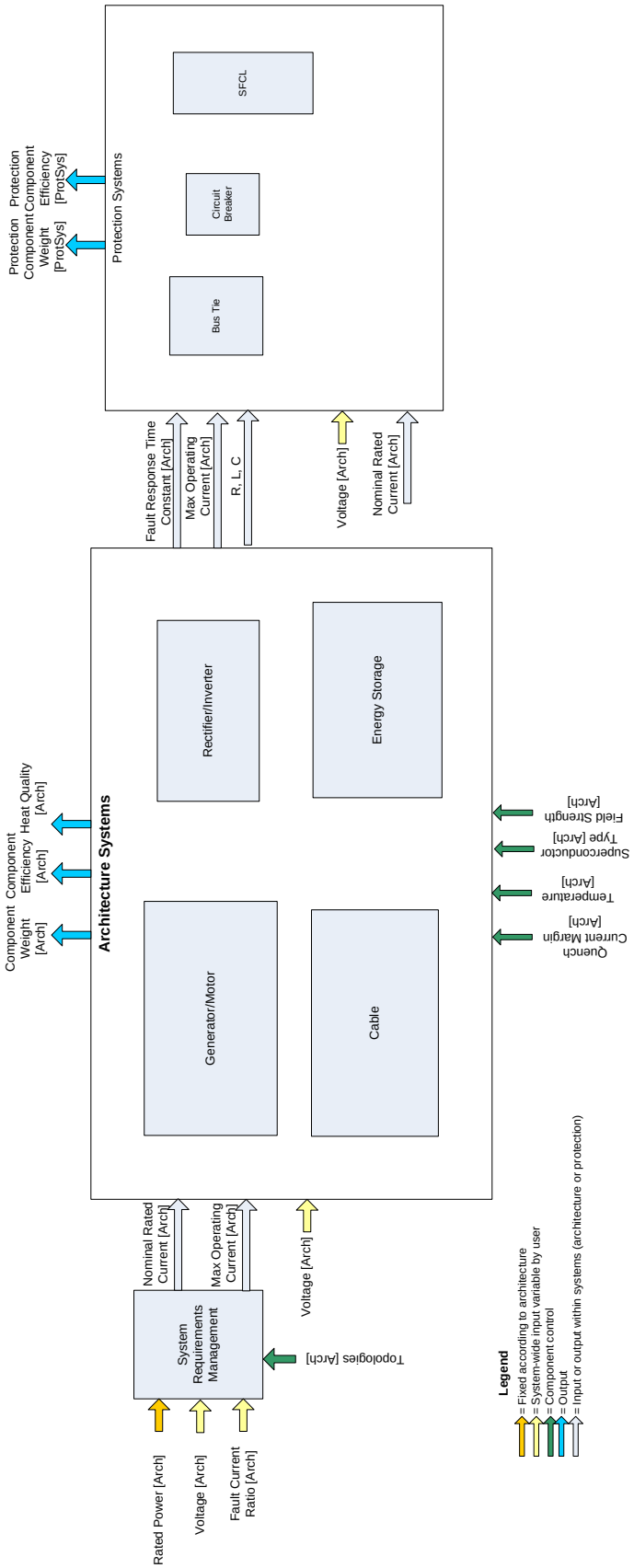

Figure 35.—Overall System Parameter Diagram with Legend for Arrow Colors.

TABLE 13.—ARCHITECTURE COMPONENT BREAKDOWN

Components		Arch1: Baseline		Arch2: Inner bus tie		Arch3: 3-bus multi-feeder		Arch4: Cross-redundant multifeeder		Arch5: 4-bus inner bus tie, multifeeder	
		Count	Rating, MW	Count	Rating, MW	Count	Rating, MW	Count	Rating, MW	Count	Rating, MW
Electric Machines	Generator	4	11.19	4	14.91	4	11.19	4	11.19	4	11.19
				2	7.46						
	Motor	16	2.80	16	1.86	16	1.60	16	1.60	16	1.60
Converter	Unidirectional AC/DC Converter	4	11.19	2	14.91	4	11.19	4	11.19	4	11.19
				2	7.46						
	Bidirectional DC/AC Inverter	16	2.80	16	1.86	16	1.60	16	1.60	16	1.60
	DC/DC Converter for SMES	4	11.19	2	14.91	4	11.19	4	11.19	4	11.19
				2	7.46						
Cables	Transmission	4	11.19 (2- by 30-m, 2- by 40-m)	2	14.91 (1- by 30-m, 1- by 40-m)	4	11.19 (2- by 30-m, 2- by 40-m)	4	7.46 (2- by 30-m, 2- by 40-m)	4	11.19 (2- by 30-m, 2- by 40-m)
				2	7.46 (1- by 30 m, 1- by 40 m)			4	3.73 (2- by 30-m, 2- by 40-m)		
	Feeder	16	2.80 (16- by 5-m)	16	1.86 (16- by 5-m)	16	1.60 (16- by 5-m)	16	1.60 (16- by 5-m)	16	1.60 (16- by 5-m)
						16	1.20 (16- by 5-m)	16	0.80 (16- by 5-m)	16	1.20 (16- by 5-m)
Breakers	AC	4	11.19	4	14.91	4	11.19	4	11.19	4	11.19
				2	7.46						
		16	2.80	16	1.86	16	1.60	16	1.60	16	1.60
	DC	8	11.19	4	14.91	8	11.19	8	7.46	8	11.19
				4	7.46			8	3.73		
		32	2.80	32	1.86	32	1.60	32	1.60	32	1.60
						32	1.20	32	0.80	32	1.20
				1	7.46					1	9.60
SFCL	AC	4	11.19	2	14.91	4	11.19	4	11.19	4	11.19
				2	7.46						
		16	2.80	16	1.86	16	1.60	16	1.60	16	1.60
	DC	4	11.19	2	14.91	4	11.19	4	7.46	4	11.19
				2	7.46			4	3.73		
				1	7.46					1	9.60
Energy Storage	SMES	4	11.19	2	14.91	4	11.19	4	11.19	4	11.19
				2	7.46						

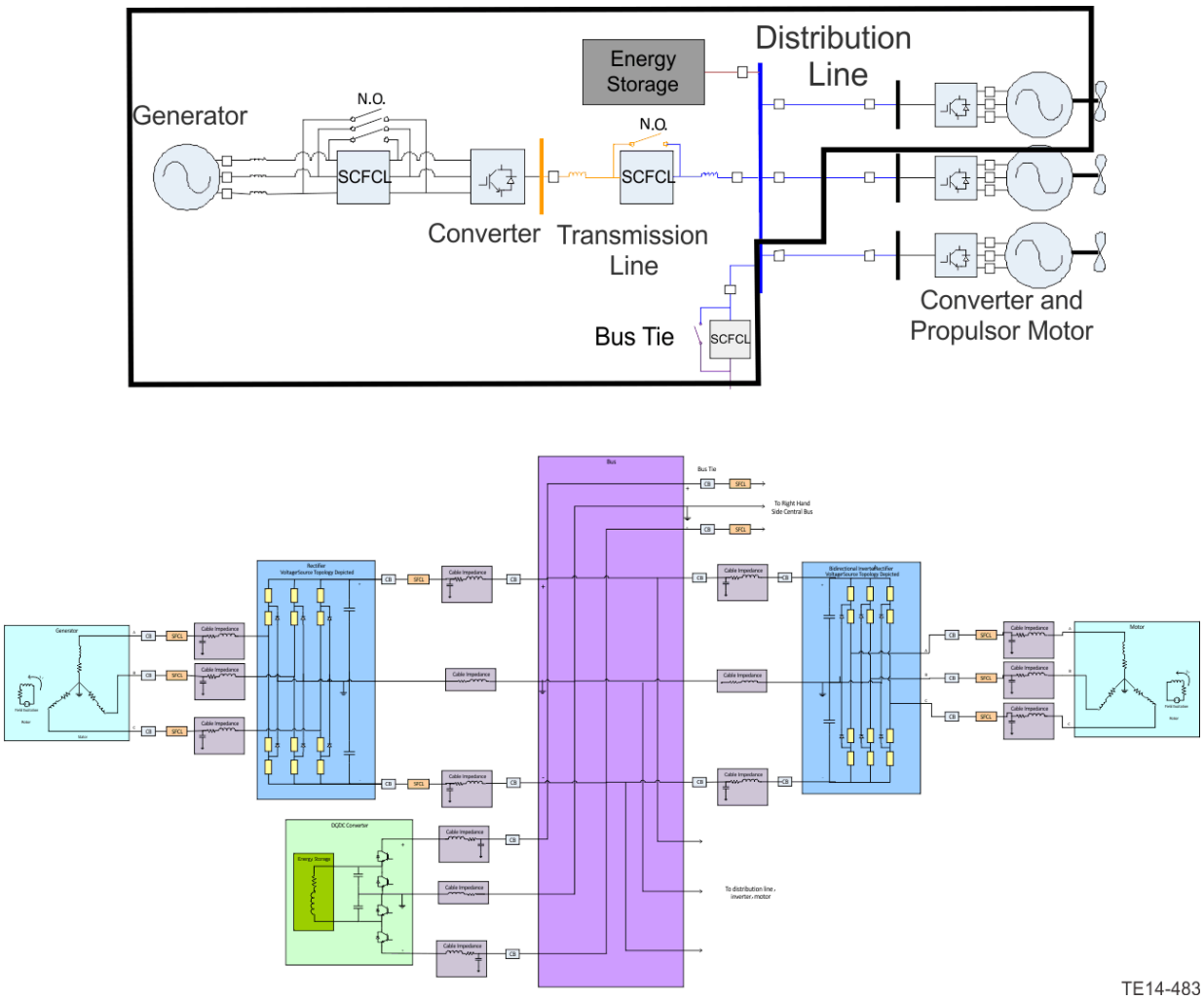

Figure 36.—Circuit Diagram for One Generation, Rectification, Distribution, Inversion, to Propulsor Motor Load Line. In Addition, an SMES Energy Storage Device and Connections to Other Feeders and the Bus Tie Connection to a Secondary Distribution Line are Illustrated.

Figure 36 illustrates this decomposition to a lower level of abstraction for the section of the architecture indicated in the black box.

It should be noted that the decompositions illustrated in this figure assume specific converter topologies. This figure illustrates a unidirectional voltage source converter for the AC/DC converter as well as a bidirectional voltage source converter for the propulsor drive. Additionally, the DC/DC converter for the SMES is simply representative. Discussion on alternative converter configurations and the specific sensitivity models generated for this study can be found in Section 5.2.

5.2 Rectifier and Inverter

This section describes the models of all of the rectifiers and inverter/rectifiers used in this architecture. First, the major inputs, outputs, and internal parameters for a system study using one or more of these power converters are described. Then, the selected topology and other considered topologies are discussed. The rectifier model and its major components are described in detail with significant model trends presented and discussed. The major components used in the converter models are also used in the solid-state circuit breaker model. Lastly, the bidirectional model trends are presented and discussed.

5.2.1 Model Overview

5.2.1.1 Parameter Diagram

The system-level power converter model is described by the parameter diagram shown in Figure 37. For the fixed architecture, the rated power is fixed and is indicated as an input to the model. Inputs to the model that can be varied are the DC voltage, electrical AC frequency, and power factor. The controls indicated in green are the converter topology, switch type, switching frequency, DC ripple voltage, and DC ripple current. For this study, the topology and switch type are fixed, but the model could be expanded to include system studies of different topologies. Outputs of the model indicated in blue are the converter mass, heat quality (losses), efficiency, and optionally harmonic content. At this stage, the harmonic content will not be computed. The intermediate outputs that are sent to the protection system to determine the protectiond device requirements are the converter fault current rating, current interruption time, equivalent capacitance, and equivalemtn arm inductance. Additional intermediate outputs from the converter to other subsystems such as the cable model are the AC voltage and AC current as determined by the converter specified power, DC voltage, and power factor. These identified parameters were used to structure the model and determine interactions with other subsystems.

5.2.1.2 Converter Topology

Several converter topologies were brainstormed before choosing a specific topology for which to model. With the converter AC conductor interface described by a three-phase system and the DC conductor interface described by a bipolar DC system with ground point, neutral (or mid) point clamped topologies were considered. This DC bus configuration is also called a three-level (or generically multilevel) configuration since it involves defined and controlled positive, grounded, and negative potentials. The traditional voltage-source mid-point clamped topology as shown in the system circuit diagram of Figure 37 was considered. This voltage-source converter (VSC) topology is widely studied and is the most common implementation of low and high power inverters and rectifiers. However, while studying and considering the design of this superconducting DC microgrid protection system (Ref. 90), the current-source converter (CSC) topology was also considered (Ref. 91). The CSC topology and switch module options will be discussed further in Sections 5.2.2 and 5.2.4. Figure 38 shows several switch module circuit options for use with the VSC. Each of these circuits would be used where each yellow rectangle is drawn in the VSC of Figure 36. Figure 38(a) shows a GTO used as the switching device with an antiparallel diode (Ref. 92). The GTO can be turned on and off (unlike an SCR) and has long turn off times (on the order of 15 μs). Figure 38(b) shows an IGBT used as a switching device with an Emitter Turn-Off Thyristor (ETO) and Metal Oxide Varistor (MOV) in parallel (Ref. 93). The ETO provides the switching module the ability to limit or interrupt current, and the MOV is used for overvoltage protection of the IGBT and ETO. Figure 38(c) shows a simple IGBT with antiparallel freewheeling diode. This switch topology cannot limit current and lacks overvoltage protection.

The VSC switch chosen impacts the converter current-limiting capability. The VSC switches are controlled as a converter to regulate the specified DC bus voltage. During the onset of a DC bus pole-to-pole fault, the large DC bus capacitor current is discharged into the short circuit (Ref. 94). If the fault current magnitude can be limited, then the fault current withstand rating of the affected protection zone can be reduced, which potentially reduces the mass of the components. VSCs with current-limiting switch modules such as that of Figure 38(b) or CSCs. The CSC topology is essentially the dual of the VSC topology. Where capacitors are used to store energy for a CSC and regulate voltage, inductors are instead used for a CSC to store energy and regulate current. This control inherently limits current.

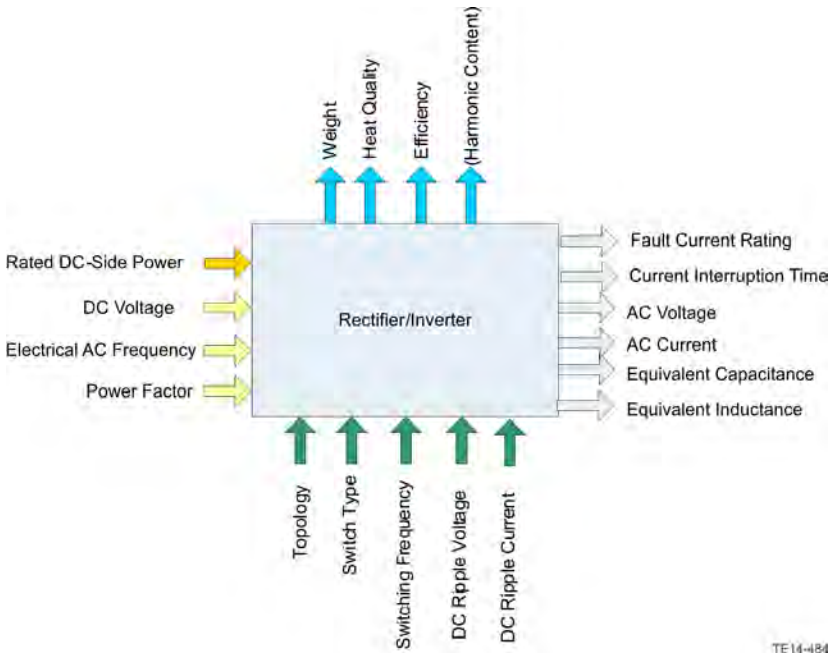

Figure 37.—Parameter Diagram for Power Converter.

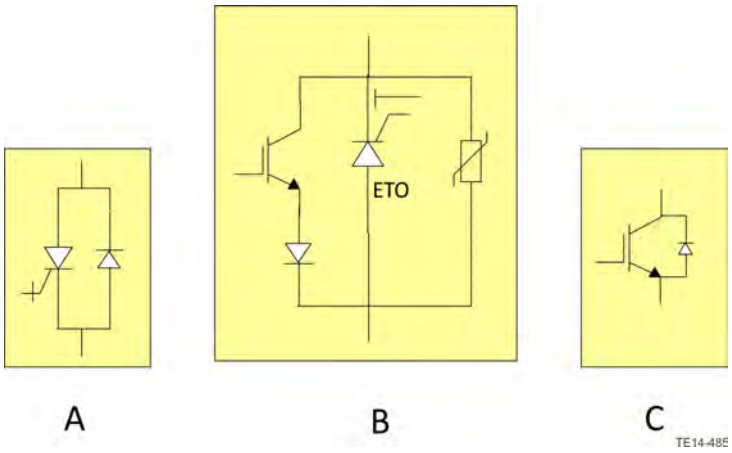

Figure 38.—Potential Switch Topologies for a Voltage Source Converter. Not Modeled in Current Study; Current-Source Converters Were Selected To Be Modeled.

Additionally, if the duration from the onset of the fault to the peak fault current magnitude be lengthened, this allows more time to detect the fault, discriminate the fault location, and interrupt and isolate the faulted section of the network. This can be accomplished with current control or the addition of inductance or resistance in the circuit such as with the use of a fault-current limiter.

Converter topologies that can be controlled to limit and interrupt current may reduce the mass of the protection devices. However, current-limiting converters make the detection and discrimination of a short circuit fault more difficult. Algorithms and analysis of the detection and discrimination of these faults for compact DC networks are discussed in Reference 95.

A comparison of VSCs and CSCs is listed in Table 14. For this system model, the CSC topology was chosen over the VSC due to the inherent current-driven nature of a superconducting network enabled by high current density of superconducting material. Additionally, it is desired to study the impact of the current-limiting capability of the CSC on the protection device weight and system efficiency.

TABLE 14.—COMPARISON OF VSC AND CSC (REFS. 96, 97, AND 98)

Comparison	Current-source converter	Voltage-source converter (dual of CSC)
Control	Current, voltage varies with power	Voltage, current varies with power
Reverse power flow	Voltage changes polarity	Current changes polarity/direction
Short-circuit fault tolerance	Tolerant	Susceptible, requires short circuit interruption protection
Open-circuit fault tolerance	Susceptible, requires emergency current path	Tolerant
Efficiency	Less efficient	More efficient
Harmonics	More harmonics, so larger filter required	Fewer harmonics
Switch bidirectional rating	Bidirectional voltage blocking	Bidirectional current blocking
Semiconductor rating	Semiconductors rated for full AC voltage	Semiconductors rated for full AC current

As part of the system study, additional converter models could be developed (VSC and CSC), and the sensitivity of the converter topology and impact on system weight and efficiency could be assessed.

5.2.2 Source-Side Converters

With the assumption that the current-source converter is the appropriate converter topology for the superconducting power distribution system, there are several configurations of the CSC depending on the direction of power flow. The higher power CSCs that convert the generator AC voltage to distribution DC voltage only require power flow in one direction (i.e., AC to DC). This simplifies and reduces the component count of the switch modules so that the switch modules are designed to only carry current in one direction. For a CSC, this is a half bridge configuration of the switching devices. The lower power CSCs that normally convert the distribution DC voltage to motor AC voltage may require power to flow in both directions (i.e., DC to AC or AC to DC). Such a scenario where power flows from the AC to DC side of the converter is in the case of the propulsor “windmilling” and turning the electric machine so that it acts like a generator and can send power to the SMES or other loads. For this scenario, the switch modules require more components so that the converter can carry current in either direction. For a CSC, this is a full bridge configuration of the switching devices and requires twice the number of switching devices compared to a half bridge.

First, the higher power unidirectional current source rectifier, scaling equations, and model trends will be presented, followed by the same discussion of the bidirectional current source converter. The converter current and voltage rating equations apply to both the unidirectional and bidirectional converters, but the component voltage and current ratings for the topologies slightly differ. These differences are indicated by referring to the switch modules as half bridge (unidirectional) or full bridge (bidirectional) configurations. The scaling of each of the converter individual components (IGBT and diode, capacitor, inductor, and housing) are the same for both topologies.

5.2.2.1 Unidirectional Current Source Rectification

The topology of the unidirectional current source rectifier is shown in Figure 39. The major components of this converter are the switching modules indicated by the yellow rectangle, capacitors, and clamping diodes. For nomenclature, the series or parallel configuration of the switching modules connected from a phase to the positive or negative terminal is called an arm.

Within a switching module, several unidirectional topologies can be chosen. Some options considered are shown in Figure 40. Note that major differences between these current-source and voltage-source converter switch modules (shown in Figure 36) are that the devices are aligned in series, inductors are required to maintain a current path and store energy, and the IGBTs are paired with series diodes rather than

antiparallel freewheeling diodes. Both CSC and VSC switch modules may require a device for overvoltage protection such as an ETO or other thyristor (Figure 33(b)) or press pack diodes (Figure 40(c)). Each switch module may also require a capacitor rather than a lumped arm capacitor as shown in Figure 39. The trends developed from these models are derived from a lumped arm capacitor. Further studies could be done to assess the capacitor mass for a capacitor per each switch module rather than a lumped capacitor. The topology boxed in red (Figure 40(c)) was chosen for this study due to the suggestion of the use of press pack diodes (Ref. 99) and the ease of scaling and modeling them over thyristors.

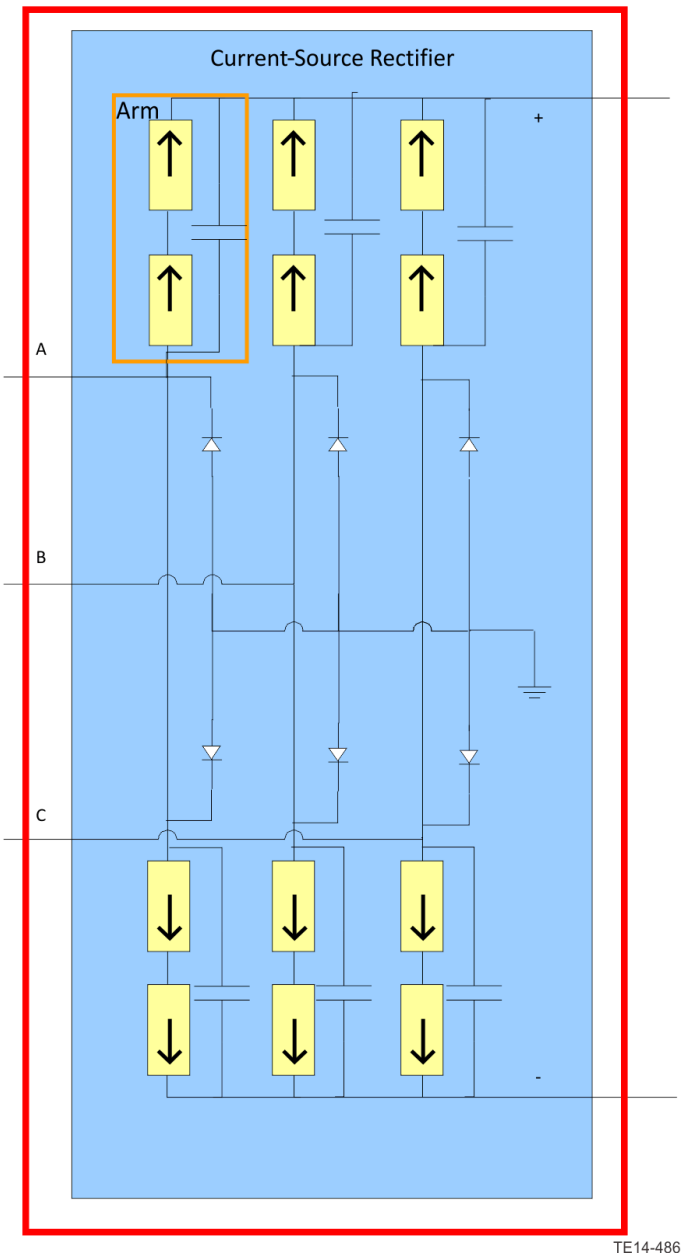

Figure 39.—Unidirectional, Current-Source Converter Topology Selected for the Power Generator Rectifier. The Yellow Blocks in This Diagram Represent Potential Variations in the Switch Topologies. Note Also That the Arrow Indicates the Direction of Current Flow.

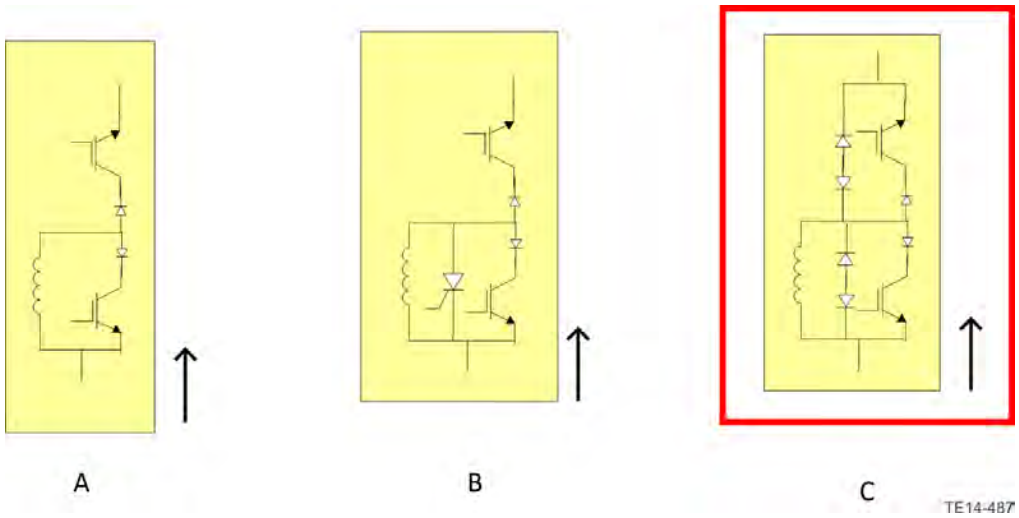

Figure 40.—Half Bridge, Unidirectional, Current-Source Converter Semiconductor Switches. Each of These Blocks Can Be Connected in Parallel to Subsequent Blocks. Topology C (Press Pack Diodes for Overvoltage Protection) Was Selected for the Switch Topology for the AC to DC Converter over Topology B (Thyristor for Overvoltage Protection) (Refs. 100 and 101).

5.2.2.2 Governing Equations

5.2.2.2.1 Converter Sizing Model

The overall converter mass and loss estimate model is used to derive the subcomponent ratings. Based on these ratings, the subcomponent weight and losses are estimated. These subcomponent weights and efficiencies are then used to estimate the overall converter mass and efficiency depending on the number of subcomponents and their configuration. The subcomponents for the power electronic devices (unidirectional rectifier, bidirectional rectifier/inverter, solid-state circuit breaker, and bidirectional DC-DC converter) are an inductor, capacitor, and IGBT with diode (series or freewheeling). The solid-state circuit breaker also includes a varistor whose weight is estimated proportionally to the IGBT weight. Further detail to estimate the mass and normal operation efficiency of a varistor or other overvoltage protection device could be added to the model to build a cryogenic scalable varistor dependent on voltage, current, interruption times, and cryogenic operation of the solid-state circuit breaker.

The overall converter mass and loss estimate is driven by the specified rated DC power, nominal DC rated voltage (pole to pole), AC side frequency, and switching frequency. Given these specifications, the converter model calculates several additional ratings. The rated DC current is simply calculated as:

$$I_{dc} = \frac{P_{dc}}{V_{dc,ptp}}$$

Where P_{dc} the specified is rated DC power and $V_{dc,ptp}$ is the nominal DC rated voltage (pole-to-pole).

The rectifier/inverter nominal peak AC current for a given rated DC current is described by the equation

$$I_{ac} = \frac{1}{\sqrt{2}} I_{dc} m \cos\theta \quad \text{(Ref. 102)}$$

Where m is the converter modulation index (between 0 and 1) and cos θ is the power factor (assuming 1 for calculations throughout this report).

The rectifier/inverter nominal peak AC voltage for a given rated DC voltage is described by the equation:

$$V_{ac} = \frac{2\sqrt{2}}{3}\frac{1}{m\cos\theta}V_{dc} \quad \text{(Ref. 103)}$$

These equations are ideal assuming that the input power equals the output power. The AC current or voltage ratings could be modified to include the converter losses through increasing the voltage or the current. The three-phase real power is calculated by the standard equation:

$$P_{3\vartheta} = \frac{3}{2}V_{ac}I_{ac}\cos\theta$$

Other inputs that can be varied that also effect the overall converter mass and lost estimate are the operating temperature, DC ripple voltage magnitude, and DC ripple current magnitude. The diode losses are calculated as a function of operating temperature. The model could also be expanded to calculate IGBT losses, inductor mass and losses, capacitor mass and losses, and heat exchanger as a function of operating temperature, but those dependencies are not currently included in the model. The DC ripple voltage magnitude is used to determine the capacitance requirements to support the DC bus voltage, and the DC ripple current magnitude is used to determine the inductance requirements for each switching module.

The capacitance requirement for the specific current-source converter topology is not analytically known but can be approximated using standard topology requirements. For a standard three-phase AC to two-level DC full-wave diode rectifier, the rectifier capacitance for voltage regulation is approximated by:

$$C_{eq} = \frac{I_{dc}}{2f_{ac}\Delta V_{dc}} \tag{1}$$

Where f_{ac} is the AC frequency and ΔV_{dc} is the peak-to-peak DC voltage ripple magnitude. Note that this topology differs in that it is actively controlled with IGBTs and the DC side has three voltage levels (mid-point clamped), so this capacitance definition is approximate across the pole-to-pole DC bus. It is apparent from this equation that the AC frequency influences the capacitance; a higher AC frequency lowers the capacitance required for the same DC bus voltage ripple and DC bus current.

Similarly, the inductance requirement for this CSC topology is not analytically known but can be approximated from standard topology theory. For the same full-wave diode rectifier with inductive filtering on the DC side, the DC ripple current is approximated by the following phasor equation at the ripple frequency $\omega = 2\pi(2f_{ac})$:

$$\tilde{I}_{DC,\text{ripple}} = \frac{2\sqrt{2V_{ac}}}{3\pi\left(R + j\omega L - \omega^2 RLC\right)} \text{ (Ref. 104)} \tag{2}$$

Where R is the DC pole-to-pole resistance, L is DC inductive filter, and C is the equivalent DC capacitive filter. This equation is adapted to the find the equivalent inductance for a specified DC current ripple by assuming that each arm for a three-phase AC side contributes to approximately one third of the total DC current ripple. With this assumption and using the quadratic formula, the arm equivalent inductance is computed.

The subcomponent ratings are determined by the overall converter specified voltages and currents. The IGBT and diode, inductor, and capacitor subcomponent masses and losses are estimated for these ratings and then totaled according to the converter topology to estimate the overall converter loss and mass. The following sections describe each subcomponent and how it is scaled.

5.2.2.2.2 IGBT and Diode Sizing Model

The cryogenic operation of the IGBTs and diodes is scaled from room temperature IGBT and diode data based on cryogenic testing and research of these devices (Refs. 105, 106, and 107). For more information on the cryogenic semiconductor device research summarized for this study, see Section 3.5.

The cryogenic scaling of the IGBT devices is derived from cryogenic IGBT test results. Proportional scaling is used based on these results discussed in Section 3.5 and Table 6. These results are based on tests 50 to 300 K. The IGBT cryogenic scaling factors used in each of the models using this device is summarized in Table 15. These scaling factors can be modified and thus improve the model estimates as further research and test results are completed to better approximate the IGBT performance as a function of temperature, voltage, current, and other factors.

The results from the dissertation research (Ref. 108) were used to approximate the cryogenic behavior of diodes as a function of temperature. The turn-on voltage increases approximately linearly as temperature falls at approximately the rate of 1.6 mV/K for a 1700 V Dynex diode module tested 50 to 300 K in 25 K increments. Based on this result, the on-state voltage is estimated by

$$V_{D,on}^{cryo} = V_{D,on}^{300K} + 0.0016\left(300 - T\right)$$

which is approximate for a temperature range of 50 to 300 K.

The diode on-state resistance from Reference 109 indicates an approximate linear increase from 200 to 300 K, and a linear but lower slop from 100 to 200 K. Below 100 K, the results show significant increase in on-state resistance likely due to carrier freeze out. An approximate linear fit from this data yields a slope of 0.01212 mΩ/K for 100 to 300 K. Using this slope, the diode on-state resistance can be approximated as a function of temperature by the equation:

$$R_{D,on}^{cryo} = R_{D,on}^{300K} + 1.212 \cdot 10^{-5}\left(T - 300\right)$$

TABLE 15.—IGBT CHARACTERISTIC SCALING FOR CRYOGENIC TEMPERATURES

IGBT characteristic	Scaling factor cryo/room temperature	Comments
Nominal current, A	1	
Over current, A	1	
Nominal blocking voltage, kV	0.5	35 to 75% reduction at lower temperatures
Conduction voltage drop, V	1	
Time to turn off, μs	0.3	5 to 50% reduction at lower temperatures
Time to turn on, μs	1	
Turn off energy, J	0.25	20 to 33% reduction at lower temperatures
Turn on energy, J	0.25	20 to 33% reduction at lower temperatures

For cryogenic diode operation, the tests from Reference 110 indicated an approximate 20 percent decrease of breakdown voltage at 50 K compared to 300 K. IGBTs indicated a 35 to 75 percent reduction in breakdown voltage for temperatures down to 30 K. It is assumed that the reduction in breakdown voltage is approximately the same for IGBTs and diodes. For IGBTs and diodes, the breakdown voltage is used in part to determine the series configuration for the rated converter voltage. For the diodes, the series configuration is the only use of the breakdown voltage.

To estimate the cryogenic scaling of the reverse recovery energy for the diode, the results for the reverse recovery time as a function of temperature are used (Ref. 111). The reverse recovery energy is related to the reverse recovery time. This study makes the assumption that the recovery energy is directly proportional to the relationship of reverse recovery time and temperature. For 100 to 200 K, the reverse recovery time was shown as constant at 300 ns (61 percent of 300 K time), and then increased linearly from 200 to 300 K with a slope of 1.63 ns/K (0.3 percent/K). These percentages are used to scale the 300 K diode reverse recovery energy as a function of temperature by the equation:

$$E_{rr}^{cryo} = \begin{cases} 0.61E_{rr}^{300K}, 100K \le T \le 200K \\ E_{rr}^{300K} + 0.003(T-300), T > 200K \end{cases}$$

The overall converter model specifies the cryogenic device nominal current and blocking voltage ratings. From these specifications, the IGBT mass, power loss, and current interruption time are estimated for the device at the specified device ratings. The existing IGBT ratings for ABB, Infineon, and Mitsubishi devices were tabulated, and trends from these devices were developed in order to develop a scalable IGBT within the current and voltage ratings of the known devices. Trends were developed for IGBTs with nominal current in the range of 200 to 1500 A and nominal blocking voltage in the range of 1.2 to 6.5 kV. This tabulated data is included in Appendix B as well as in all of the models using IGBTs.

Because these trends are within a current range of 200 to 1500 A and voltage range of 1.2 to 6.5 kV, modules of IGBTs (half bridge for the unidirectional converter and full bridge for the bidirectional converter) are configured in series and/or in parallel to size the IGBTs within the current and voltage range for which data is available. If the current rating of the overall converter is higher than the maximum current for IGBT data, then two or more IGBT modules are connected in parallel to divide the overall converter current into the multiple modules and thus avoid extrapolating the IGBT sizing trends. Analogously, if the voltage rating of the overall converter is higher than the maximum voltage for IGBT data, then two or more IGBT modules are connected in series to divide the overall converter voltage. On the minimum rating of the IGBTs, the minimum voltage is within the minimum converter rated voltage scaling, but the minimum IGBT current data is greater than the minimum converter rated current for the lower powered bidirectional converters at higher voltages. The trends presented in this report thus are extrapolating the IGBT scaling for these conditions. An improvement to the models to avoid extrapolation of the IGBT trends is to gather IGBT data at lower current ratings but similar voltages and add this data and corresponding trends to the IGBT scaling model.

The rated blocking voltage across the IGBT module is:

$$V_{block,IGBT} = \left(V_{ac} + \frac{V_{dc,ptp}}{2} \right) \frac{1}{N_{s,\text{module}} N_s} \text{ (Ref. 112)}$$

With V_{ac} as the peak nominal line-to-neutral AC side voltage, $V_{dc,ptp}$ as the pole-to-pole nominal DC side voltage, $N_{s,\text{module}}$ as the number of series IGBTs within the module blocking the voltage (1 for half bridge, 2 for full bridge), and N_s as the number of series IGBT modules. N_s is calculated so that $V_{block,IGBT}$ is within the IGBT scaling data and for the lowest number of IGBTs in order to minimize the IGBT and total converter mass.

The steady-state rated conduction current through the IGBT module is:

$$I_{IGBT} = \left(\frac{I_{dc}}{3} + \frac{I_{ac}}{2} \right) \frac{1}{N_p} \quad \text{(Ref. 113)}$$

With I_{ac} as the peak nominal AC side current, I_{dc} as the nominal DC side current, and N_p as the number of parallel IGBT modules. Within the module, there are no parallel-connected IGBT modules. N_p is calculated so that I_{IGBT} is within the IGBT scaling data (below the maximum current but not necessarily above the minimum current) and for the lowest number of IGBTs.

Trends from this existing IGBT data follow and are used to estimate a scalable IGBT mass and losses for given nominal current and blocking voltage ratings (Figure 41 and Figure 42). The turn-on time used for scaling is the average of the IGBT turn-on time data (2.128 μs) since it did not vary significantly with rated voltage or current.

The IGBT mass in kg is estimated by the trend as a function of nominal current in A and nominal blocking voltage in kV by the equation:

$$Mass_{IGBT,\mathrm{kg}} = 1.405 + 0.350 \frac{\left(I_{C,rated} - 884.6\right)}{376.6} + 0.173 \frac{\left(V_{block,rated} - 4.215\right)}{1.871} + 0.0413 \frac{\left(I_{C,rated} - 884.6\right)}{376.6} \frac{\left(V_{block,rated} - 4.215\right)}{1.871} + 0.0102 \frac{\left(V_{block,rated} - 4.215\right)^2}{1.871}$$

Note that this IGBT mass data includes the antiparallel free-wheeling diode in the same module. For the current-source converter topology, the diode is in series with the IGBT rather than free-wheeling. For similar voltage and current ratings as the IGBT, the diode mass estimate is included as part of the IGBT mass estimate.

The IGBT turn-off energy in J is estimated by the trend as a function of nominal current in A and nominal blocking voltage in kV by the equation:

$$E_{off,IGBT} = 2.319 + 0.8858 \frac{\left(I_{C,rated} - 884.6\right)}{376.6} + 1.54 \frac{\left(V_{block,rated} - 4.215\right)}{1.871} + 0.101 \frac{\left(I_{C,rated} - 884.6\right)^2}{376.6} + 0.801 \frac{\left(I_{C,rated} - 884.6\right)}{376.6} \frac{\left(V_{block,rated} - 4.215\right)}{1.871} - 0.1364 \frac{\left(V_{block,rated} - 4.215\right)^2}{1.871}$$

Once the individual IGBT and diode mass and loss estimates are calculated for the specified current and voltage ratings, the total IGBT and diode mass and losses are calculated based on the converter topology. The IGBT and diode total mass for the rectifier/inverter CSC topology is calculated by

$$Mass_{IGBT,total} = Mass_{IGBT} N_M N_{MpA} N_A$$

Where N_M is the number of IGBTs per switching module (2 for half bridge, 4 for full bridge), N_{MpA} is the number of switching modules per arm based on the series/parallel configuration, and N_A is the number of arms for the converter (6 for the midpoint clamped topology). This same equation is used to calculate the IGBT and diode mass since each IGBT is paired with a series diode and the IGBT mass estimate includes the diode mass estimate (Figure 43).

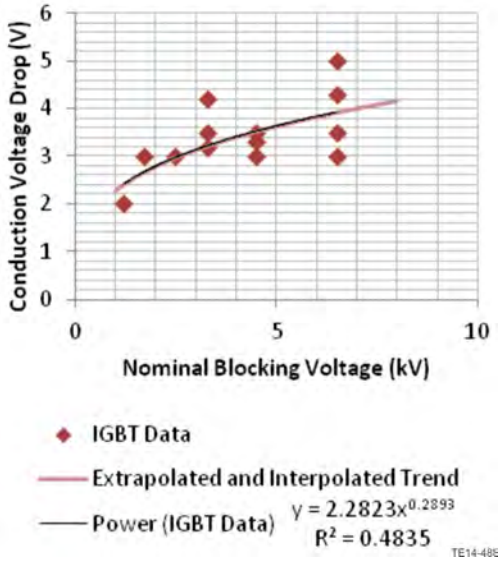

Figure 41.—IGBT Conduction Voltage Drop Data and Trends versus Blocking Voltage for Room Temperature IGBT Scaling.

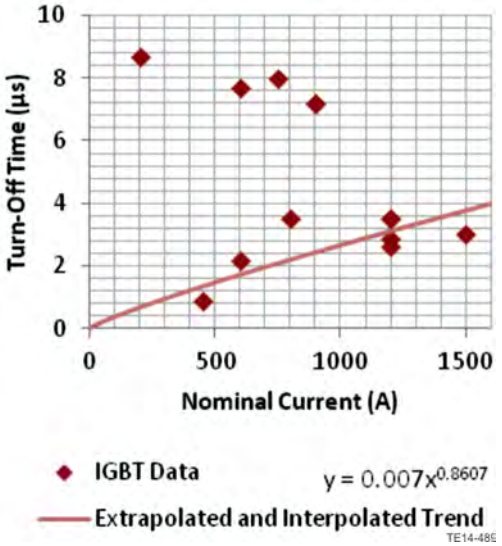

Figure 42.—IGBT Turn-Off Time Data and Trends versus Nominal Current for Room Temperature IGBT Scaling.

The total loss contribution of the IGBTs and diodes is described by the equation:

$$P_{loss,Subtotal} = \left(P_{loss,IGBT} + P_{loss,diode}\right)\frac{N_M}{2}N_{MpA}N_A$$

$$= \left(P_{cond,IGBT} + 2P_{sw,IGBT} + P_{cond,diode} + 2P_{sw,diode}\right)\frac{N_M}{2}N_{MpA}N_A$$

Where P_{cond} and P_{sw} are the conduction and switching losses, respectively. These power loss calculations are described in the next few pages. The number of IGBTs or diodes per module is halved for the conduction loss contribution since only half of the devices are conducting at any time.

The overall converter model specifies the series/parallel configuration of the converter IGBTs so that each device has voltage and current ratings within this range (if possible) so as to minimize the extrapolation of the scalable IGBT trends. It will be shown how extrapolation of these trends affects the high power rectifier total mass and losses. In order to avoid extrapolation and potentially achieve smoother total converter trends, additional existing IGBT data can be included in the table, and revised trends can be developed. Additional data for lower current rated IGBTs is necessary to avoid extrapolation of the existing trends for lower power devices rated for higher DC voltages. An alternative approach, as cryogenic device and converter operation is further researched and developed, would be to develop IGBT models based on required material and configuration in order to achieve the desired voltage, current, and interruption time ratings. Such a model requires in-depth knowledge of the device physics and material science. An example of the construction of punch-through and non-punch through IGBTs is shown in Figure 44.

To estimate the power losses of the IGBT and diode devices, the switching and conduction losses are estimated and summed. The conduction and switching losses for standard voltage-source two-level inverters and rectifiers are well known and can be used to approximate the conduction and switching losses for this converter topology for this system study. An improved estimate of the losses can be calculated using circuit simulations.

For the use of IGBTs and diodes in an inverter or rectifier, the converter is operated using pulse-width modulation (PWM). The IGBT conduction losses for a PWM-controlled converter are approximated by:

$$P_{cond,PWM} = \frac{1}{2}\left(V_{CE}\frac{I_C}{\pi} + r_{CE}\frac{I_C^2}{4} \right) + m\cos\phi\left(V_{CE}\frac{I_C}{8} + \frac{1}{3\pi} r_{CE} I_C^2 \right) \text{ (Ref. 114)} \quad (3)$$

Where V_{CE} is the collector-emitter voltage during conduction, I_C is the collector current, r_{CE} is the equivalent collector-emitter resistance, and m cos ϕ is the equivalent PWM duty cycle for a given operating point. The value used for m cos ϕ to compute rectifier operation conduction losses throughout this study is $\frac{-2}{\pi} \approx -0.64$. For inverter operation, the value used is 0.64. Nominal conduction r_{CE} can be computed for rated conduction V_{CE} and I_C by:

$$r_{CE} = \frac{V_{CE}}{I_C}$$

The diode conduction losses may be calculated using the same for IGBT conduction losses since they are in series for the current-source configuration rather than antiparallel for the traditional voltage-source configuration. In that case, V_{CE} is instead the diode forward voltage, I_C is the diode conduction current, and r_{CE} is the diode on-state resistance.

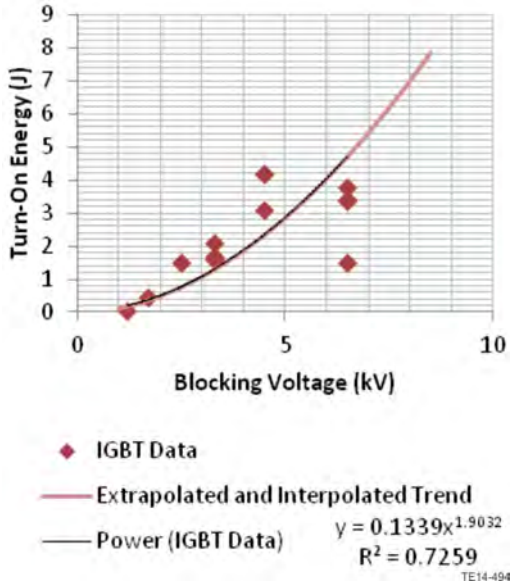

Figure 43.—IGBT Turn-On Energy Data and Trends versus Blocking Voltage for Room Temperature IGBT Scaling.

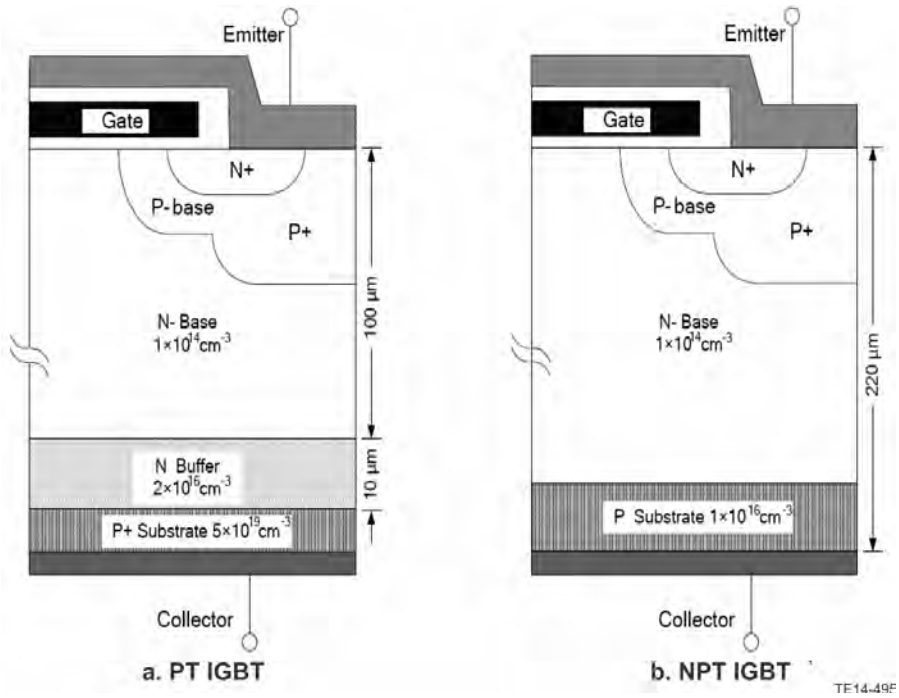

Figure 44.—PT and NPT IGBT Structure (Ref. 115).

IGBT or diode switching losses for a PWM-controlled converter are approximated by:

$$P_{sw,PWM} = \frac{1}{\pi} f_{sw}\left(E_{on} + E_{off}\right) \tag{4}$$

Where f_{sw} is the converter switching frequency, E_{on} is the turn on energy, and E_{off} is the turn off energy.

When IGBTs and diodes are used in a DC/DC converter, such as the bidirectional converter used to interface the SMES to the DC distribution bus, the converter duty cycle (D) drives switching losses. The IGBT or diode conduction losses for use in a chopper configuration (DC/DC converter) are approximated by:

$$P_{cond} = \left(V_{CE} I_C + r_{CE} I_C^2\right) D \tag{5}$$

With each switch turning on and off once per cycle, the switching losses for the DC/DC converter are approximated by:

$$P_{sw} = f_{sw}\left(E_{on} + E_{off}\right) \tag{6}$$

5.2.2.2.3 Capacitor Sizing Model

The specified capacitance, voltage, and current from the overall converter model are used to estimate the capacitor mass and losses. The total converter capacitance requirement is determined by:

$$C_{eq} = \frac{I_{dc}}{2 f_{ac} \Delta V_{dc}}$$

For the converter topologies modeled, the equivalent capacitance is divided among six separate capacitors, one for each arm. For three identical capacitors in parallel, all in series with an additional set of three identical capacitors in parallel, the individual arm capacitance is calculated by

$$C_{arm} = \frac{3}{2} C_{eq}$$

The average arm capacitor voltage is:

$$V_{Carm} = \frac{V_{dc,ptp}}{2}$$

The estimated arm capacitor current is the total arm current. However, the arm capacitor current may even higher depending on the DC bus voltage ripple and frequency.

$$I_{Carm} \approx \left(\frac{I_{dc}}{3} + \frac{I_{ac}}{2} \right)$$

These arm capacitor specifications are given to the capacitor sizing model to estimate the arm capacitor mass and equivalent series resistance (ESR). A cylindrical film-foil type capacitor is used to model the arm capacitor. This type of capacitor is chosen because the permittivity of the dielectric, polypropylene, used in high power capacitors performed well when tested in cryogenic environments (Refs. 116 and 117). When tested at 77 K, 0.99 μF room temperature rated capacitors had the same capacitance at 77 K, and the ESR decreased by more than a factor of 2. Film capacitors are widely used as DC link capacitors and IGBT snubbers such as the capacitors for these power converters. Aluminum was chosen as the foil electrode material for this capacitor scaling (Ref. 118). A different metal may be used to further reduce the capacitor ESR. An example of a metalized polypropylene film capacitor construction is shown in Figure 45.

To construct the capacitor, layers of foil and dielectric film are added in cylindrical form until the capacitor has the desired capacitance rating. The capacitance of each foil+dielectric+foil set of layers is estimated by the capacitance of a cylinder:

$$C_{layer} = 2\pi\varepsilon_r\varepsilon_0 \frac{L}{\ln\left(\frac{b}{a}\right)}$$

Where ε_r is the relative permeability of the dielectric, ε_0 is the permittivity of a vacuum (constant at $8.8541878176 * 10^{-12}$), L is the cylinder length, b is the outer conductor radius, and a is the inner conductor radius. This equation is valid when L is large compared to b. For polypropylene dielectric, ε_r is 2.2-2.36. The value used for this modeling is 2.2. A fixed length of 0.1 m is used for the capacitor models throughout this study. The capacitor model could be modified to minimize mass while allowing the length and other parameters to vary.

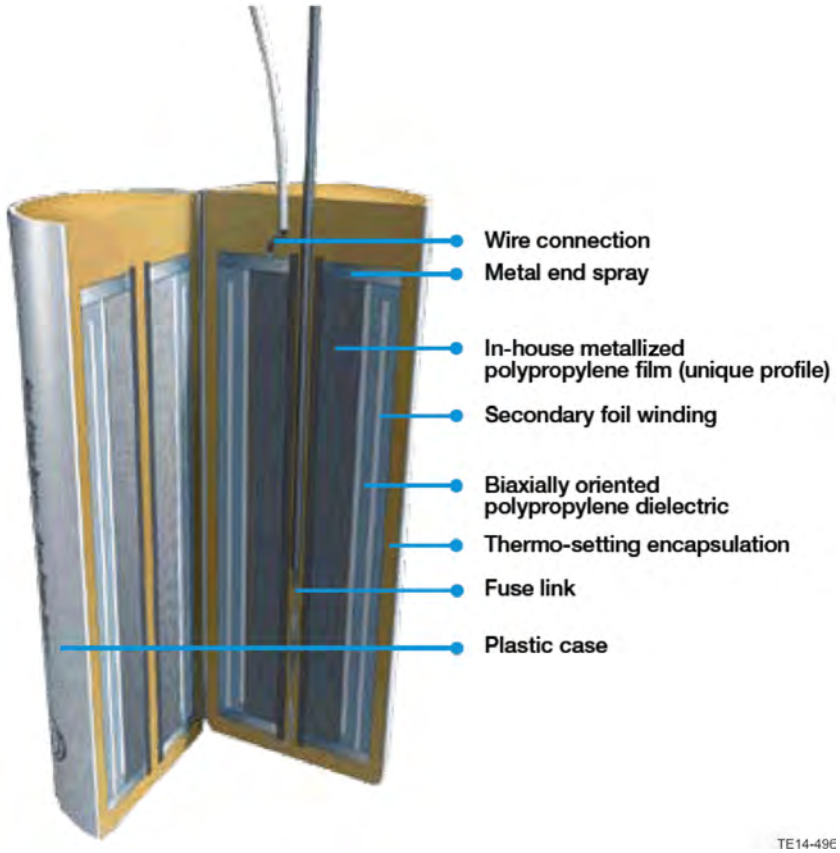

Figure 45.—Metallized Polypropylene Film Capacitor Construction from ABB (Ref. 119).

To estimate the outer and inner conductor radii, material properties for polypropylene film capacitors are used. The standard film thickness for polypropylene is 2.4 to 3.0 μm, and its dielectric strength ε_s is 650 V/μm. The modeled film thickness in μm is described by:

$$F_t = \text{Maximum of}\left(2.4, \frac{V_{arm}}{\varepsilon_s}\right)$$

so that the dielectric thickness meets the minimum capacitor voltage rating. This allows only one capacitor to be modeled for a given capacitance and voltage rating. The foil thickness M_t is assumed to be twice the dielectric thickness. These dielectric and foil thicknesses are the same for every cylindrical layer used to form the capacitor.

From these thicknesses and the cylindrical capacitance estimate equation, the number of film foil layers N_{layers} is calculated to form the capacitor with the specified capacitance by adding a layer, computing the layer's capacitance, and checking whether the total capacitance thus far is greater or equal to the specified capacitance. If it is less, then another layer is added.

Once the number of film foil layers is determined, the cylinder radius is calculated by:

$$r_{cyl} = N_{layers}\left(F_t + M_t\right)$$

The mass of the cylinder is estimated by calculating the mass of the dielectric and metal layers from the dielectric and metal volume and density. Constants used are the polypropylene density of 946 kg.m^3 and Aluminum density of 2700 kg/m^3

The capacitor ESR is calculated by the equation:

$$ESR = \frac{M_r L}{\pi\left(r_{cyl}^2 - \left(r_{cyl} - Mt\right)^2\right)}$$

where the M_r is the metal resistivity (Aluminum used for the conductor has a resistivity of 28.2 nΩ-m). This is the resistance for the outer conductor layer.

The room temperature capacitor scaling model results were checked against Cornell Dubilier polypropylene round axial film capacitor ratings and masses (Ref. 120) to understand the accuracy of this capacitor scaling method.

The cryogenic scaling of this capacitor is based on the test results of polypropylene film capacitors at 77 K (Refs. 121 and 122). Relevant results from this study are summarized in Table 16. Based on this results, the room temperature capacitor is scaled to a cryogenic environment by a 1:1 ratio for capacitance, and multiplying the room temperature ESR by 0.5. Also, a packing material improvement factor for the N+3 application is used. In this case, it is specified as 0.7, which indicates the capacitor mass can for N+3 is approximated as 70 percent of the present capacitor mass.

5.2.2.2.4 Inductor Sizing Model

Given the total lumped arm inductance from Equation (2), the individual switching module inductance specifications are determined. From those specifications, the mass and loss of each inductor is estimated by the inductor model which is based on the SFCL model. For detail on the SFCL model, see Section 5.6.

The switching module link inductance is calculated by:

$$L_{\text{module}} = \frac{N_p}{N_s} L_{arm}$$

TABLE 16.—CRYOGENIC 100 VDC POLYPROPYLENE CAPACITOR OPERATION AT 77 K

Capacitor rating	Control at room temp			In-situ LN_2			Conclusions	
Capacitance, μF	Frequency, kHz	Dissipation factor x10^{-2}	ESR, Ω	Capacitance, μF	Dissipation factor x10^{-2}	ESR, Ω	ESR ratio cryogen/room temperature	Capacitance ratio cryogen/ room temperature
0.99	1	0.02	0.03215	1	0.01	0.01591	0.495	1.01
0.99	20	0.18	0.01445	1	0.08	0.00637	0.44	1.01
0.99	50	0.49	0.01575	1	0.31	0.00987	0.626	1.01

The module inductor current rating is the nominal AC peak current. The rated voltage is approximated by:

$$V_{L\text{module}} = L_{\text{module}} \frac{di_{\text{module}}}{dt} \approx L_{\text{module}} \frac{1}{N_s} \left(\Delta I_{dc} + 2\pi f_{ac} I_{ac} \right)$$

These specified inductance, voltage, and current ratings are then used by the inductor model to estimate the module inductor mass and losses. The main difference between the inductor model and SFCL model is that there is no quench state resistance for which the inductor is sized; the inductor is sized to meet the desired inductance only.

5.2.2.2.5 Packaging Model

The packaging mass estimates, which include the heat exchanger, housing, bus bars, and current sensors, are based on scaling of state-of-the-art power converters. This was discussed previously in Section 3.5. Using the data and studies from references (Refs. 123 and 124), mass percentages of the packaging components were estimated and are listed in Table 17. Using these percentages, the packing component masses are scaled according to the subtotal mass of the inductor, presspack diodes, and IGBT and series diodes as estimated by the model. More detailed models of each of these components could be described so that they are more independent of the IGBT and inductor scaling models. Some ways in which these models could be developed and scaled are:

- The heat exchanger mass could be estimated based on the converter losses and thermal transfer capability.
- The housing could be based on a volume estimate of the converter.
- The bus bars could be estimated by the rated AC and DC currents and estimated connections of all of the circuit components.
- The current sensors could be scaled as a function of the AC and DC currents.

For such packaging models, these models should be verified against the existing state-of-the-art high power electronic devices. For the N+3 time frame and this sensitivity study, using scaling to estimate the packaging mass is assumed to be appropriate.

5.2.3 Source-Side Converters Trends

The unidirectional rectifiers are used as the power converters to convert the generator AC voltage to DC bus voltage. With four generators for this architecture, these rectifiers are rated for 50 percent of the minimum takeoff power of 25 MW. This power rating is 12.5 MW. The parameters used to develop the following trends are described in Table 17.

TABLE 17.—ASSUMED PARAMETERS AND VALUES FOR UNIDIRECTIONAL CURRENT-SOURCE CONVERTER TRENDS

Parameter	Value
Converter Sizing	Modulation index: 0.8
	Power factor: 1
	Operating temperature: 100 K
	DC voltage ripple magnitude, %: 20
	DC current ripple magnitude, %: 10
Inductor	DC pole-to-pole resistance for inductance requirement: 1 Ω
	Insulator dielectric strength (LPP): 100 kV/mm
	Ambient temperature of the superconductor and cooling reservoir: 100 K
	Superconductor critical temperature: 110 K
	Flux-creep region exponent (at 77 K): 6
	Flux-flow region exponent: 3
	Initial critical current density (at 77 K), i.e., current density where E=1μV/cm: 1.5×10^8 A/m^2
	Initial electric field: 0.0001 V/m
	Electric field at transition from flux-creep state to flux-flow state: 0.1 V/m
	Coefficient for heat transfer to cooling reservoir: 1500 W/K m^2
	Superconductor density: 6500 kg/m^3
	Dielectric insulation density: 900 kg/m^3
	Former density: 1800 kg/m^3
	Coolant medium: N_2
	Former thickness: 2 mm
	Inductor L/D limit: 10
IGBT and Diode	N+3 mass improvement scaling factor: 0.9
	Ideal duty cycle: 0.5
	Conduction modulation (PWM): –0.64
Capacitor	Cylinder length: 0.1 m
	Capacitor scaling cryo/room temperature: 1
	ESR scaling cryo/room temperature: 0.5
	Improved materials and packaging = (N+3 mass)/(N mass): 0.7

From Figure 46, the nonlinear specific power trend for the high power bidirectional CSC versus DC bus voltage is shown. Note that the discontinuities in these trends occur because of the switching module series/parallel configuration changes as the DC bus voltage increases. As described previously, the IGBTs are scaled for a certain current and voltage range. To interpolate the IGBT data, a series/parallel configuration of the IGBTs is required for operation of the converter beyond the current and voltage for which IGBT data is scaled. The series/parallel configuration is graphed in Figure 47 and should be used to understand the discontinuities.

For each of the AC frequency trends, the specific power is maximized for a DC bus voltage of 5.5 kV. Looking at one AC frequency trend, the below the 5.5 kV DC bus voltage, the specific power increases (mass decreases for fixed power). Above the 5.5 kV DC bus voltage, the specific power gradually decreases (mass gradually increases). This trend can be further explained by analyzing the converter mass breakdown by component. Figure 48 shows the converter mass breakdown for a 100 Hz AC system, and Figure 49 shows the converter mass breakdown for an 800 Hz AC system.

For the lower bus voltages, the capacitor mass a high percentage of the total converter mass. For the higher bus voltages, the inductor mass increases but is not as significant a portion of the total converter

mass as is the capacitor. This mass breakdown shows that the high power unidirectional power converter mass is sensitive to the DC bus voltage ripple and capacitance required at lower DC bus voltages. This trade-off between capacitance and inductance requirements and DC bus voltage is shown in Figure 50.

Comparing Figure 48 and Figure 49 for lower and higher AC frequency systems, respectively, the trends clearly indicate a decreased total converter mass as well as decreased capacitor and inductor mass for the higher frequency AC system. These mass breakdowns show that the high power bidirectional converter mass is sensitive to the AC system frequency. The converter structure mass (current sensors, bus bars, housing, heat exchanger) are scaled with IGBT + diode + inductor mass.

The total IGBT and diode mass increases as the DC bus voltage increases. This can be attributed to the IGBT mass scaling as a function of voltage and current and required number of series IGBTs to block the required voltage.

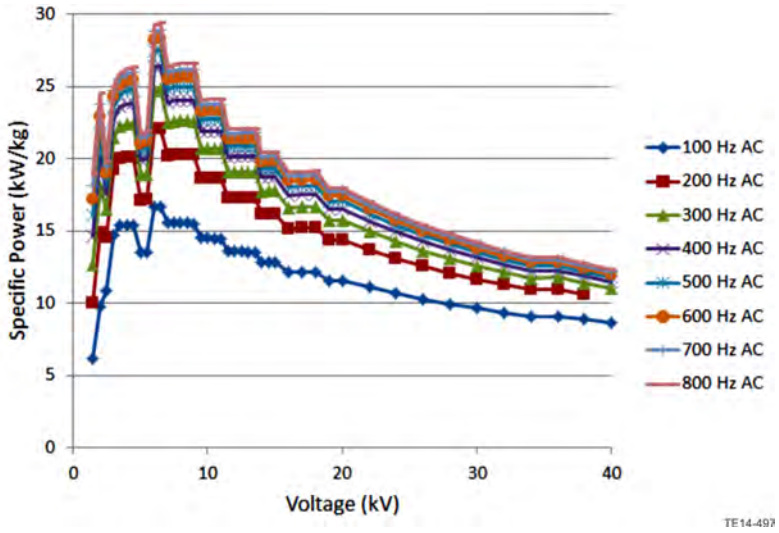

Figure 46.—Unidirectional CSC Specific Power versus DC Voltage for Several AC Frequencies.

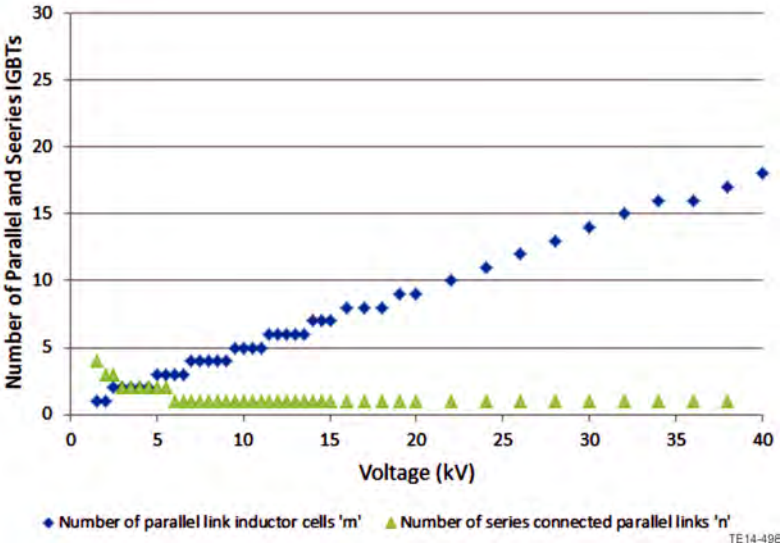

Figure 47.—Unidirectional CSC Number of Parallel and Series Switching Modules versus DC Voltage.

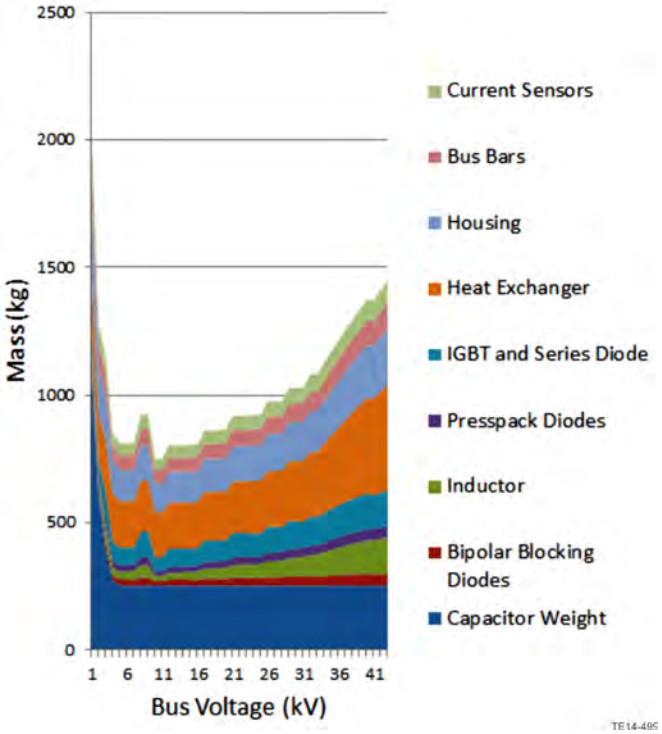

Figure 48.—Unidirectional Converter Mass Breakdown for 100 Hz AC Frequency.

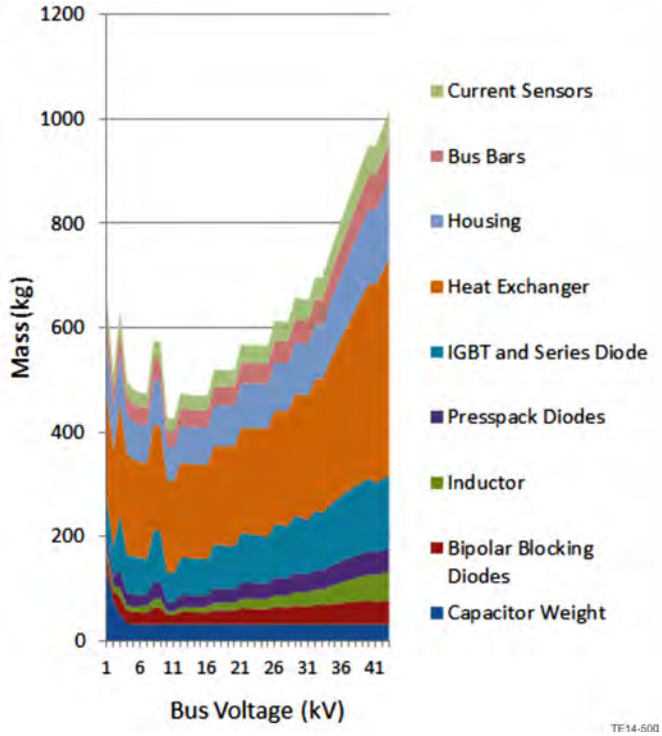

Figure 49.—Unidirectional Converter Mass Breakdown for 800 Hz AC Frequency.

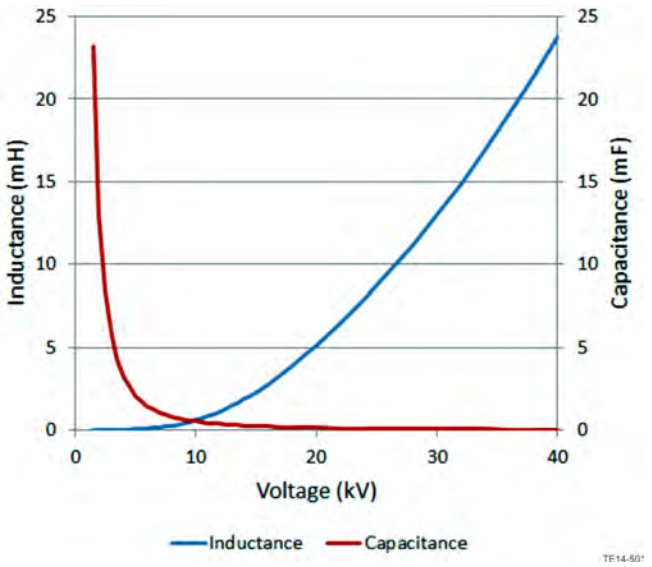

Figure 50.—Unidirectional CSC Inductance and Capacitance.

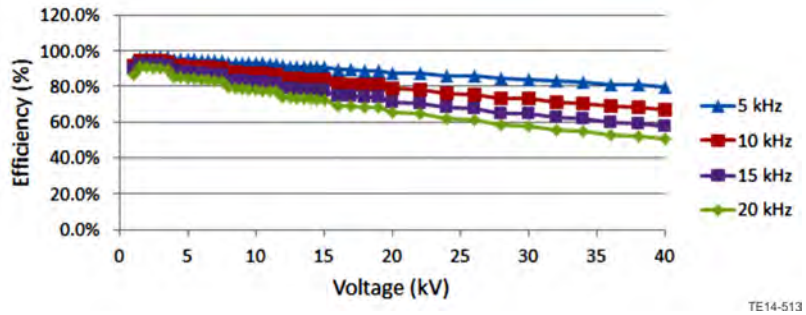

Figure 51.—Unidirectional CSC Efficiency versus DC Voltage for Several Switching Frequencies.

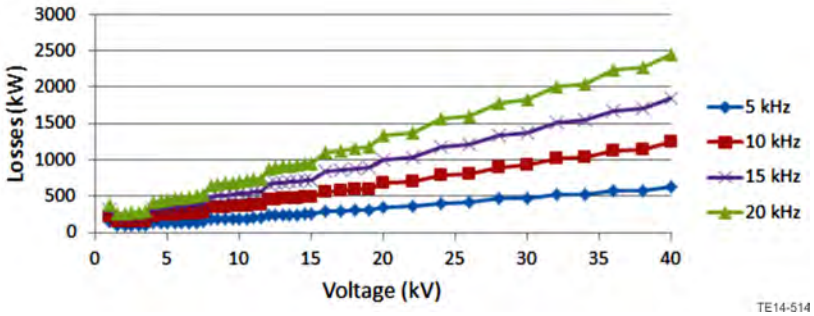

Figure 52.—Unidirectional CSC Losses versus DC Voltage for Several Switching Frequencies.

Figure 51 and Figure 52 show the trends of the converter efficiency and losses for several switching frequencies. As the DC bus voltage increases, the efficiency decreases. This decrease is more pronounced for higher switching frequencies. Also, higher switching frequencies correspond to the decreased overall efficiency. This can be further explained by examining the switching and conduction losses that form the total power loss. An example of these trends for a 5 kHz switching frequency is shown in Figure 53. As the DC bus voltage increases, the conduction losses decrease due to the lower conduction current. However, the switching losses increase due to the scaling of the IGBT turn-on and turn-off energies.

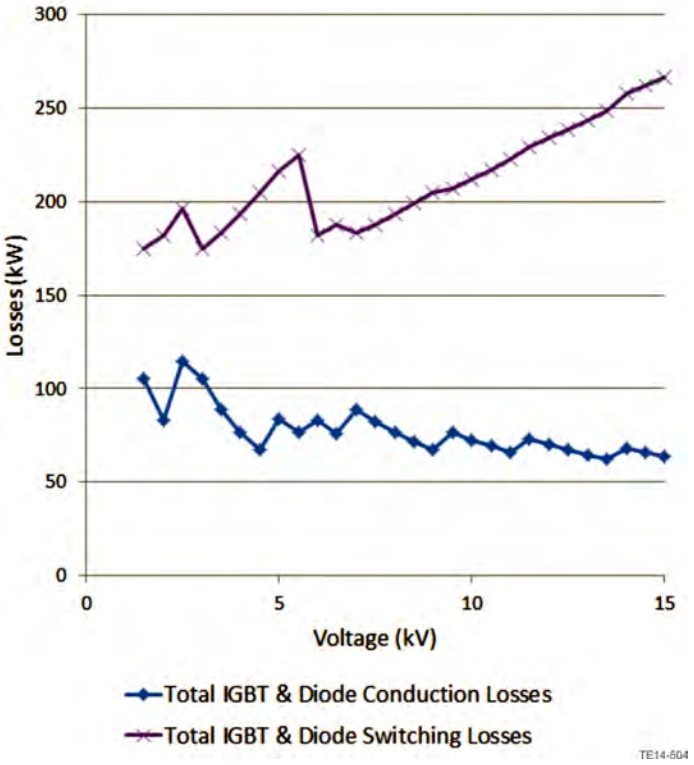

Figure 53.—Unidirectional CSC IGBT and Diode Total Switching and Conduction Losses versus DC Bus Voltage for an Example 400 Hz AC System, 5 kHz Switching Frequency.

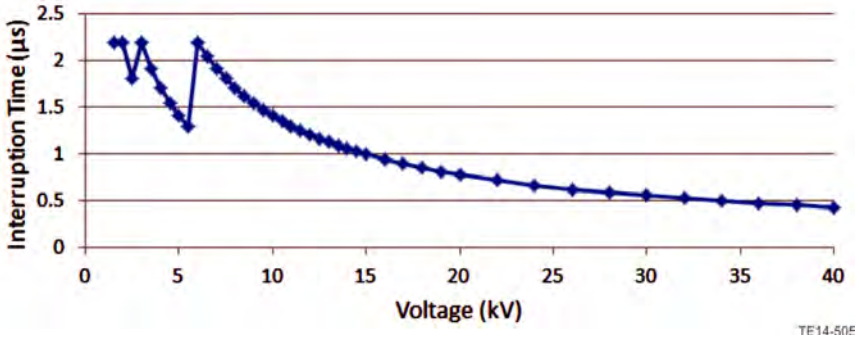

Figure 54.—Unidirectional CSC Interruption Time versus DC Voltage.

Figure 54 shows the trend of the converter interruption time versus DC distribution voltage. Generally, the interruption time decreases with increased DC voltage, which may be advantageous for the protection system in order to limit the amount of fault current through the system. The discontinuities in this trend are attributed to the change in parallel switching module configuration. The interruption time is based on the IGBT turn off time which is scaled as a function of current. IGBTs are arranged in parallel for total current ratings exceeding the scaling range.

Figure 55 combines several of these model trends to assess the converter losses as a function of interruption time. This trend indicates that to achieve interruption times less than 1 µs, the converter will have additional losses. For interruption times greater than 1 µs, the converter losses are approximately the same.

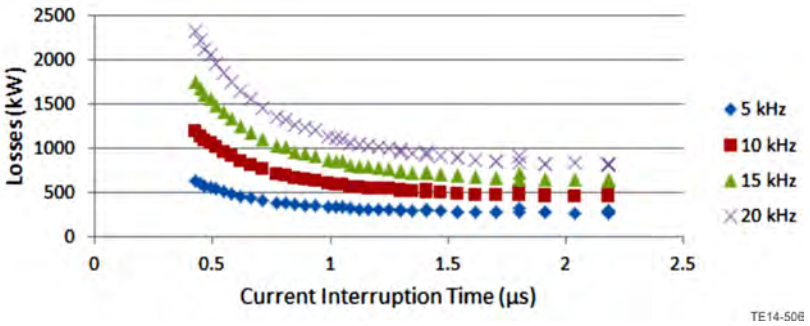

Figure 55.—Unidirectional CSC Losses versus Interruption Time for Several Switching Frequencies.

5.2.4 Load-Side Converters

As previously discussed, the load-side converters require bidirectional current flow. In order to achieve this, a similar topology is used, but the switching modules must be bidirectional. Such switching modules are formed in the full bridge configuration.

Current source converters may be used for the load side as well as the source side as long as only one of the converters controls the current and there is one or more "sink" buses through which energy not used can be stored or additional energy required can be fed to the system. These "sink" buses are the SMES units located on each of the four distribution buses.

The topology chosen for the bidirectional CSC is similar to that for the unidirectional CSC with the exception of the switching modules. Figure 56 illustrates the bidirectional CSC topology, and Figure 57 illustrates several of the switching module circuit options. These switching module options are similar to those for the unidirectional CSC except that they are arranged in a full bridge configuration to enable bidirectional current flow. Note that as with the unidirectional switch modules, only half of the IGBTs conduct current at any given time. For the full bridge case, that means that two IGBTs and series diodes conduct at a time. Thus the conduction losses include two IGBT and series diode conduction losses. The individual IGBT voltage rating is half the overall switching module rating but must carry the full switching module current.

The switch module topology options shown in Figure 57 include a full bridge without overvoltage protection (Figure 50(a)), full bridge with thyristors for overvoltage protection (Figure 57(b)), and full bridge with presspack diodes for overvoltage protection (Figure 57(c)) (Ref. 91). The topology in Figure 57(c) was chosen for this model. The converter components are all scaled the same way as for the unidirectional CSC but have voltage and current ratings for the switching module topology in Figure 57(c). Note that, similar to the unidirectional converter model, the required capacitance is lumped as a single arm capacitor rather than distributed to each switching module. It is possible that the simulation or implementation of this converter topology may indicate that a capacitor is required for each switching module, rather than a lumped capacitor, in order to equally divide the voltage among each of the series-connected switch modules.

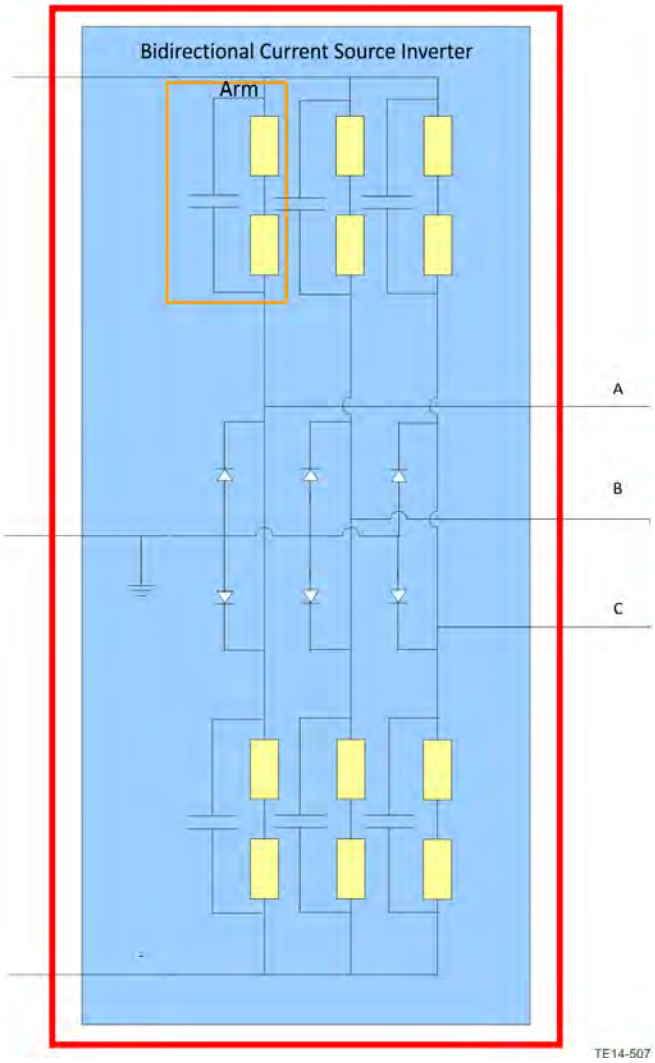

Figure 56.—Bidirectional, Current-Source Converter Topology Selected for the Propulsor Motor Drive. The Yellow Blocks in this Diagram Represent Potential Variations in the Switch Topologies.

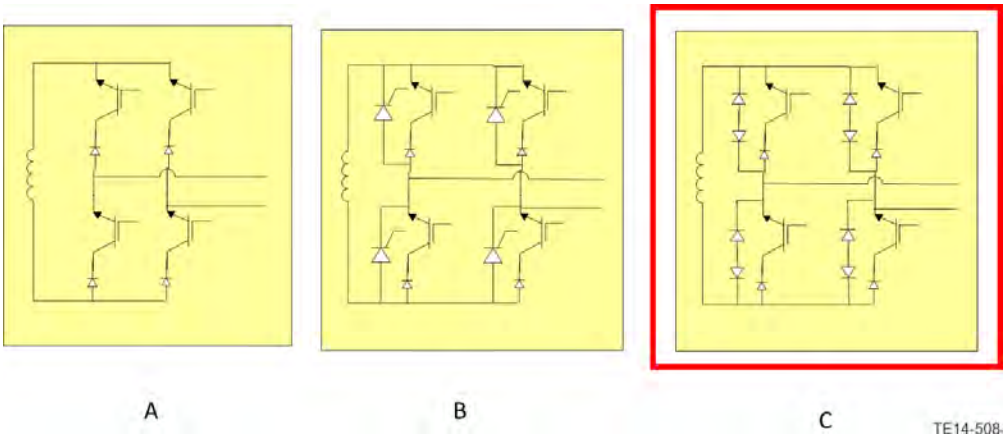

Figure 57.—Full-Bridge, Bidirectional, Current-Source Converter Semiconductor Switches. Topology C (Presspack Diodes for Overvoltage Protection) Were Selected for the Switch Topology for the AC to DC Converter over Topology B (Thyristor for Overvoltage Protection).

5.2.5 Load-Side Converter Trends

The bidirectional converters are used as the motor drives and are all rated for 7.14 percent of the minimum takeoff power 25 MW. This power rating is 2.5 MW. The assumed parameters for which these trends were developed are described in Table 17 and in Section 5.2.2.2 except that the conduction modulation for PWM is positive 0.64 for inverter operation.

When interpreting these trends, it is important to note that development of these trends required extrapolation of the IGBT trends. The IGBT trends were based on room temperature IGBT current ratings 200 to 1500 A, but for this lower power rated converter, the room-temperature translated IGBT current rating is less than 200 A when the DC pole-to-pole converter bus is greater than 4.5 kV. Consequently, for system-level sensitivity studies at higher voltages, existing IGBT data for lower current levels but similar voltage levels need to be added to the IGBT scaling for higher confidence in the converter model trends.

From Figure 58, the specific mass versus voltage does indicate a nonlinear trend at which the bidirectional converter's mass can be minimized (specific mass maximized for the given power rating). For each AC frequency, the maximum specific power occurs at 2.5 kV. With increasing AC frequency, the specific power trend is higher. This is due to the smaller inductance and capacitance required for higher AC frequencies for fixed DC voltage and current ripple magnitudes. The smaller inductance and capacitance requirements generally result in lighter devices.

The general trend for specific pass can be explained by analyzing the converter mass breakdown in Figure 59 and Figure 60.

For lower DC voltages, the capacitor mass is larger and is a large percentage of the overall converter mass. For higher DC voltages, the capacitor mass decreases while the inductor mass increases. The percentage of the capacitor and inductor mass relative to the total converter mass is due to the scaling of the packaging components (heat exchanger, hosing, bus bars, and current sensors) relative to the baseline mass breakdown and the estimated IGBT and series diode total mass.

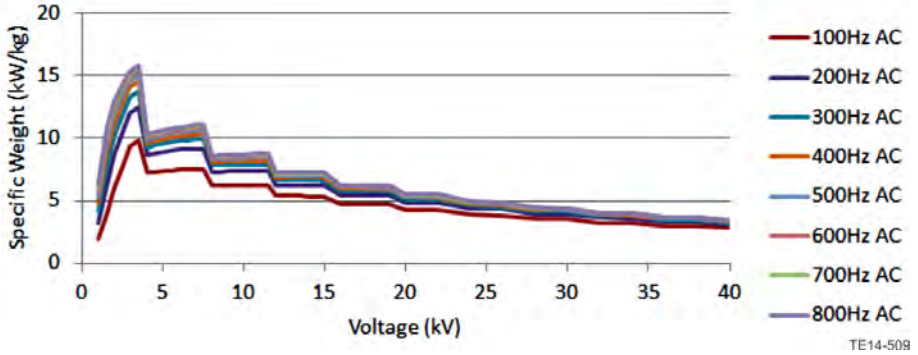

Figure 58.—Bidirectional CSC Specific Power versus DC Voltage for Several AC Frequencies.

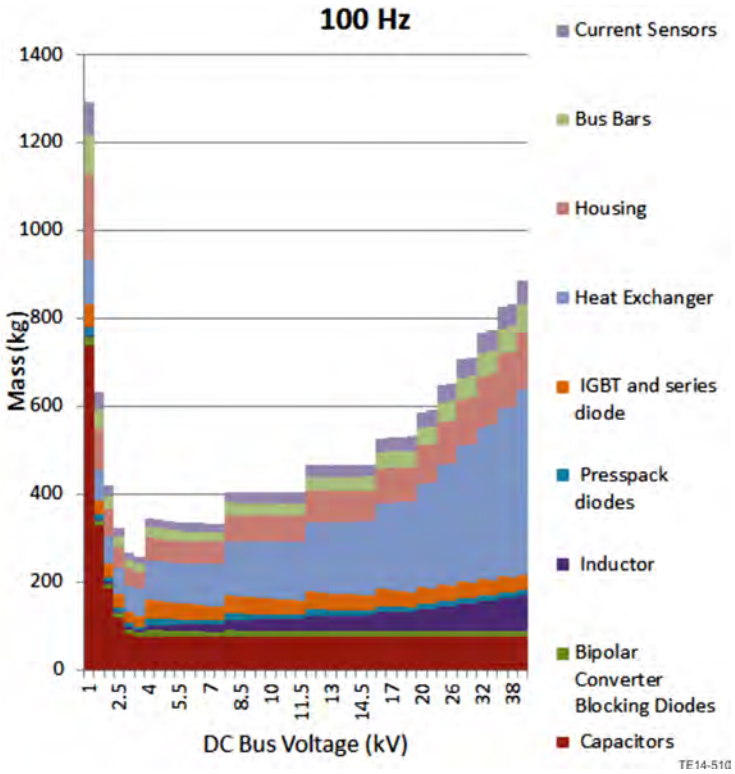

Figure 59.—Bidirectional Converter Mass Breakdown for 100 Hz AC Frequency.

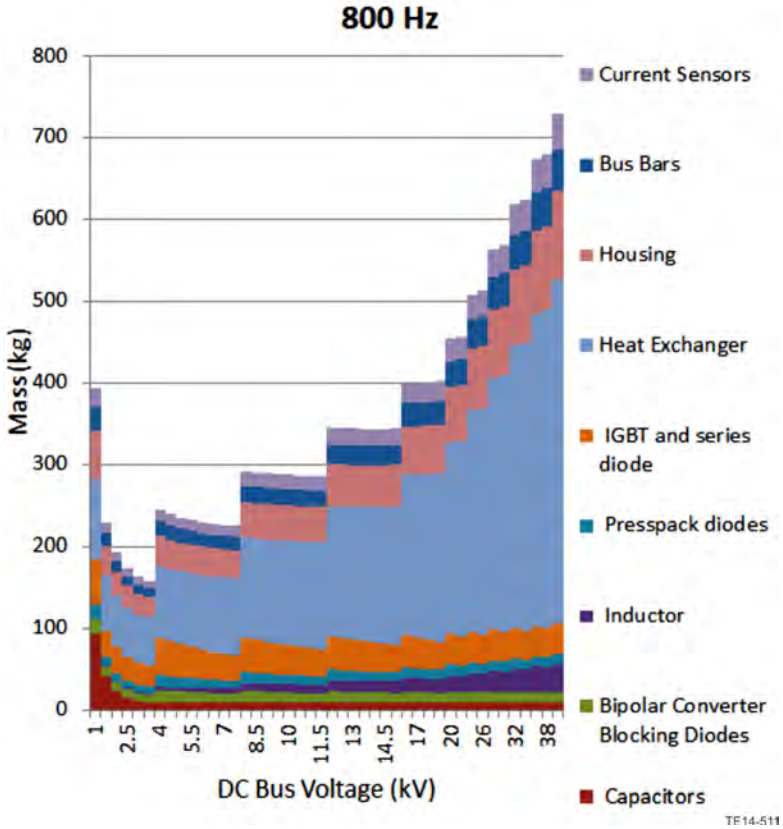

Figure 60.—Bidirectional Converter Mass Breakdown for 800 Hz AC Frequency.

The capacitor mass is larger for lower DC voltages due to the capacitance requirements and the relationship between the rated DC current and DC ripple voltage magnitude from Equation (1). The decrease in rated DC current for the fixed converter power at higher DC voltages drives the decrease in capacitance for the fixed DC bus voltage ripple. Generally, as explained in the capacitor model in Section 5.2.2.2.3, the higher the capacitance required, the more film-foil layers required for a fixed capacitor length, and the heavier the capacitor. The increase in inductor mass for higher voltages is generally due to the increase in individual and total inductance requirement which requires more mass. The discontinuous changes in the inductor mass are due to the addition of a series switching module as required for higher voltages and the need to interpolate IGBT data for scaling purposes.

Figure 61 shows the equivalent capacitance and arm inductance requirements versus DC bus voltage for a 400 Hz AC frequency.

Figure 62 and Figure 63 show the CSC efficiency and loss trends. Generally, for a specific switching frequency, as the DC bus voltage increases, this converter model at the specified power level indicates an increase in losses As the DC bus voltage increases, the individual switching module current rating decreases, and this decreases the conduction losses. However, the turn-on energy increases according to the IGBT scaling trends, and this increases the switching losses. Note that the turn-on energy is scaled as a function of IGBT rated voltage. Figure 64 illustrates an example trend of the IGBT and diode switching and conduction losses versus DC bus voltage.

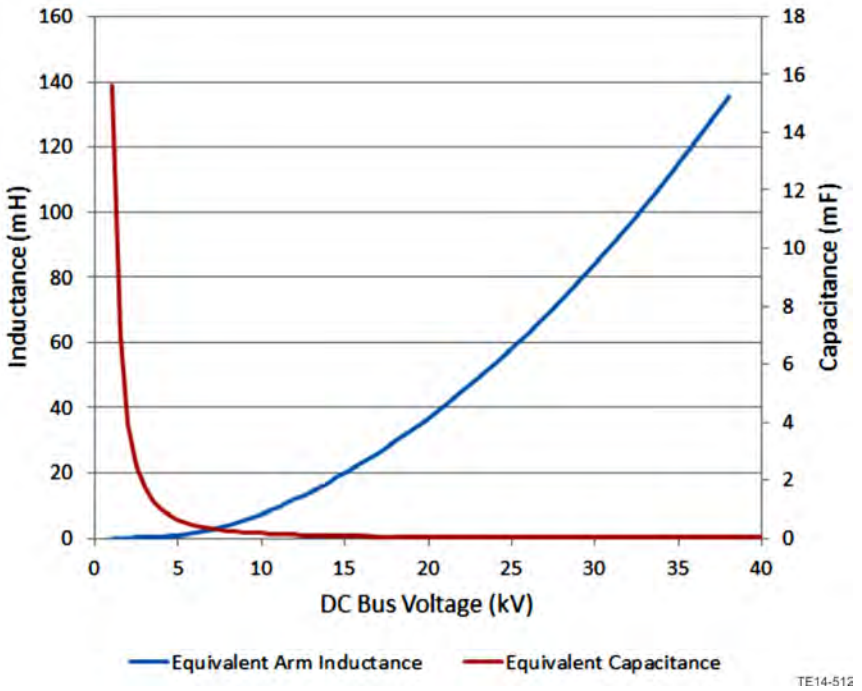

Figure 61.—Bidirectional CSC Inductance and Capacitance Requirements versus DC Bus Voltage for 400 Hz AC.

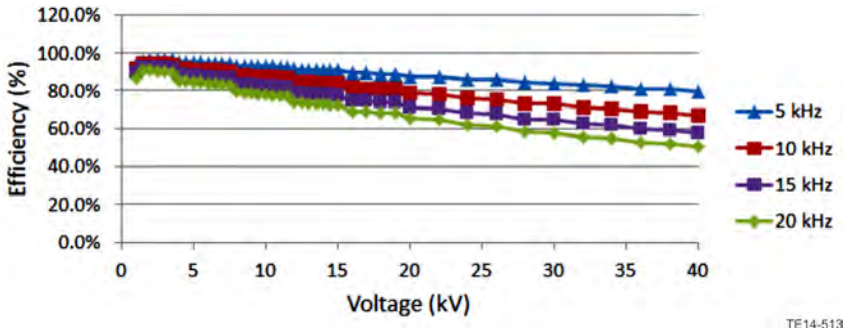

Figure 62.—Bidirectional CSC Efficiency versus DC Voltage for Several Switching Frequencies.

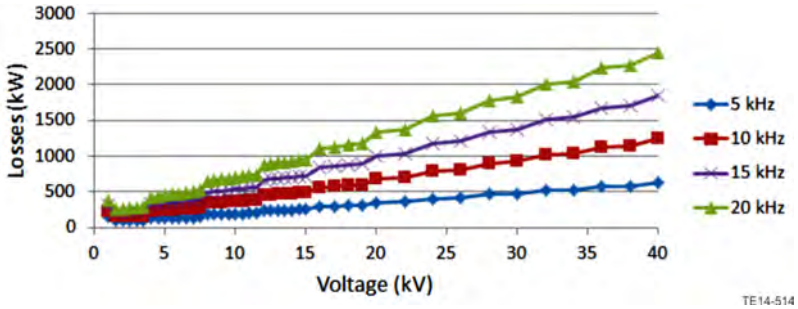

Figure 63.—Bidirectional CSC Losses versus DC Voltage for Several Switching Frequencies.

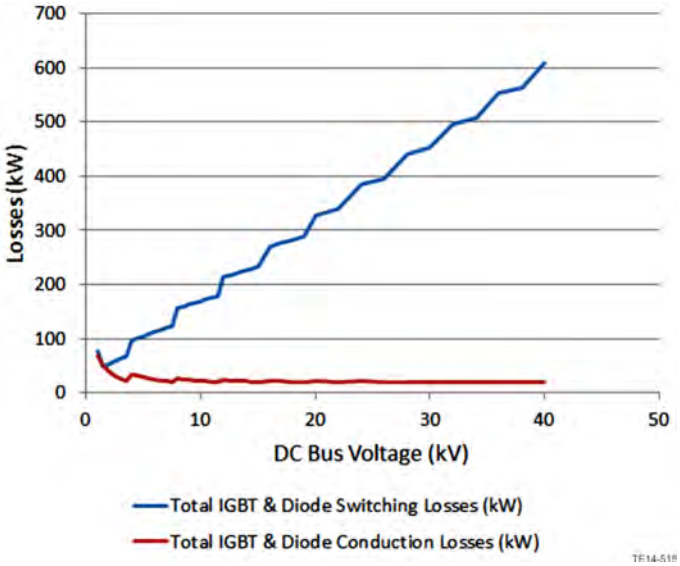

Figure 64.—Bidirectional CSC IGBT and Diode Total Switching and Conduction Losses versus DC Bus Voltage for an Example 400 Hz AC System, 5 kHz Switching Frequency.

For a higher switching frequency, the switching losses increase due to more switching events per second, and the total converter losses increase. For this converter power rating, the switching losses are more significant than the conduction losses even at lower DC bus voltages.

Figure 65 illustrates the series/parallel configuration of the switching modules for each bus voltage. For this low power rating, only one module is required (none in parallel) due to the lower current rating and IGBT current scaling range. As the DC bus voltage range increases, more switching modules are

configured in series to divide the pole-to-pole DC bus voltage. This trend is provided so as to help the reader understand the locations of the discontinuities in the trends.

Figure 66 indicates a decrease in interruption time for higher rated DC bus voltage. This is due to the IGBT scaling trend for turn-off time as a function of rated current as shown in Figure 42. Note that the turn-off time trend is extrapolated for DC pole-to-pole converter bus voltage greater than 4.5 kV. Further confidence in these turn-off times can be gained with additional lower current rated IGBT data and trend development.

Figure 67 shows a combination of the trends presented with total CSC losses versus interruption time. This shows that, based on the model data, there is a trade-off in lower losses and faster interruption time especially for the interruption times less than 1 μs. For longer interruption times, lower losses generally result from lower switching frequencies.

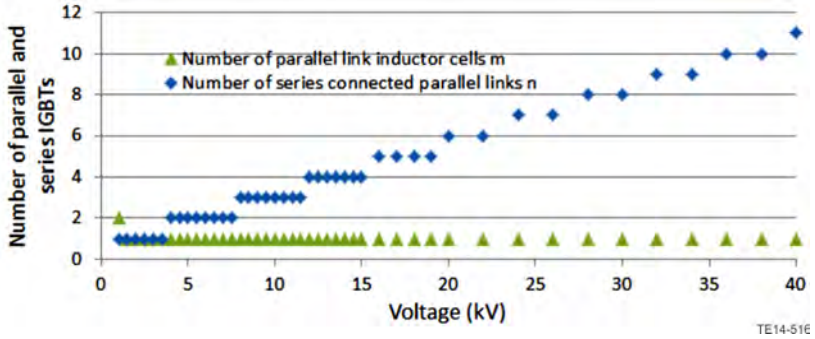

Figure 65.—Bidirectional CSC Number of Parallel and Series Switching Modules versus DC Voltage.

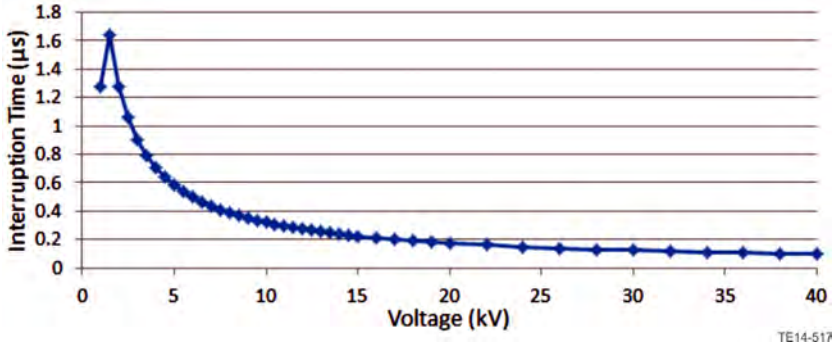

Figure 66.—Bidirectional CSC Interruption Time versus DC Voltage (Extrapolated IGBT Data).

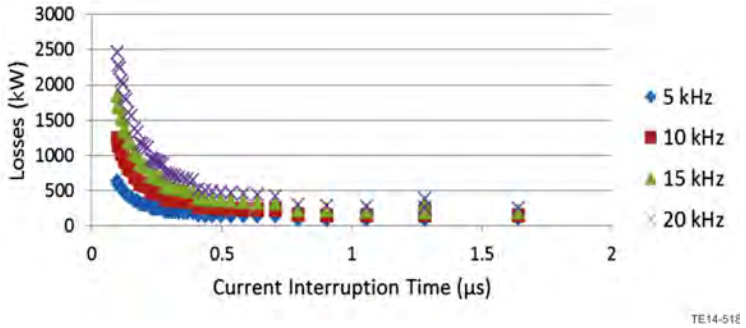

Figure 67.—Bidirectional CSC Losses versus Interruption Time for Several Switching Frequencies (Extrapolated IGBT Data).

5.3 Cables Model Overview

The cable models determine the mass efficiency and losses associated with the previous estimates determined that the cable system contributes roughly 4 percent of the overall mass of the TeDP microgrid system. However, the overall contribution of cables to system weight depends on the operating voltage (AC_{RMS} or DC), the power rating for the cable, and its length. The cable model was defined following the general parameter structure illustrated in Figure 68.

As illustrated in this figure, the outputs of interest are cable weight and efficiency, as well as the loss properties. This includes the heat loss at the rejection temperature (heat quality) as well as the power required for coolant pumping. The cable design is sensitive to the fault current margins required, the topology of the cable, the superconductor type, and the operating temperature of the cable.

Cable impedance values are also desired for the cables. This information will be used to determine the fault response for the architecture. Current impedance information reported from the cable model is limited to estimated resistive losses based on cable length.

5.3.1 Cable Layout

There are many superconducting cable concepts (Ref. 125). Generally, cable concepts fall into two categories: coaxially arranged cables with multiple conductors and parallel runs of single conductor cables. For the purposes of this model a Nexans Triax cable configuration was selected (Ref. 126).

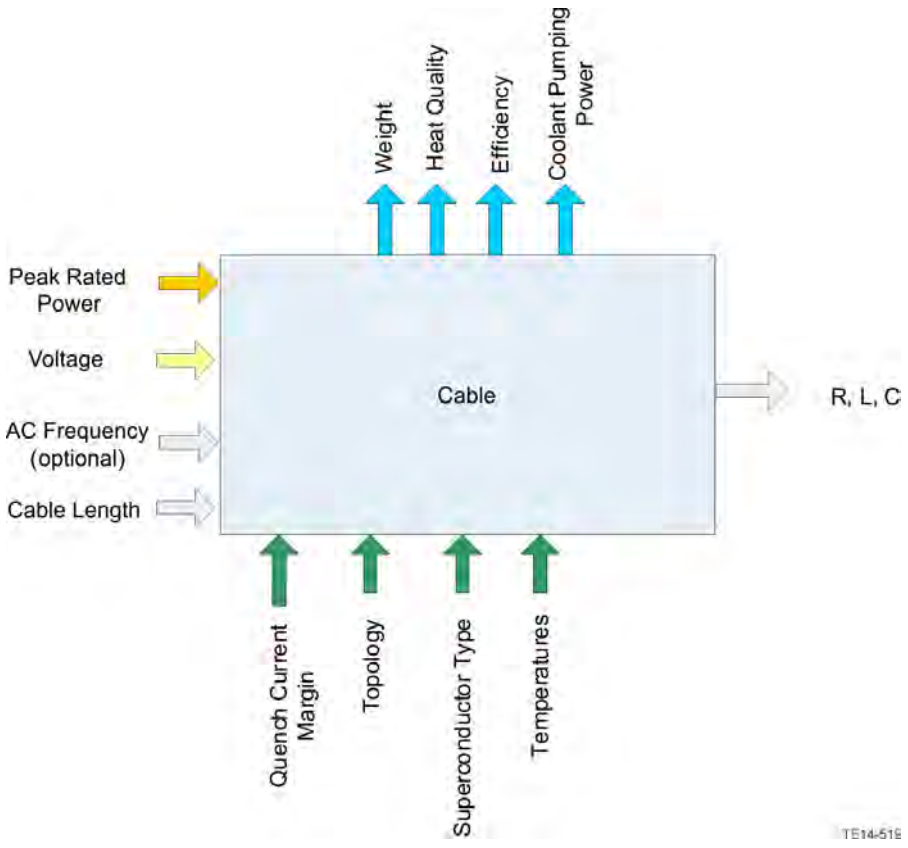

Figure 68.—Parameter Diagram for Cable Model.

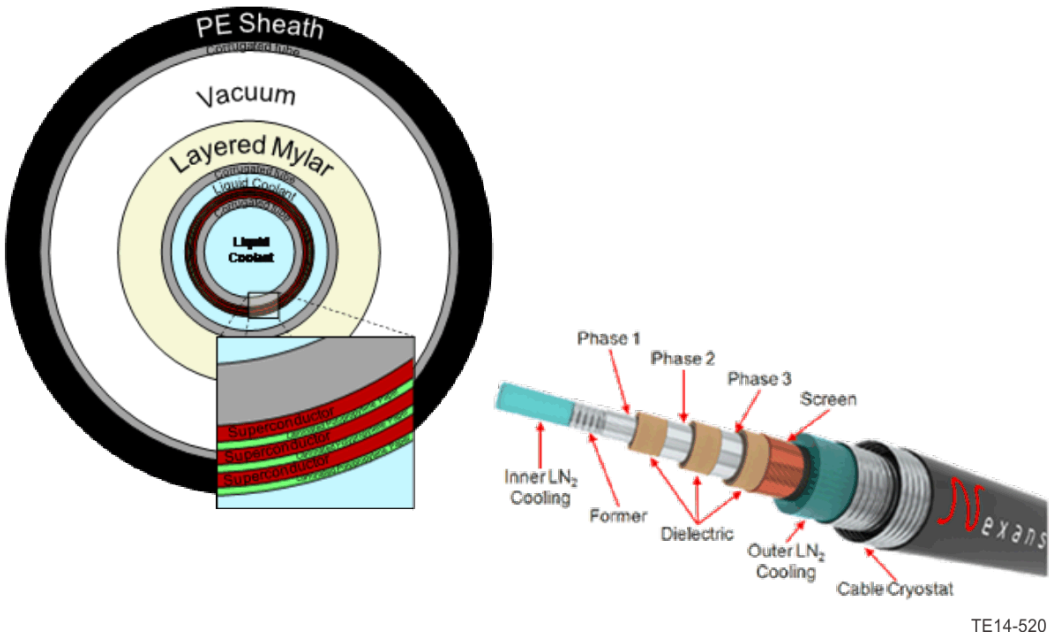

Figure 69.—Modeled Cable Layout.

As illustrated in Figure 69, this cable formed around a hollow mandrel through which liquid coolant is pumped. This mandrel is wound with layers of superconducting material and dielectric insulation. These layers are bathed in another layer of coolant. This coolant is contained within a vacuum cryostat lined on the inner surface with layered Mylar film insulation to reduce radiated heat from the outside environment to the cable.

The Nexans configuration includes a copper EMI screen for three phase AC applications. For the bi-polar DC configuration of this cable the copper screen is removed.

The lack of quench conductors in this Nexans cable requires that the superconductor be sized to withstand all overcurrents for the systems. Therefore, the protection systems must be configured in a manner which allows enables this capability. Including superconducting fault current limiters in the protection system provides support for this assumption. With adequate protection, quench does not occur in the cable itself, but is managed at the fault current limiter pinch points.

Four cable configurations are modelled with this cable topology. Three of these calculations DC: Monopolar, Bipolar with 100 percent single pole loss capability, and bipolar with 50 percent single pole loss capability. The final configuration is a three phase AC capability. Both bipolar DC configuration and the three-phase AC configuration take advantage of the Triax cable layout, while the monopolar DC configures only requires a two wire coaxial layout.

5.3.2 Monopolar, Bipolar, Redundancy and Three Phase AC

Sizing for these different configurations is driven primarily by the carrying current for each conducting element and the strength of the dielectric material required between each superconducting layer. For the three-phase AC cable, the insulation is configured to manage the max phase to phase voltage differential. The bipolar configuration requires a dielectric thickness depending on the voltage differential applied between the central ground conductors during a single phase short scenario. In order to minimize dielectric thickness, the neutral or ground conductor is situated between the two positive and negative conductors in the bipolar configuration.

5.3.3 Superconducting Material

The required thickness of the superconducting material is based on its current carrying capacity. The critical current density (J_c) for a superconducting material depends is a function of the operating temperature the magnetic to which the material is exposed. A comparison of superconducting performance for various superconducting material is Figure 70.

Specific trends of critical current density for 3 superconducting material were included in the cable models. These materials are YBCO, MgB_2, and BSCCO. The applied field and operating temperature scaling of critical current density of these materials were applied according to the relationships shown in Figure 71 and Figure 72.

Figure 71 illustrates the sensitivity of YBCO tape to operating temperature and both a parallel and perpendicular magnetic field. YBCO exhibits preferable superconducting capability. Especially at very low temperatures, the critical current density is very high and insensitive to the applied magnetic field.

The published critical current densities for HyperTech's BSCCO round wire are illustrated in Figure 72. This graph gives the material critical current density (J_c) and the engineering critical current density (J_e). The engineering critical current density is given as roughly an order of magnitude below the material critical current density. This scaling of performance is implemented in the cable sizing model via a performance factor of 0.1 applied to J_c.

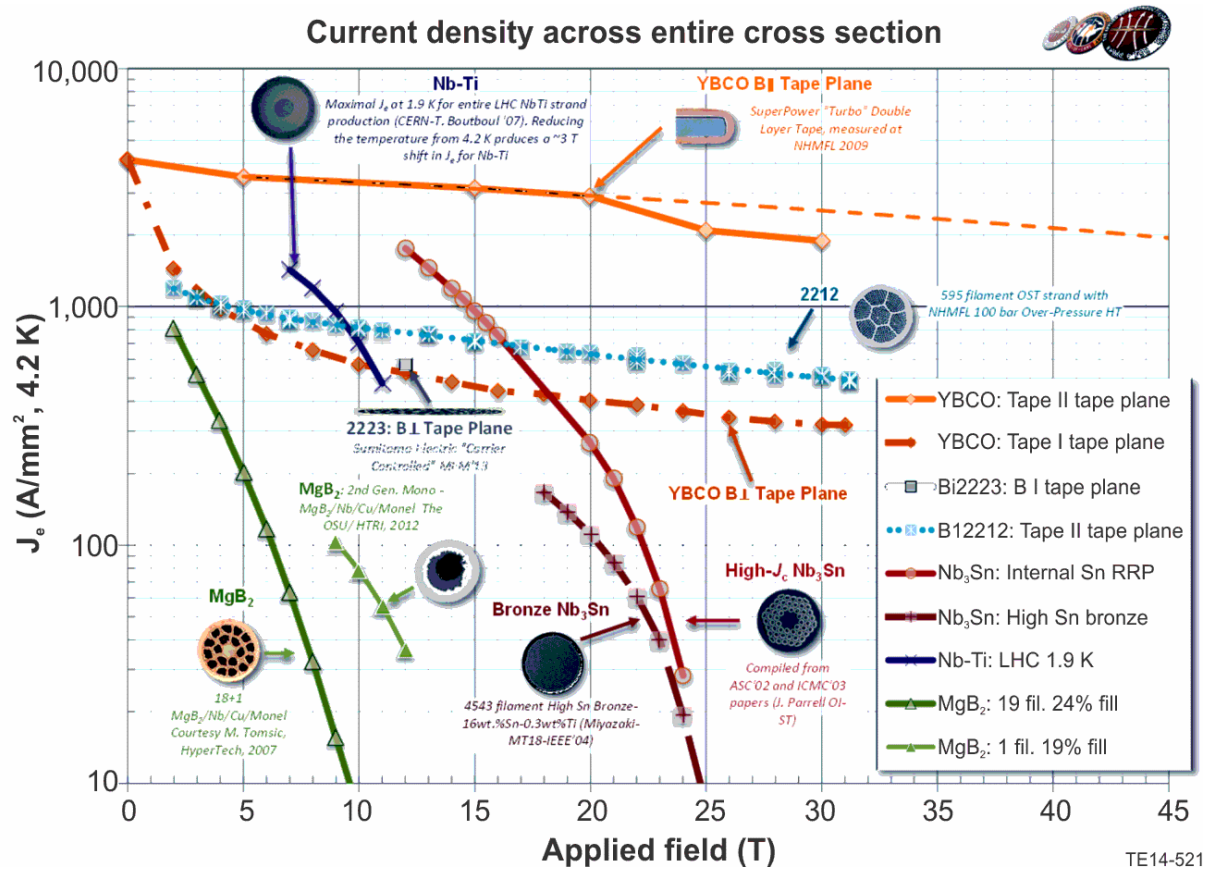

Figure 70.—Comparison of Critical Current Density for Various Superconducting Materials (Ref. 127).

Following the application of the Nexans cable concept, it is assumed that the cable applies a wrapped tape construction approach. The cross sectional area of the conductor is determined by assigning a max operating current and estimating the critical current density based on temperature and field. This then determines the thickness of the tape required.

Conductor mass depends on the material applied. Density values of 6.38, 2.57, and 6.5 g/cm^3 were applied for YBCO, MgB_2, and BSCCO, respectively.

5.3.4 Applied Field

For the purposes of the cable sizing it was assumed that there is no externally applied field acting on the cables.

5.3.5 Cryostat

The cryostat performance and weight approximations were estimated using published geometry, performance, and weight data from Nexans Cryoflex cryostat datasheets (Refs. 128 and 129). Cryoflex consists of two coaxially configured corrugated metal tubes, the inner wrapped with layered Mylar insulation. A vacuum is pulled between these layers to minimize the heat leakage into the cable from the environment. The layout and cable information are given in Figure 73.

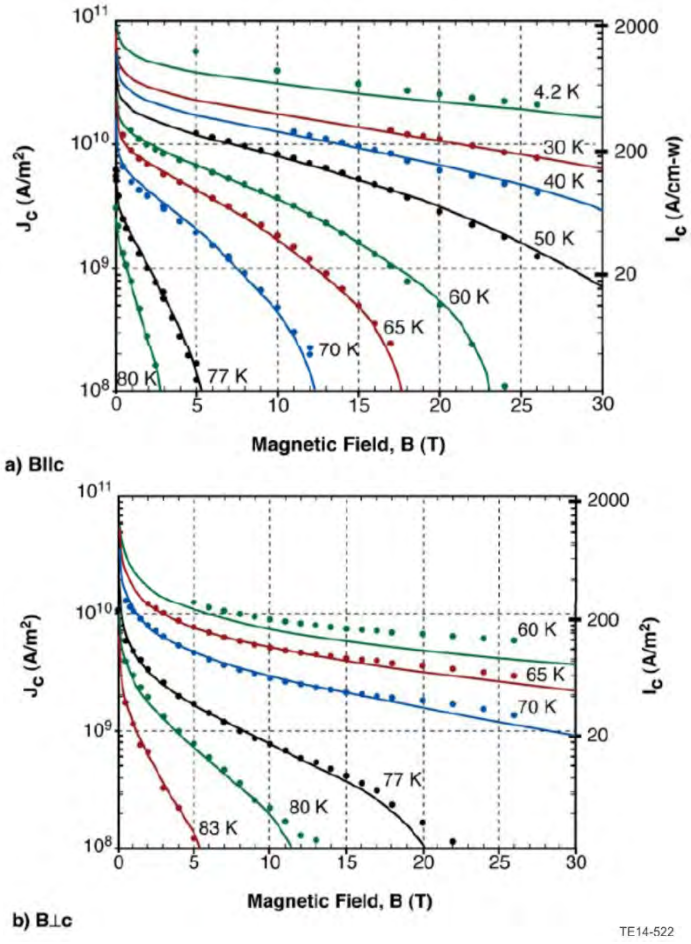

Figure 71.—YBCO Critical Current Density Sensitivity to Temperature and Field (Ref. 130).

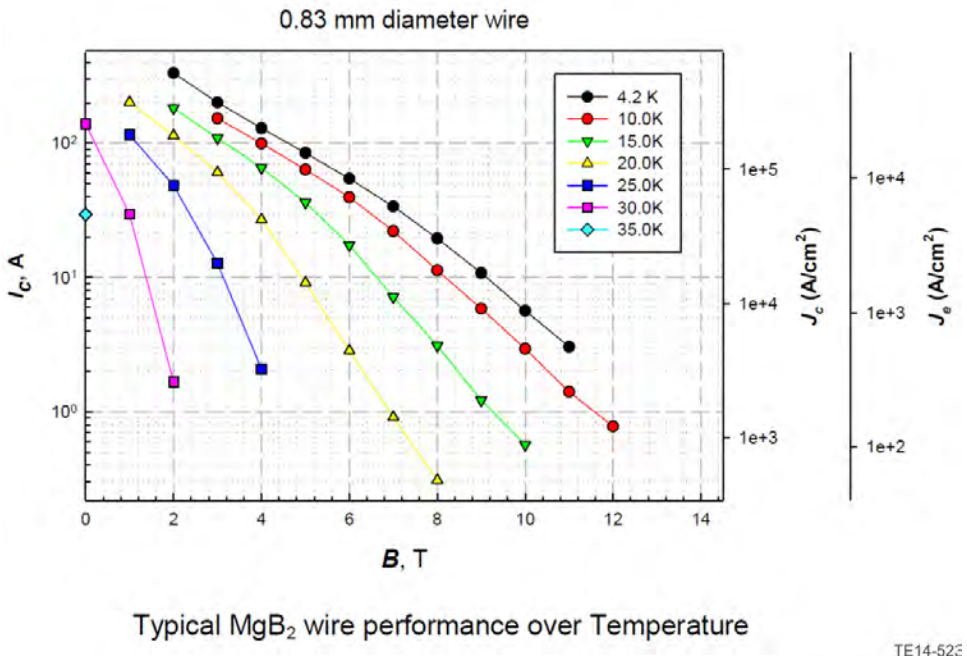

Figure 72.—MgB_2 Critical Current Density Sensitivity to Temperature and Field (Ref. 131).

Description		Dimensions (mm)				
I.D. of inner corrugated tube	A	14	21	30	39	60
O.D. of outer corrugated tube	B	34	44	58	66	110
O.D. of PE-jacket	C	38	48	62	70	115
Length of rigid tube end	D	175	190	205	210	250
	D_1	335	340	355	360	470
Length of bendable tube	E	to be specified by customer				
O.D of rigid tube end	G	54	54	76	76	128
	G_1	170	170	190	190	240
Overall length	L	almost unlimited				
Desired connection	N	Standard couplings or to customer's specification				
Min. bending radius						
Several bends	R	600	700	900	1100	2000
One bend	R	300	350	450	550	1000
Heat inleak watt/meter		0.4	0.6	0,8	1.0	1.2
Weight/meter (kg)		0.5	0.8	1.3	1.7	4.0

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Figure 73.—Cryoflex Physical Properties (Ref. 132).

Trends for cryostat outer diameter as well as the overall insulation system mass were created given this data and are illustrated in Figure 74 and Figure 75. These trends were used to estimate the physical properties of the cable system.

It was assumed that the inner cryogenic return fluid flow tube around which the superconducting material is wound has a diameter of 5 mm. The cross-sectional area of the outer coolant flow channel is the same as the inner.

The wall thickness of the corrugated stainless steel tubing was assumed to 1 mm and the roughness coefficient was assumed to be 0.02 for Reynolds number flow calculations

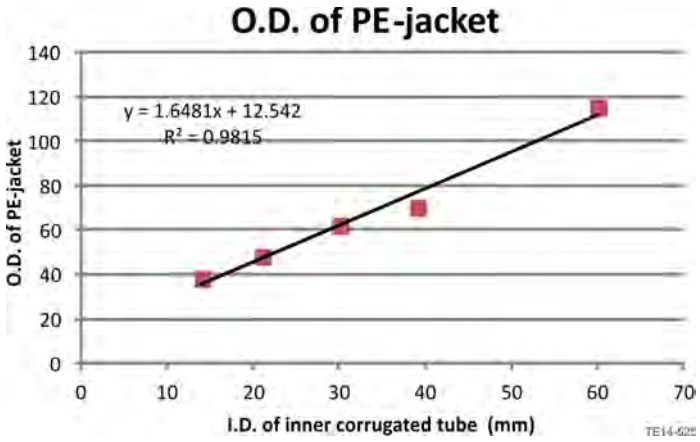


Figure 74.—Trend for Cryostat Outer Diameter in as a Function of Cryostat Inner Diameter from Cryoflex Data.

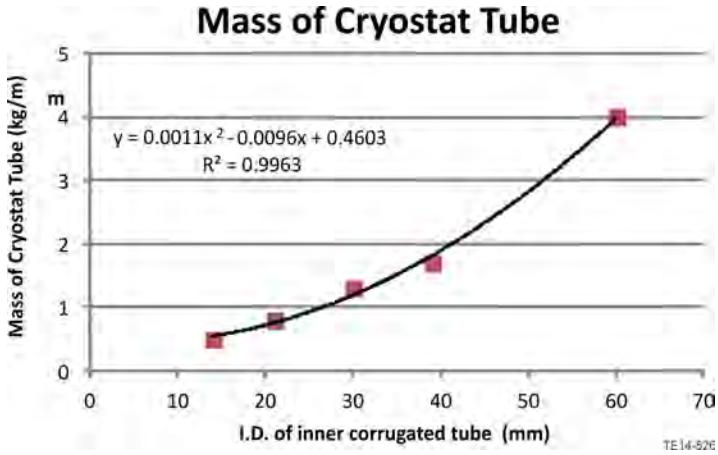


Figure 75.—Trend for Cryostat Linear Mass as a Function of Inner Diameter from Cryoflex Data.

TABLE 18.—COOLANT PHYSICAL PARAMETERS ASSUMPTIONS

	LN_2	LH_2
Density, kg/m^3	810	71
Dynamic viscosity, μPa	140	150
Specific heat	11.8 at 20 K	2.23 at 70 K

5.3.6 Cooling

Data from both liquid hydrogen and liquid nitrogen was used in this model depending on the type of superconductor selected. Coolant parameters are given in Table 18.

5.3.7 Losses

The role of the cryostat is to maintain appropriate operating temperature for the superconducting cables. The primary source of inefficiencies for a DC superconducting cable system is not due to losses in the cable itself, but heat leakages into the system from the environment (Refs. 133 and 134) As such, the heat leakage into the cable was estimated using the Cryoflex physical data (Ref. 135), illustrated in Figure 76.

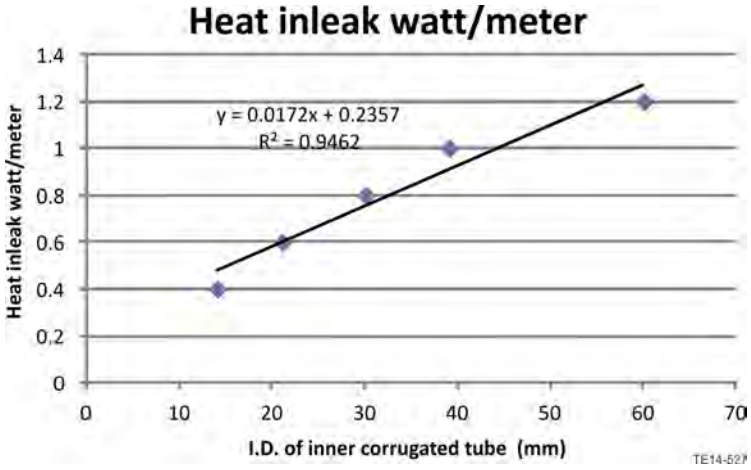


Figure 76.—Heat Leakage per Meter from the Environment to the Cryofluid from Cryoflex Data.

Additionally, research shows a potential 34 percent improvement in cryostat performance is available with alternative cryostat configurations (Ref. 136). Therefore, this estimated heat leakage value can be scaled to represent future technology improvements.

5.3.8 AC Losses

AC superconducting cables introduce additional conduction losses which effect coolant flow requirements (Ref. 137). The AC losses are a log-log function of the RMS current and the AC frequency. Figure 77 illustrates the trend used to estimate the losses per unit length for the AC portions of this superconducting microgrid.

The losses on a superconducting AC cable are a function of frequency and the ratio between the critical current and the operating current. In this report, this is termed the critical current ratio. The critical current ratio is used in the cable to trade between conduction losses and additional conductor mass.

DC cable efficiency is also a function of critical current ratio. This trend is illustrated in Figure 78.

5.3.9 Dielectric

The dielectric referenced in this study was laminated polypropylene paper (LPP) due to its favorable performance at low temperature. Referencing Cheon et al., (Ref. 138), it was assumed that the dielectric strength was 50 kV/mm. While this value is sensitive to the number of layers of the LPP and the electrical signal (AC, DC, or Impulse) and the pressure, this assumption provides a reasonable estimate for dielectric performance. Dielectric performance is illustrated in Figure 79.

The thickness and weight of the LPP depends on the off-stand voltage and the material density. For the 100 percent redundant bipolar configuration, each layer of dielectric insulation must be able to withstand the nominal off-stand voltage. During a failure of the negative pole, the neutral conductor operates at the negative voltage. For the 50 percent redundant system the dielectric material must withstand 50 percent of the total off-stand voltage; maintaining the positive or negative pole with respect to a neutral ground conductor. During a failure of the negative pole in this scenario, the neutral pole remains neutral and the power available is reduced to half to the original capability.

For the AC case, the dielectric is sized considering the peak to peak voltage. The density of the LPP was set at 900 kg/m^3 (Refs. 139 and 140).

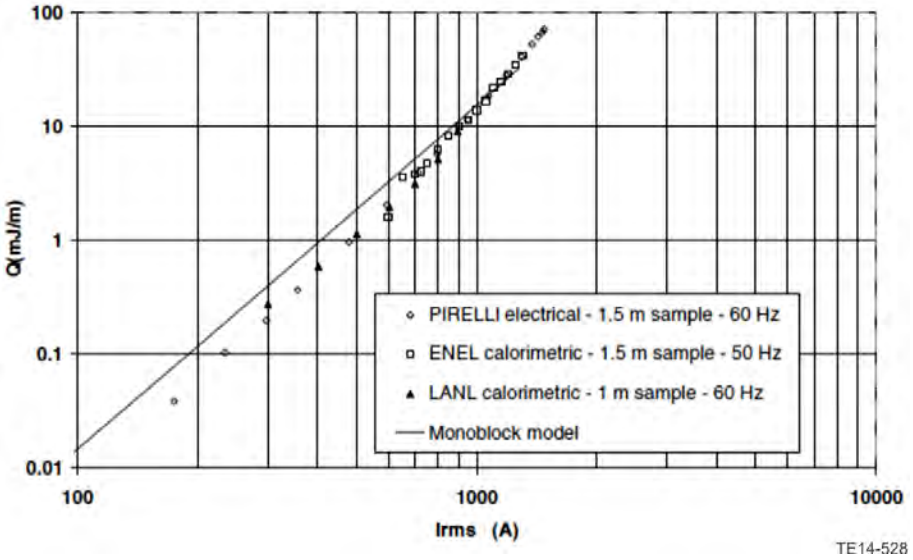


Figure 77.—Superconductor AC Losses (Ref. 141).

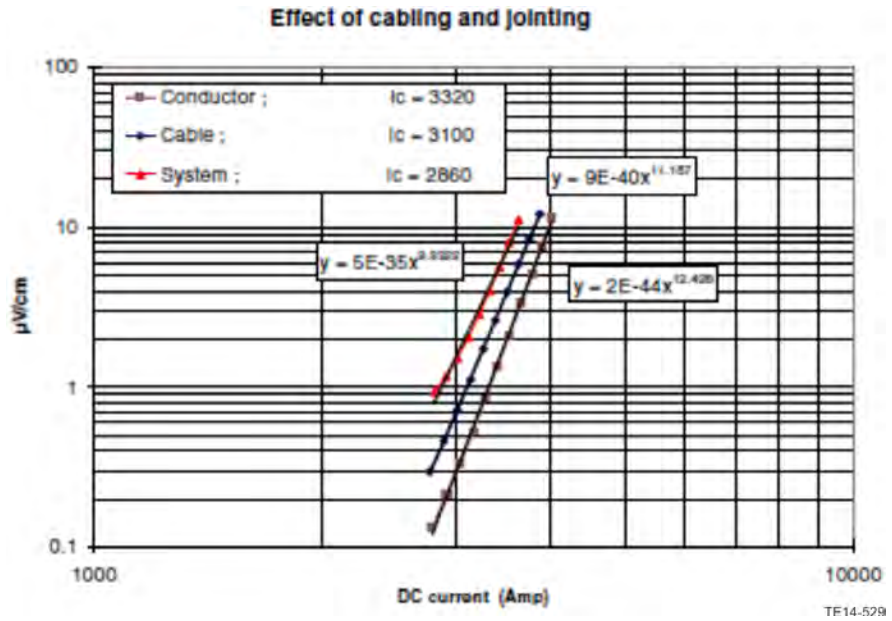


Figure 78.—Superconducting DC Losses (Ref. 141).

5.3.10 Mass and Efficiency Trends

This section presents the sensitivity of the cable mass, diameter, and losses in terms of the operating voltage. The variation in these parameters was observed while varying the cable power rating, the operating voltage, the configuration (AC or 50 percent redundant bipolar DC), and the AC frequency where applicable. The values sampled in this study are given in Table 19.

The remaining assumptions applied in executing this sensitivity study are listed in Table 20. Cryogenic assumptions are given in Section 5.8.

Several independent variables were selected to minimize the predicted mass of the overall system (including the cryogenic system). The optimized parameters are given in Table 21. Pipe flow diameters and critical current ratio both affect the cable weight via conductor and coolant mass. However, they also affect the cooling system requirements by changing the pumping power required and the cable losses.

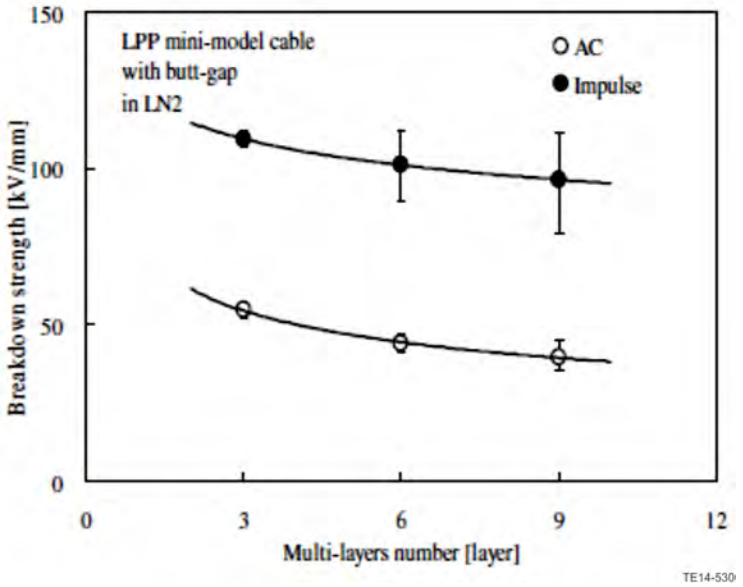


Figure 79.—Dielectric Performance (Ref. 138).

TABLE 19.—CABLE SENSITIVITY STUDY VARIABLE RANGES

Variable	Values
Power, MW	2, 4, 6, 8, 10, 12, 14, 16, 18, 20
Voltage, kV (RMS if AC, ±X if DC)	2, 4, 6, 8, 10, 15, 20, 25, 30, 35
AC or DC	AC, DC
AC frequency, Hz	NA, 100, 200, 300, 400, 500

TABLE 20.—CABLE VOLTAGE SENSITIVITY STUDY ASSUMPTIONS

Variable	Value
Superconducting material	YBCO
Conductor density	6380 kg/m^3
Critical current density (J_c)	2.00×10^{10} A/m^2
Cooling medium	LN_2
Temperature	70 K
Final temperature	77 K
Coolant density	810 kg/m^3
Dynamic viscosity	150 µPa*s
Specific heat	2.14 kJ/kg*K
Stainless wall thickness	1 mm
Ambient temperature	300 K
Applied field (perpendicular)	0 T
Inner cooling flow diameter	0.005 m
Pipe roughness	0.02
Safety factor (engineering J_e/J_c)	0.1
Insulator dielectric strength (LPP)	50 kV/mm
LPP density	900 kg/m^3

TABLE 21.—CABLE OPTIMIZATION VARIABLES

Variable	Range
Cooling flow pipe diameter, m	$(0,\infty)$
Critical current ratio	(0, 1]

In general, the mass and diameter sensitivities take the form of a unimodal curve with a minimum mass between 4 and 10 kV. The downward slope at very low voltages is generated due to increased conductor mass and thickness. The upwards slope at higher voltages is the result of increased insulation mass and thickness.

5.3.11 DC Cable

The sensitivity results for the DC cable are given in Figure 80 and Figure 81. The geometry and mass of these cables were determined for a 30-m length cable. Overall cable and cryogenic system mass approximations are balanced taking the associated heat leakage from the environment into account.

Figure 80 shows the mass and diameter sensitivity to voltage for the 12 MW DC case. This case is of interest due to power level. The power transmission requirement for the architecture of interest is 12.5 MW. In this case, the minimum cable weight per meter length is approximately 0.595 kg/m. This is achieved at around ±6 kV DC.

Figure 81 shows the variation in optimal voltage as a function of overall power. The optimal voltage for a 2 MW cable is roughly 4 kV, while the optimal voltage for the 20 MW cable is approximately 10 kV shows the variation in overall cable diameter as a function of voltage for multiple power levels.

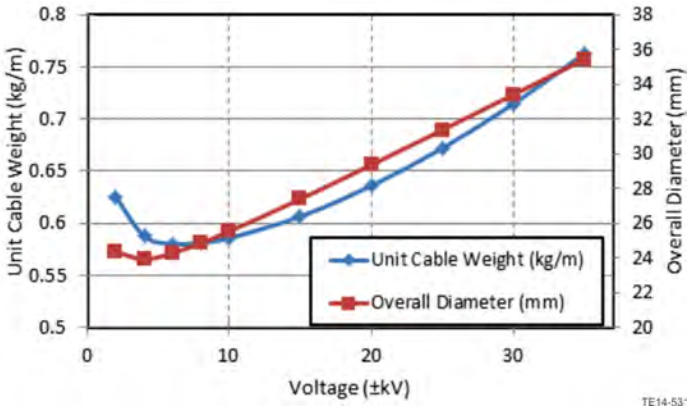


Figure 80.—Mass and Diameter Voltage Sensitivities for a 12 MW capable LN_2 Cooled Triax YBCO Bipolar DC Cable.

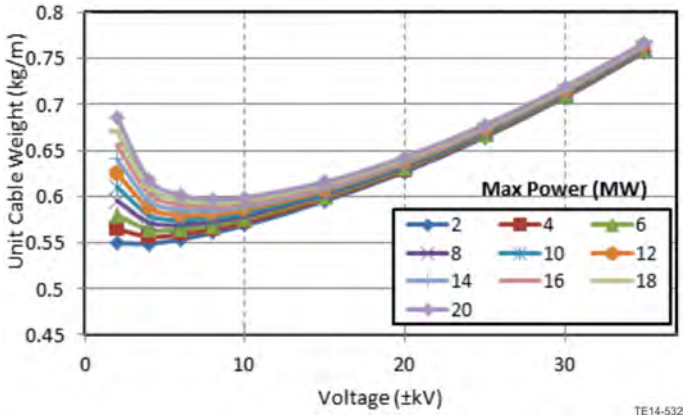


Figure 81.—Per Unit Mass Voltage Sensitivity for LN_2 Cooled Triax YBCO Superconducting Bipolar DC Cable.

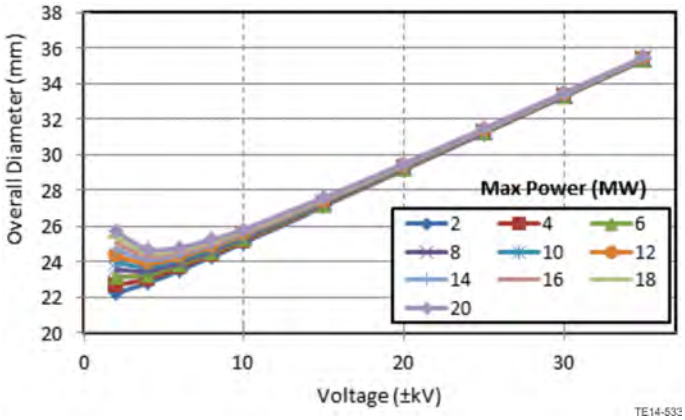


Figure 82.—Diameter Sensitivity for LN_2 Cooled Triax YBCO Superconducting Bipolar DC Cable.

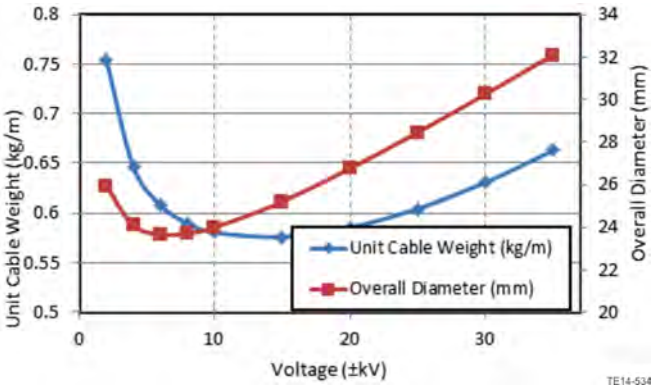


Figure 83.—Per Unit Mass and Diameter Voltage Sensitivities for a 12 MW capable LN_2 Cooled Triax YBCO Superconducting Three-Phase AC Cable at a Frequency of 400 Hz.

5.3.12 AC Cable

The mass and diameter sensitivity results for the AC cables are given in Figure 83, Figure 84, and Figure 85. The AC cable geometry and mass are determined assuming 1 m cable runs with their associated heat leakage from the environment. This significantly reduces the contribution of cryogenic systems during mass minimization. Considering the cooling system mass in the cable construction, the shorter the cable runs leads to a lower per unit mass.

As illustrated in Figure 83, the general trends for the 12 MW three-phase AC cable are similar the 12 MW bipolar DC cables discussed previously. However, the optimal voltage shifts to ±15 kV_{rms}. The optimal cable mass is also similar for the AC and DC cables. The mass per meter of the AC cable is approximately 0.576 kg/m. This reduction in per unit mass compared to the DC result is due to the ability to optimize cable design with little effect on cryocooling requirements (short length).

Comparable to the bipolar DC case optimal voltage for the AC cable also shifts depending on the power level. This is illustrated in Figure 84. However, as the power level increases the optimal trend tends to become shallower; the system mass is less sensitive to the selected voltage between 8 and 25 kV_{rms}.

Figure 85 illustrates the sensitivity of diameter to voltage for the cable. This diameter is slightly larger in the AC case compared to the DC case due to the increased insulation thickness.

5.3.13 Cable Losses

Heat leakage and conduction losses for superconducting cable systems are illustrated in Figure 86. In general, reductions in operating currents reduce the conduction losses for both AC and DC cable configurations. However, the heat leakage from the environment increase with voltage due to overall cable diameter increases.

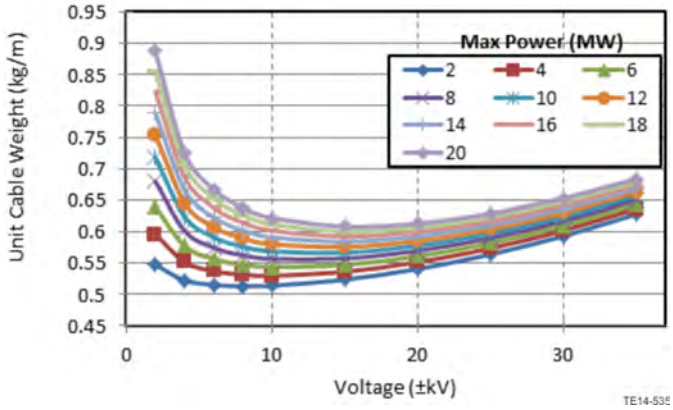


Figure 84.—Per Unit Mass Voltage Sensitivity for LN_2 Cooled Triax YBCO Superconducting Three-Phase AC Cable.

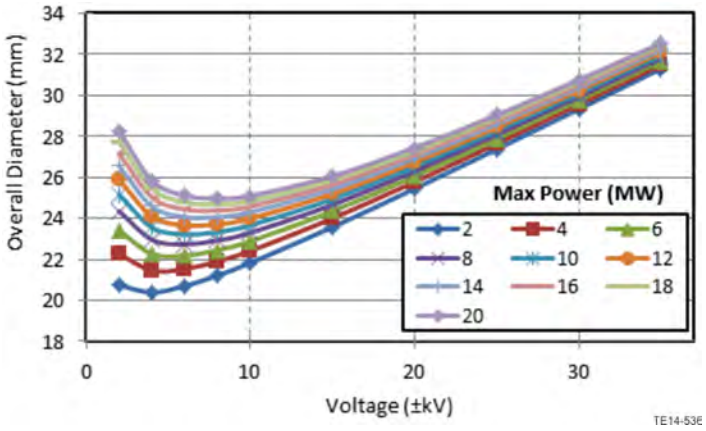


Figure 85.—Diameter Sensitivity for LN_2 Cooled Triax YBCO Superconducting Three-Phase AC Cable.

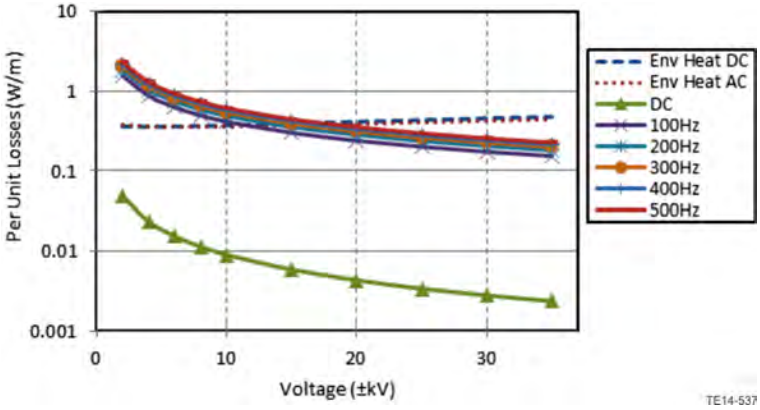


Figure 86.—Per Length Superconducting Conduction Losses and Environmental Heating as a Function of Voltage.

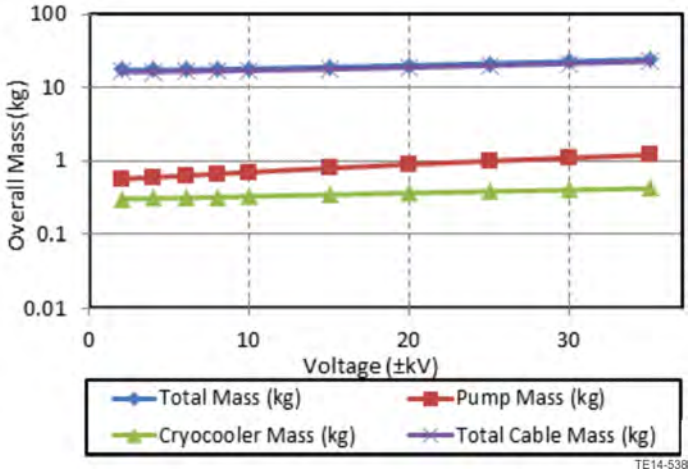


Figure 87.—DC Cable and Support Systems Mass Contributions.

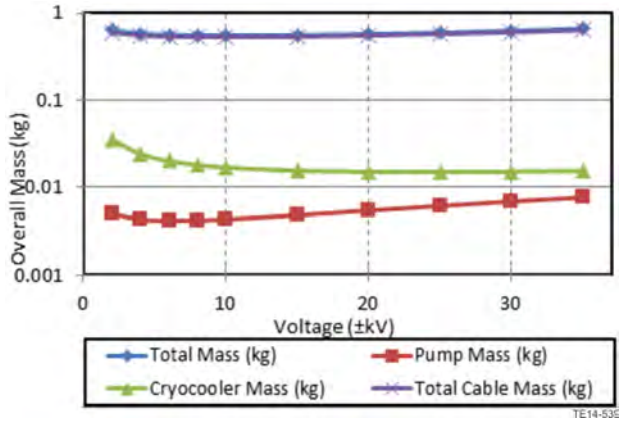


Figure 88.—DC Cable and Support Systems Mass Contributions.

The AC cable losses are over an order of magnitude higher than the losses for a DC cable. However, they are of the same general magnitude as the environmental leakage values.

The heat leakage and conduction losses lead to increase in overall system mass from cryogenic cooling system. These contributions are illustrated in Figure 87 and Figure 88 for DC and AC systems, respectively.

Cooling systems are minor contributors to the overall systems mass. However, the results illustrated here include optimal balancing of the critical current ratio and coolant flow cross sectional areas.

5.4 Superconducting Magnetic Energy Storage

For the purposes of this sensitivity study, a superconducting magnetic energy storage (SMES) device was selected as the energy storage element. The advantages for this type of energy storage were summed up by Nielsen as follows (Ref. 142):

- Capability of absorbing and delivering large amounts of power
- High efficiency
- Long lifetime
- Short response time
- Completely static construction, low maintenance
- All electric energy storage

Within the TeDP architecture, the SMES will support bus stability and provide fill in power during loss of generating capability. This sensitivity model assumes air cored SMES in a force balanced coil (FBC) winding configuration (Refs. 143 and 144). An FBC SMES applies a winding method which allows for the management of forces within the coil.

The FBC winding configuration is shown in Figure 89.

The size of the toroidal coil is defined in terms of its major and minor radii. These radii are shown in red in Figure 90.

The ratio of major to minor radii affects the winding geometry and, in turn, the tensile and compressive forces acting on the SMES windings and structure (Ref. 145).

5.4.1 Parameter Diagram

Component sensitivity model I/O for the SMES is illustrated in the parameter diagram in Figure 91.

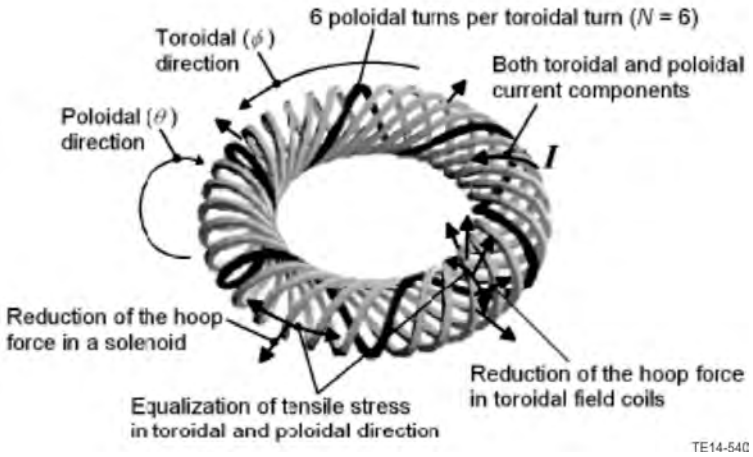


Figure 89.—Force Balanced Coil Winding Configuration (Ref. 142).

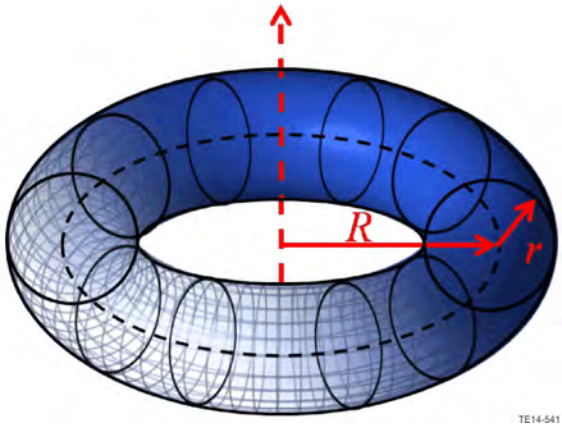


Figure 90.—Major (R) and Minor (r) Radii for the SMES Torus.

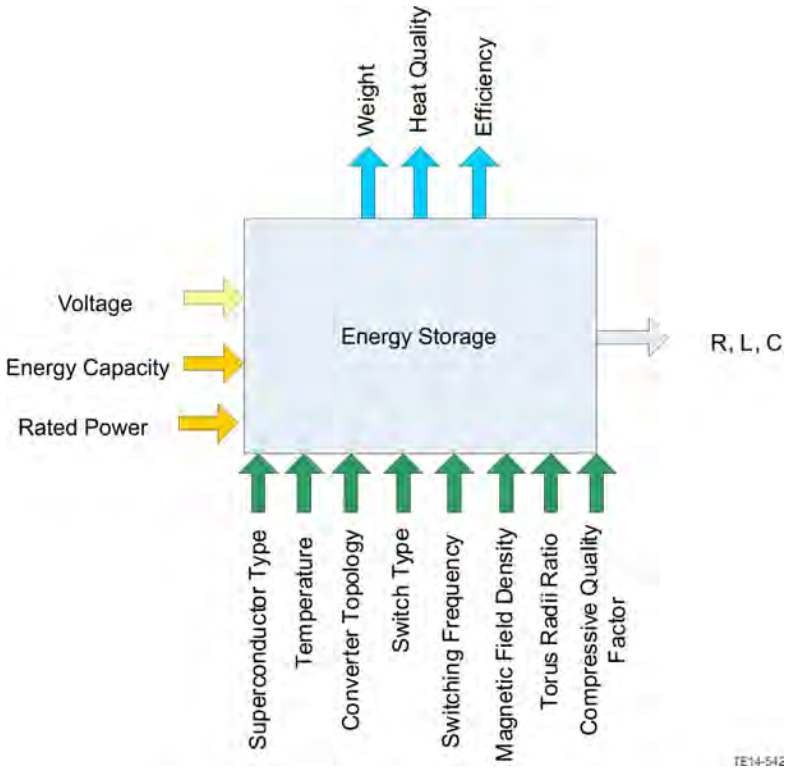


Figure 91.—Parameter Diagram for Energy Storage Device with Converter.

5.4.2 Sizing Equations

5.4.2.1 Toroidal SMES Sizing

There are a number of article extending the analysis of Moon (Ref. 146) or quoting Lorentz force, current density crossed with magnetic field (Refs. 147 and 148). Tsutsui et al. applied the point version of Maxwell's equations to an "object," in the end being a toroid SMES.

$$j \times B + \nabla \cdot S = 0$$
$$\nabla \times B = \mu_0 j$$
$$\nabla \cdot B = 0$$

The Lorentz forces are not quite as straight forward as assumed by Tsutsui et al. due to the exclusion of magnetic field in the bulk of superconducting material. Only in relatively large magnetic fields, does either type 1 or type 2 superconductors allow penetration of their surface by magnetic field.

Alternatively, ignoring the power source portion of the Poynting vector and integrating over a volume and time results in the energy within that volume for a magnetic material. Therefore, the fundamental expression which sizes the SMES device relates energy to inductance and current:

$$E = \frac{1}{2} L i^2$$

where

E Energy stored in the SMES
L SMES inductance
i SMES current

The inductance for a toroidal inductor can be calculated if the geometry and winding number are known:

$$L = N^2 \mu \frac{r^2}{2R + 2r}\left[1 + \left(\frac{r}{2R + 2r}\right)^2\right]$$

where

N	number of turns
μ	SMES inductance
i	SMES current
R	major radius of the torus
r	minor radius of the torus

Substitution of the inductance equation for a toroidal coil into the energy equation for the SMES yields:

$$E = \frac{1}{4}\frac{\mu r^2}{(R + r)}\left[1 + \left(\frac{r}{2(R + r)}\right)^2\right](Ni)^2$$

This equation can be expressed as a function of the ratio of torus radii $\left(\alpha = \frac{R}{r}\right)$ instead of the minor radius:

$$E = \frac{\mu R}{4\alpha(\alpha + 1)}\left[1 + \left(\frac{1}{2(\alpha + 1)}\right)^2\right](Ni)^2$$

The product of N and i in this expression can also be expressed in terms of the SMES magnetic field strength:

$$B = \mu \frac{Ni}{2\pi R} \Rightarrow Ni = \frac{2\pi BR}{\mu}$$

This yields an expression for energy in terms of the major radius, the magnetic field density, and the ratio of torus dimensions:

$$E = R^3 \frac{\pi^2 B^2}{\mu}\frac{1}{\alpha(\alpha + 1)}\left[1 + \left(\frac{1}{2(\alpha + 1)}\right)^2\right]$$

Thus, the size of the magnetic coil can be expressed as a function of the energy storage required, the ratio or torus radii, and the magnetic field strength.

$$R^3 = E\left(\frac{\mu}{\pi^2 B^2}\right)\left[\frac{\alpha(\alpha+1)}{1+\left(\frac{1}{2(\alpha+1)}\right)^2}\right]$$

For typical values for α (ranging from 4 to 6 (Ref. 149)), an approximation for major radius can be used.

$$R^3 \approx E\left(\frac{\mu}{\pi^2 B^2}\right)\alpha(\alpha+1)$$

5.4.2.2 Superconductor Mass Equations

The mass of the SMES superconducting material is a function of the length, density, and cross-sectional area of the superconducting windings. The cross-sectional area is a function of current and critical current density.

$$m_{sc} = \rho_{sc} l_{sc} a_{sc} \;\Rightarrow\; m_{sc} = \rho_{sc} l_{sc} \frac{i}{J_e}$$

The number or windings is calculated from the magnetic field density equation and a simple relationship between the SMES power required and the operating voltage ($P = iV$).

$$N = \frac{2\pi BR}{\mu}\frac{V}{P}$$

The length of the superconducting windings can then be calculated considering the toroidal geometry.

$$l_{sc} = 2\pi N\sqrt{r^2 + \left(\frac{R}{N}\right)^2}$$

Combining these equations gives an expression for superconductor mass.

$$m_{sc} = \rho_{sc}\frac{4\pi^2 BR}{\mu J_e}\left[r^2 + \left(\frac{\mu}{2\pi B}\frac{P}{V}\right)^2\right]^{\frac{1}{2}}$$

From this expression we see that the mass of the windings is a weak function of operating voltage. However, for typical SMES devices the *R/N* value is negligibly small. Therefore, the expression can be simplified to

$$m_{sc} \approx \rho_{sc}\frac{4\pi^2 BR}{\mu\alpha J_e}$$

5.4.2.3 Structural Weight Calculation

Magnetic energy storage in a toroid inductor results in compression for the minor radius and tension in the major radius. This seems to contradict with some other research. Yet, even that research seems to

diverge from later experimental research (Refs. 150, 151, 152, 153, and 154). Upon further review of literature, the fundamental Lorentz forces for superconductors seem to be in international discussion, with a conclusion not in sight. Of which, none conveniently match the normal conductor Lorentz force description, i.e., the electrical version of Newtonian versus Einsteinian. One researcher's experiments indicate that the relative mechanical force measured approaches zero when conventional definition indicates maxima (Ref. 155). Due to the ongoing research defining superconductor electromagnetic forces.

Moon's estimation was chosen for our estimations. We assumed that the "quality factor," which is a description of compression to tension relationship, is optimal. Assuming tension, a Zylon epoxy type material ratings are used. Virial theorem based SMES structural mass estimates do not show sensitivity to operating voltage (Ref. 156). The main drivers are the energy stored in the device and the material properties of the structure.

$$m_{str} = (1+2Q)\frac{\rho_{str} E}{\sigma_{str}}$$

The Q value in this expression is a ratio of tensile to compressive strength (Ref. 157). It is expected that this value will be sensitive to the ratio of torus radii. However, without a clear relationship between SMES geometry and Q value, the sensitivity results sample Q on its range from 0 to 1.

5.4.2.4 Dielectric Insulation Weight Calculation

It is assumed that the dielectric insulation is a function of the surface area of the torus (A_{Torus}), the operating voltage (V), and the number of insulation layers required (n).

$$m_{ins} = \rho_{ins} A_{Torus} \frac{V}{\kappa_{ins}}(n)$$

The equation for the surface area of a torus is given by:

$$A_{Torus} = 4\pi^2 Rr$$

The number of insulation layers depends on the number of winding layers are needed. The inner circumference of the torus, number of windings, and the geometry of the superconductor are all factored into determining how many layers of windings are required. This number is calculated with this equation:

$$n = roundup\left[\frac{N w_{sc}}{2\pi(R-r)}\right]$$

5.4.3 Power Electronics

SMES charge and discharge operations are facilitated by an H-bridge circuit (Ref. 158). This is illustrated in Figure 92 with the operating mode power flows: charge, steady state, and discharge. Power flow is maintained with two diodes and two modulated IGBTs. The control of these IGBTs determines the operating mode for the SMES system.

Diode, IGBT, and capacitor parametric sizing and efficiency models use the converter device trends discussed in Section 5.1. Output capacitance requirements require assumptions regarding the duration over which the capacitor can maintain voltage.

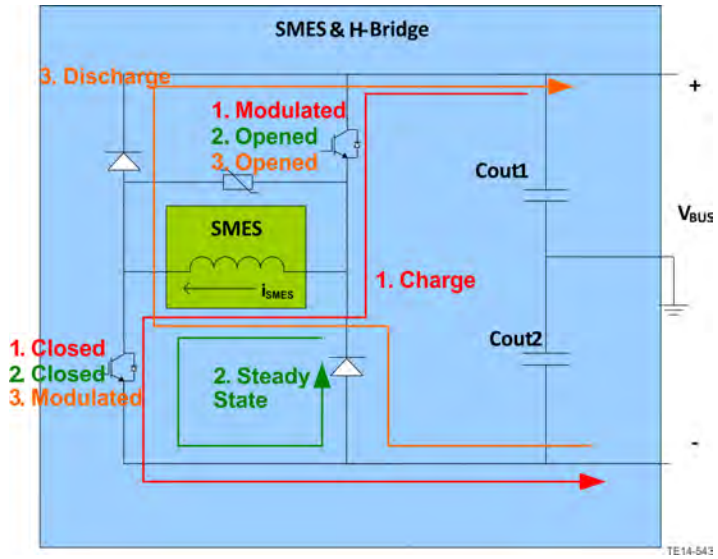


Figure 92.—SMES H-Bridge with Mode Power Flow Superimposed.

The only device illustrated in Figure 91 not modelled in the sensitivity study is the dissipative element placed in parallel to the SMES inductor. In the case of a SMES loop fault condition, this arresting device may be required to overcurrent while the energy can be dissipated during fault conditions. High power dense power dissipation device alternatives and fault tolerant SMES configurations need to be explored further to enable implementation in the TeDP architecture.

5.4.4 Cryocooling Weight Calculations

A recirculated layer of cryocoolant is required to maintain superconducting temperatures. The SMES toroidal inductor introduces some heat from conduction losses. Additionally, some heat is transferred to the coolant from the environment through the insulation. A conformal tank is used around the SMES toroid with flow of coolant around the SMES toroid as illustrated in Figure 93.

The coolant channel is sized to minimize the mass of the overall system by considering the pumping requirements and the mass of the coolant. The coolant layer is contained in a vacuum jacketed insulation system with an assumed structure as introduced in Section 5.3.5.

5.4.5 SMES Sensitivity Study Parameters and Assumption Overview

SMES sensitivity study variables ranges are provided in Table 22, and SMES voltage sensitivity study assumptions are provided in Table 23.

The overall system mass is optimized by varying the independent parameters given in Table 24. Cryogenic assumptions are given in Section 5.8.

TABLE 22.—SMES SENSITIVITY STUDY VARIABLE RANGES

Variable	Values
Aspect ratio	3, 4, 5, 6
Magnetic field	5, 7.5, 10
Energy stored, MJ	30, 60, 100, 150, 200
Operating voltage, kV	2, 4, 6, 8, 10, 12, 15, 20, 25
Compressive quality factor	0, 0.25, 0.5, 0.75, 1
Cryocoolant	LN_2, LHe, LN_2

TABLE 23.—SMES VOLTAGE SENSITIVITY STUDY ASSUMPTIONS

Variable	Value
Superconducting material	YBCO
Conductor density, kg/m^3	6380
Insulator dielectric strength (LPP), kV/mm	50
LPP density, kg/m^3	900
Structural material	Zylon fiber
Structural material density, kg/m^3	1560
Output capacitor voltage support duration, s	1
Ultimate tensile strength, GPa	5.8

TABLE 24.—SMES OPTIMIZATION VARIABLES

Variable	Range
Inlet coolant temperature, K	(Depends on medium)
Critical current ratio	(0,1)
Number of Mylar insulation layers	[0, ∞)
Coolant delta T, K	(Depends on medium and inlet temperature)
Coolant layer thickness, mm	[1, ∞)

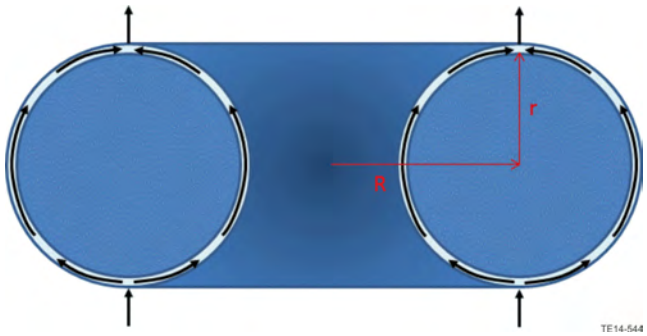


Figure 93.—SMES Coolant Flow.

5.4.6 Mass and Efficiency Trends

The mass of the structural and superconductive elements are insensitive to voltage. However, increase in voltage does affect the insulation weight due to increased off-stand voltage required and the numbers of layers of insulation. As such, assuming a fixed power requirement, the maximum energy density of the SMES coil is achieved on a SMES device by minimizing the operating voltage. To provide a fixed power, a reduction in voltage requires an increase current. Therefore, the induction requirement is reduced and the number of windings decreases.

The low voltage power density of the SMES coil must be balanced with power density of the power electronics and cooling systems both of whose power density increases with voltage. The sensitivity of the SMES to energy and voltage are illustrated in Figure 94. All results in this section apply a power requirement of 12.5 MW supplied by the SMES.

Figure 95 and Figure 96 illustrate the overall SMES system mass and energy density as a function of the amount of stored energy and operating voltage.

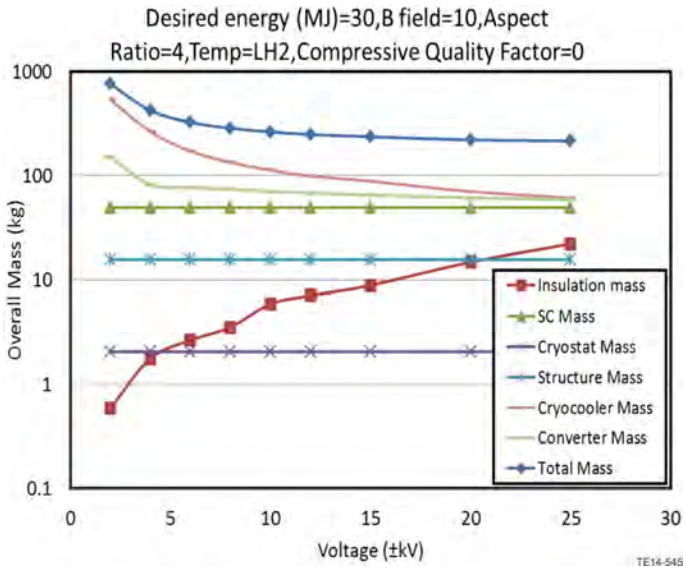


Figure 94.—Sensitivity of Overall SMES System Mass to Voltage.

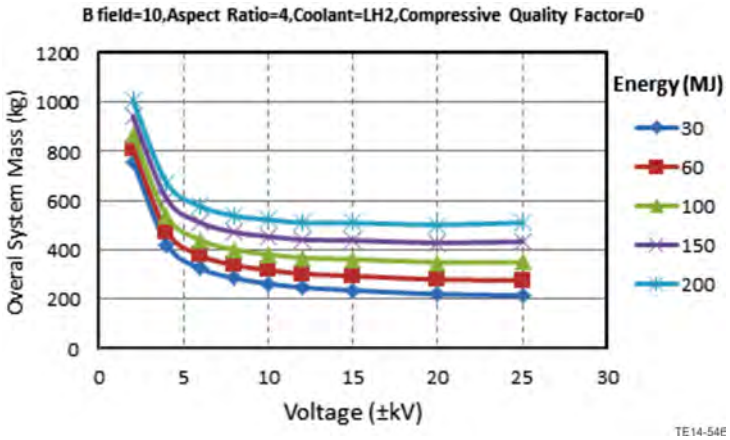


Figure 95.—Sensitivity of SMES Mass to Voltage and Energy Considering Power Electronics and Cooling Systems.

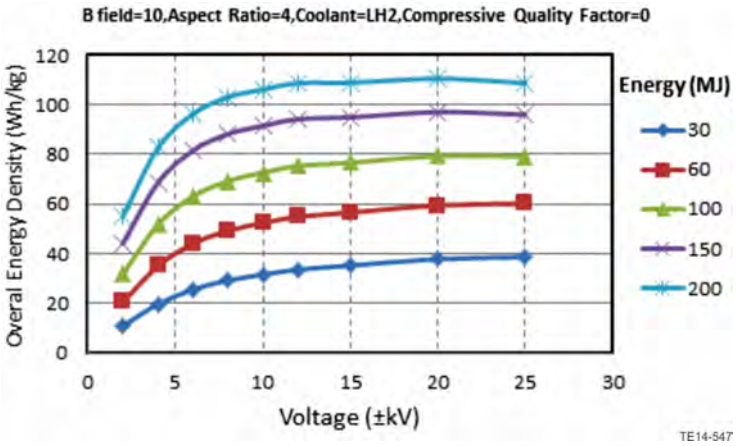


Figure 96.—Sensitivity of SMES Energy Density to Voltage and Stored Energy Considering Power Electronics and Cooling Systems.

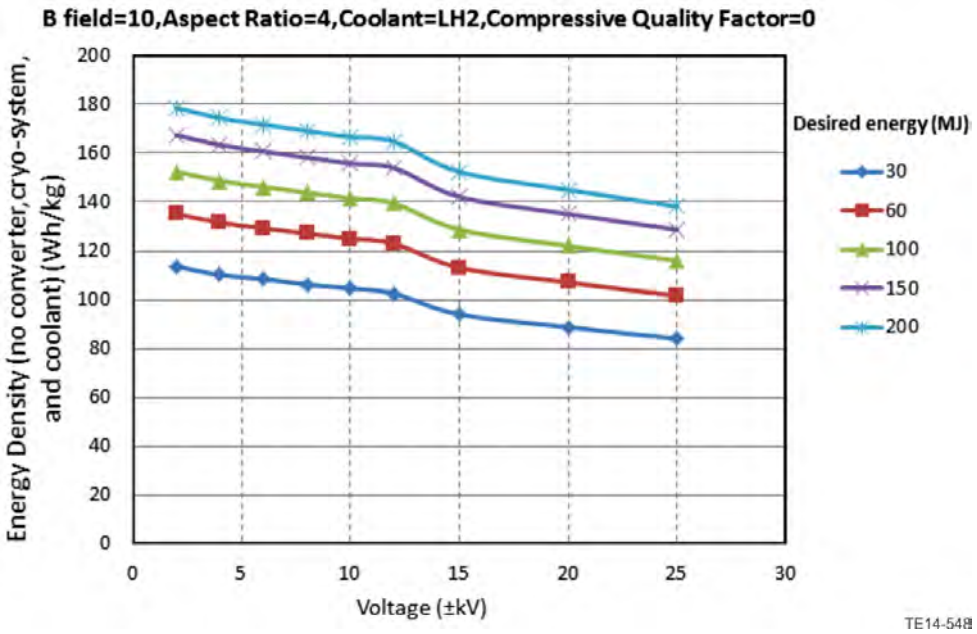


Figure 97.—Sensitivity of SMES Energy Density to Voltage and Stored Energy for Structural and Electric Components Only.

The primary driving trends for voltage selection for this system are the power electronics and cryocooling systems. The power density of the SMES toroid without the support systems is illustrated in Figure 97.

5.4.6.1 Toroidal Inductor Mass Sensitivities

Operating voltage has a large effect on the number of windings on the SMES. The mass of the superconducting material may by insensitivity to this voltage (Figure 98). However, the winding complexity increases dramatically with increased voltage. An increased number of windings requires additional layers of insulation required for dielectric protection (Figure 99).

Field, aspect ratio and the compressive quality factor play a lesser role in the SMES sensitivity. These trends are illustrated in Figure 100, Figure 101, and Figure 102.

The energy density of the SMES inductor is also sensitive to the operating temperature. By assuming the use of YBCO as the superconducting material for SMES windings, the superconducting temperature range is quite large. However, the critical current density is affected greatly by the operating temperature. This effect is illustrated in Figure 103.

The primary loss mechanisms during SMES discharge are driven by conversion and power electronics cooling. During standby operation, a fully charged SMES toroid exhibits losses as illustrated in Figure 104. These losses are driven by conduction losses in the superconductor and heat leakage from the environment.

During SMES charge and discharge at 12.5 MW, the power loss is much higher as illustrated in Figure 105.

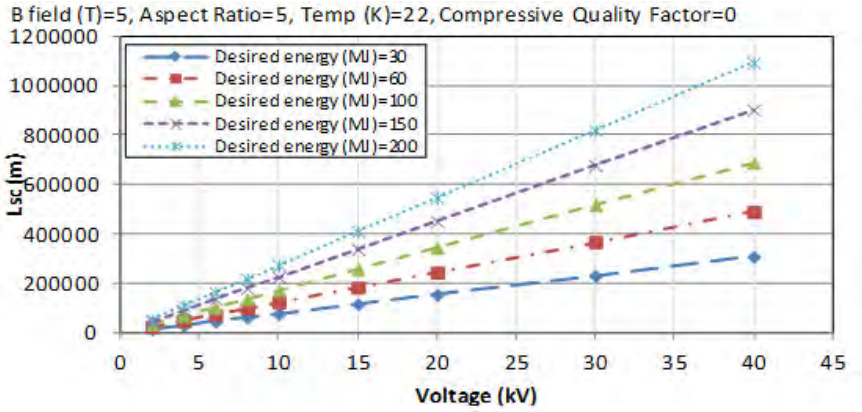


Figure 98.—Sensitivity of the Number of SMES Windings to Voltage and Stored Energy.

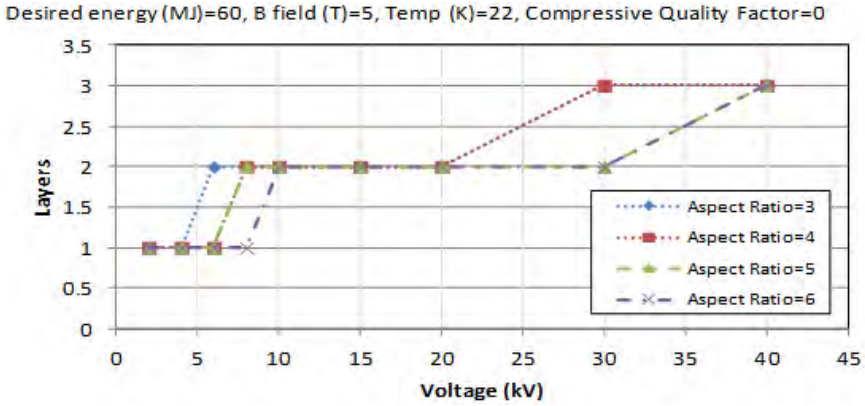


Figure 99.—Number of Layers of Superconductor Windings.

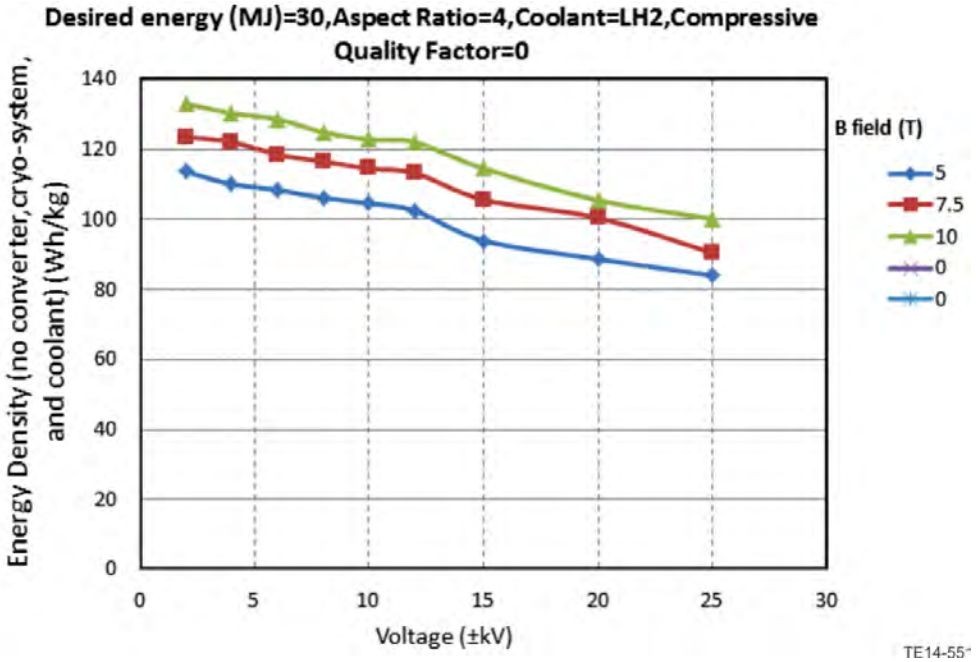


Figure 100.—Mass Sensitivity of SMES Structural and Electrical Elements to Voltage and Magnetic Field Density.

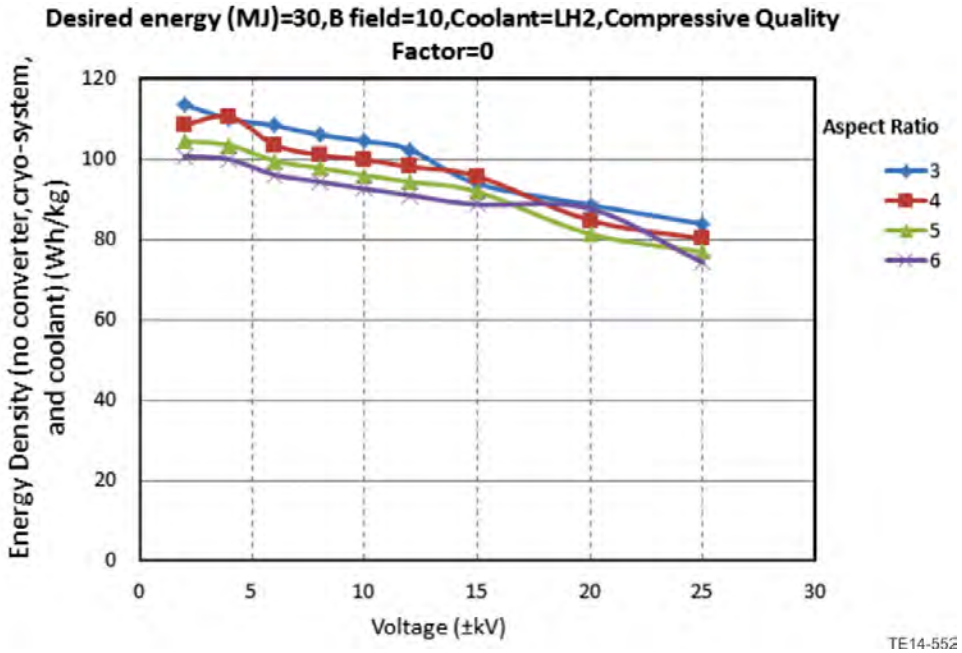


Figure 101.—Sensitivity of SMES Energy Density to Voltage and Torus Aspect Ratio.

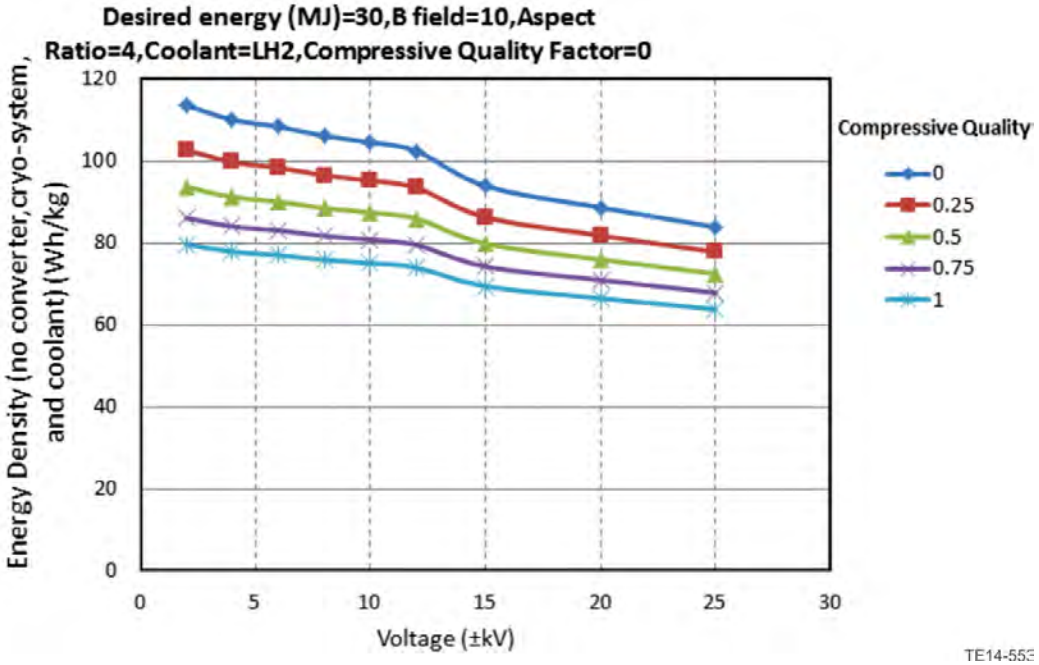


Figure 102.—Sensitivity of SMES Energy Density to Voltage and Compressive Quality Factor.

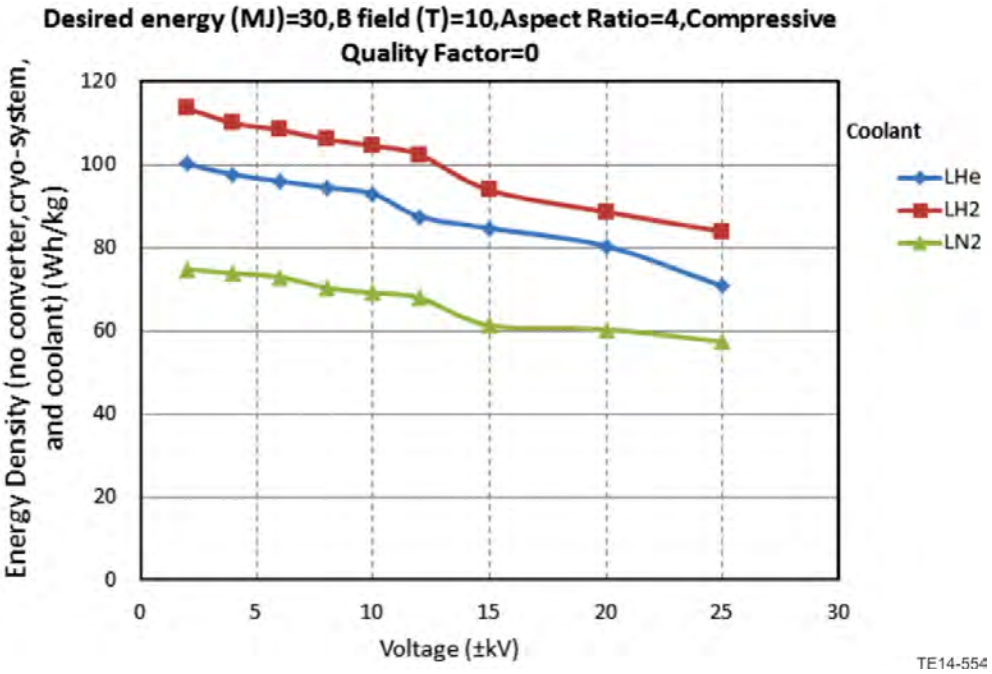


Figure 103.—Sensitivity of SMES Energy Density to Voltage and Temperature.

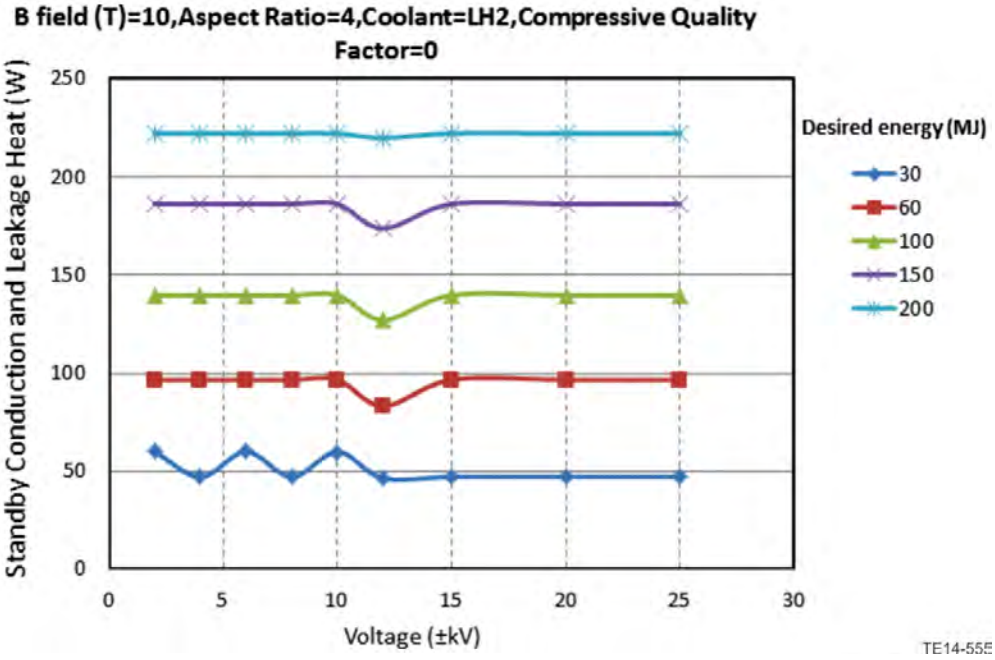


Figure 104.—Standby Losses for Fully Charged SMES Toroid.

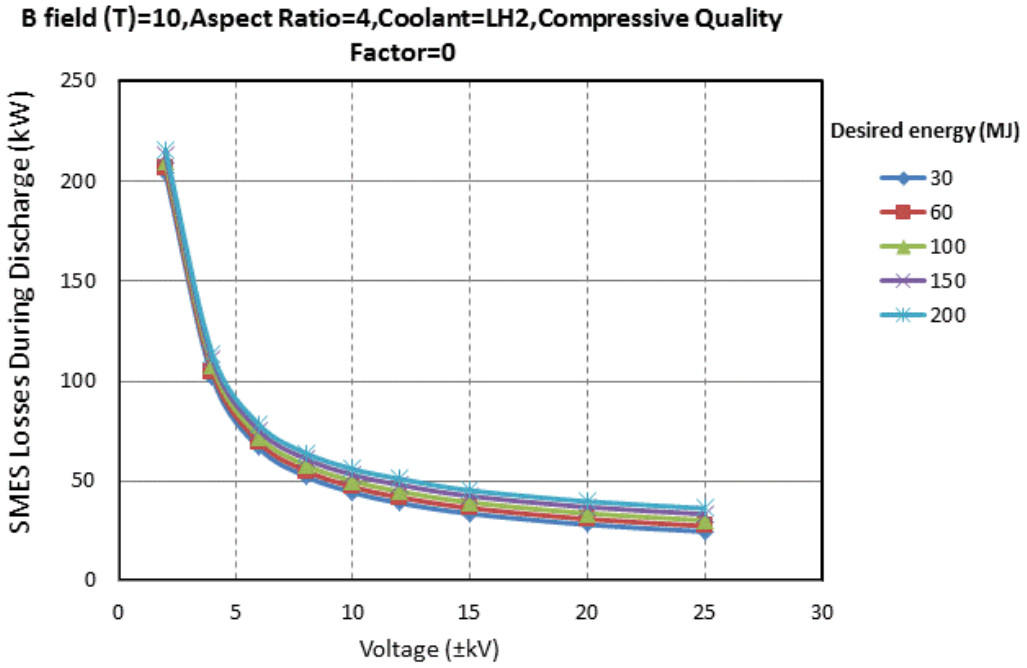


Figure 105.—SMES System Losses during 12.5 MW Charge/Discharge.

5.5 Circuit Breakers

The current interruption devices serve as the fault isolation devices for this architecture. Sections 3.4 and 4.0 discuss the types and trade-offs of electromechanical, hybrid, and solid-state circuit breakers. Schematics of examples of these types of circuit breakers are illustrated in Figure 106. Based on prior studies and simulations of DC microgrid systems (Refs. 159, 160, and 161), the time from the fault initiation to the fault current peak magnitude for this superconducting system will likely occur in several microseconds. The resulting fault energy will be subject to the system component's quench transition. If it takes longer for the protection equipment to interrupt the fault current, the equipment will have to be oversized to have a higher fault current rating, the circuit breakers will have to have higher interruption ratings and a larger cryocooler mass will be need to dissipate the fault energy generated during an event. If the circuit breaker can interrupt the fault current before the peak fault current magnitude, then the rest of the faulted system will only have to withstand a reduced peak current magnitude. The desire to minimize size and weight of the electrical components and cryocooler necessitated a very fast interruption time and based on the interruption times of the time of the considered circuit breakers, the solid-state circuit breaker was chosen for this study. This was based on the assumption that the protection system should be designed interrupt the fault current as early as possible and limit the fault current, to twice nominal current in this study. The schematic of the modeled SSCB is shown in Figure 106C. Other hybrid and SSCB topologies were previously discussed in Sections 4.3 and 4.4.

Additional interrupter models of an electromechanical and/or hybrid circuit breaker could be developed and used with system trade studies to determine the impact of the current interruption device on the system weight and efficiency.

The following sections describe the DC SSCB. An AC SSCB model would use similar scaling of the SSCB components, but the ratings of these components would differ, and the losses of the SSCB would differ.

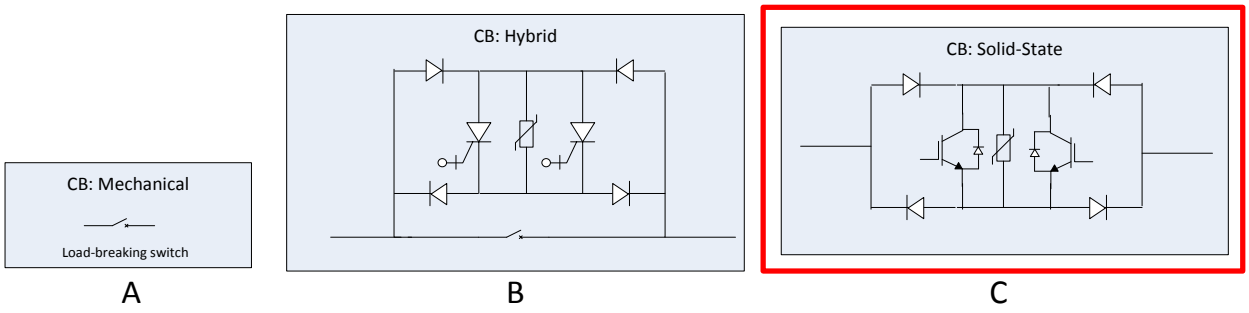


Figure 106.—Current Breaker Device Topologies. Solid-State Circuit Breaker Selected for Modeling.

5.5.1 Model Overview

5.5.1.1 Parameter Diagram

The parameter diagram shown in Figure 107 outlines the SSCB model major inputs, outputs, and control parameters. For a given rated power based on the SSCBs placement in the architecture and the desired DC voltage for study, the model estimates the SSCB mass and losses. Other control parameters used to scale the SSCB are the operating temperature and topology. For this study, the topology is fixed for the topology shown in Figure 106C. Intermediate outputs of the SSCB model are its current interruption time and fault current rating based on IGBT scaling. These outputs will be used by the protection system to coordinate SSCB and SFCL interaction. Instead of these values computed as an output of the SSCB model, they could be specified as inputs to the SSCB model by the protection system.

The SSCB model is structured similarly to the inverters and rectifiers. Given the specified rated power and DC voltage, the component voltage and current ratings are specified. From these component specifications, the component masses and losses are computed and totaled. As indicated by Figure 106C, the SSCB components are the conduction diodes, IGBTs with freewheeling diodes, and a metal oxide varistor (MOV). The MOV is used as an overvoltage protection device during switching events.

5.5.1.2 Governing Equations

Several equations are used to determine the component ratings. The nominal DC current rating is calculated by

$$I_{dc} = \frac{P_{dc}}{V_{dc,ptp}}$$

Given these ratings, the IGBT component voltage and current ratings are calculated by:

$$V_{block,IGBT} = \left(\frac{V_{dc,ptp}}{2}\right)\frac{1}{N_s}$$

$$I_{IGBT} = \frac{I_{dc}}{N_p}$$

The IGBTs are arranged in series and/or parallel in a similar manner as for the IGBT power converter scaling in order to maintain interpolation of the IGBT scaling data. The IGBT scaling data is the same for both the power converter and SSCB IGBTs.

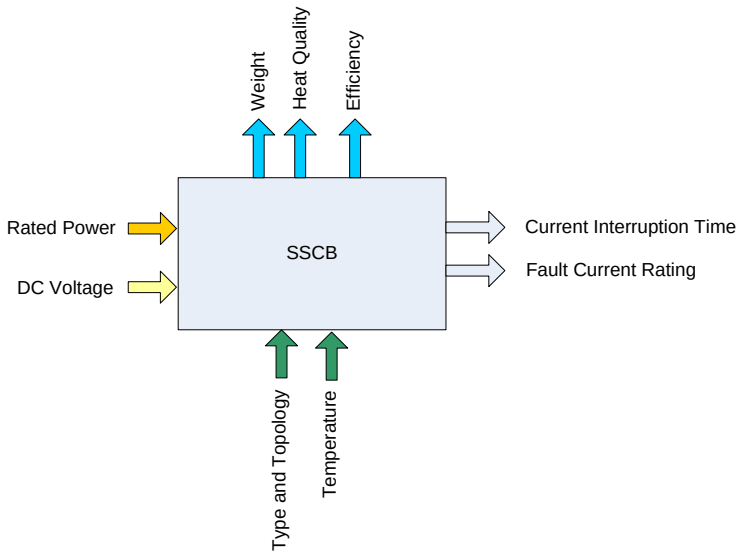


Figure 107.—Parameter Diagram for Current Interrupter.

The voltage rating is determined by half of the DC bus pole-to-pole voltage since a SSCB is used on both of the DC poles and will be required to block the single pole-to-ground voltage.

These voltage and current ratings are used by the IGBT, diode, and varistor component sizing model to estimate the mass and losses of these devices. The IGBTs are scaled based on room temperature and cryogenic test data in the same way as for the power converters. For this topology, two diodes also normally conduct along with the IGBT. The cryogenic diode scaling is the same as previously described in Section 5.2.2.2.2. The conduction diode mass is estimated as a percentage of the IGBT mass based on the ratio of an individual diode mass to a similarly rated IGBT and freewheeling diode mass. The model could be expanded to create an independent conduction diode scaling model and mass estimate.

Only the conduction losses are considered to estimate the normal operational efficiency of the SSCBs. During a switching event, the switching losses could also be estimated, but these losses are not part of the normal SSCB operation. Any type of DC circuit breaker will incur switching losses to interrupt current, but different types of DC circuit breakers have different conduction losses. The purpose of this model is to estimate the SSCB conduction losses during normal operation. The IGBT and diode conduction losses are estimated by equation

$$P_{cond} = \left(V_{CE} I_C + r_{CE} I_C^2\right) D$$

where the duty cycle is equal to 1.

The total IGBT and diode losses are calculated by

$$P_{loss} = \left(P_{cond,IGBT} + 2P_{cond,diode}\right) N_s N_p$$

Note that the SSCB can operate bidirectionally. This capability results in a SSCB with almost twice the number of components as a unidirectional SSCB. Only half of the components conduct during normal operation.

The MOV mass is estimated from existing surge arrester masses and the ratio of those masses to IGBT masses with similar voltage rating. Surge arrester data from ABB for devices rated for 1 to 2 kV and 2.5 to 4.7 kV were gathered (Refs. 162 and 163). The MOV mass estimate is calculated by:

$$M_{MOV,total} = N_s \begin{cases} \dfrac{M_{MOV1,single}}{M_{IGBT1,single}} M_{IGBT,scaled}, V_{block,IGBT} \le 2 \text{ kV} \\ \dfrac{M_{MOV2,single}}{M_{IGBT2,single}} M_{IGBT,scaled}, V_{block,IGBT} > 2 \text{ kV} \end{cases}$$

Where $M_{MOV1,single}$ is the surge arrester mass data for a voltage range of 1 to 2 kV operation, $M_{IGBT1,single}$ is the average IGBT mass for the voltage rating 1 to 2 kV, $M_{MOV1,single}$ is the surge arrester mass data for a voltage range of 2.5 to 4.7 kV, $M_{IGBT2,single}$ is the average IGBT mass for the voltage range 2.5 to 4.7 kV, and $M_{IGBT,scaled}$ is the IGBT mass estimate per the model IGBT scaling.

Further understanding of varistor operation and material properties at cryogenic temperatures is needed to adequately scale the varistor at different operating temperatures. It is assumed that no significant losses are incurred by the varistor during normal operation.

The current interruption time is estimated from the IGBT scaling for the specified voltage and current ratings as described by Section 5.2.2.2.2 and Figure 42.

5.5.2 Mass and Efficiency Trends

5.5.2.1 High Power SSCB Trends

The high power DC SSCBs are rated at 12.5 MW which is 50 percent of the minimum takeoff power 25 MW. The following trends in Figure 108, Figure 109, and Figure 110 were developed from the equations and assumptions discussed in Section 5.5.1.2 and tabulated in Table 25.

TABLE 25.—ASSUMED PARAMETERS FOR SSCB MODEL TRENDS

Parameter	Value
Converter Sizing	Operating Temperature..... 100 K
Conduction Diode	Mass Scaling Ratio Diode/IGBT..... 0.9
Varistor	Mass Scaling Ratio MOV/IGBT, ≤ 2 kV ..... 0.76923 Mass Scaling Ratio MOV/IGBT, >2 kV 0.65011

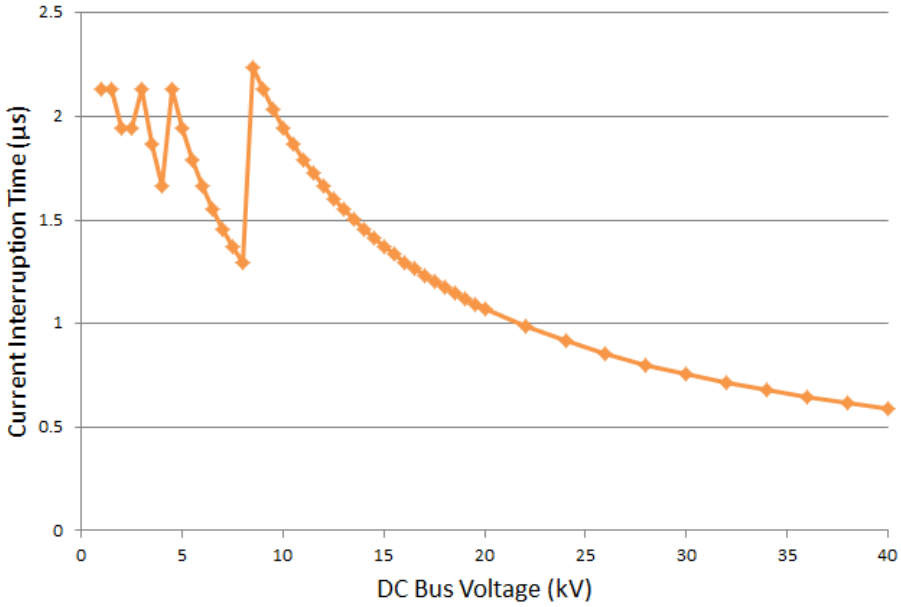


Figure 108.—High Power SSCB Current Interruption Time versus DC Bus Voltage.

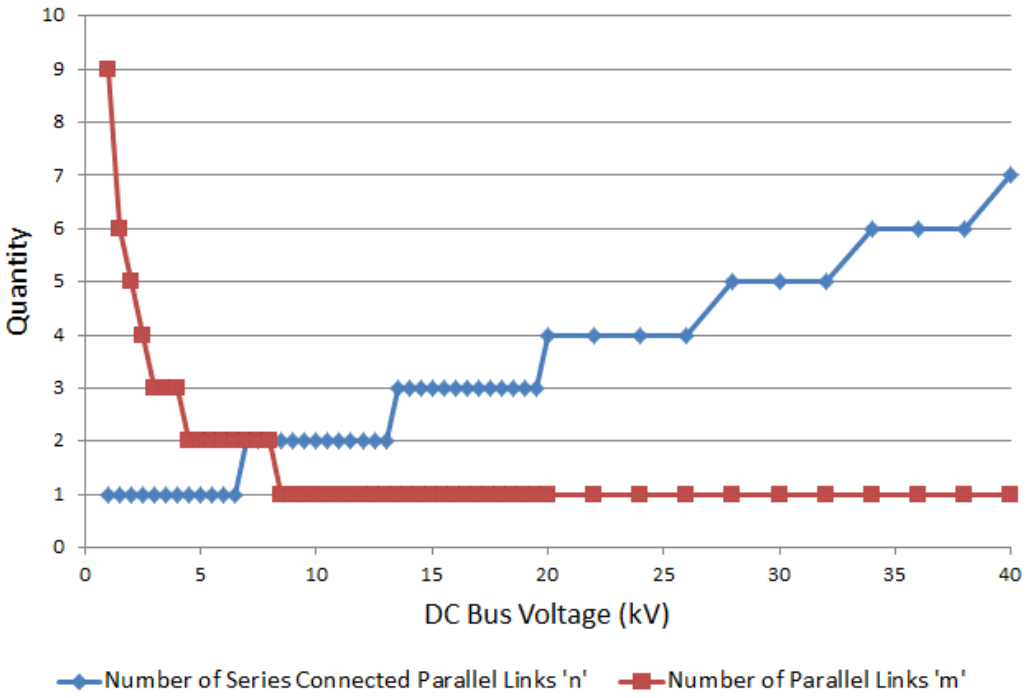


Figure 109.—High Power SSCB Quantity of Series and Parallel Switches versus DC Bus Voltage.

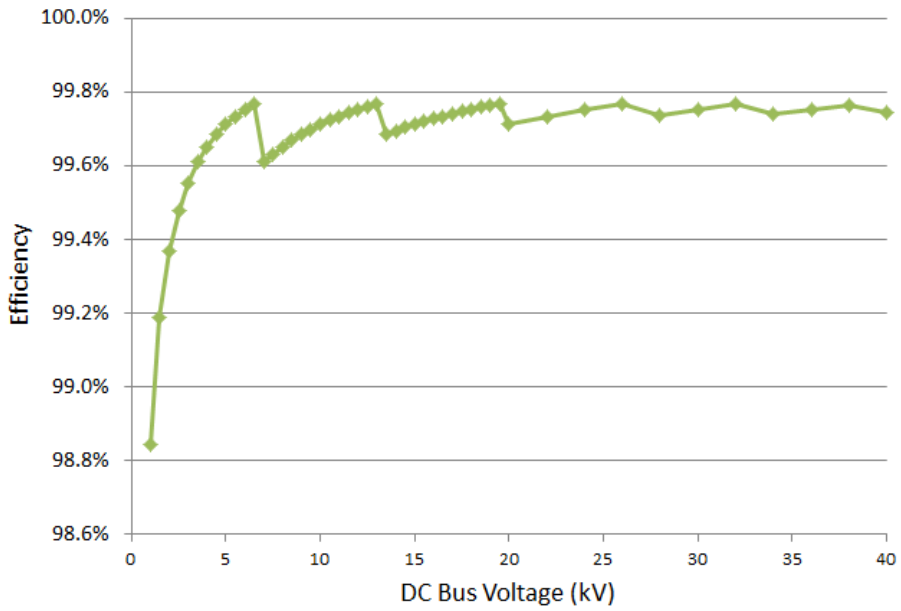


Figure 110.—High Power SSCB Efficiency versus DC Bus Voltage.

Figure 111, Figure 112, and Figure 113 show the high power SSCB mass trends as a function of DC bus voltage. The minimum mass of 33.9 kg (maximum specific power of 329 kW/kg) for this high power SSCB is found at a DC bus voltage of 6.5 kV. Note that the discontinuities in these trends are due to the IGBT configuration in parallel and in series in order to interpolate the IGBT data for scaling. Figure 109

shows the number of IGBTs in parallel and series used to form each solid-state switch for each DC bus voltage.

The trends in mass versus DC bus voltage can be further interpreted by analyzing the mass breakdown versus DC bus voltage as shown in Figure 114. The diode mass contributes to a slightly larger percentage of the total SSCB mass for lower voltages, while the varistor mass contributes a higher percentage of the total mass for higher voltages. However, the mass trends are dominated by the IGBT mass sizing.

Figure 113 and Figure 114 show the high power SSCB efficiency and conduction losses. These trends show an improvement in efficiency for high DC bus voltages. The losses continue to decrease for increasing voltages up to 6.5 kV to achieve an efficiency of 99.77 percent at 6.5 kV. For voltages greater than 6.5 kV, the efficiency and losses remain approximately the same. The conduction losses are determined in part by the IGBT conduction voltage drop scaling as a function of the rated IGBT voltage.

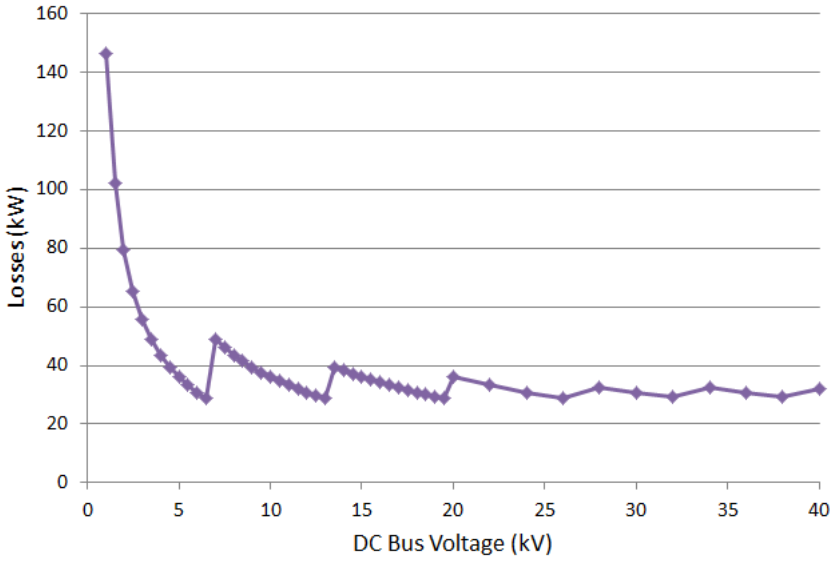


Figure 111.—High Power SSCB Conduction Losses versus DC Bus Voltage.

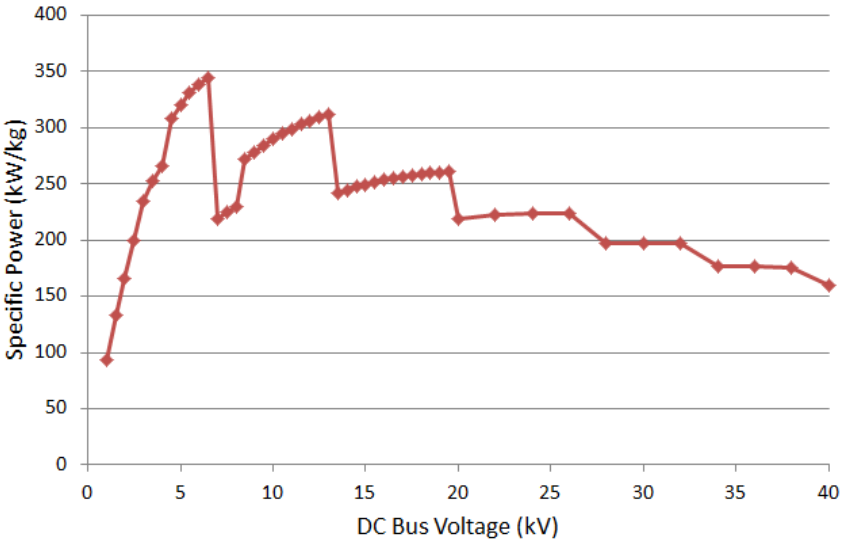


Figure 112.—High Power SSCB Specific Power versus DC Bus Voltage.

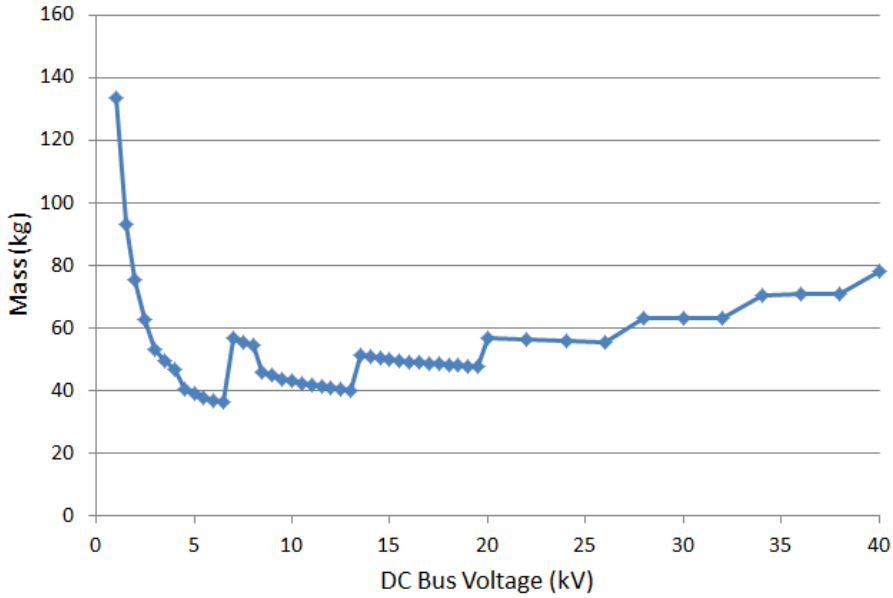


Figure 113.—High Power SSCB Mass versus DC Bus Voltage.

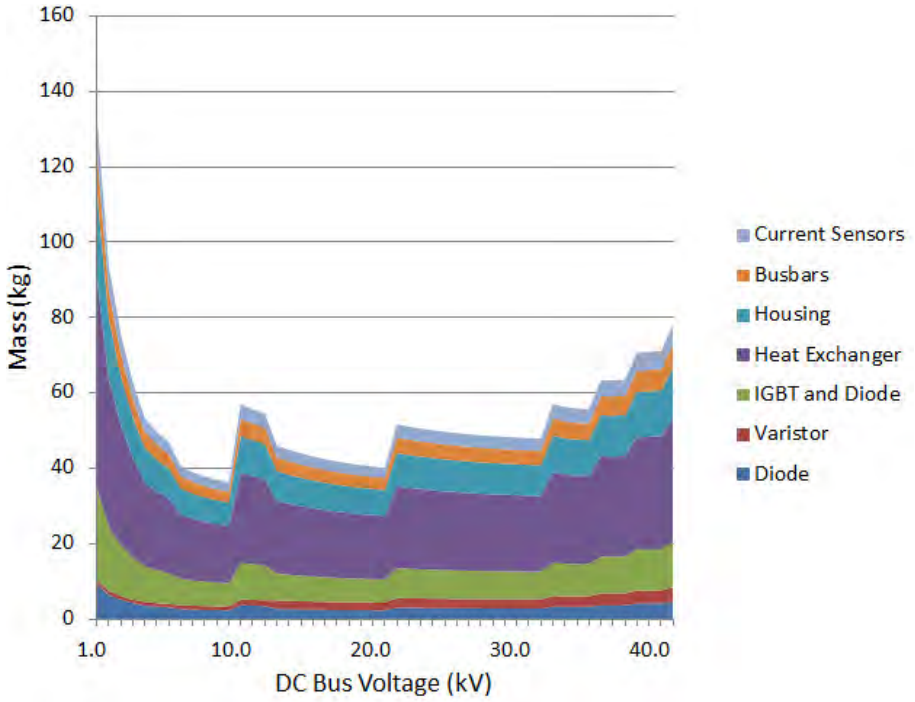


Figure 114.—High Power SSCB Mass Breakdown by Component versus DC Bus Voltage.

Figure 114 shows the high power SSCB current interruption time trends versus DC bus voltage. This trend is similar to the power converter interruption time trends due to similar scaling of IGBT turn-off times. The discontinuities for lower voltages are due to the parallel switch configurations. Generally for higher voltages, the interruption time decreases.

5.5.2.2 Low Power SSCB Trends

The low power SSCB trends that follow in Figure 115 to Figure 121 were developed from the SSCB at a rated power of 2.5 MW which is 7.14 percent of the minimum take-off power. These trends are developed with the same assumptions as listed in Table 25. Note that according to the selected architecture, the low power SSCBs are rated at either 5.36 percent (1.88 MW) or 7.14 percent of the minimum takeoff power. The trends for the 1.88 MW SSCBs are not included in this report but are similar to the 2.5 MW SSCB trends.

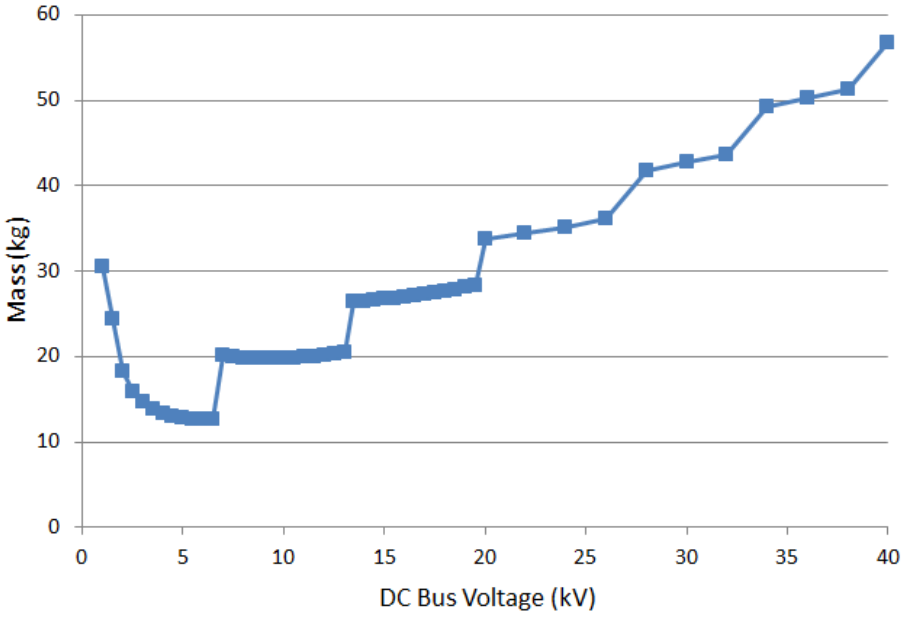


Figure 115.—Low Power SSCB Mass versus DC Bus Voltage.

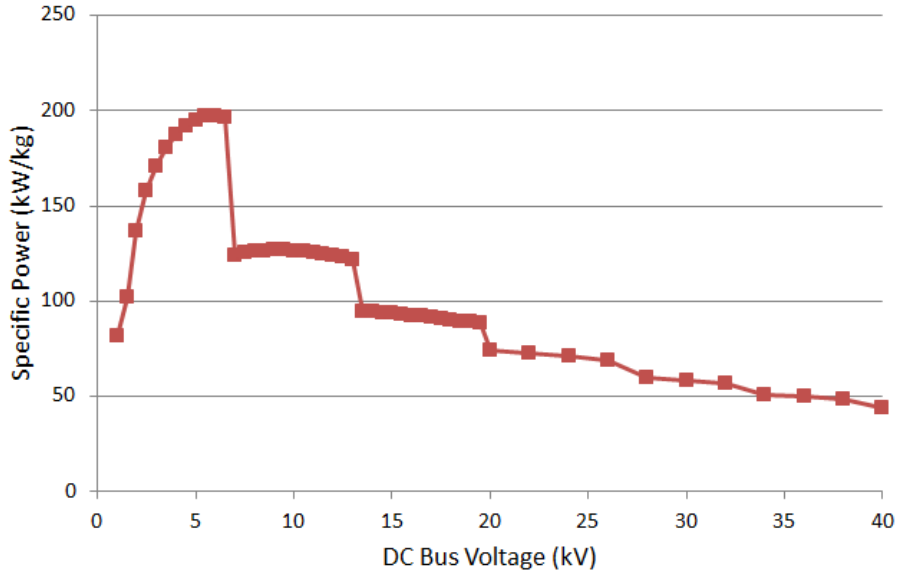


Figure 116.—Low Power SSCB Mass versus DC Bus Voltage.

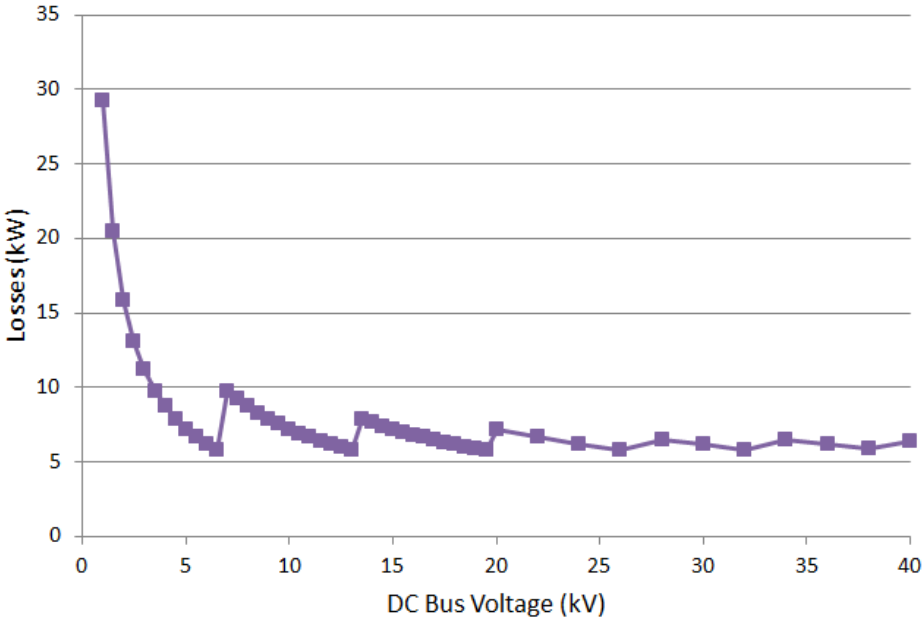


Figure 117.—Low Power SSCB Conduction Losses versus DC Bus Voltage.

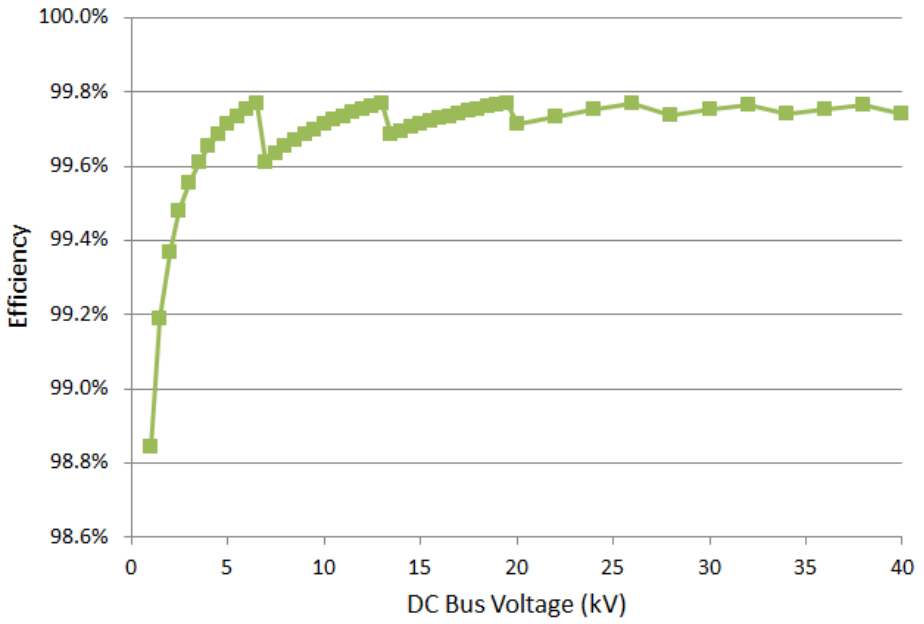


Figure 118.—Low Power SSCB Efficiency versus DC Bus Voltage.

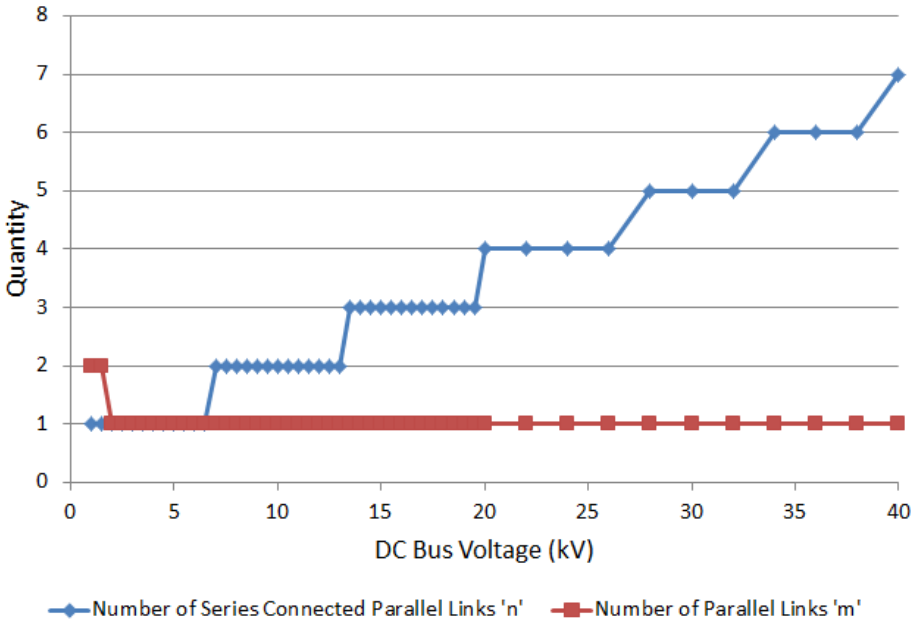


Figure 119.—Low Power SSCB Series and Parallel Configuration versus DC Bus Voltage.

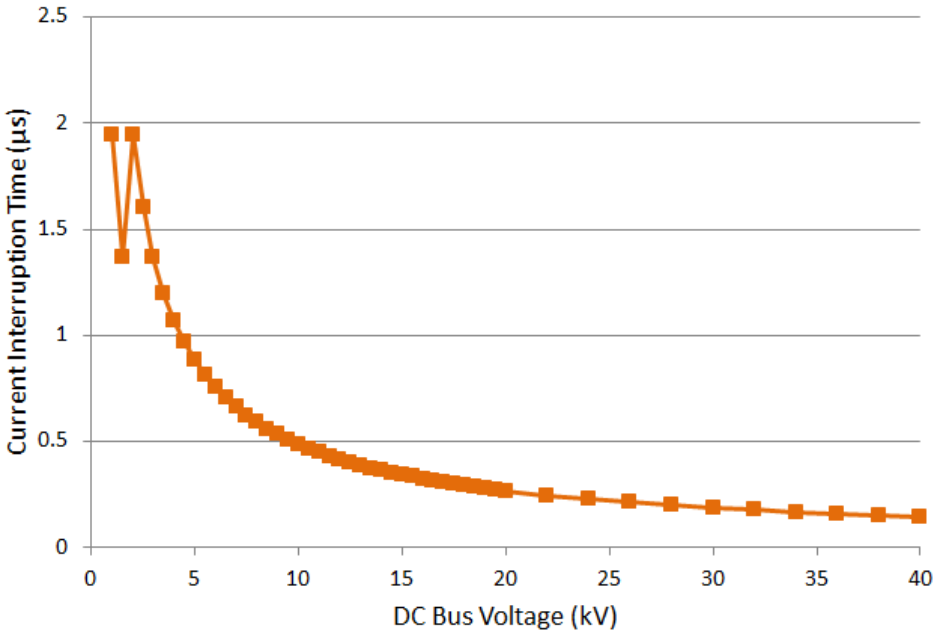


Figure 120.—Low Power SSCB Current Interruption Time versus DC Bus Voltage.

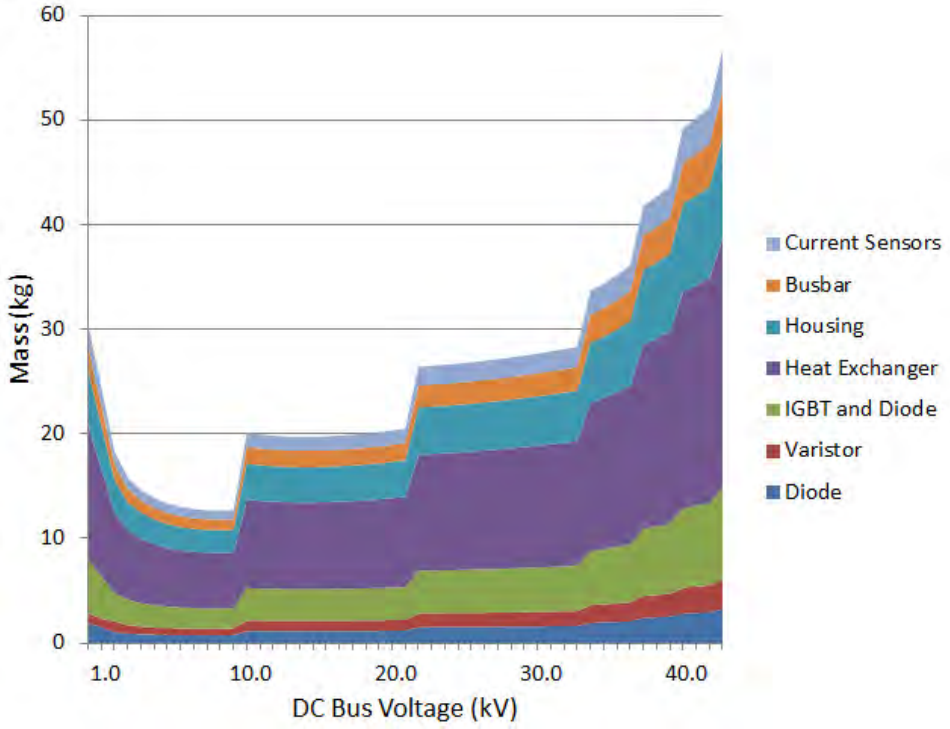


Figure 121.—Low power SSCB Mass Breakdown by Component versus DC Bus Voltage.

Figure 115 and Figure 116 show the low power SSCB mass trends versus DC bus voltage. The minimum mass for this trend is 10.70 kg at 5 kV, yielding a maximum specific power of 149.4 kW/kg. Note that the discontinuities follow the series and parallel configuration of the IGBTs as shown in Figure 119. Also, the data developed for these trends beyond 7.5 kV required extrapolation of the IGBT scaling data. Because the power rating is lower, the minimum mass for the 2.5 MW SSCB is lower than for the 12.5 MW SSCB, but the specific power of the lower power SSCB is about half that of the higher power SSCB. Looking at the SSCB component mass breakdown in Figure 121, the mass of each component for the lower power SSCB has a similar percentage of the total SSCB mass as for the higher power SSCB. So, the specific power difference is not attributed to the component scaling. The low power SSCB specific power difference is attributed to the IGBT mass scaling for voltage and current. For similar voltages but much lower currents, the IGBTs cannot process as much power per kg as IGBTs rated for higher currents. This increases the high power SSCB specific power.

Figure 117 and Figure 118 show the conduction loss and efficiency trends for the low power SSCB. The efficiency increases to 99.75 percent for increasing voltage up to 6 kV and then maintains a relatively constant efficiency. This efficiency is similar to the high power SSCB.

Figure 120 shows the low power SSCB current interruption time as a function of bus voltage. The current interruption time generally decreases for higher voltage. The rate of range of the decrease in interruption time is greater from 1 to 15 kV than for voltages greater than 15 kV. Note that the interruption times greater than 7.5 kV are the result of IGBT scaling data extrapolation.

The trend profiles for both the high and low power SSCBS are similar. A notable difference is that the specific power of the low power SSCB is approximately half that of the high power SSCB. The high power SSCB power rating is 7 times higher than the low power SSCB. The efficiency of the high and low power SSCBs are similar. The DC bus voltages for the high and low power SSCB minimum weight and maximum efficiency are similar.

5.6 Superconducting Fault Current Limiters

The role of superconducting fault current limiters (SFCL) in this TeDP system is, first, to provide quench protection for the overall system, and secondly to reduce the current requirements for interruption equipment.

With regard the first protection role; the fault current limiter is designed to be the first and only piece of the system to respond to an overcurrent via quench. Other equipment will be exposed to an elevated during the faulted conditions. However, they will not be required to manage internal quenches.

The second protection role of the fault current limiter is to reduce the magnitude and duration of the overcurrent experienced by the remaining equipment. This leads to a reduction in equipment weight.

5.6.1 Modeling Approach

There are many different types of superconducting fault current limiters. For the purposes of this study the resistive type SFCL was selected.

The resistive type fault current limiter has some distinct advantages. Chiefly, by relying on the natural resistivity transition properties of superconductors, it has the simplest design and construction. Additionally, the resistive SFCL tends to be the lightest solution. For these reason this option is the most widely implemented method for conventional terrestrial systems.

This transition between superconducting and non-superconducting states is illustrated in Figure 122. This figure shows a generic log-log relationship between the electric field generated by a superconductor and current density. Three states are indicated: flux-creep state, flux-flow, and resistive. As the current increases in a superconductor the losses increase. Once the transition to flux-flow occurs, thermal effects in the superconducting material further increase the generated electric field losses.

The key to resistive SFCL protection design is balancing the current capability of all system components with the quench current (Figure 123). Using linear approximations between temperature and resistivity during superconducting transition, Blair et al. analytically solve for quench transition time for BSCCO round wire in a DC system (Ref. 164). His results are illustrated in Figure 123.

A similar relationship between fault current and quench time can be envisioned for each super-conducting component within the system. Proper protection is provided by ensuring the quench time/fault current curves for all equipment sit substantially to the right of the curve to the SFCL.

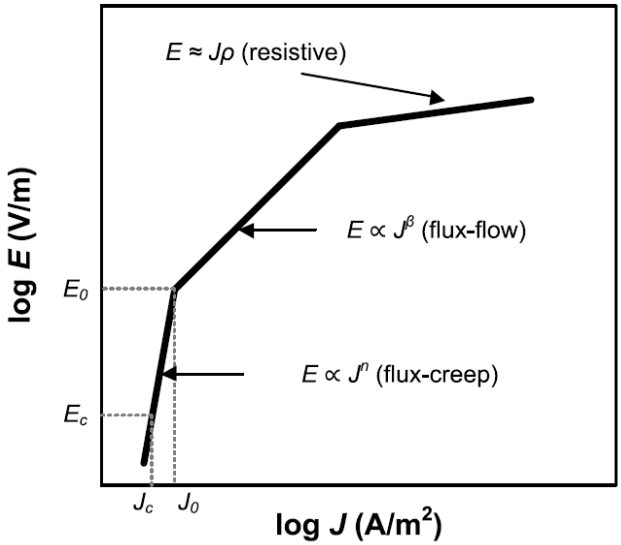


Figure 122.—Generic E-J Characteristic Superconductor (Ref. 165).

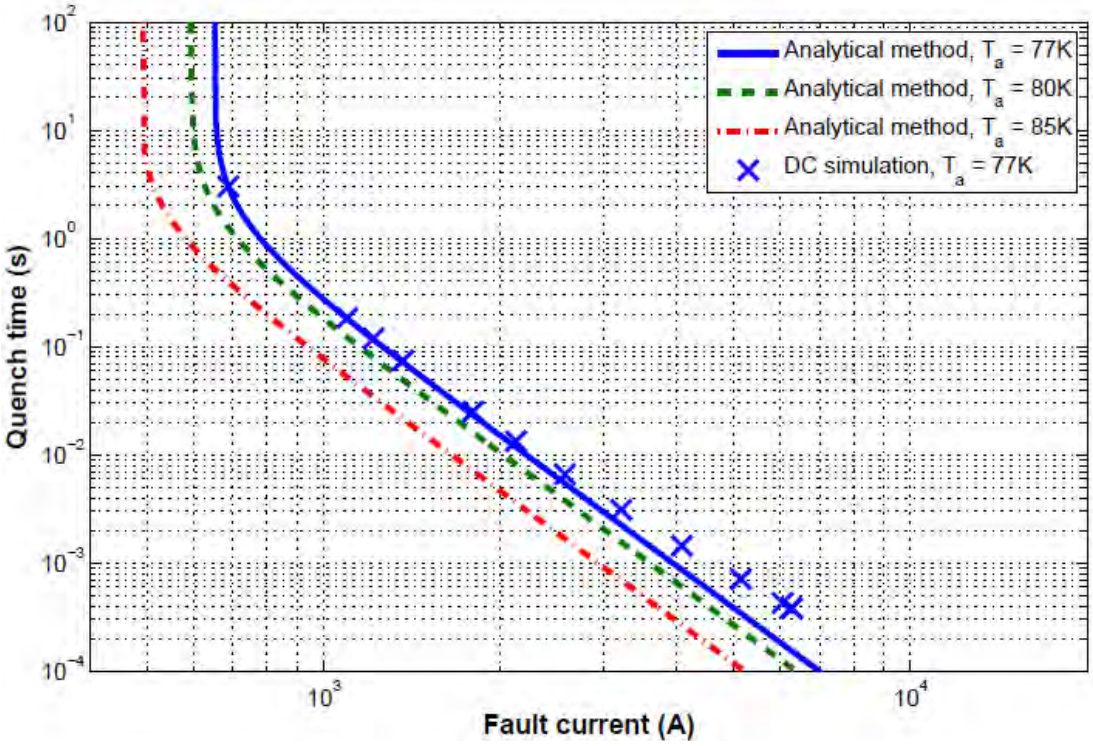


Figure 123.—SFCL DC Quench Time Analytical Solution from Reference 164.

5.6.2 Geometry and Winding

The reference configuration for this fault current limiter voltage sensitivity study is a prototype unit developed in Manchester University (Refs. 166, 167, and 168). This SFCL unit consists of helical wound MgB_2 wire around a slotted alumina former. This unit is shown in Figure 124 and Figure 125.

The Manchester unit applied two interleaved solenoid coils which were wound with opposing currents to cancel out solenoid inductive fields. Additionally, as seen in the two figures, copper braid was also situated on the former to allow for transitioning between superconducting and normally conducting wires. This entire former, winding assembly is placed in a cryostat bath.

For the purposes of this component sensitivity exercise, Manchester's general solenoidal construction method is applied. However, the Manchester University resistive type SFCL coil was wound and operated in a manner which reduced inductance generated by the superconducting coil. In contrast, for this DC microgrid, operating the fault current limiter as an inductor is beneficial to the protection system performance. Therefore, the desired inductance provided by the SFCL coil determines impacts geometry of the solenoidal coil.

The spacing between each winding is determined to achieve the desired inductance, and minimize weight, while ensure adequate dielectric protection and limit the magnetic field in the core. Additionally, alumina is replaced with a glass reinforced plastic (GRP) composite to further minimize the former weight.

The general arrangement for the notional SFCL developed for these sensitivity models is illustrated in Figure 126.

Figure 124.—University of Manchester SFCL Windings on Slotted Former (Ref. 168).

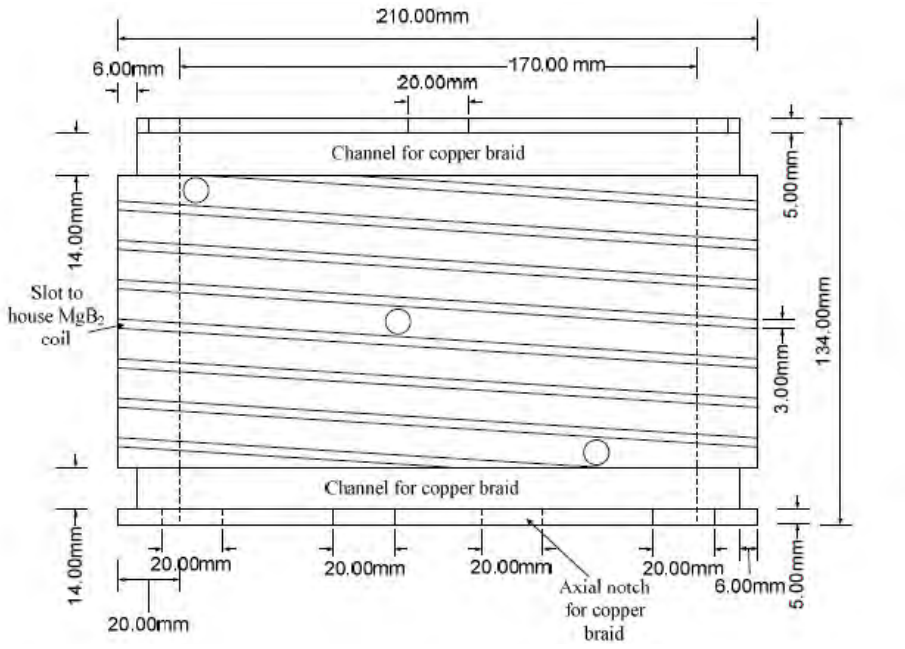


Figure 125.—University of Manchester SRCL Former Drawing (Ref. 168).

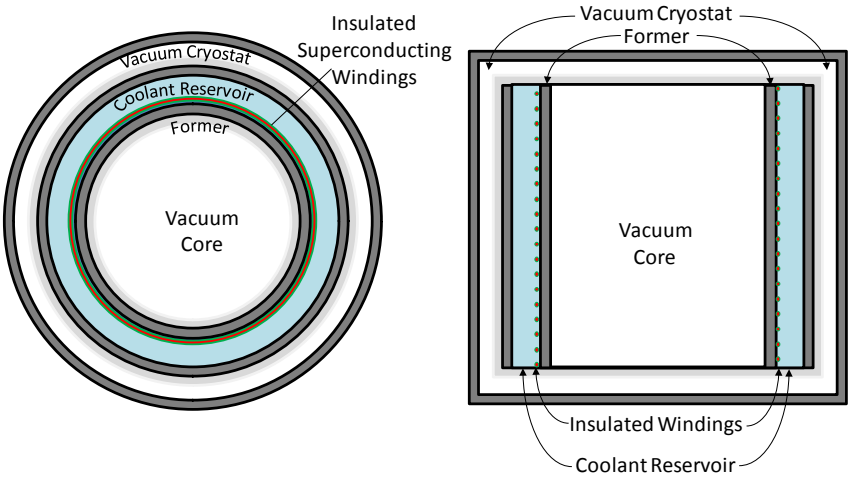


Figure 126.—General Arrangement of a Notional Vacuum Cored Solenoidal SFCL used for First Principles Based Mass and Efficiency Sensitivity Modeling.

5.6.3 Parameter Diagram

The SFCL model inputs and outputs follow the structure illustrated in Figure 127. The primary attributes of interest are the weight and efficiency of the fault current limiter. Additional outputs provide information to determine protection system effectiveness. SFCL superconducting, and quench state resistance, as well as the quench transition time are reported out to determine the expected overcurrent for the system.

To size the SFCL, information about the nominal operating current and the quench to nominal current ratio are required. Additionally, the protection system must specify the inductance desired from this solenoidal coil and the time expected between fault occurrence and fault interruption. Finally, the operating voltage is specified to size the required dielectric insulation.

There are many internal variables that affect the sizing trends for this device. This includes the coolant temperatures for nominal operation, resistance transitions parameters required from Blair's quench time models, material assumptions for former and dielectric, and the geometry and flux density limits for the solenoidal sizing.

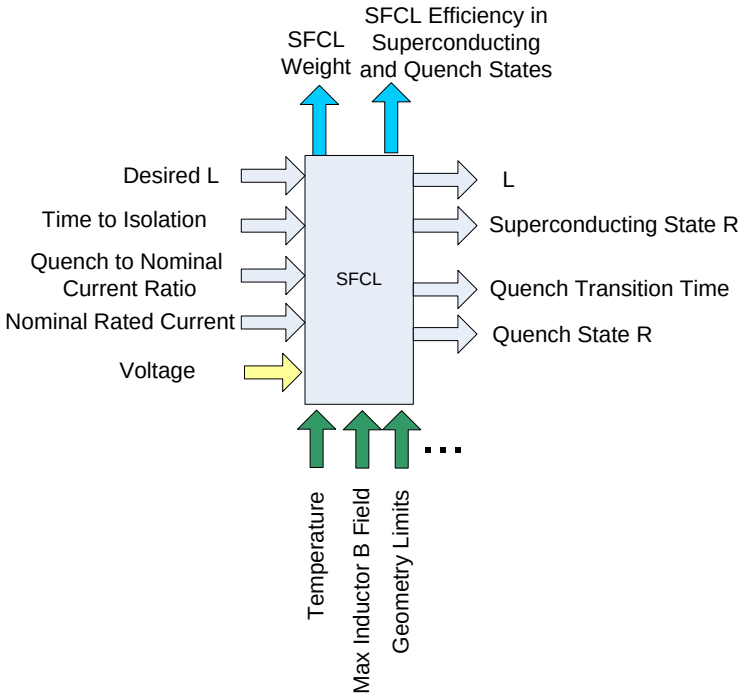


Figure 127.—Parameter Diagram for Superconducting Fault Current Limiter.

5.6.4 Governing Equations

The governing equations for the fault current limiter model are presented in four sections: quench transition modeling, inductor modeling, mass modeling, and solver overview.

1. The quench transition modeling equations determine the time to quench for the SFCL device as well as the heat that is dissipated to the cryocoolant.
2. The induction equations capture the relationships between the physical geometry of the cable coil and which determines the impedance properties of the SFCL.
3. The mass equations take the geometry properties and the dissipated heat information to determine the overall mass of the inductive coil and the coolant.
4. The solver routine determines the geometry parameters of the SFCL required to minimize the mass of the device.

5.6.5 Quench Modeling

The SFCL sensitivity model applied the processes developed by Blair et al. to determine the time to quench (Ref. 169). This process makes a fundamental assumption that the resistivity of the superconductor varies linear with temperature during a quench event when the temperature is greater than over the critical temperature.

This assumption is reflected in the induced field and critical current density equations. Blair presents these equations thusly:

$$E(t,T) \approx \rho\left(\frac{T}{T_C}\right)J(t)$$

$$J_C(T) \approx J_{c0}\left(\frac{T_C - T(t)}{T_C - T_0}\right)$$

where

E	electric field
ρ	normally conducting resistivity
T	superconductor temperature
J	current density
J_C	critical current density
T_C	critical temperature
T_0	reference temperature
J_{c0}	J_C at reference temperature
t	time

The next equation used to determine quench time is an expression for electric field sensitivity to temperature developed by Paul et al. (Ref. 170):

$$E(T) = E_0\left(\frac{E_c}{E_0}\right)^{\frac{\beta}{n_{77k}}}\left(\frac{J_{c0}}{J_C(T)}\right)\left(\frac{J(t)}{J_{c0}}\right)^{\beta}$$

where

E_0 field at flux flow to flux creep transition
E_c E at critical current density
T temperature
β flux flow region exponent
n_{77K} flux creep region exponent at 77 K reference temperature

The final expression needed to solve for quench time is the superconductor material temperature:

$$T(t) = T_a + \frac{1}{c_{cs}} \int [Q_{sc}(t) - Q_{\text{coolant}}(t)] dt$$

where

T_a coolant reservoir initial ambient temperature
c_{sc} superconductor heat capacity
Q_{sc} heat dissipated in the superconductor
Q_{coolant} heat removed by coolant reservoir

Combining the linear assumptions and the field transition expressions, and substituting into the thermal equation, the time to quench can be solved by the following equation:

$$t = c_{sc} \int \frac{dT}{\left[k \frac{T_c - T_{init}}{T_c - T} - \frac{T - T_{amb}}{\theta_{sc}} \right]}$$

where k is defined by

$$k = E_0 \left(\frac{E_c}{E_0} \right)^{\frac{\beta}{n_0}} \left(\frac{I^{\beta+1}}{J_{C0} a_{sc}} \right) l_{sc}$$

and where

l_{sc} length of the superconducting wire
a_{sc} cross-sectional area of superconducting wire
θ_{sc} thermal resistance from superconductor to reservoir

Blair et al. provides an analytical solution the integral expression for quench time.

5.6.6 Quench Cooling

The quench transition time equations assume that the overall quench energy is only partially dissipated to the coolant reservoir, while the remainder acts to heat the superconducting material. For this estimate, the heat transfer coefficient between the cable and the reservoir to determine the thermal energy dissipated to the coolant during the quench event.

However, a conservative estimate for coolant reservoir sizing assumed that the entire quench energy is dissipated to a fixed volume of coolant. Under this assumption the total amount of heat assumed the following expression:

$$Q_{\text{coolant}} = \int_{t_{\text{fault}}}^{t_{\text{isolate}}} i_q(t)^2 R(t) dt$$

where

Q_{coolant} Heat removed by coolant reservoir
i_q Quench current
R Resistance in superconducting wire

Applying linear superconducting to conduction resistivity transition assumption, the overall heat which must be dissipated is a function of the time to quench and the time it takes to interrupt the current. Therefore the overall heat dissipated in the cooling plenum is given by:

$$Q_{\text{coolant}} = {i_q}^2 \left[\frac{R_{sc}}{2} + \frac{R_{sc} + R_q}{2t_q} t_{\text{isolate}} + R_p \max\left(0, t_{\text{isolate}} - t_q\right) \right]$$

where

R_{sc} superconducting state resistance
R_q quench state resistance
R resistance in superconducting wire
t_q time to quench
t_{isolate} time to isolation

This heat value is used to determine the mass and volume of the coolant reservoir.

5.6.7 Induction Equations

Solenoid inductance equations were used to size the SFCL coil geometry. It should be noted that this set of equations is only valid for coils where the diameter is much smaller than the length. Additionally, air core assumptions were applied for the field and inductance equations for these SFCL sensitivity models. Therefore the relative permeability was assumed to be roughly unity.

Determining the performance for the optimal SFCL inductor design required that the mass be minimized in terms of inductor geometry which still providing the requirement functionality and concept feasibility. The optimization followed the formulation below:

$$\begin{aligned} \min_{(d_F, N)} \quad & m_{\text{total}} \\ & s.t. \\ & B \le B_{\max} \\ & a \le \frac{l_F}{d_F} \\ & b \le d_F \\ & L_{\min} \le L \le L_{\max} \end{aligned}$$

where

d_F solenoid diameter
N number of solenoid windings
B,$B_{\max}$ magnetic flux density and limit
l_F solenoid length
a,b solenoid geometry limits
L,$L_{\min}$,$L_{\max}$ solenoid inductance and limits

Several limits were applied to in this solenoid inductance model. Firstly, the spacing between inductor windings was limited to ensure that the induced magnetic field was limited to a desired value. Variation of SFCL performance with respect to the limiting *B* field is captured in the component sensitivity portion of this section. Magnetic flux density for an air core solenoid inductor is given by:

$$B_{\max} \geq \mu \frac{N i_q}{l_F}$$

where

$B_{\max}$ maximum allowable magnetic flux density
μ magnetic constant
N number of solenoid windings
i_q quench current
l_F length of solenoid

The length of the solenoid is directly proportional to the product of the number of windings and the winding spacing:

$$l_F = Nh$$

where

h solenoid winding spacing

Substituting this relationship into the magnetic flux density relationship provides a constrained relationship between winding spacing and magnetic field.

The next set of limits applies to the geometry of the solenoid former. Minimum geometric limits on solenoid diameter (d_F) and length (l_F/d_F) are applied in this voltage sensitivity model which can be manipulated to ensure validity of the solenoid inductance equations. For more accurate estimation and sizing, a series of inductance equations could be implemented in future model iterations which are applicable to various inductor geometries (solenoid, pancake, toroidal, etc.)

The final constraint on the SFCL geometry comes from the protection system requirements. With limits on the maximum allowable flux density and limits on the solenoid diameter and length, the inductance value can be overconstrained if the solenoid winding spacing is fixed. Therefore, the inductance value was allowed to float so long as it meets a set of minimum requirements and does not affect system performance by being too large.

$$L_{\min} \leq \mu \frac{N^2 \pi {d_F}^2}{4 l_F} \leq L_{\max}$$

where

$L_{\min}$ minimum required inductance
$L_{\max}$ maximum required inductance
d_F solenoid diameter

If the inductance value is not allowed to float above the minimum value, than the solenoid winding spacing value varies depending on the specified inductance.

Winding spacing is therefore subject to three limits: cable geometry, magnetic field, and inductance. The winding spacing must be larger than the insulated cable diameter. It must also be large enough to ensure that the magnetic field does not exceed the requirement. Finally, it must be large enough to ensure that the desired inductance is equal to the value specified.

$$h = \max\left(2\frac{V}{\kappa_{ins}} + d_{sc}, \mu\frac{i_q}{B_{\max}}, \frac{N\pi {d_F}^2}{4L} \right)$$

where

κ_{ins} dielectric strength of the insulation
V cable voltage
d_{sc} diameter of the BSCCO round wire

The cable diameter in this equation assumes that the insulation is wound around the BSCCO round wire.

The efficiency of the SFCL is a simple function of the length of the superconductor cable (l_{sc}). This length is calculated in terms of the inductor geometry as a helical coil:

$$l_{sc} = N\sqrt{\pi^2 {d_F}^2 + h^2}$$

5.6.8 Mass Equations

The overall system mass is a combination of the masses of the superconducting wire (m_{sc}), the solenoid former (m_F), the dielectric insulation (m_{ins}), and the coolant (m_{coolant}). While the cryostat contributes greatly to the mass of the SFCL devices, this mass estimate is not currently included in these sensitivity models.

The contributing mass equations are given here:

$$m_{sc} = \rho_{sc} l_{sc} a_{sc}$$

$$m_F = \rho_{GRC} l_F 2\pi\left(\frac{d_F}{2} - \frac{\tau_F}{2} \right)\tau_F$$

$$m_{ins} = \rho_{ins} l_{sc} 2\pi\left(\frac{d_{sc}}{2} + \frac{\tau_{ins}}{2} \right)\tau_{ins}$$

$$m_{coolant} = \frac{cp_{coolant}}{Q\left(T_{\max} - T_{init}\right)}$$

where

ρ_{sc} density of the superconducting wire (BSCCO)
ρ_{GRC} density of the solenoid former (GRC)
ρ_{ins} density of the dielectric insulation (LPP)
τ_F solenoid former thickness
τ_{ins} insulation thickness

5.6.9 Assumptions Overview

The SFCL voltage sensitivity study assumptions are provided in Table 26. SFCL sensitivity study variable ranges are shown in Table 27, and SFCL sensitivity study optimization variables are shown in Table 28.

TABLE 26.—SFCL VOLTAGE SENSITIVITY STUDY ASSUMPTIONS

Variable	Value
Insulator dielectric strength (LPP), κ_{ins}	50 kV/mm
Final superconductor temperature, T	92 K
Coolant (starting) temperature, T_{a0}	70 K
Superconductor critical temperature, T_c	92 K
Ambient final temperature after quench, T_{af}	77 K
Flux-creep region exponent (at 77K), n_{77K}	6
Flux-flow region exponent, β	3
Initial critical current density, J_{c0}	1.5×10^8 A/m^2
Initial electric field, E_c	0.0001 V/m
Electric field at transition from flux-creep state to flux-flow state, E_0	0.1 V/m
Normal conducting state resistivity (at Tc), ρ	0.000001 Ωm
Coefficient for heat transfer to cooling reservoir, κ	1500 W/K m^2
Superconductor volumetric specific heat, c_v	1000000 J/K m^3
Superconductor density, ρ_{sc}	6500 kg/m^3
Max magnetic flux density, B	0.5 T
Dielectric Insulation density, $\rho_{insulation}$	900 kg/m^3
Former density, ρ_{former}	1800 kg/m^3
Coolant medium	N_2
Former thickness, τ_F	6 mm
Coolant (LN_2), cp,	2.05 at 77 K kJ/kg*K
Coolant density (LN_2), P_{LN2}	810 kg/m^3

TABLE 27.—SFCL SENSITIVITY STUDY VARIABLE RANGES

Variable	Values
Power (MW)	11.2
Voltage (kV) (RMS if AC, ±X if DC)	2, 4, 6, 8, 10, 12.5, 15, 17.5, 20
Fault current ratio	2, 4, 6
Time to isolation (μs)	100, 5000, 100000
Min desired inductance (μH)	10, 1000, 100000
Max allowable inductance (μH)	Not specified
Min quench resistance (Ω)	0.1, 0.5, 1
Time to heat dissipation (s)	1, 10, 30

TABLE 28.—SFCL SENSITIVITY STUDY OPTIMIZATION VARIABLES

Variable	Range
Initial cryogenic temperature (K)	Depends of coolant
Number of turns	[1,∞)
Diameter of solenoid (m)	[0.01,100]
Limit	**Range**
Min quench resistance (Ω)	See variable ranges
L/d of solenoid	[0.1,100]
Inductance (μH)	See variable ranges

5.6.9.1 Mass Trends

In general, results show that increasing the operating voltage has favorable effects on the mass of the system. The magnitude of these effects depends on the protection and geometric requirements placed on the device.

The sensitivity of the SFCL mass to operating voltage and other protection parameters (overcurrent, desired inductance, and time to isolation) is shown in Figure 128, Figure 129, and Figure 130.

The ratio of fault current to nominal operating current primarily effects the SFCL mass via three physical properties: cryogenic fluid reservoir volume (variation in time to quench and energy dissipated), and solenoid winding (maximum magnetic field). As illustrated in Figure 128, increasing the fault current ratio has a proportional effect on the SFCL mass. It also has a significant impact on the degree to which voltage effects mass.

With the variable settings indicated in the figure, for a ratio of fault to nominal current ratio of 9 the mass of the SFCL varies from 16 kg at 2 kV to 2 kg at 40 kV. Whereas, for a fault current to nominal current ratio of 3, the mass varies from approximately 6 to 2 kg on the same range.

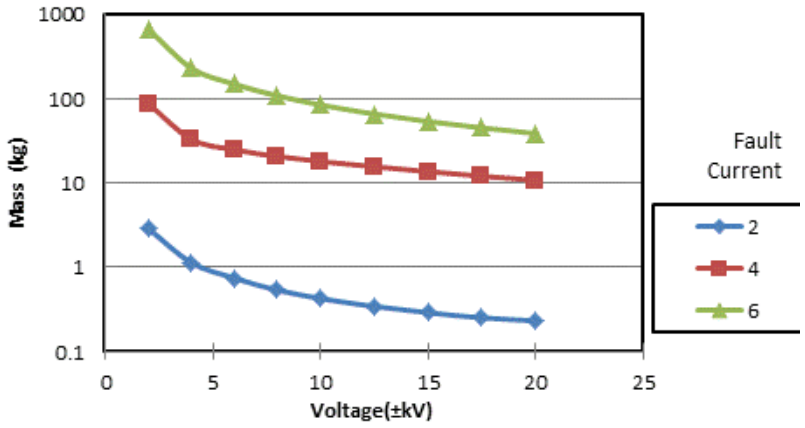


Figure 128.—SFCL Sensitivity of Mass to Voltage with Varying Fault Current Ratios.

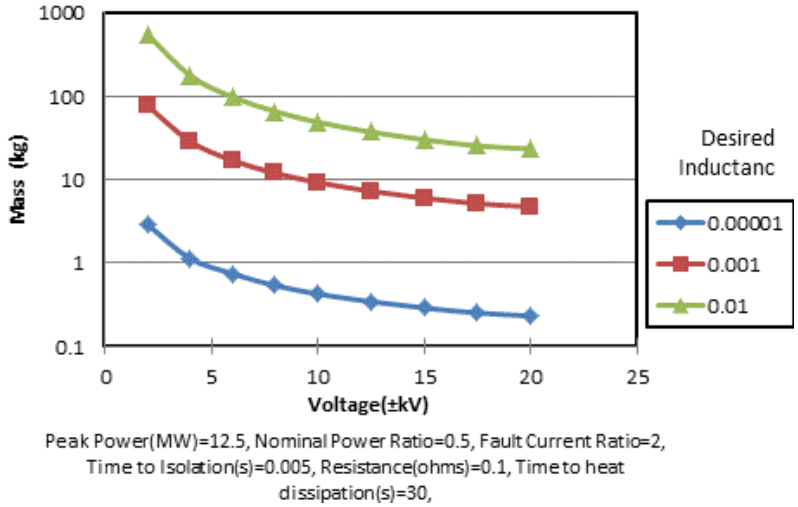


Figure 129.—SFCL Sensitivity of Mass to Voltage with Varying Inductance Requirements.

In desired inductance has a similar impact on the SRCL mass trends. As shown in Figure 129, a higher desired inductance requires a larger device and more sensitivity to voltage. The manner in which the mass inductance requirements impact the weight is not directly through the field and cryogenic system mass. The required inductance effects mass directly through impacts to the solenoid geometry (number of windings, turns, and diameter).

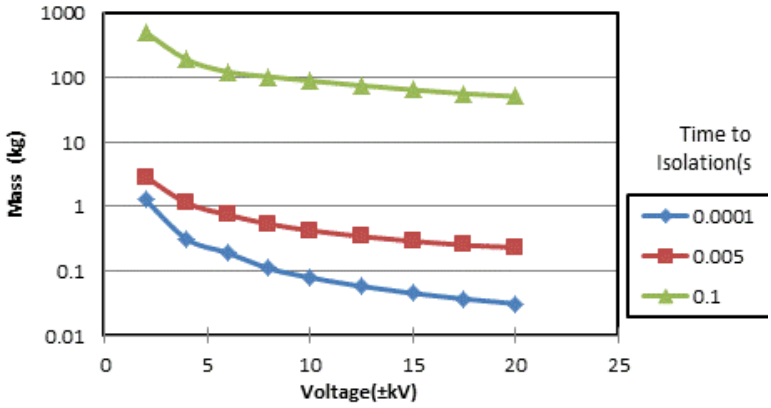
The time to isolation requirement has a singular impact on the mass of the SFCL. This value only impacts the mass and volume of the cryocooling fluid reservoir. The impact of this mass is shown in Figure 130.

The benefit of a fault current limiter is its ability to increase resistance during a fault. The level of resistance required after quenching affects the overall system mass as illustrated in Figure 131. This mass increase is due to the increased heat generated during the fault and the increased length of the superconductor.

SFCL performance also affects the cryogenic system mass. The amount of cooling power required from the cryocooler depends on the time in which the heat generated during a quench/isolation event to be dissipated. These mass trends are indicated in Figure 132.

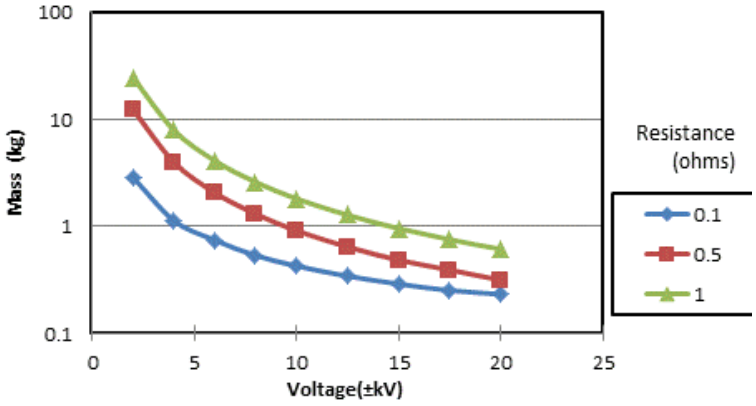
The voltage trends for all of SFCL components are shown in Figure 133 and Figure 134. The weight of all components goes down with voltage with the exception of the dielectric insulation.

Additionally, the mass of the overall SFCL assembly is sensitive to the required impedance. Increased quench resistance and inductance can dramatically increase the SFCL weight.



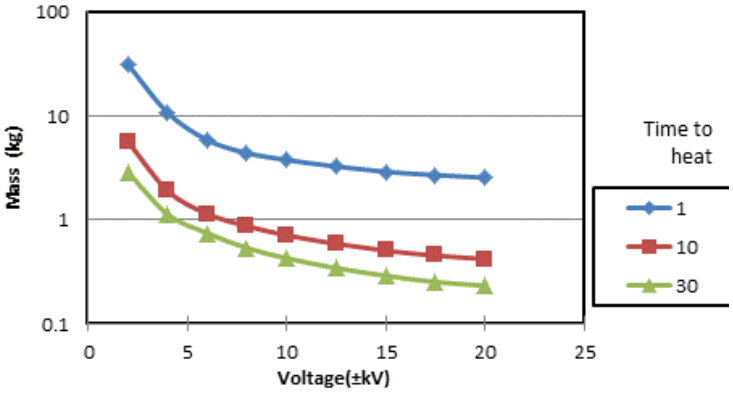
Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Fault Current Ratio=2, Desired Inductance(H)=0.00001, Resistance(ohms)=0.1, Time to heat dissipation(s)=30,

Figure 130.—SFCL Sensitivity of Mass to Voltage with Varying Breaker Response Times.



Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Fault Current Ratio=2, Time to Isolation(s)=0.005, Desired Inductance(H)=0.00001, Time to heat dissipation(s)=30,

Figure 131.—SFCL Sensitivity of Mass to Voltage with Varying Minimum Required Quench Resistance.



Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Fault Current Ratio=2,
Time to Isolation(s)=0.005, Desired Inductance(H)=0.00001,
Resistance(ohms)=0.1,

Figure 132.—SFCL Sensitivity of Mass to Voltage with Varying Time to Dissipate Quench Energy with Cryogenic Systems.

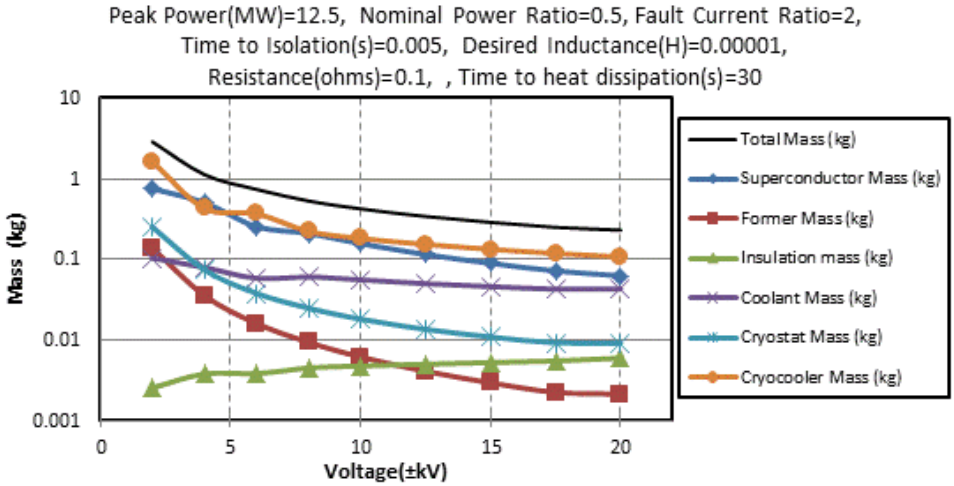


Figure 133.—Mass Contributions for Superconducting Fault Current Limiter for with Low Quench Resistance and Low Inductance Requirements.

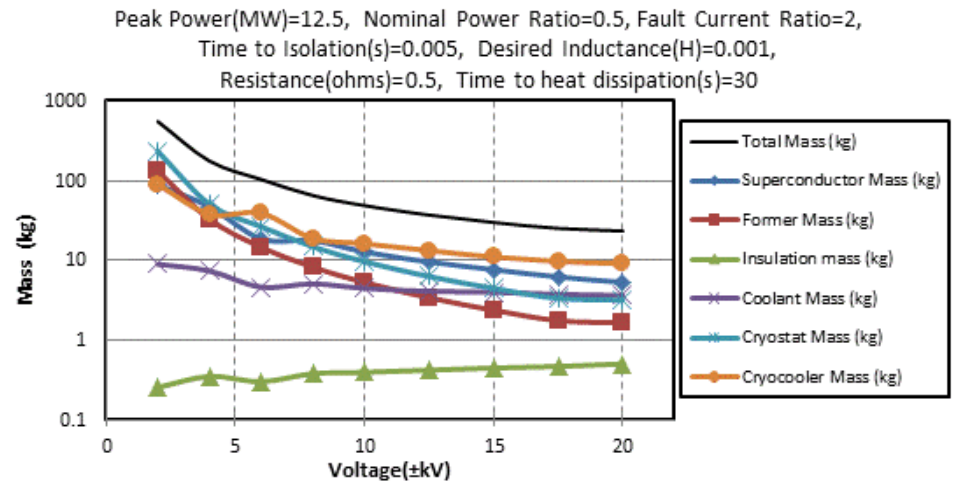


Figure 134.—Mass Contributions for Superconducting Fault Current Limiter for with Higher Quench Resistance and Higher Inductance Requirements.

5.6.10 Geometry Sensitivity

Geometry limits play a large role in limiting the benefits available. Field constraints affect the mass of the SCFL at lower voltages and geometry constraints begin to act on the mass as voltage increases. This is illustrated in Figure 135, Figure 136, and Figure 137.

In Figure 135 the magnitude of the max magnetic field density limit does not impact the SFCL mass at voltages over approximately 15 kV for the variables settings indicated on the graph. For voltages under 15 kV, increasing in the max allowable magnetic field density produces decreases in SFCL mass. Both diameter constraints and L/D constraints drive the unit mass at higher voltages; depending on the requirements. This is illustrated in Figure 136 and Figure 137.

As shown in Figure 136, for each L_f/d_f limit corresponds to a point at which increased voltage may not yield added mass improvements. For the min L_f/d_f case of 1 the voltage sensitivity curve flattens around 20 kV while for a min L_f/d_f of 10, this point of diminished returns occurs around 6 kV.

A similar point of diminishing returns occurs when imposing a minimum diameter limit on the SFCL former. An increase in min diameter has a proportional effect on the mass at higher voltage.

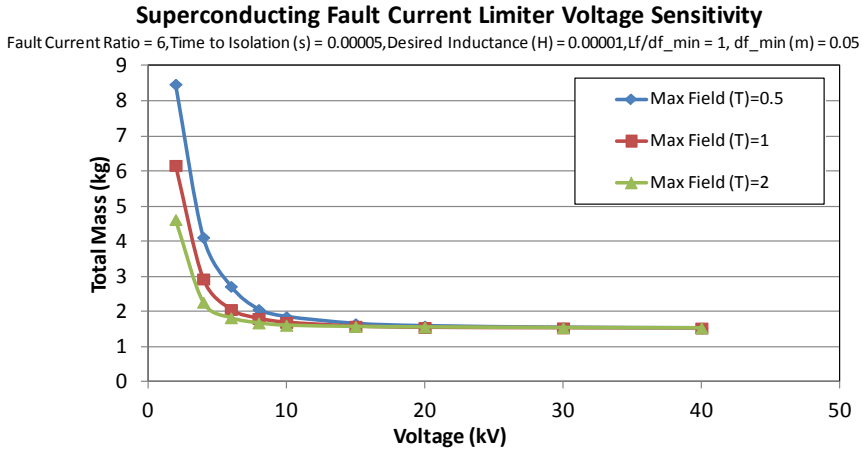


Figure 135.—SFCL Sensitivity of Mass to Voltage with Varying the Maximum Allowable Magnetic Flux Densities.

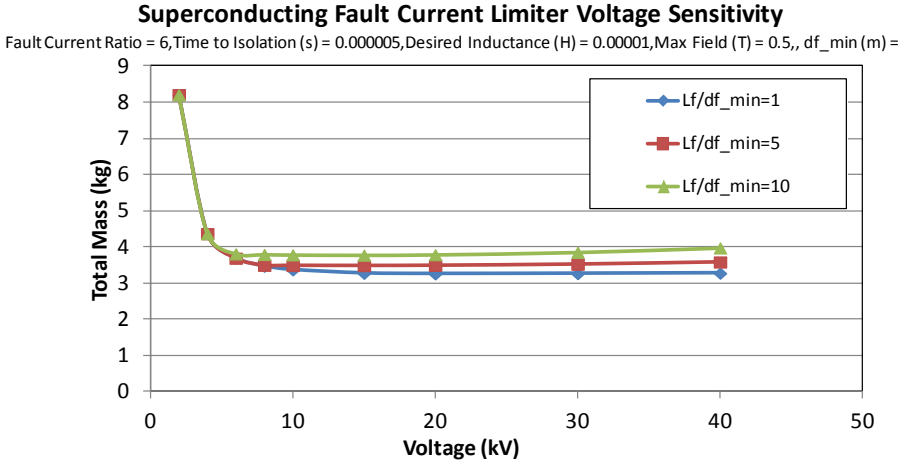


Figure 136.—SFCL Sensitivity of Mass to Voltage with Varying Minimum L/D Limits on the Solenoid Geometry.

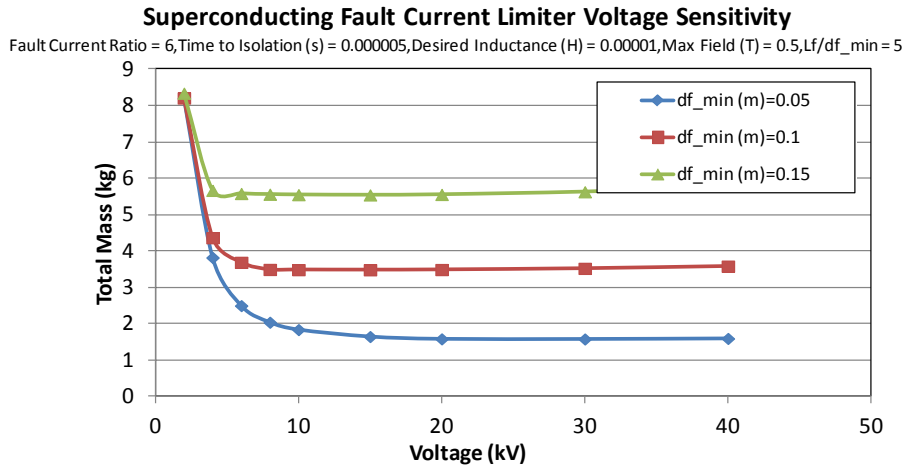


Figure 137.—SFCL Sensitivity of Mass to Voltage with Varying Minimum Diameter Limits on the Solenoid Geometry.

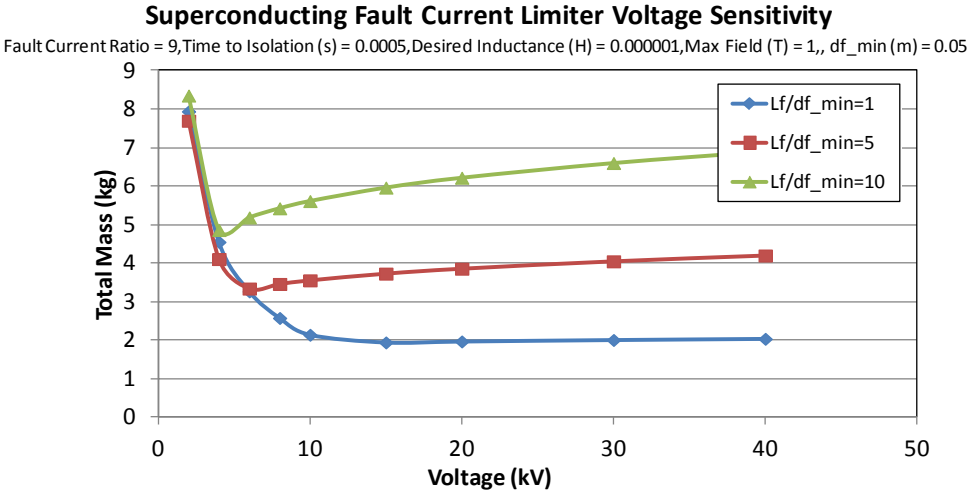


Figure 138.—Effect of Geometry Limits and Increased Inductance on SFCL Mass Sensitivity of Mass to Voltage.

In some instances, geometric constraints create a clear optimal voltage level for the SFCL. If the winding spacing is held fixed by field and wire geometry and the inductance value is allowed to float above the specified minimum inductance, geometric constraints may increase the SFCL mass as the voltage increases. In these scenarios, the decreased voltage impacts the winding spacing due to reduction in wire diameter. Therefore, this yields an increase in the number of windings available on the fixed geometry solenoid. In turn, the number of windings increases, which drives the inductance up. This is illustrated in Figure 138, Figure 139, and Figure 140.

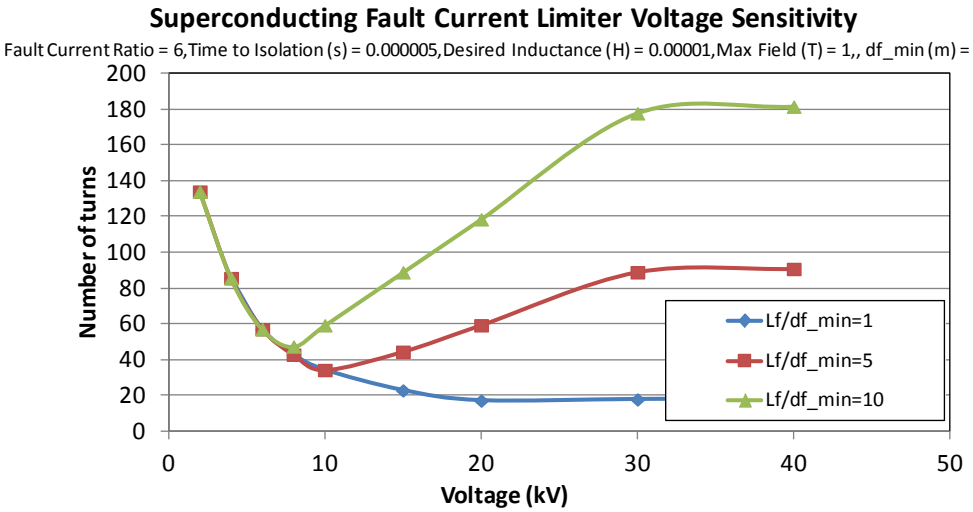


Figure 139.—Increased Number of Windings with Increased Voltage.

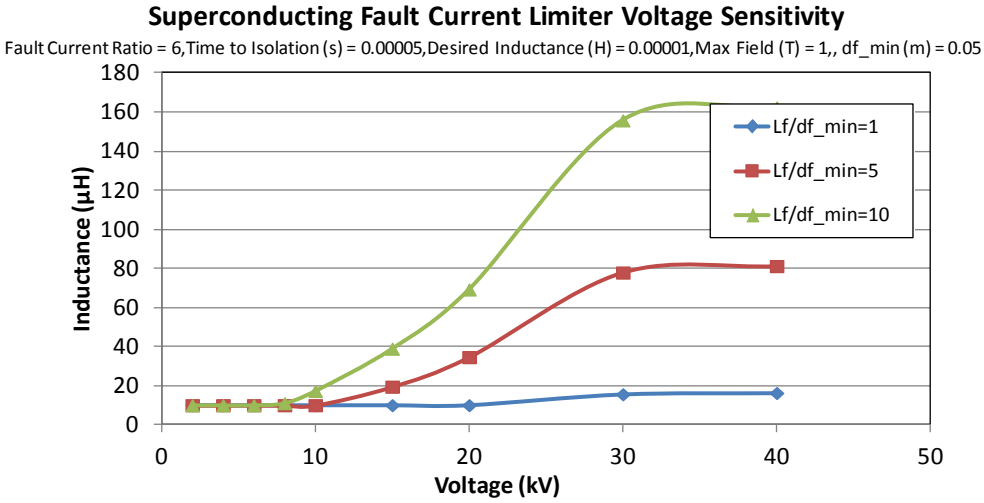


Figure 140.—Increase in Inductance at Higher Voltages due to Geometry Limits.

The increase in mass for the higher L/d limited cased in Figure 138 is a result of the increased number of windings (shown in Figure 139), with the increase in inductance from the increase in induction (shown in Figure 140).

5.6.11 Efficiency Trends

The efficiency of the SFCL is a function of the length of the superconducting wire and the superconducting resistive losses per unit wire length.

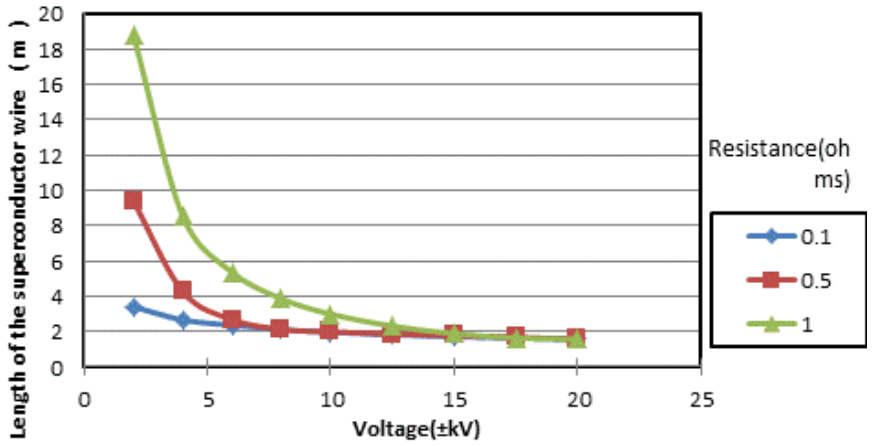
$$R_{sc} = \frac{EV}{P} l_{sc}$$

where

R_{sc} minimum required inductance
E per unit length superconducting electric field
P power required
l_{sc} length of the superconducting wire

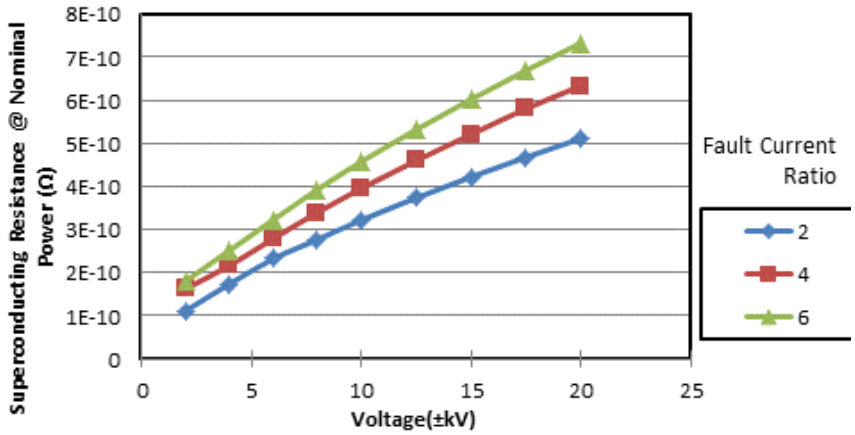
It is assumed that the power required remains constant at the design point, and that the electric field losses are defined for the critical current density at this design point. The resistance is directly proportional to the design voltage and the length of the superconducting wire (plotted against each other in Figure 141.

Resistance trends are illustrated in Figure 142 to Figure 145. In general, it is observed that as the design voltage increases the length of the superconducting cable required decreases. However, the critical current also decreases. Assuming a constant electric field loss per unit length at the critical current yields this upward trend.



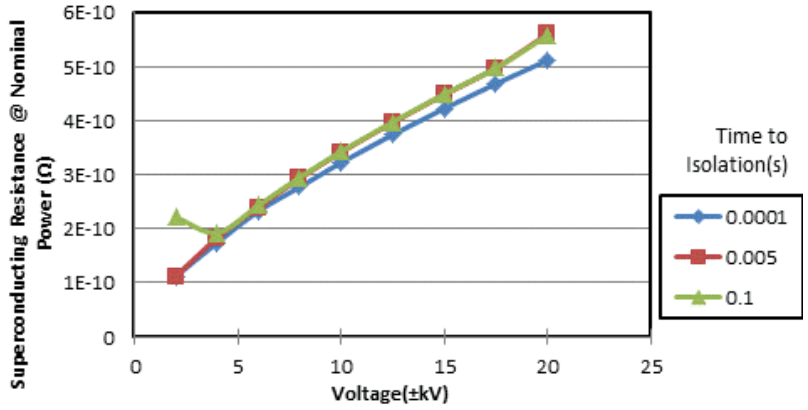
Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Fault Current Ratio=2, Time to Isolation(s)=0.0001, Desired Inductance(H)=0.00001, Time to heat dissipation(s)=30,

Figure 141.—Decreased Length of Superconducting Cable with Increased Voltage.



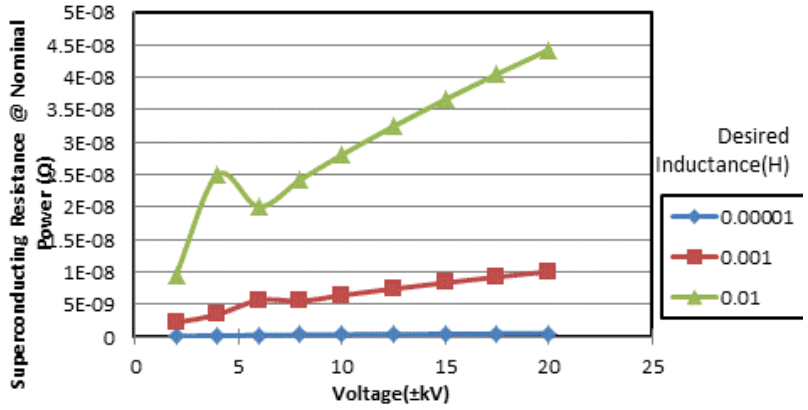
Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Time to Isolation(s)=0.0001, Desired Inductance(H)=0.00001, Resistance(ohms)=0.1, Time to heat dissipation(s)=30,

Figure 142.—Increase in SFCL Resistance w.r.t. Design Voltage for Varying Fault Current Ratio Requirements.



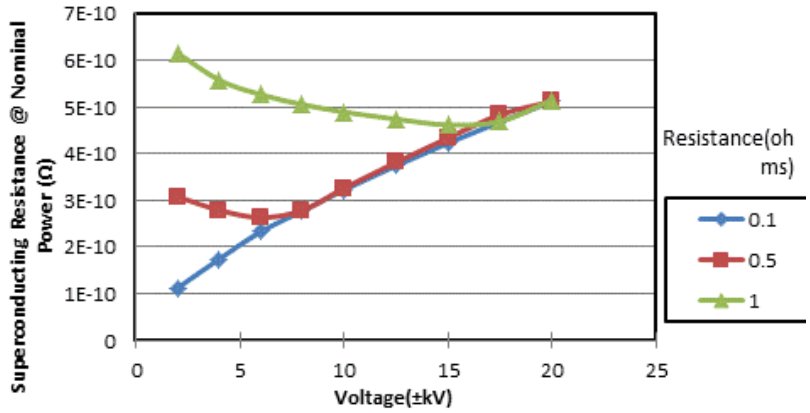
Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Fault Current Ratio=2, Desired Inductance(H)=0.00001, Resistance(ohms)=0.1, Time to heat dissipation(s)=30,

Figure 143.—Increase in SFCL Resistance w.r.t. Design Voltage for Varying the Time to Isolation.



Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Fault Current Ratio=2, Time to Isolation(s)=0.0001, Resistance(ohms)=0.1, Time to heat dissipation(s)=30,

Figure 144.—Increase in SFCL Resistance w.r.t. Design Voltage for Varying Solenoid Geometry Limits.



Peak Power(MW)=12.5, Nominal Power Ratio=0.5, Fault Current Ratio=2, Time to Isolation(s)=0.0001, Desired Inductance(H)=0.00001, Time to heat dissipation(s)=30,

Figure 145.—Increase in SFCL Resistance w.r.t. Design Voltage for Varying Desired Quench Resistance.

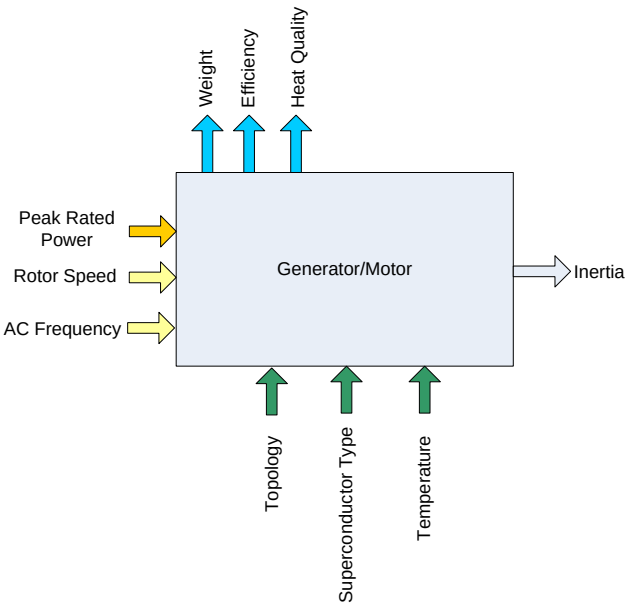


Figure 146.—Parameter Diagram for Motor Generator Model.

5.7 Generators

Generator weight and efficiency estimates were calculated using a high temperature superconducting machine design tool provided by NASA (Ref. 171). The weight and efficiency sensitivity assessments follow the parameter diagram in Figure 146.

The primary parameters used in machine scaling are rotor speed, AC frequency, and peak power rating. A fixed topology and superconducting type are assumed in this sensitivity. A three pole BSCCO square wire wound generator is assumed in this tool's machine sizing and performance sensitivity.

5.8 Cryogenic System

Very rough estimates of the weight penalty associated with system inefficiencies were used in this study. The cryocooler system was assumed to be a 30 percent efficient reverse Brayton cycle system with a power density of 3 kg/kW.

Cooling reservoirs, tubing, and flow management systems were not considered in detail for these parametric trade studies.

5.9 Component Sensitivity Modeling Summary

Through this section, the governing equations and development of each component model were presented along with the resulting component mass and efficiency trends as a function of the DC distribution voltage. Each individual component (generator, power converter, cable, circuit breaker, SFCL, and SMES) has an optimum mass or efficiency with corresponding DC bus voltage at which that optimum is achieved. The next phase of this contract will include assembling all of the component models and corresponding weight and efficiency sensitivities to DC bus voltage to form the designated TeDP architecture selected for this study. The framework for this assembly and system sensitivity modeling is discussed in Section 6.0. The system sensitivity model will be used to understand the system mass and efficiency sensitivity to DC distribution voltage. It is expected that the mass contribution of each component will serve as a weighting function and influence how each component's mass and efficiency sensitivity affect the system's sensitivities. To determine the system sensitivities, the system model will be exercised by sweeping the DC distribution bus voltage and computing the system mass and efficiency trends for many component control parameters such as AC system frequency, temperature, and superconductor type. Based on the system sensitivities, a narrower range of DC bus voltages will be recommended.

6.0 Narrowed DC Voltage Range

6.1 Introduction

The voltage range was narrowed by integrating the component sensitivity models generated for the prior deliverables. These models include sizing estimates for power electronics (converter, rectifiers), SMES energy (including converter), cables, superconducting fault current limiters, solid state circuit breakers, and electric machines. The models used for this systems sizing were described in the previous contract deliverables.

This integrated model was sampled over a range of operating voltages under series of assumptions regarding requirements and performance parameters. Additionally, the mass and power required for cryocooling was also captured by recording the cooling required for each system device, assuming a 30 percent reverse Brayton cycle efficiency, and assuming a specific power of 5 hp/lb for the cryocooling equipment.

On- and off-design scenarios were identified which size the electrical equipment, the cryocoolers, and determine the nominal system efficiency. Considering fail-safe operations, the equipment sizing requirements are generated by the single-engine-out scenario at takeoff. A thrust power of 25 MW is required from one turbogenerator during this scenario. While these requirements size the electrical and cryogenic equipment, the nominal efficiency was calculated assuming a 10 MW cruise thrust power required.

The energy storage system's role was limited to assisting with temporary fill-in power during a source failure.

The trends presented reflect general assumptions regarding protection system requirements. More accurate transient performance requirements for these devices will be explored as dynamic models of the system are completed and exercised.

6.2 Architecture Assumptions

The system considered for voltage selection is outlined in Table 29. The number of each component is given as well as the nominal and peak power requirements.

TABLE 29.—ARCHITECTURE COMPONENT BREAKDOWN

		Count	Single engine out rating at takeoff, MW	Nominal rating at cruise, MW
Electric Machines	Generator	4	12.5	6.25
	Motor	16	1.79	1.5625
Converter	AC/DC converter	4	12.5	6.25
	DC/AC inverter	16	1.79	1.5625
	DC/DC converter for SMES	4	12.5	0
Cables	AC	4	12.5	6.25
		16	1.79	1.5625
	Transmission	4	12.5 (2- by 30-m, 2- by 40-m)	6.25
	Feeder	16	1.79 (16- by 5-m)	1.5625
		16	1.34 (16- by 5-m)	0
Breakers	AC	12	12.5	6.25
		48	1.79	1.5625
	DC	16	12.5	6.25
		64	1.79	1.5625
		64	1.34	0
		2	12.5	0
SFCL	AC	12	12.5	6.25
		48	1.79	1.5625
	DC	8	12.5	6.25
		32	1.79	1.5625
		32	1.34	0
		2	12.5	0
En. storage	SMES	4	12.5	0

In the case of solid state circuit breakers and fault current limiters, the number of devices is large due to the number of poles or phases required for bi-polar DC and three-phase AC distribution. Each transmission and feeder line is configured to have two breakers at each end of the run to isolate line failures. Therefore, there are a total of four breakers per DC cable run. There is a single pair of fault current limiters per DC cable run and a set of three for each AC run.

Baseline assumptions for mass results displayed here are outlined in Table 30.

TABLE 30.—SYSTEM MODEL PARAMETERS BASELINE ASSUMPTIONS

Generator	Turbine speed ..... 8000 rpm Pole count ..... 3 Fault current ratio 2
Motor	Propulsor speed ..... 4000 rpm Pole count ..... 3 Fault current ratio 2
Cables	Transmission lengths ..... 30 m ..... 40 m AC lengths ..... 1 m Feeder length ..... 5 m Temperature rise on cable run ..... 0.5 K Fault current ratio 2
SFCL	Desired inductance ..... 100 μ H Desired quench resistance ..... 1 Ω Inductor core flux density ..... 0.5T Time to heat dissipation w/ fault ..... 5s Fault current ratio 2
SMES	Stored energy (4 s at 12.5 MW) ..... 50 MJ SMES voltage ratio to bus voltage ..... 0.25 Temperature ..... 18 Major to minor radius ratio ..... 4 Compressive quality factor ..... 0.5 Temperature rise across SMES ..... 0.5 K
Converters	Fault current ratio ..... 2 Temperature ..... 100 K Modulation index ..... 1 Power factor ..... 1 DC ripple voltage magnitude ..... 20% DC ripple current magnitude 10%
SSCB	Fault current ratio ..... 2 Temperature ..... 100 K

6.3 Electrical System Mass Sensitivity to Voltage

Assuming this configuration of system protection, the protection devices are the single largest contributing technology group to overall mass. This weight breakdown is illustrated in Figure 147. For this baseline architecture the optimal voltage is roughly ±4.5 kV.

Reductions in system weight may be possible by balancing the current blocking capability of the breakers and the converters. The switches sized for the generator and propulsor power electronics were selected due to their ability to block fault currents. If the conversion devices prove sufficient in fault current interruption, additional SSCB devices can be removed. However, solid state switches may still be required to reroute power from the alternative sources during a failure scenario.

The baseline configuration uses SSCBs and SFCLs for the protection of each device within the system. The result is a protection strategy which includes 7 protection zones between a single generator and a single propulsor. This zonal configuration is illustrated in Figure 148 with solid blue lines on the L1 brand. This protection strategy requires that each all of the devices highlighted in green and yellow be engaged in system protection. The alternative extreme would be to rely completely on the converter devices to provide fault isolation and only retain the SSCBs which allow for power rerouting during a failure. This eliminates all the yellow highlighted SSCBs in Figure 148 and results in a 3 zone protection scheme. This means that any feeder fault will result in a loss of the branch. However, it may remove the 12 higher power AC SSCBs on the generator side and 48 lower power AC SSCBs on the motor side. Additionally, 16 high power DC SSCB are eliminated and 64 low power DC SSCB on the feeders.

Figure 149 illustrates the weight breakdown for the system for this reduced protection equipment approach. Removal of all of these overly-protective devices results in a reduction in overall system weight of approximately 20 percent.

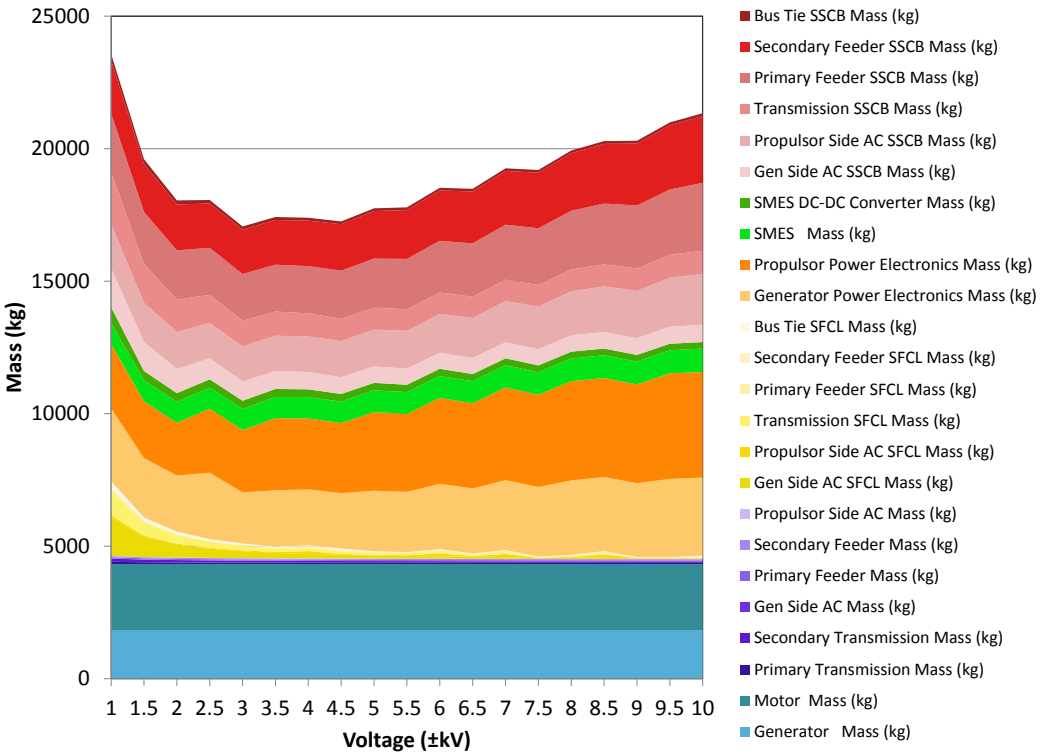


Figure 147.—Weight Decomposition with Component Count from Table 1 and Assumptions from Table 2.

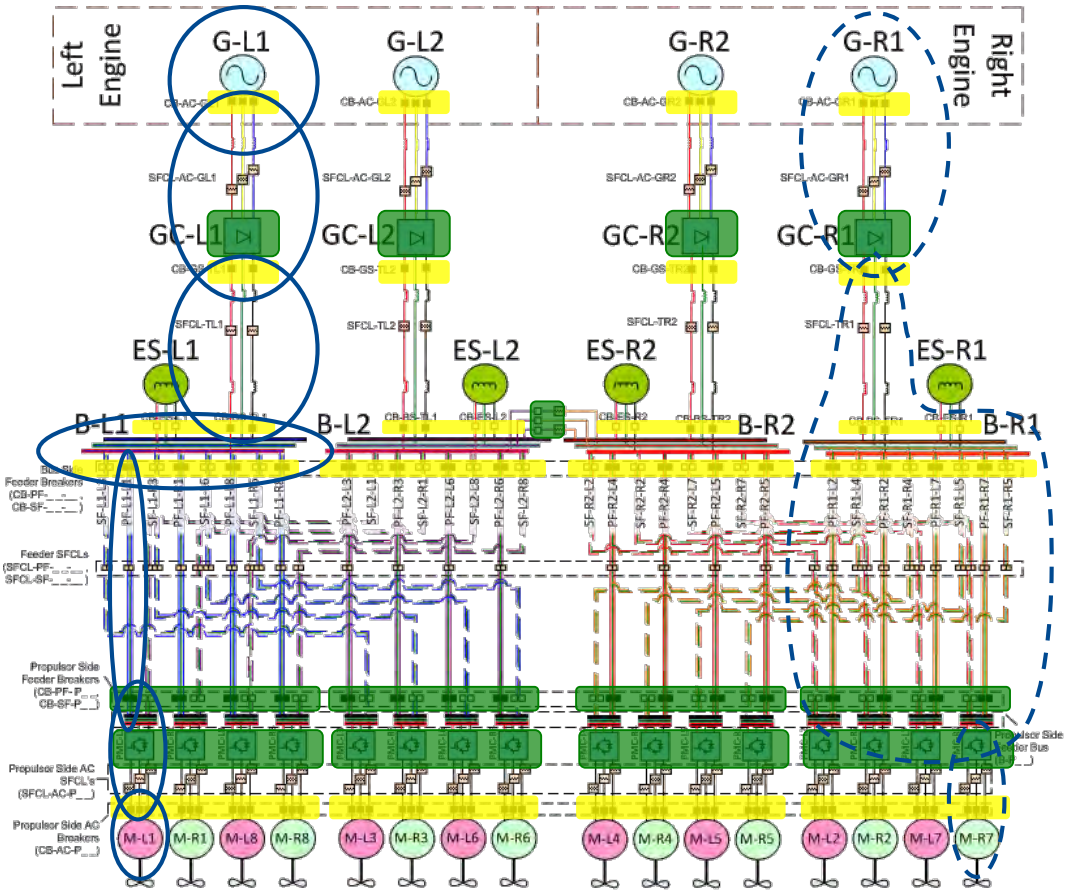


Figure 148.—Zonal Protection Alternatives.

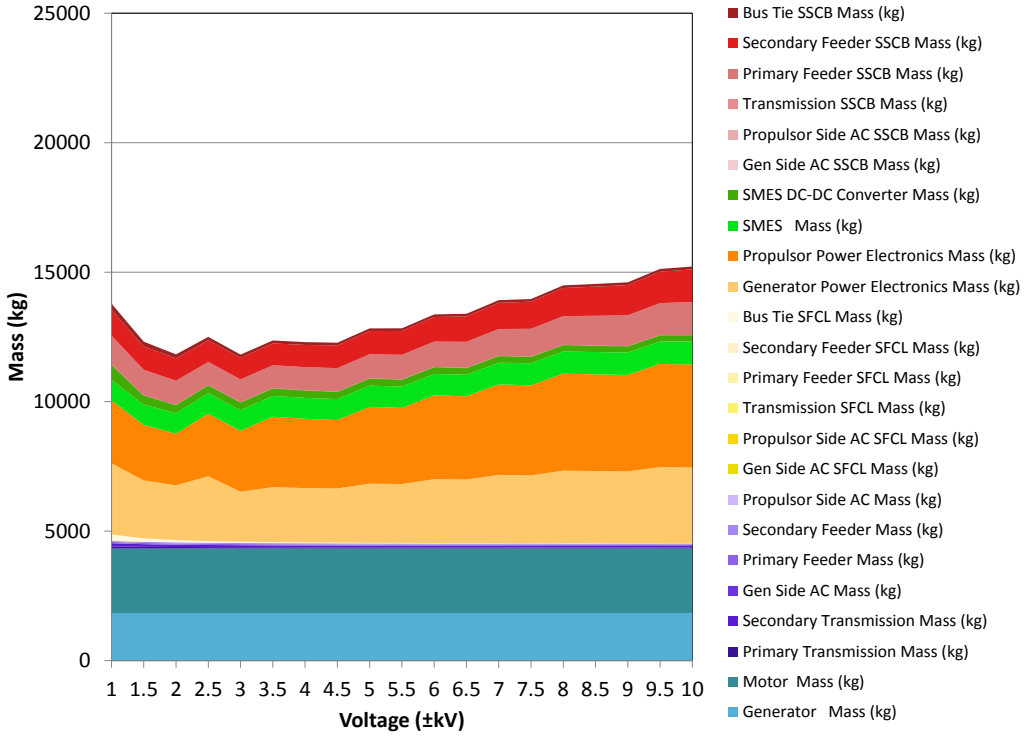


Figure 149.—Weight Decomposition with no Protection SSCBs or SFCLs.

In addition to addressing specific technology improvements, other weight savings may be available by descoping or removal of the energy storage, eliminating fault current limiters, or refocusing on AC distribution with oversized AC lines to reduce conductivity losses. While this approach does reduce the ability to independently throttle the propulsors, it reduces the weight of the converters and eliminates converter switching and conduction losses. This benefit must be balanced with the increase the AC conduction losses in the distribution system.

It is likely that the actual protection and recovery solution will yield a system which sits between the baseline and minimalist systems considered in this section. Configuring the system for fault isolation and recovery depends on the results of dynamic models. However, evaluation of the voltage sensitivity for both of these systems indicates that the optimal voltage is not highly dependent on the number and ratings of the protection devices.

6.4 Electrical System Cooling Requirements Sensitivity to Voltage

Losses play a major role in determining the overall system mass. Figure 150 and Figure 151 illustrate the overall heat load to the cryo-cooling system generated during nominal and peak loading scenarios.

The major contributors to the heat load which must be managed by the cryogenic cooling system can be sources to the SSCBs (pink layers) and the converters (orange layers). The solid state circuit breaker losses decrease with voltage, while the propulsor converter losses increase with voltage. These trends follow the IGBT and diode device scaling discussed in the previous deliverable.

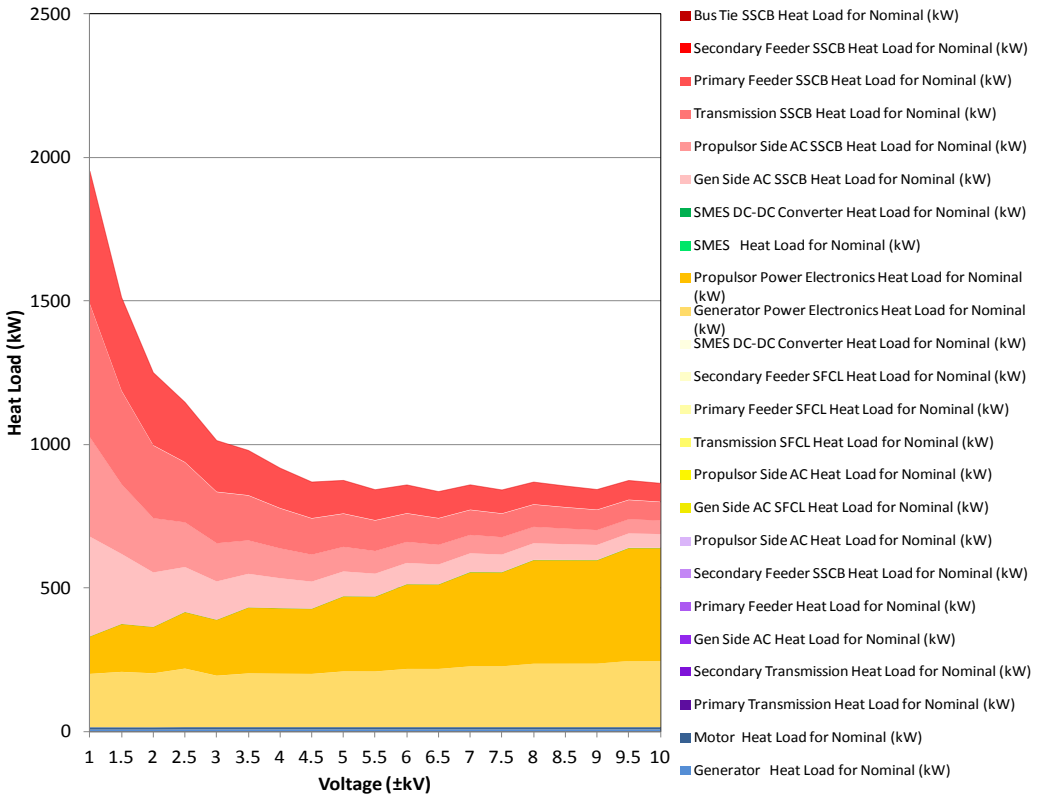


Figure 150.—Heat from Devices during 10 MW Nominal Operation for Baseline Configuration and Losses.

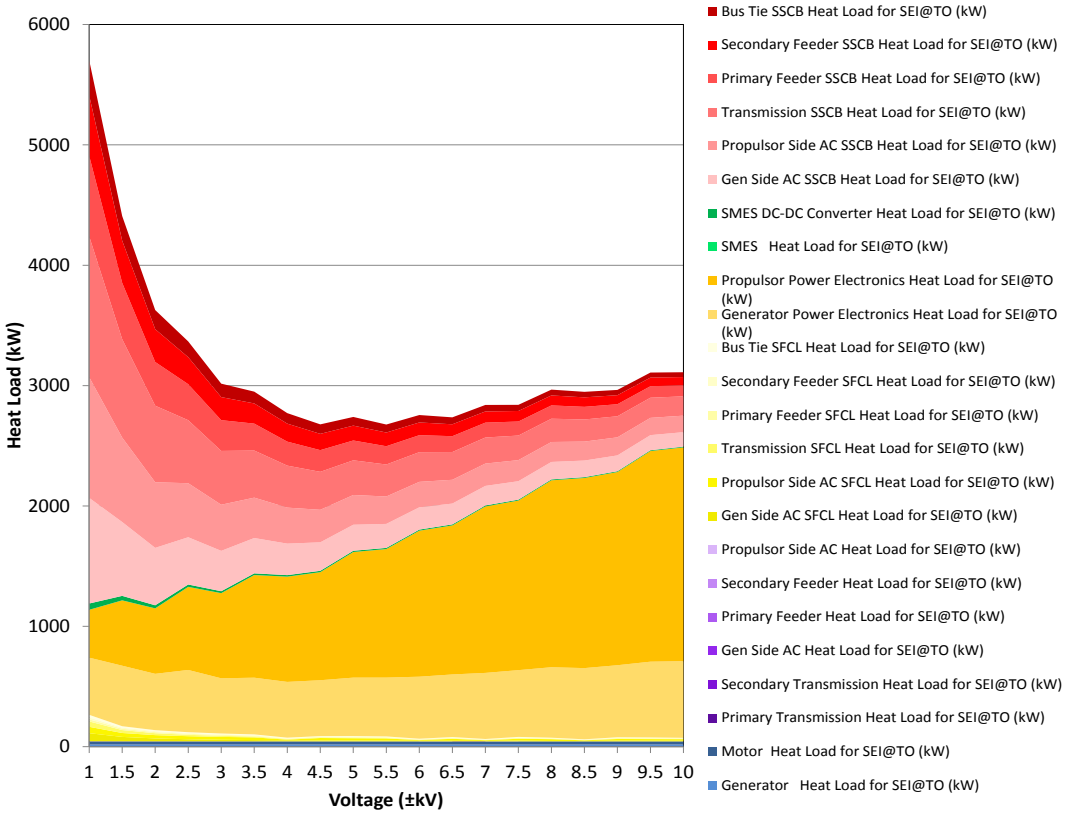


Figure 151.—Temporary Heat from Devices during 25 MW Single Engine Out at Takeoff Scenario for Baseline Configuration and Losses.

The minimum heat load from the baseline system during nominal operation is approximately 800 kW. This represents an 8 percent of the overall 10 MW nominal load. Assuming a 30 percent efficient cryocooler and the operating temperatures in Table 2, the power required for cryocooling is a little less than 6 MW.

For the single engine out scenario at takeoff, the power required is 25 MW. Fill-in power is provided temporarily by the energy storage (illustrated in Figure 151). After this support during system reconfiguration, the loss sensitivity to voltage follows the trends in Figure 152. For this baseline configuration, the steady state losses during this scenario are equal to roughly 9 percent of the overall power. For this magnitude of losses, the overall cryocooling power required is roughly 16 MW. As with mass reduction, it is expected that the losses will be reduced by reducing the scope of the protection equipment. Removing all SSCB which are not allocated to rerouting of power yields improvements illustrated in Figure 152 and Figure 153 (this does not capture the increase in size and losses due to modifications to converter requirements). Conversion losses and rerouting SSCB's are retained for these trends.

Comparing the results illustrated in Figure 149, Figure 150, and Figure 151 with those illustrated in Figure 152, Figure 153, and Figure 154, there is an obvious reduction in overall heat loss to the cryogenic system with a reduction in protection equipment. Also, large low voltage losses associated with the SSCB's is also largely mitigated and a clear optimal voltage which minimized the losses is evident.

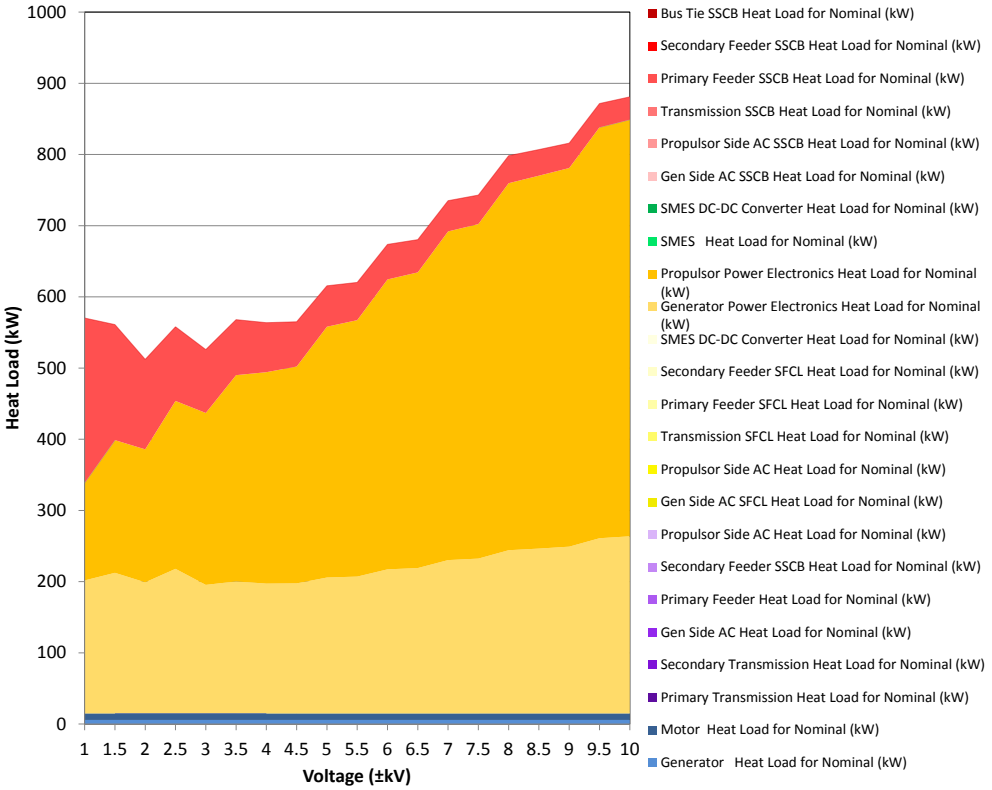


Figure 152.—Heat from Devices during 10 MW Nominal Operation for Configuration with no Protection SSCB's or SFCL's.

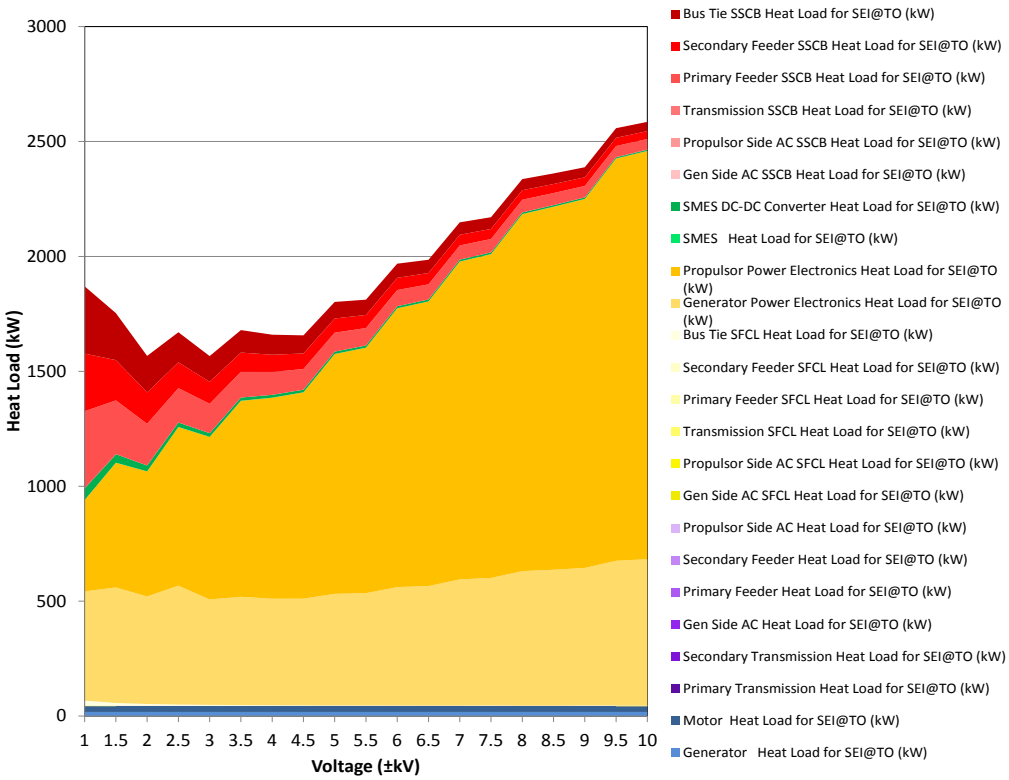


Figure 153.—Temporary Heat from Devices during 25 MW Single Engine Out at Takeoff Scenario for Configuration with no Protection SSCB's or SFCL's.

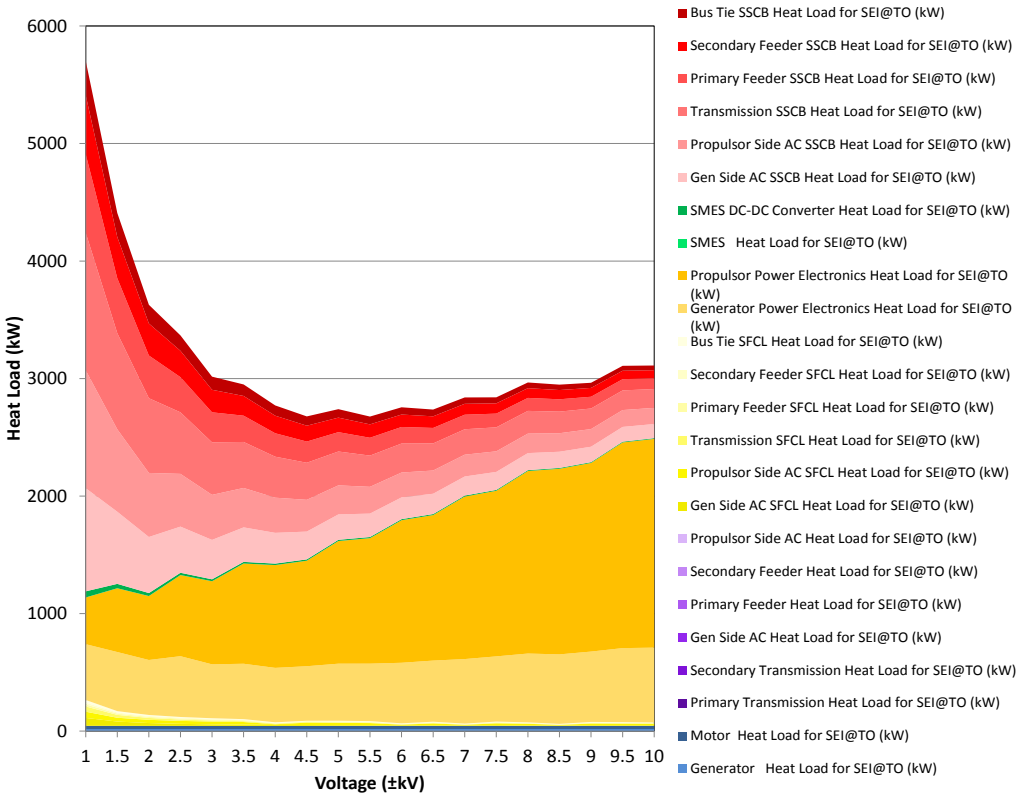


Figure 154.—Steady State Heat from Devices during 25 MW Single Engine Out at Takeoff Scenario for Baseline Configuration.

6.5 IGBT and Diode Switching and Conduction Losses

An alternate method to descoping the protection system is to target device improvements. The largest contributor to system inefficiencies are the switching and conduction losses in the converters and SSCB's generated by the IGBT's and diodes. Improvement in switching and conduction efficiency has a dramatic effect on the overall system weight. Improvements in IGBT and diode efficiency of 50 and 90 percent are illustrated in Figure 154, Figure 155, and Figure 156.

The improvements illustrated in these figures also drive corresponding decreases in cryocooler power requirements.

6.6 Cryocooler Mass

Depending on the redundancy of the cryogenic cooling systems, its mass lies between two limits illustrated in Figure 157. The lower limit is generated by the total heat load during the takeoff scenario. This scenario requires the largest magnitude of thrust power and the largest magnitude of heat rejection to the thermal management system. The upper limit is a system with components dedicated to each electrical device exclusively as sized for the single engine out at takeoff scenario.

Cryogenic system mass reductions are available with reduction in overall heat rejection as discussed in the previous section. Reductions in the mass range for these systems are illustrated in Figure 158.

As is evident from these trends, the optimal mass of the system can be more a function of the efficiency of the electrical system than the mass of the system itself. Mass improvements on the electrical side are desirable. However, these improvements must avoid associated increases in heat loss to the cryo-system. Figure 159 illustrates the relative size of the cryo-system (in blue) to the electric system (in purple) with variations in the switching and conduction efficiency.

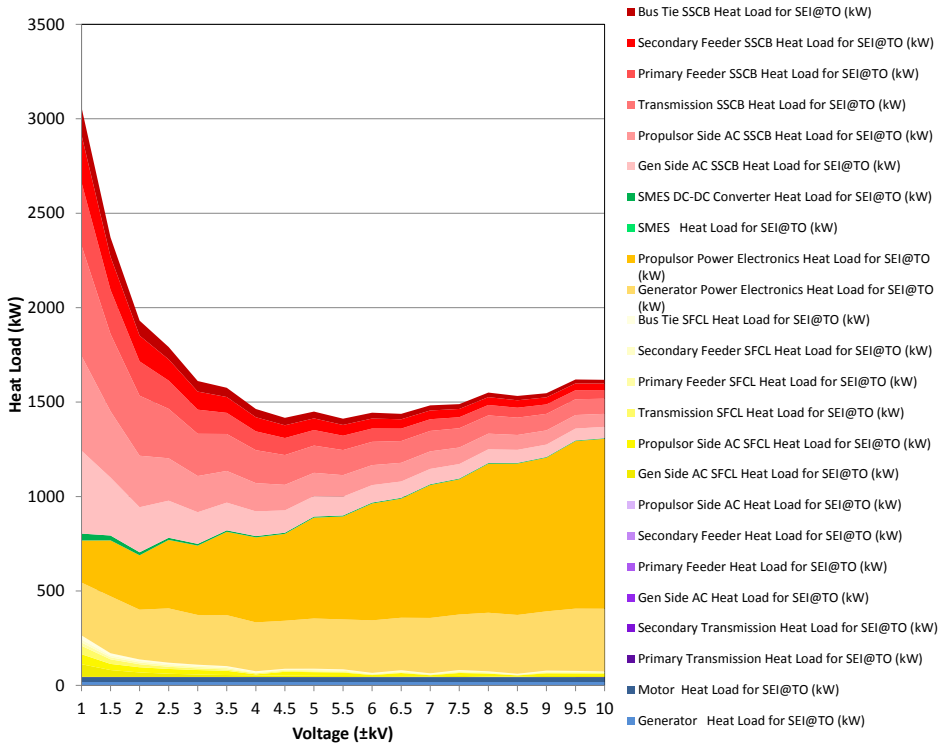


Figure 155.—Steady State Heat from Devices during 25 MW Single Engine Out at Takeoff Scenario for Baseline Configuration with 50 percent Decrease in Switching and Conduction Losses.

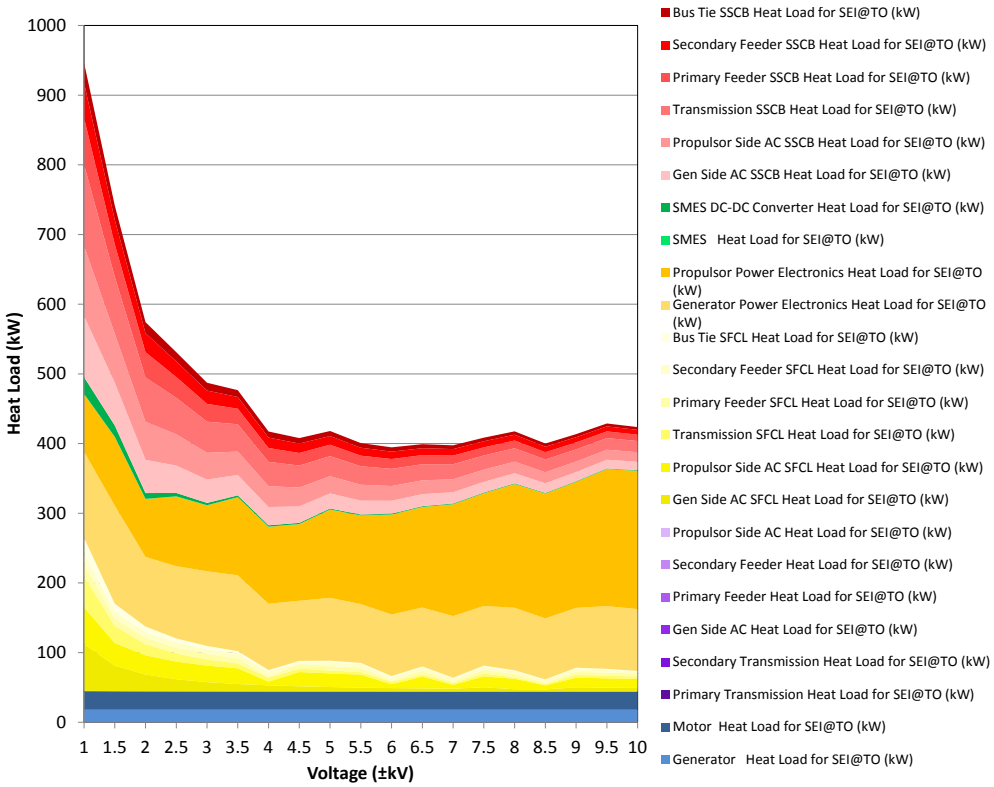


Figure 156.—Steady State Heat from Devices during 25 MW Single Engine Out at Takeoff Scenario for Baseline Configuration with 90 percent Decrease in Switching and Conduction Losses.

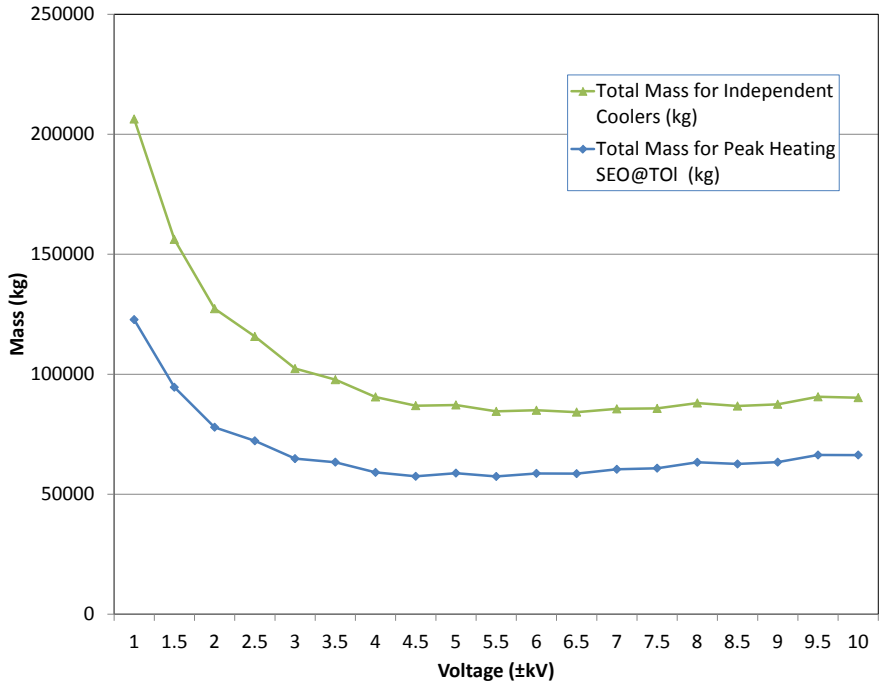


Figure 157.—Upper and Lower Limits for Cryocooler Size with a Reduction.

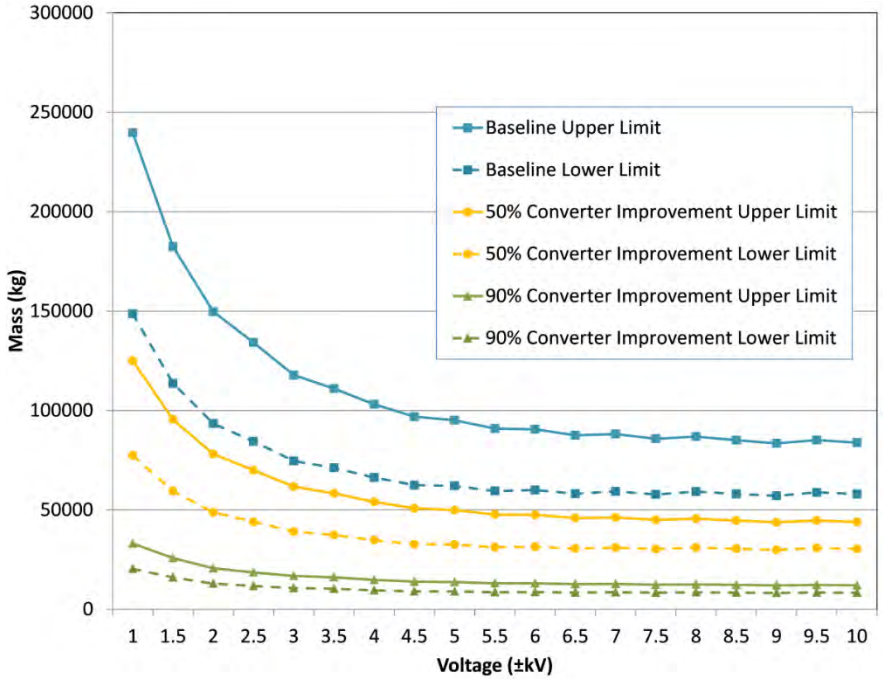


Figure 158.—Reductions in Cryogenic System Mass Due to Converter Efficiency Improvements.

6.7 Narrowed Voltage Range

For all the configuration and converter efficiency variations of the architecture discussed here, the optimal voltage level never exceeds ±4.5 kV. With architecture changes and efficiency improvements, the optimal voltage may drop as low as ±2 kV. This remains consistent with variations in the converter efficiency (Table 31).

TABLE 31.—OPTIMAL POLE VOLTAGE FOR A 25 MW TEDP SYSTEM
FOR VARIOUS CONFIGURATION AND EFFICIENCY IMPROVEMENTS

	Baseline switching loss	50% improvement in converter losses	90% improvement in converter losses
Baseline system	±4.5 kV [17,254 / 57,434]	±4.5 kV [16,451 / 31,170]	±4.5 kV [15,808 / 10,159]
Without protection SSCBs and all SFCLs	±3 kV [11,816 / 33,659]	±3 kV [11,126 / 18,872]	±4.5 kV [10,828 / 6,611]
Without energy storage, protection SSCBs and SFCLs	±2 kV [10,708 / 33,175]	±3 kV [10,036 / 18,672]	±4.5 kV [9.748 / 6,563]

Optimal Voltage (±kV)
[Mass of electrical/cryo equipment (kg)]

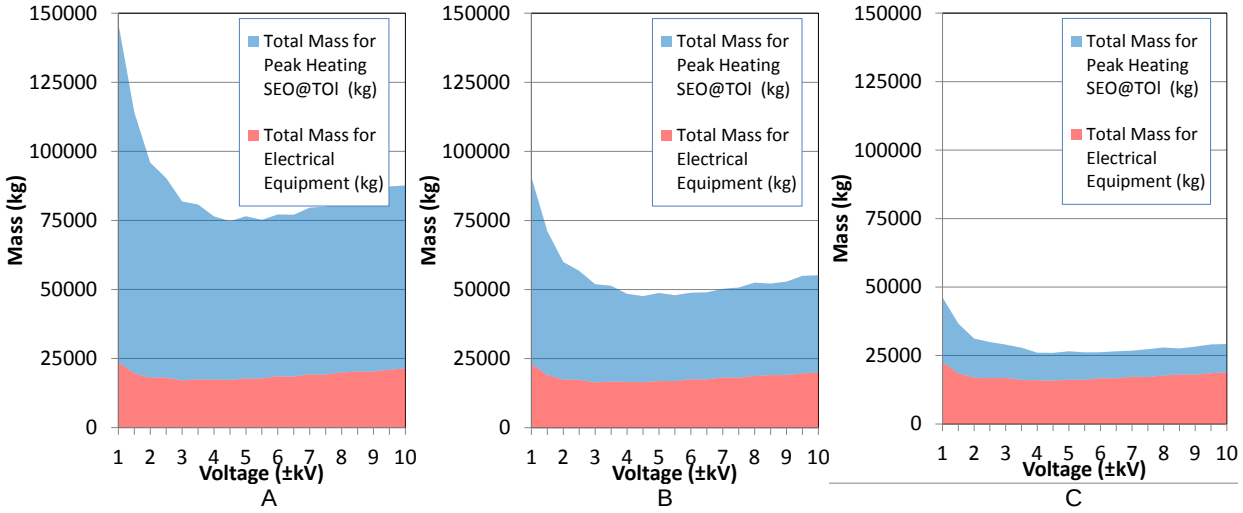


Figure 159.—Relative Mass of the Cryo and Electric Systems with Converter Efficiency Improvements (A- Baseline Switching and Conduction Losses, B- 50 percent Improvement, C- 90 percent Improvement).

Considering these results and taking into account both electrical and cooling contributions, the target voltage range for this system is between ±2 and ±4.5 kV. However, it is expected that system improvements necessary to reduce the losses to minimize cryogenic system mass will push this optimal voltage to the lower end of that range. The mass was also seen to be insensitive to voltage selection on the range of approximately ±2 kV. For a baseline system, a 2 kV increase or a 1 kV decrease from the sizing voltage only results in an approximate 5 percent increase in system mass. For the minimalist protection system, the target voltage range shifts as a function of converter efficiency. These 5 percent mass variability ranges are highlighted in Figure 160 and Figure 161.

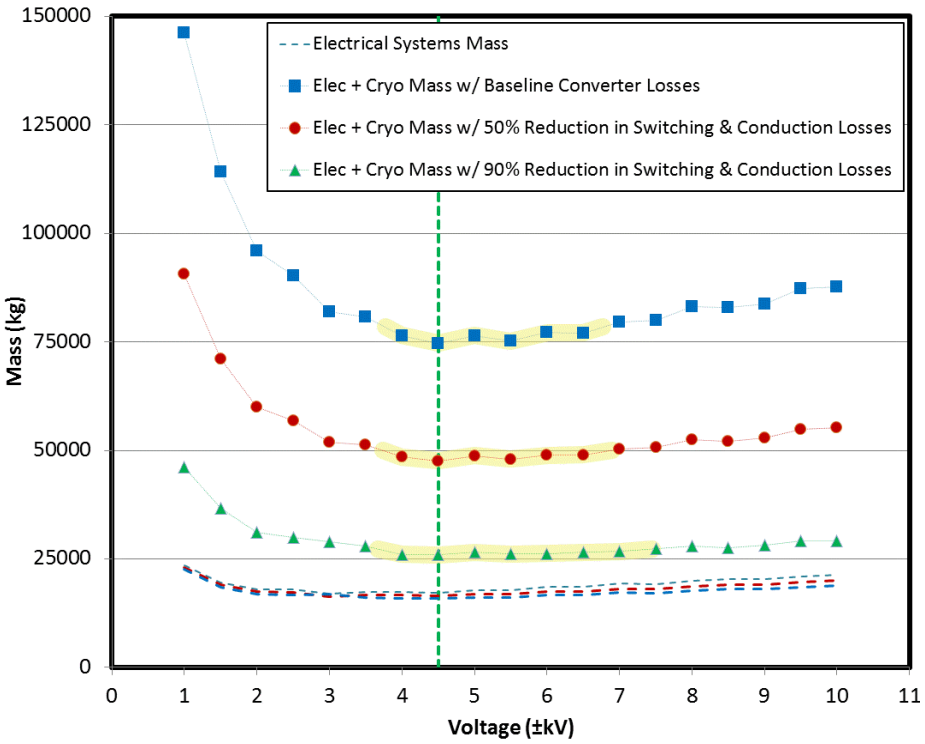


Figure 160.—Baseline Architecture Voltage Sensitivity.

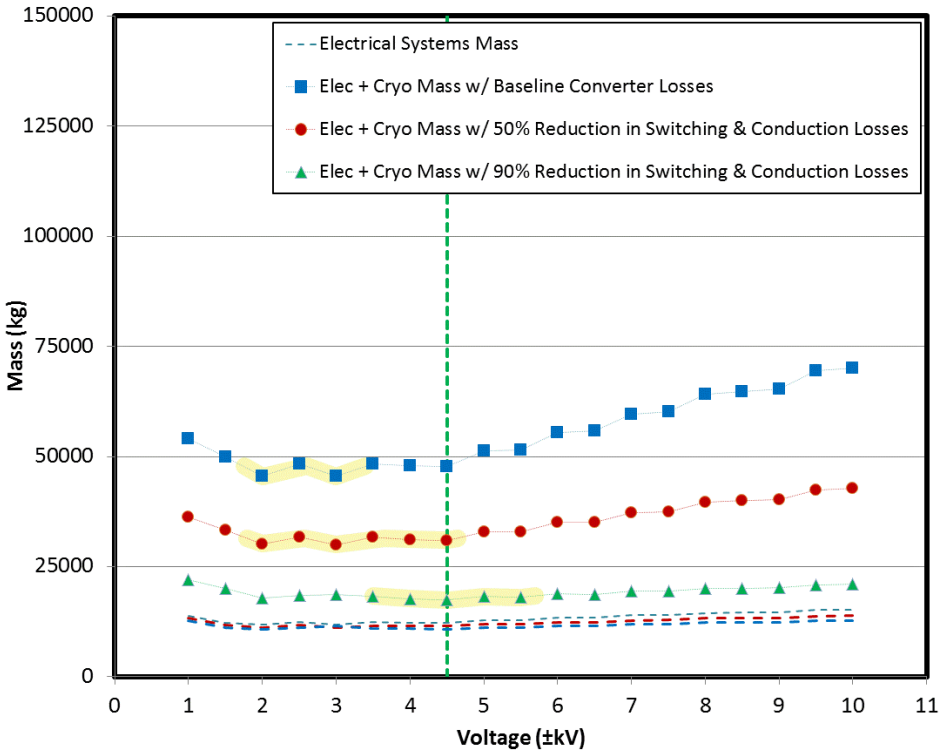


Figure 161.—Reduced Protection System Architecture Voltage Sensitivity.

7.0 GT Dynamic Model

7.1 Introduction

To identify regulation, protection, and recovery requirements, Georgia Tech/ASDL was tasked with developing preliminary models of switching, isolation, and protection components. The components that were modeled include: superconducting fault current limiter, solid-state circuit breaker, rectifier, inverter, and superconducting magnetic energy storage. Most of the models were created using the SimPowerSystems toolbox in MATLAB Simulink (The MathWorks, Inc.). Some state-space models were created as well in an effort to decrease the required time for simulation.

Once the protection component models were completed, dynamic system models were developed which captures the response of the state variables (current and voltage). Several failure scenarios were modeled including branch faults and engine failures. The current and voltage excursions observed in this system, as well as loss of propulsive power to the loads provide more accurate requirements to the TeDP system components and establish the voltage limits for normal and abnormal operating scenarios.

7.2 Superconducting Fault Current Limiter

As discussed in the parametric sizing model development, superconducting fault current limiters can fall under two categories: resistive type and inductive type. The resistive type SFC has advantages of having a high limitation level and compact size (Ref. 172), so the resistive type was selected for the model. Resistive type SFCL can be made using either YBCO; however, Bi-2223 is commonly used since its resistivity changes faster with temperature (Ref. 173). Hence, Bi-2223 was selected for the models that will be described. The approach to identifying quench dynamics for this component follows similar assumptions as those applied for estimating the quench time for the parametric sizing model.

7.2.1 SFCL Modeling Overview

During the literature review, several approaches to modeling the resistance of the SFCL were available. The most widely used is the one that is presented in Blair and Nemdili (Refs. 173 and 174). With this approach, the resistance of the SFCL is determined based upon the operating point of the SFCL. The resistance of the SFCL is calculated as:

$$R_{SFCL} = \frac{E * L_{sc}}{I}$$

L_{sc} is the length of the superconductor. I is the current flowing through the SFCL. E is the electric field. How the electric field is calculated is dependent on the state of the SFCL. The SFCL can operate in three regions: superconducting, flux flow, and normal conducting. The operating region of the SFCL can be determined using the SFCL temperature (T_{sc}) and electric field calculation from the previous iteration. (The initial electric field of the superconductor (E_0) is an input provided by the user.)

If the temperature of the SFCL is less than the superconductor critical temperature (T_c) and less than E_0, then it is assumed that the SFCL is operating in the superconducting region. In this region, the electric field can be calculated as (Ref. 173):

$$E = E_c\left(\frac{J}{J_c(T)}\right)^{\alpha_T}$$

E_c is the critical electric field. J is the current density of the SFCL. $J_c(T)$ is the temperature dependent critical current density of the superconductor. If the SFCL temperature is less than the superconductor temperature, the critical current density can be calculated as (Ref. 173):

$$J_c(T) = \left[\frac{T_c - T_{sc}}{T_c - T_a}\right] J_{c77K}$$

T_a is the ambient temperature. In the model, it is assumed that this is the temperature of LN_2 (77 K). J_{c77K} is the critical current density of the superconductor at the ambient temperature of 77K. If the temperature of the SFCL is higher than the critical temperature, then the critical current density is set to J_{c77K}.

α_T is a temperature dependent shaping parameter. It is calculated as (Ref. 173):

$$\alpha_T = \max[\beta, \alpha'(T)]$$

$$\alpha'(T) = \frac{\log\left(\frac{E_0}{E_c}\right)}{\log\left[\left(\frac{J_{c77K}}{J_c(T)}\right)^{1-\frac{1}{\beta}}\left(\frac{E_0}{E_c}\right)^{\frac{1}{\alpha(77K)}}\right]}$$

β is another shaping parameter which is dependent on the material of the superconductor. $\alpha(77K)$ is the α shaping parameter at the ambient temperature of 77 K. This parameter is also dependent on the material selection.

If the temperature of the SFCL is less than the critical temperature, but the electric field from the previous iteration is greater than the initial electric field, the SFCL is in the flux-flow region. In this region, the electric field is calculated as (Ref. 173):

$$E = E_0\left(\frac{E_c}{E_0}\right)^{\frac{\beta}{\alpha(77K)}}\left(\frac{J_c(77K)}{J_c(T)}\right)\left(\frac{J}{J_c(77K)}\right)^{\beta}$$

If both the critical temperature and the initial electric field are exceeded, then the SFCL is in the normal conduction region. In this region, the electric field is calculated as (Ref. 173):

$$E = \rho(T_c)J$$

ρ is the normal resistivity of the superconductor. Again, this value will be dependent on the material chosen for the superconductor.

These calculations require that the temperature of the SFCL be calculated. The temperature of the SFCL will depend on the ambient temperature, resistance of the SFCL, current flow, and the heat transfer properties of the SFCL and coolant.

7.2.2 SFCL SimPowerSystems Model

A model of the SFCL was created using SimPowerSystems. The model is shown in Figure 162. A simple power system was created to test the performance of the SFCL. The system has a source that consists of an ideal AC voltage source in series with a resistance and inductance. The system has a simple resistive load. A ground fault is placed in the system and activated at a time specified by the user of the

model. The resistance calculation block contains the algorithm for calculating SFCL resistance that was presented in the previous section. The temperature calculation is performed using a thermal equivalent circuit which is shown in Figure 163. The thermal model has an input of the SFCL current. Also, the thermal resistance and capacitance of the SFCL must be specified. In a thermal equivalent circuit, voltage is equivalent to temperature. So, the ambient temperature is represented by a voltage source is the system. The temperature of the SFCL is found by measuring the voltage across the capacitor in the circuit.

The parameters that must be set by the user are shown in Table 32 along with the settings that were used for an example simulation. The large number of input variables allows the user to model a variety of types of SFCL designs.

An example simulation is presented to demonstrate the capabilities of the model. Of course, if input parameters are changed, (different system with a fault, different type of SCFL, etc.) the performance of the SFCL will change.

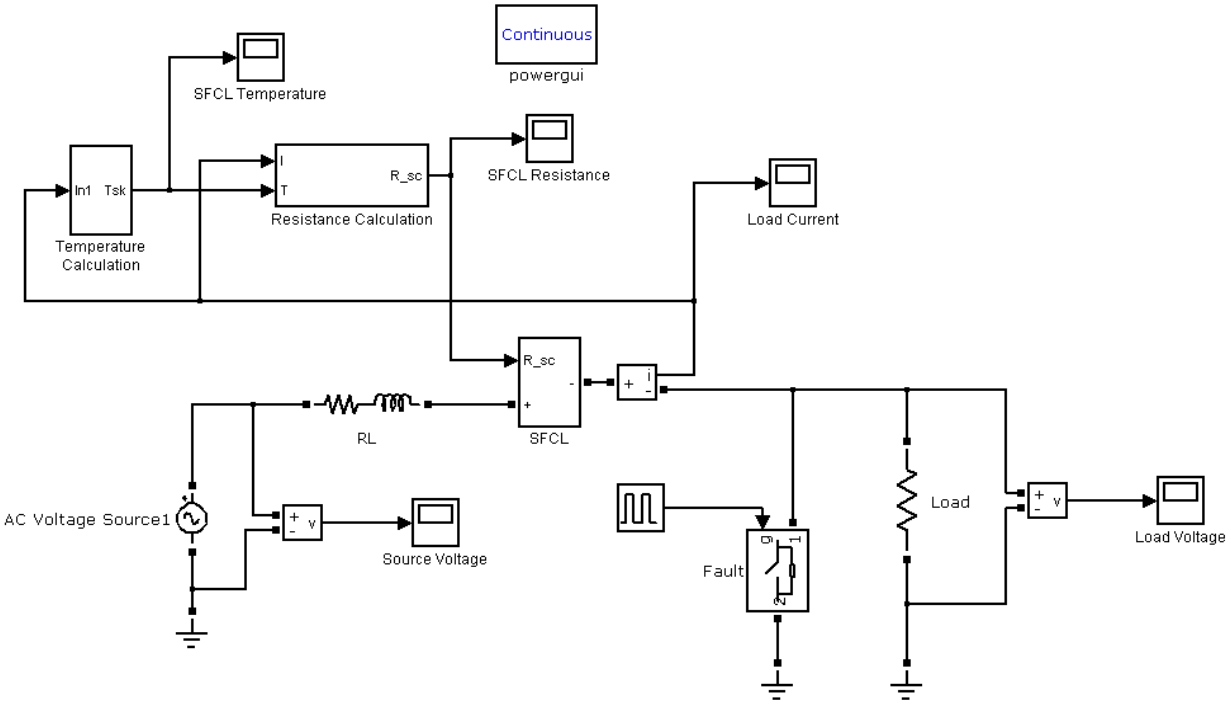


Figure 162.—SFCL SimPowerSystems Model.

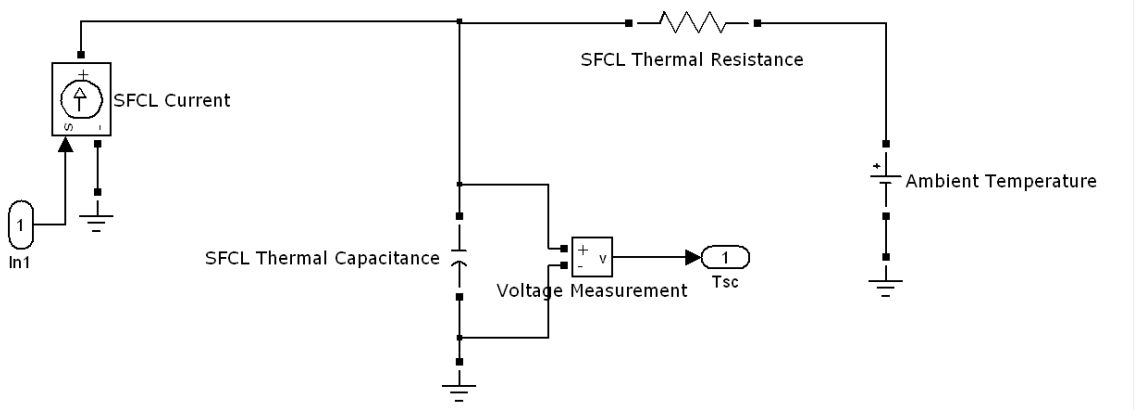


Figure 163.—SFCL Thermal Equivalent Circuit.

TABLE 32.—SFCL SIMPOWERSYSTEMS MODEL PARAMETERS

	Parameter	Setting for example simulation
System parameters	Source voltage, V	110
	Source frequency, Hz	60
	Line resistance, Ω	0.001
	Line inductance, H	0.0006
	Load resistance, Ω	2
	Fault start time, s	0.05
	Duration of fault, s	0.01
	Ambient temperature, K	77
Superconductor properties	Material density, kg/m^3	9.2×10^{3}
	Cross-sectional area, m^2, (Ref. 175)	2.4×10^{-6}
	Length, m	22
	Initial electric field, V/m, (Ref. 173)	0.1
	Critical electric field, V/m, (Ref. 173)	1×10^{-4}
	Critical current density at 77 K, A/m^2, (Ref. 174)	1.5×10^{7}
	Beta (Ref. 174)	3
	Alpha at 77 K (Ref. 174)	6
	Normal resistivity, Ω/m, (Ref. 174)	1×10^{-6}
	Critical temperature, K	95
	Thermal conductivity, W/(mK)	6.5
	Heat capacity at constant pressure, J/gK, (Ref. 176)	0.162

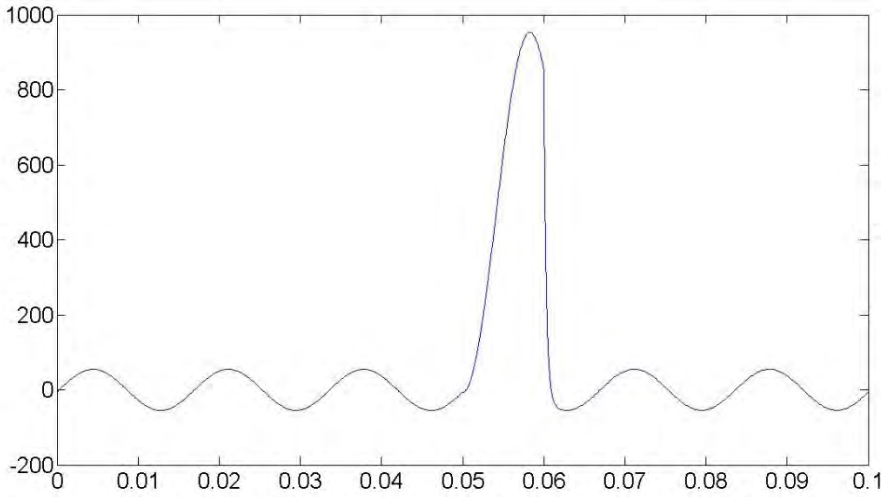


Figure 164.—System Fault Current without Protection.

First, the system was simulated without the SCFL to show the fault condition of the system without any protection. The fault current is shown in Figure 164, and the load voltage is shown in Figure 165. The results show a rapid rise in current when the fault occurs. The current during the fault rises to almost 10 times the steady-state current. When the fault clears, there is a large increase in voltage across the load, and the voltage spikes to about 15 times the steady-state condition.

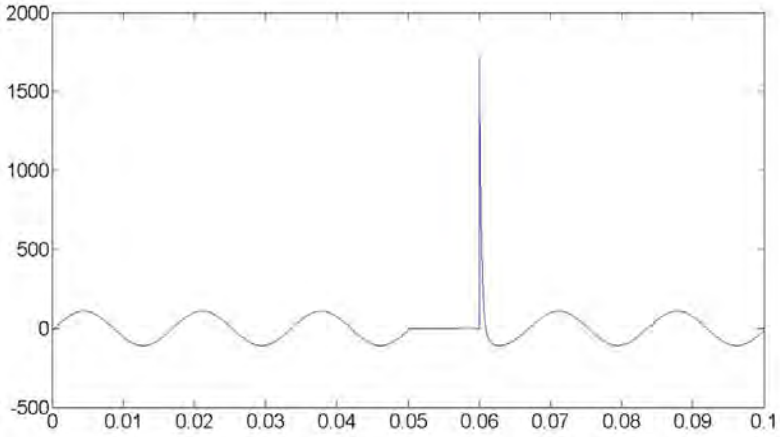


Figure 165.—Example System Load Voltage without Protection (V).

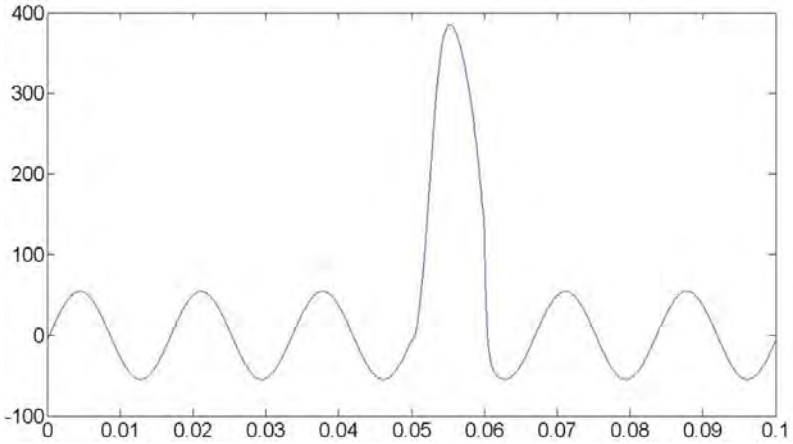


Figure 166.—Fault Current with SFCL (A)—SimPowerSystems Model.

Next, the simulation was performed with the added resistance from SFCL. The new fault current and load voltage are shown in Figure 166 and Figure 167. The change in resistance and temperature of the SFCL are shown in Figure 168 and Figure 169. The SFCL limits the current to about 400 A—smaller than half the magnitude of the fault current without any protection. Also, the magnitude of the voltage spike after the fault is greatly reduced. Rather than spiking to almost 1800 V, the voltage is limited to less than 300 V. These benefits are realized due to the increase in resistance of the SCFL. As shown in Figure 168, the resistance of the SCFL increases from almost zero to about 0.25 Ω. Figure 169 demonstrates a temperature rise of about 3° in the SCFL. While this temperature rise will cause some changes in the SCFL, it is not enough to cause it to quench. Therefore, the increase in current must be due to an increase in electric field caused by the increase in current. Soon as the current is restored to normal levels, the SCFL will recover and return to a superconducting state.

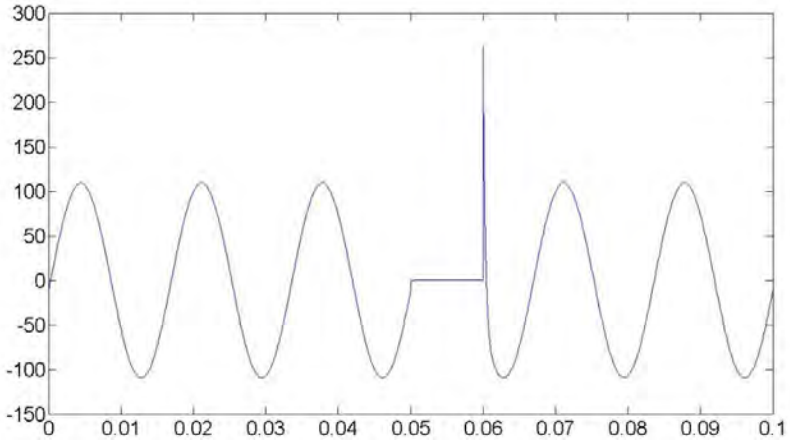


Figure 167.—Load Voltage with SFCL (V)—SimPowerSystems Model.

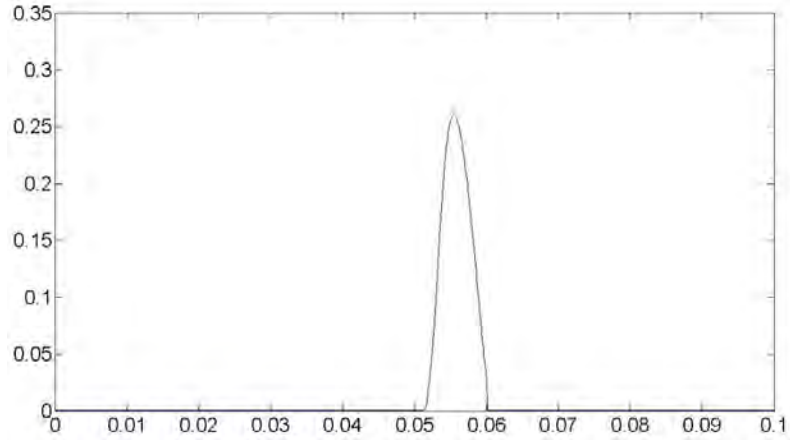


Figure 168.—SFCL Resistance (Ω)—SimPowerSystems Model.

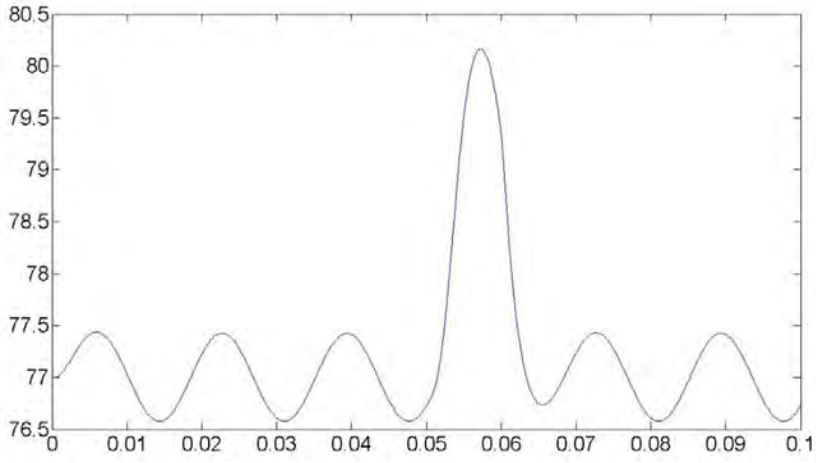


Figure 169.—SFCL Temperature (K)—SimPowerSystems Model.

7.2.3 SFCL State-Space Model

While the SimPowerSystems model represents the system well, it can be slow to run and also requires the use of the SimPowerSystems toolbox. To overcome these obstacles, a state-space model of the SFCL was also constructed. The state-space model solves a set of partial differential equations to find the response of the system. The set of equations can be found by using Kirchhoff's circuit laws. Applying Kirchhoff's voltage laws to the circuit shown in the SimPowerSystems model, the following three equations are obtained:

$$V_s(t) = IR + L\frac{dI}{dt} + IR_{SFCL} + i_F R_F$$
$$i_F R_F = i_L R_L$$

$$V_s(t) = IR + L\frac{dI}{dt} + IR_{SFCL} + i_L R_L$$

V_s is the source voltage. R is the line resistance. L is the line inductance. I is the current through the SFCL. R_{SFCL} is the resistance of the SFCL. R_f is the resistance of the switch that causes the fault. Under normal conditions, this is set to a very high value. When the fault occurs, this resistance becomes very small. i_F is the current through the switch causing the fault. i_L is the current through the load. R_L is the resistance of the load.

Also, using Kirchhoff's current law:

$$I = i_F + i_L$$

Using the current law relation and the second voltage law equation, the following relation is obtained:

$$i_L = \frac{IR_F}{R_L + R_F}$$

Substituting into the third voltage law equations, the following circuit equation is obtained:

$$V_s(t) = IR + L\frac{dI}{dt} + IR_{SFCL} + \frac{IR_F}{R_L + R_F}R_L$$

The equation can be solved to obtain the fault current in the system. The load voltage can be calculated as the product of the load current and load resistance. The resistance of the superconductor was calculated the same way as described in the beginning of this section and used in the SimPowerSystems model. Instead of using a thermal equivalent circuit, a different approach was used to calculate the temperature of the SFCL. The equations used were (Ref. 177):

$$C\frac{dT}{dt} = Q - W$$
$$Q = I^2 R_{sc}$$
$$W = \alpha A(\Delta T)$$

C is the thermal capacitance of the superconductor or shunt. T is the temperature of the superconductor or shunt. I is current. α is the heat transfer coefficient to the coolant (set to 5×10^3 W/m^{2}K in the model

(Ref. 178)). ΔT is the temperature difference between the superconductor or shunt and the coolant. A is the surface area of the contact between the SFCL and the coolant.

The same system was simulated using the state-space model that was simulated with the SimPowerSystems model. The load current and voltage are shown in Figure 170 and Figure 171. The SFCL resistance and temperature are shown in Figure 172 and Figure 173. The results obtained by the state-space model are similar to those found using the SimPowerSystems model. The largest discrepancy is the SFCL temperature calculation. Two different models were used to calculate temperature. Further study is needed to determine the accuracy of each temperature model. The difference in the temperatures causes a slight difference in the calculated resistance of the SFCL (Ref. 179). This led to a small difference in the calculated fault current and load voltage.

7.3 Solid-State Circuit Breaker

Solid-state circuit breakers use modern high-power semiconductors rather than electromechanical devices to protect a system from overload or a short circuit. Solid-state circuit breakers can react in a few microseconds versus a mechanical device that can take at least 100 ms to clear. With the fast response, the magnitude of the fault current will be greatly reduced and will help prevent damage to equipment in the system and prevent superconducting elements in the turboelectric system from quenching (Ref. 180).

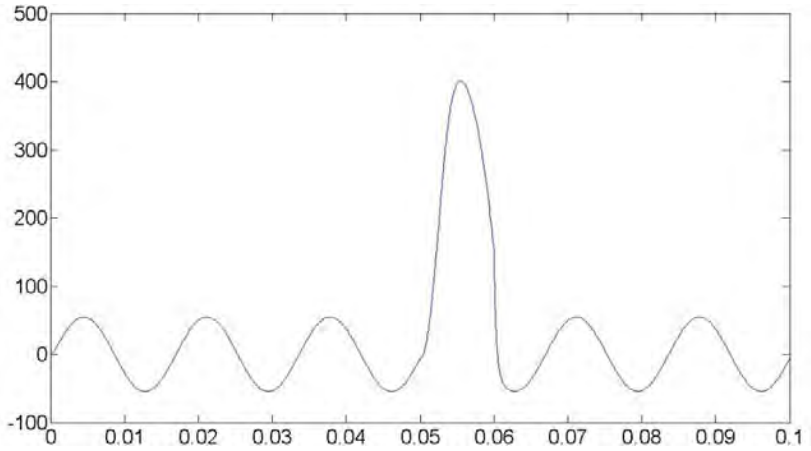


Figure 170.—Fault Current (A)—State-space Model.

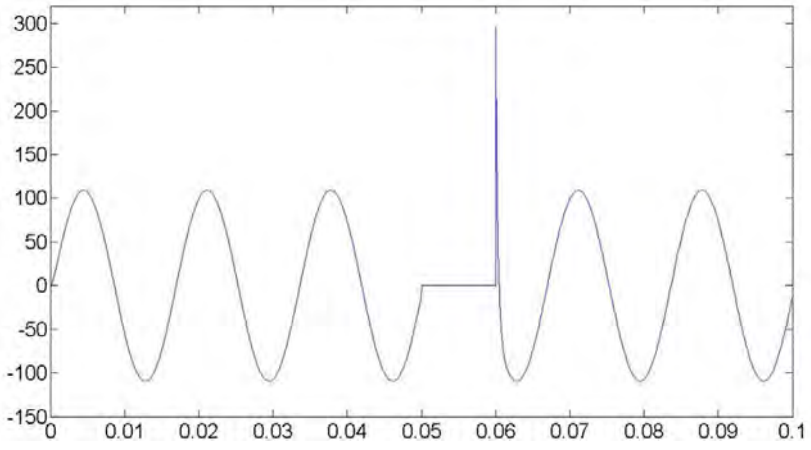


Figure 171.—Load Voltage (V)—State-Space Model.

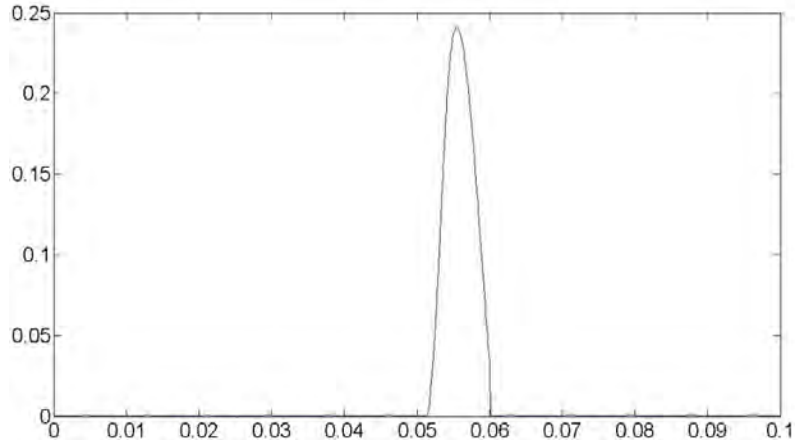


Figure 172.—SFCL Resistance (Ω)—State-Space Model.

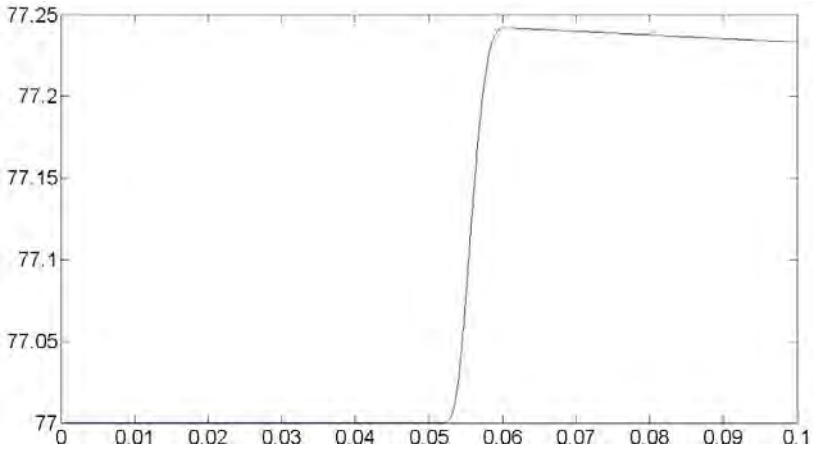


Figure 173.—SFCL Temperature (K)—State-Space Model.

7.3.1 SSCB Modeling Overview

The circuit breaker topology that was modeled is shown in Figure 174. The IGBTs are on when the system is under normal operating conditions. When an over-current is sensed, the circuit breaker will be tripped and the IGBTs will be turned off.

Determining when to turn on and off the IGBTs is critical to the effectiveness of the SSCB. The protection scheme needs to be sensitive enough to quickly trip the circuit breaker when a fault occurs so that the fault current is minimized. However, if the control is overly sensitive, the circuit breaker may trip during a temporary over-current condition.

The most widely used control scheme for SSCB is inverse-time over-current protection. This scheme senses the ratio of the actual current to a set tripping current. When an over-current is detected, the breaker will be tripped after a given amount of delay is determined using inverse-time curves. The inverse time curve can be calculated using the following equation (Ref. 179):

$$t_{\text{trip}} = \left(\frac{A}{\left(\frac{I}{I_{\text{tripping}}} \right)^{P-1}} + B \right) \frac{14 * TD - 5}{9}$$

I is the sensed current. $I_{tripping}$ is the tripping current. A, B, P, and TD (time dial) are all shaping parameters. Their settings are determined based upon how sensitive the designer wants the control scheme to be. A variety of curve options exist. A list is provided in Table 33, and Figure 175 shows the curves with a time dial setting of 0.5. (The lower the time dial setting, the faster the circuit breaker will be tripped.)

A timer is started at the instant that an over-current is sensed. When the amount of time counted by the timer exceeds the calculated t_{trip} time, the breaker will be tripped. At any point during this period, if the sensed current falls to less than $I_{tripping}$, the timer can be reset until an over-current is encountered again.

TABLE 33.—INVERSE-TIME CURVES (REF. 179)

Inverse-time curve	*A*	*B*	*P*
Normal inverse	0.0086	0.0185	0.02
Very inverse	2.855	0.0712	2
Extremely inverse	6.407	0.025	2
Short time inverse	0.00172	0.0037	0.02
Short time extremely inverse	1.281	0.005	2

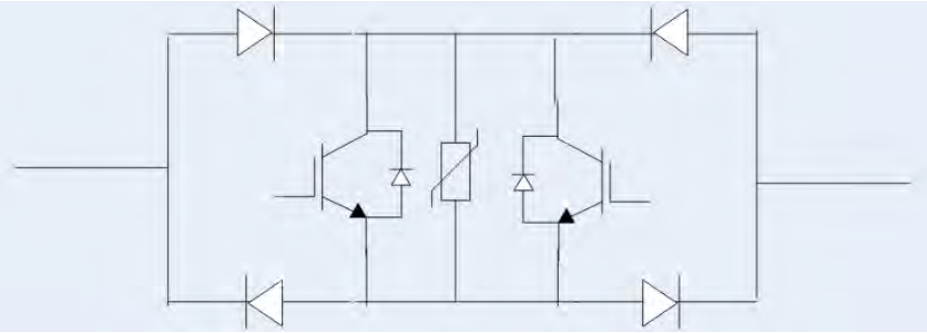


Figure 174.—SSCB Circuit Diagram.

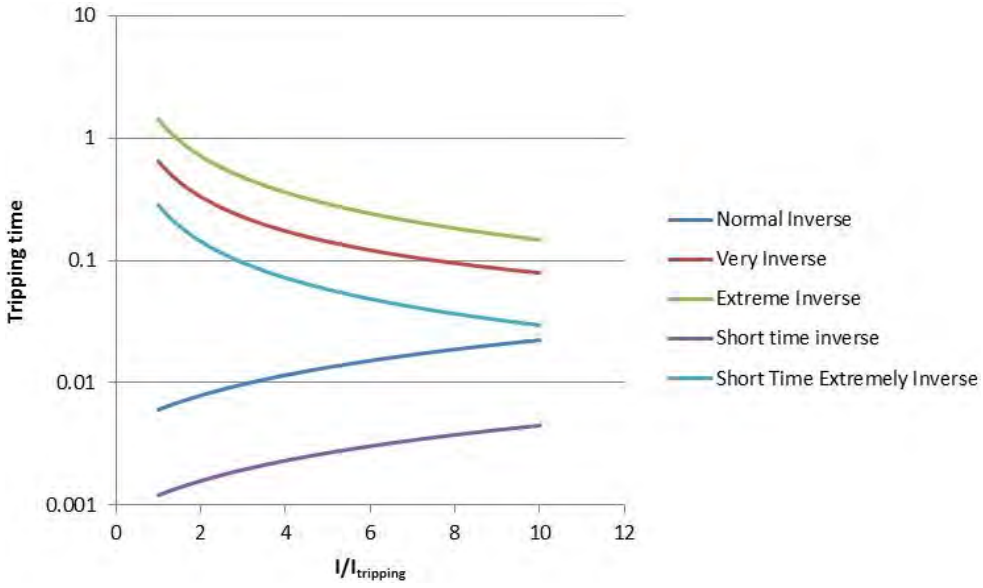


Figure 175.—Inverse-Time Curves with Time Dial Setting of 0.5.

7.3.2 SSCB SimPowerSystems Model

A simple DC circuit was used to simulate the SSCB. The model is shown in Figure 176. The system consists of an ideal DC voltage source, a line resistance and inductance, SSCB, line-to-line fault, and a resistive load. To create the SSCB, the SimPowerSystems models for a diode, IGBT, and surge arrestor were used. (The design of the SSCB uses a varistor, but the SimPowerSystems surge arrestor model can be used to simulate a varistor given the correct settings.) The IGBTs are controlled using the inverse-time over-current protection scheme that was described in the previous section.

The model allows the user to set a number of parameters. The input variables are shown in Table 34 along with their settings for an example simulation that was performed. The results of the simulation are shown in Figure 177 to Figure 180. First the system was simulated without the circuit breaker. Figure 178 and Figure 179 show the response of the system under this condition. Figure 178 shows that the fault current reaches nearly 6000 A. Next, the system was simulated with the circuit breaker in place. Figure 179 shows the fault current response, and Figure 180 shows the voltage across the load. With the use of the SSCB, the fault current is limited to about 1/3 of the fault current when no protection is used. The responses show that there is a slight delay between the start of the fault at 0.2 s and the activation of the circuit breaker. This delay is about 0.051 s. The size of this delay can be altered by changing the inverse-time over-current protection parameters.

TABLE 34.—SSCB MODEL PARAMETERS

	Parameter	Setting for example simulation
System Parameters	Source voltage, V	6000
	Line resistance, Ω	1
	Line inductance, H	0.02
	Load resistance, Ω	6
	Fault start time, s	0.2
	Fault end time, s	0.3
Overcurrent Protection Parameters	Inverse-time curve	Short inverse time
	Time dial	0.3
	Tripping current, A	2000
IGBT Parameters (Ref. 181)	On resistance, Ω	0.000625
	On inductance, H	0
	Forward voltage, V	1
	Current 10% fall time, s	40×10^{-9}
	Current tail time, s	45×10^{-9}
	Initial current, S	0
	Snubber resistance, Ω	1×10^{5}
	Snubber capacitance, °F	inf
Diode Parameters (Refs. 182 and 183)	On resistance, Ω	0.001
	On inductance, H	0
	Forward voltage, V	0.85
	Initial current, A	0
	Snubber resistance, Ω	1×10^{5}
	Snubber capacitance, F	250×10^{-9}

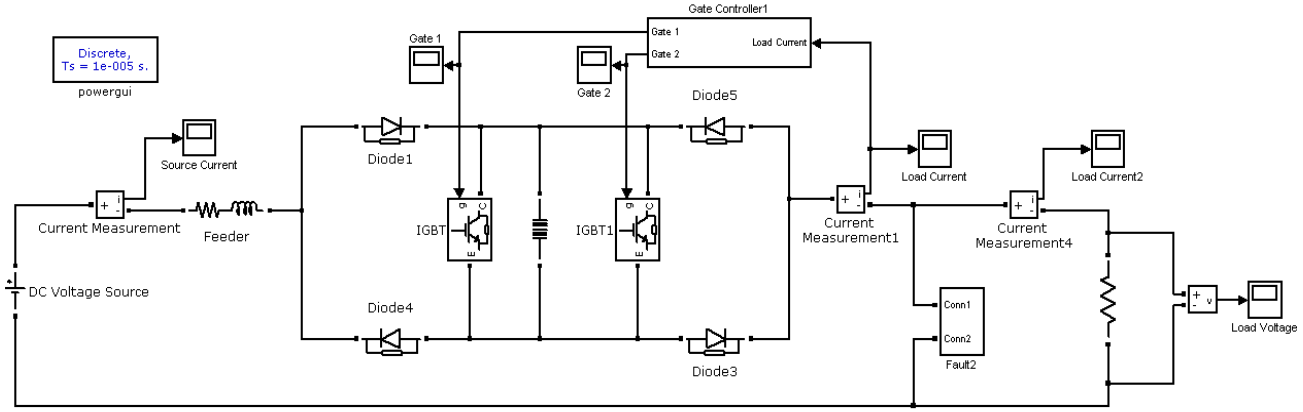


Figure 176.—SSCB Model.

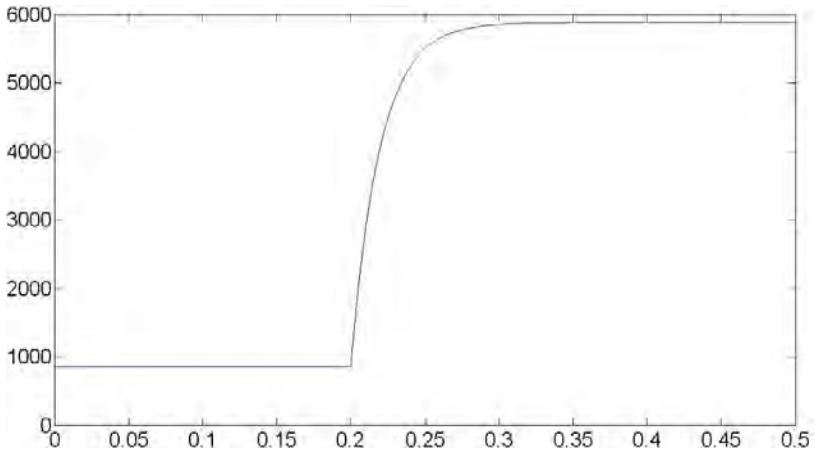


Figure 177.—Example System Fault Current without Protection (A).

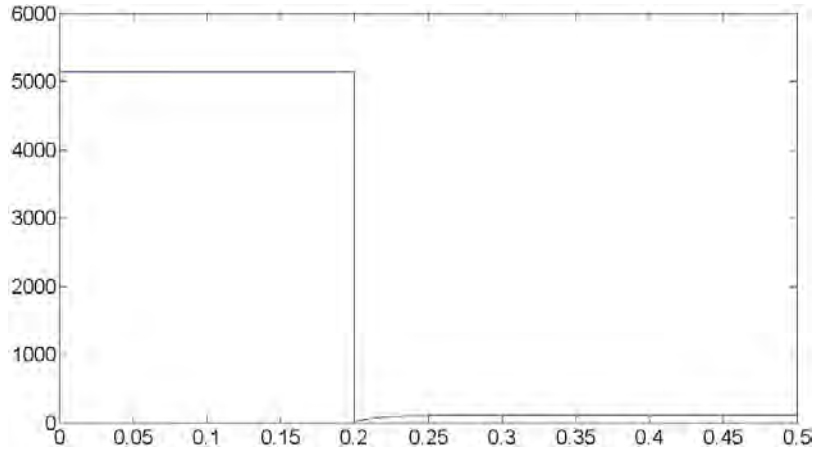


Figure 178.—Example System Load Voltage without Protection (V).

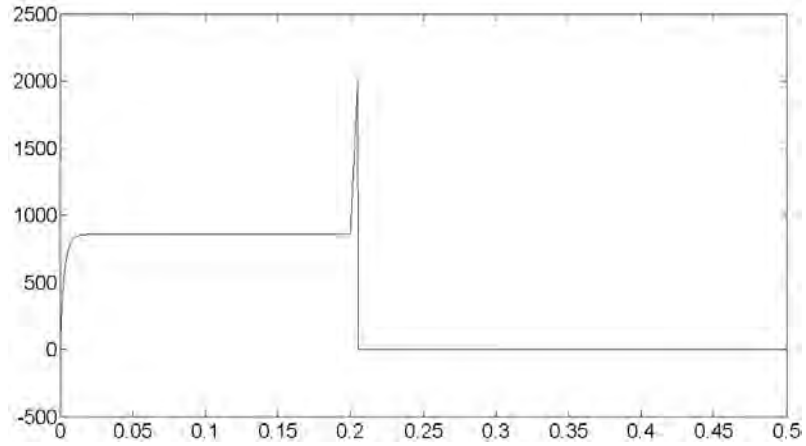


Figure 179.—Fault Current with SSCB.

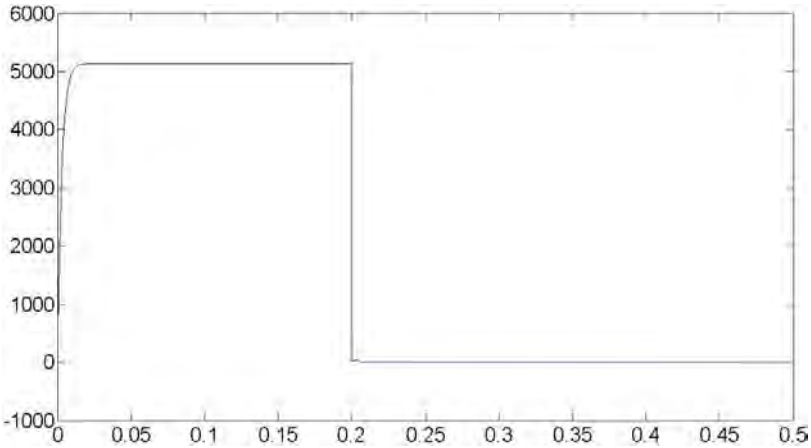


Figure 180.—Load Voltage with SSCB (V).

7.4 Energy Storage Model (SMES)

The energy storage device selected for this system is superconducting magnetic energy storage. The topology of the device is shown in Figure 181.

Figure 181 shows that the SMES operates in one of three states: charging, steady-state, and discharging. The state of the SMES can be changed by switching the IGBTs in the H-bridge. The SMES will charge until the current flow through the inductor reaches steady-state. Then the SMES will switch to the steady-state mode of operation until backup power is required. Figure 182 shows the system used to simulate the SMES. Table 35 lists the settings in the model. Figure 183 shows the charging of SMES. The figure shows that the SMES steady-state current is about 10 kA and it takes around 400 s to reach steady-state.

After the SMES is charged, if a failure occurs in the system and backup power is needed, the SMES will switch to the discharge state. Figure 184 shows voltage across the load after a fault at 5 s. At 5.2 s, the SMES becomes the source for the load. Figure 185 shows the current flow through the load.

Figure 184 shows that the SMES can create an over-voltage. The H-bridge can also be used to regulate the output voltage of the SMES. This is accomplished by rapidly switching between the discharge and steady-state modes of operation. A controller senses the output voltage of the SMES. If the voltage is reaching an unacceptable level, then the controller will switch the SMES to steady-state. The controller will monitor the voltage, and if it drops below the target voltage (within a set tolerance), then the controller will switch the SMES back to the discharge mode. The fast switching can create noise in

the output of the SMES. The amount of noise can be mitigated by increasing the output capacitance of the SMES. A small inductor can also be added to the output of the SMES to smooth current flow. Figure 186 and Figure 187 show the load voltage and current, respectively if voltage control is implemented.

TABLE 35.—SMES MODEL PARAMETERS

Parameter	Setting
Source voltage	1000 V
Source resistance	1 Ω
Source inductance	0.002 H
Load resistance	8.33 Ω
SMES inductance	64 H
SMES capacitance	1.3×10^{-3} °F

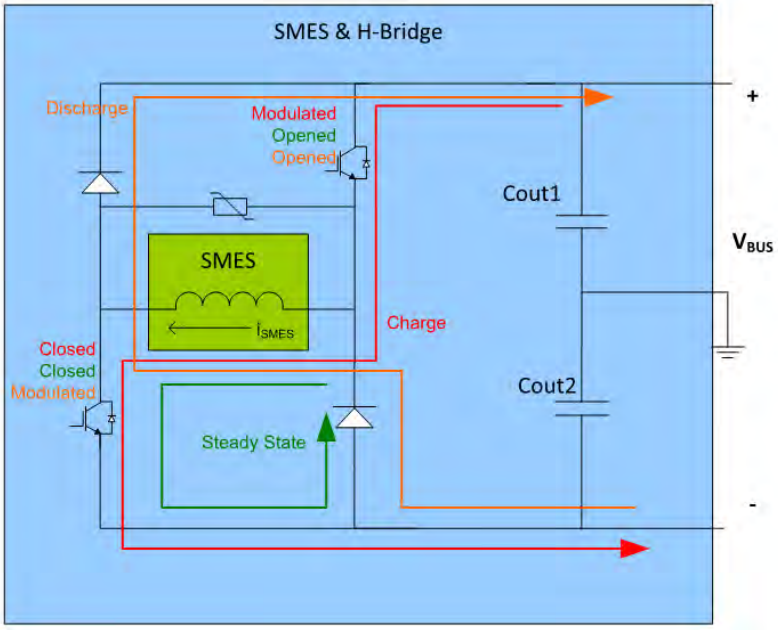


Figure 181.—SMES circuit and states.

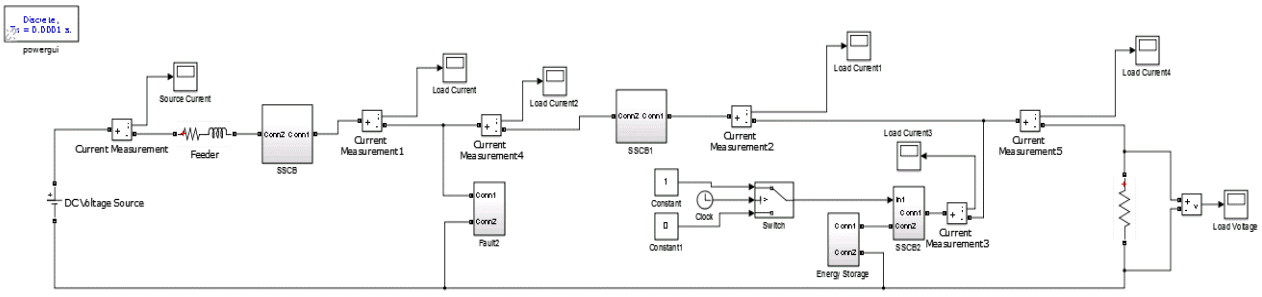


Figure 182.—SMES Model.

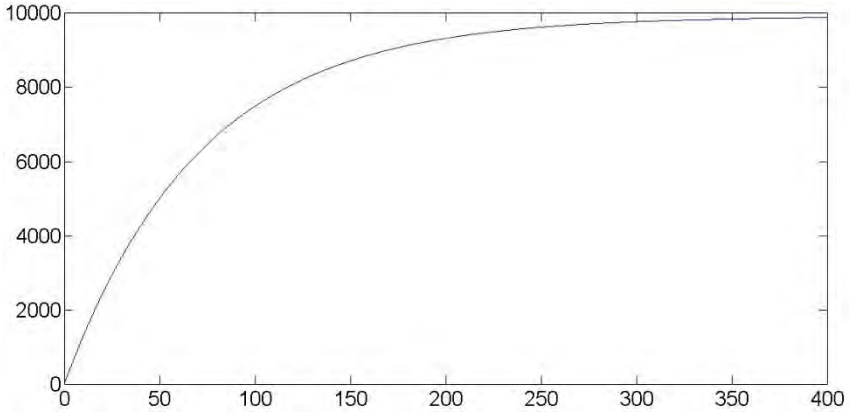


Figure 183.—SMES Voltage during Charging.

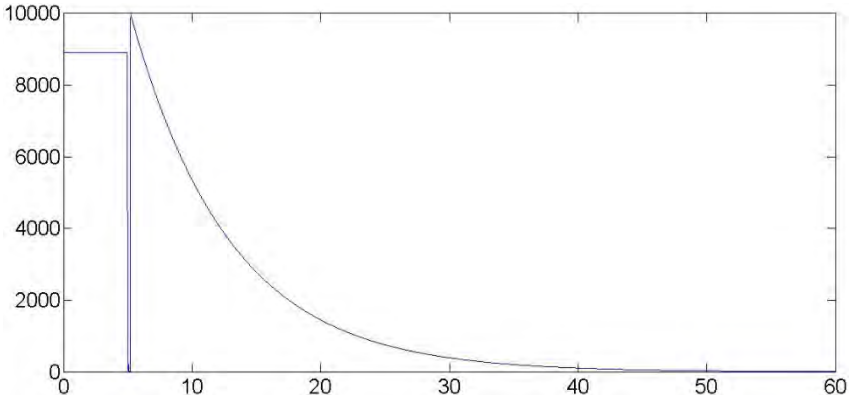


Figure 184.—SMES Voltage during Discharge.

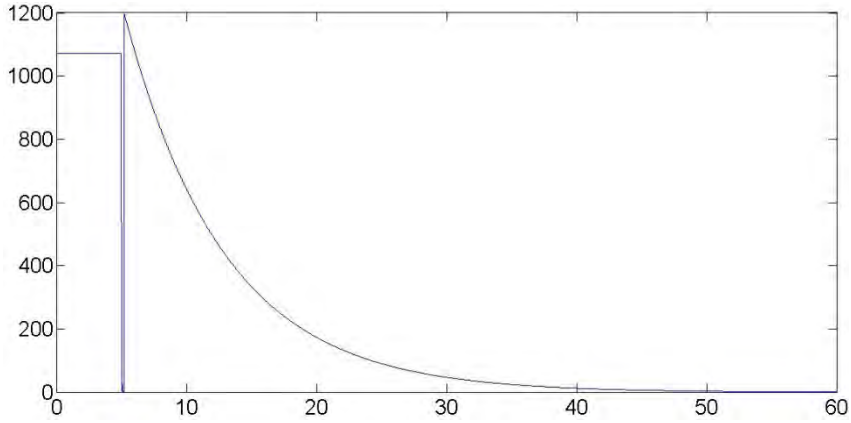


Figure 185.—SMES Current during Discharge.

7.5 Power Converter Models

The types of power converters needed for the TePD system are inverters and rectifiers. Two topologies were considered for each type of power converter—a current source topology and voltage source topology.

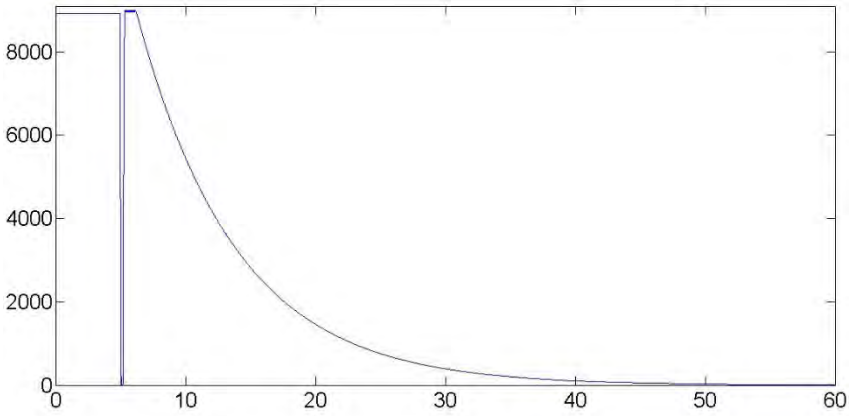


Figure 186.—SMES Voltage during Discharge with Voltage Control.

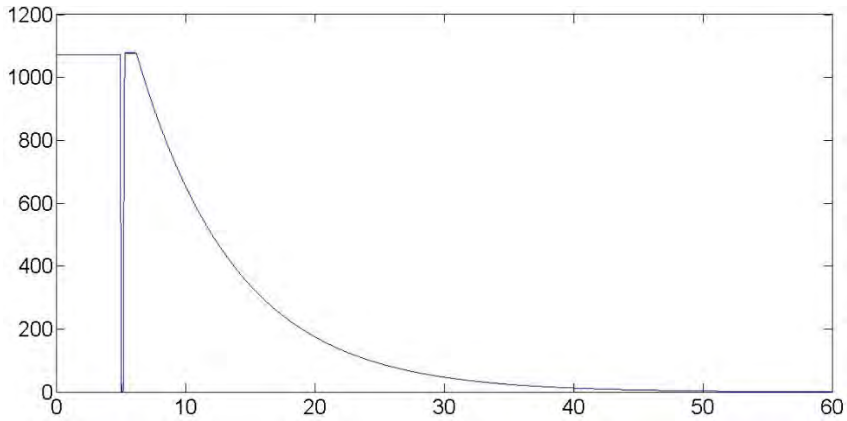


Figure 187.—SMES Current during Discharge with Voltage Control.

7.5.1 Rectifiers

Rectifiers are required in the system to covert AC power from the generators to DC power for the buses.

7.5.1.1 Current Source Rectifier

The first topology examined was a modular current source converter, which is shown in Figure 188.

The current source rectifier is designed for overvoltage protection. Also, the modular design allows modules to be added or deleted based upon the power requirements of the rectifier. However, this rectifier posed a number of challenges. First of all, limited information about the control of this rectifier is available. The control scheme is complex due to the number of switches and modules. Each module has to be individually controlled such that the output of the rectifier achieves the desired voltage. To simplify the process the module design shown in Figure 189 was used for the analysis (Ref. 184).

The control scheme used in the model was adapted from Solas (Ref. 184). The control scheme is PWM based. The PWM control consists of a control signal and triangular signal. A triangular signal is generated for each module. For each arm of the rectifier, four triangular signals are generated.

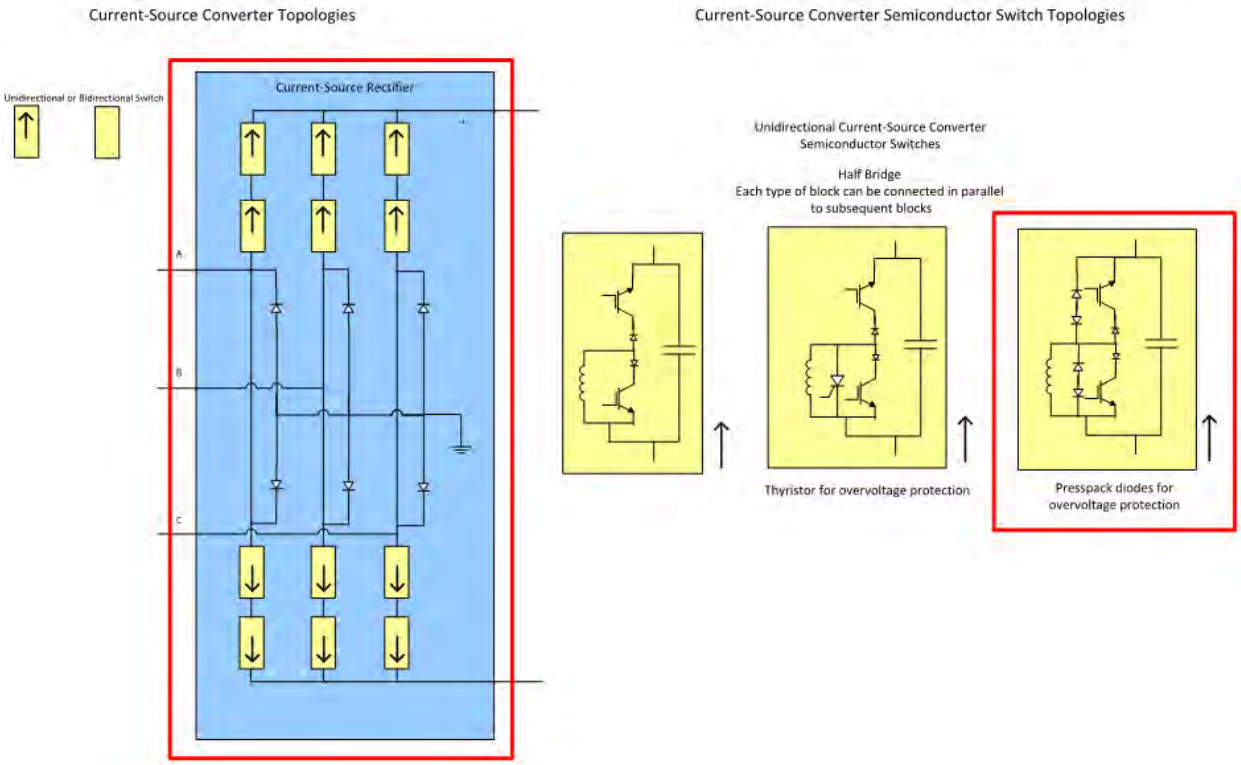


Figure 188.—Current Source Rectifier Topology.

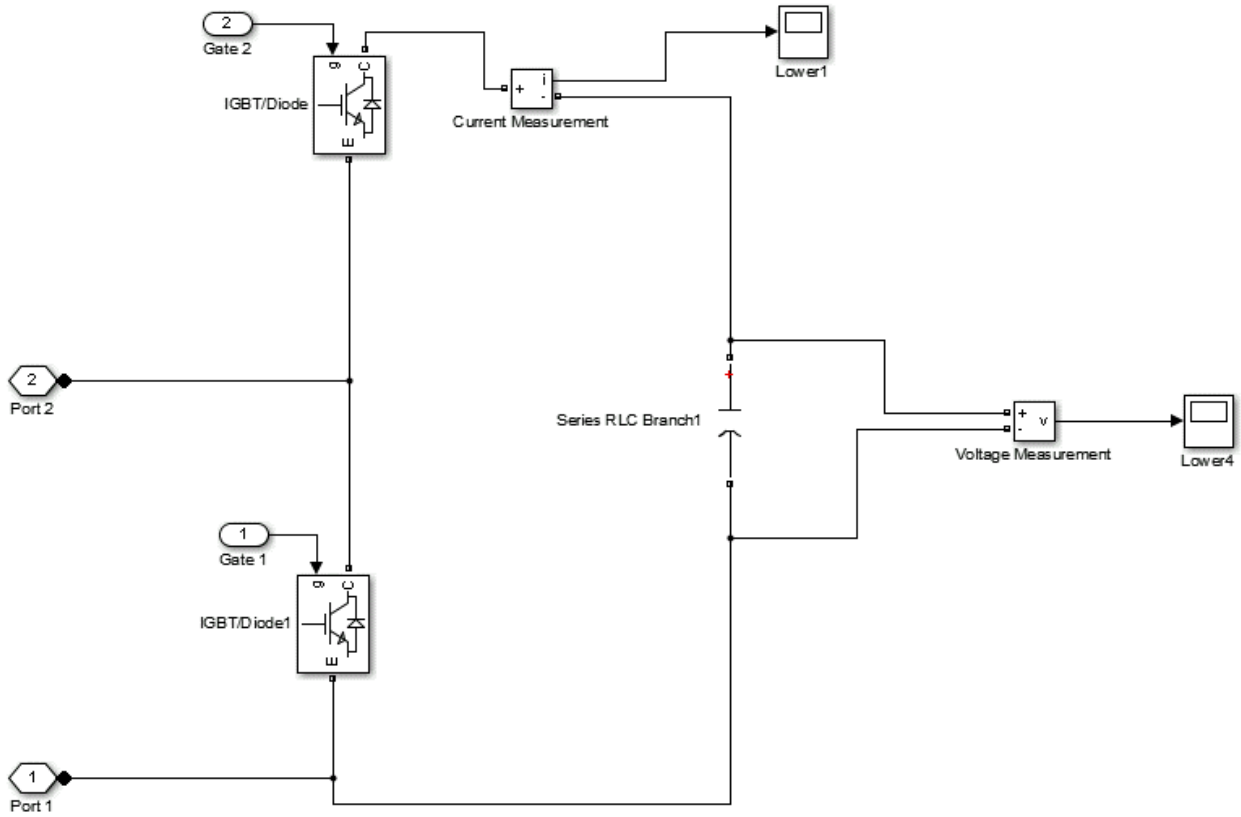


Figure 189.—Current Source Rectifier Module.

The phase of each wave is 90° apart. The phase shift between signals for each arm is 120°.

The reference signal is generated using the algorithm shown in Figure 190. The reference signal attempts to drive the output of the rectifier to the reference signal specified.

Once the triangular and reference signals are generated, the algorithm shown in Figure 191 is used to determine the switching states of each module. A switching state of 1 for the upper modules means that the lower IGBT in the module is conducting and the upper is closed. A switching state of 0 for the upper modules means that the upper IGBT is conducting and the lower IGBT is closed. The opposite switching state occurs for the lower modules (i.e., a switching state of 1 means that the upper IGBT is conducting and the lower is not).

The model used to test the rectifier designs is shown in Figure 192. The model was run using the parameters listed in Table 36. The output current and voltage are shown in Figure 193 and Figure 194.

TABLE 36.—CURRENT SOURCE RECTIFIER MODEL PARAMETERS

Parameter	Setting
Source current	75000 A
Source frequency	400 Hz
Source resistance	1 Ω
Source inductance	0.001 H
Rectifier inductance (per inductor)	0.017 H
Rectifier capacitance (per module)	0.0034 F
Rectifier output capacitance	0.34 F
Switching frequency	18000 Hz
Kp	0.5
Kp'	1
Reference voltage	4500 V
Load resistance	0.32 Ω

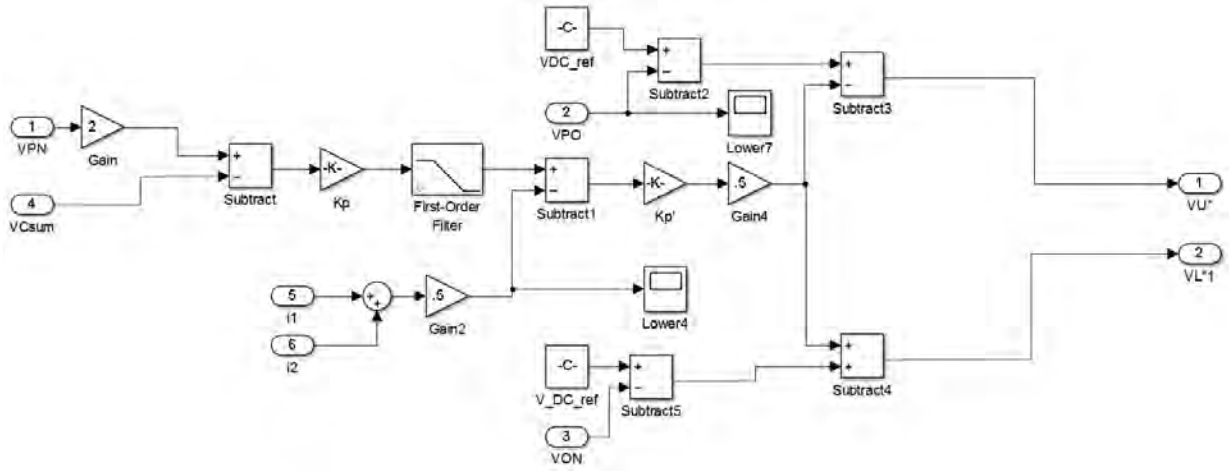


Figure 190.—Reference Signal Calculation.

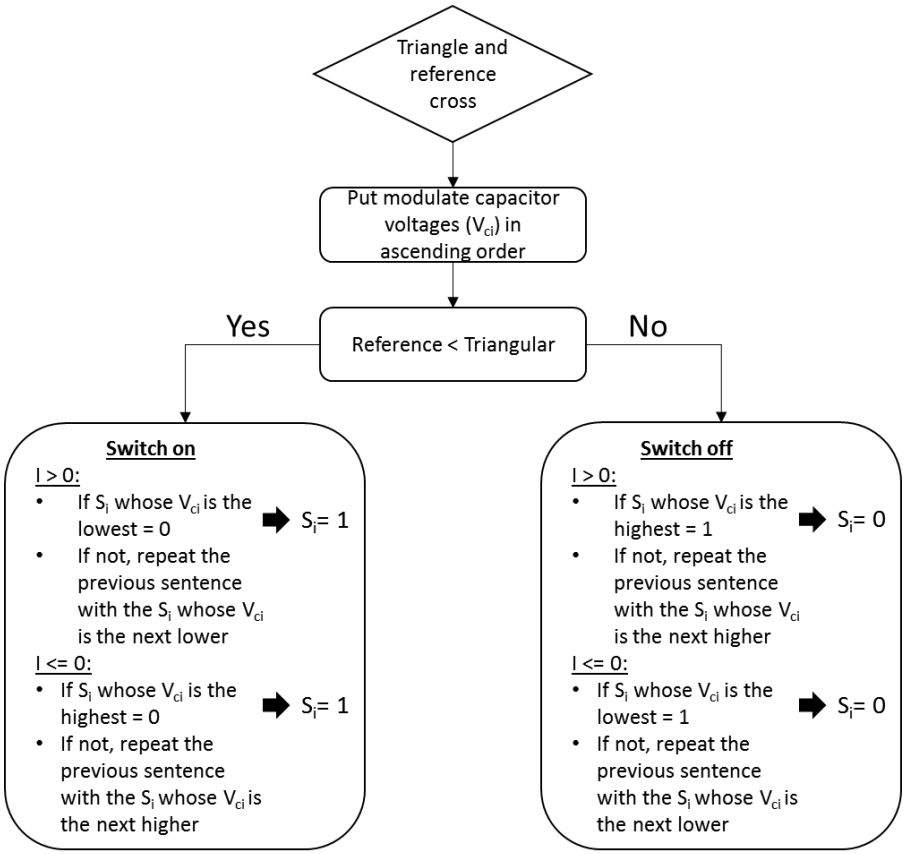


Figure 191.—Current Source Rectifier Switching Algorithm.

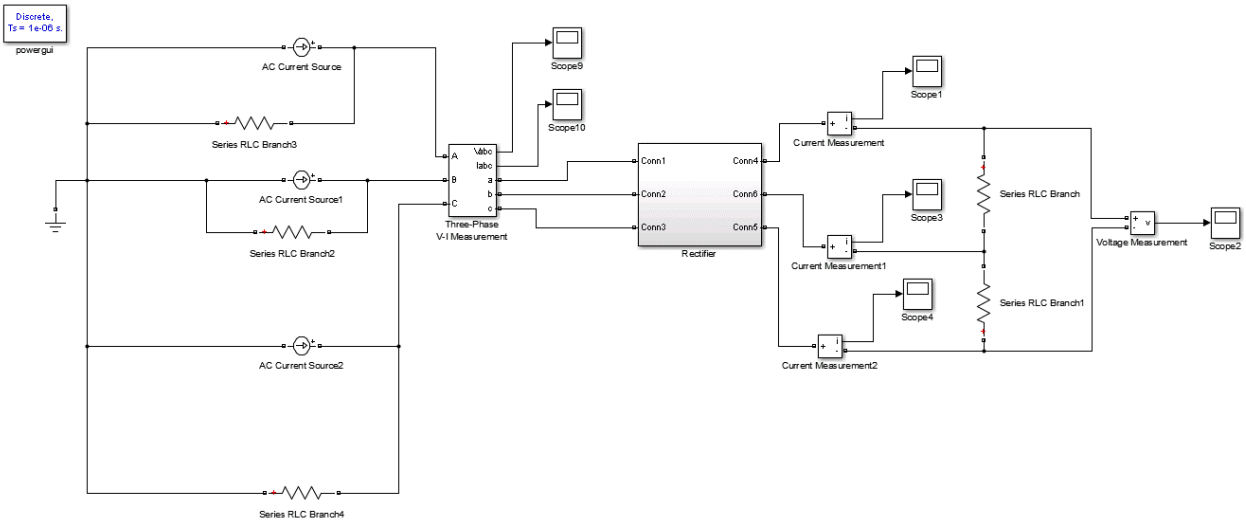


Figure 192.—Current Source Rectifier Model.

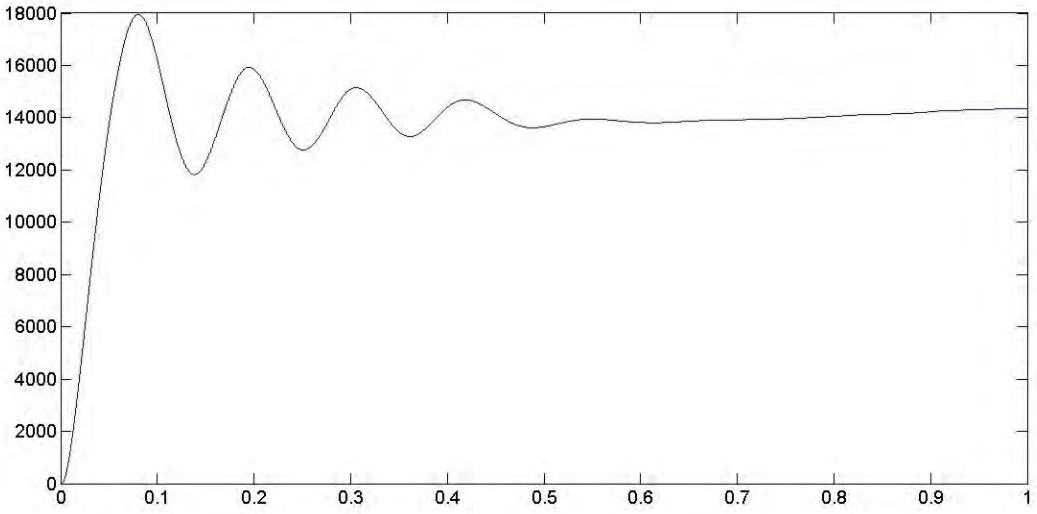


Figure 193.—Current Source Rectifier Output Current.

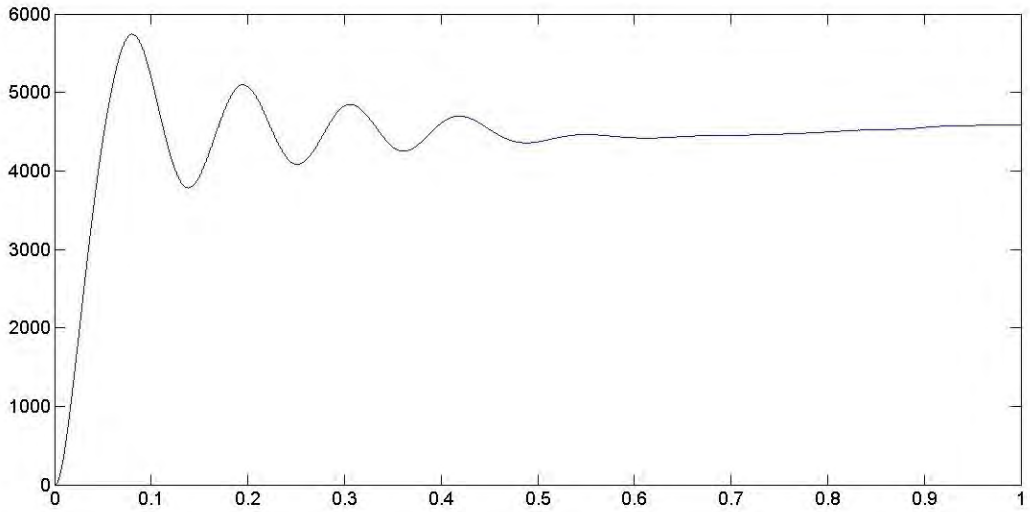


Figure 194.—Current Source Rectifier Output Voltage.

A second problem with this type of rectifier is a high amount of losses. The input current and voltage (generated by a controlled current source) are shown in Figure 195 and Figure 196. Figure 195 demonstrates that the input voltage must be extremely high in order to meet the target output voltage of the rectifier. The high number of switches in this topology leads to a high amount of switching losses.

7.5.1.2 Voltage Source Rectifier

Due to the control and efficiency problems created by the current source rectifier, a voltage oriented controlled, voltage-source rectifier was considered. The voltage source topology is shown in Figure 197 (Ref. 185).

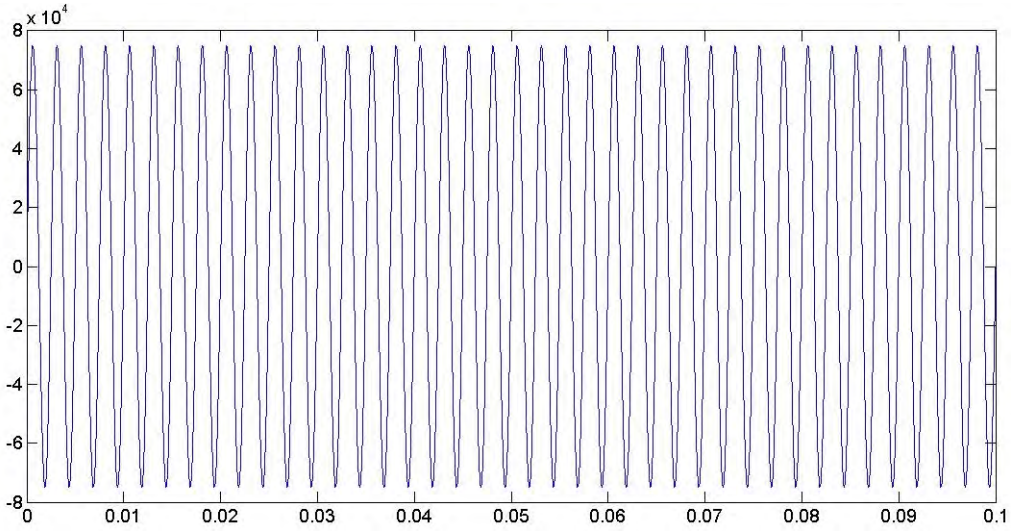


Figure 195.—Current Source Rectifier Input Current.

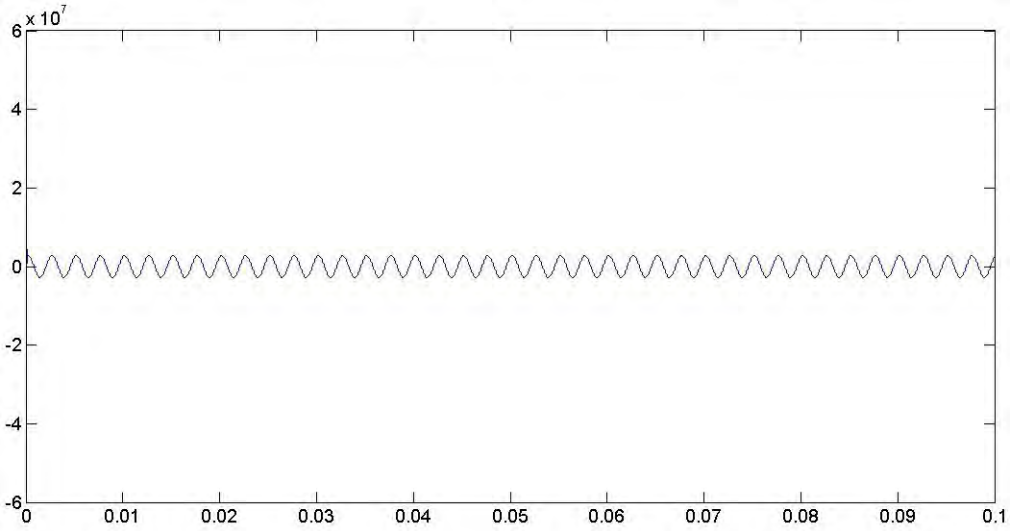


Figure 196.—Current Source Rectifier Input Voltage.

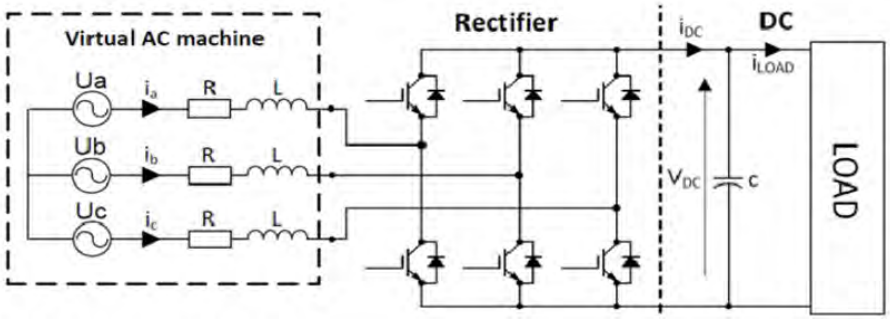


Figure 197.—Voltage Source Rectifier Topology.

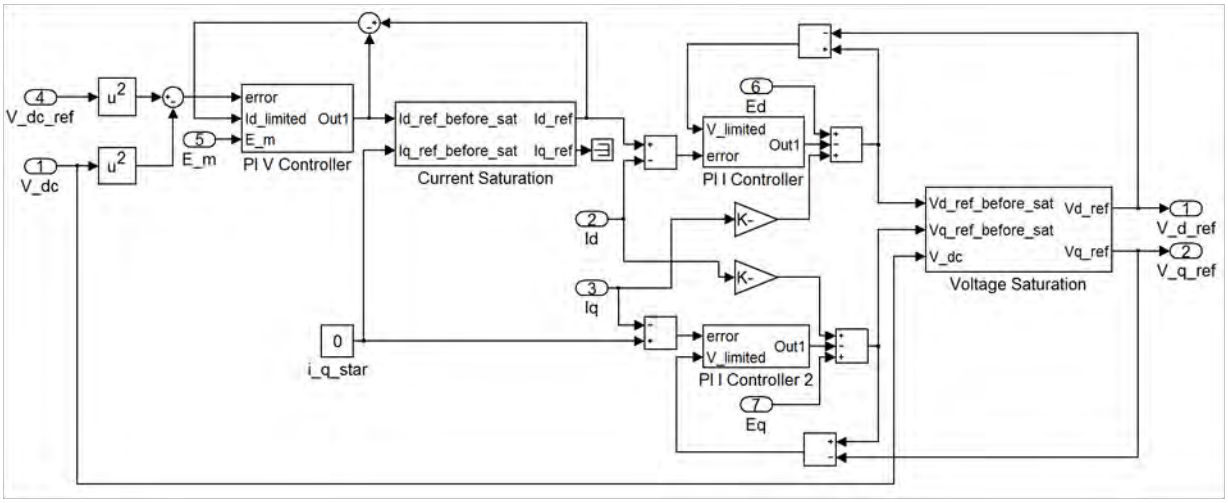


Figure 198.—VOC Control.

The control scheme for the voltage source rectifier is much less complex than the current source rectifier. The basic control scheme, called voltage oriented control (VOC), is shown in Figure 198 (Ref. 186). The controller contains an outer PI voltage control loop with an inner current control loop. The voltage control attempts to regulate the output voltage of the rectifier to the specified value. The current loop strives to drive the current to a state of active power and minimizes the reactive component. The control scheme of this converter can help control bus voltage in a failure scenario. Also, the reduced number of switches greatly reduces the switching losses in the converter. However, scaling this converter is more difficult than the current source modular design.

The VOC scheme selected for this rectifier uses the stationary *dq* reference frame. In order to use this reference frame, a coordinate transformation is required. The equations used to transform the coordinates are (Ref. 187):

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix}$$

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix}$$

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix}$$

Where θ is the voltage angle which is found using a phase locked loop (PLL). A PLL is a feedback controller which "locks" two waveforms to the same frequency. This controller also has the ability to determine the frequency of a wave and find the phase between waveforms.

Once the coordinate transformation has taken place, the voltage and current signals are sent to the decoupled controller. Figure 177 shows the decoupled controller. As shown in the diagram, three PI controllers are required, two of which are current controllers. The proportional (k_{ip}) and integral (k_{ii}) coefficients of the current PI controllers are:

$$k_{ip} < \frac{2\pi F_s}{10} L;\ k_{ii} < \frac{2\pi F_s}{10} R$$

Where F_s is the PWM switching frequency. The proportional (k_{vp}) and integral (k_{vi}) coefficients for the PI voltage controller are:

$$k_{vp} < \frac{2\pi F_s C}{30 E_m};\ k_{vi} = 0.001$$

The integral portion of the PI voltage controller has almost no effect on the outcome of the model. This is why a small coefficient is arbitrarily chosen. The proportional coefficient for the voltage controller has a very strong influence on the performance of the controller. If the value of the coefficient is too large, the model will not be able to converge on a solution or will not be able to reach the target voltage. If the value selected is too small, a large amount of harmonic distortion will be present in the bus voltage.

In some cases, there may be a large step in the reference voltage. This large step will cause the controller to demand a higher voltage than the rectifier can supply; therefore, a saturation block needs be added to the current controller to ensure that the reference voltage does not exceed the maximum voltage output of the rectifier. This issue can also arise for the voltage controller, so a saturation block will also be used in conjunction with it. Although using saturation fixes the problem of demanding too large of a voltage or current, it introduces another problem. When the voltage or current is limited, a phenomenon called integrator wind-up can occur. This causes an overshoot in the response of the PI controller and the controller error will increase. In order to correct this problem, the error input into the current controller should become

$$\bar{\varepsilon} = \varepsilon + \frac{\bar{v} - v}{k_p}$$

where $\bar{\varepsilon}$ is the limited error and $\bar{v}$ is the limited voltage. The same principle can be applied to the voltage controller.

The voltage source rectifier was tested using the model shown in Figure 199 and the parameters listed in Table 37. The input current and voltage of the rectifier are shown in Figure 200 and Figure 201. The output current and voltage is shown in Figure 202 and Figure 203. The output does contain some harmonic interference. This response can be smoothed by fine tuning the controller parameters or increasing the output capacitance.

TABLE 37.—VOLTAGE SOURCE RECTIFIER MODEL PARAMETERS

Parameter	Setting
Source voltage	70000 V
Source frequency	60 Hz
Source resistance	1 Ω
Source inductance	0.001 H
Rectifier inductance	0.0006 H
Rectifier output capacitance	0.34 F
Switching frequency	18000 Hz
α_v (PI control variable)	10000
α_i (PI control variable)	100000
Reference voltage	4500 V
Load resistance	0.32 Ω

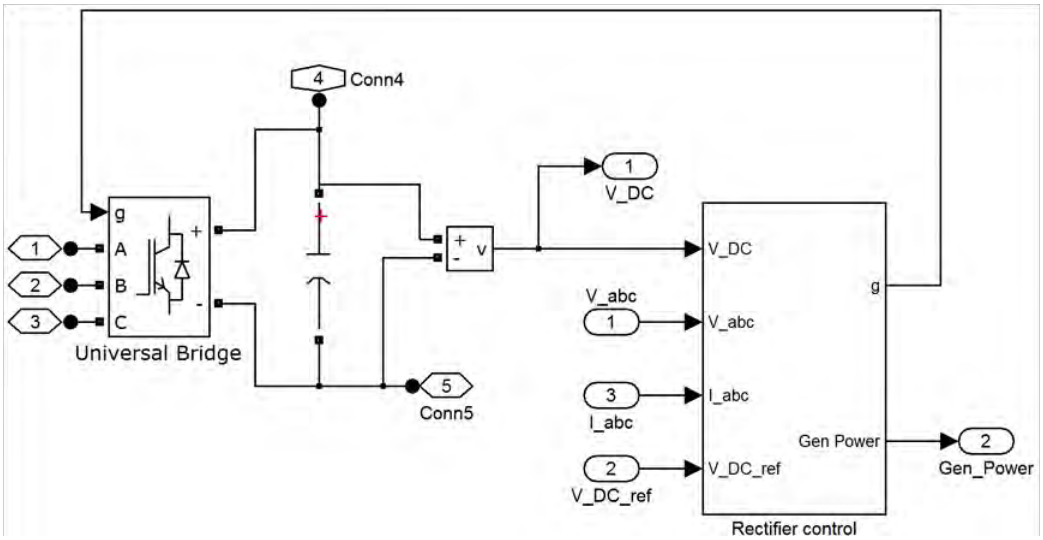


Figure 199.—Voltage Source Rectifier Model.

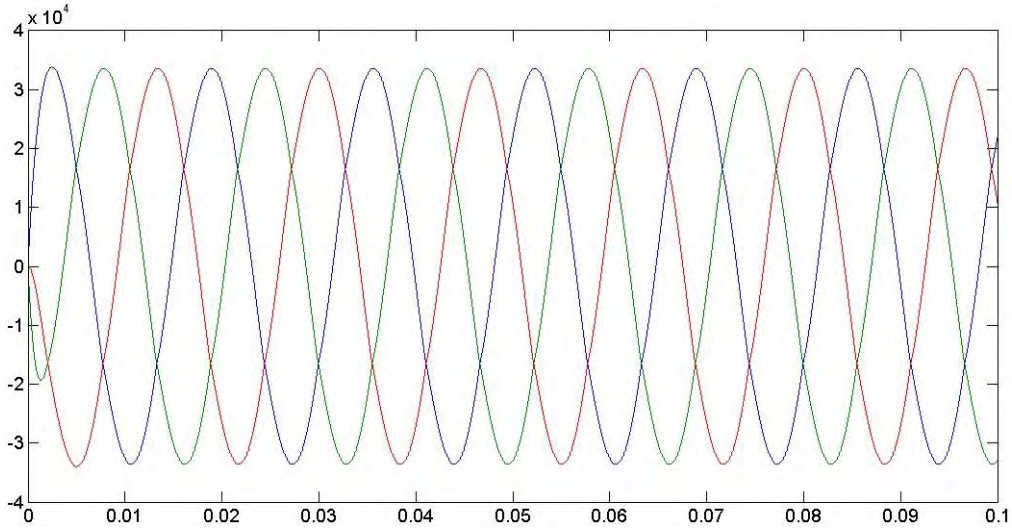


Figure 200.—Voltage Source Rectifier Input Current.

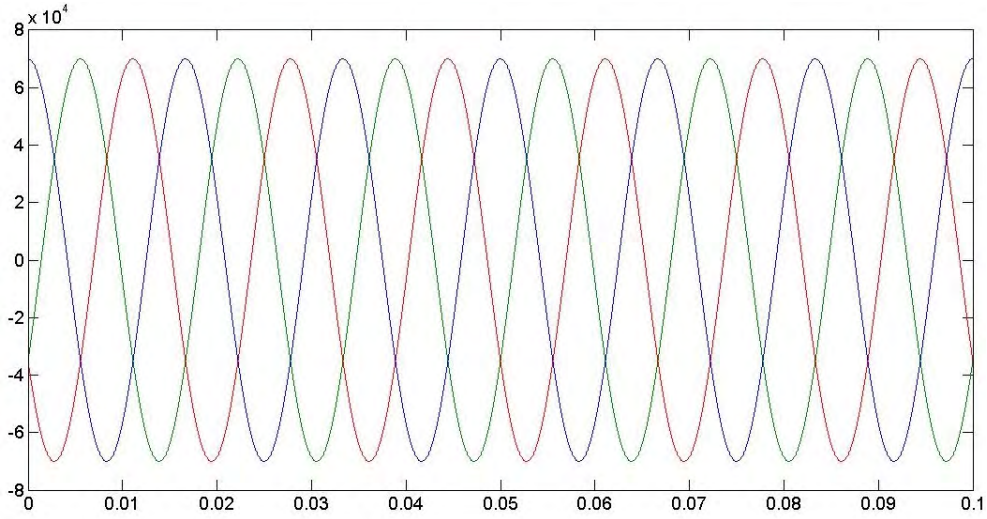


Figure 201.—Voltage Source Rectifier Input Voltage.

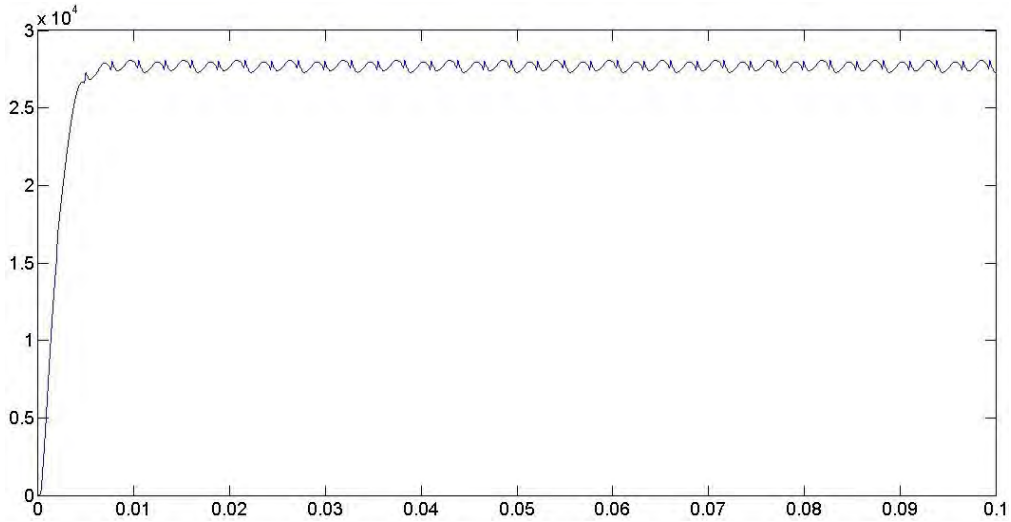


Figure 202.—Voltage Source Rectifier Output Current.

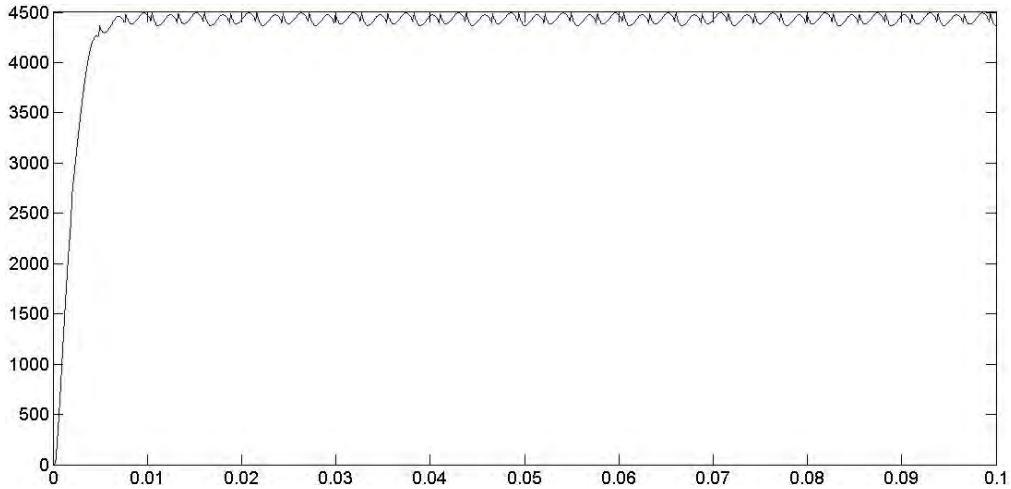


Figure 203.—Voltage Source Rectifier Output Voltage.

The voltage source rectifier was chosen for the system studies since the controller has proved to be more stable than that of the current source rectifier. Furthermore, the losses are much smaller with the voltage source design.

7.5.2 Inverters

As in the case of the rectifier, two inverter topologies were considered – current source and voltage source.

7.5.2.1 Current Source Inverter

The topology shown in Figure 204 is the current source inverter. This converter is bi-directional, meaning that it can also function as a rectifier. The pulses to control the switches are created using a PWM generator. The PWM signals are created by comparing a carrier signal to a control signal. The carrier signal is a triangle wave that is set to a high frequency. In this example, it was set to 20,000 Hz. The control signal is a sinusoidal signal at the desired output frequency. These signals are shown in Figure 205. The blue signal is the carrier signal and the green signal is the control signal. The magnitude of the carrier signal corresponds to the modulation index. The modulation index determines the amplitude of the output voltage of the inverter. The amplitude of the control signal should not be greater than that of the carrier signal to ensure that overmodulation does not occur. The pulses sent to the switches are created by comparing the carrier signal to the control signal. Based upon this comparison, the signal is set to 0 or 1. For each arm of the bridge, two signals are sent. These signals should be opposite of each other. An example of the pulses is shown in Figure 206. A set of pulses is generated for each of the three arms of the inverter.

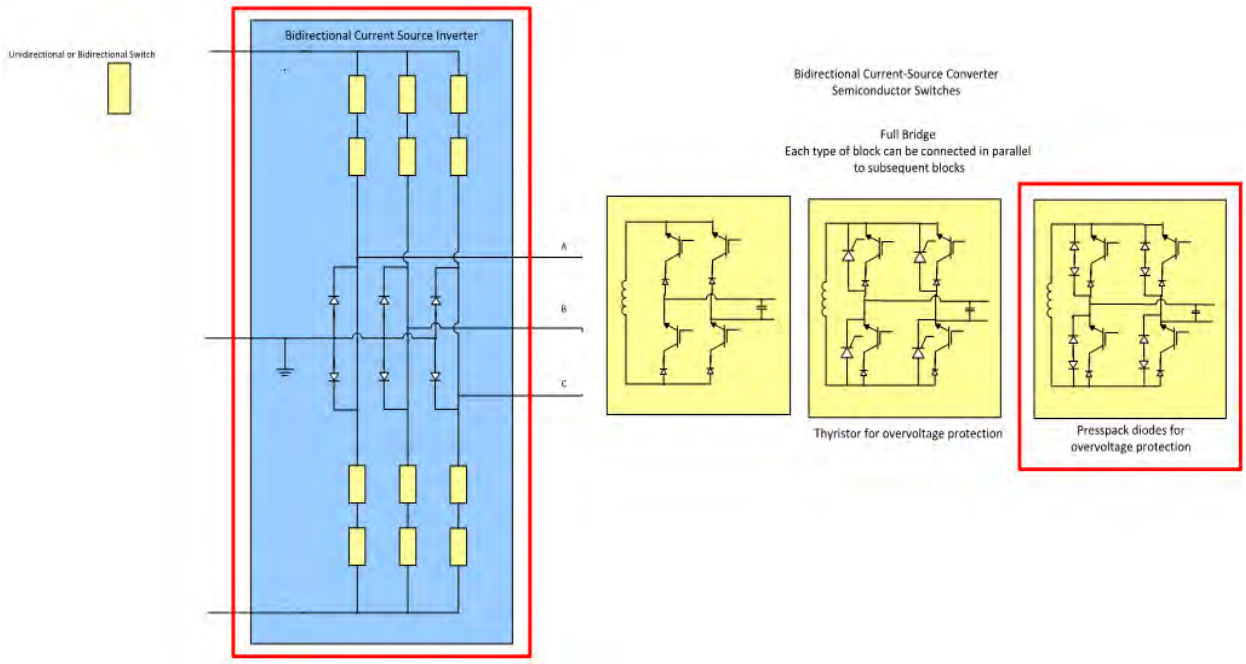


Figure 204.—Current Source Inverter Topology.

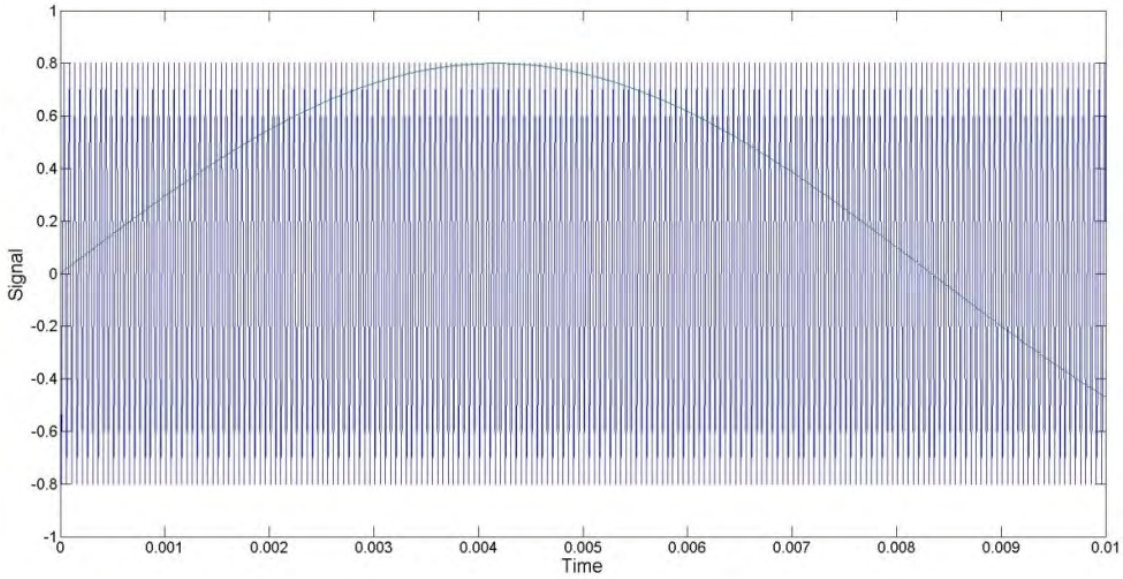


Figure 205.—PWM Control and Carrier Signals.

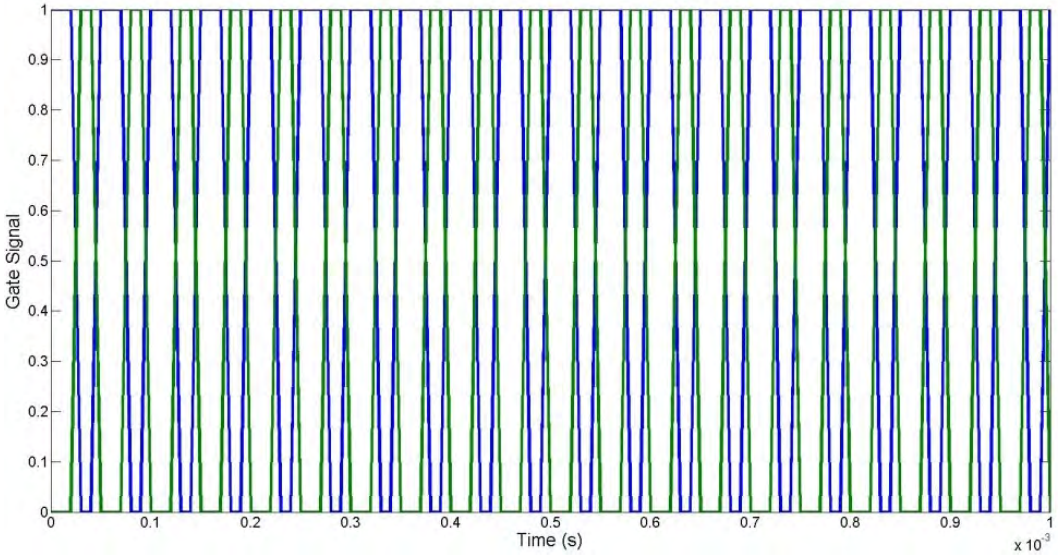


Figure 206.—PWM switching pulses.

TABLE 38.—CURRENT SOURCE INVERTER MODEL PARAMETERS

Parameter	Setting
Source current (DC)	1200 A
Switching frequency	10000 Hz
Modulation	0.8
Output frequency	400 Hz
Inverter capacitance	6×10^{-4} F
Inverter inductance	0.0012 H
Load power	5400000 W

The model was run using the parameters shown in Table 38. The input voltage to the inverter is shown in Figure 207. The output voltage and current of the inverter are shown in Figure 208 and Figure 209.

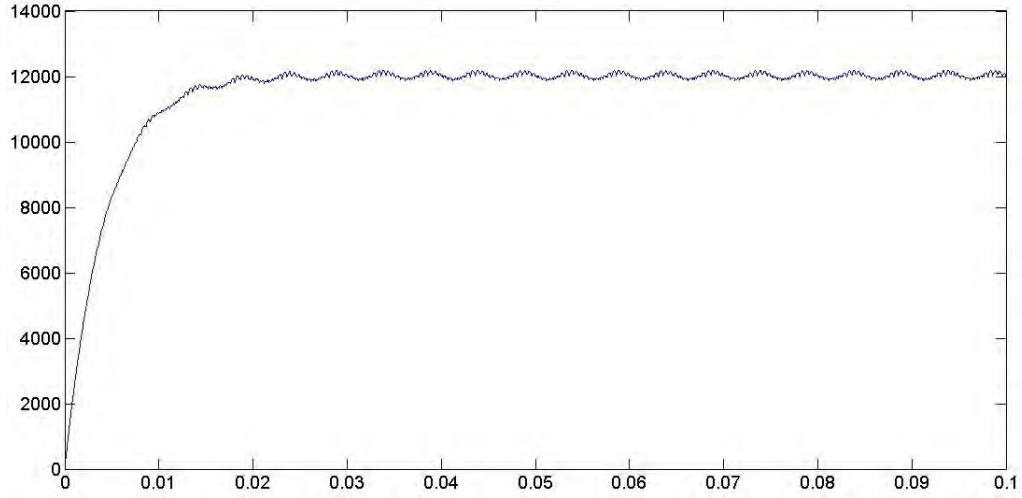


Figure 207.—Current Source Inverter Input Voltage.

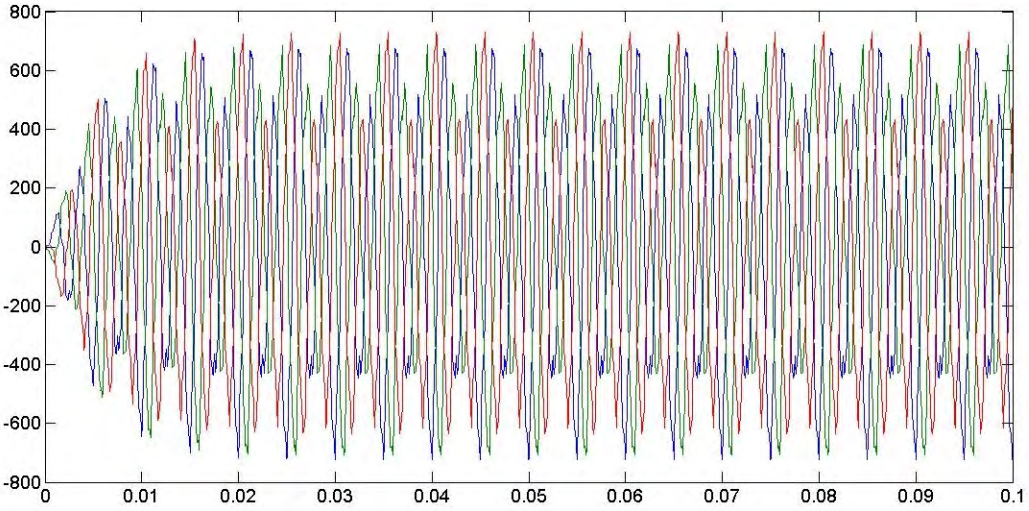


Figure 208.—Current Source Inverter Output Voltage.

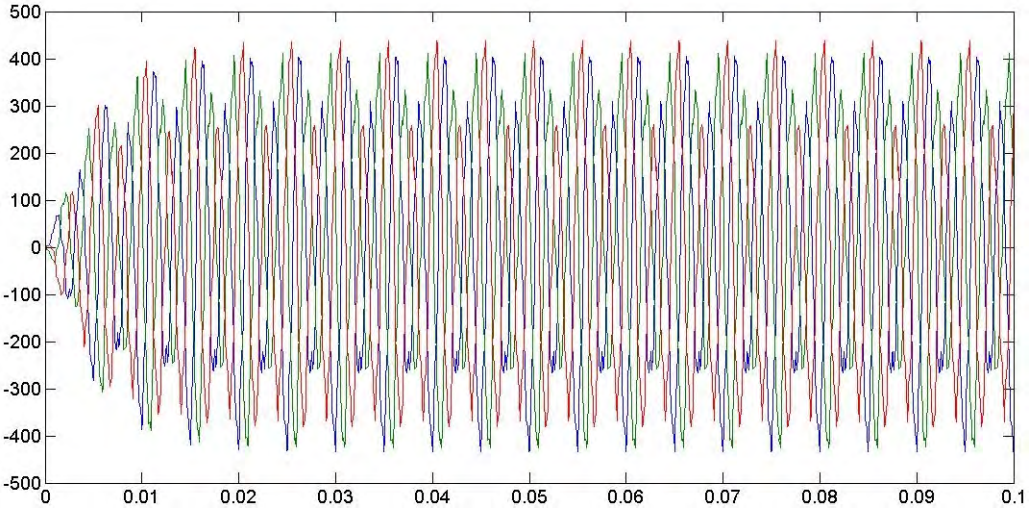


Figure 209.—Current source inverter output current.

7.5.2.2 Voltage Source Inverter

Figure 208 and Figure 209 show that the output of the current source inverter is noisy. For this reason, a voltage source inverter topology was considered. The circuit of voltage source inverter with a load is shown in Figure 210. The model is shown in Figure 211. The inverter model consists of a capacitor connected across the terminals of a three phase IGBT/diode bridge. Like the current source inverter, the voltage source inverter is PWM controlled. The model was run using the parameters listed in Table 39. The input current for the inverter is shown in Figure 212. (The current can be smoothed by using an inductor in series with the voltage source.) The output current and voltage of the inverter is shown in Figure 213 and Figure 214. The response of this inverter topology is much smoother than that of the current source inverter. For this reason, the voltage source topology was selected for the system modeling.

TABLE 39.—VOLTAGE SOURCE
INVERTER MODEL PARAMETERS

Parameter	Setting
Source voltage, V	12000
Switching frequency, Hz	10000
Modulation	0.8
Output frequency, Hz	400
Load power, W	5400000

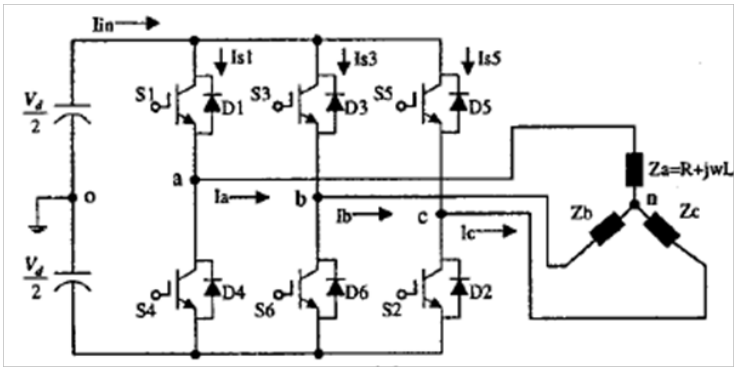


Figure 210.—Voltage Source Inverter Topology.

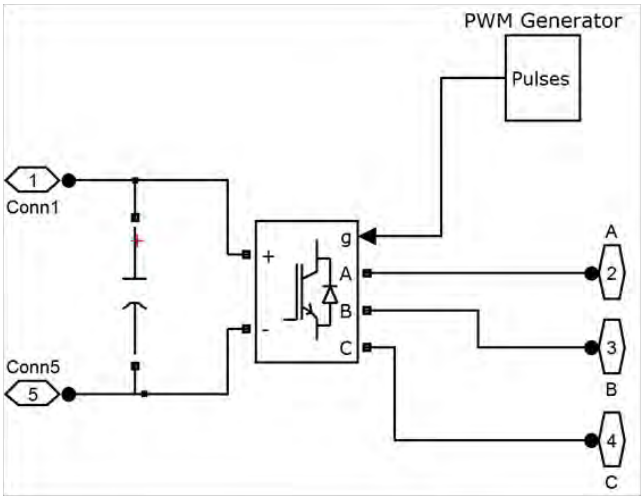


Figure 211.—Voltage Source Inverter Model.

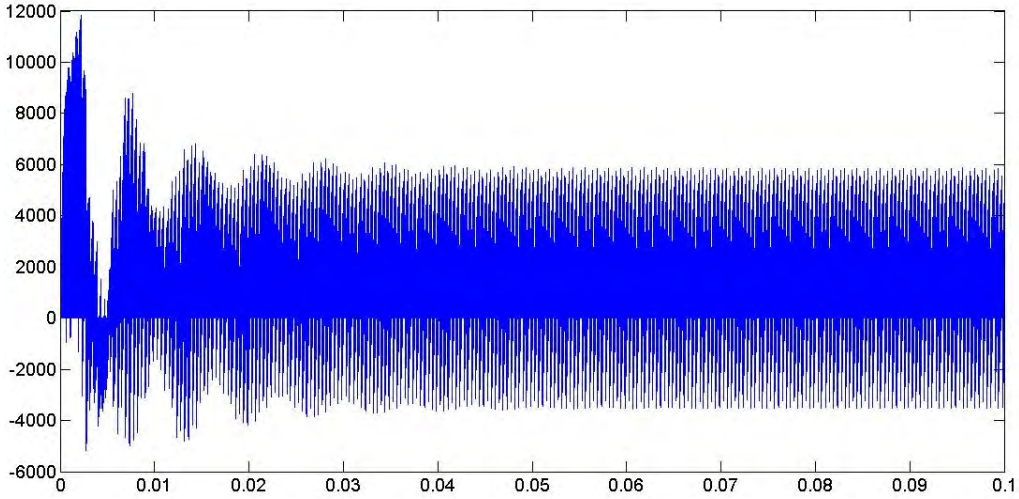


Figure 212.—Voltage Source Inverter Input Current.

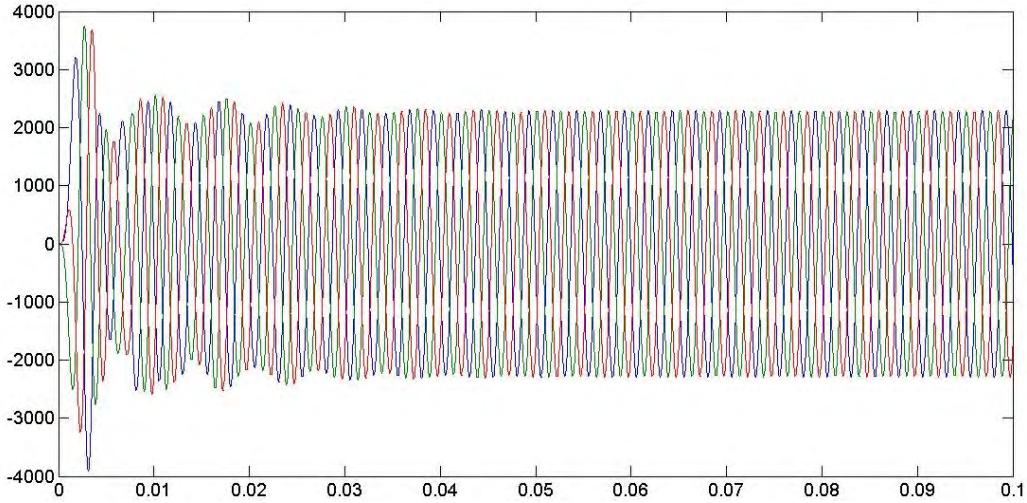


Figure 213.—Voltage Source Inverter Output Current.

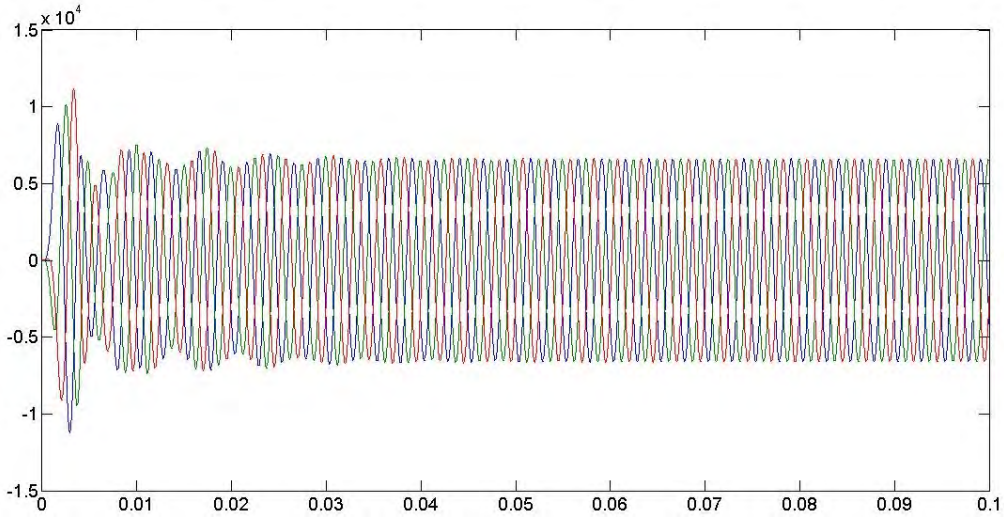


Figure 214.—Voltage Source Inverter Output Voltage.

7.6 System Modeling

The components described in the previous sections were used to construct the system models. A variety of system models were created to simulate several failure conditions. The models were created in Simulink using SimPowerSystems. (The state-space models were not used because some of the dynamic behavior of the system would be lost.) All the models are run using a MATLAB script, and all variables in the model can be changed by the script.

The generator in the models was represented by a voltage source with an inductance and resistance in series. The generator parameters used for the system models are shown in Table 40.

The motors were modeled using SimPowerSystem's permanent magnet machine model. The motor model can be speed or torque controlled. The parameters that were set in the model are shown in Table 41.

All component variables have the settings that were listed in the component model summaries.

The naming convention used for all components in the Simulink models and MATLAB scripts are shown in Figure 215. The figure also shows which SSCB are open and closed during normal operation. The same convention will be used the failure scenario diagrams. In the failure models, the SSCB will switch from the normal operation state to the state shown in the failure diagram after a set delay from the time of the fault. The breakers that switch and the switching times are dictated by the MATLAB script.

TABLE 40.—SYSTEM MODEL GENERATOR PARAMETERS

Parameter	Setting
Voltage amplitude, V	25000
Frequency, Hz	60
Resistance, Ω	0.001
Inductance, H	0.01

TABLE 41.—SYSTEM MODEL MOTOR PARAMETERS (REFS. 188 AND 189)

Parameter	Setting
Speed, rpm	3000
Armature inductance, H	0.000102
Armature resistance, Ω	0.2
Pole pairs	4
Amplitude of the flux induced by the permanent magnets of the rotor in the stator phases	0.044235
Combined viscous friction of rotor and load, N.m.s	0.1035
Combined inertia of rotor and load, kg/m^2	0.00112

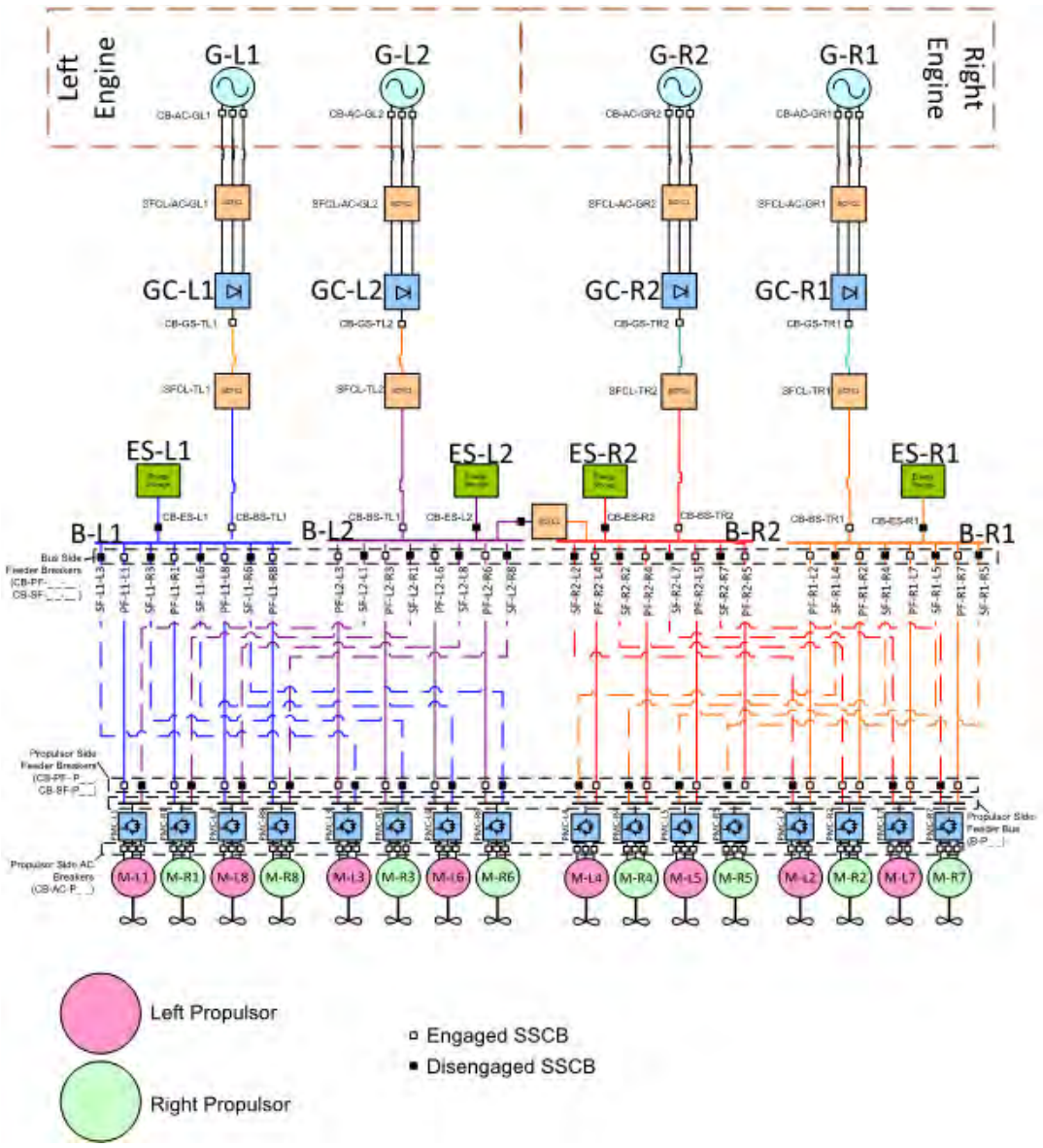


Figure 215.—System Naming Convention.

7.6.1 Single Motor Model

The single motor model represents the interactions of the components along a single path from a generator to one motor. Faults can be placed in the path and the response of the system can be tracked. To demonstrate the model capabilities, the model was run with a line to ground fault on the bus that occurs at 0.6 s. Figure 216 and Figure 217 show that the source is mostly unaffected by the fault. Figure 218 shows the fall in bus voltage after the fault. It takes the bus about 0.04 s to drop to zero. Figure 219 and Figure 220 show the bus current upstream and downstream of the fault. The figures demonstrate the magnitude of the fault current which is about 5 times the nominal current. Figure 220 shows a delay between the circuit breakers isolating the fault and the time that the SMES activates. The SMES current is not filtered in this case. Filtering can be added to smooth the bus current when the SMES is discharging. Figure 221 and Figure 222 show the load voltage and current. The delay between the fault and the SMES discharge is again present. In this simulation, voltage regulation for the SMES was not active; therefore, an overvoltage situation occurs.

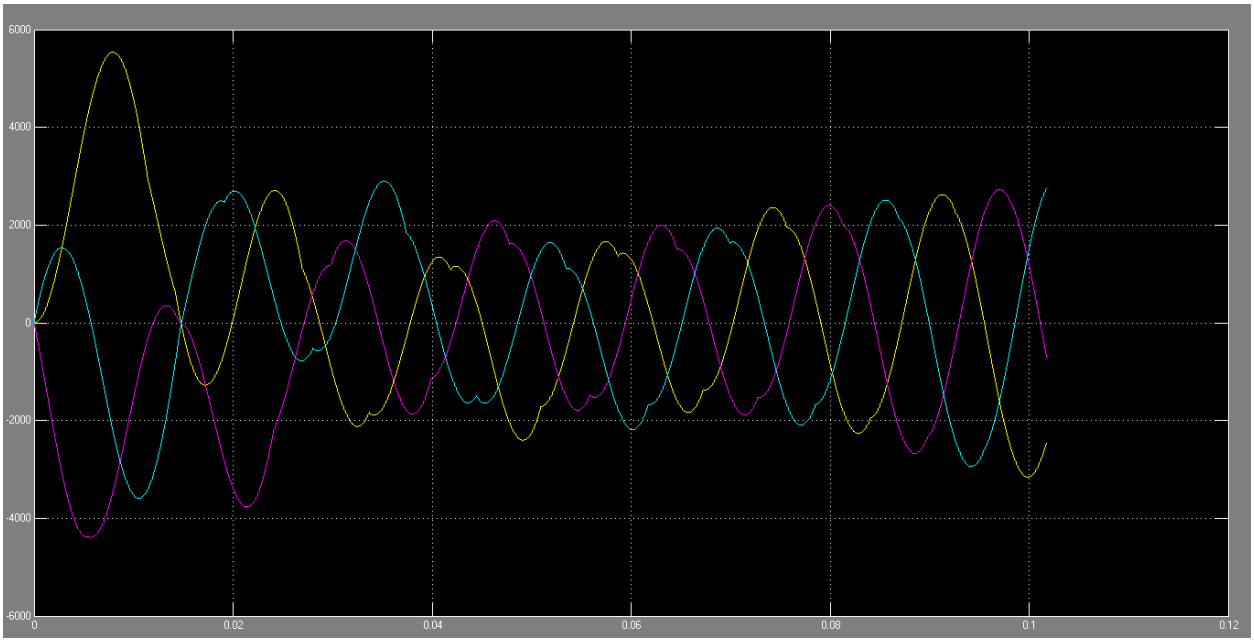


Figure 216.—One Motor Simulation Source Current (A).

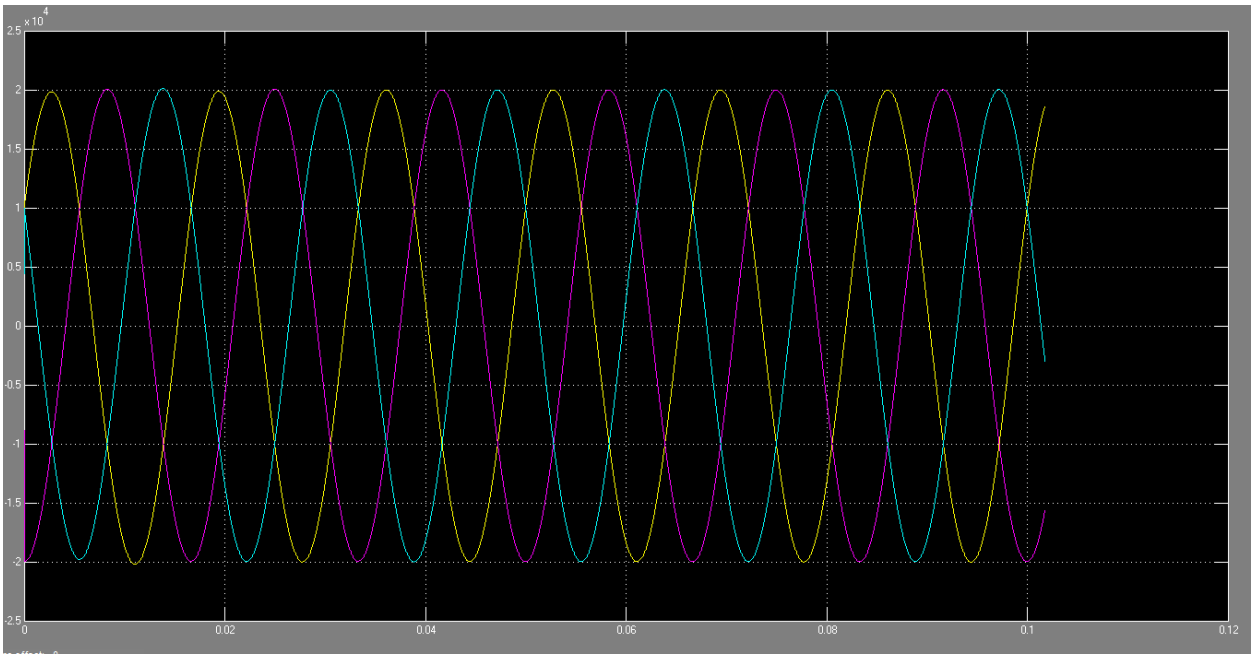


Figure 217.—One Motor Simulation Source Voltage (V).

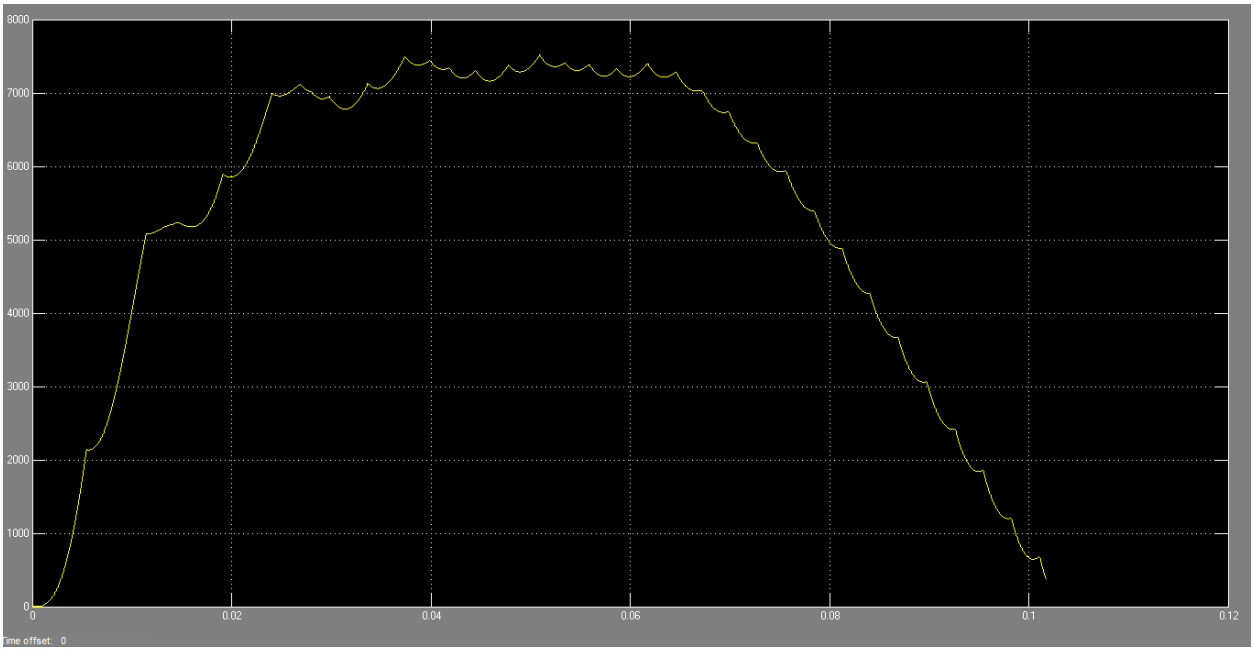


Figure 218.—One Motor Simulation Bus Voltage (V).

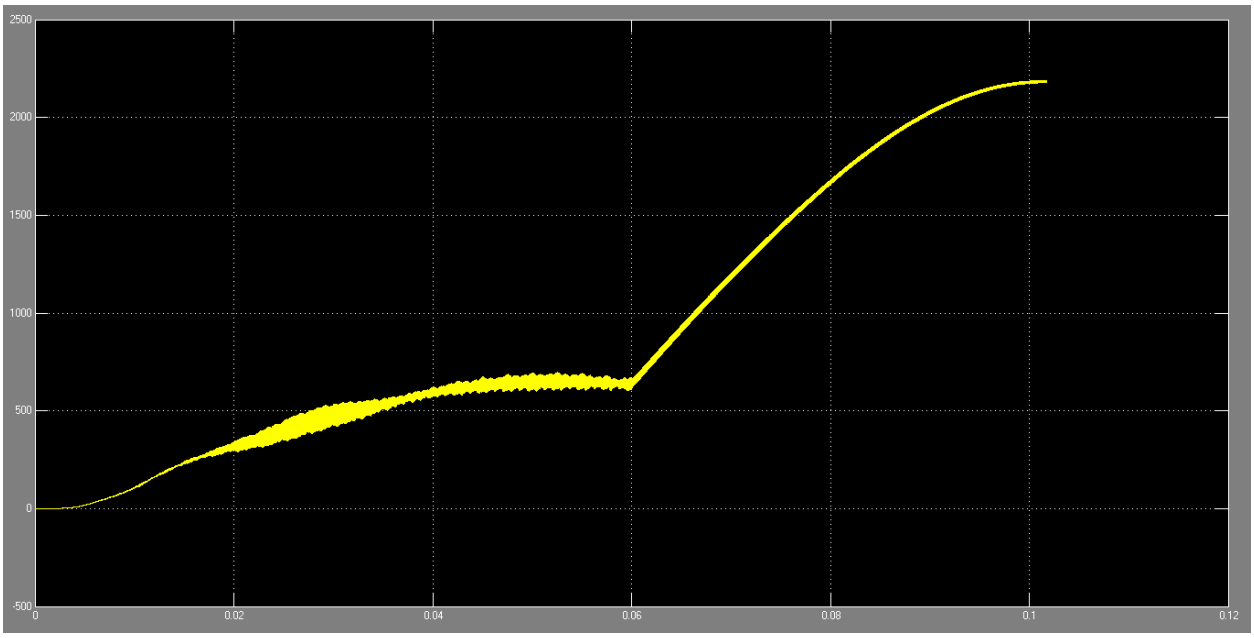


Figure 219.—One Motor Simulation Bus Current Upstream of the Fault (A).

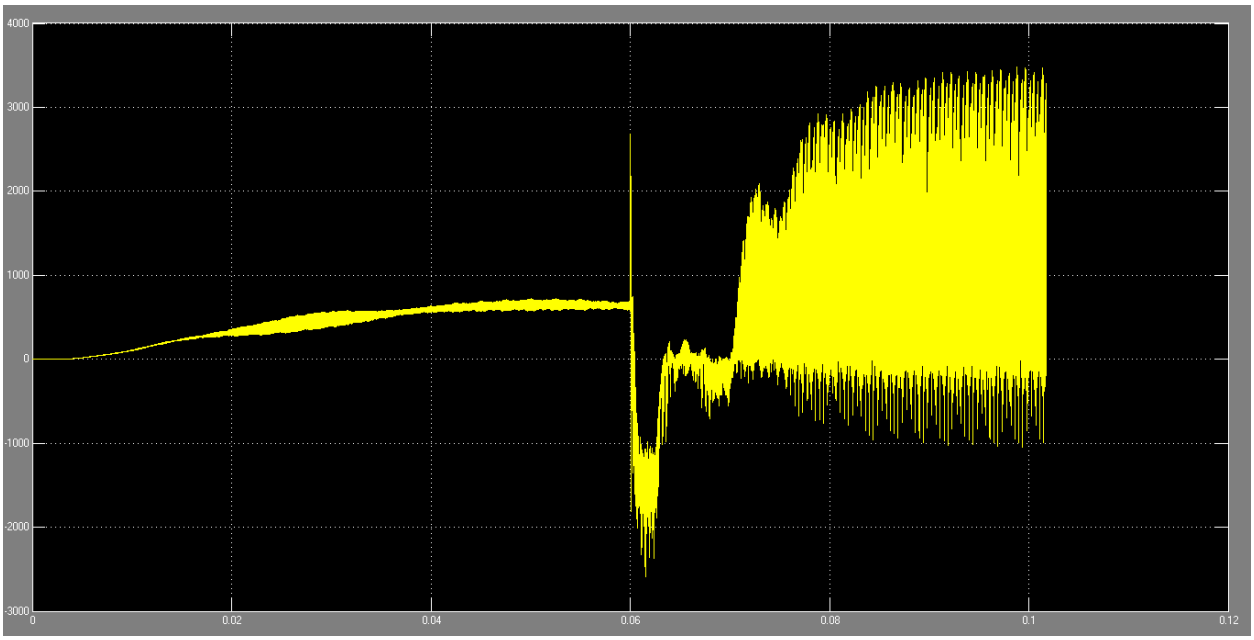


Figure 220.—One Motor Simulation Bus Current Downstream of Fault (A).

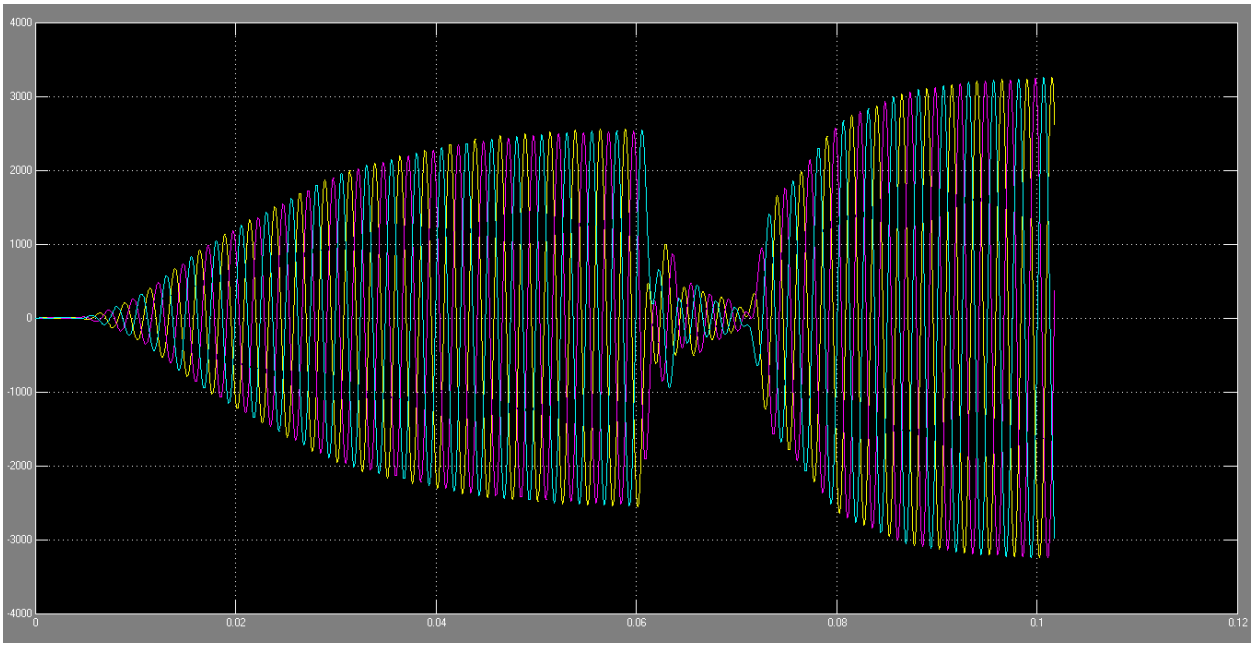


Figure 221.—One Motor Simulation Load Voltage (V).

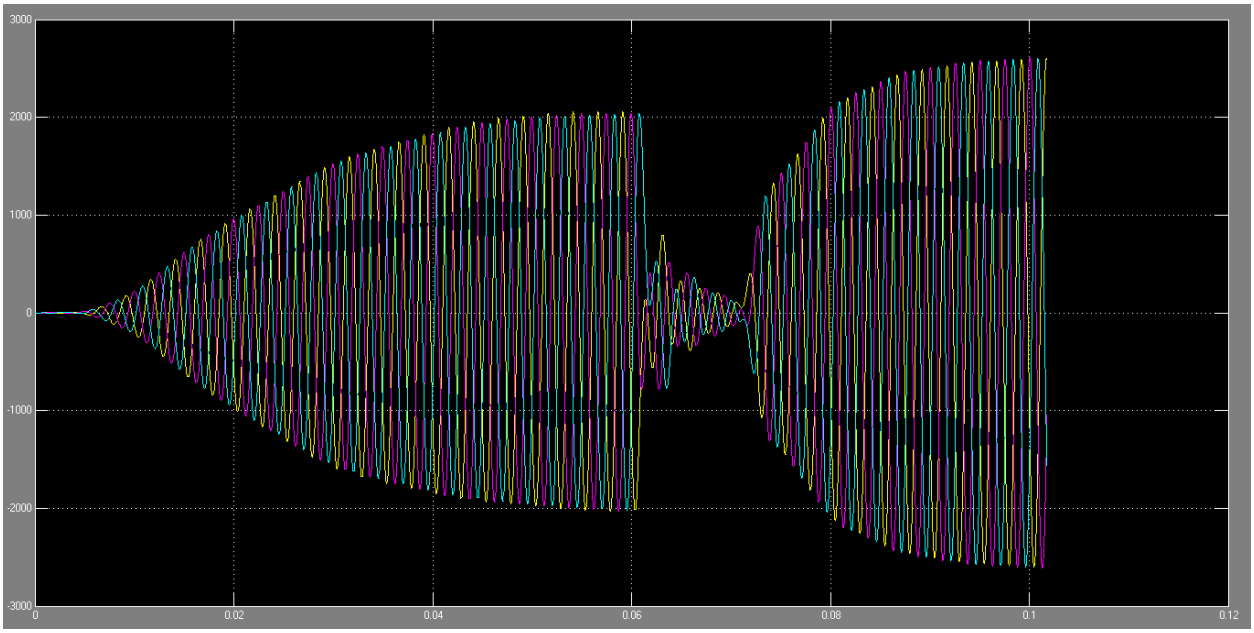


Figure 222.—One Motor Simulation Load Current (A).

7.6.2 Fault Isolation Model

The fault isolation model simulates the response of one branch of the system. A branch consists of a generator, rectifier, bus, four inverters, four motors, and any required protection devices. The model can be used to track the response of the branch if a fault occurs. This model will only allow the effect of a fault to be examined; it does not include recovery. This model serves as the base to the models created to simulate a variety of failure scenarios.

7.6.3 Nominal Recovery Model

The nominal recovery model is the fault isolation model with an emulation of the L-1 branch and right side of the architecture. The generator, rectifier, and bus for the L-1 branch are emulated using a DC voltage source with an added inductance. The L-1 branch loads were modeled as resistors. Resistive loads were chosen since the power factor of the superconducting motors should be close to unity; however, an inductance can be added to the model. Simply change the load block to a RL load. The inductance will automatically be pulled from the MATLAB script.

The emulation of the right side of the architecture is dependent of the failure scenario being modeled. In the case of a failure on the right side of the architecture, the right side will be emulated as a load. In all other scenarios, the right side of the architecture will be emulated as a voltage source. The model can be viewed in Appendix B. The model is used as the base to simulate the failure scenarios.

7.6.4 Failure Scenarios

7.6.4.1 Right Engine Failure Model

The right engine model simulates the system response in the event that the right engine fails. The model consists of the nominal recovery model with a load that represents the right half of the electric grid. An overview of the failure scenario is shown in Figure 223. When the right engine fails, power from the left engine must be rerouted to supply power to the right engine loads. L-1 is used to power its loads and the loads of L-2. The power from L-2 is routed to the R-1 and R-2 loads. Energy storage is used to power R-1 and R-2 for the time that it takes to reroute the power from GL-2.

The right engine failure model was run with a failure occurring at 0.025 s. The source and bus voltage on the L-2 branch is similar to that of the single motor model. The biggest difference is now the power is rerouted to the right side of the architecture during the failure. The current flow to the right side load emulation is shown in Figure 224. The current is shown as zero before failure because the right side source is not simulated in this case. After power is rerouted, the load current reaches steady state after about 0.005 s. When the failure occurs, the SMES is discharged to supply power to the loads while power is being rerouted. The SMES discharge current is shown in Figure 225. Since the power is rerouted from L-2 to the right side of the architecture, L-1 must now supply the L-2 loads. The input current to the inverters to the L-2 loads is shown in Figure 226. It appears that the emulated source for L-1 has difficulty supplying the current to the L-2 loads in this situation. The unsteady and low amount of current causes the motors to lack input power. The input voltage and current for the motors are shown in Figure 227 and Figure 228. Further study is needed to determine how to emulate the L-1 load so that the correct level of power is delivered to the L-2 loads in the case of the right engine failure. Also, the shared power from L-1 causes a drop in current supplied to the L-1 loads, which is shown in Figure 229.

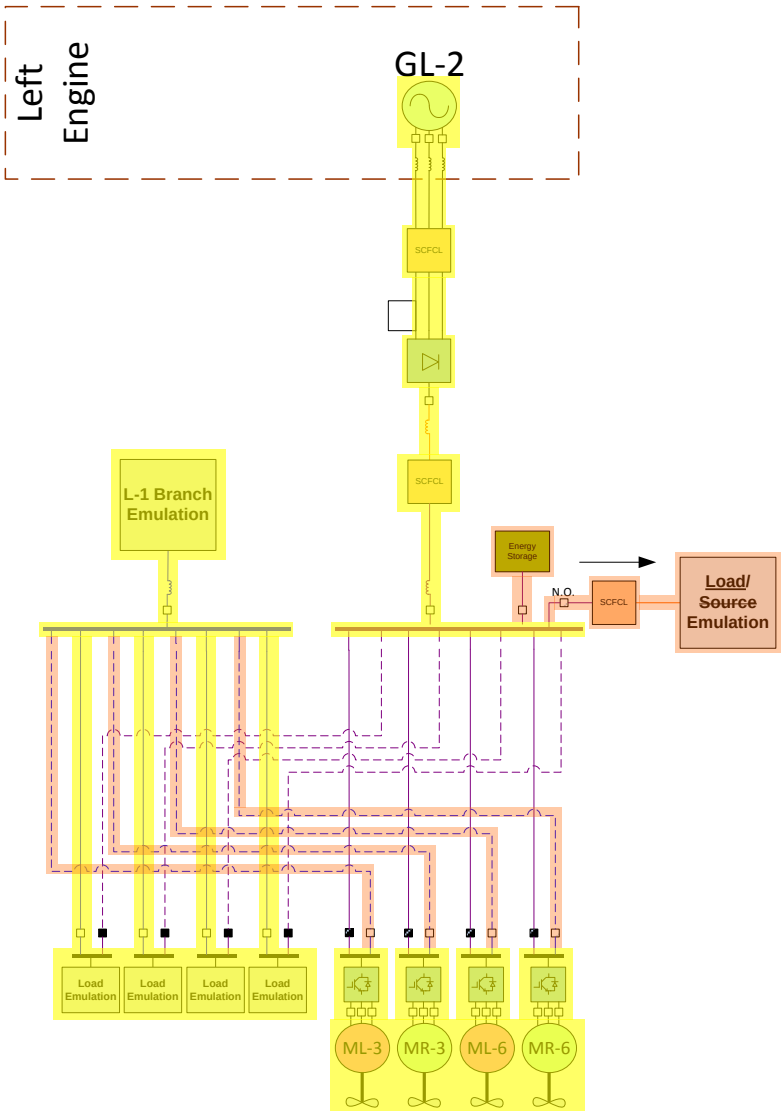


Figure 223.—Right Engine Inoperable Power Flow.

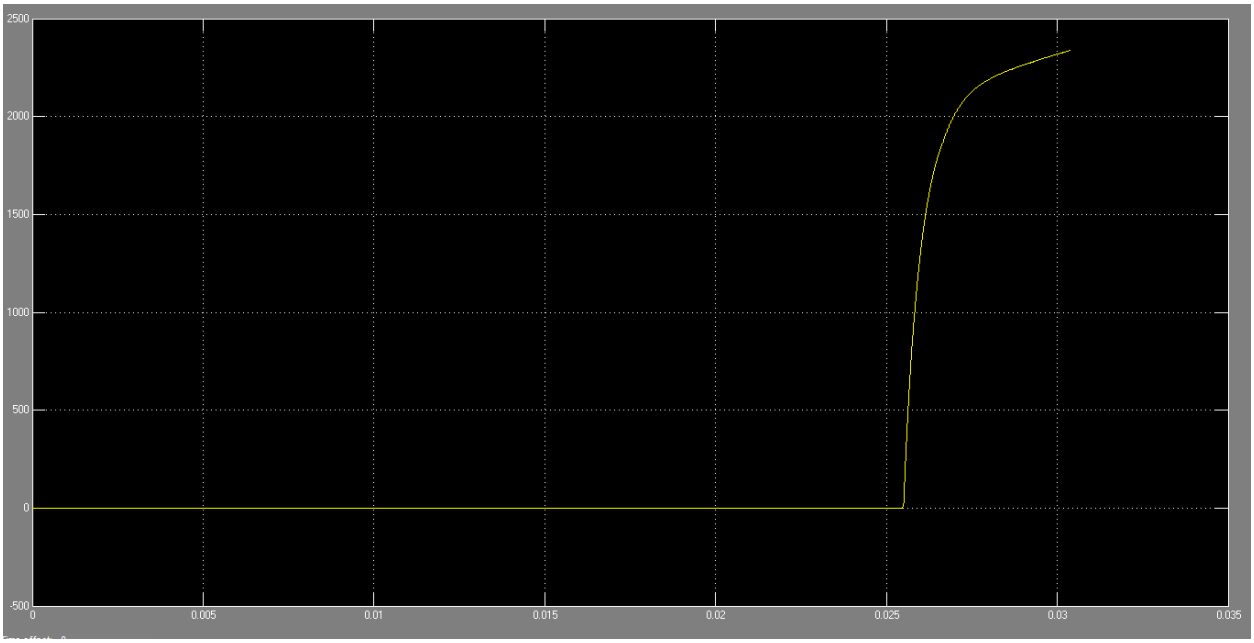


Figure 224.—Right Engine Failure—Right Engine Load Emulation Current (A).

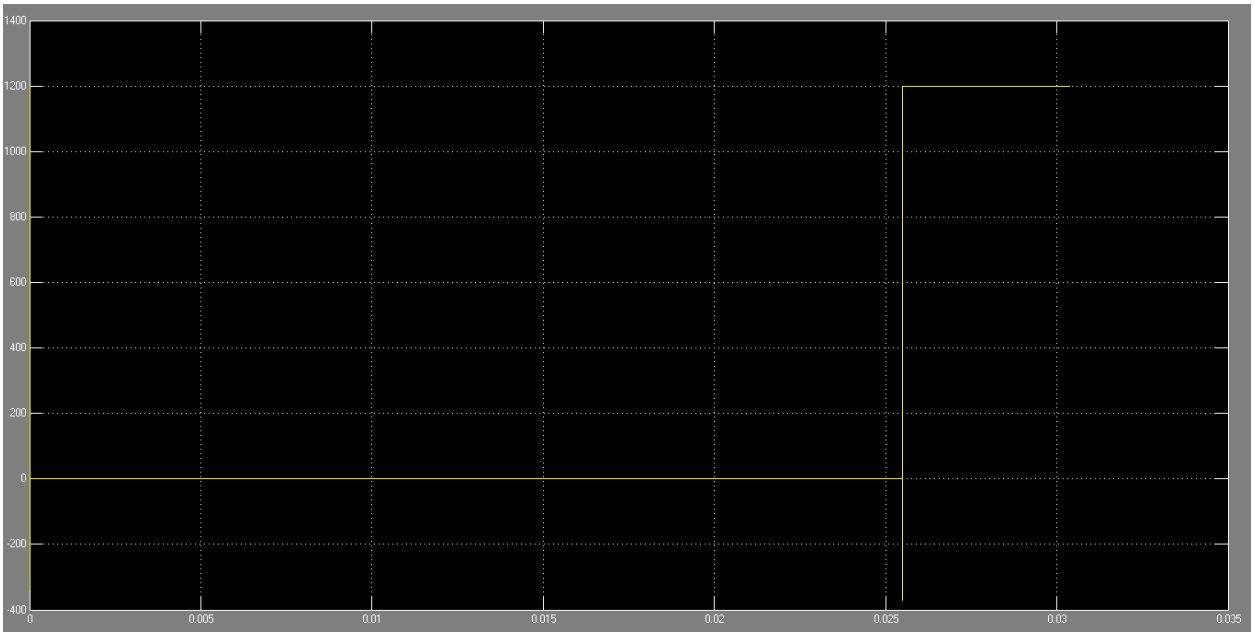


Figure 225.—Right Engine Failure SMES Discharge.

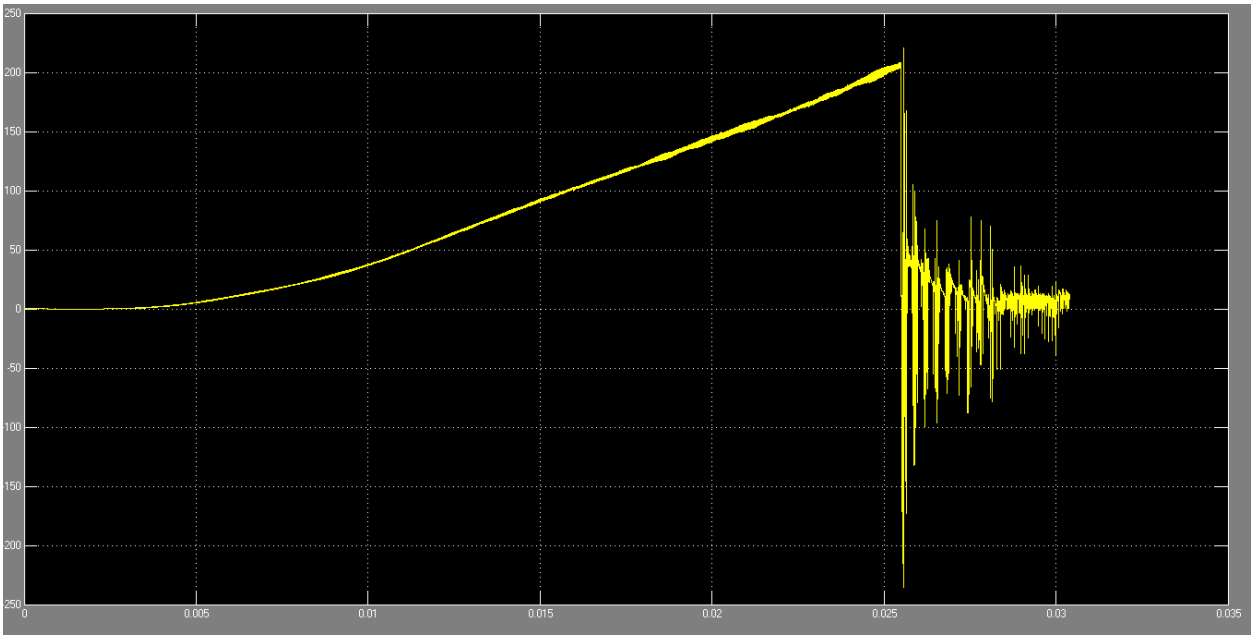


Figure 226.—Right Engine Failure L-2 Inverter Input Current (A).

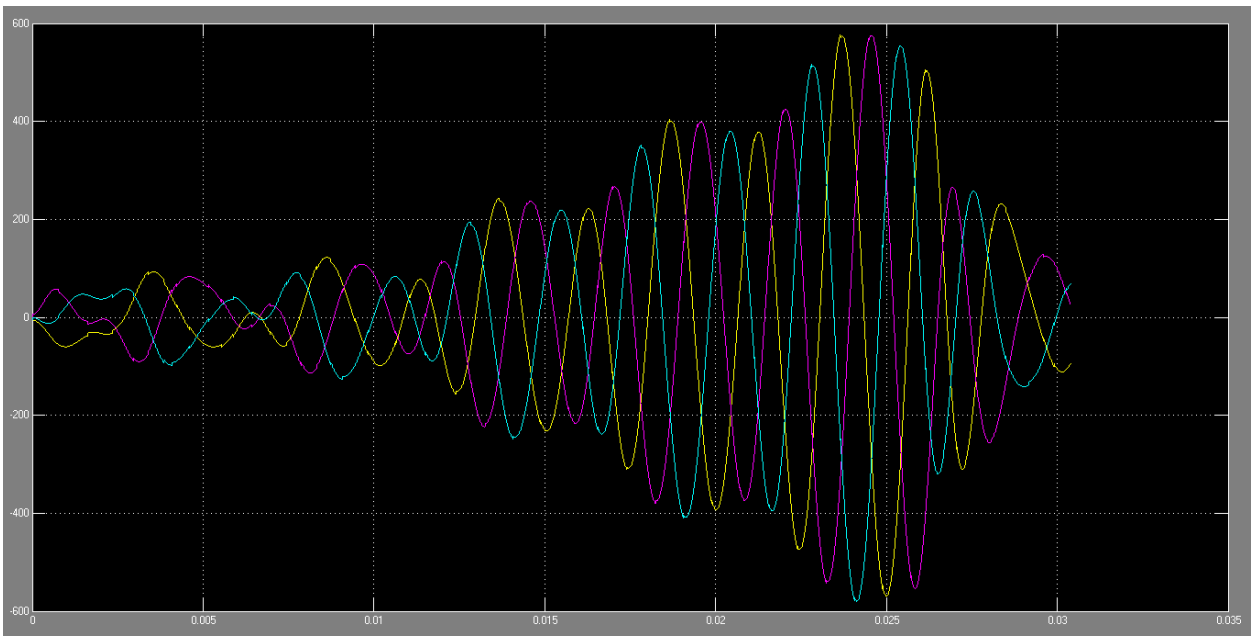


Figure 227.—Right Engine Failure Motor Input Voltage (V).

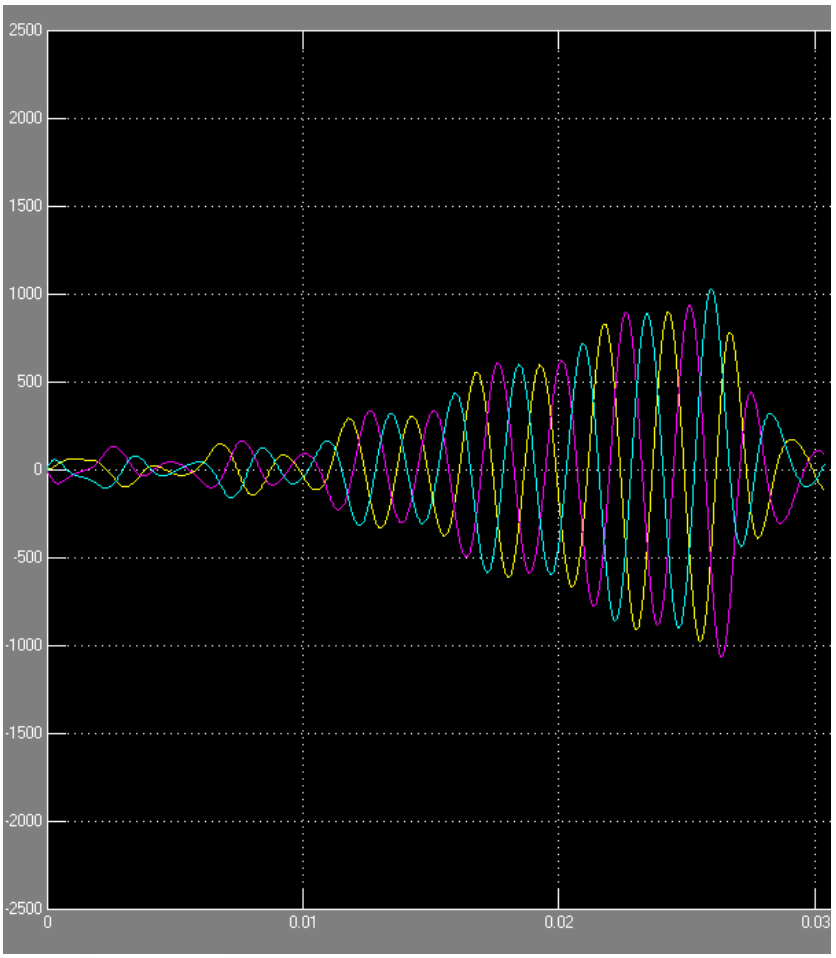


Figure 228.—Right engine failure motor input current (A).

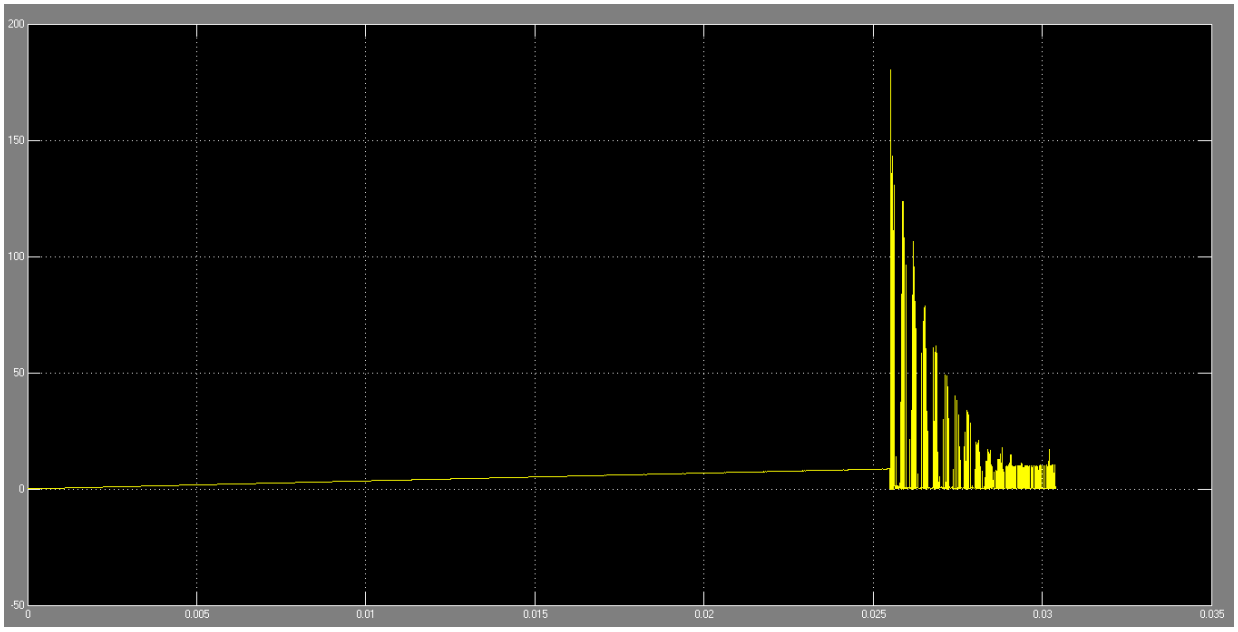


Figure 229.—Right Engine Failure L-1 Load Current (A).

7.6.4.2 Left Engine Failure Model

The left engine failure model is the same as the right engine failure model except the right side of the grid is now modeled as a source rather than a load. A diagram of the left engine out scenario is shown in Figure 230. Like the L-1 emulation, the right side of the grid is modeled as a DC voltage source and inductance. When the left engine fails, the L-1 and L-2 loads must be powered by the right side of the grid. The SMES is used to power the loads for the short amount of time that it takes to reroute power from the right side of the grid to the L-1 and L-2 loads.

The engine out condition was simulated using this model. When the engine fails, the source current and voltage are driven to zero. The results of the simulation are shown in Figure 231 to Figure 235. In this simulation, the engine failure occurs at 0.089 s. Figure 231 shows that the bus voltage rapidly falls after the failure; however, there is a rapid increase in voltage once power is rerouted. Figure 232 shows the bus current. After the failure, bus current falls to zero after about 0.0005 s. The SMES discharge current is shown in Figure 233. Figure 234 shows the inverter input current. Current flow is actually reversed after the failure. This may be due to a back EMF being produced by the motor. More study is needed to determine the exact cause of this phenomenon. Figure 235 and Figure 236 show the motor current and voltage. The motors lose a great deal of power during the failure. More analysis is needed to determine the cause of the power loss and how to update the recovery scheme in order to return the motors to normal operation.

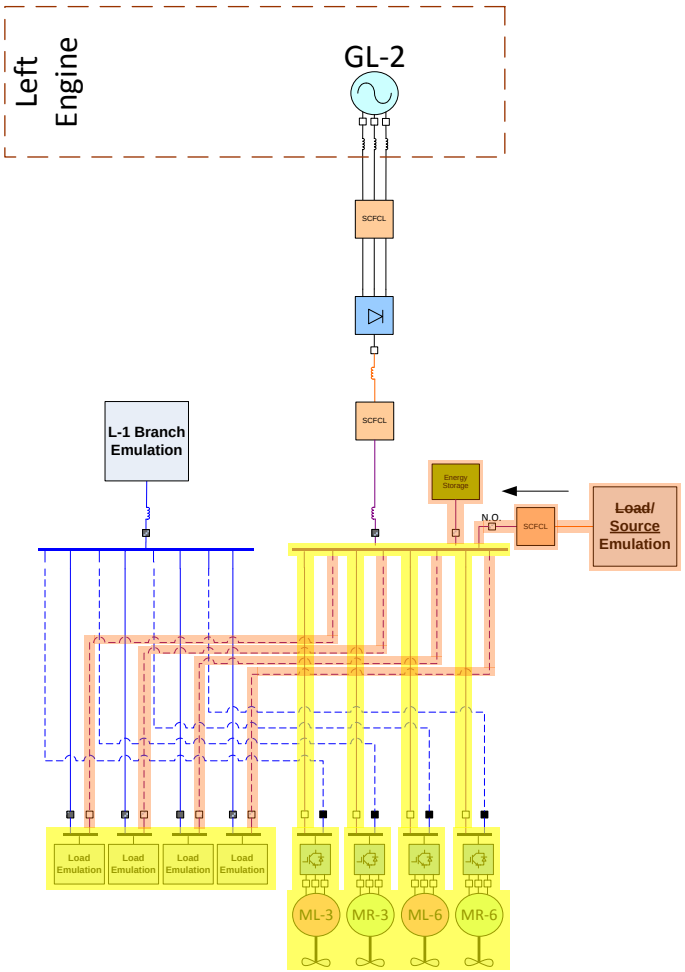


Figure 230.—Left Engine Inoperable Power Flow.

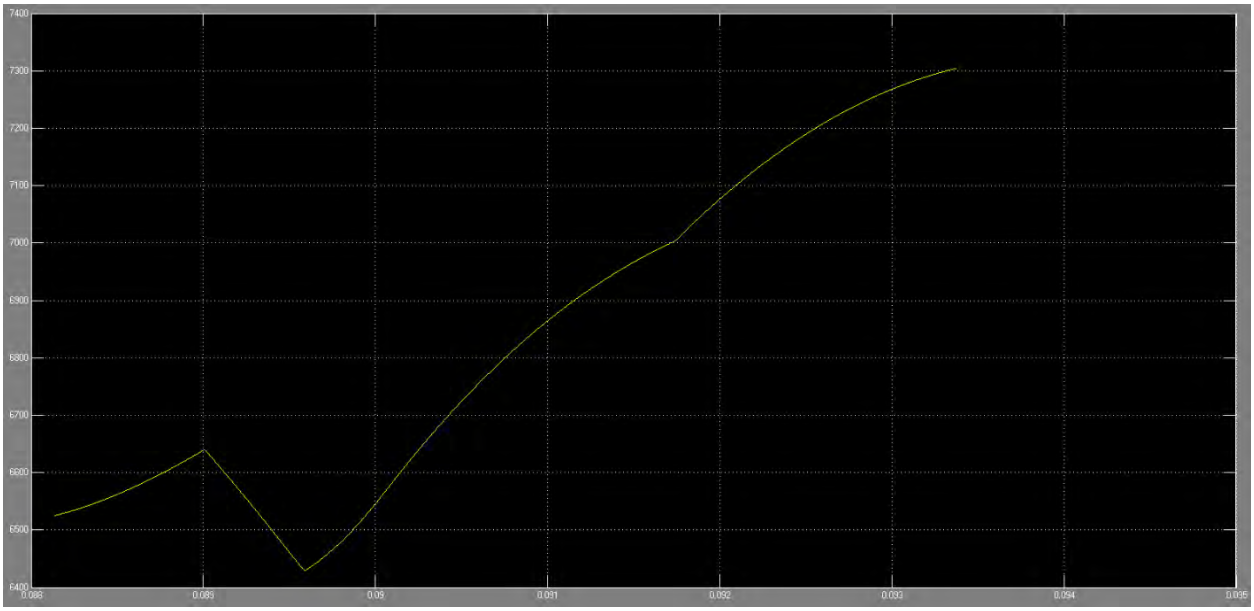


Figure 231.—Left Engine Bus Voltage.

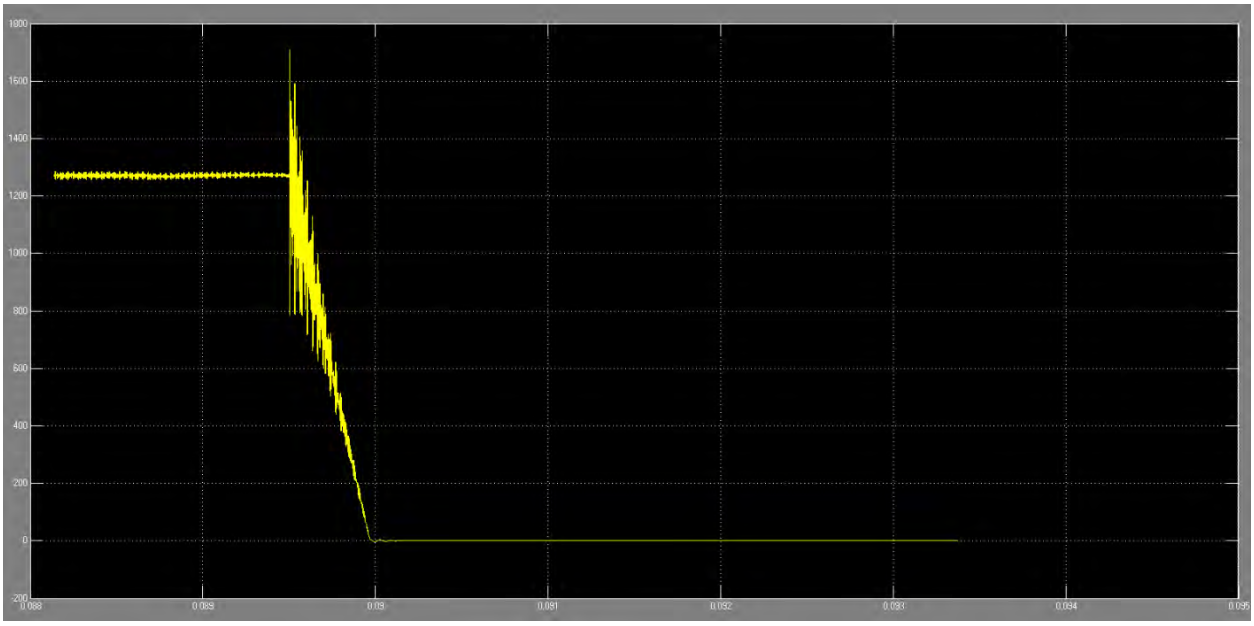


Figure 232.—Left Engine Failure Bus Current.

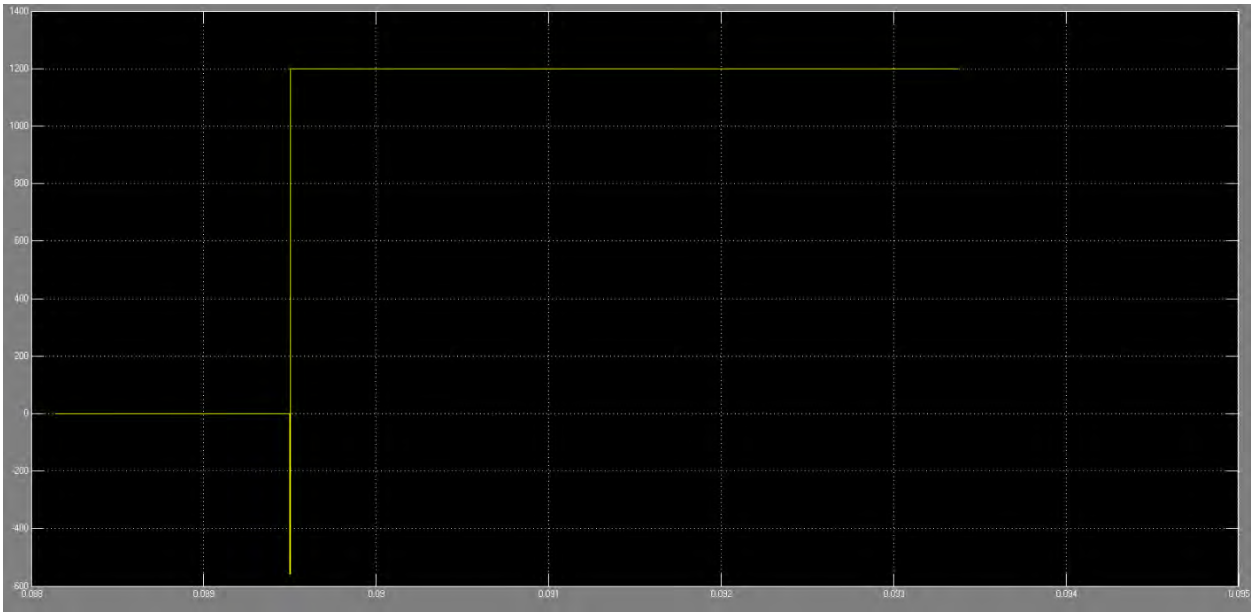


Figure 233.—SMES Discharge Current.

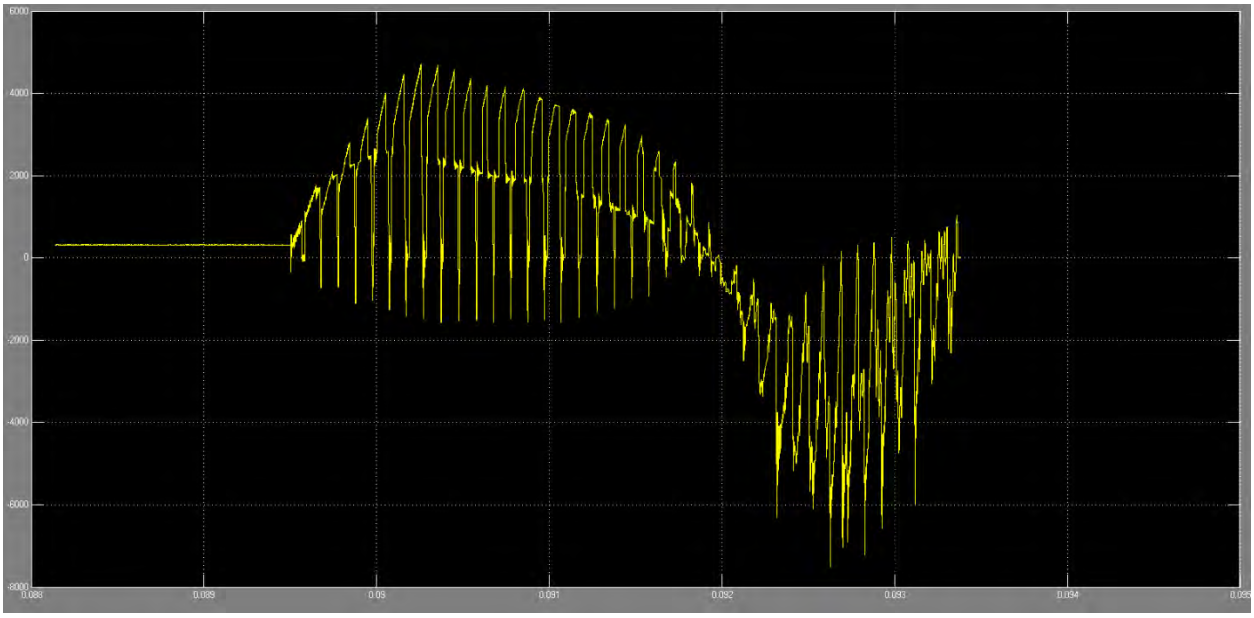


Figure 234.—Left Engine Failure Inverter Input Current.

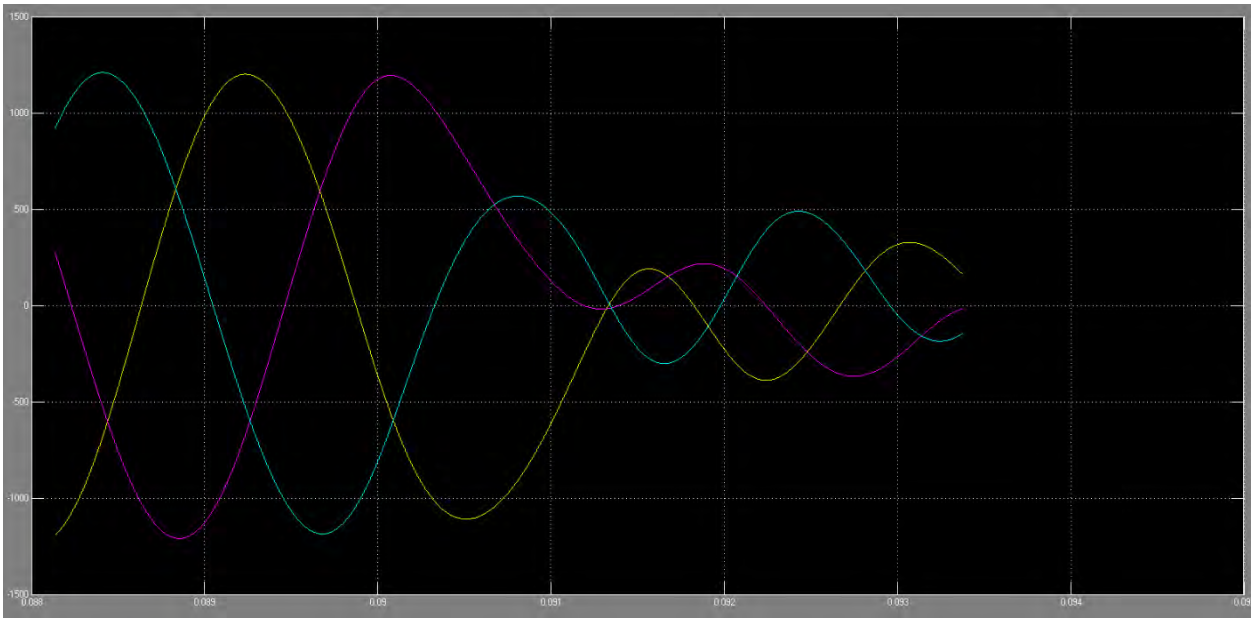


Figure 235.—Left Engine Failure Motor Input Current.

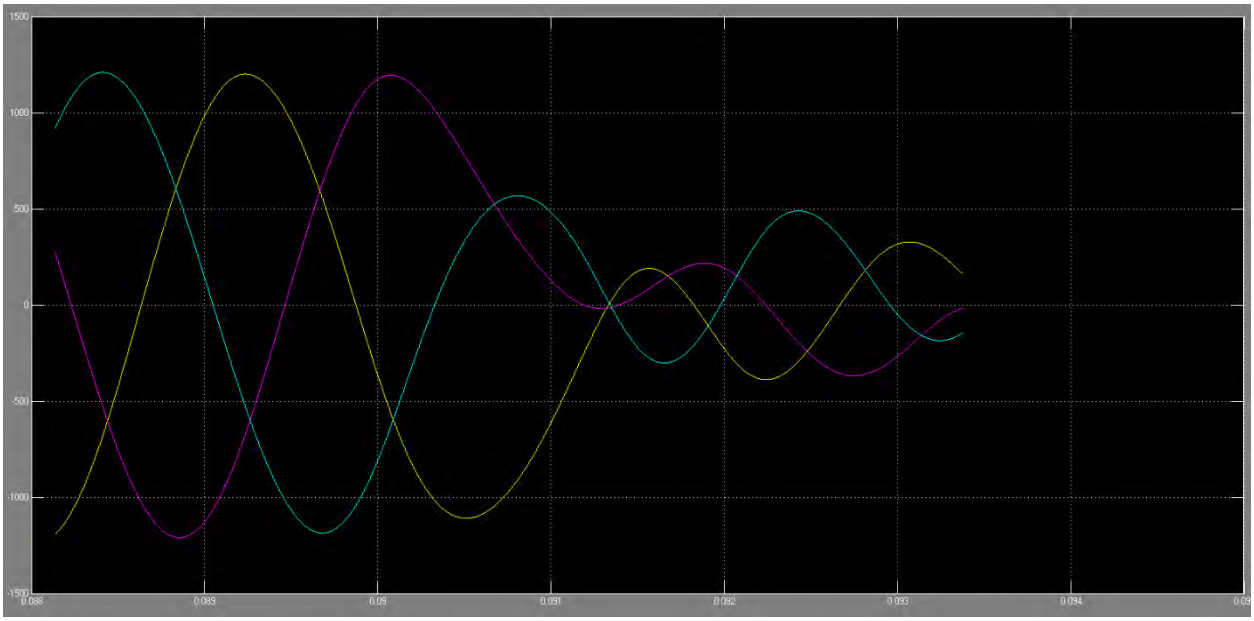


Figure 236.—Left Engine Failure Motor Input Voltage.

7.6.4.3 L-2 Branch Fault Model

The L-2 branch fault model is the nominal recovery model with a fault inserted on the L-2 bus. (The fault block can be moved to other locations on L-2 to simulate other scenarios.) A diagram explaining this scenario is shown in Figure 237. When the fault occurs, power is rerouted from the L-1 branch to the L-2 loads. A demonstration of the fault model is shown in Figure 238 to Figure 243. In this case, the system was faulted at 0.04 s. Figure 238 demonstrates the fall of bus voltage after the occurrence of the fault. Figure 239 shows the increase in current on the bus upstream of the fault. Figure 240 shows the fault current on the bus. The fault current is about 3 times the level of the nominal current. Figure 241 shows the input current into the inverter. A delay between the time of the fault and when the SMES begins to supply current to the load is shown in the figure. Again, the SMES current can be smoothed with the use of inductive filters. Figure 242 and Figure 243 show the load voltage and current. Again the time delay between the fault and recovery is present. Also, with the component parameters settings, the input power for the load is reduced during recovery.

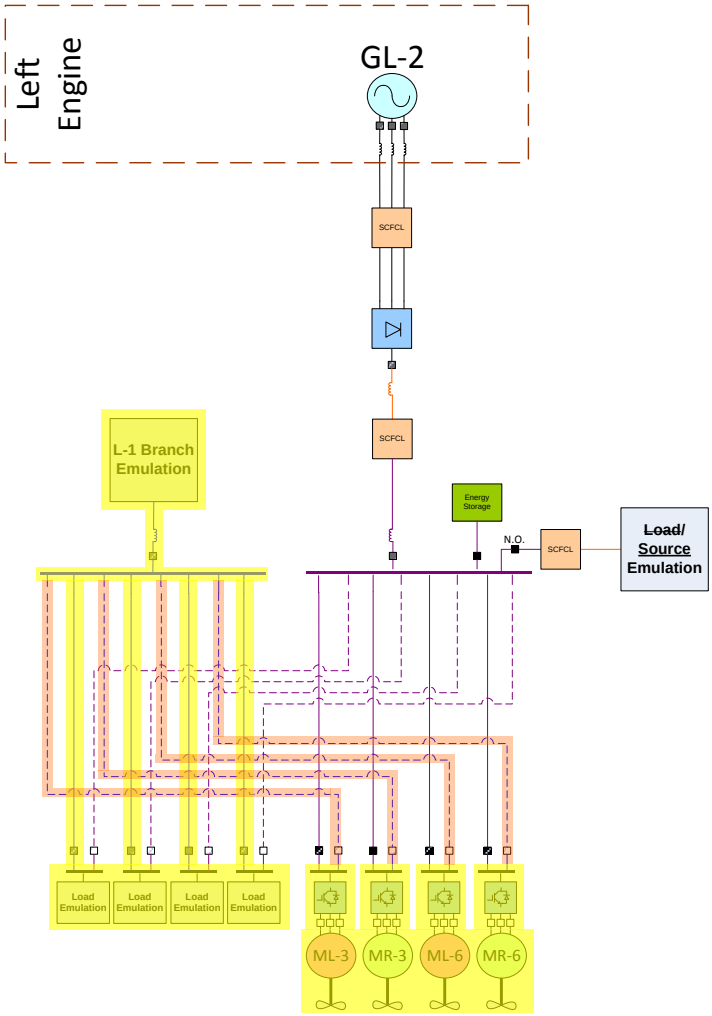


Figure 237.—L2 Branch Fault Power Flow.

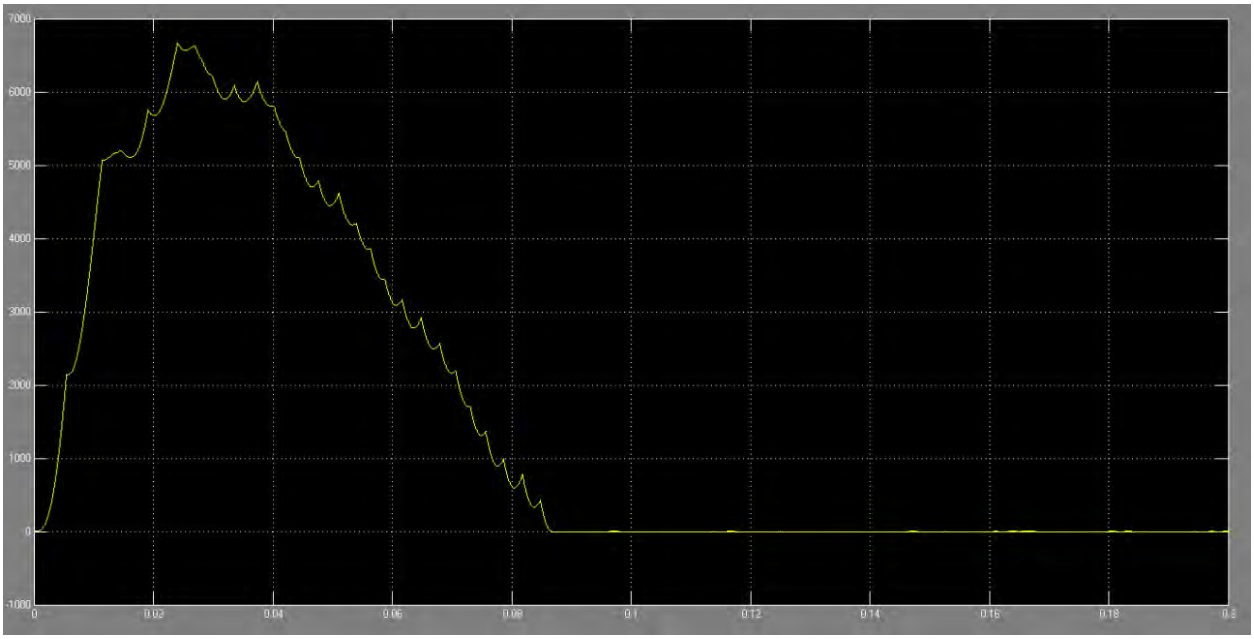


Figure 238.—L-2 Branch Fault Simulation Bus Voltage (V).

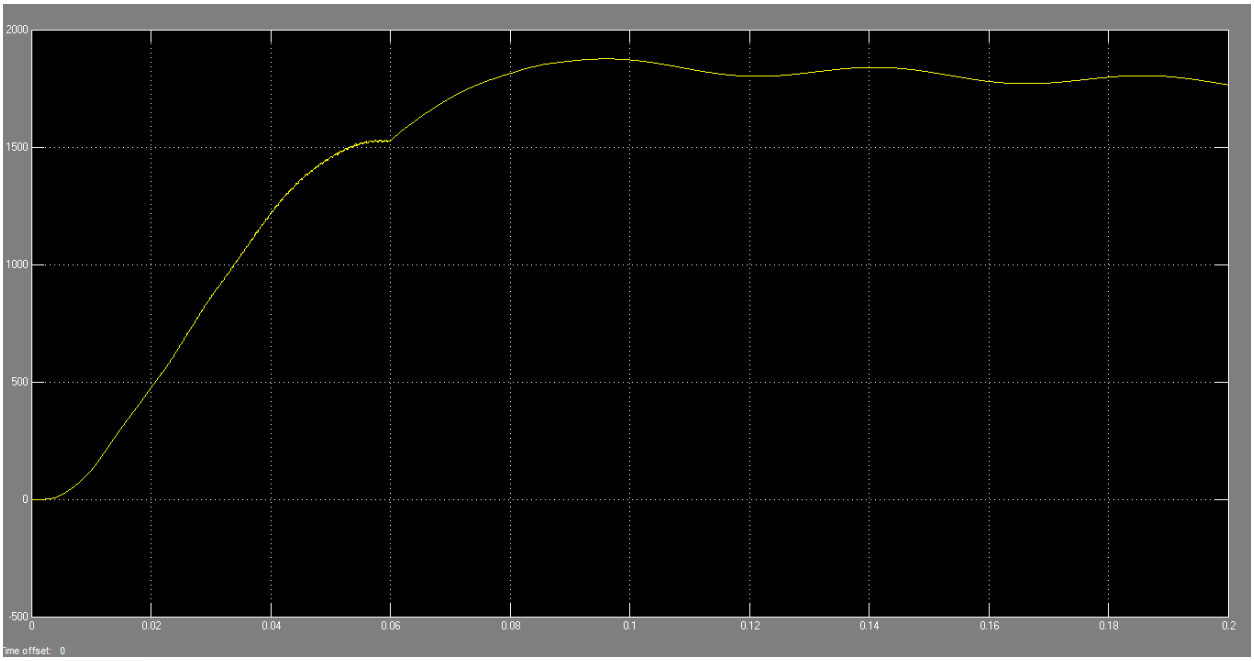


Figure 239.—L-2 Branch Fault Simulation Bus Current Upstream of Fault (A).

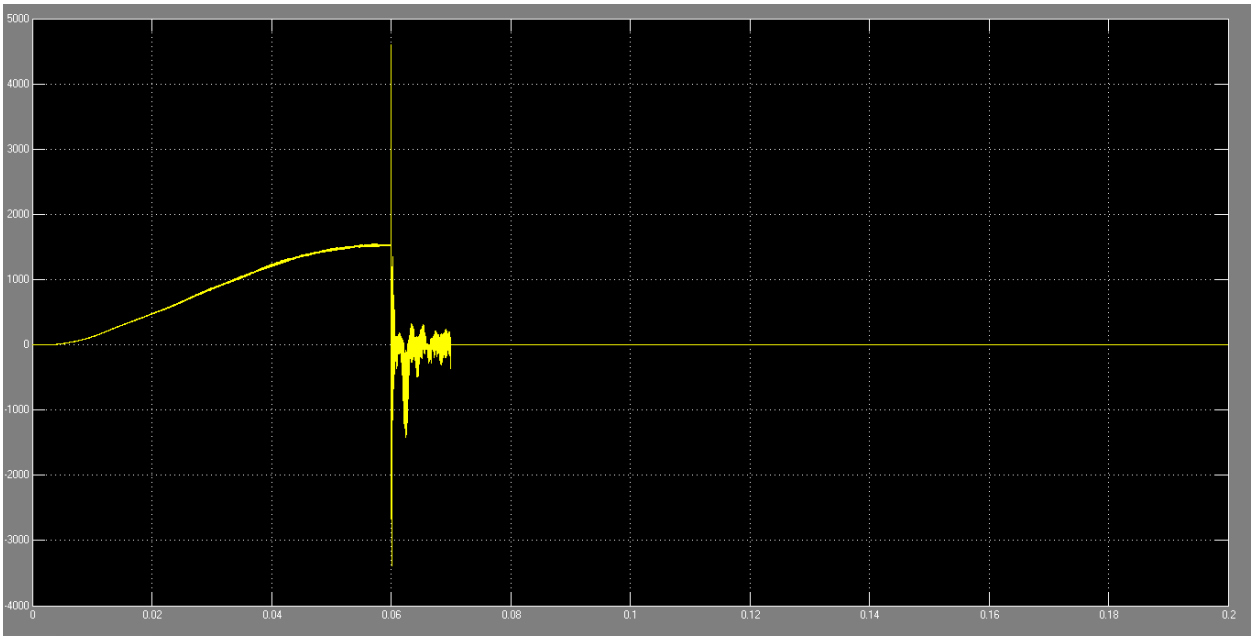


Figure 240.—L-2 Branch Fault Simulation Bus Current Downstream of Fault (A).

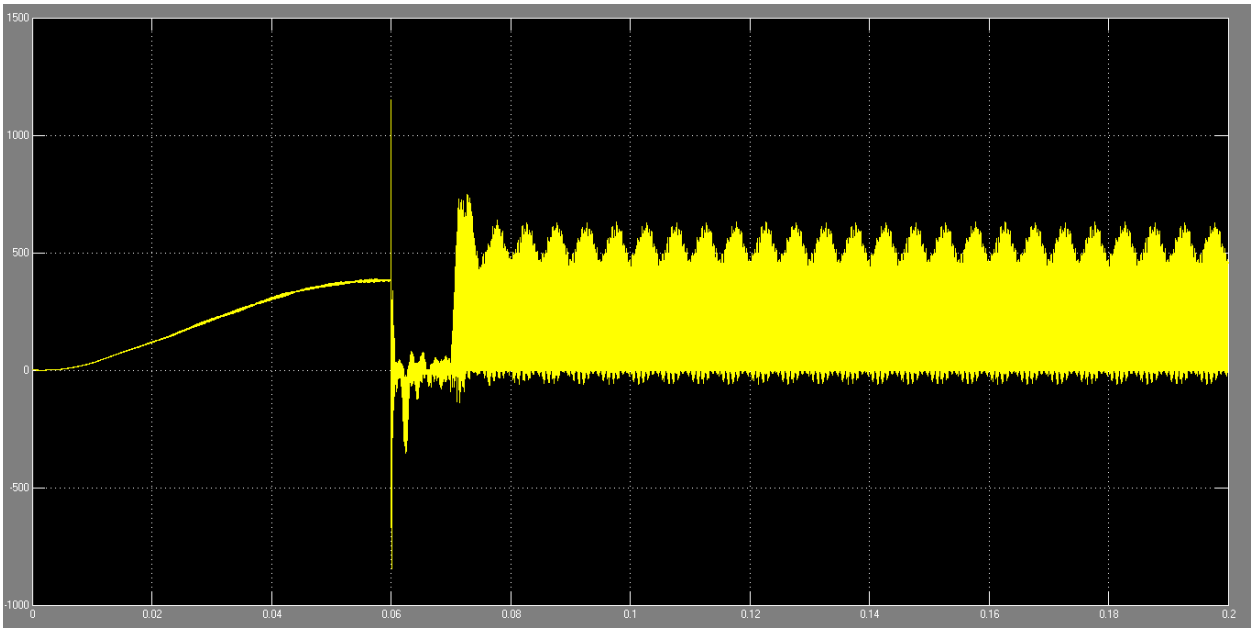


Figure 241.—L-2 Branch Fault Simulation Inverter Input Current (A).

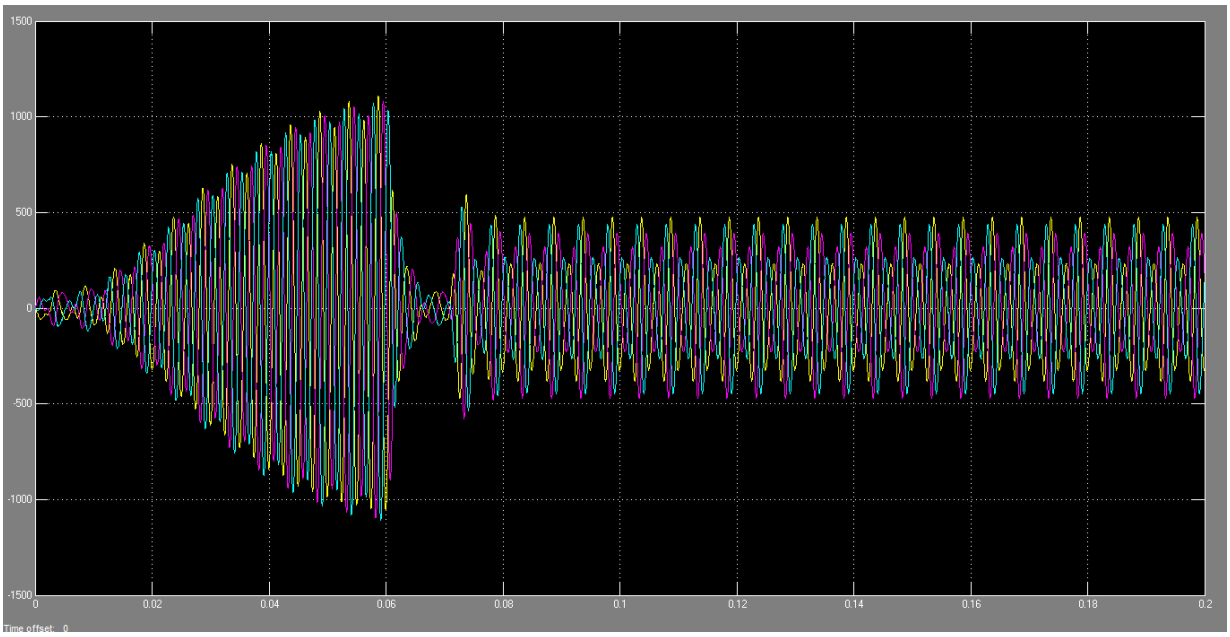


Figure 242.—L-2 Branch Fault Motor Input Voltage (V).

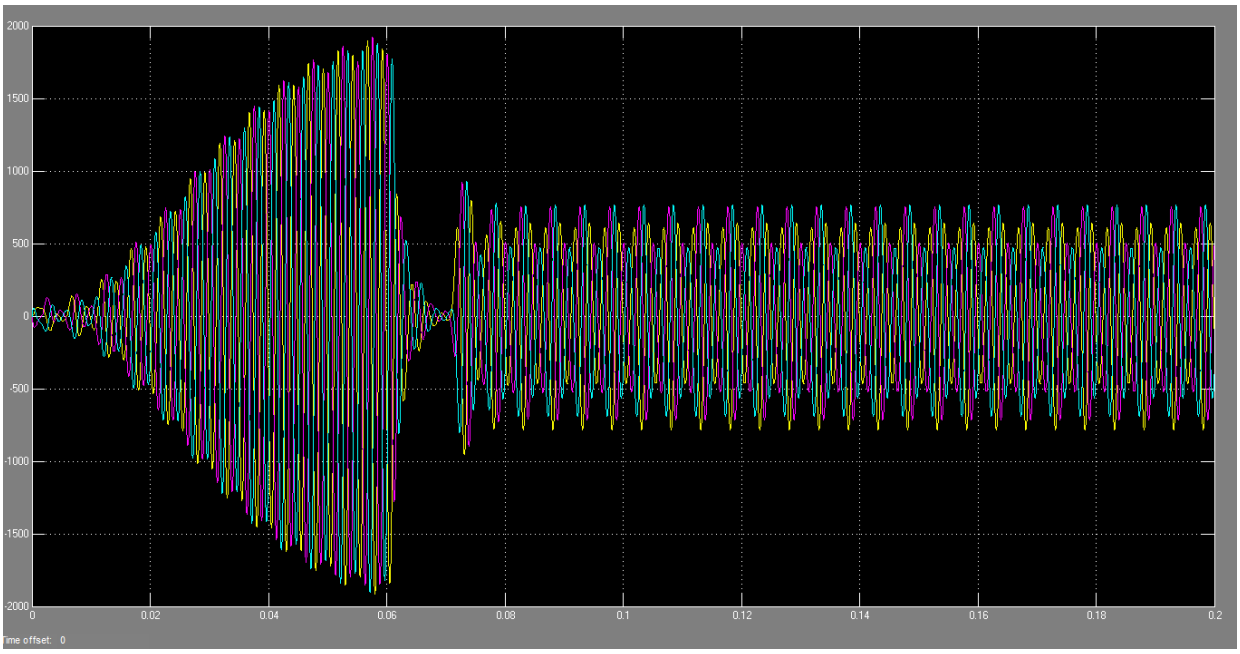


Figure 243.—L-2 Branch Fault Simulation Motor Input Current (A).

7.6.4.4 L-1 Branch Fault Model

Like the L-2 branch fault model, the L-1 branch fault model is the nominal recovery model with a fault (Figure 244). This time the fault occurs on the L-1 branch. When the fault occurs, power is routed from the L-2 branch to the L-1 loads. Energy storage is used to power the L-1 loads for a short amount of time. The behavior of this fault scenario will mimic the behavior of the L-2 branch during a fault.

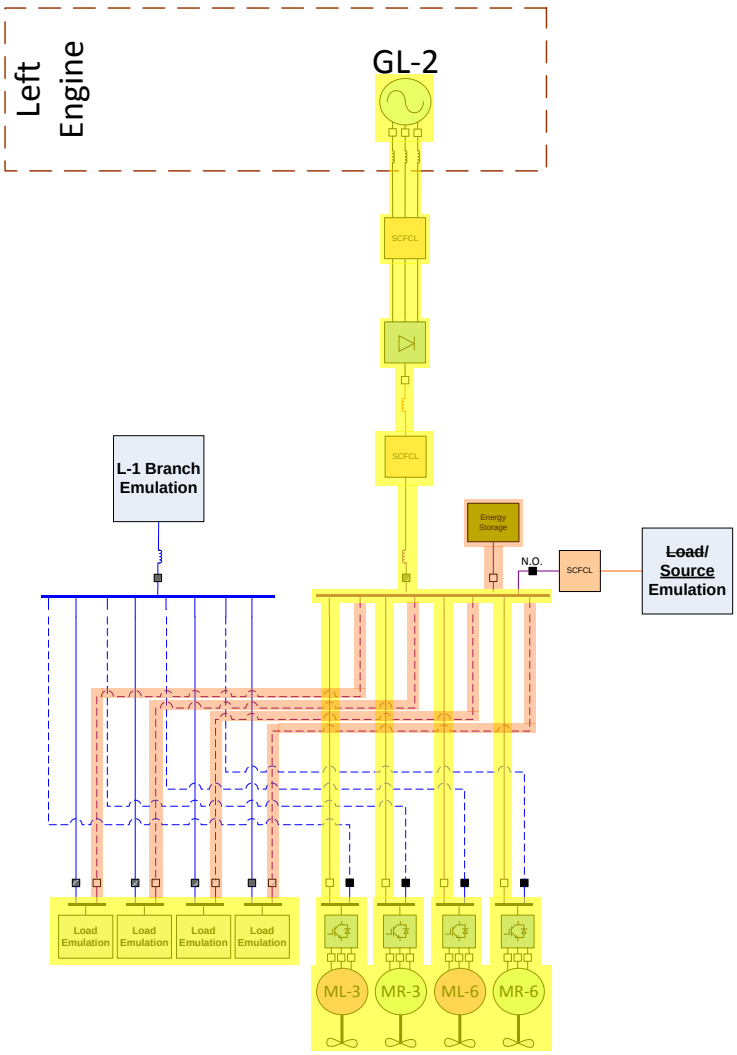


Figure 244.—L1 Branch Fault Power Flow.

7.6.5 Running the Models

The first step in running any of the models is to first run the corresponding m-file. The models will not run properly unless the correct corresponding script is used. Once the script runs, the Simulink model can be run. Scopes can be added to the model to track the system states. However, the addition of scopes will slow the model.

The full system dynamic simulations are computationally intensive and require a large amount of computer speed and run-time. Using a 64-bit machine with a minimum of 4.00 GB of ram is recommended for running the models. With a 64-bit machine with 8.00 GB of ram and a 3.4 GHz processor, a simulation of 0.1 s using the recovery model takes approximately 4 days. The single motor model can be run in approximately 3 hr.

One way to reduce the amount of time needed for the simulations is to start the models at steady-state. One way to achieve this is to run the nominal recovery model to steady-state and save the simulation state. To save the simulation state, go to the configuration parameter window and navigate to the data import/export pane. Select the final states check box, and then select the save complete SimState in final state check box. Enter a variable name for the SimState; then run the model long enough for the system to reach steady state. Once these results are saved, the simulation can start from this point. To resume the

simulation from the saved point, again go to the configuration parameters window. In the data import/export pane, select the initial state box under load from workspace. Enter the name of the variable used to save steady-state simulation. Keep the start value at the same start time. For the stop time, use the original stop time plus any additional time needed to simulate the failure. The different failure scenarios can then be studied by immediately causing the fault or failure.

7.7 Summary and Future Studies

During this study, a variety of component and system models were developed. The models will help determine component and system responses under steady-state and failure scenarios. Some important parameters that can be extracted from the simulations are fault currents and recovery time. Also, protection components can be activated and deactivated in order to determine the necessary level of protection in the system.

While the models are a good representation of the system, a number of improvements can be made to increase the fidelity of the simulations. One improvement needed for the SFCL model is to further examine the temperature calculation. This will include determining whether to use the thermal equivalent circuit approach or to use heat transfer equations. Also, the current model assumes that the amount of coolant is large enough that its temperature will remain at 77 K. This may not be the case and the model will need to be altered. Also, a copper shunt can be included in the model that was presented. Often resistive SFCL use a copper shunt in parallel. The shunt helps smooth the temperature rise in the superconductor during quenching to reduce the risk of damage from the heat being generated.

For the SSCB model, the inverse-time overcurrent protection scheme can be improved. In many applications, a rotating disc model is used in the control. In this case, the timer is not completely reset when the current falls below the tripping current. Instead, a “disc” with some inertia is slowed to a stop. The disk will not immediately stop, so if an over-current is detected again, the disk will already have some speed and ramp up to the tripping condition faster (Ref. 190). Lastly, the possibility of constructing a state-space model of the SSCB will be investigated.

The SMES model could be refined by creating a more sophisticated overvoltage protection scheme. The current scheme can create noise in the output response. The use of a surge arrester in the circuit could be studied as another means of protection.

The current source rectifiers and inverters still need to be studied to find a stable control scheme that minimizes the losses in the component. The control of advanced power electronics is an ongoing area of research. New approaches to the control of these types of converters will likely emerge in the near future. Updated control schemes can be incorporated into the base model to further test the current source converter topologies.

The most significant improvements to this system model can be achieved by creating a higher fidelity generator and motor models. This would entail detailed component modeling for the machines and then incorporating the new models into the existing system models. Fan maps can also be included in the model to better predict the speed or required torque for the motors.

Another area of improvement for the system model is increasing model speed. One possibility for decreasing simulation time is to use state-space models. However, the state-space models for the converters would average the response of the converter over several switching periods, and some of the dynamic response would be lost. Due to this problem, further study is needed to determine whether using the state-space models would accurately portray the response of the system.

8.0 Conclusions

Electrical system integration requirements are immature for revolutionary electric propulsion systems. As such, TeDP component technology development requires assumptions to be made regarding the voltage levels, regulation, and protection requirements when assessing concept performance. Therefore, this study represents an effort to provide initial justification for the selection of TeDP architecture voltage levels and limits. The system of interest for this study was the N3-X superconducting DC architecture. However, the models and tools developed in this study provide many of the building blocks for addressing voltage selection for variety of electric propulsion system architectures with varying requirements and compositions. As these tools are applied to maturing TeDP concepts, it is hoped that the methods applied in this study will begin to frame the development of voltage standards for airborne propulsive power systems.

The voltage envelopes are consistent throughout the electrical standards literature review. At the point of interface, the voltage can drop to zero for a period of time followed by a recover time and recovery limit. The boundaries of the transient and abnormal voltage regulation will be determined from the regulation and protection system's capabilities. Improvement in voltage regulation will come at the expense of adding filtering thereby increasing weight. The voltage quality may also be driven by requirements from operators and regulatory bodies to control issues such as EMI. The literature review on voltage standards also brought attention to specifying voltage and frequency together. This can be prudent as an overvoltage condition at the same time as an underfrequency condition can result in overfluxing of the electric machines which will lead to damaging eddy currents and excessive heating in the machine core. The voltage standards for isolated microgrids and for grids with a high penetration of distributed sources also defined the power factor of the loads in establishing voltage response during a transient. As load characteristics are better defined, the converter controls and filtering will be revisited to ensure that the converters meet the required voltage regulation. The IEEE recommended practice for MVDC power systems on ships provides several area of further work that will be necessary to create a voltage standard. Areas include the categorization of loads, limits of fault conditions on the equipment, stability studies and safety cases.

Parametric sizing models for all components within NASA's N3-X TeDP electrical system were generated and exercised to determine the optimal operating voltage for the system. Mass and efficiency sensitivity was evaluated for superconducting generators, AC and DC cable runs, power conversion equipment, superconducting fault current limiter, solid state circuit breakers, and a superconducting magnetic energy storage system. The combined sensitivity for component mass and efficiency were evaluated assuming general cryocooling mass sensitivity assumptions. For the baseline bi-polar DC architecture configuration, in all cases the optimal operating voltage was found to be less than ±4.5 kV. Systems which rely on converters for isolation and redundancy for recovery, as opposed to breakers and energy storage, the optimal voltage was found to be ±2 kV. Additionally, the system mass is insensitive to voltage on a fairly reasonable voltage range.

Observations and outstanding questions related to the TeDP system components modeled in this study provide potential areas of further consideration in the development of the electrical systems architecture.

8.1 Power Electronics

The preferred voltage ranges selected for this architecture are unique to the architecture selected and the component performance assumptions made. Voltage sensitivity analysis showed that the mass and efficiency of the semiconducting drive the voltage sensitivity of the overall systems. Considering mass penalties for cryocooling, the efficiency trends for IGBTs and diodes have the largest impact on mass

sensitivity. As such, for an airborne high power DC TeDP system, light weight and highly efficient power conversion equipment is a pacing technology.

Current Source Converters (CSCs) were chosen to rectify the AC generator voltage and invert the DC power to the propulsor motors. Current source converters use inductors to store energy and that architecture inherently limits the current giving the system an additional level of protection in the event of a fault. The source converters were unidirectional and the load converters where bi-directional. Both converter topologies showed the ideal voltage in the range between ±3 to ±6.5 kV. IGBTs do not have the ability to block higher voltages so as the voltage increased more IGBTs were needed to effectively block the voltage, increasing the weight.

At low voltages, the current in the system required multiple IGBTs to be in parallel driving up the weight. Some of the IGBT and diode parameters used to model the weight and efficiency sensitivities were derived from extrapolating normally conducting devices down to superconducting temperatures so using modelling data near the freeze out temperature would improve the modelling. The freeze out temperature is the temperature low temperature beyond which semiconductors will not function and is typically determined by the ionization energy of the dopants as well as the doping concentration of the semiconductors (Ref. 191). Heavy doping may allow devices to operate below the freeze out temperature and allow semiconducting devices to operate in the same environment as the rest of the TeDP power system. Further characterization of semiconducting materials and types over a range of temperature will provide more model fidelity. This additional characterization would also work to reducing the switching losses as the energy turn on and turn off is directly related to the energy losses of the IGBTs. Models that use first principles to model the behavior of IGBTs and diodes at low temperature will improve the weight and efficiency estimates of the converters. Finally, the converter models will need to incorporate filtering elements to reduce Electronic Magnetic Interference (EMI) to a reasonable level and maintain power quality. Filtering can add significant weight to the converters but can also be used to improve system stability.

8.2 Protection

The protection of the superconducting TeDP electrical system will be a challenge due to speed that faults and disturbances occur while maintaining power to the propulsors. The speed that a circuit breaker can interrupt a fault is directly related to the amount of energy that requires dissipation during a disturbance. The slower the fault interruption, the more energy has to be absorbed by the cryogenic system. In turn, leading to increases in the size of the cryo-system. Also, fast circuit breakers may reduce the number of required fault current limiters or eliminate them altogether. Solid-state circuit breakers (SSCBs) were chosen for this study due to the fast operating time and ability to operate at near cryogenic temperatures. The drawback to SSCBs is that they have higher conduction resistances than electromagnetic circuit breakers or hybrid circuit breakers. The higher losses of SSCB may be sufficient to perform a trade in the efficiency of the system during normal operation and the efficiency penalty of carrying extra weight from a larger cryo-system and SFCLs if slower circuit breakers are used. The dual use of the converters as regulation and protection may eliminate both the circuit breakers and fault current limiters though some isolation equipment may still need to be necessary to physically separate electric machines and energy storage from the network for maintenance or after reconfiguration.

8.3 Energy Storage

The dynamic models are also crucial in identifying the requirements on energy storage devices. For this architecture, the role of energy storage in this TeDP architecture was limited to that of an uninterrupted power system to support the loads during a source fault. In order to eliminate interfaces between room temperature and cryogenic electrical systems, superconducting magnetic energy storage

was selected for UPS power. The SMES benefits from the ability to rapidly discharge the stored energy and is shown to exhibit fairly high energy densities when assuming the use of high strength structural materials. This energy density increases with the amount of energy stored. Additional work is necessary to develop discharge management and control logic so the SMES can provide DC power to the loads during a fault in a regulated manner.

The SMES is attractive as a high energy and power dense system which operates at cryogenic temperatures. However, it also suffers from several deficiencies. First, the weight of the power electronics to allow for charging and discharging of the SMES introduce detriments to the overall system mass. Second, SMES cryocooling requirements also increase the overall system mass. Third, the volume of a SMES device may be limited for a high energy airborne application. Fourth, the mass and length of the superconductor for high energy, high voltage, SMES devices may introduce prohibitive costs and manufacturing challenges. Lastly, concepts for fault tolerant SMES designs are needed which can dissipate the massive amounts of energy within the inductive coil in a controlled fashion when a fault occurs.

8.4 Distribution

Cables systems are practically negligible in contributions to mass and efficiency for this DC system. Additionally, as with all the other systems, the insulation and cryogenic cooling systems contribute more to the overall mass than the superconductor and dielectric insulation. As such, for both AC and DC superconductor, the ratio of operating and fault currents to the critical current can be selected so as to minimize the losses at a very small detriment to cable weight. The N3-X architecture concept was prescribed with a DC distribution system. As such, the losses and masses associated with power conversion were adopted in the system. However, by operating at higher critical current ratios of the distribution cables, superconducting AC TeDP electrical system concepts may begin to look more promising. However, these concepts would require additional analysis of the implications of regulation, protection, and recovery.

8.5 Dynamic Modeling

During the voltage sensitivity analysis assumptions were made regarding the overcurrent and regulation requirements for the system. Therefore, dynamic models of the entire system were made to define voltage regulation requirements and simulate critical fault scenarios to determine the isolation, protection, and recovery strategies for the system.

The dynamic models developed in this project will be paramount in establishing the fault current and undervoltage that the equipment will see during disturbances and how fast those faults will propagate through the system. That will help future work in sizing the protection equipment and the speed at which protection equipment needs to act to isolate failures. Initially the dynamic models will help set the limits around current and voltage during faults so that the faulted lines are removed from operation and the models can be then used to tune the converter controls and protection settings so that the system does not disconnect for high motor start currents. Protection zones can be established once the dynamic models can give indication of speed of failures and the usability of power electronics in the protection scheme. The analysis of reducing the size and weight of the system using different converter topologies and control schemes to determine if it is viable to use the power electronics for protection will utilize dynamic models for failure and recovery scenarios.

The dynamic models may also be used to study the impact that converter filtering and distribution line impedances have on stability. Literature review of DC systems showed the importance of understanding the system impedances especially around bi-directional converters. The fact that the current can flow in both directions increases the risks of instability and the possibility of using those converters for protection in both directions will requires careful study.

Appendix A.—Acronyms and Abbreviations

AC	Alternating current
BPS	Bypass switch
DC	Direct current
CSC	Current-source converter
EDR	Engineering Department Report
EMCB	Electromechanical circuit breaker
EPACS	Electrical Power and Control Systems
EPRI	Electric Power Research Institute
ESR	Equivalent series resistance
ETL	Energy Transfer Line
ETO	Emitter turn-off thyristor
GE	General Electric
GTO	Gate turn-off thyristor
HCB	Hybrid circuit breaker
I.D.	Inner diameter
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated gate bipolar transistors
IGCT	Integrated gate-commutated thyristor
J_c	Critical current density
J_e	Engineering critical current density
kV	Kilovolt
MGT	MOS gated thyristor
MCT	MOS controlled thyristor
MOS	Metal Oxide Semiconductor
MOV	Metal oxide varistor
NERC	North American Electric Reliability Corporation
NPT	Non-punch through
O.D.	Outer diameter
POI	Point of interconnection
PSS	Power system stabilizer
PT	Punch through
PWM	Pulse-width modulation
RMS	Root Mean Square
RTAPS	Research and Technology for Aerospace Propulsion Systems
SCR	Silicon Controller Rectifier
SEI	Sumitomo Electric Industries
SFCL	Superconducting fault-current limiters
SMES	Superconducting Magnetic Energy Storage
SSCB	Solid-state circuit breaker

TeDP	Turboelectric Distributed Propulsion
TG	Trench-gate
TRL	Technology readiness level
UPS	Uninterrupted power supply
UTC	University Technology Center
Vdc	Volts direct current
VSC	Voltage source converter

Appendix B.—IGBT Data

TABLE B.1.—ROOM TEMPERATURE IGBT DATA FOR EXISTING IGBTS.

Manufacturer	ABB	ABB	Infineon	Mitsubishi	Mitsubishi	Mitsubishi	Mitsubishi	Mitsubishi	Mitsubishi	Mitsubishi	Mitsubishi	Mitsubishi	Mitsubishi
IGBT Part Number	5SNA0600G650100	5SNA1200G450300	FZ600R65KE3	CM1200HA-50H	CM750HG-130R	CM900HG-90H	CM450DY-24S	CM800HB-66H	CM900HC-90H	CM1500HC-66R	CM1200HA-34H	CM1200HC-66H	CM200HG-130H
Nominal current, A	600	1200	600	1200	750	900	450	800	900	1500	1200	1200	200
Over current, A	1200	2400	1200	2400	1500	1800	900	1600	1800	3000	2400	2400	400
Surge current, A	6000	9000											
Over current withstand duration, ms	10	10	1										
Nominal blocking voltage, kV	6.5	4.5	6.5	2.5	6.5	4.5	1.2	3.3	4.5	3.3	1.7	3.3	6.5
Conduction voltage drop, V	3.5	3	3	3	5	3.3	2	4.2	3.5	3.2	3	3.5	4.3
Current rating for conduction voltage drop, A	600	1200	600	1200	750	900	450	800	800	1500	1200	1200	200
Gate drive resistance, Ω	3.9	1.5	1.3	2.5	3.9	10	8	2.5	10	1.6	1.6	1.6	30
Time to turn off, µs	2.16	2.88	7.7	3.5	8	7.2	0.9	3.5	7.2	3	2.6	3.5	8.7
Time to turn on, µs	0.91	0.96	1.03	3.6	1.23	3.6	1	3.6	3.6	1.28	2.7	2.6	1.55
Turn off energy, J	1.95	4.96	2.9	0.86	3.1	2.5	0.048	1.2	2.5	2	0.45	1.55	1.2
Turn on energy, J	3.8	3.08	3.4	1.5	3.35	4.2	0.0549	1.7	4.2	2.1	0.45	1.6	1.5
Turn on di/dt, A/µs	2600	4800	2.9	1.2									
Overcurrent withstand relative to nominal	2	2	2	2	2	2	2	2	2	2	2	2	2
Conduction loss - DC/DC duty cycle, W[a]	1050.00	1800.00	900.00	1800.00	1875.00	1485.00	450.00	1680.00	1771.88	2400.00	1800.00	2100.00	430.00
Conduction loss - PWM for inverter/rectifier, W[b]	1073.62	1840.50	920.25	1840.50	1917.18	1518.41	460.12	1717.80	1780.57	2453.99	1840.50	2147.25	439.67
Switching loss - DC/DC converter, W[c]	57500.00	80400.00	63000.00	23600.00	64500.00	67000.00	1029.00	29000.00	67000.00	41000.00	9000.00	31500.00	27000.00
Switching loss - PWM control, W[c]	18302.82	25592.11	20053.52	7512.11	20530.99	21326.76	327.54	9230.99	21326.76	13050.71	2864.79	10026.76	8594.37
Semiconductor power loss - DC/DC converter, W	58550.00	82200.00	63900.00	25400.00	66375.00	68485.00	1479.00	30680.00	68771.88	43400.00	10800.00	33600.00	27430.00
Semiconductor power loss - PWM control, W	19376.44	27432.61	20973.77	9352.61	22448.17	22845.17	787.66	10948.78	23107.33	15504.70	4705.28	12174.01	9034.04
Maximum collector dissipation, W	11900.00	10500.00	12500.00	10400.00	10400.00	11300.00	3330.00	10400.00	11900.00	15600.00		14700.00	2900.00
Mass, kg	1.76	1.76	1.4	2.2	1.4	1.35	0.58	1.5	1.5	1.2	1.5	1.5	0.5
Freewheeling diode	**ABB**	**ABB**	**Infineon**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**	**Mitsubishi**
Part Number	5SNA0600G650100		FZ600R65KE3	CM1200HA-50H	CM750HG-130R	CM900HG-90H			CM900HC-90H	CM1500HC-66R	CM1200HA-34H	CM1200HC-66H	CM200HG-130H
Forward voltage, V	3.2		3	2.8	3.3	4			4.8	2.2	2.4	2.8	4
Rated current for forward voltage, A	600		600	1200	750	900			900	1500	1200	1200	200
Reverse recovery energy, J	1.1		1.1		1	1			1	1.05			0.7
Approx. diode resistance, Ω	0.005333333		0.005	0.002333333	0.0044	0.004444444			0.005333333	0.001466667	0.002	0.002333333	0.02

Data used to populate this table is from datasheets available from the manufacturer's website (accessed Jan-March 2014).

[a] Calculated for DC/DC Duty Cycle = 0.5

[b] Calculated for PWM duty = -0.64 (negative for rectifier operation)

[c] Calculated for switching frequency = 10 kHz

Appendix C.—Dynamic Models

An overview of the dynamic nominal recovery model is shown in this appendix. The right side of the architecture is emulated as a source in this case. The color-coded boxes in Figure C.1 refer to Figure C.2 to Figure C.8, which show that section of the model in more detail.

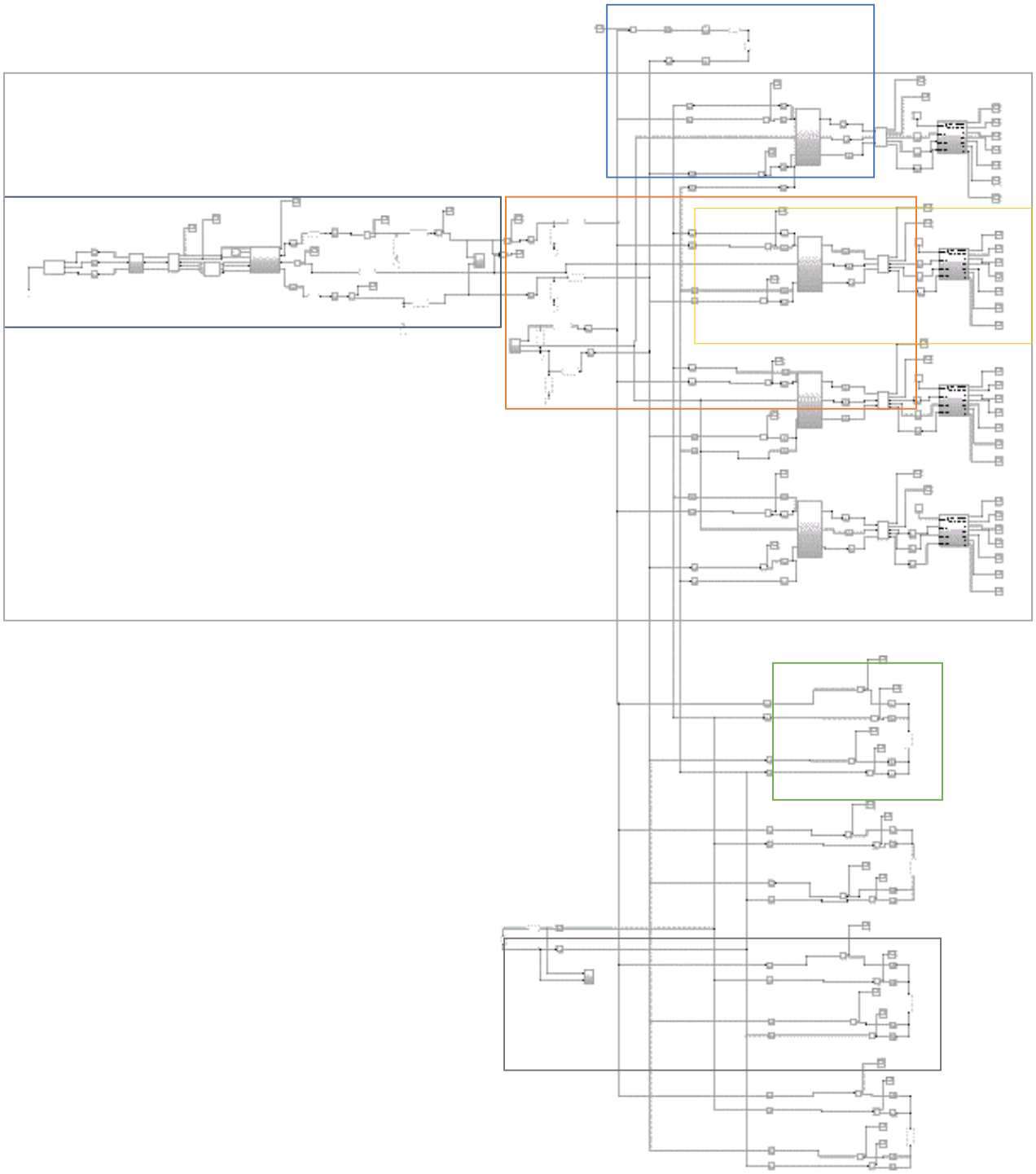


Figure C.1.—Nominal Recovery Model.

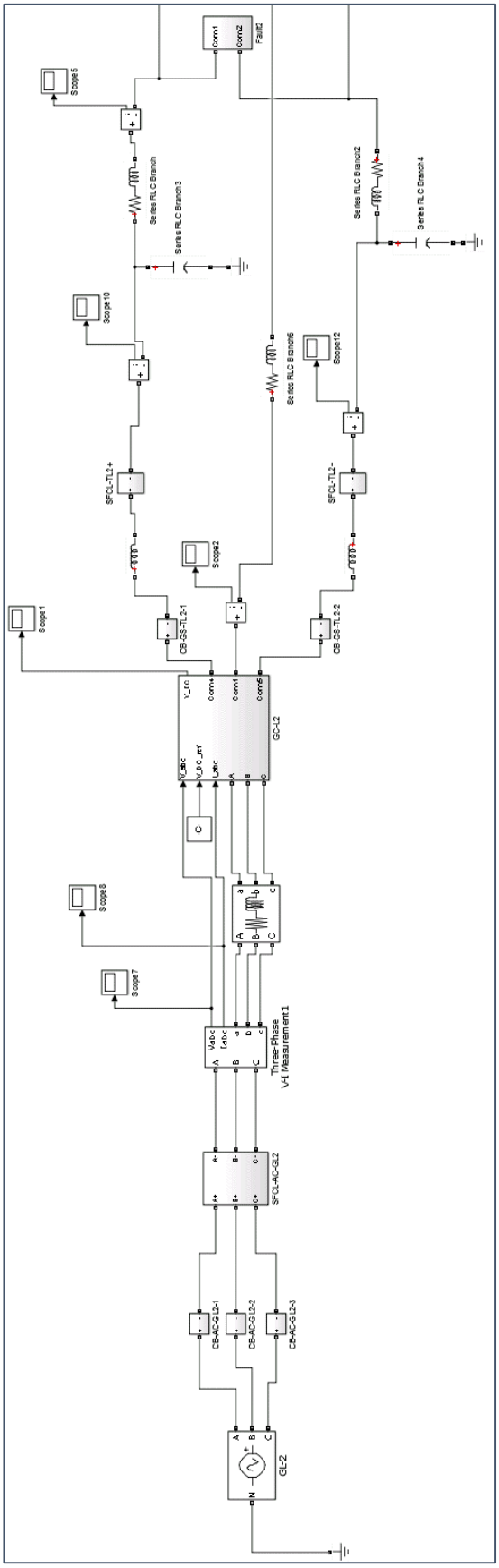


Figure C.2.—Source to Line Fault.

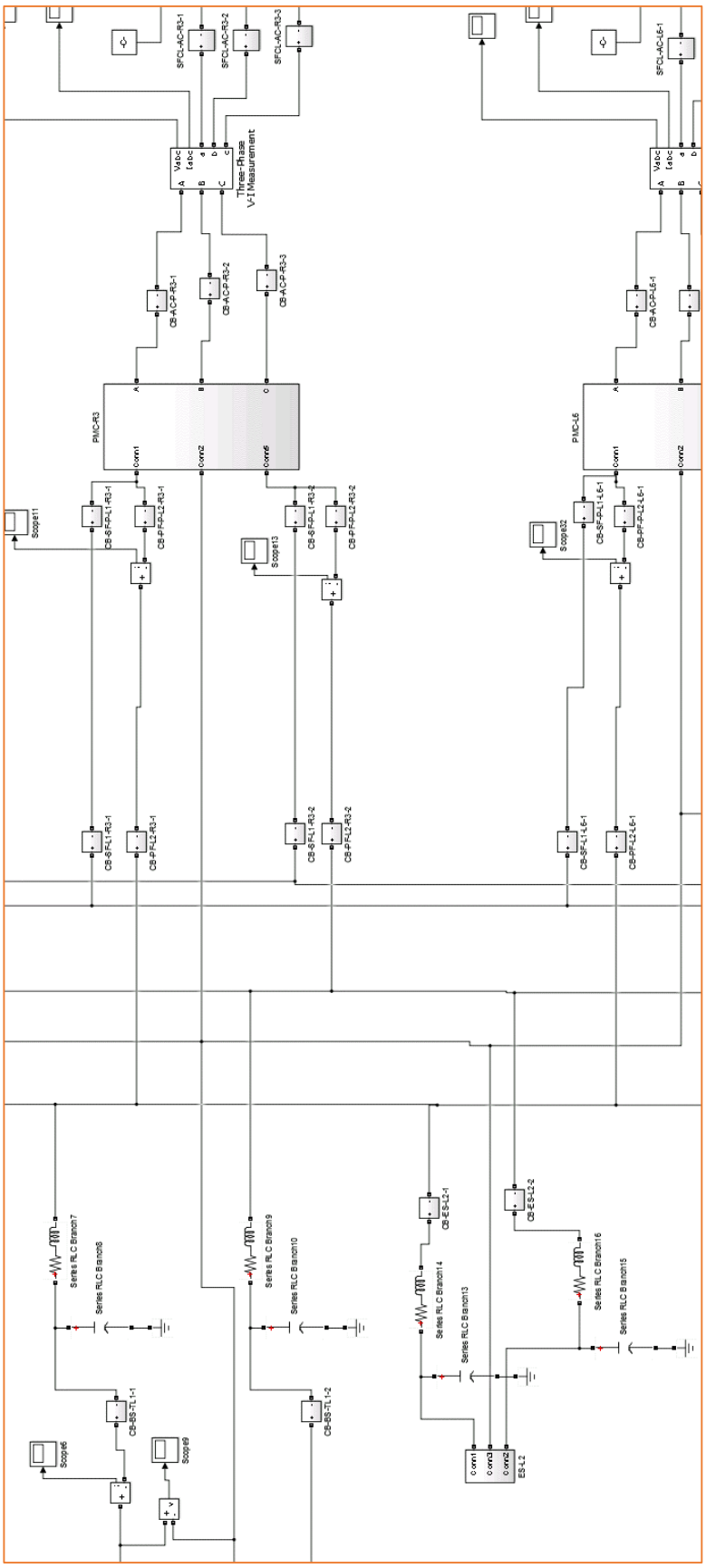


Figure C.3.—Line Fault and Energy Storage.

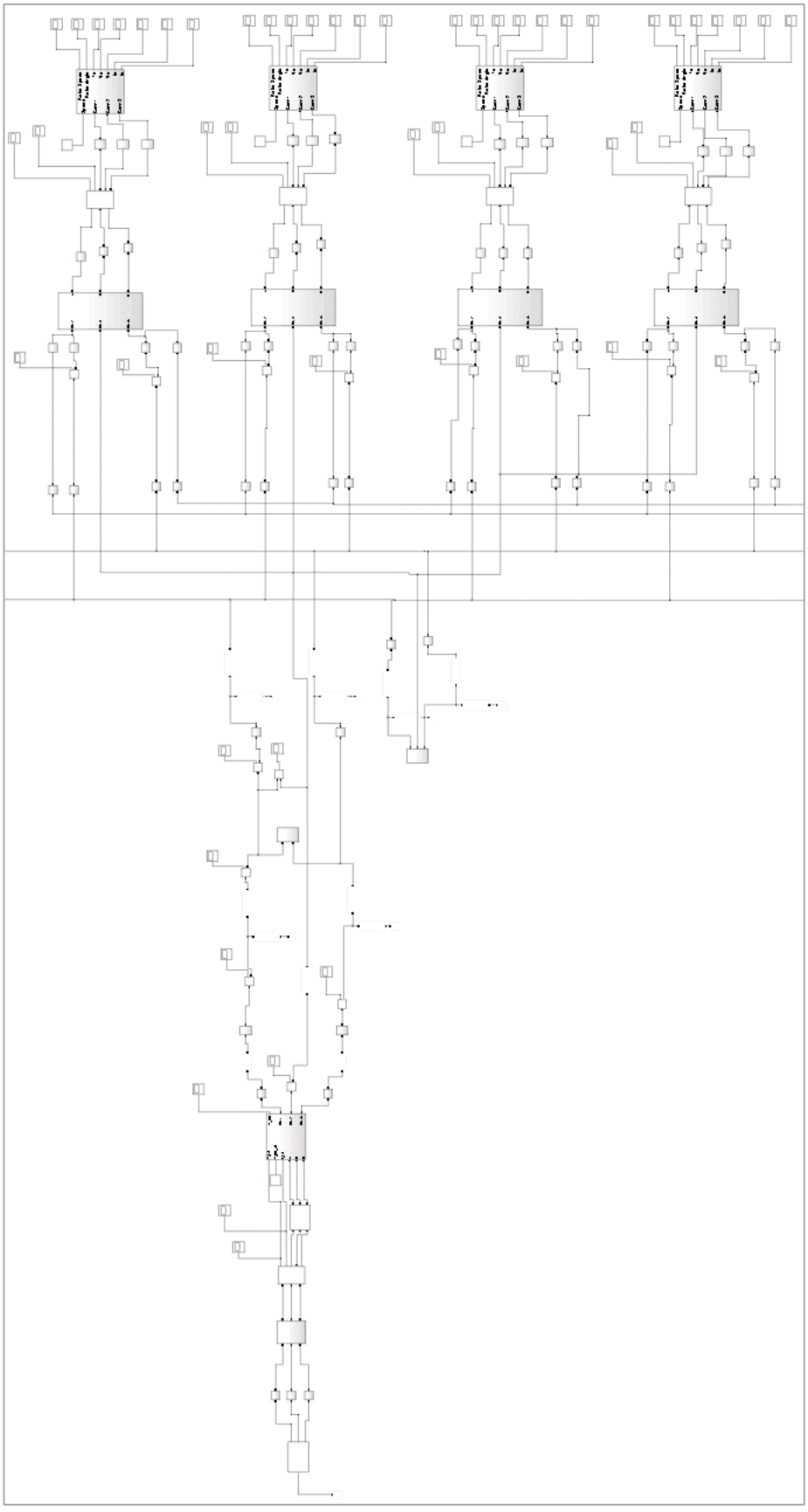


Figure C.4.—L-2 Branch.

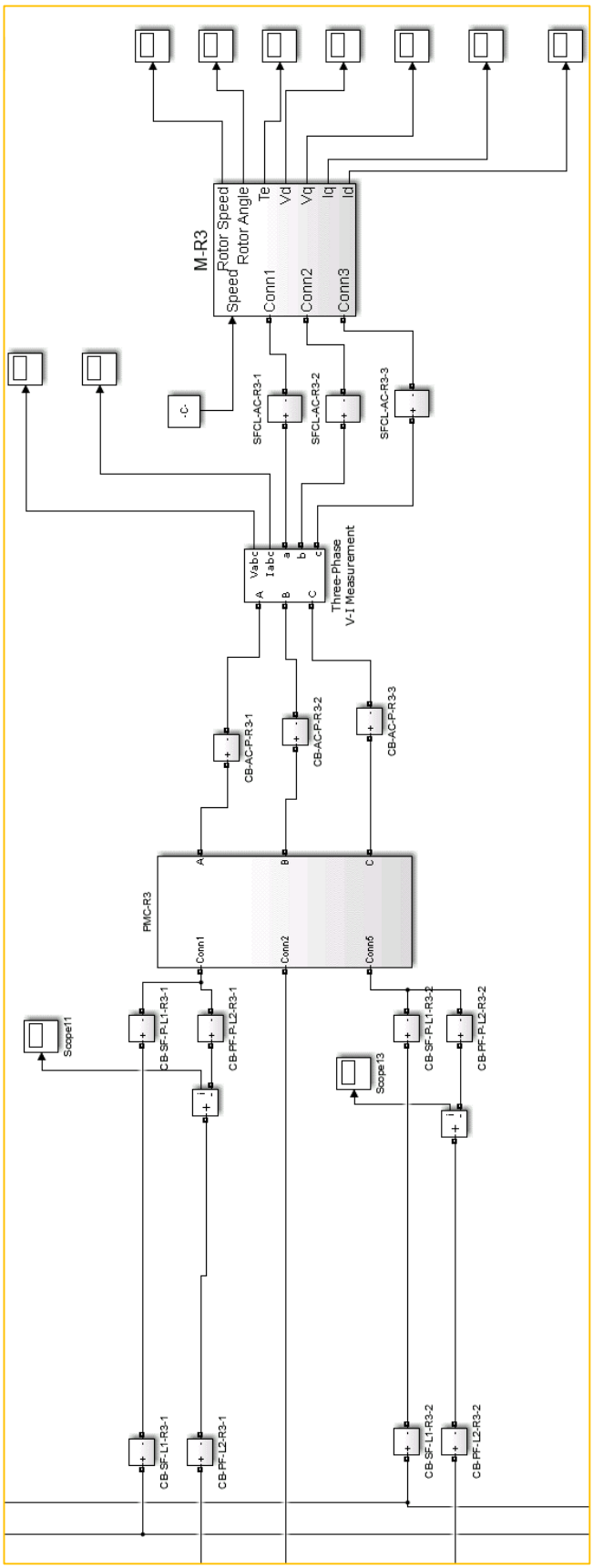


Figure C.5.—Inverter and Motor Connection.

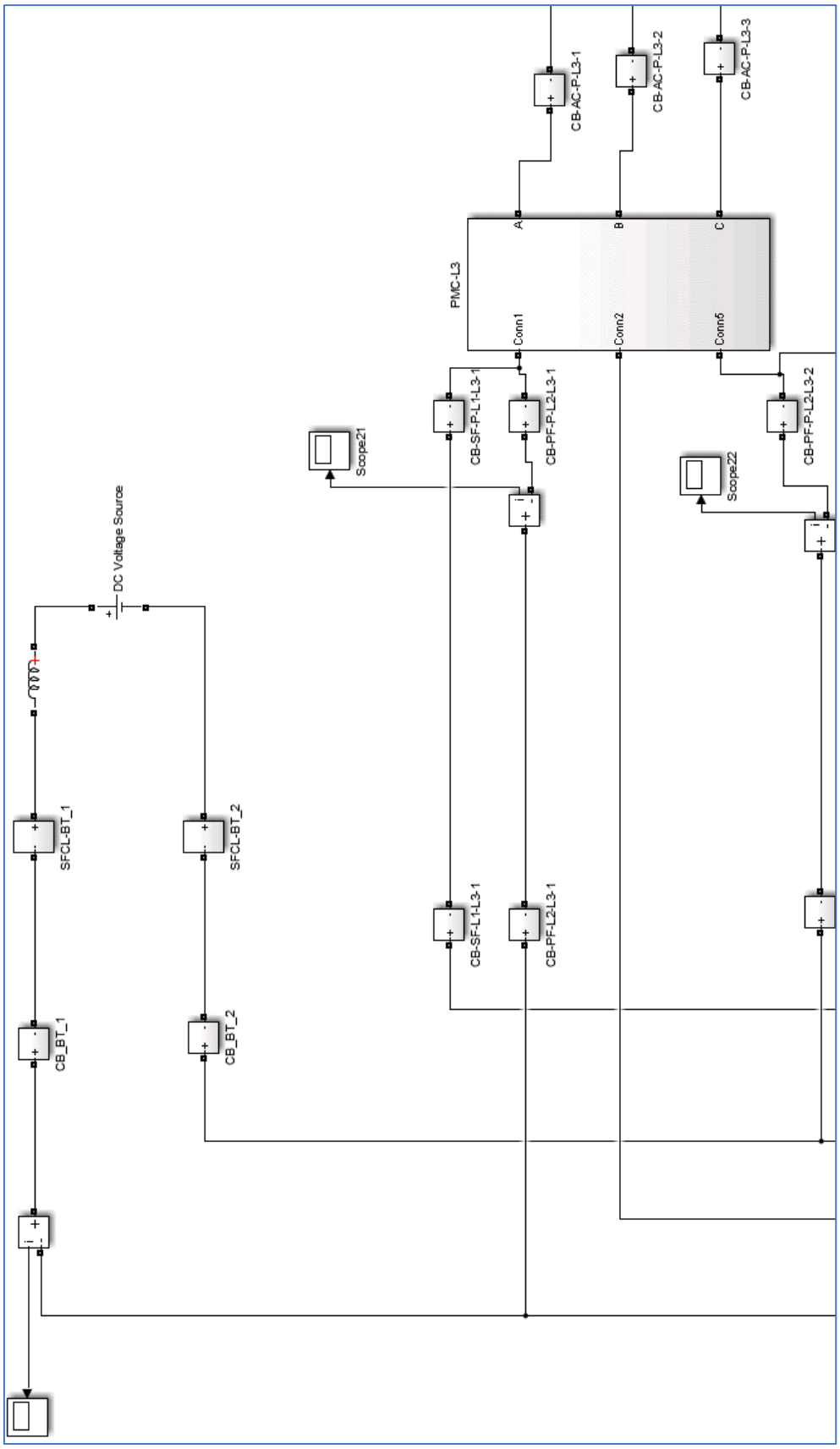


Figure C.6.—Right Engine Emulation.

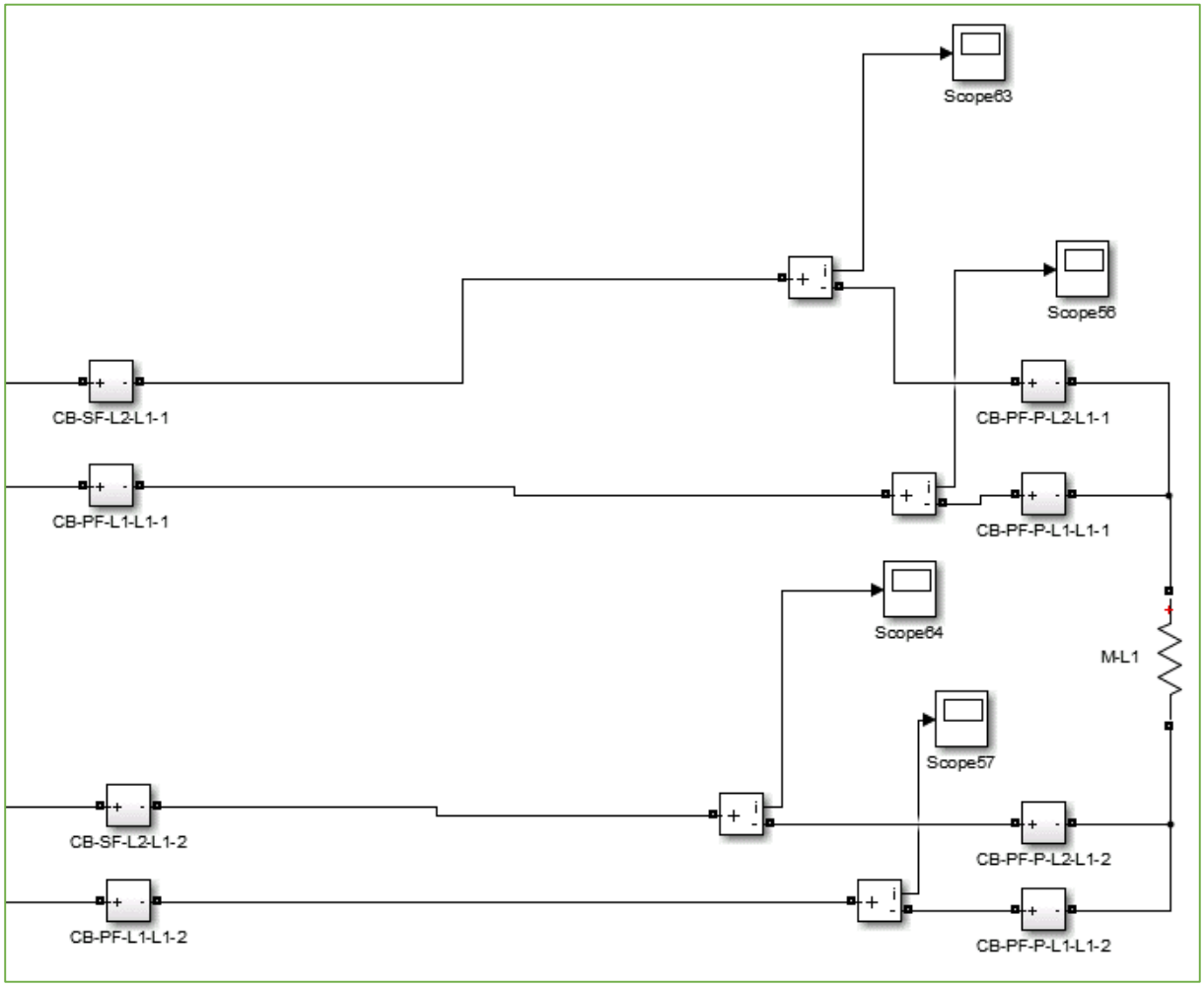


Figure C.7.—L-1 Load Emulation.

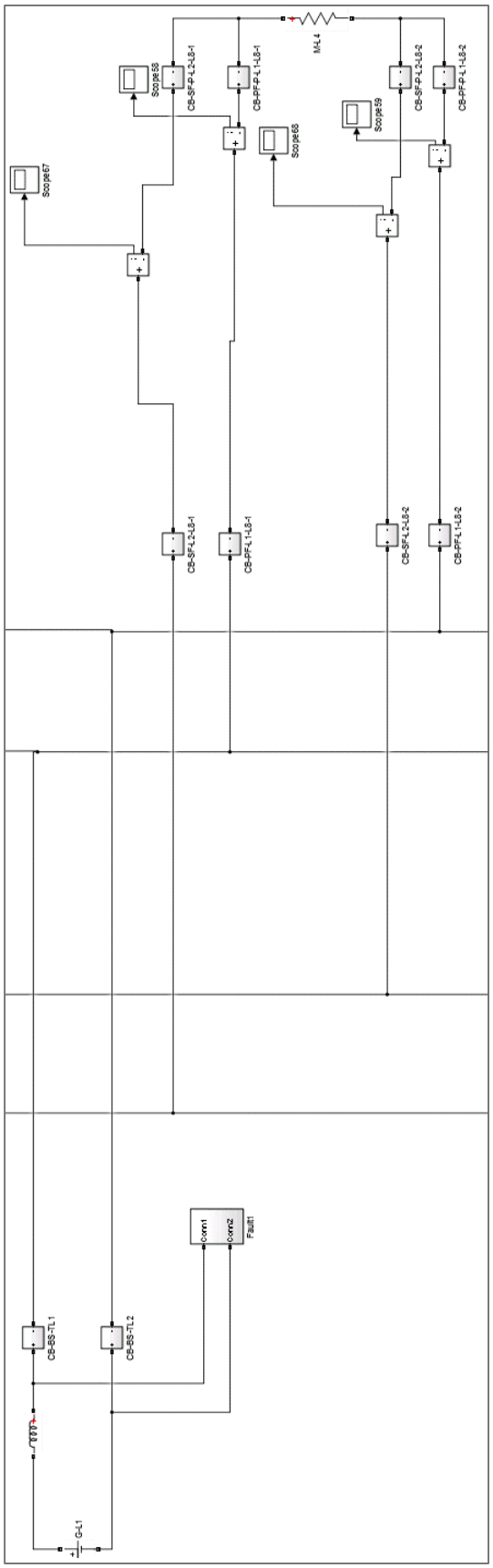


Figure C.8.—L-1 Source and Load Emulation.

Appendix D.—Strathclyde Report

Sensitivity models of system components of an example N3-X TeDP aircraft electrical network

Author:

Dr. Catherine Jones.

Co-author:

Dr. Patrick Norman

Strathclyde UTC Approval and Distribution:

Dr. Stuart Galloway

R-R Distribution:
Mike Armstrong (Rolls-Royce North American Technologies)
Andrew Bollman (Rolls-Royce North American Technologies)
Mark Blackwelder (Rolls-Royce North American Technologies)
James Bossard (Rolls-Royce EPACS Bristol)

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Contents

1 Glossary

EPACS	Electrical power engineering and control systems
UTC	University technology centre
RTAPS	Research and technology for aerospace propulsion
TeDP	Turboelectric distributed propulsion
TRL	Technology readiness level
P-diagram	Parametric diagram
SFCL	Superconducting fault current limiter
SSCB	Solid state circuit breaker
FCR	Fault current ratio
SMES	Superconducting magnetic energy storage
CPQ	Compressive quality factor
B-field	Magnetic field

2 Executive Summary

As part of the RTAPS II programme, a scalable sensitivity model of an example turboelectric distributed propulsion (TeDP) architecture has been developed by Strathclyde UTC, utilising data provided by Rolls-Royce North American Technologies. The final model, which is presented in this document, is a tool which can be used to analyse the sensitivity and scalability of the components within the model architecture, in terms of their efficiency and weight, primarily to different system voltage levels, but also to other variables such as fault current ratings or fault response time.

This report describes the full sensitivity model, including the individual component models and the approach and method used to integrate these component models together to form the fully integrated model. The model at present uses data for when the TeDP system is running at maximum power, for example during the take-off phase of flight.

The report presents preliminary results from sensitivity studies carried out using the model to investigate the sensitivity of the TeDP system to different DC voltage levels. In addition a short study is presented to investigate the influence of certain components on the optimum DC voltage operating point of a TeDP electrical system.

3 Introduction and background

3.1 Position within the RTAPS II project

The 2014 statement of work for the University of Strathclyde UTC supports the fulfilment of Rolls-Royce North American Technologies's contract with NASA for the Research and Technology for Aerospace Propulsion (RTAPS) project [1]. The goal of the RTAPS project is to enumerate, characterise and evaluate the critical dynamic and safety issues for the electrical grid for electrical propulsion of an N+3 TeDP aircraft [2]. N+3 aircraft are expected to reach TRL 4-6 by 2025 [3].

3.2 Aims and objectives of this study

This study aims to develop a fully integrated, sensitivity model of the example TeDP architecture, shown in Figure 1 below. The simulation model developed is a tool which enables the sensitivity of the weight and efficiency of the example TeDP system to variations in certain operating conditions, such as DC bus voltage levels, to be investigated. Ultimately the model therefore acts as a tool for the system parameters to be optimised for weight and efficiency. The data used in the model developed has been for maximum power conditions, rather than nominal power. Therefore the model developed returns the cryogenic system power requirements and electrical losses for a period of flight when maximum power is required, for example at take-off.

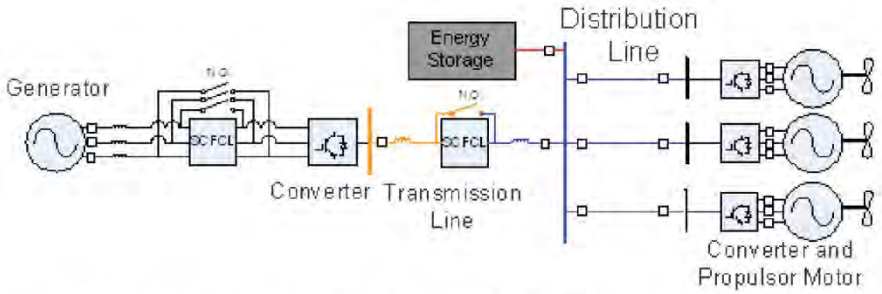


Figure 1: Example TeDP architecture used for the RTAPS II sensitivity study.

By inspection of Figure 1, it can be seen that the example TeDP architecture consists of a number of different electrical components.

These have been identified as:

- Cables (AC and DC)
- Generator
- Motor
- Rectifier
- Inverter
- Energy storage: SMES with DC-DC converter
- Superconducting fault current limiter (SFCL)
- Solid state circuit breakers (SSCBs)

Figure 2 is a more detailed diagram of the example architecture shown in Figure 1. From this diagram it can be seen that the architecture can be divided up into 4 distinct subsections: 12.5MW AC ("AC Generation"), 12.5 MW DC ("DC transmission"), 2.5 MW DC ("DC Distribution") and 2.5 MW AC ("AC Motor").

This report will describe the sensitivity model which has been built of this example TeDP architecture, discuss its capability and present some example results from the model.

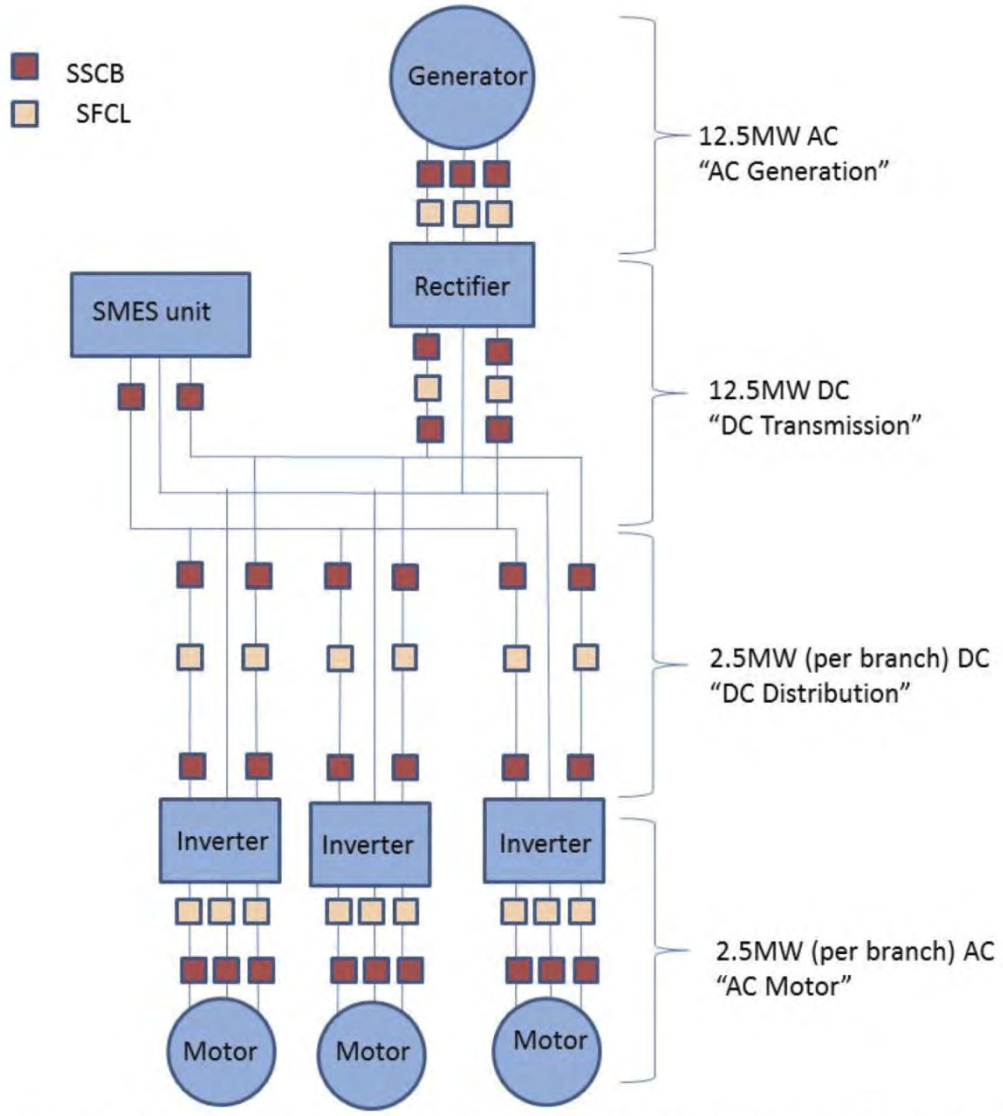


Figure 2: Detailed diagram of the example TeDP architecture, showing the superconducting fault current limiter (SFCL) and SSCB devices.

4 The full system sensitivity model

4.1 Methodology

4.1.1 The full system model and parametric diagrams

As described in Section 3, the example TeDP architecture is made up from 6 main components, which are then operating in one of 4 different main sections of the TeDP architecture. Therefore the approach chosen to developing the model has been to develop a component block for each of the identified architecture components. These component blocks are then integrated together to form a full system model. Hence a generic approach to developing these component models has been taken to allow the blocks to be integrated together to form a model representative of the full system.

4.1.2 Parametric Diagrams

Rolls-Royce have, for each of the components, developed a parametric diagram (P-diagram) [4]. These component level P-diagrams have then been used to build up a full system model, which splits into two main sections: an architecture section and a protection section. The P-diagrams have been used as a starting point for a frame work for developing a sensitivity model of a TeDP architecture. The choice of components to model and how they fit together in the final sensitivity model is based on the P-diagrams.

Figure 3 shows the full system P-diagram. By inspection it can be seen that the architecture block consists of the cable, electrical machines (generator/motor), power electronics (rectifier/inverter) and energy storage. The protection block comprises the bus ties, circuit breakers and SFCLs. The P-diagrams for the architecture components are shown in Figure 4, and the P-diagrams for the protection components are shown in Figure 5.

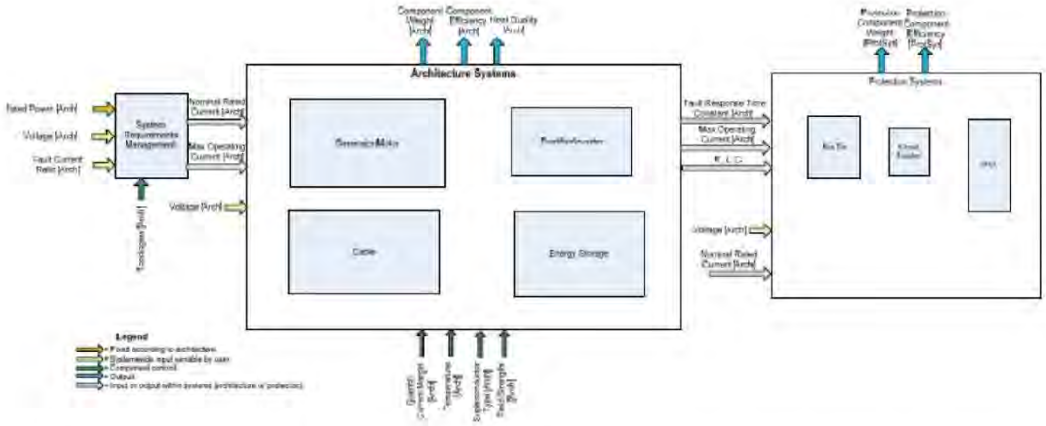


Figure 3: Full system P-diagram showing the architecture and protection blocks and the components which make up these blocks.

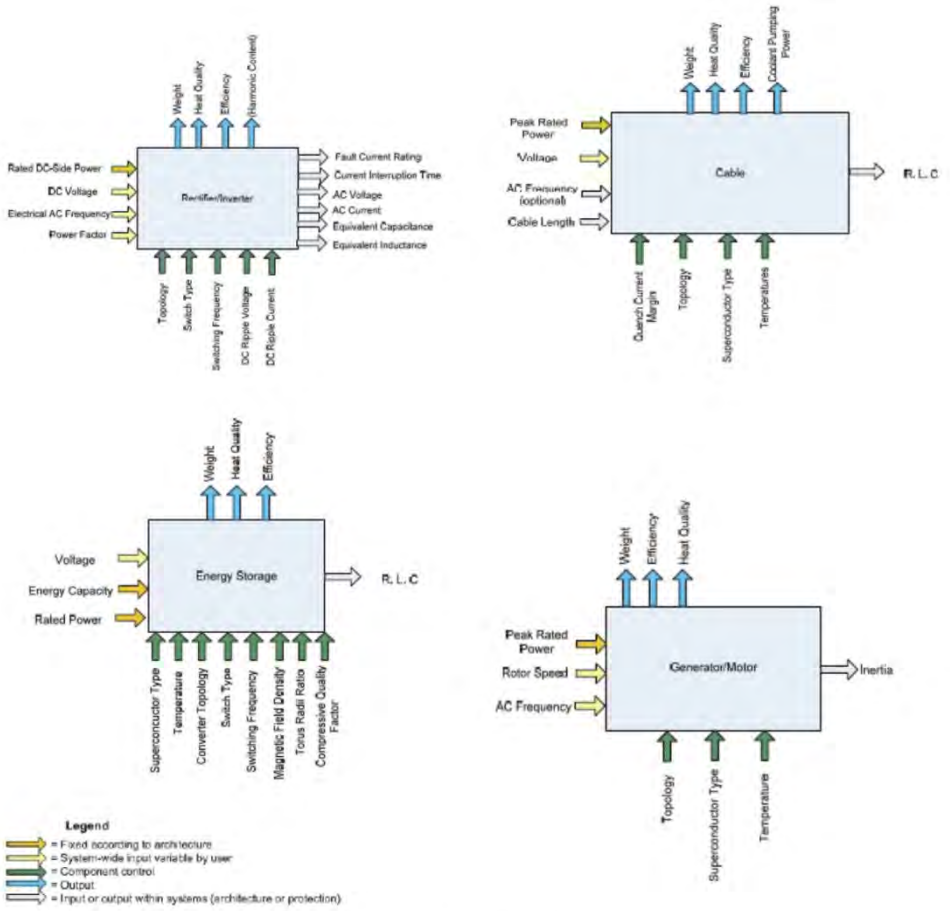


Figure 4: P-diagrams for the architecture components.

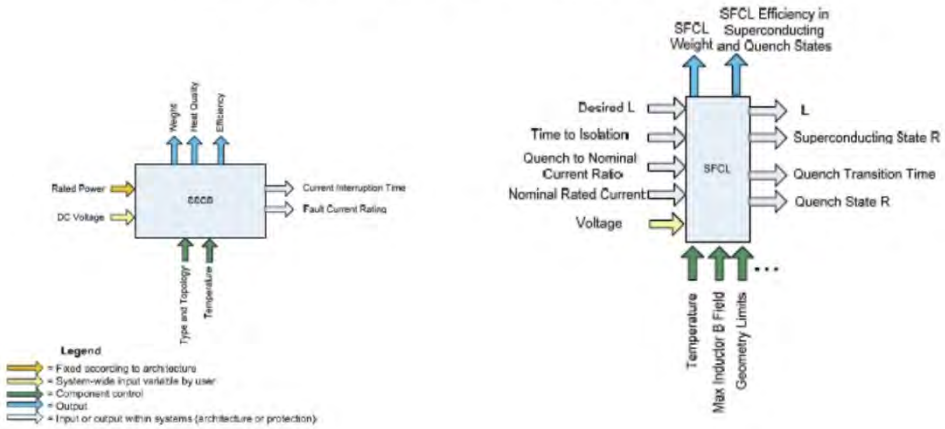


Figure 5: P-diagrams for the protection system components.

The P-diagrams form the full system using a modular, hierarchical structure. Therefore the

sensitivity model developed in Matlab has also followed this hierarchical structure, as shown in Figure 6. To achieve this, a model of each of the 6 components identified has been developed, and then these have been grouped together to form an architecture and protection block. These two blocks then form the full system. Key system variables which are input to the blocks include voltage, power, AC frequency and fault current ratio (FCR). The model returns the total mass of the electrical and cryogenic systems, the electrical losses and the power required by the cryogenic system. The efficiency of the system can be calculated from the total electrical losses and the input power from the generator, as will be described in Section 4.2.

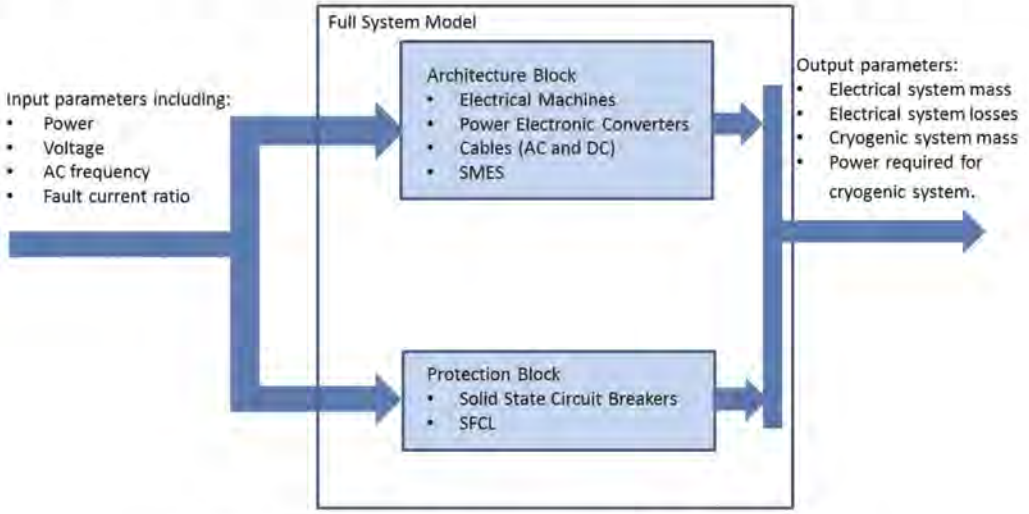


Figure 6: Block diagram of the structure of the full system model.

4.2 Component Models

4.2.1 Overview of the component models

As discussed in Section 4.1, a generic approach was taken for developing the component models to enable the blocks to be integrated together to form the full system sensitivity model. Each component block has been developed to have similar structure and functionality. Therefore a standard block architecture has been developed, and then this has subsequently been adapted as appropriate for each of the six component blocks.

The inputs to the component models take two broad forms: either an input is a set condition, for which there will be a distinct data set (for example: a set of data for when a particular coolant is used at a particular power rating), or it is an input which requires interpolation between different values for that variable (and possibly other variables, for example: voltage, FCR and AC frequency). The models have been developed in Matlab Simulink, with data read in from MS Excel spreadsheet files using Matlab scripts.

The blocks are hierarchical in structure. The generic block structure to select an output value for a particular set of input variables is shown in Figure 7. In this structure, non-interpolated values are used to choose a particular look-up table of data specific for those values. For example, the top level, level 1, could be choice of coolant and level 2 could be the power rating. The number of levels ("y" in Figure 7) will vary depending on the number of set conditions which must be considered for each output variable within a block. The number of

inputs to the data look-up tables ranges between one and three inputs and varies between component models. The look-up tables interpolate linearly between these data points, and will extrapolate linearly if the input data is outwith the ranges of the data points within the look-up tables.

The data provided for different components, indicates their sensitivity and insensitivity to a number of variables. Therefore, the same input variables are not used for all component blocks and the variables which are interpolated between in look-up tables also are not consistent between different component blocks.

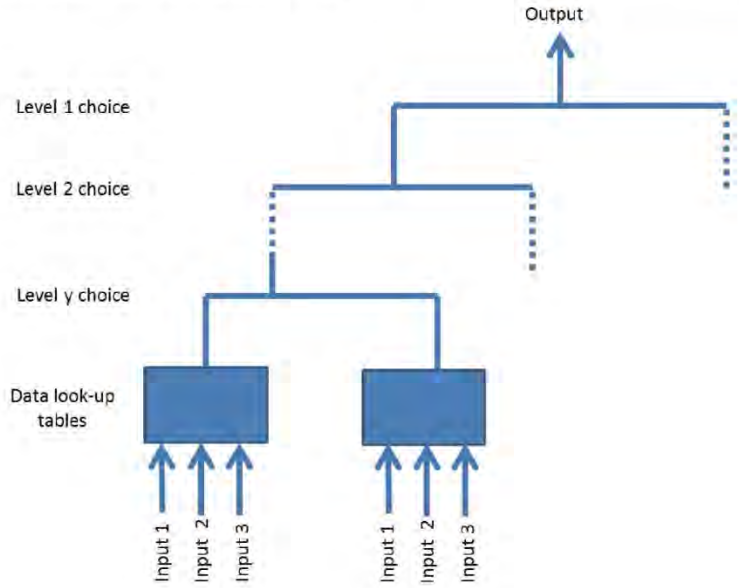


Figure 7: Generic hierarchical component block structure to select particular output values from a given set of conditions and input variables.

In order to implement this in Matlab Simulink, a mask has been created for the top level of each component block in Matlab Simulink. Variables, which are interpolated in data sets within the model, are set as inputs to the mask. These are connected to look-up tables within the model. For each component block, the parameters for the block that determine which set of data to use are set in the top level mask of that particular block.

For each component block the weight of the electrical and cryogenic system, the electrical losses and the power required by the cryogenic system is returned. The efficiency of the full system is subsequently calculated using Equation 1, as a function of the input power, Pin, and the output power, P_{out}.

$$\eta_{full\ system} = \frac{P_{out}}{P_{in}} = \frac{P_{gen} - P_{losses}}{P_{gen}} \quad (1)$$

Where P_{losses} are the total electrical losses in the system and P_{gen} is the input power to the system from the generator.

The efficiencies of individual component blocks are not calculated, but if this were required, this could be achieved using Equation 1, using the input power to the component and the electrical losses incurred in the component.

4.3 Description of component blocks

4.3.1 Power Converter (rectifier, inverter)

The power converter block determines the electrical system weight, cryogenic system weight, electrical losses and cryogenic system power requirements of the power electronic converters used. The power electronics in the TeDP architecture are not superconducting, but are expected to operate at a low temperature of around 100K. Hence a cryogenic system is present to keep the power electronics operating at this temperature, which has a weight and power requirements. These are calculated using Equations 2 and 3 below.

$$P_{cryo} = \dot{Q}\frac{(T_{amb} - T_{cool})}{T_{cool}} * \eta_{carnot} \qquad (2)$$

Where P_{cryo} is the power requirement of the cryocooler to keep the system at the desired temperature (T_{cool}) of 100K in an ambient temperature (T_{amb}) of 300K. The heat to be removed by the cryocooler is the heat from switching losses in the power electronics (Q) and the Carnot efficiency (η_{carnot}) (30%).

$$Mass = kP_{cryo} \qquad (3)$$

Where P_{cryo} is calculated using Equation 2 and k is 3kg/kW.

The power converter block has two levels: upper and lower. The upper level (shown in Figure 8) calculates the total electrical weight and losses, along with the cryogenic cooler power requirements and weight. The lower level blocks are the actual converter sensitivity blocks, the detail of which is shown in Figure 9, which return the weight and losses for a converter operating at a particular power rating and switching frequency. These blocks are called "12.5MW power sensitivity block" and "2.5MW power sensitivity block" in Figure 8.

The number of high power (12.5MW) and low power (2.5MW) converters are set at the mask for the top level of the converter block, as shown in Figure 10. The number of 2.5MW converters is set to be the same as the number of motors in the architecture, as one converter is required for each motor. For the example architecture considered, this is 3. The number of 12.5MW converters is set to match the number of generators in the architecture. For the example architecture considered, this is 1. The switching frequency is also set in the top level mask. This has been set at present to 5kHz, but could be set to 10kHz, 15kHz or 20kHz.

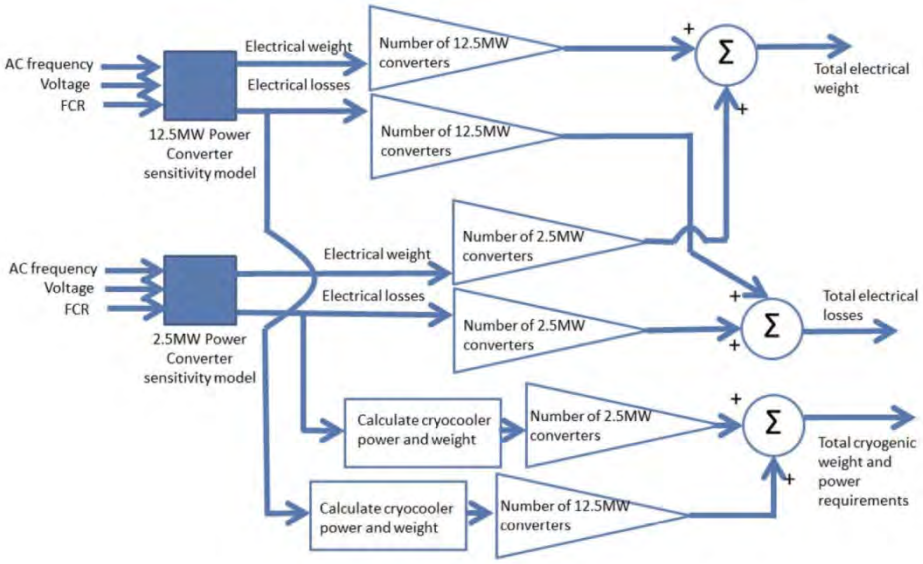


Figure 8: Upper level of power converter block.

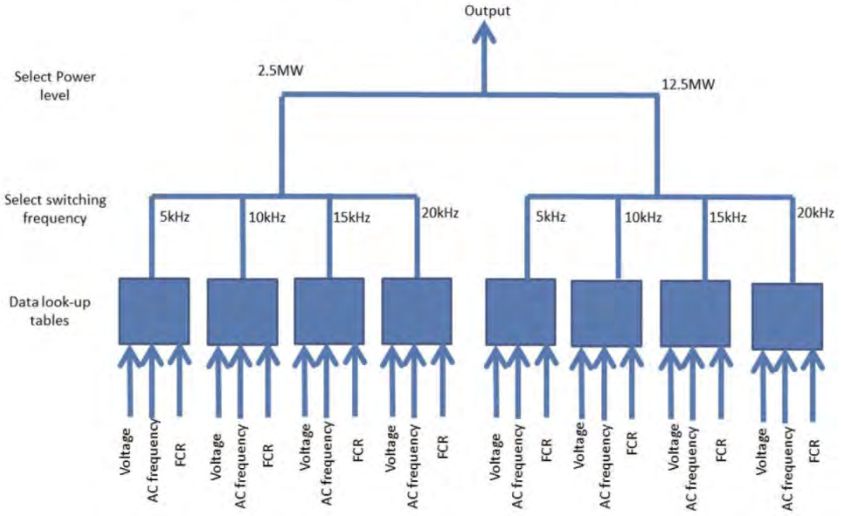


Figure 9: Structure of the power electronics sensitivity model.

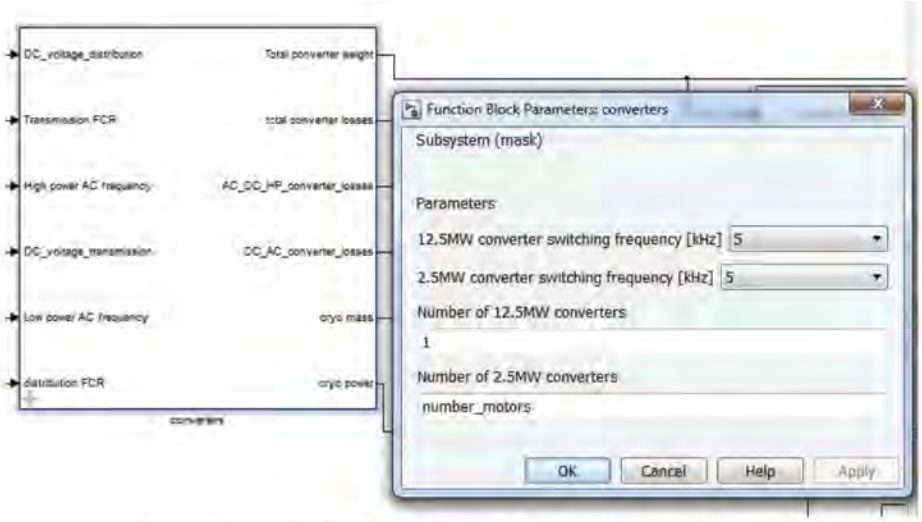


Figure 10: Mask for the top level of the power converter block.

4.3.2 Cable (AC and DC)

The TeDP architecture includes both DC and AC cables which are superconducting and operate at cryogenic temperature of 77K. The cable component model developed calculates the total weight of the electrical system, the total weight of the cryogenic system, the electrical losses and the total power required by the cryogenic system for all the cables in a TeDP architecture.

By inspection of Figure 1, it can be seen that there are 4 broad categories of cable in the example TeDP architecture. These are AC cable at generator power level, AC cable at motor power level, DC cable at transmission power level and DC power at distribution power level. The AC sections of the architecture are three phase, hence requiring three cables with each rated at one third of the total power rating. The DC cables have a positive and negative busbar, with a third, neutral wire.

Therefore the top level of the AC cable model has the structure shown in Figure 11. Each of the cable sensitivity model blocks return the weight of the electrical system, the total weight of the cryogenic system, the electrical losses and the power requirements of the cryogenic system for the section of cable that each represents (as shown in Figure 12). The inputs to the blocks are the voltage, power, frequency (for DC this is set to 0Hz) and length of the section of cable.

The internal structure of each of the model data blocks in Figure 12 is shown in Figure 13. For the DC cable, the voltage, power and cable length are used as inputs to the look-up tables to determine the weights, losses and power requirements for the length of DC cable. If the cable is AC, then the AC frequency, voltage and power are used to determine the weight, losses and power requirements for 1 metre of AC cable. The length of the cable is used to multiply the weight, loss or power and calculate the total weight, losses or power requirements for that length of AC cable. The AC cable is three phase, therefore the weights, losses and power requirements returned by the look up tables are multiplied by 3 to give the total value for a set length of AC cable.

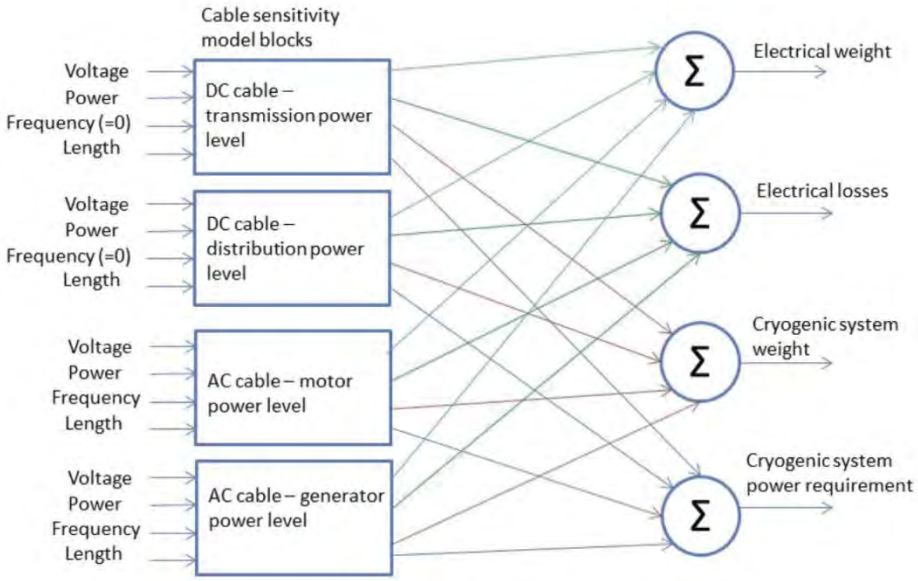


Figure 11: Top level of cable component block.

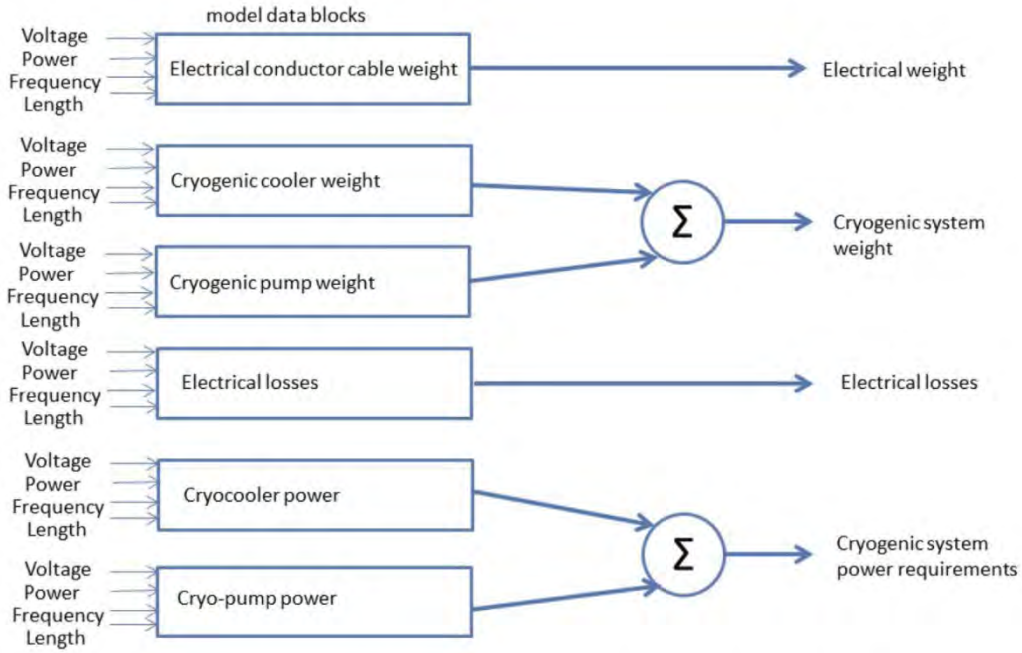


Figure 12: Model structure inside each of the cable sensitivity blocks in Figure 11.

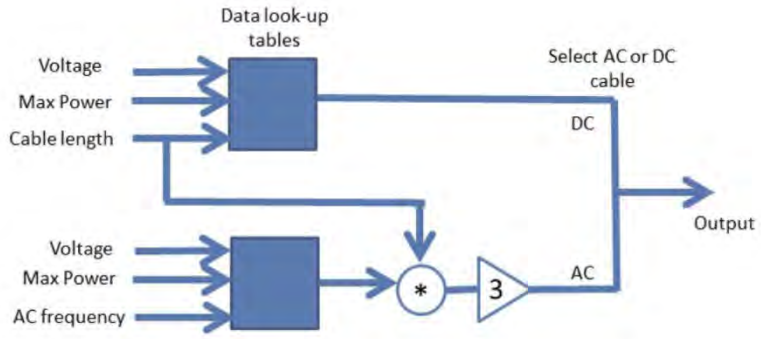


Figure 13: internal structure of model data blocks.

The mask of the data block for the cable component model in Matlab Simulink is shown in Figure 14. The user must select whether a section of cable is AC or DC. By putting several of these blocks together, the different sections of cable which make up a TeDP architecture can be configured.

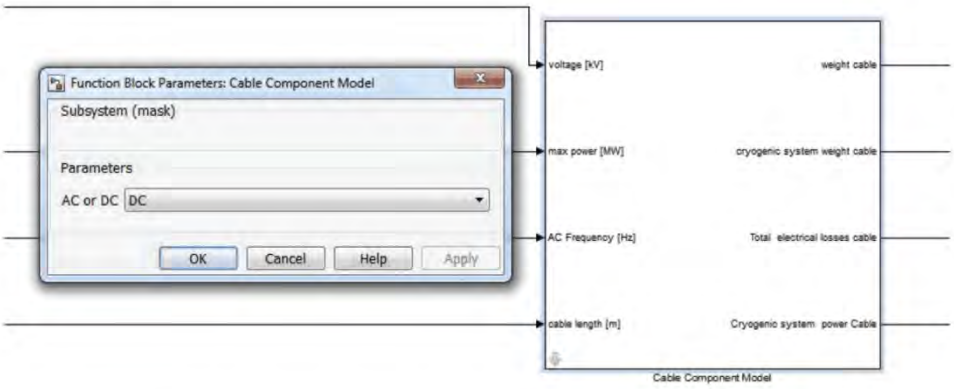


Figure 14: Mask of the data block for the cable component model in Matlab Simulink.

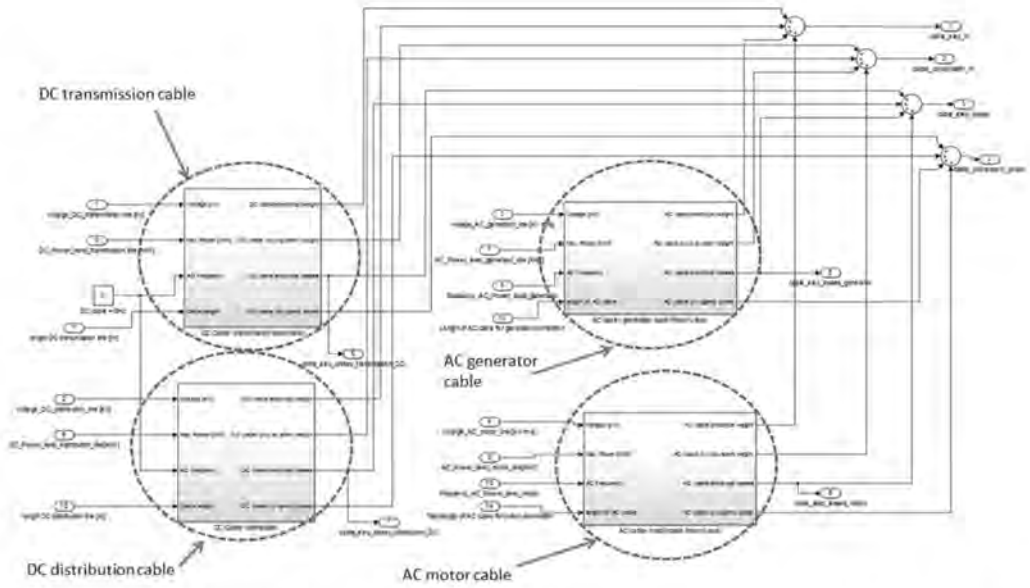


Figure 15: Full cable model in Matlab Simulink for the TeDP example architecture, with AC and DC high power sections, and AC and DC low power sections of cable.

4.3.3 Electrical machines

It has been proposed that an N+3 TeDP system will include two, wing-tip mounted turboshaft engines. Each of these will drive two superconducting generators [5]. These generators will supply power to the electrical power network on the N+3 aircraft. Ultimately, this electrical network will supply a number of superconducting fan motors, each of which is driving a propulsor. It is these propulsors which will provide thrust for the aircraft. In the example TeDP architecture shown in Figure 1, it can be seen that the example architecture considered for this RTAPS II study includes one superconducting generator and three propulsor motors.

Figure 16 shows the structure of the electrical machines component model. There are two data blocks, one for the generator and one for the motor. These each take in the maximum rated power and rated speed for the generator and motor and return the electrical weight, cryocooler weight, electrical losses and the cryocooler power requirements.

The cryocooler losses for the electrical machines have been calculated using Equations 4 and 5 below, with the data which was provided by Rolls-Royce North American Technologies. This calculation takes place within the Matlab "m-file" script for the electrical machines data. The cryocooler losses data is then read from there directly into look-up tables alongside the other data for the electrical machines using the "m-file" script.

$$\eta_{motor\_only} = 1 - \frac{iron\_losses + total\_AC\_losses}{take\_off\_power} \quad (4)$$

$$\eta_{tot} = 1 - \frac{iron_{losses} + total\_AC\_losses + cooler\_power}{take\_off\_power} \quad (5)$$

The structure of the electrical machines component model is shown in Figure 16. A detailed diagram of the model data block structure for the "generator data block" and "motor data block" is shown in Figure 17. The values for weights, losses and power requirements which are returned from the data blocks are multiplied by the number of generators or number of motors ("No. generators" and "No. motors" in Figure 16), and then the total weights, losses and power requirements are summed together to calculate the total weights, losses and power requirements for the electrical machines for a particular TeDP architecture. It is assumed that multiple generators or multiple motors within an architecture will be identical. The number of generators and the number of motors are set by the user in a top-level mask in the component block in Matlab Simulink, as shown in Figure 18.

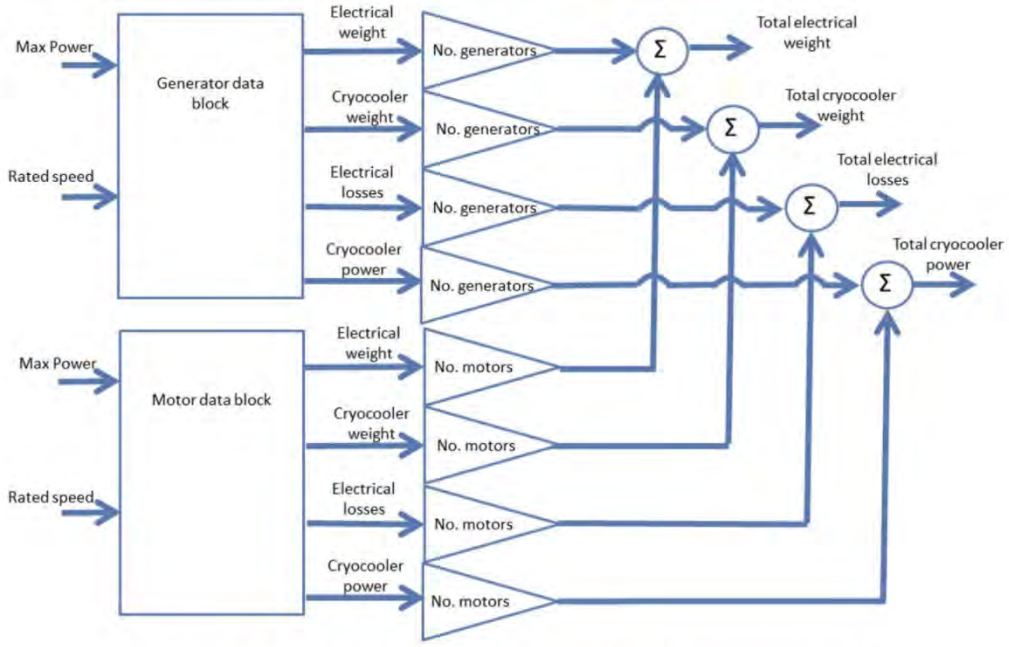


Figure 16: Structure of the electrical machines component model.

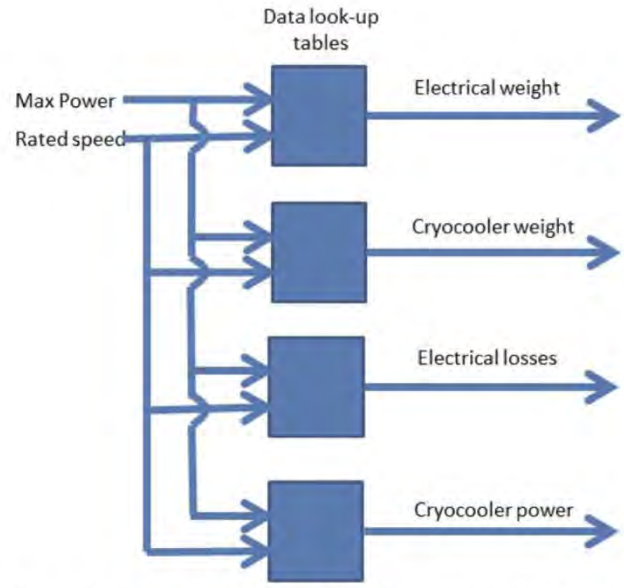


Figure 17: Internal structure of model data blocks for the electrical machine component model.

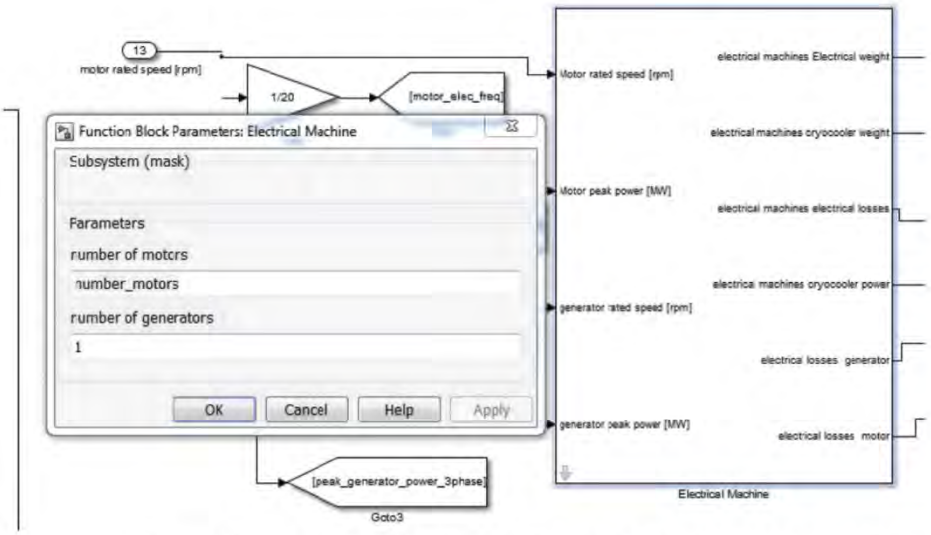
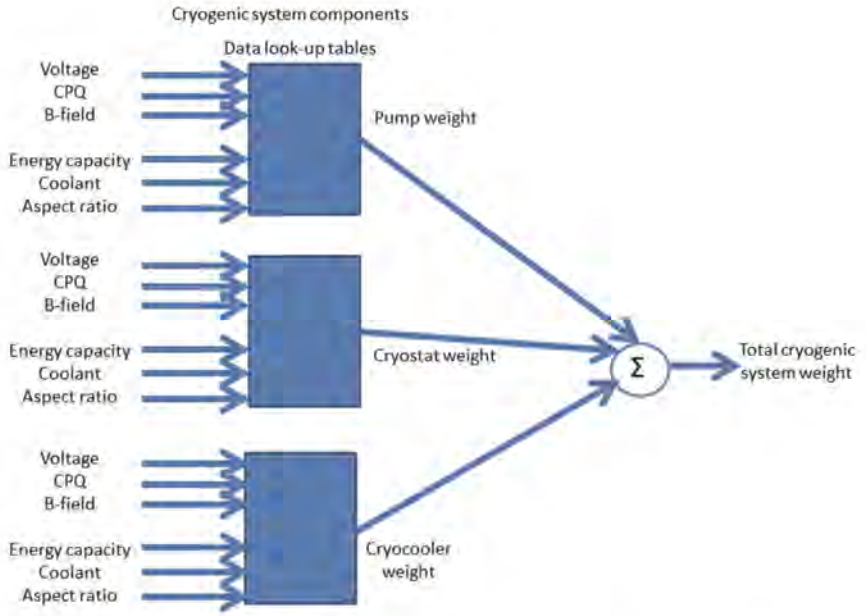


Figure 18: top level mask of the electrical machine component model.

The cryocooler power requirements for the electrical machines have been calculated using Equations 4 and 5.

4.3.4 Superconducting magnetic energy storage (SMES)

The TeDP architecture includes a SMES, which is connected to the DC transmission bus. The SMES unit includes the SMES device and a DC-DC converter which interfaces the SMES to the DC transmission bus. Hence the sensitivity model for the SMES includes both the SMES device and the interfacing DC-DC converter.



and Figure 20 show the structure of the top level of the SMES component model. There are 6 parameters input to the data look-up table blocks within the SMES model. These data look-up table blocks return the weights of the different elements of the electrical and cryogenic systems for the SMES. These are then summed together to give the total electrical system and cryogenic system weights. A similar method for calculating the total electrical losses and cryogenic power system requirements attributable to the SMES has been applied and this is shown in Figure 21.

The 6 inputs to the data look-up tables are the DC bus voltage, the type of coolant used, the compressive quality factor (CPQ), the magnetic field (B-field), the aspect ratio and the rated energy capacity of the SMES. Figure 22 shows the structure of each of the data look-up table blocks. The look up tables interpolate between the voltage, CPQ and B-field. There are 60 lookup tables in each data look-up table block, with each set of data specific to a set energy capacity, aspect ratio and coolant type. The specific look-up table to use is selected within the block, by the set aspect ratio, energy capacity and coolant type for the SMES. These are selected using menus on the top level block mask in Matlab Simulink, as shown in Figure 23.

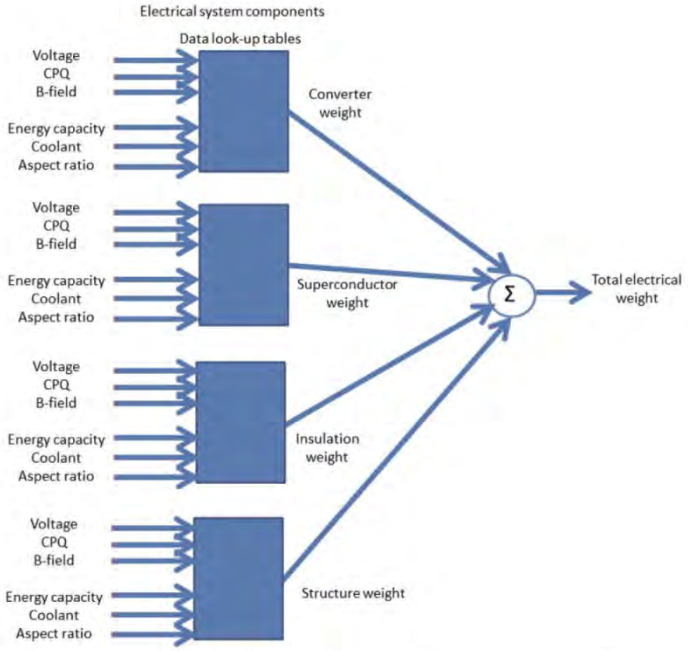


Figure 19: Calculation of electrical weight for the SMES

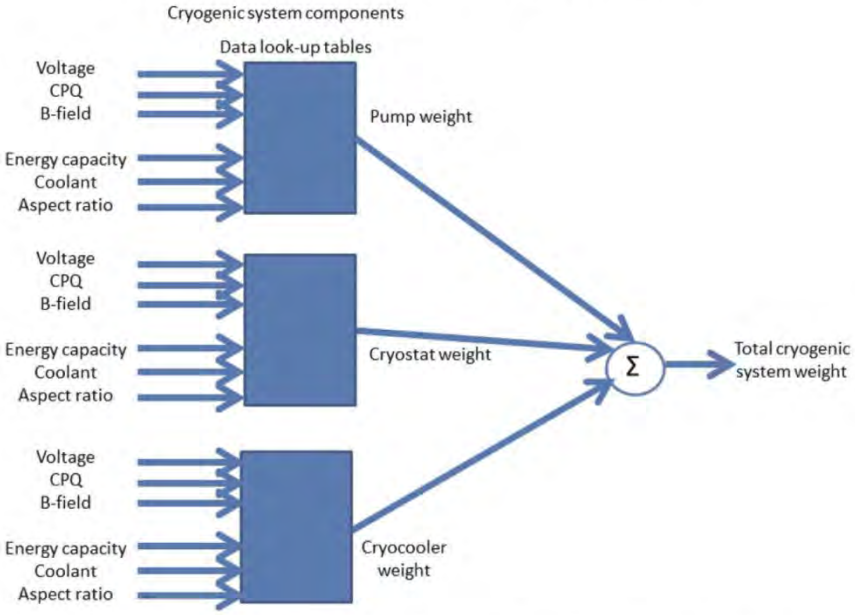


Figure 20: Calculation of cryogenic system weight for the SMES.

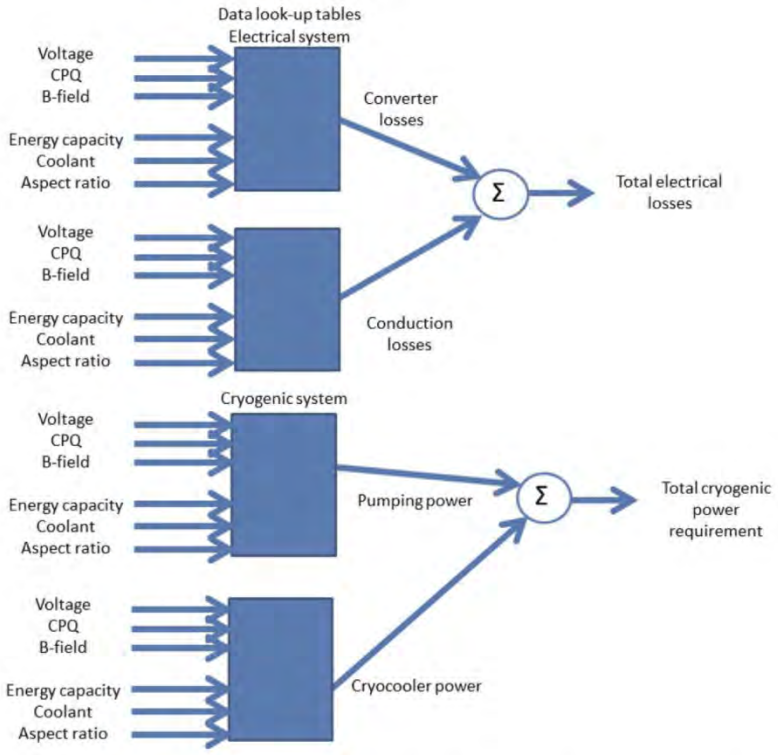


Figure 21: Calculation of the electrical losses and the cryogenic system power requirements for the SMES.

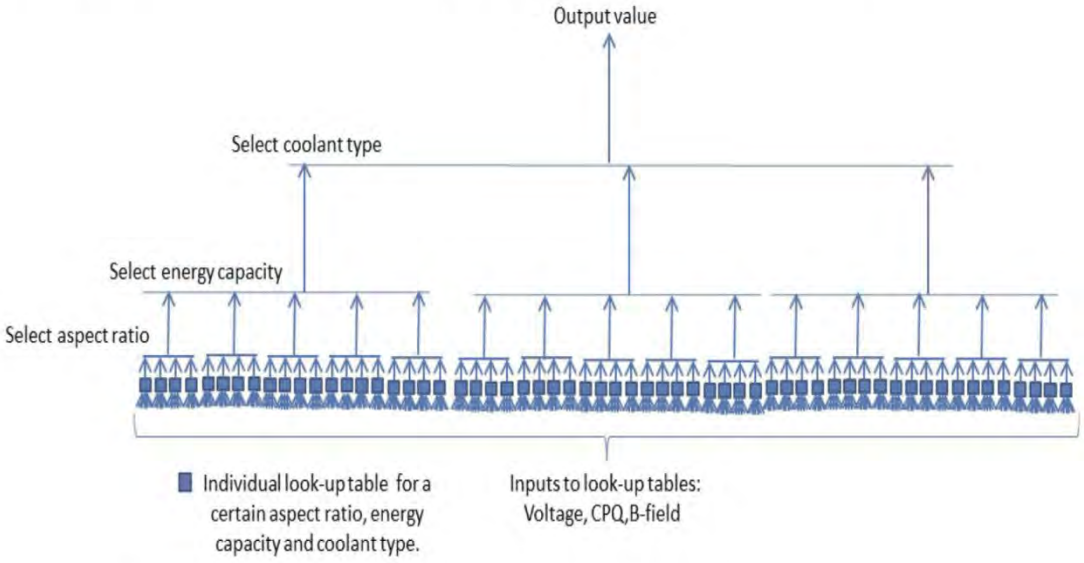


Figure 22: Detail of the data look-up table blocks within the SMES component model.

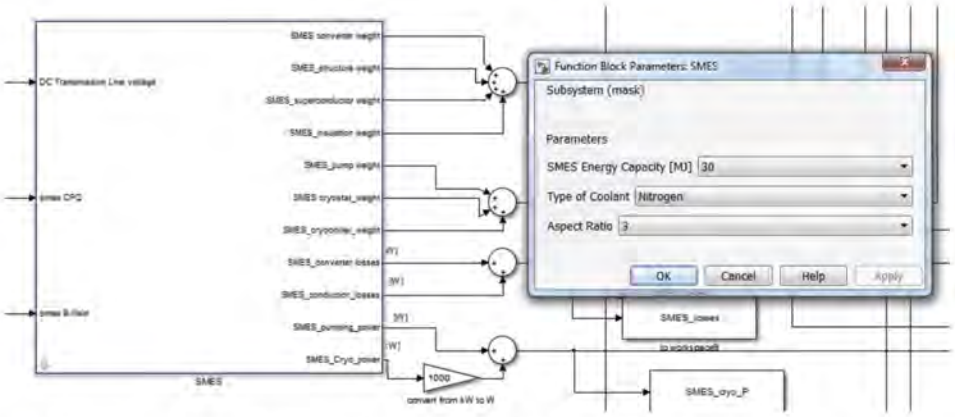
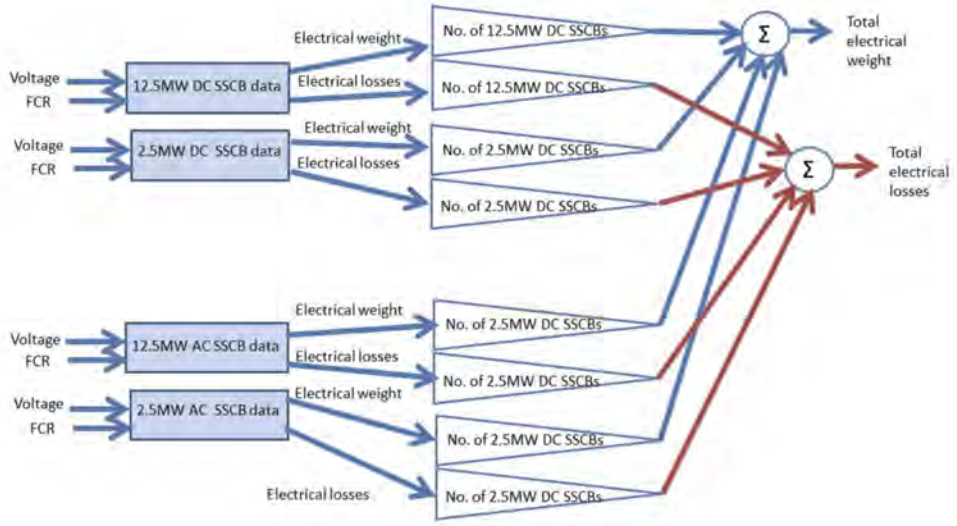


Figure 23: Top level mask of the SMES block with menus to select aspect ratio, energy capacity and coolant type in Matlab Simulink.

4.3.5 Solid State Circuit Breakers (SSCBs)

There are two components included in the protection block of the sensitivity model which has been developed: the super conducting fault current limiters (SFCLs) and the solid state circuit breakers (SSCBs). These devices are present in both the AC and DC sections of the TeDP architecture and at both the 12.5MW and 2.5MW rated power levels. Figure 2 indicates the possible number, and location of, the SFCL and SSCB devices.

The SSCB data used for the SSCB component model is for devices which are not superconducting but operate at a cryogenic temperature of circa 100K. The structure of the component model block is shown in Figure 24. The look-up tables within the block interpolate between the voltage and fault current ratio. The power rating of the SSCB is fixed at either 12.5MW or 2.5MW. At present, the data used in all of the look-up tables is for DC SSCBs. In the future data specific to AC SSCBs could be included. The cryocooler weight and power requirements have been calculated using Equations 2 and 3.



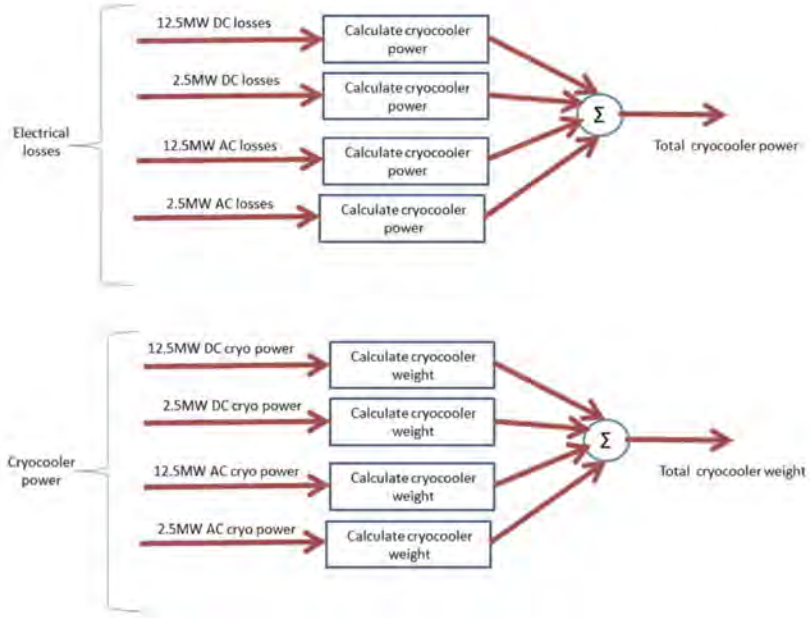


Figure 24: Structure of the SSCB component block.

The number of SSCBs in the TeDP architecture is set using the mask on the top level of the SSCB component block. This is shown in Figure 25.

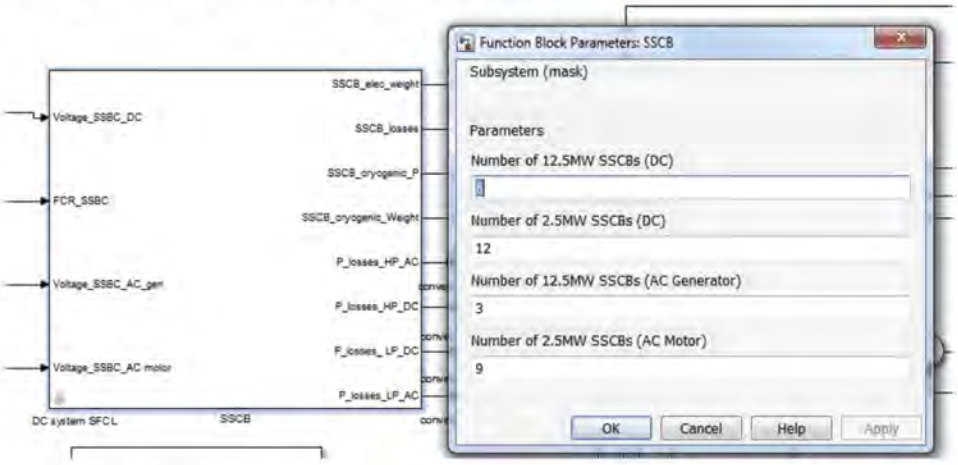


Figure 25: Top level mask of the SSCB block with menus to set the number of SSCBs in Matlab Simulink.

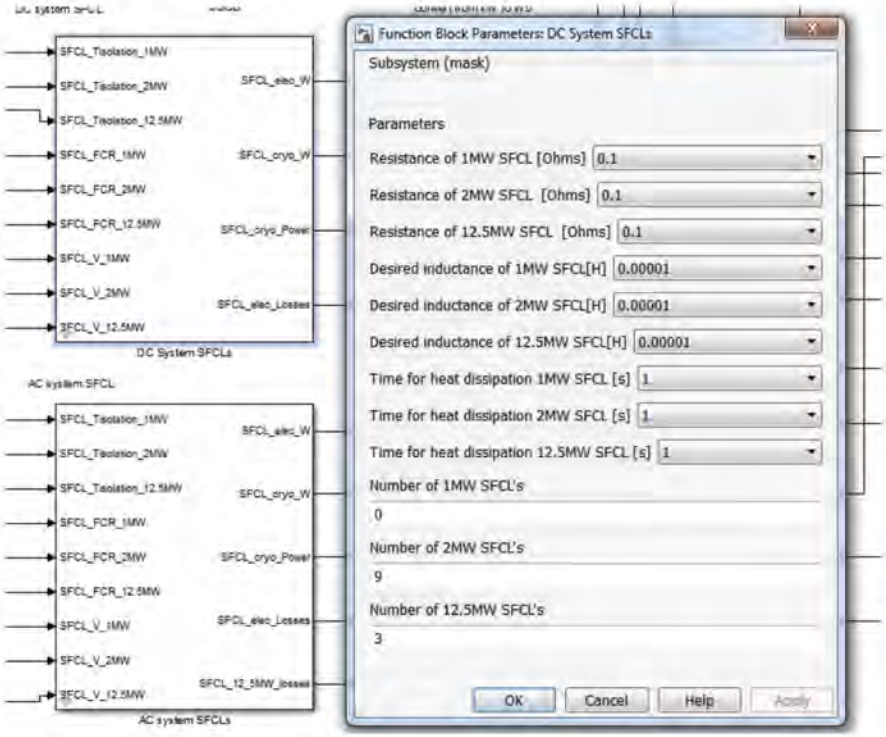
4.3.6 Superconducting fault current limiter (SFCL)

The SFCL component model is split into two parts within the protection block in the Matlab Simulink model. One is for the AC SFCL and the other is for the DC SFCL. The data used and the structure of these two SFCL component models is identical. The reason for having the two blocks is for clarity on how many SFCLs are AC and how many are DC in the architecture which the sensitivity model is representing.

The SFCL model is complex. There are 7 variables which affect the electrical weight, losses, cryogenic weight and cryogenic power requirements of an SFCL: voltage, power rating, time to dissipate heat, time to isolation, fault current ratio, resistance and desired inductance. The cryocooler data was calculated using Equations 2 and 3, taking the coolant to be at 77K and an ambient temperature of 300K. The Carnot efficiency and k remained at 30% and 3kg/kW respectively.

Figure 26 shows the structure of the lowest level of the SFCL sensitivity model. The input variables of voltage, fault current ratio (FCR) and time to isolation are interpolated between in each of the look up tables. For the 9 look-up tables in each of these blocks, the resistance and desired inductance is held constant. The power rating and the time to dissipate the heat are used to select a set of data.

The choice of inductance and resistance is made in the next level up in the SFCL block, in the middle layer. The structure of this block is shown in Figure 27. Each "Data look-up table block" in this diagram contains one set of look-up tables for a specific inductance and resistance, shown in Figure 26.



shows the calculation of the total weight (electrical and cryogenic) and cryogenic power requirements for the SFCL, for one particular power rating. The lowest and middle layers of the SFCL block are contained within the blue block as indicated. The total weights and power requirements are calculated by multiplying the weights and power requirements returned by the look-up tables, from the lower and middle levels of the component model, by the number of SFCLs of that power rating which are required.

To get the total weights and power requirements for all of the SFCLs in the AC or DC system, the total weights and power requirements for each power rating of SFCL are summed together. Finally the weights and power requirements for the AC and DC SFCLs are summed

together to calculate the total weight and power requirements.

Numbers of SFCLs of particular power ratings, alongside setting of resistance, desired inductance and time for heat dissipation are set on the top level mask of the SFCL block in Matlab Simulink. Figure 29 illustrates this.

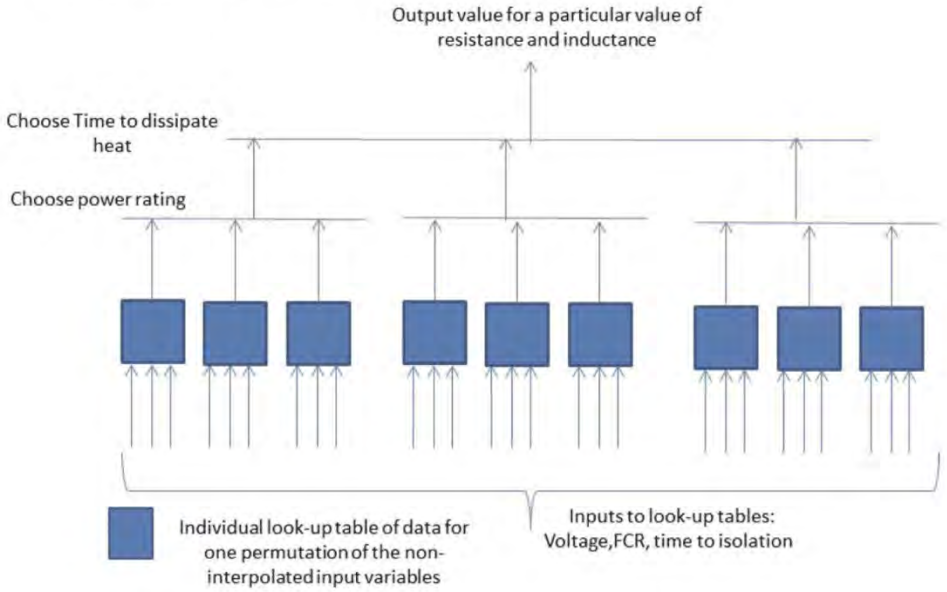


Figure 26: Lowest level of the SFCL model – data look-up table blocks.

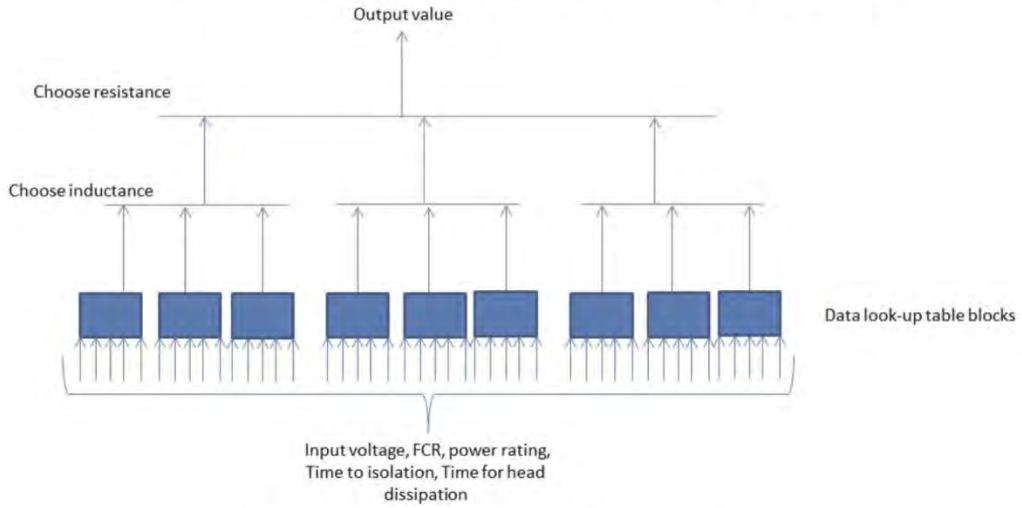


Figure 27: Middle layer of the SFCL component block. Each "data look-up table block" contains the structure shown in Figure 26.

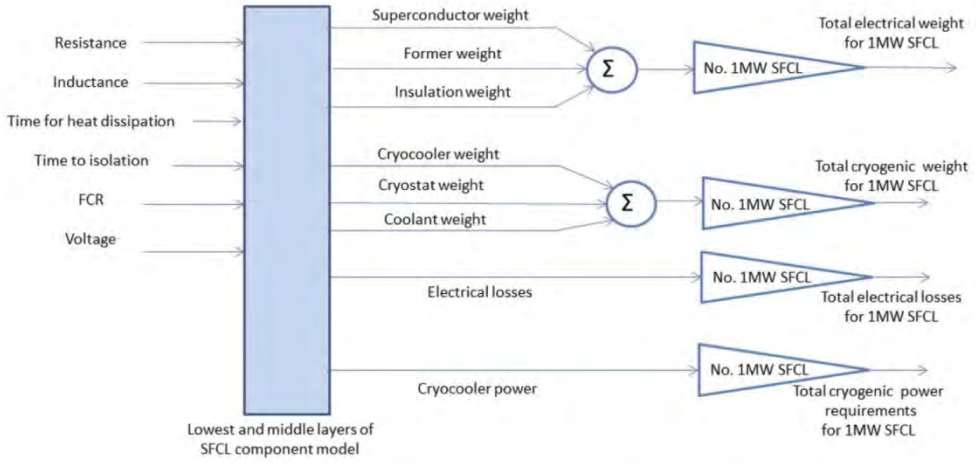


Figure 28: Calculation of electrical system weight, cryogenic system weight and cryogenic system power requirements for one particular power rating of SFCL.

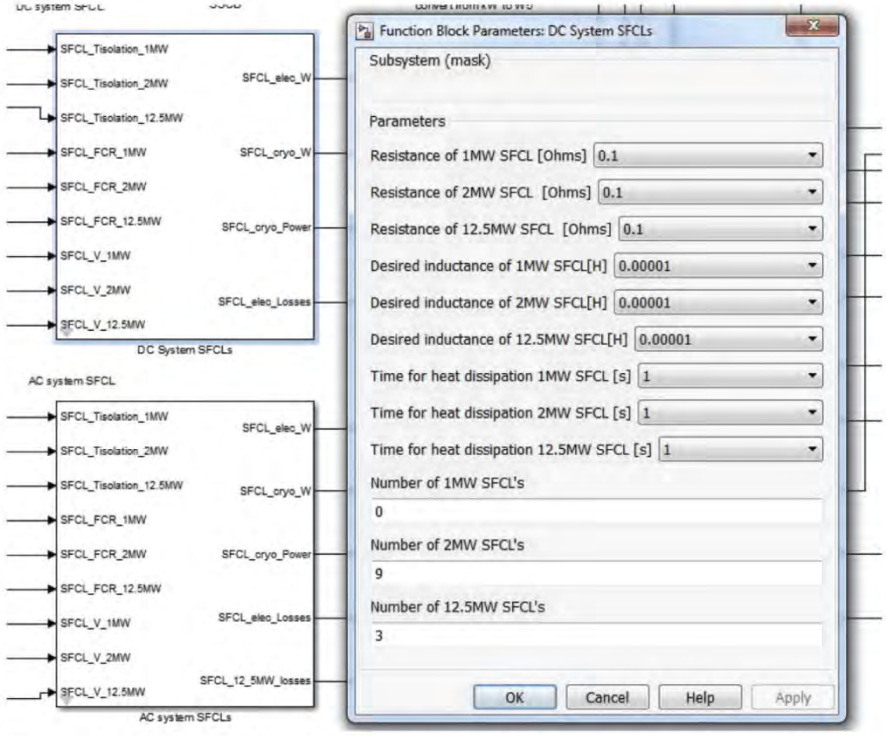


Figure 29: top level mask of SFCL to choose numbers of, and set fixed parameters, for a TeDP architecture in Matlab Simulink.

4.4 The full system sensitivity model

4.4.1 Description of the top level of the full system model in Matlab Simulink.

To implement the full system model, the component blocks described in Section 4.3 are placed within the architecture block (electrical machines, power electronics, SMES and cables) or the protection block (SSCBs and SFCLs). Figure 30 and Figure 31 show the top level of the architecture block and protection block in Matlab Simulink.

The model has been set up such that any values which are used in any of the look-up tables within the component models are connected to the top level of the protection and architecture blocks. This is to enable these values to be varied and the sensitivity of a TeDP architecture to variation in these input variables to be studied. For example, the voltage can be varied and the sensitivity of the system to this can be carried out.

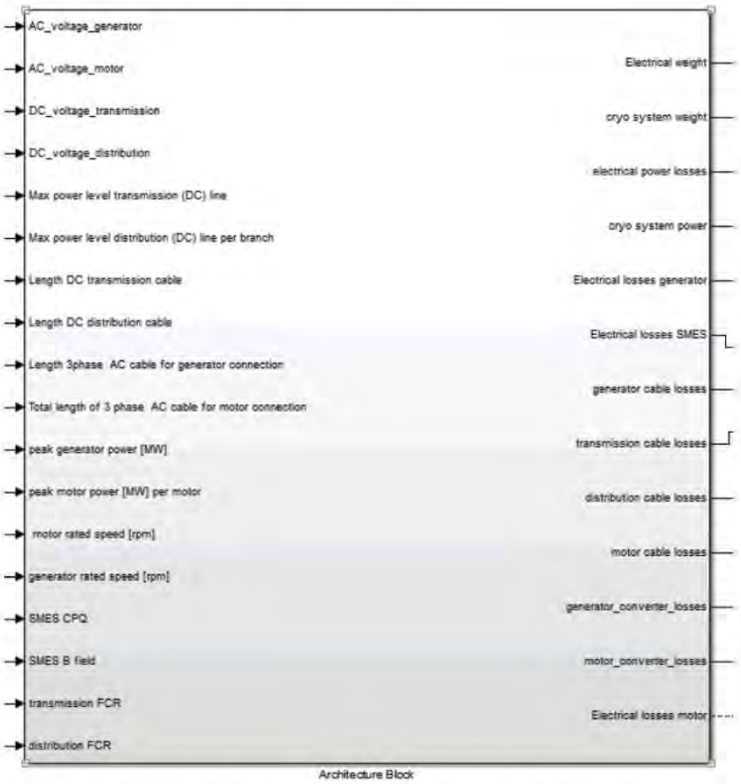


Figure 30: Architecture block in Matlab Simulink.

Figure 31: Protection block in Matlab Simulink.

As identified in Figure 2, there are four different sections of the architecture: AC generator, DC transmission, DC distribution and AC motor. The amount of power input to each section will be the amount of power input to the previous upstream section minus any electrical losses incurred in that section. This enables the losses in each section to be taken into account, so that the correct net power is supplied to the next downstream section of the TeDP architecture. This is illustrated in Figure 32. The generator in the example architecture supplies power to the full system. The model assumes that the distribution branches of the TeDP architecture are identical and that the total power supplied by the DC transmission system to the DC distribution system is equally shared between the branches of the distribution network.

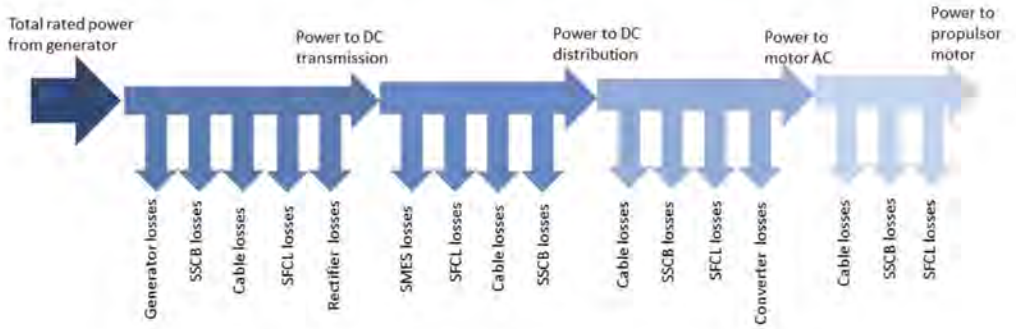


Figure 32: Electrical power losses in the full system.

It has been assumed that due to the negligible resistance of the DC sections, that the voltage drop over the DC cables would be extremely low. In addition it is assumed that the length of AC cable is short enough that any voltage drop in these sections can be neglected at this stage.

The electrical and cryogenic weights, electrical losses and the power requirements of the cryogenic system are returned from the protection and architecture blocks. These can then be summed together as required to carry out analysis. The data is output to the Matlab Workspace. The full efficiency of the system is calculated using Equation 1, with the full electrical losses for the architecture and protection systems. The weights, losses and power requirements from individual component blocks are output to the Matlab Workspace.

4.4.2 Model limitations

There are 3 key areas which limit the flexibility and possible accuracy of the results from the model.

Firstly, interpolation between data points, and extrapolation beyond the range of data points that are available is linear. Therefore, if sensitivity to a parameter is tested in a certain range, and not all components have data that extends over the complete range to be tested, then there will be a degree of error in the final result. The level of this error depends on the data trend for a particular parameter of a particular component.

Secondly the practical limit of the number of dimensions of a look-up table in Matlab Simulink is 3. It is theoretically possible to go above this number, but the modelling required to achieve this becomes extremely complex. Therefore there are some components (for example the SFCL) where it may be more desirable to have certain variables as interpolated variables in the look-up table rather than set points, to increase the flexibility of the model.

Thirdly the data is for the peak power demand. So the model is currently configured for the case of take-off. In terms of the weight of the electrical system, this will be the same for if the nominal power case was considered. However, the losses at nominal power (e.g. during cruise conditions) will be different to losses at full, peak power and hence the power requirements for the cryogenic system will also be different at nominal power.

5 Model Results and Discussion

5.1 Sensitivity study description

The aim of the sensitivity model described in Section 4, is to provide a tool which can be used to analyse and explore the sensitivity of an example TeDP architecture to variations in particular input variables. Of particular interest is the DC voltage level. This section will present the results from a voltage sensitivity test using the model described in the previous sections.

Aside from the voltage, it is clear that the model could also be used to test for sensitivity to fault current ratio, different motor and generator speeds (which are directly proportional to the AC frequency) and lengths of different sections of cable. Due to the modular nature of the model, it could also be used to contrast and compare the weights and efficiencies of different architectures: for example the weight penalty for including an extra propulsor motor.

5.2 Representation of the example TeDP architecture in the sensitivity model

The example TeDP architecture which is to be represented in the sensitivity model developed, was shown in Figure 1, and in more detail in Figure 2. Table 1 details the architecture and the settings which were chosen for running the model. These have been either been chosen based on data provided by Rolls-Royce North American Technologies and presented in [5], or in some cases, for example the switching frequency of the power converters, the values have been chosen as being considered sensible estimates.

There are three distribution branches, each is assumed to be identical. The number of distribution branches is set by the parameter "number_motors" which is set within the the m-file "full_RTAPS_sensitivity_model_run.m". This file also runs the appropriate m-files to populate the look-up table data into the model from the MS Excel spreadsheet files.

The fault current ratio was set at 2 throughout the whole of the architecture. The power delivered to the sections of cables, is calculated as described in Section 4 of this report: the input power to the previous section minus the electrical losses incurred in the previous section. Similarly, the power at the input of each of the propulsor motors at present is one third of the net power delivered by the DC transmission system, minus the losses incurred in the distribution cables, protection devices and the motor inverter.

The rated power of the SFCLs for the DC distribution and AC motor sections is 2MW, as this was the closest power rating to the rating of 2.5MW which is used for the motor inverters. The AC frequency on the motor and generator cables is directly linked to the motor and generator speeds, by a multiplying constant of 1/20. This constant comes from inspection of the motor data provided by Rolls-Royce North American Technologies.

Table 1: Model settings for the example TeDP architecture shown in Figure 2.

Component	Power rating (if appropriate)	Fixed settings	Number/Length
Generator	12.5MW	Speed = 8000 rpm	1
Motor	n/a	Speed = 4000 rpm	3
Rectifier	12.5MW	Switching Frequency = 5kHz FCR = 2	1
Inverter	2.5MW	Switching Frequency = 5kHz FCR = 2	3 (one per motor)
SMES	n/a	Energy capacity = 30MJ B-field = 5T Coolant = Nitrogen CPQ = 0.5 Aspect ratio = 3	1
Cable: AC Generator	n/a	AC frequency = 400Hz	1m (3m in total for 3 phases)
Cable: DC Transmission	n/a	-	40m
Cable: DC Distribution	n/a	-	15m per branch (45m total)
Cable: AC Motor	n/a	AC frequency = 200Hz	1m (3m in total for 3 phases)
SSCB: AC Generator	12.5MW	FCR = 2	3
SSCB: DC Transmission	12.5MW		6
SSCB: DC Distribution	2.5MW		12
SSCB: AC Motor	2.5MW		9
SFCL: AC Generator	12.5MW	Resistance = 1Ω Desired inductance = 0.1mH Time for heat dissipation = 1s Time to isolation = 0.0001s FCR =2	3
SFCL: DC Transmission	12.5MW		2
SFCL: DC Distribution	2 MW		6
SFCL: AC Motor	2 MW		9

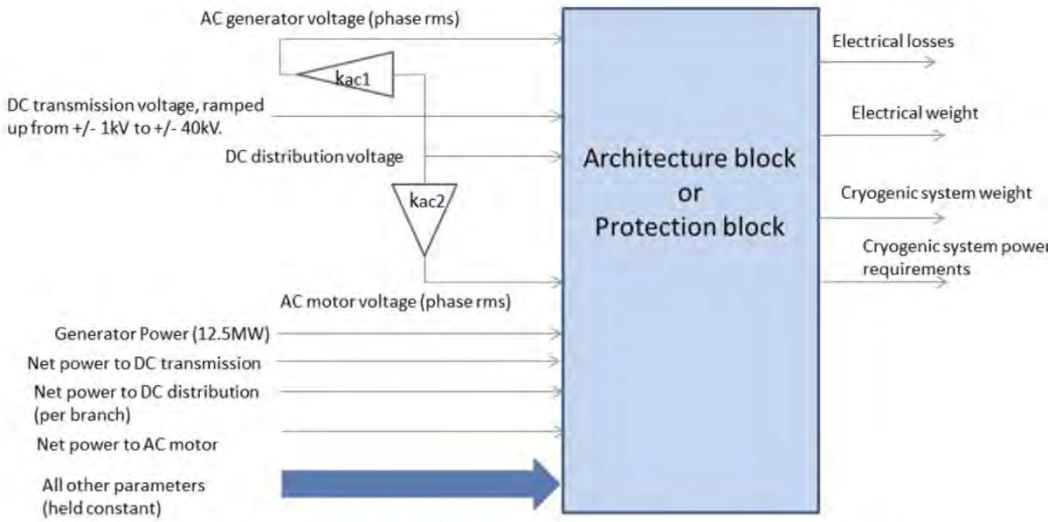


Figure 33: Model set up in Matlab Simulink for voltage sensitivity study, where kac1=Kac2=0.855.

To run the voltage sensitivity study, the DC voltage is ramped up from +/-1kV to +/-40kV. The per phase generator voltage is calculated from this value using Equation 6 [6]. The factor of 2 is required to account for the full voltage across the DC link. Equation 5 has also been used to calculate the rms phase voltage to the motor.

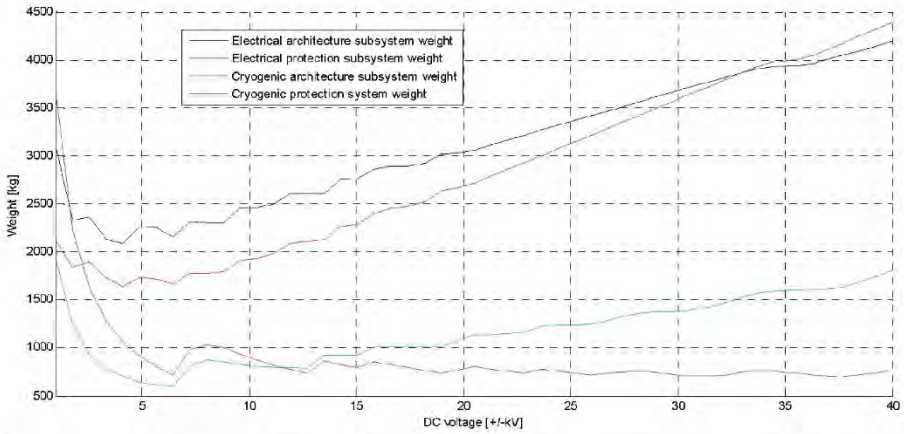
$$V_{ph\,rms} = \frac{2 * V_{dc}}{1.35 * \sqrt{3}} \tag{6}$$

Where V_{dc} is the positive rail DC voltage, assuming there is a positive, negative and return rail for the DC transmission and distribution system.

5.3 DC voltage sensitivity

The sensitivity of the weight and efficiency of the TeDP architecture in Figure 2, with the settings described in Section 5.3, to variation in the DC link voltage was carried out using the Matlab Simulink model. The DC link voltage was initially swept through from +/- 1kV to +/- 40kV.

By inspection of



it can be seen that the minimum weight of the electrical system is when the DC voltage is at around +/-4.5kV and again at around +/-6kV. The minimum weight of the cryogenic system is at a slightly higher voltage of around +/-6kV. Hence the minimum weight of the whole system is at this higher voltage of around +/-6kV. It is clear from Figure 35 that this minimum weight is driven by the weight of the protection system, and in Figure 36 it can be seen that the electrical weight of the protection subsystem is dominated by the weight of the SSCBs.

By inspection of Figure 35 and Figure 36 it can also be seen that the electrical weight of the architecture subsystem is dominated by the power converters. The minimum weight of the power converters occurs at +/-4.5kV, but there is a dip in the power converter weight at +/-6.5kV. This dip at +/-6.5 kV corresponds to the minimum weight of the SSCBs, and the combined effect of the minimum weight of the SSCBs and the dip in the converter weight, results in the minimum weight of the full system occurring at +/-6.5kV. It is clear from these results firstly that the contribution of the weight of the cryogenic system to the total system weight is significant, and secondly it is the weight of the converters and their associated cryogenic systems and of the SSCBs and their cryogenic systems which dominate the weight of the total system.

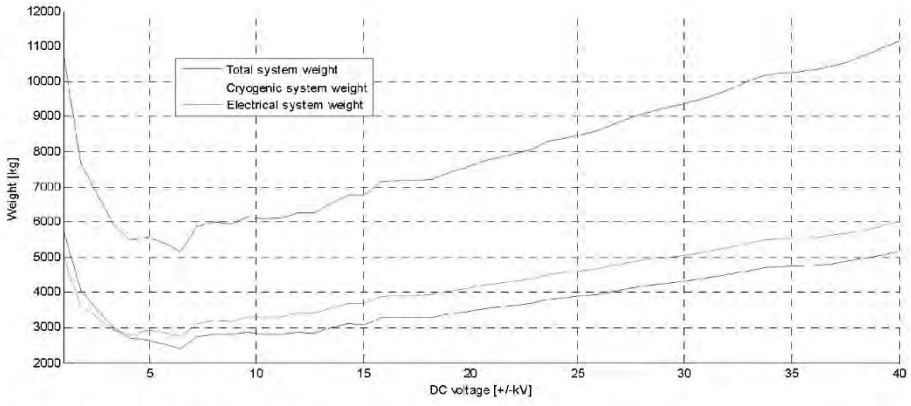


Figure 34: Total weight of the TeDP system, weight of the electrical system and weight of the cryogenic system as the DC link voltage varies from +/-1kV to +/-40kV.

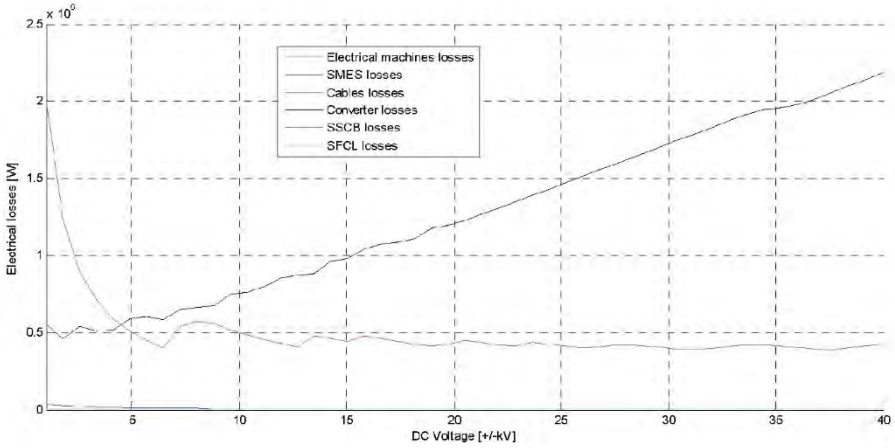


Figure 38 it can be seen that the electrical losses are dominated by both the SSCB in the protection subsystem, and the converters in the architecture subsystem. Hence the minimum losses are at around +/-6.5kV. Above this voltage the converter losses increase and dominate the system. Hence the electrical efficiency (Figure 39) for the system is at a maximum of circa92% when the DC voltage is at around +/-6.5kV.

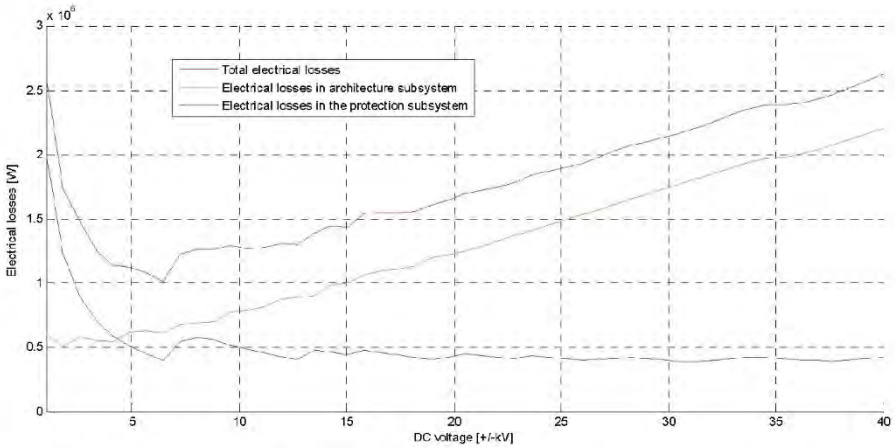


Figure 37:Total electrical losses, and the electrical losses of the architecture and protection sub-systems.

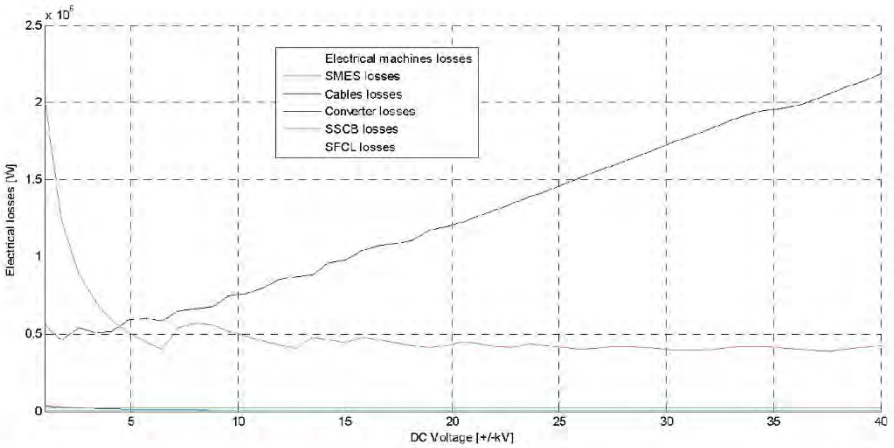


Figure 38: The electrical losses due to individual components which make up the TeDP electrical system

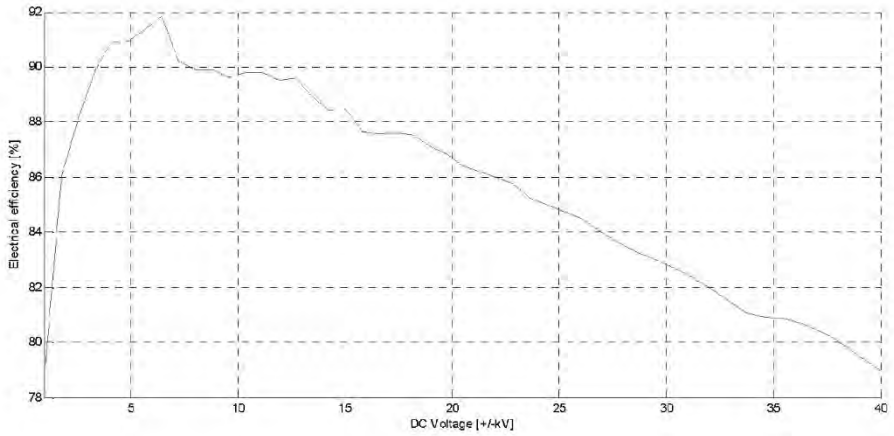


Figure 39: Overall electrical efficiency

Figure 40 shows the cryogenic power requirements for the system as the DC voltage is increased. The requirements for the architecture increase as the voltage increases because the losses in the converters increase with voltage, and this power loss is dissipated as heat. Similarly, the power requirements of the cryogenic system for the protection subsystem are dominated by the SSCBs. As the voltage increases, the trend is for the losses in the SSCBs to decrease, resulting in the power requirements of the protection system cryogenic system decreasing as voltage increases. Hence as the DC voltage increases, the power requirement of the cryogenic system is dominated by the architecture system, namely the converters.

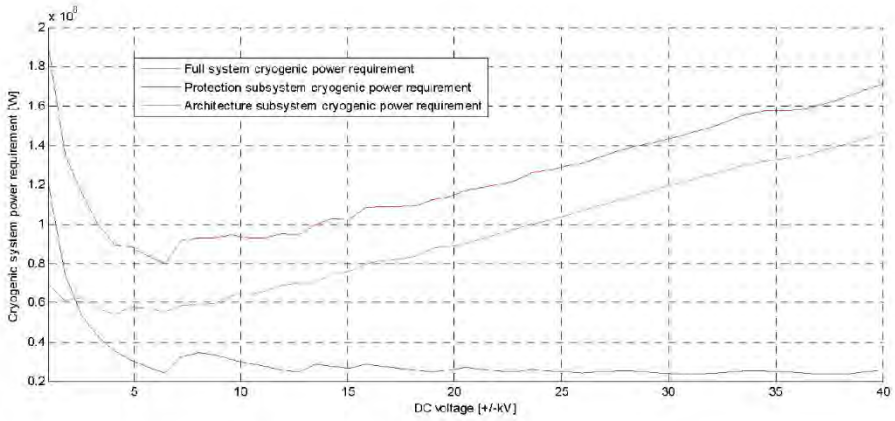


Figure 40: The cryogenic power requirements for the full system, the architecture and protection sub-systems.

The trends shown in Figures 34-40 in general match those presented in [5]. Both studies have shown that the converters and SSCBs have a significant impact on the system weight and efficiency. The optimum operating voltage in the results presented in this report has been found to be around +/-6.5kV, whereas the optimum operating voltage presented in [5] is +/-4.5kV. By inspection the results suggest that it is the impact of the SSCBs which is pulling the optimum operating voltage up from +/-4.5kV to around +/-6.5kV.

A possible reason for the differences in the optimum operating voltage between the sensitivity study carried out in [5] and the sensitivity study carried out in this report is that the architecture and system settings for the two studies may be different. Therefore due to the fact that the optimum operating voltage of +/-6.5kV is within the broad range of acceptable DC voltages put forwards in [5], and the general trends shown in Figures 34-40 match those presented in [5], confidence can be given to the results obtained from the sensitivity model presented in this report.

To investigate the impact of the SSCBs on the system weight and efficiency further, the voltage sensitivity study was re-run with four different cases, with each case having a different number of SSCBs as shown in Table 2.

Table 2: the numbers of SSCBs for the four different case studies to investigate impact of SSCB on system weight and efficiency.

Case	Total number of AC Generation SSCBs	Total number of AC motor SSCBs	Total number of DC transmission SSCBs	Total number of DC distribution SSCBs
1	3	9	6	12
2	3	9	4	6
3	0	0	4	6
4	0	0	0	0

Selected results from the case studies are shown in Figures 41 to 44. It can be seen that as the number of SSCBs in the system increases, the DC voltage which gives minimum system

weight increases from +/-4.5kV to +/-6.5kV. The DC voltage which returns the highest electrical efficiency also increases from around +/-2kV to +/- 6.5kV. With no SSCBs present, the converters dominate the electrical efficiency, and for the set of data used in the model, the converters are most efficient at around +/-2kV.

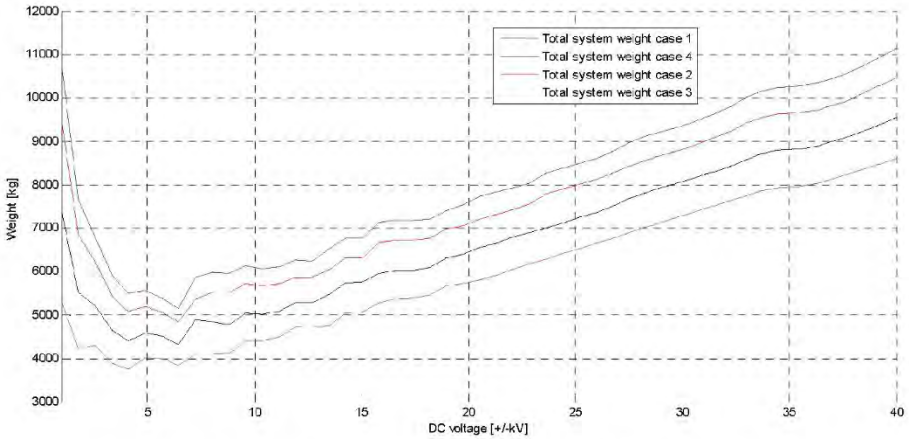


Figure 41: Total system weight for the four SSCB case studies.

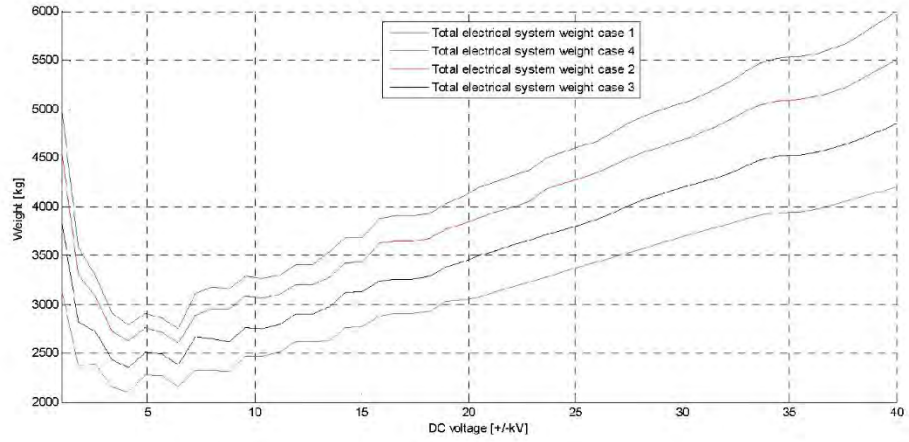


Figure 42: Electrical system weight for the four SSCB case studies.

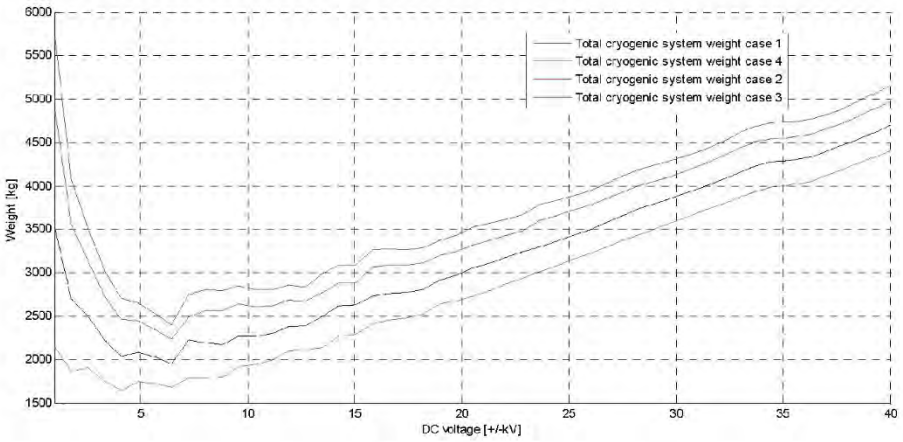


Figure 43: Cryogenic system weight for the four SSCB case studies.

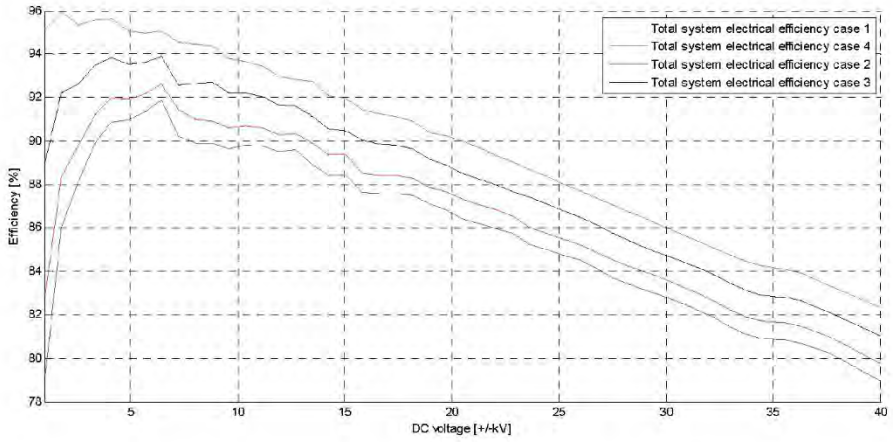


Figure 44: Efficiency of the full electrical system for the four SSCB case studies.

6 Future model development and conclusions

In conclusion an integrated system sensitivity model has been built for an example TeDP N+3 architecture. The model developed is modular in structure and therefore can be adapted to represent different TeDP architectures if required. The model has been used to carry out a voltage sensitivity study, the results of which give an indication of the type of information which the model could be used to determine in the future: for example the influence of certain system components on weights and efficiencies and hence assist with the design of optimised architectures and protection systems.

At present the model is limited to only be used for TeDP systems at peak power. It would be useful if the model was extended in the future to be able to represent a TeDP system operating at nominal power. An aircraft only operates at peak power load for a short period of its flight, hence if the model could represent the losses and cryogenic power requirements

during periods of nominal electrical load, then this would allow for a more representative sensitivity study of the electrical system efficiency and cryogenic requirements over a whole flight to take place.

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