

# The NASA Electronic Parts and Packaging (NEPP) Program: Roadmap for FY15 and Beyond

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<http://nepp.nasa.gov>

## **Acknowledgment:**

This work was sponsored by:  
NASA Office of Safety & Mission Assurance

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# Acronyms

Acronym	Definition
AMOLED	Active Matrix Organic Light Emitting Diode
CBRAM	Conductive Bridging Random Access Memory
CGA	Column Grid Array
CIGS	Copper Indium Gallium Selenide
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
DDR4	Double Data Rate Four
DNA	Deoxyribonucleic Acid
DoD	Department of Defense
DRAM	Dynamic Random Access Memory
EEE	Electrical, Electronic, and Electromechanical
EPC	Efficient Power Conversion
ESL	Electronic System Level
FeRAM	Ferroelectric RAM
FPGA	Field Programmable Gate Array
FY	Fiscal Year
GaN	Gallium Nitride
Gen	Generation
GSFC	Goddard Space Flight Center
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Testing
HEMTs	High-electron-mobility transistors
HP Labs	Hewlett-Packard Laboratories
HW	Hardware
IC	Integrated Circuit

Acronym	Definition
IP	Intellectual Property
IR	Infrared
IR/Infineon	International Rectifier/Infineon Technologies
LCoS	Liquid-Crystal-on-Silicon
MEMS	Micro Electrical-Mechanical System
MOSFETS	Metal Oxide Semiconductor Field Effect Transistors
MRAM	Magnetoresistive Random Access Memory
NASA	National Aeronautics and Space Administration
NAVY Crane	Naval Surface Warfare Center, Crane, Indiana
NEPP	NASA Electronic Parts and Packaging
Occam	Open Conditional Content Access Management
OLED	Organic Light Emitting Diode
PBGA	Plastic Ball Grid Array
R&D	Research and Development
RERAM	Resistive Random Access Memory
RF	Radio Frequency
SEE	Single Event Effect
SERDES	Serializer/Deserializer
SiC	Silicon Carbide
SOC	Systems on a Chip
TI	Texas Instruments
TRL	Technology Readiness Level
VNAND	Vertical NAND
WBG	Wide Band Gap



# Technology Selection Criteria for NEPP Investigation

- **The technologies should satisfy all or most of the following criteria:**
  - Wide applicability,
  - Product level or in productization, and,
  - No distinction: COTS to hi-reliability aerospace.
- **Partnering arrangements with other organizations preferred.**
- **In general, we avoid:**
  - Laboratory technologies, e.g., <TRL3,
  - Limited application devices with certain exceptions (critical application or NASA center specialization).

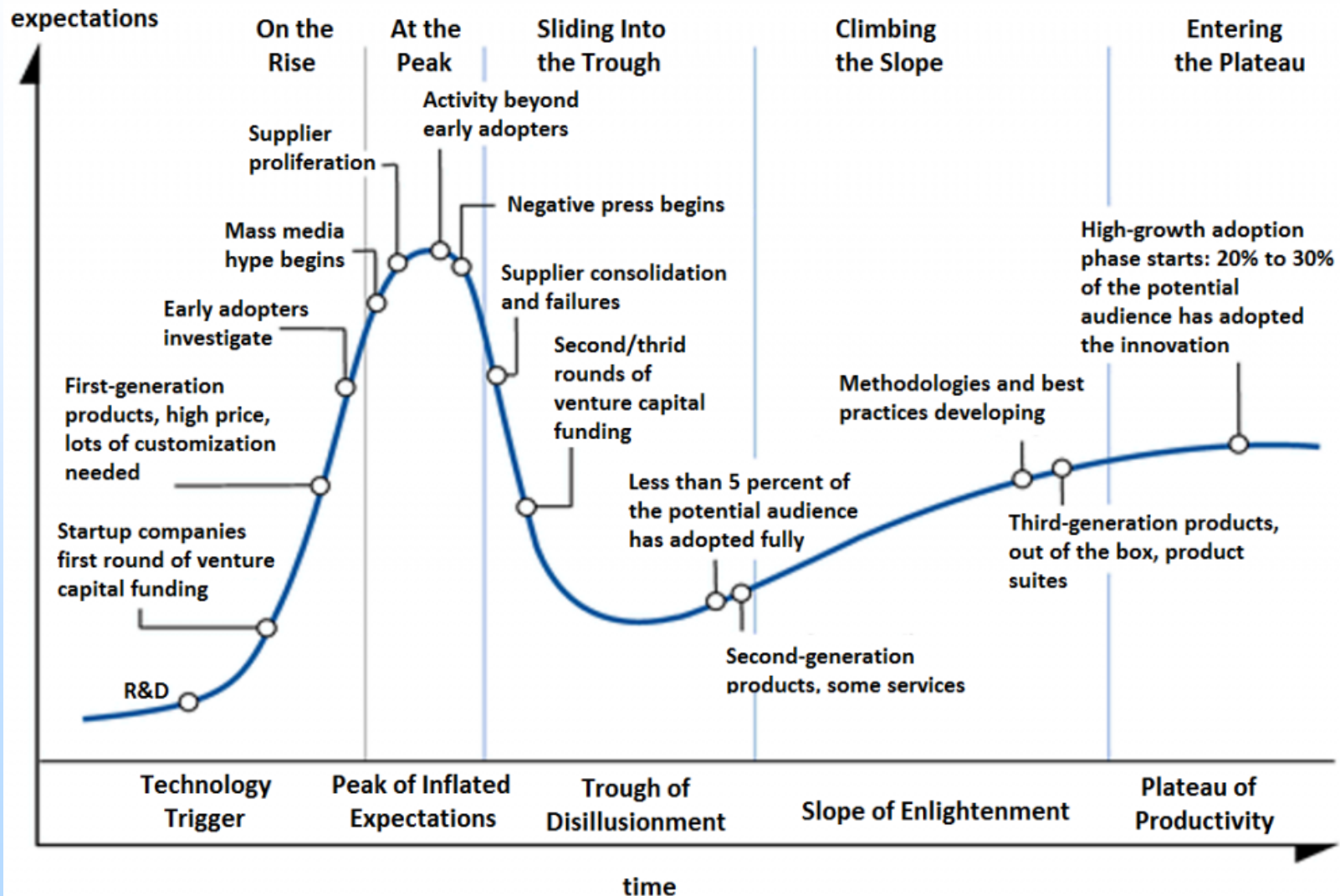


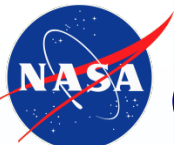
# Technology Investigation Roadmap Discussion

- **Technology assurance efforts are not explicitly included except on “Small Missions” chart.**
  - *Guidelines are a product of many technology evaluation tasks.*
- **Only major product categories shown.**
- **Technology areas not on Roadmap but under consideration include:**
  - Electro-optics (fiber optics),
  - Advanced analog and mixed-signal devices,
  - Imaging sensors,
  - Modeling and simulation,
  - High-speed communication (SERDES, fast data switches), and,
  - Adjunct processors (eg., graphics, signal processing)
- **Note 1: Advanced CMOS technologies not explicitly included:**
  - NEPP leverages samples from ongoing DoD and/or commercial sources.
  - 14nm is current target.
- **Note 2: “Reliability testing” may include product and/or package testing.**

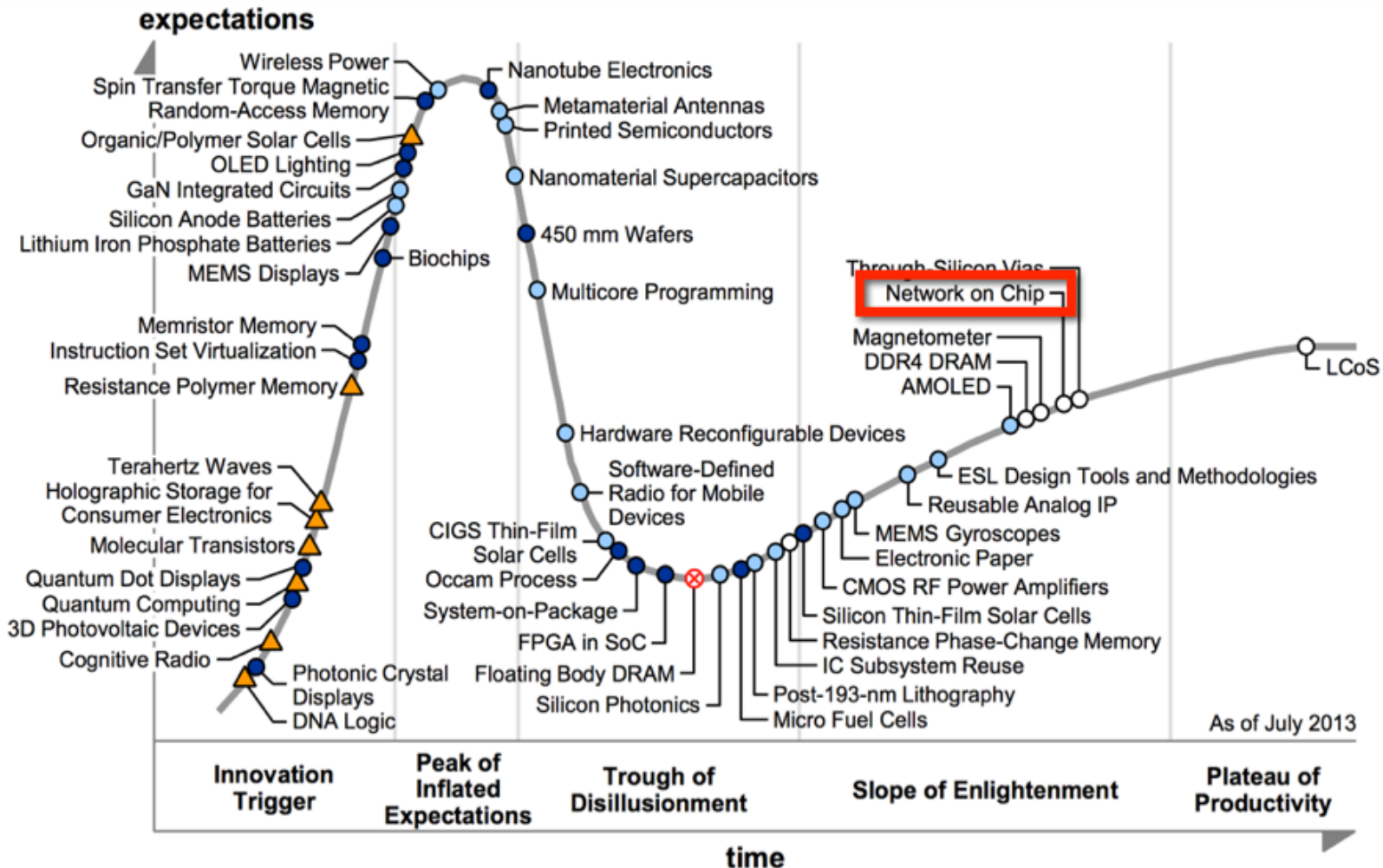


# Gartner Hype Cycle Concept





# Gartner Hype Cycle for Electronics 2013



As of July 2013

Plateau will be reached in:

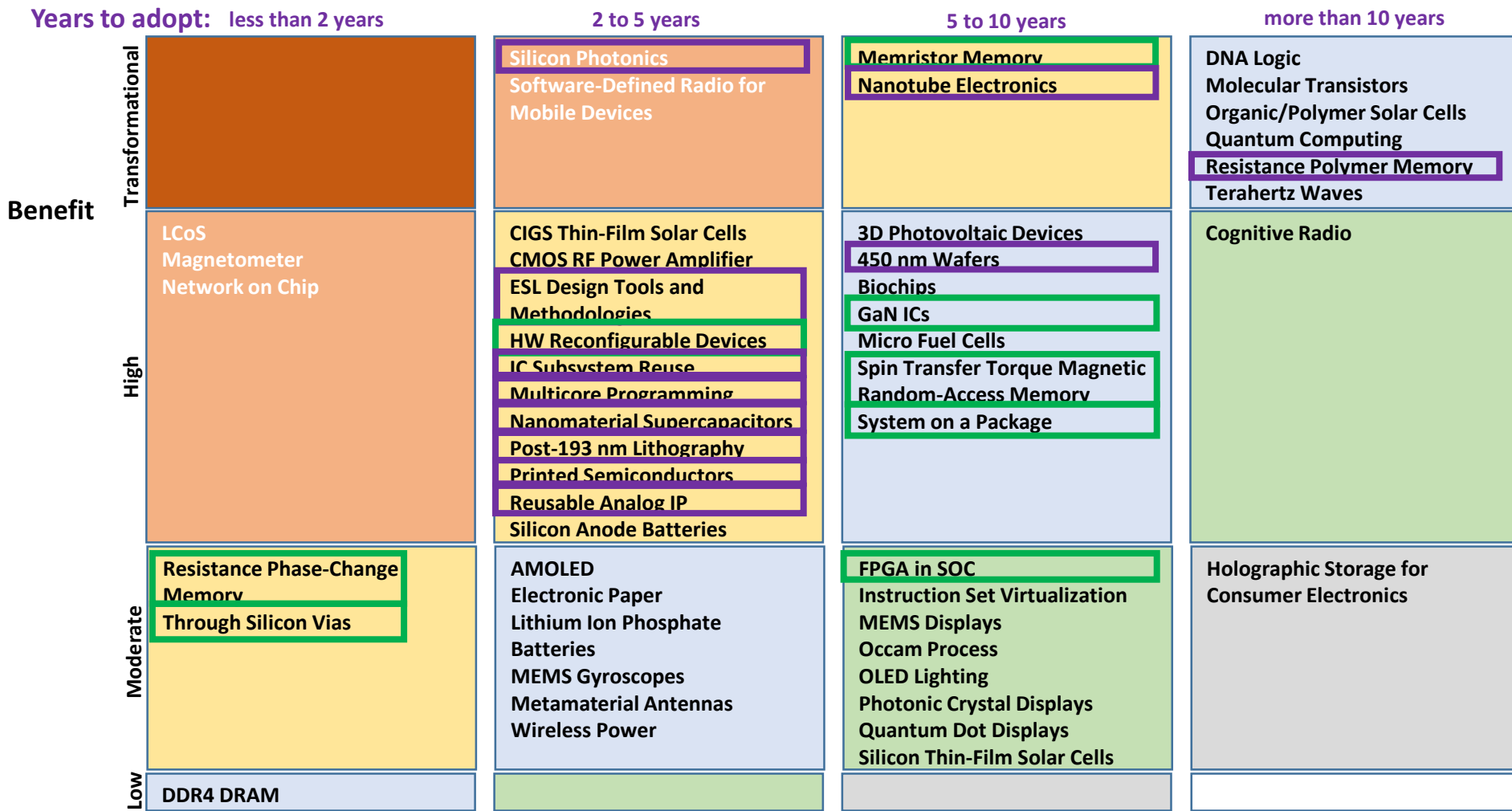
- less than 2 years
- 2 to 5 years
- 5 to 10 years
- ▲ more than 10 years
- ⊗ obsolete before plateau

Source: Gartner (July 2013)

Deliverable to NASA Electronic Parts and Packaging (NEPP) Program to be published on nepp.nasa.gov originally presented by Kenneth LaBel at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 23-26, 2015.



# NEPP and Gartner Electronics Hype Cycle 2013



NEPP Task Area

Future NEPP Area or Tracking Developments

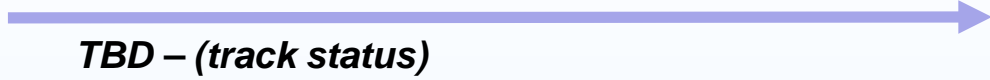
After Gartner 2013 Electronics Hype Cycle



# Field Programmable Gate Arrays (FPGAs)

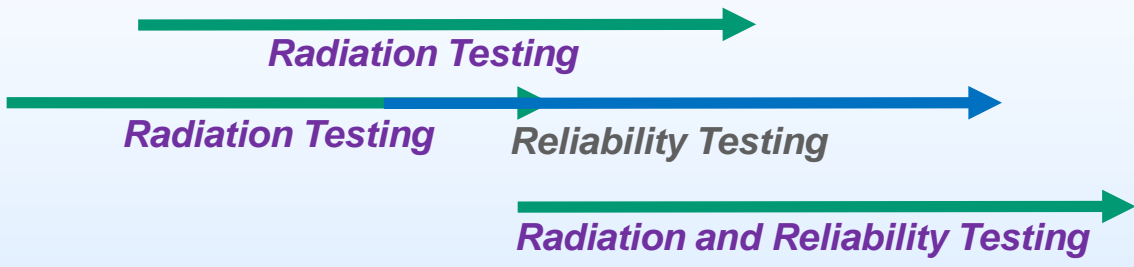
## Trusted FPGA

- DoD Development



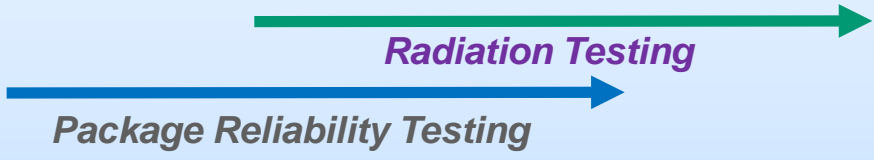
## Altera

- Stratix 5 (28nm TSMC process commercial)
- Max 10 (55nm NOR based commercial – small mission candidate)
- Stratix 10 (14nm Intel process commercial)



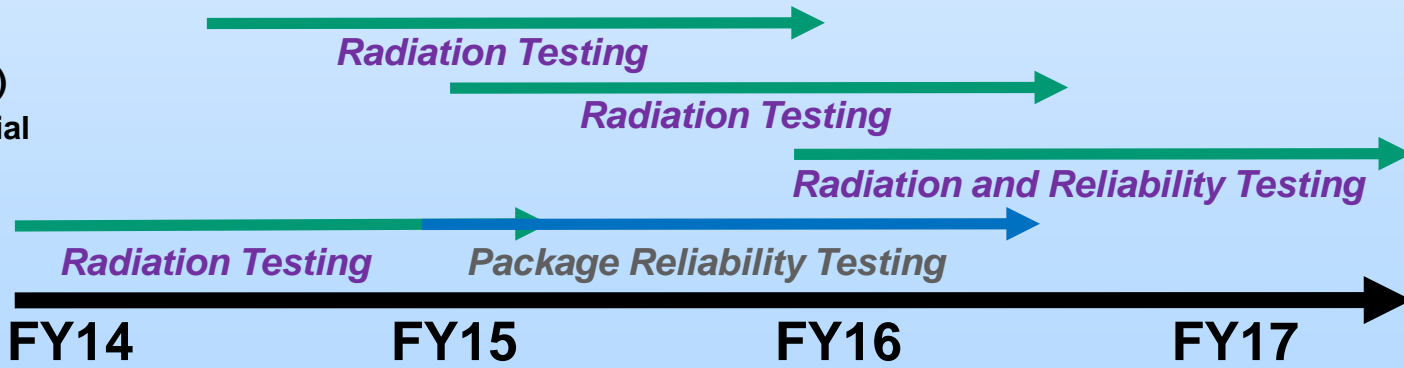
## Microsemi

- RTG4 (65nm RH)

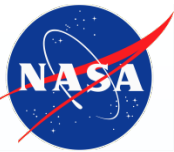


## Xilinx

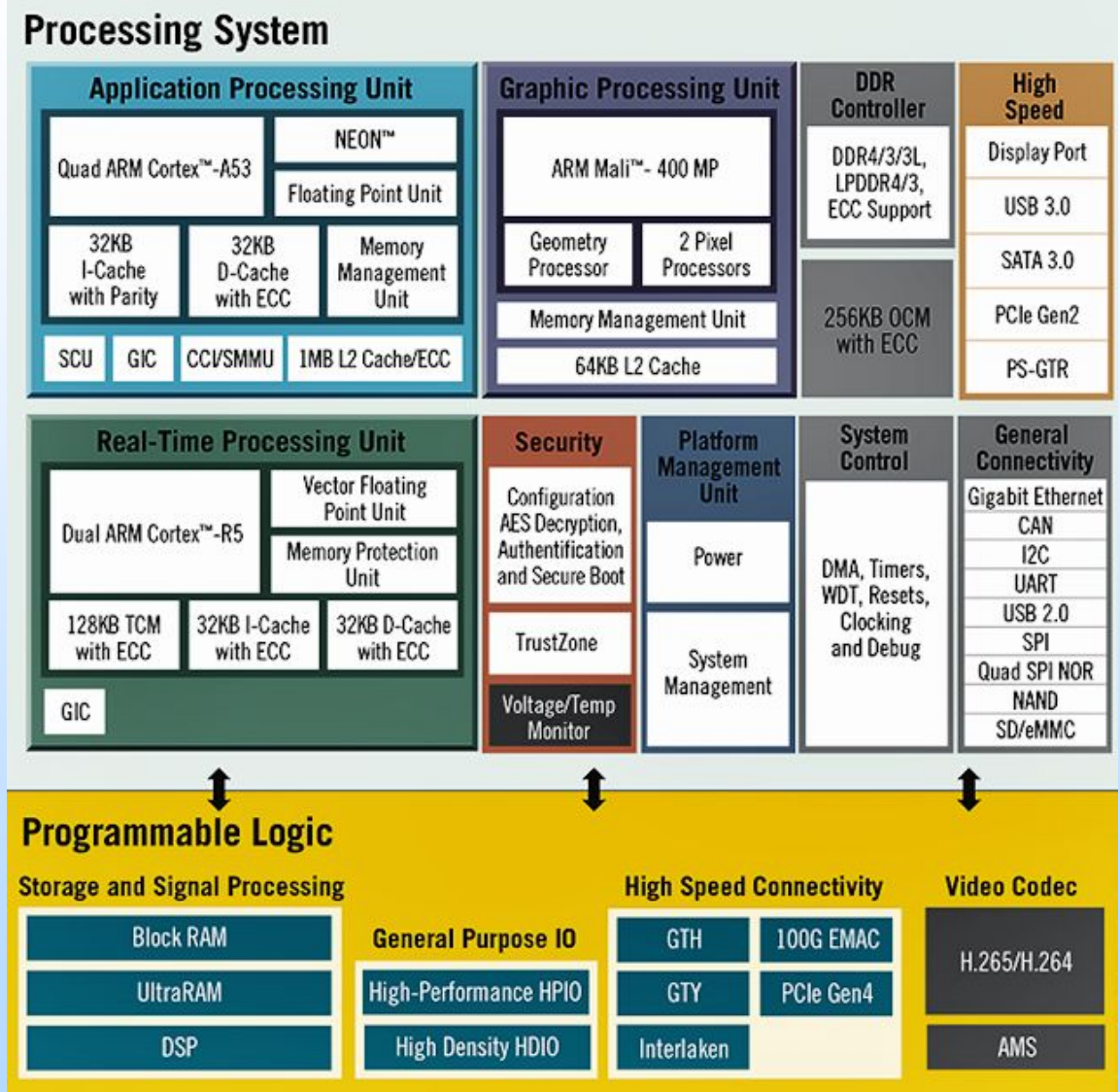
- 7 series (28nm commercial)
- Ultrascale (20nm commercial – planar)
- Ultrascale+ (16nm commercial - vertical)
- Virtex 5QV (65nm RH)







# Xilinx Zynq UltraScale+ Multi-Processor System on a Chip (MPSoC) family



*From Xilinx.com*



# Advanced Processors

## Next Generation Space Processor (NGSP)

- Joint NASA-AFRL Program for RH multi-core processor
- TBD architecture/process



## RH Processor

- BAE Systems RAD5510/5545
- Replacement for RAD750



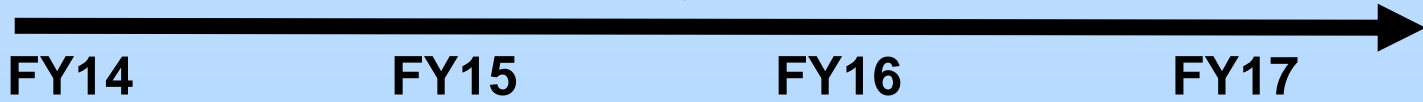
## Intel Broadwell Processors

- 14nm FinFET commercial
- 1<sup>st</sup> high-performance sans heatsink (lower power for performance)



## Freescale P5020/5040

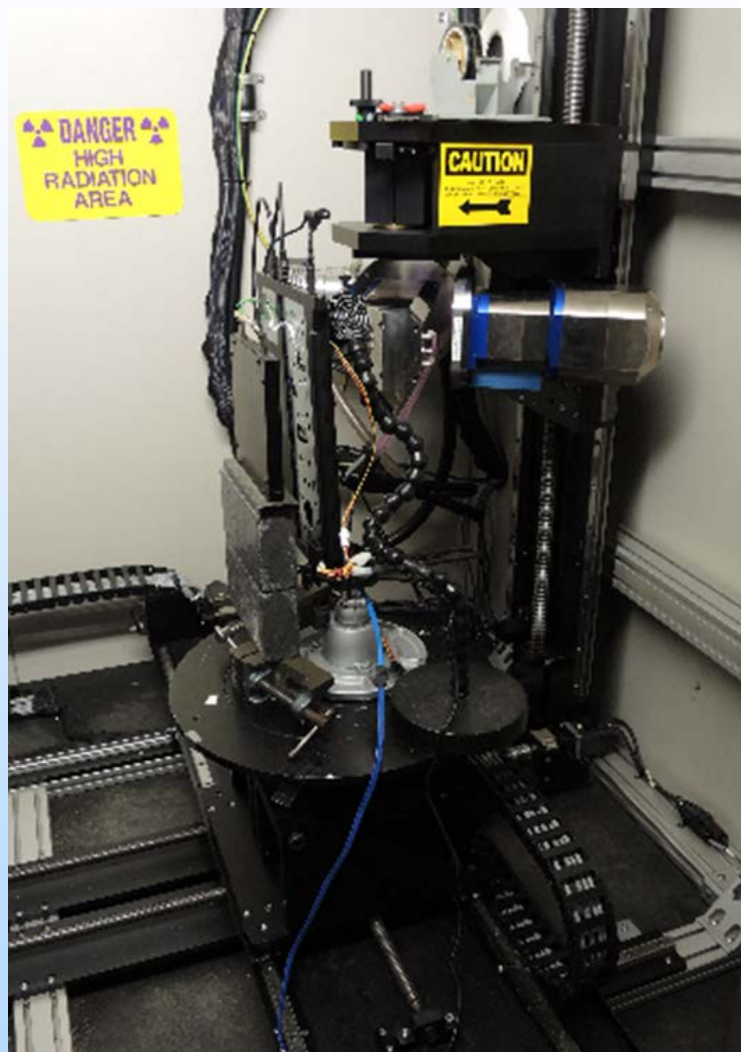
- Commercial 45nm network processor
- Preparation for RH processor

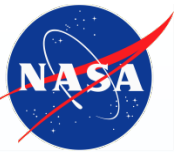


**Note: Future considerations under discussion include automotive “self-driving” processor options.**



# Preliminary Radiation testing of 14nm Intel with Navy Crane

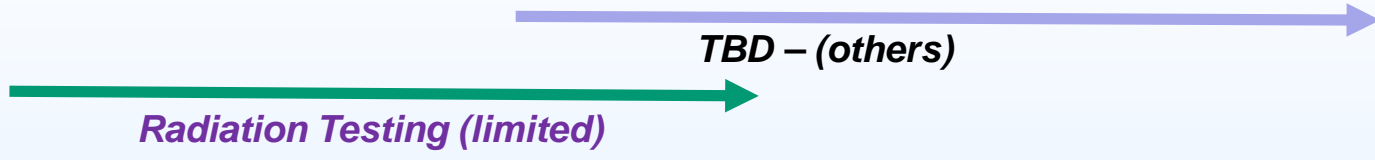




# Microcontrollers and Mobile Processors (Small Missions)

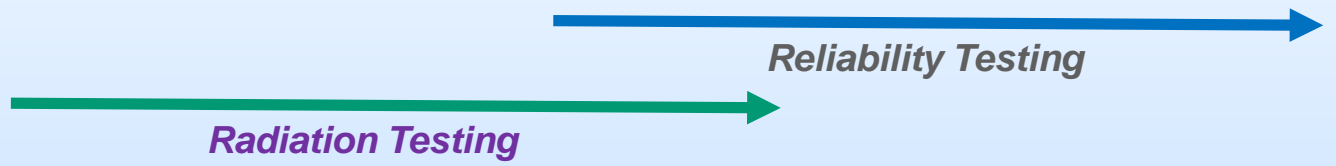
## TBD – other

- Atmel AT91SAM9G20, and TI Sitara AM3703,
- ARM (Snapdragon), Intel Atom mobile



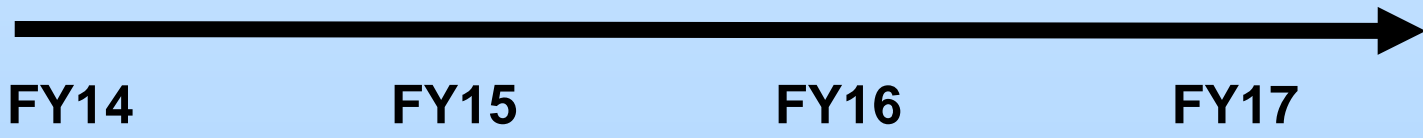
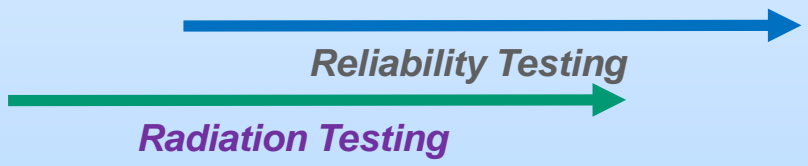
## TI MSP430

- Popular CubeSat microcontroller
- Several varieties



## Freescale MPC56XX

- 90nm on-shore fab
- Automotive Grade
- Being used for both part and board level testing





# Commercial Memory Technology

## Other

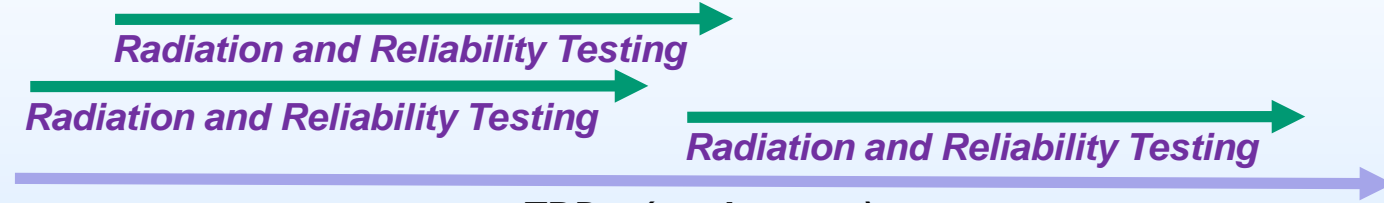
- MRAM
- FeRAM



*TBD – (track status)*

## Resistive

- CBRAM (Adesto)
- ReRAM (Panasonic)
- ReRAM (Tezzaron)
- TBD (HP Labs, others)



*Radiation and Reliability Testing*

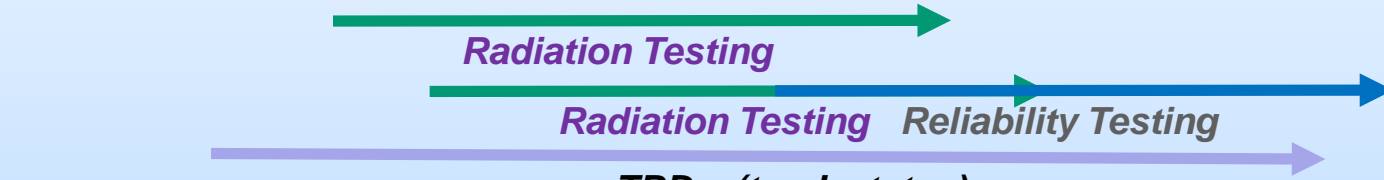
*Radiation and Reliability Testing*

*Radiation and Reliability Testing*

*TBD – (track status)*

## DDR 3/4

- Intelligent Memory (robust cell twinning)
- Micron 16nm DDR3
- TBD – other commercial



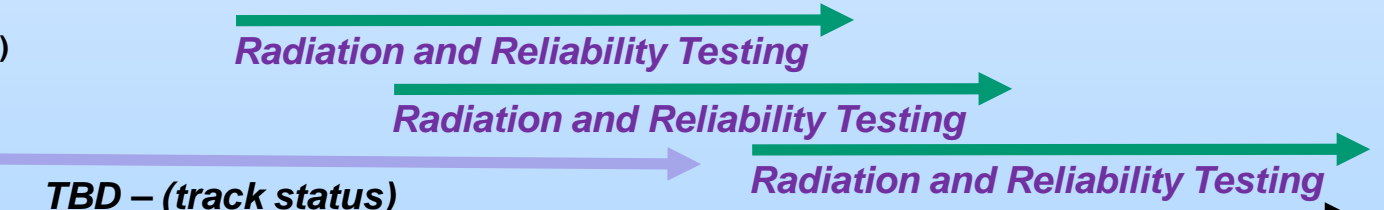
*Radiation Testing*

*Radiation Testing Reliability Testing*

*TBD – (track status)*

## FLASH

- Samsung VNAND (gen 1 and 2)
- Micron 16nm planar
- Micron Hybrid memory Cube
- TBD - other commercial



*Radiation and Reliability Testing*

*Radiation and Reliability Testing*

*TBD – (track status)*

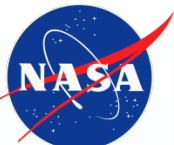
*Radiation and Reliability Testing*

**FY14**

**FY15**

**FY16**

**FY17**



# Small Missions

## EEE Parts Guidelines

- Small missions (Class D, CubeSat – 2 documents)
- System on a chip (SOC) single event effects (SEE) guideline



## Commodities evaluation

- See commodities roadmaps for processors, power
- CubeSat Star Tracker



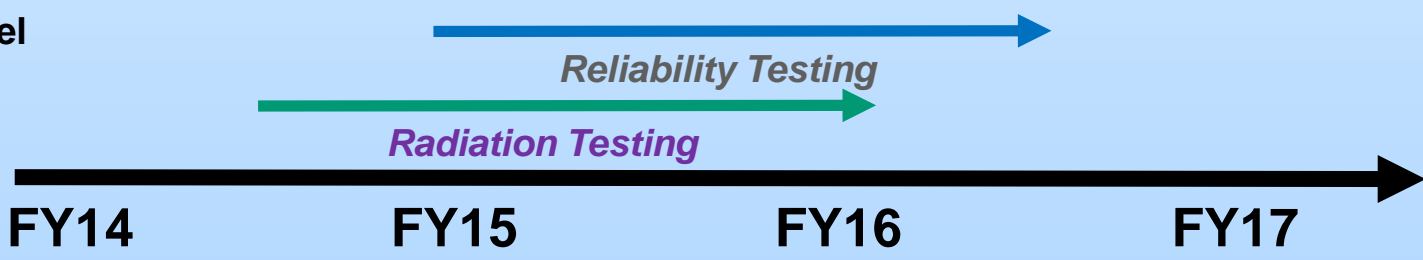
## Automotive grade electronics

- Multiple classes of electronics (passives, actives, ICs)
- Testing by NASA and Navy Crane



## Alternate test – board level

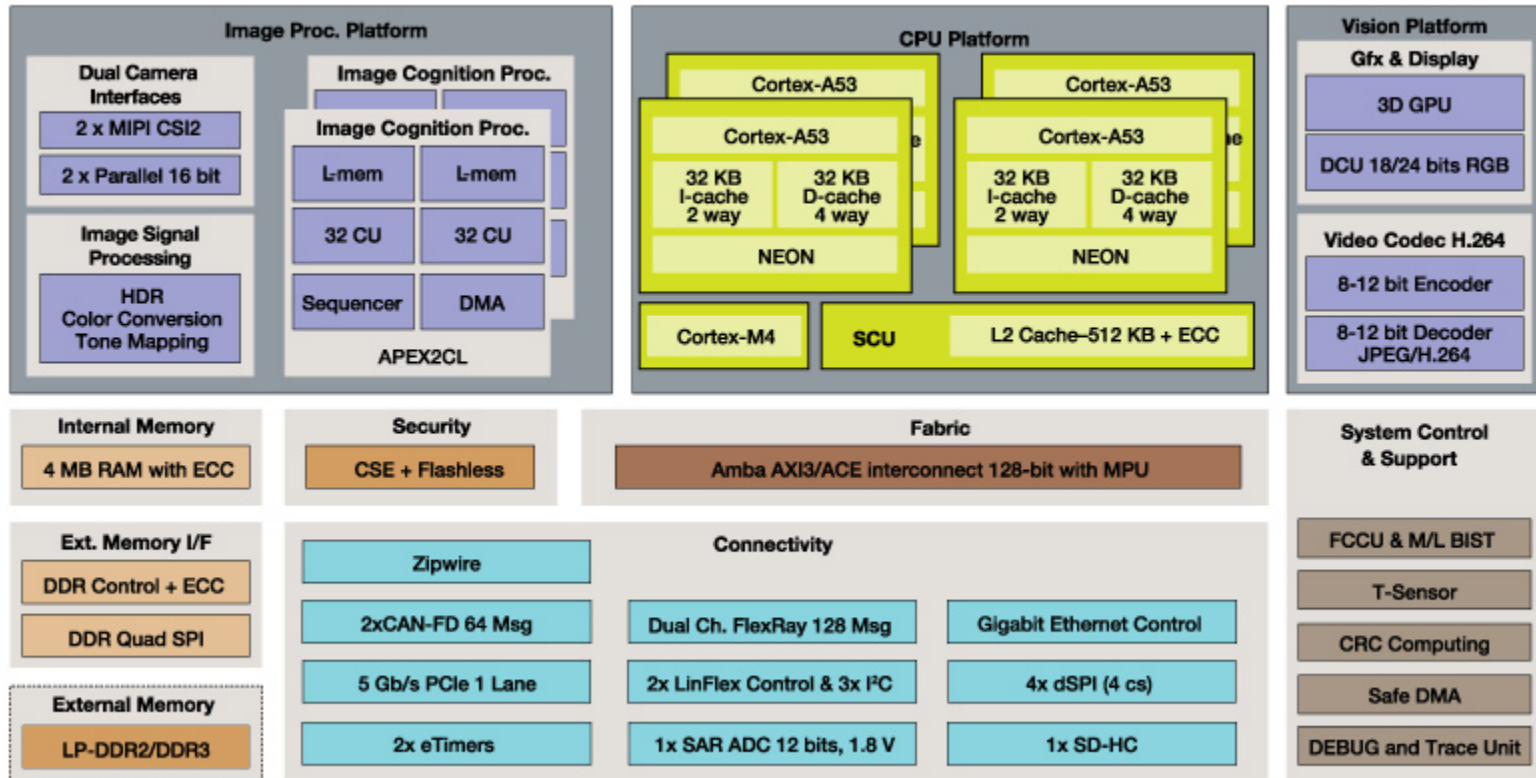
- Freescale MPC56XX
- Automotive Grade
- Both part and board level reliability testing





# Automotive Processors and Systems for Self-Driving Cars?

## S32V234 Block Diagram



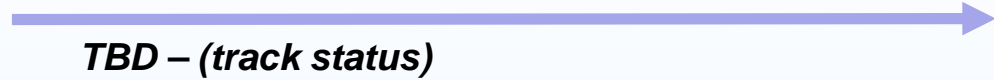
From Freescale.com



# Wide Band Gap (WBG) Technology

## GaN Class V development

- Microsemi with EPC



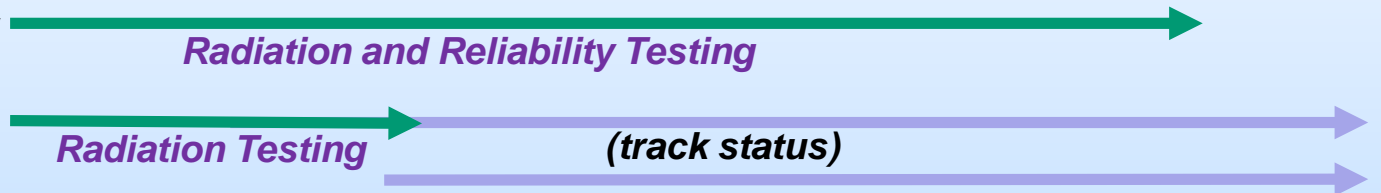
## GaN Enhancement Mode HEMTs

- EPC Gen 2-3, 200 V - 600 V
- GaN Systems 100 V, 650 V
- Panasonic 600 V (target)
- IR/Infineon 600 V (target)



## SiC MOSFETs

- Cree Gen 1-2 1200 V - 1700 V
- Gen 3- narrower neck
- STMicro baseline SEE test
- Rohm Trench design



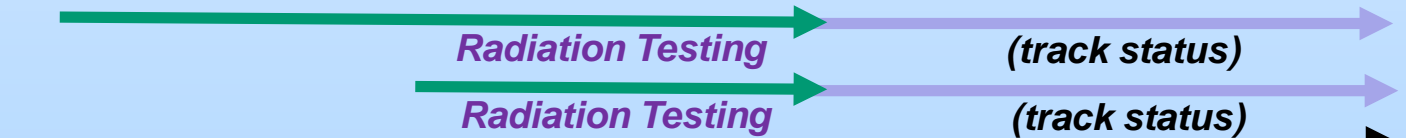
## SiC Diodes

- Manufacturer X SEE baseline and hardening efforts



## SiC ICs

- Ozark IC
- Manufacturer X



FY14                                      FY15                                      FY16                                      FY17

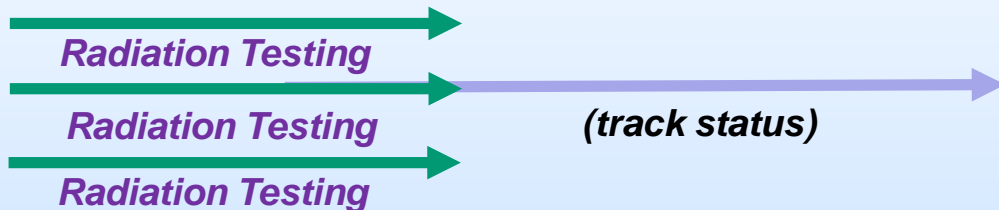




# Silicon Power Devices

## MOSFETs – Rad Hardened

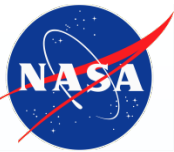
- Microsemi i2MOS
- Infineon superjunction  
100 V, 600 V (target)
- IR/Infineon R8 trench 20 V



## Schottky Diodes

- Multiple vendors, reverse voltage ratings, and forward current ratings





# Packaging Technologies (1 of 2)

## High Density, Non-hermetic Column Grid Array (CGA)

- Xilinx CN/Kyocera Daisy Chain
- Microsemi Daisy Chain
- *Materials analysis, long term stress, root cause failure*



## HALT Methodology/Qualification

- HALT/HAST comparison
- Plastic BGA matrix



## Area Array Column

- Selection guide

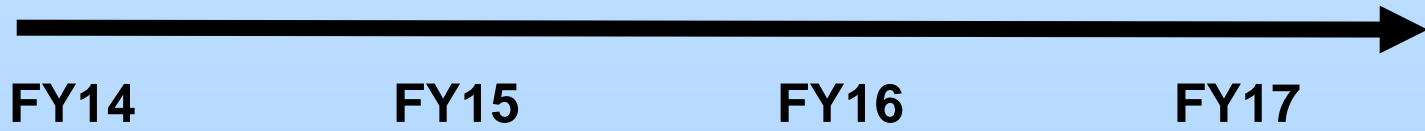


## Thermal Interface Materials

- Selection guide



## PBGA Thermal Cycle Evaluation





# Packaging Technologies (2 of 2)


## Bump Reliability

- Technology review
- Test vehicle options

  
*Guideline research*

## 3D Packaging Technologies

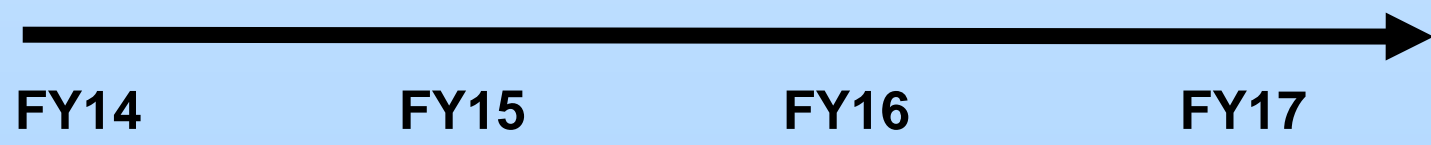
- Technology review
- Test vehicle options

  
*Guideline research*

## QFN package reliability

- Reliability/Qualification metrics

  
*Reliability Testing*

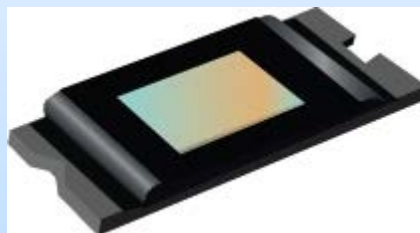




# And Just When You Think Your Roadmap is Set, New Parts are Released

- **Examples**

- **More complex processors**
  - TI Multicore DSP+ARM KeyStone II System-on-Chip (SoC)
- **Integrated “instruments”**
  - TI DLP2010NIR – near IR sensing and controller





# Summary and Comments

- **NEPP Roadmaps are constantly evolving as technology and products become available.**
  - Like all technology roadmaps, NEPP's is limited to funding and resource availability.
  - Not shown are TBD passives and connector roadmaps under development.
  - NEPP is working to develop preliminary plans on interfacing to the NASA Reliability and Maintainability Program and its work on Model Based System Engineering (MBSE) approaches.
- **We look forward to further opportunities to partner.**

***<https://nepp.nasa.gov>***