Advanced Stirling Convertor Dual Convertor Controller Testing at NASA Glenn Research Center in the Radioisotope Power Systems System Integration Laboratory

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NASA Glenn Research Center (GRC) developed a non-nuclear representation of a Radioisotope Power System (RPS) consisting of a pair of Advanced Stirling Convertors (ASC), a Dual Convertor Controller (DCC) EM (engineering model) 2 & 3, and associated support equipment, which were tested in the Radioisotope Power Systems System Integration Laboratory (RSIL). The DCC was designed by the Johns Hopkins University/Applied Physics Laboratory (JHU/APL) to actively control a pair of Advanced Stirling Convertors (ASC). The first phase of testing included a Dual Advanced Stirling Convertor Simulator (DASCS) which was developed by JHU/APL and simulates the operation and electrical behavior of a pair of ASC's in real time via a combination of hardware and software. RSIL provides insight into the electrical interactions between a representative radioisotope power generator, its associated control schemes, and realistic electric system loads. The first phase of integration testing included the following spacecraft bus configurations: capacitive, battery, and supercapacitor. A load profile, created based on data from several missions, tested the RPS and RSIL ability to maintain operation during load demands above and below the power provided by the RPS. The integration testing also confirmed the DCC's ability to disconnect from the spacecraft when the bus voltage dipped below 22 V or exceeded 36 V. Once operation was verified with the DASCS, the tests were repeated with actual operating ASC's. The goal of this integration testing was to verify operation of the DCC when connected to a spacecraft and to verify the functionality of the newly designed RSIL. The results of these tests are presented in this paper.

Nomenclature

ACU	=	advanced Stirling convertor control unit
A/D	=	analog to digital
ASC	=	advanced Stirling convertor
D/A	=	digital to analog
DASCS	=	dual advanced Stirling convertor simulator
DAQ	=	data acquisition system
DCC	=	dual convertor controller
DSP	=	digital signal processor
EM	=	engineering model

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EMI = electromagnetic interference
GRC = Glenn Research Center
GSE = ground support equipment
FCDA = facility control and data acquisition
FET = field effect transistor
FPC = failsafe protection circuit
FPGA = field programmable gate array
IEEE = Institute of Electrical and Electronic Engineers
IGBT = insulated gate bipolar transistor
IV&V = independent verification and validation
JHU/APL = the Johns Hopkins University/Applied Physics Laboratory
PDCU = power distribution control unit
PID = proportional integral derivative
PMAD = power management and distribution system
PWM = pulse width modulation
RMS = root mean square
RPS = Radioisotope Power System
RSIL = radioisotope power system systems integration laboratory
SRU = shunt regulator unit
SSPC = solid state power controller

I. Introduction

The Radioisotope Power Systems (RPS) program has worked to develop Advanced Stirling Convertor (ASC) technology for applications in future space missions. After extended operation of the ASCs at Glenn Research Center (GRC), it was determined a need existed for the ability to verify and validate RPS units that are unfueled. This is driven by the fact that contractors who build RPS units and spacecraft developers can change over time requiring the RPS Program to develop and sustain the capability to test generator to spacecraft electrical interfaces. This capability allows the RPS Program and Planetary Science Division Missions to validate and verify current and future electrically heated RPS unit operations, providing for a better understanding and characterization of fueled units. In addition, spacecraft vendors will require data on the RPS units that only NASA, as an independent agency, can provide. This avoids duplication of work among contractors, potential conflicts of interests and ensures that information is properly shared across the community and archived for future application. The resulting test bed, the Radioisotope Power System Systems Integration Laboratory (RSIL), is capable of simulating an end-to-end power system in order to provide insight into the electrical interactions among a representative RPS, its associated control scheme and realistic electric system loads. The RSIL addresses five major goals:

1) Provides the ability to IV&V RPS generators for missions
2) Provides future missions with the capabilities to verify their spacecraft power system designs
3) Provides electrical test bed for current missions in development and already deployed
4) Supports the RPS product line development by providing the capability to test new technologies related to RPS power systems
5) Provides future missions with the capabilities to verify their fault protection and flight software, relating to RPS.

This paper presents the first RSIL test series which utilized two ASC convertors, a dual advanced Stirling convertor simulator (DASCS), and dual convertor controller (DCC) EM (engineering model) 2 & 3.

II. Testing Components

A. ASC

The ASC-1 #3 & #4, second generation prototypes shown in Fig. 1, were designed and fabricated by Sunpower, Inc. These convertors were designed to operate at the parameters shown in Table 1.

Table 1. ASC-1 #3 & #4 Operating Parameters.

Maximum operating temperature		**Alternator voltage**	**Alternator Current**	**Alternator Power**	**Charge Pressure**
T_{hot}	T_{cold}				

(°C)	(°C)				
850	90	12 V_{rms}	7 A	80 W	515 psig

ASC-1 #3 & #4 are oriented in the dual-opposed configuration, with the heater heads facing outward and the pressure vessel sections rigidly attached to each other. This configuration permits operation at near zero net vibration because the piston motions are equal but opposite in direction to achieve dynamic balance.

The ASC support hardware was designed to allow adjustment of operating conditions, including: hot-end and rejection temperatures, piston amplitude of oscillation, and mean charge pressure of the working gas. The ASC's were instrumented to measure these parameters and all output characteristics, such as alternator voltage, alternator current, operating frequency, and alternator power. The hot end of each ASC is heated with electric cartridge heaters and the rejection temperature is maintained with a water/glycol bath.

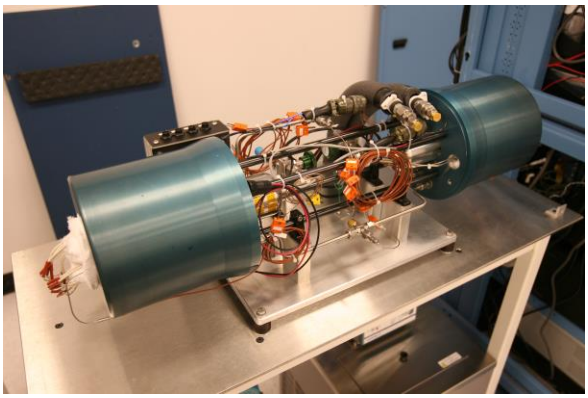

Figure 1. Photograph of ASC-1 #3 & #4.

B. DCC EM 2 & 3

A block diagram of the DCC connected to a convertor and a typical redundant spacecraft is shown in Fig. 2. The DCC consists of two identical controller boards packaged in separate chassis. A photograph of theDCC is shown in Fig. 3. Each board is capable of controlling both ASC channels. One controller board is actively in control of both convertors at all times, while the other is a hot standby used to recover from a fault. Each controller board contains the power handling, data acquisition, signal processing, and secondary voltage conditioning circuits needed to control two convertors and deliver DC power to the spacecraft. A block diagram of the controller board is shown in Fig. 4.

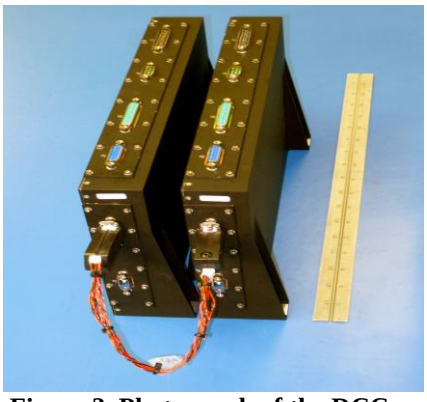

Figure 3. Photograph of the DCC.

Power flows from each convertor through an electronic switch for each channel that acts as an AC circuit breaker. The AC circuit breaker is opened in the event of a fault to isolate the convertor from the failure and allow the redundant board to initiate control. Transient suppression devices on each controller board clamp voltage spikes that may occur when an AC breaker is opened. A field effect transistor (FET) H-bridge is pulse width modulated (PWM) as determined by the control law implemented in the field programmable gate array (FPGA). The H-bridge output is a DC voltage but with a large ripple current. That node is connected through an output buck regulator stage designed to minimize ripple in spacecraft output load current rather than maintain a specific output voltage. The regulator also limits current while connecting to the spacecraft load. An additional FET switch in combination with the buck regulator will isolate the load and controller from faults in either. An electromagnetic interference (EMI) filter on the board limits switching noise propagating from the controller to the spacecraft load. While the output regulator/DC breaker FETs are open, convertor power flows to an external shunt resistor controlled using a pulse width modulated FET based regulator to maintain a fixed H-bridge output voltage.

The control law inputs and key status analog voltages are digitized by a 12-bit analog to digital converter (A/D) and processed by logic in the FPGA. The control law is implemented digitally by a co-processor in the FPGA. The

co-processor contains an Institute of Electrical and Electronics Engineers (IEEE) single precision compliant data path controlled by a finite state machine sequencer programmed to implement the control law algorithm. A 16-bit microcontroller, also implemented in the FPGA, adjusts control law parameters, accepts user commands, and produces status telemetry. A combination of analog circuits, FPGA logic, and microcontroller software monitor DCC operation and detect and correct potential faults. A custom-designed DC/DC converter accepts input power from the spacecraft bus or external source and provides secondary voltages to board circuitry.

The DCC not only provides power to the spacecraft but it also must regulate operation of both ASCs to avoid damage to their internal components and maintain safe thermal conditions after fueling. The two controller boards are fully redundant. If a board fails, the redundant controller board will continue to safely operate the ASCs. Commands to the active controller board can also electrically isolate the backup board so that it can be replaced without use of external equipment to restore fault tolerant operation. Analysis and simulation of the methods used to detect and recover from faults without damage to the ASCs as well as the ASC control algorithm are described in [Ref 1].

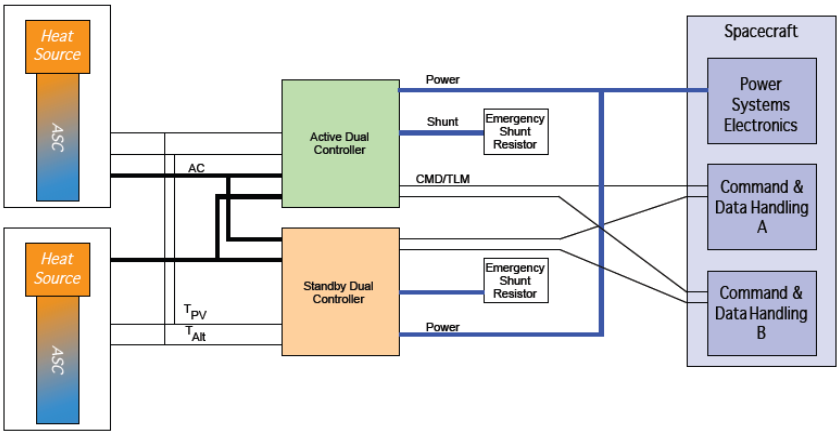

Figure 2. DCC spacecraft application.

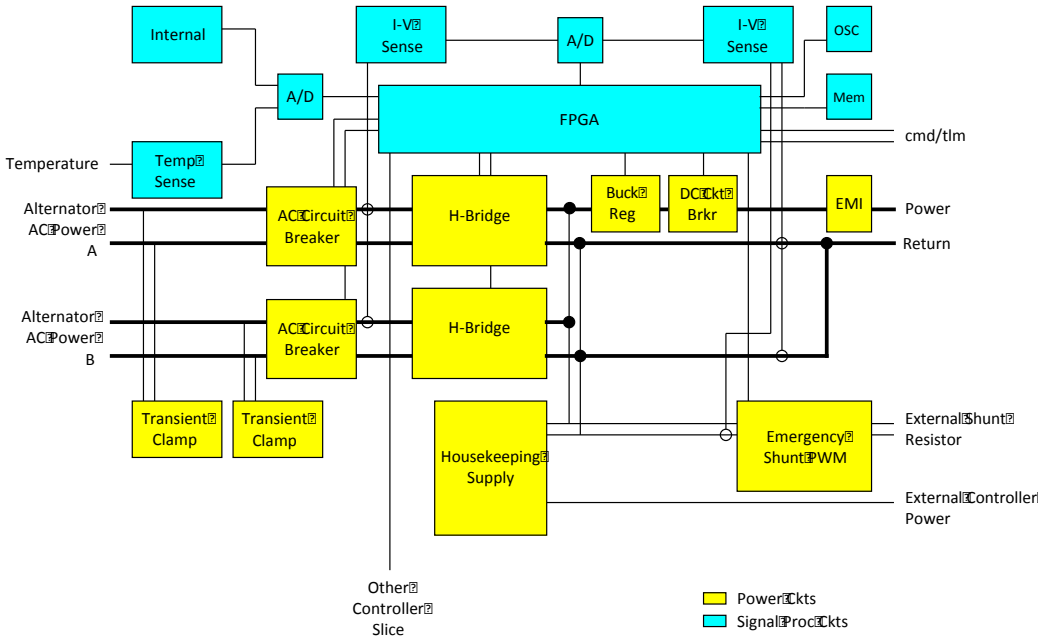

Figure 4. DCC board block diagram.

C. DASCS

A DASCS was developed using custom-designed circuits, commercial equipment, and a linearized ASC model [Ref 2] implemented in software on an off-the-shelf digital signal processor (DSP) development board. A block diagram including user interface capabilities of the DASCS is shown in Fig. 5 while a photograph of the DASCS is shown in Fig. 6.

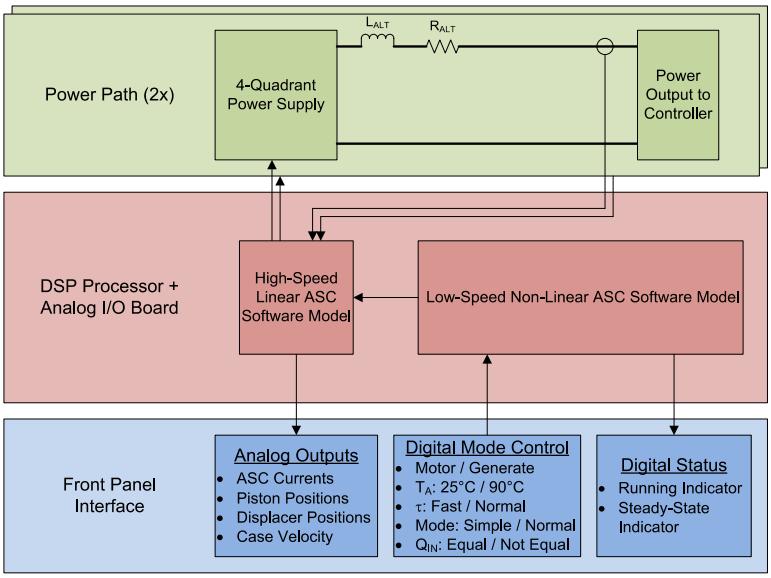

Figure 5. DASCS block diagram with user interface.

Alternator inductance and resistance are modeled with physical components with electrical properties similar to the actual alternator in series with a back emf voltage source. A commercial current sensor is filtered and then digitized by an A/D in the DSP development system. The DSP is programmed to use the input current to calculate and produce an output voltage through a digital to analog converter (D/A), also part of the DSP, proportional to the ideal converter back emf voltage based on the ASC model equations. The back emf voltage passes through an electrical isolator and is then used to control the output of a 400W commercial power supply. The power supply output is the equivalent of the back emf output of the convertor alternator. The DASCS output is calculated from ASC model equations and includes convertor mechanism dynamics beyond the alternator electrical inductance and resistance. The DASCS can be reprogrammed to mimic other types of ASCs by changing the linear model implemented in the DSP and the physical alternator inductance and resistance components.

Previous engine simulator designs used an AC source, resistor, and inductor and only modeled electrical performance with no consideration of convertor mechanical behavior. Designers frequently found that their controllers did not function the same with an ASC as with their engine simulator. The impact of controller problems like AC input current sampling noise or spacecraft bus voltage changes on mechanical parameters like piston amplitude could only be investigated using time-consuming testing with a real ASC. In addition, damage to the ASC might occur during such evaluations.

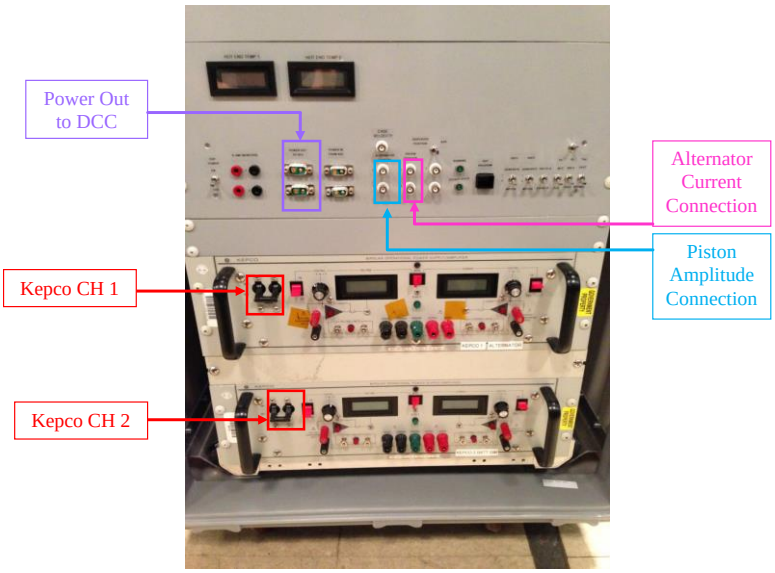

Figure 6. DASCS photograph.

The DASCS was used to test the DCC prior to operating with an actual ASC. The DASCS helped solve numerous nonlinearity and noise-related problems in sensing the alternator current. Overcoming those issues reduced output power fluctuations at the load, resulting in smaller peak-to-peak variations in piston amplitude and improved operating efficiency. The effectiveness of the DASCS was shown when the ASC was successfully controlled, at full power, on the first attempt by the DCC controllers. If DCC testing was only performed with an ASC, the success of the controller design and its 2-year time to full-power ASC demonstration would not have been possible. The same behavior observed while testing with the ASC was also seen

while testing with the DASCS including piston amplitude noise, controller efficiency, and sensitivity to load changes. The DASCS also provides an easy-to-use environment for debugging and testing fault detection and recovery of the DCC without risk of damage to a real ASC.

D. Support Hardware

The test rack comprises the data system, hard-wired failsafe protection devices, hot-end temperature control systems, power meters and DCC commanding and support hardware. The data system utilizes National Instruments' LabVIEW-based data acquisition (DAQ) hardware and software to acquire data and monitor the test. It displays and records data on a computer, collects and saves data in various time frames, calculates parameters with received data, and provides safety to the convertors. The DAQ software, which was developed to operate in unattended mode, can control the support systems without user intervention.The user may specify upper and lower bounds for any parameter monitored by the DAQ system. The DAQ software will safely shut down operation of the test article when an out-of-bounds condition is sensed. Parameters that may trigger a shutdown include: hot-end and rejection temperatures, convertor mean charge pressure, piston amplitude of oscillation, and loss of building power. Data collection allows for detailed analysis of ASC operation. To achieve this, LabVIEW collects and displays several parameters, including

- Heater voltage and current
- Electric heat-source temperature
- Hot-end, cold-end, ambient, and pressure vessel temperature
- Alternator root mean square (RMS) voltage, RMS current, and power
- Piston amplitude
- ASC operating frequency
- Power factor
- DASCS voltage, current and power

A complete data record of these parameters is stored every hour. In addition, the DAQ system maintains a buffer of data recorded over the last 24 hours at a 2-second scan rate, records an average of the data over the last 5 minutes of every hour, and allows these data to be stored manually as needed for detailed analysis. From the stored data, numerous parameters are calculated, including

- Heater resistance and power
- Average hot-end temperature
- Cold-end temperature
- Piston amplitude
- Net heat input

Hard-wired protection devices were also installed in the operations rack that function independent of the software-based protection. The hot-end temperature of each convertor is monitored by a limit controller. If either hot-end temperature exceeds the user-defined limit, the limit controller removes heater power from both ASC's via a relay. A failsafe protection circuit (FPC) was implemented to prevent piston over-stroke. When the user defined piston amplitude is exceeded, the controller is disconnected and an emergency load is applied across both alternators in less than one-half of a piston cycle.

Hot-end temperature control is accomplished by use of programmable DC power supplies driven by closed-loop proportional-integral-derivative (PID) controllers. Each hot-end temperature is controlled individually. Power input and output are measured using power meters and are recorded by the DAQ system.

Support hardware for the DCC include a DC electronic load, shunt resistors, capacitors, ground support equipment (GSE) power supply, and terminal emulator. The DCC relies on a DC electronic load to sink power in an output voltage range between 22.0 and 36.0 V_{dc} and is determined by the end user. The DCC will track to this voltage, providing power as a constant-power source, and will sense a bus overvoltage condition. The DCC will provide constant power as long as the end user is in the required voltage range, but it will internally shunt power and disconnect itself from the bus if the voltage range is exceeded. Shunt resistors sized for maximum output power of the convertors are mounted on the test stand for this purpose. The bus is connected to a capacitor bank for transient energy storage that allows a range of 10,000 to 100,000 µF. During motoring of the ASC's, power is provided to the internal DCC circuits by means of a DC power supply in the test rack. When the ASC's are producing positive power, the power supply is no longer needed and is turned off. The terminal emulator provides an interface for commanding the DCC. These commands include:

- Changing the voltage applied to the convertor , Vm
- Convertor operating frequency

- Disconnect from the spacecraft
- Connect to the spacecraft
- Operation with or without the backup controller card
- Open load or short circuit fault injection

III. RSIL

The RSIL is comprised of five major components designed to simulate a prototypical spacecraft which is powered by a RPS. The major components shown in Fig. 7 are: RPS power sources (the test article, here a pair of ASC convertors), a power management and distribution system (PMAD), an energy storage system (i.e. bus capacitor, battery or super capacitor), electrical load simulators, and a flight control computer simulation. These components are connected together to simulate a spacecraft's main electrical bus feeding a set of electrical loads all powered by RPS generators. This integrated electrical system tests RPS generators as part of an end-to-end spacecraft system rather than as stand-alone power generators. RSIL's spacecraft simulation capabilities are:

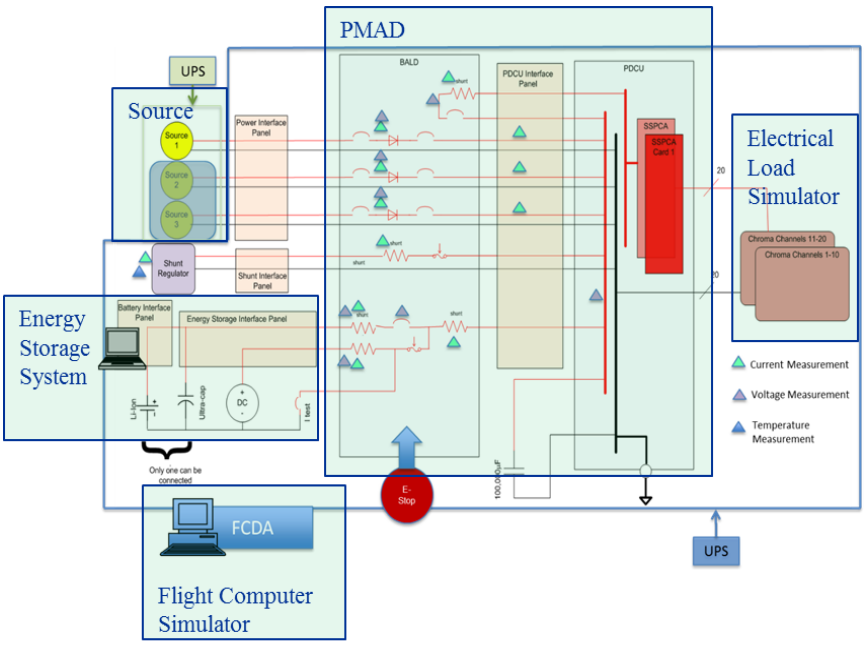

Figure 7. RSIL system architecture.

- Generators: 1, 2, or 3 200W RPS generators.
- Energy Storage: 100,000 µF bus capacitor, 165F supercapacitor, or 24A-hr Li+ battery
- Electrical Loads: 20 channels at 100W each.
- Main Bus:
  - Regulation: ±0.05 volts with power shunt engaged.
  - Control Range: 22 to 38 volts (26 to 33 with Li+ battery)
- Battery Charging: Adjustable rate limit 2 to 25 amp.

The power management and distribution subsystem consists of an interface unit, power distribution and control unit (PDCU) utilizing solid-state power controllers (SSPCs) for load switching, and a shunt regulator unit (SRU) to shunt excess power not used by the loads and to regulate charging of the energy storage device. The electronic loads consist of 20 independent channels capable of simulating constant resistance, constant current, constant power or constant voltage loads. An overall facility control and data acquisition system (FCDA) manages the data storage and display. The RSIL can be configured in 3 ways:1) stand-alone bus capacitor, 2) bus capacitor with a battery unit, and 3) bus capacitor with a supercapacitor. Since the ASC's are constant power sources, the energy storage unit is used to provide power at times when the load demand exceeds the source capabilities.

In addition to these components, the RSIL incorporates an electrical safety system in the event of system failures. The control panel, which monitors various system signals, and associated alarm panel are shown in Fig. 8. The safety system includes 2 levels of safety: alarms and shutdowns, with the emergency shutdown logic shown in Fig. 9.

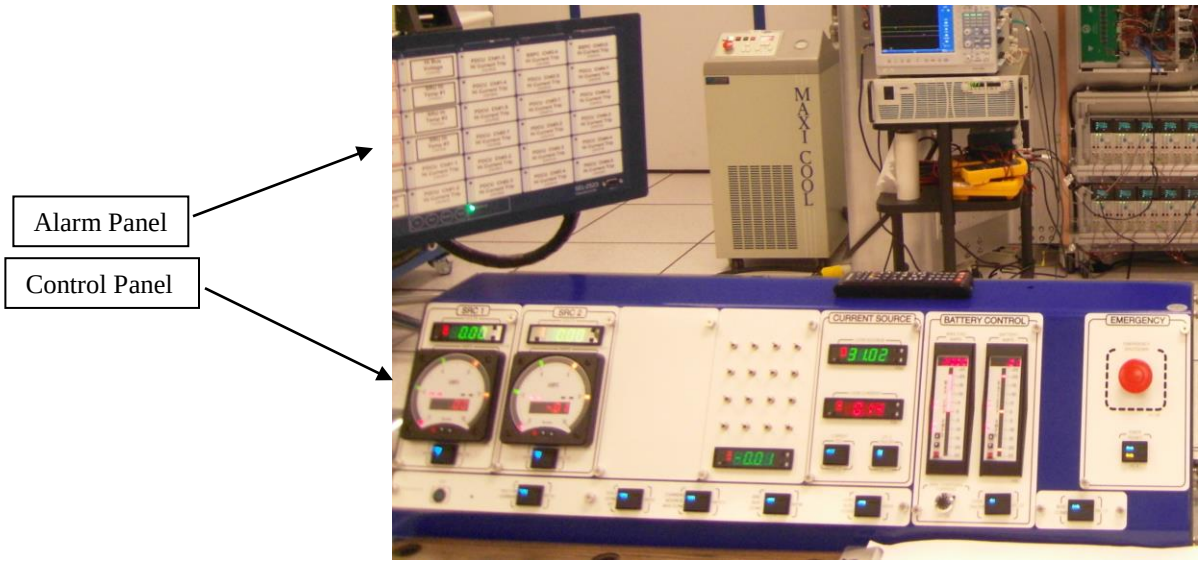

Figure 8. Control and alarm panels.

Electric power distribution system parameters, voltages, currents, and temperatures, are continuously monitored for out-of-tolerance operation. The monitors provide audible and visual alarms. The RSIL operator is responsible for correcting the out-of-tolerance condition.

Electrical power parameters that are out-of-limit trigger an automatic emergency shutdown procedure. This shutdown procedure can also be initiated by the RSIL operator. Visual and audible alarms annunciate occurrences. The emergency shutdown procedure for RSIL is:

1. Removes all energy sources from the spacecraft simulator via mechanical contactor.
2. Disconnects all loads from the simulator via mechanical contactor.
3. Notifies ASRG test controls of the event.

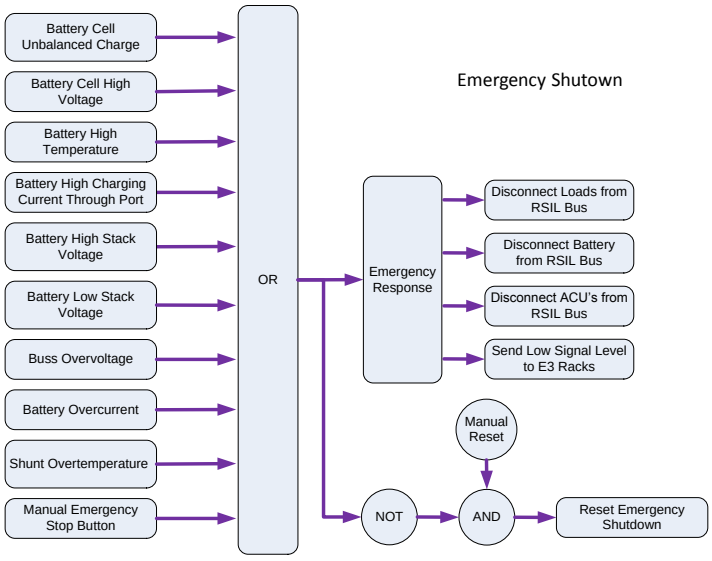

Figure 9. Emergency shutdown diagram.

The goal of the initial set of tests with the non-fueled RPS equipment mentioned in Section 1 was to validate the functionality of the RSIL platform prior to integration with an Advanced Stirling Convertor Controller Unit (ACU) and a pair of DASCS's.

IV. Single Input Channel Testing

For the single input channel testing, the DCC EM 2 & 3 was connected to the RSIL and operated with ASC-1 #3 & #4 for a flight-like hardware simulation of an RPS connected to a spacecraft. A photograph of the test setup is shown in Fig. 10. The ASC-1 #3 & #4 operating points for this test are listed in Table 2.

Table 2. ASC operating parameters.

Convertor Power Level (W)	Hot-end (°C)	Cold-end (°C)	Piston amplitude (mm)	Alternator Voltage (V)	Alternator Current (A)	Charge pressure (psig)
120	650	25	3.5	12.5	6.7	515
138	650	25	4.0	13.7	7.0	515

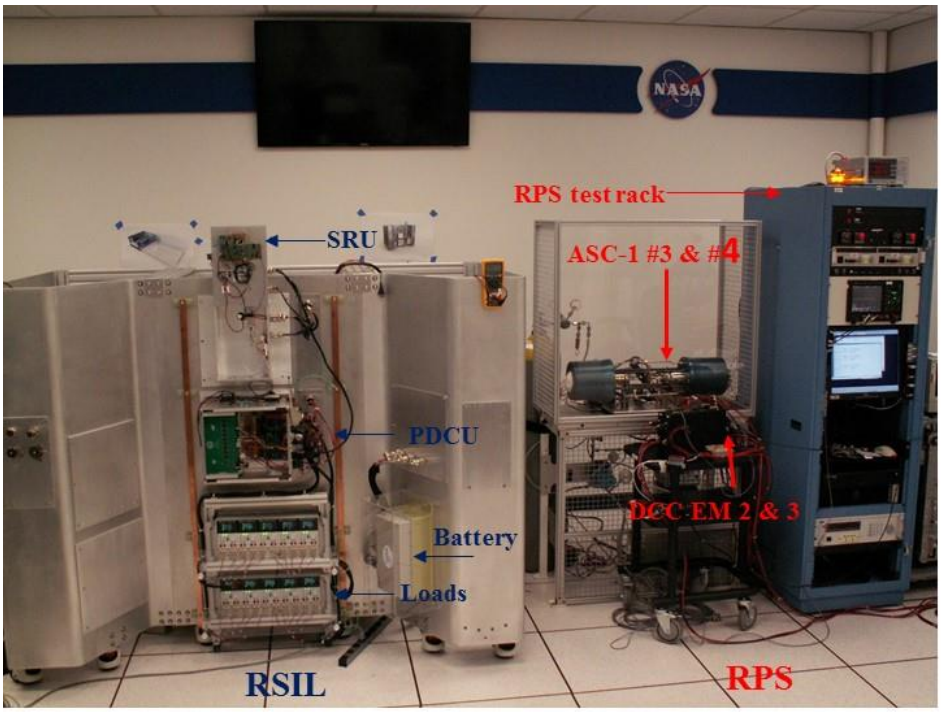

Figure 10. RSIL and RPS setup.

Prior to integration of the ASC's with RSIL, a suite of testing with a DASCS, listed in the first part of Table 3, was performed to verify both the functionality of the DCC and RSIL. The DASCS has proved to be a reliable testing resource, due to the design and testing as described in Section IIC, to mitigate risk to ASC hardware. For all tests, the DASCS, DCC, and RSIL operated as predicted with the DCC maintaining control of DASCS, and RSIL managing the power bus via energy storage and dissipative loads. The results of this testing are not shown in this paper for brevity.

Table 3. Summary of single input channel testing in RSIL.

Test Configuration	Energy Storage	Test
DASCS 120 W and 138 W ASC Power Output	Capacitor	Load Step Change
		Short Circuit
	Supercapacitor	Load Step Change
		Load Profile
		Voltage Limit
		Short Circuit

	Battery	Load Profile
		Short Circuit
DASCS 138 W ASC Power Output		Load step change
ASC-1 #3 & #4 120 W ASC Power Output	Capacitor	Load Step Change
		Voltage Limit
	Supercapacitor	Load Step Change
		Load Profile
		Voltage Limit
		Short Circuit
	Battery	Load Step Change
		Short Circuit
ASC-1 #3 & #4 138 W ASC Power Output	Capacitor	Load Step Change
		Voltage Limit
	Supercapacitor	Load Step Change
		Voltage Limit
		Short Circuit
	Battery	Load Step Change
		Load Profile
		Short Circuit

Single input channel testing included operations using capacitive, battery, and supercapacitor bus configurations. The results presented in this paper include DCC operation with ASC-1 #3 & #4 at both 120 and 138 W convertor power output. RSIL scope traces are only included in this paper at the 120 W convertor power output level. It should be noted that the power received by RSIL is approximlatey 25 W less than that provided by the ASC due to line loss and an apprximaltey 88% efficient DCC. The RSIL power is listed in each testing section below.

Four main tests were completed during RSIL testing which included load step change, load profile, voltage limit, and short circuit.

1) The load step change test verified the RSILs ability to respond to a change in the load demand. It also verified that the DCC and ASC were not impacted by this load change. Step changes in electrical load were executed using the Chroma programmable loads using the following settings:
   - Constant load current regulation.
   - 2 amp/μsec current slewing rate.
2) A load profile, based on data from several representative missions, tested the RPS and RSIL ability to maintain operation during load demands above and below the power provided by the RPS. The load profile used during the ASC 120 W power tests is shown in Fig. 11. When the RSIL required more power than the RPS could accommodate, the energy storage device (supercapacitor or battery) supplied the additional power. When the RSIL demanded less power than what the source provided, the shunt regulator unit dissipated the excess power.
3) The voltage limit tests verified the DCC's ability to disconnect from the RSIL when out of range from 22-36 V bus voltage for which it was designed.
4) The short circuit test verified the RSIL's ability to respond to a short on one of the loads. For the short circuit test, a switch-operated Insulated Gate, Bipolar Transistor (IGBT) was connected across the inputs to a Chroma load with the IGTB's emitter connected to the power return. When the IGBT's gate was energized, the device shorted the high side of the Chroma's input to the return power connection. Shorting events were induced manually by the RSIL Operator. The IGBT used was a Fuji Electric 1MBI400-060 unit with ratings of 400 amps, 600 volts.

Prior to connecting to RSIL, the ASC's are brought to full power operation with the DCC dissipating power in external shunt resistors (as described in section II.D). When steady state operation of the ASC's is achieved, a command is sent to the DCC to connect to RSIL.

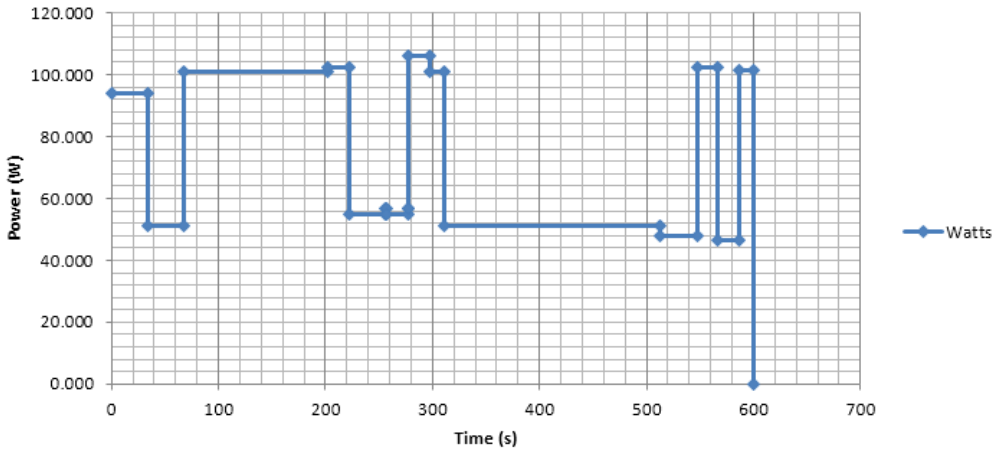

Figure 11. 106 W maximum load profile.

A. Capacitor bus

Two tests were performed in the RSIL bus capacitor configuration at both the 120 and 138 W convertor power output level: load step change and voltage limit testing. Table 4 describes the bus voltage and current at each power level. Fig. 12 depicts the shunt tracking (dissipating) of the source current at the 120 W convertor power output. Fig 14 and 15 show the ASC-1 #3 alternator voltage, current and power and piston amplitude response during the capacitor bus tests.

Table 4. Bus voltage and current for capacitor bus testing.

Power Level (W)	Bus Voltage (V)	Bus Current (A)	RSIL Power (W)
120	28.6	3.54	101.2
138	N/A	N/A	113

The load test at the lower power level consisted of a positive 3 A load step change, followed by a 2 A step decrease, and then removal of the remaining 1 A load. Fig. 13 shows the results of trhe 3 A increase. All systems operated as expected with no disturbances seen at the RPS.

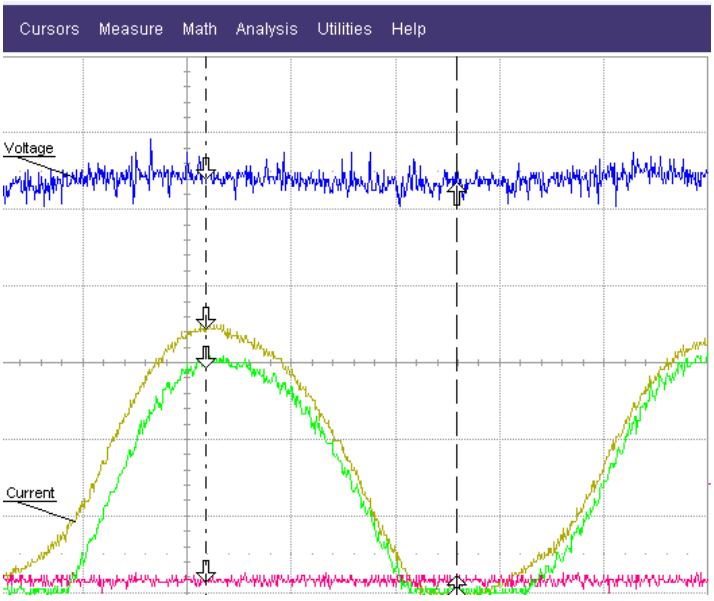

Figure 12. 120 W: no added energy storage.

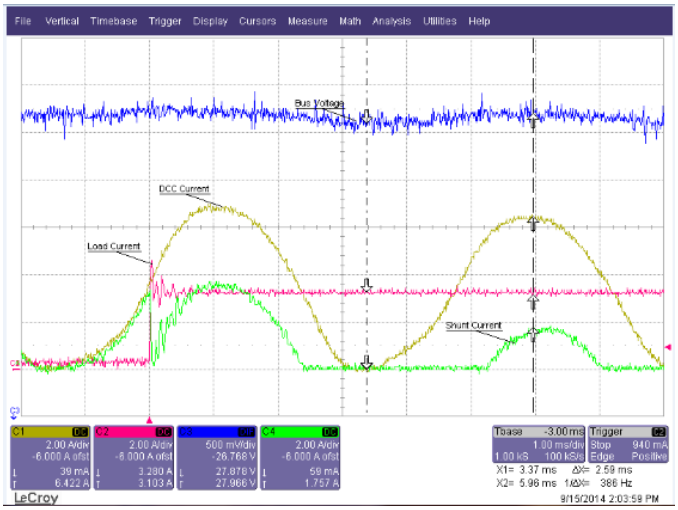

Figure 13. 120 W: 3A load step change with bus capacitor.

The load step change test at the higher ASC output power level consisted of applying 2 A on each of two load channels. All systems operated as expected with no disturbances seen at the RPS.

For the voltage limit tests, the bus voltage was raised above 36 V and then lowered below 22 V to verify the DCC's ability to disconnect from the bus when out of range from its designed bus voltage range. Table 5 shows the voltage at which the DCC disconnected at each convertor power output level. The DCC successfully disconnected when out of range of the 22-36 V bus voltage for which the unit was designed.

Table 5. Bus voltage at disconnect for capacitor bus testing.

Convertor Power Output (W)	Low Voltage Disconnect (V)	High Voltage Disconnect (V)
120	20.8	36.05
138	20.52	36.8

This paper presents tests results for ASC-1 #3 only but ASC-1 #4 responded in the same manner. The variation of +/-2.5 W in alternator power occurs when connecting/disconnecting from the bus. This same variation was observed while operating with the DASCS. The reason for this power change has not been identified as of yet.

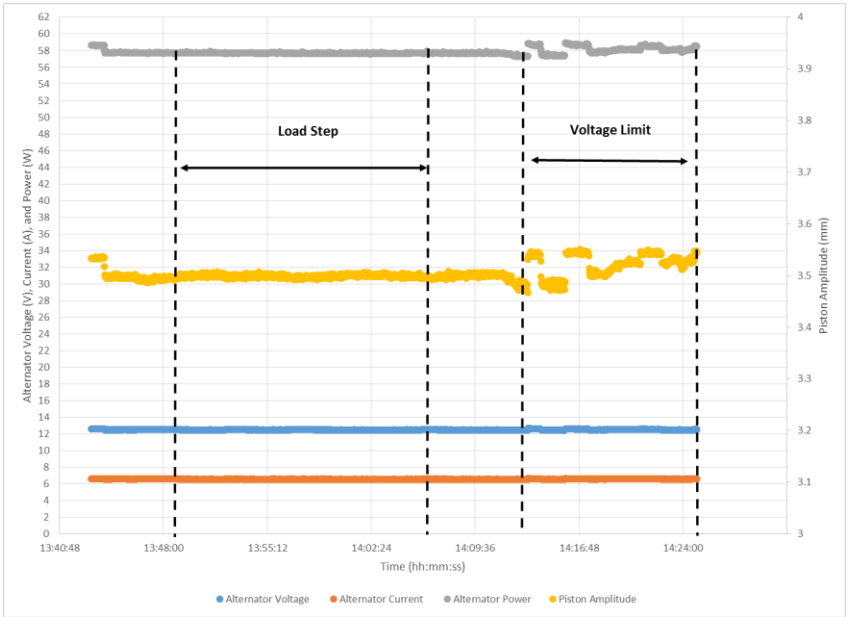

Figure 14. 120 W operation: ASC-1 #3 operating with DCC EM 2 & 3 for RSIL capacitor bus testing.

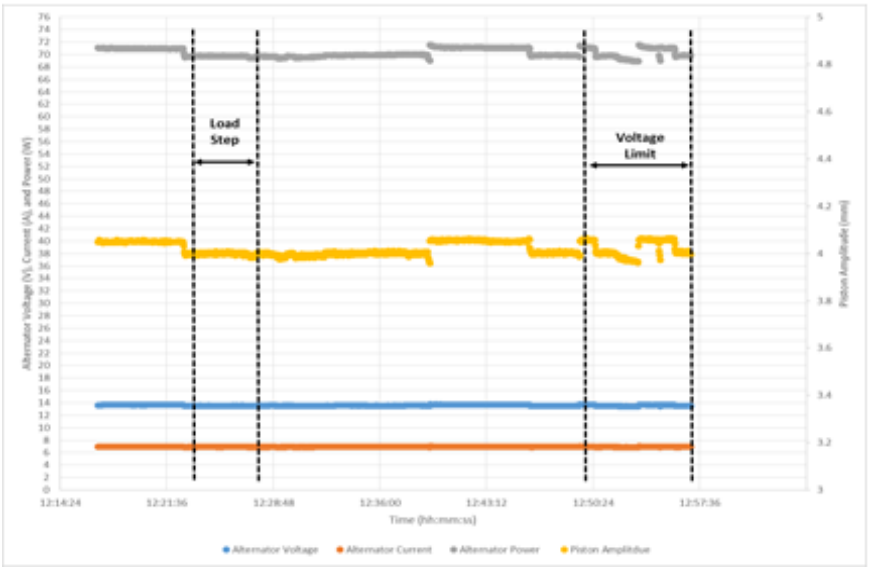

Figure 15. 138 W operation: ASC-1 #3 operating with DCC EM 2 & 3 for RSIL capacitor bus

B. Supercapacitor bus

Four tests were performed in the supercapacitor bus configuration at the 120 W convertor power output level: load step changes, load profile, voltage limit and short-circuit tests. Three tests were performed in the supercapacitor bus configuration at the 138 W convertor power output level: load step change, voltage limit, and short circuit. Table 6 lists the bus voltage and current levels for this test. Fig. 19 and 20 show the ASC-1 #3 alternator voltage, current and power and piston amplitude response during the supercapacitor tests.

For both power levels, a positive 2 A step load change, seen in Fig. 16, was initiated and all systems operated as expected. The load was then removed, as shown in Fig. 17, with no disturbances observed at the source.

Table 6. Bus voltage and current for supercapacitor testing.

Power Level (W)	Bus Voltage (V)	Bus Current (A)	RSIL Power (W)
120	28.06	3.53	99
138	28.88	3.9	113

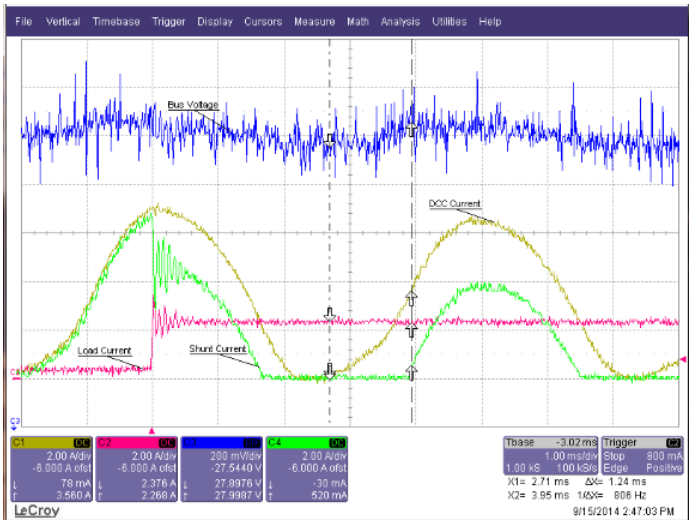

Figure 16. 120 W: 2A load step change with supercapacitor.

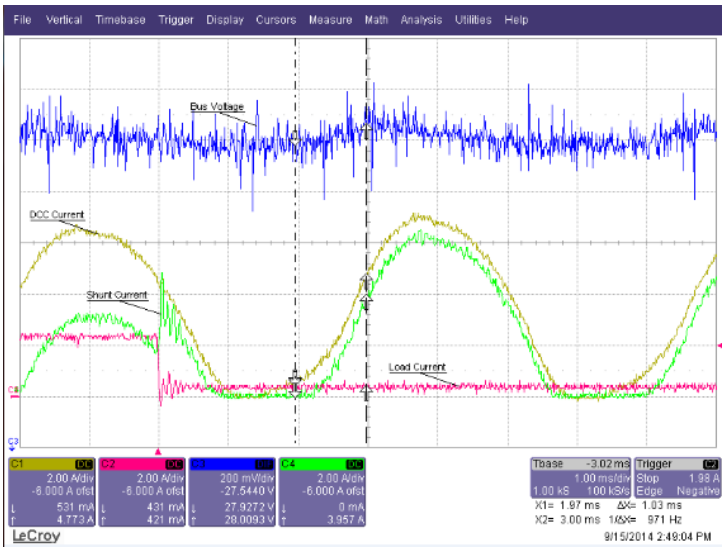

Figure 17. 120 W: 2A load removal with supercapacitor.

A load profile, shown in Fig. 11, test was performed at the 120 W convertor power output level. The RPS and RSIL operated in the manner expected with the DCC maintaining control of the ASCs and RSIL providing power via energy storage and dissipating power via the shunt regulator.

As described in the capacitor bus section III.A, the voltage limit tests were performed. The DCC successfully disconnected when out of range of the 22-36 V bus voltage for which the unit was designed. Table 7 lists the voltage at which the DCC disconnected from the bus.

Table 7. Bus voltage at disconnect for supercapacitor bus testing.

Convertor Power Output (W)	Low Voltage Disconnect (V)	High Voltage Disconnect (V)
120	21	36.09
138	21.6	36.62

For the 120 W power level short circuit test, one load channel was set to 2 A and then shorted with a trip time of 85.2 us. The results of this test are shown in Fig. 18. For the 138 W power level short circuit test, one load channel was set to 3 A and then shorted. For both power levels, no disturbances or abnormalities were seen at the source and all systems operated as expected.

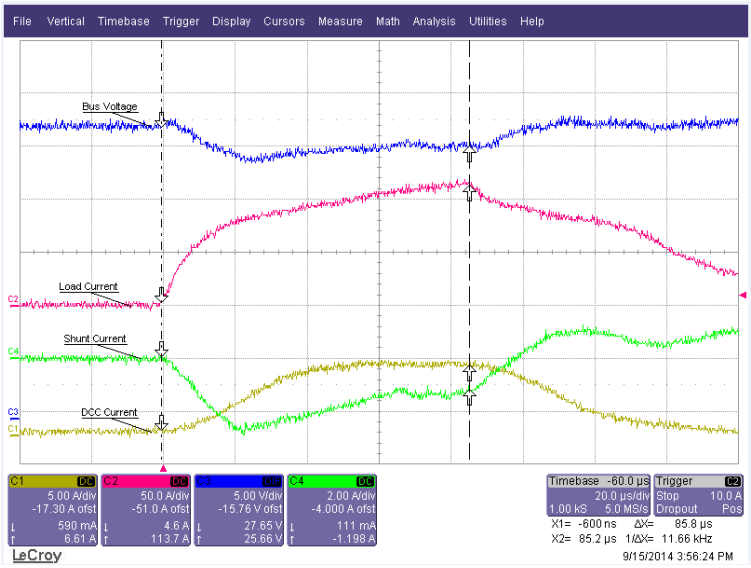

Figure 18. 120 W: shorted load test with supercapacitor.

Vm is a command that is sent to the DCC to control the piston amplitude of the ASC. Vm had to be adjusted for both the 120 and 138 W operation in order to connect to the bus. The reason for this has not be identified as of yet.

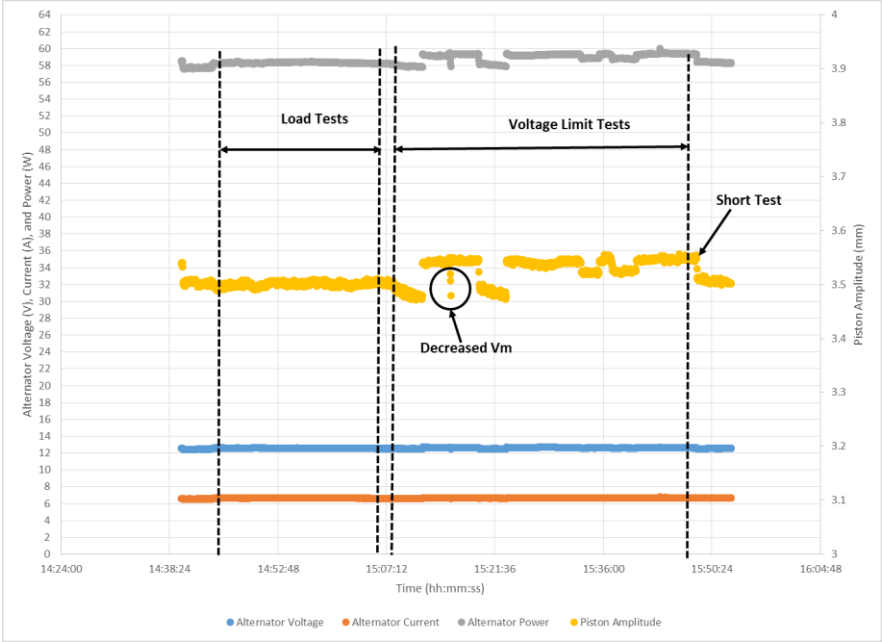

Figure 19. 120 W: ASC-1 #3 operating with the DCC EM 2 & 3 supercapacitor

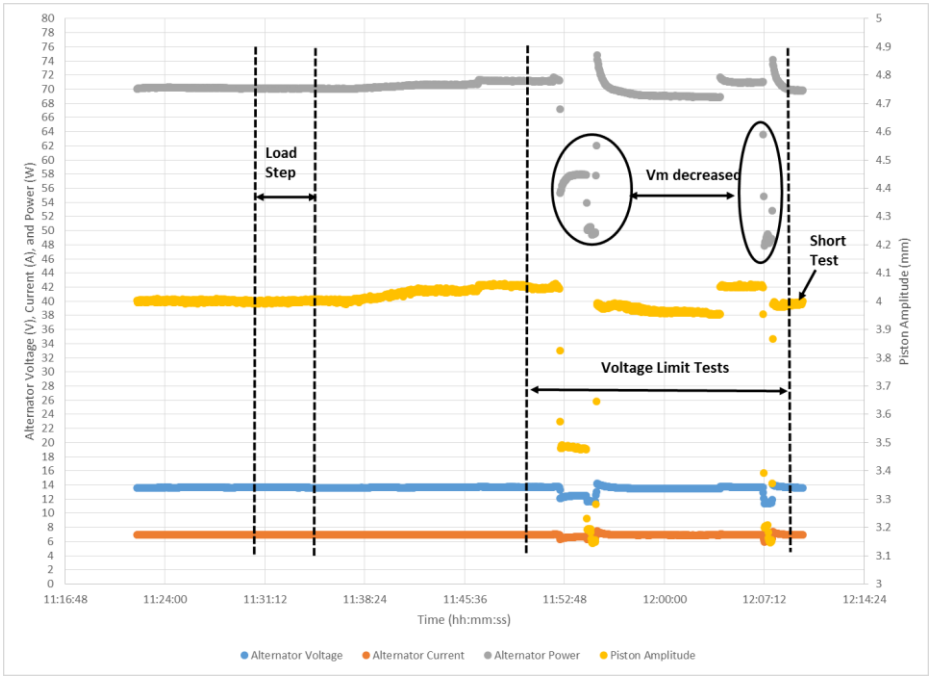

Figure 20. 138 W: ASC-1 #3 operating with the DCC EM 2 & 3 supercapacitor testing.

C. Battery bus

Two tests were performed in the battery bus configuration at the 120 W convertor power output level: load step change and short-circuit. Three tests were performed in the battery bus configuration at the 138 W convertor power

output level: load step change, load profile, and short circuit. Fig. 25 and 26 show the ASC-1 #3 alternator voltage, current and power and piston amplitude response during the supercapacitor tests.

For the 120 W power level, a positive 2 A step load change, seen in Fig. 21, was initiated. The load was then removed, as shown in Fig. 22. For the 138 W power level, a step change of 4 A was initiated by providing 2 A loads on each of two load channels. No disturbances observed at the source for either of the load tests.

Table 8. Bus voltage and current for battery bus testing.

Power Level (W)	Bus Voltage (V)	Bus Current (A)	RSIL Power (W)
120	31.2	3.24	101.1
138	31.24	3.61	113

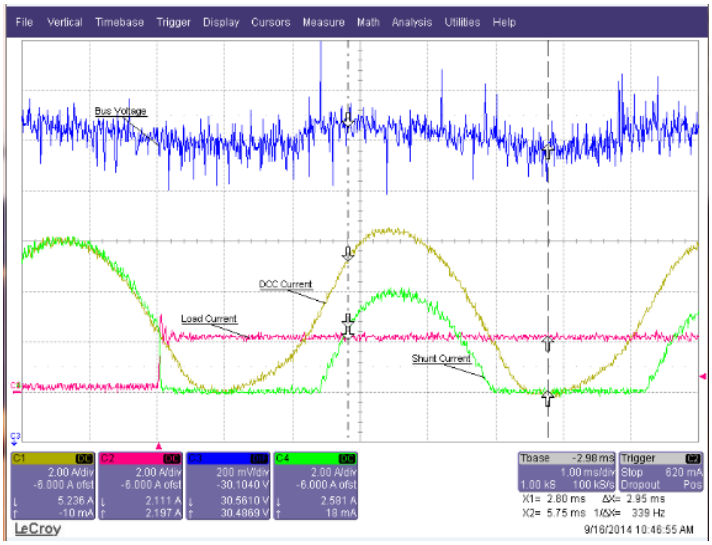

Figure 21. 120 W: 2A load step change with battery bus.

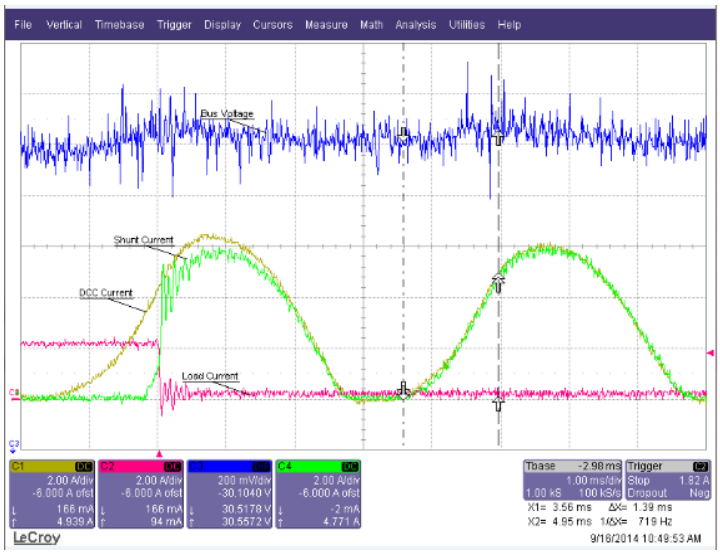

Figure 22. 120 W: 2A load removal with battery bus.

For the 120 W power level short circuit test, one load channel was set to 2 A and then shorted. The results of this test are shown in Fig. 23. For the 138 W power level short circuit test, one load channel was set to 3 A and then shorted with a trip time of 85.4 us. For both power levels, no disturbances or abnormalities were seen at the source and all systems operated as expected.

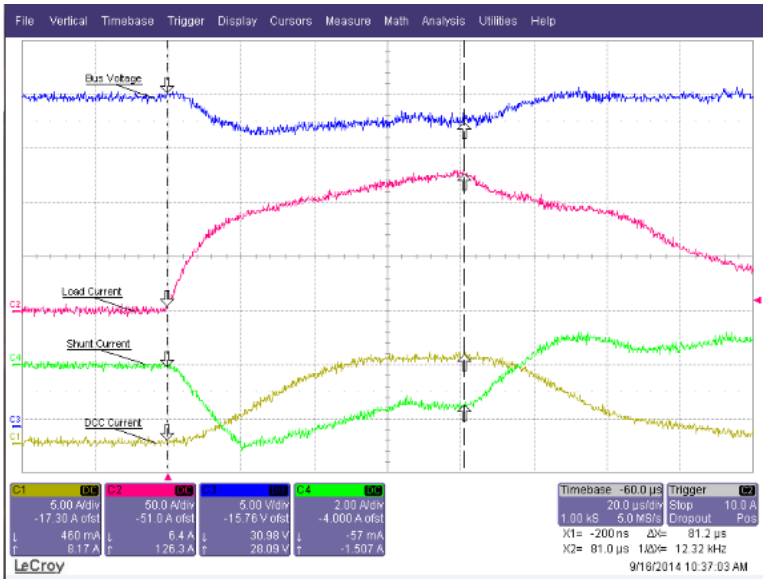

Figure 23. Shorted load test with battery unit.

A load profile, shown in Fig. 24, test was performed at the 138 W convertor power output level. The RPS and RSIL operated in the manner expected with the DCC maintaining control of the ASCs and RSIL providing power via energy storage and dissipating power via the shunt regulator.

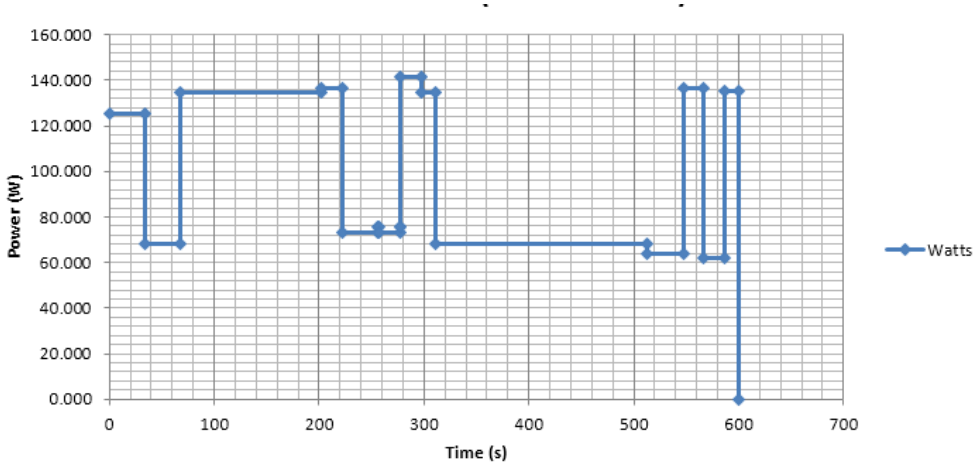

Figure 24. 141 W maximum load profile.

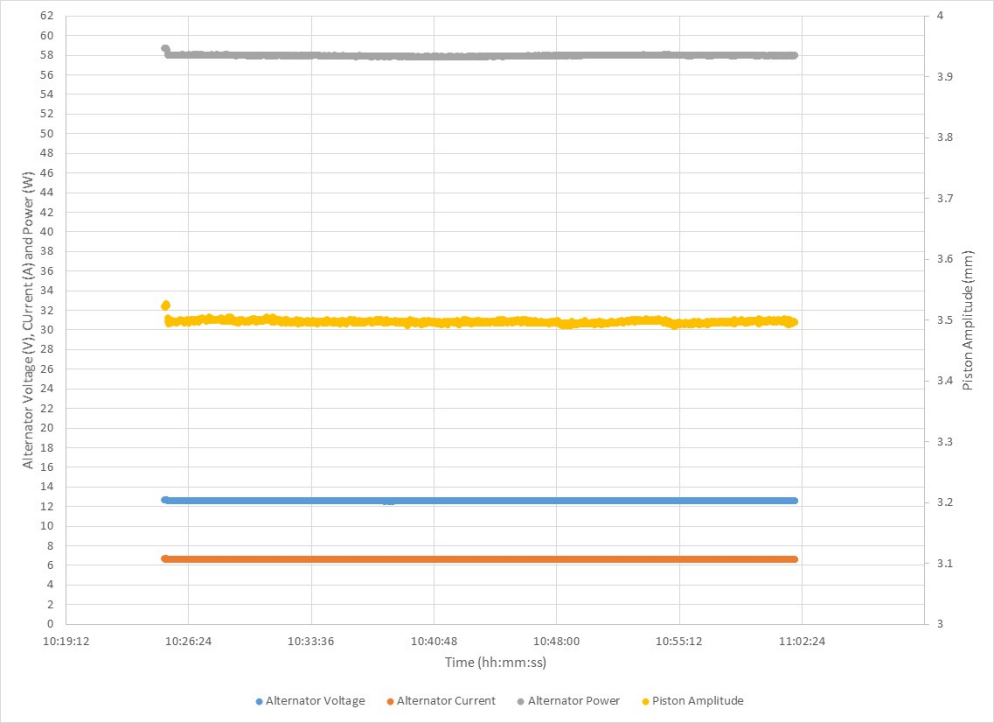

Figure 25. 120 W: ASC-1 #3 operating with DCC EM 2 & 3 for RSIL battery bus testing.

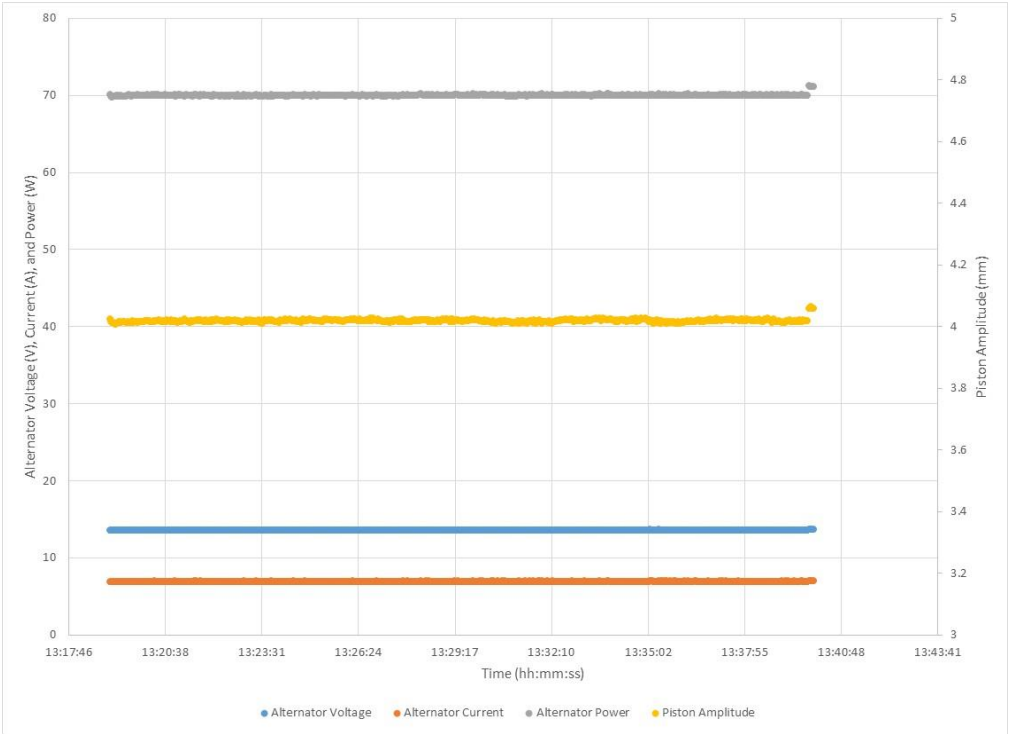

Figure 26. 138 W: ASC-1 #3 operating with DCC EM 2 & 3 for RSIL battery bus Testing.

V. Dual Input Channel Testing

As a follow-on to previous single input channel Stirling generator testing in RSIL, a test was performed using a flight-like hardware simulation of two RPS's connected to a spacecraft. In order to demonstrate two channel operation, the DCC was configured to utilize both of its two controller cards simultaneously. Fig. 27 describes the RPS setup for this test. The primary objectives were to verify stable operation of each DCC card with its DASCS's and to verify two input channel functionality of the RSIL with parallel RPS inputs.

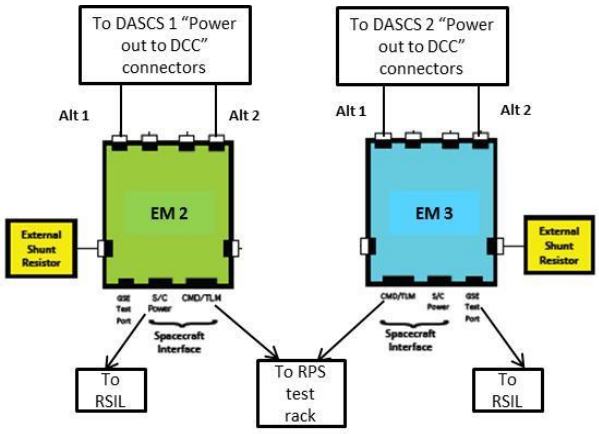

Figure 27. Dual input channel RPS test setup.

Dual input channel testing included operations using capacitive, battery, and supercapacitor bus configurations. Table 9 below describes summarizes the dual input channel DCC testing that was performed in RSIL. The results presented in this section are at a convertor power output level of 100 W per DASCS. Table 10 lists the DASCSs and RSIL power levels. This testing could not be performed at a higher DASCS convertor power output due to limitations of the SRU. Table 10 lists the power level on each RSIL input channel. As with the single input channel testing, four main tests were completed which included load step change, load profile, voltage limit, and short circuit.

Table 9. Summary of dual input channel testing.

Capacitor Bus	Voltage Limit
	Short Circuit
Supercapacitor Bus	Load Step Change
	Voltage Limit
	Short Circuit
Battery Bus	Load Profile

Table 10. Summary of DASCS and RSIL power.

DCC Card #	DASCS #	RSIL Input Channel	DASCS Power (W)	RSIL Power (W)
2	1	1	101	78
3	2	2	100	71

A. Capacitor bus

Two tests were performed in the RSIL bus capacitor configuration: voltage limit and short circuit. Table 11 lists the bus voltage and current on each RSIL input channel during these tests. Since this was the first operation with two RSIL input channels, this test was completed at a lower power level than the superacapactior and battery tests. The initial dual input test utilized the bus capacitor to determine under voltage trips for each DCC card.

For the voltage limit tests, the bus voltage on each RSIL input channel was raised above 36 V and then lowered below 22 V to verify each DCC's ability to disconnect from the bus when out of range from its designed bus voltage range. Table 12 shows the voltage at which each DCC disconnected.

For the short circuit test, one load channel was set to 2 A and then shorted. The trip was realized in 85.6 us and the short did not impact RPS or RSIL operation.

Table 11. RSIL bus voltage and current for dual input channel capacitor bus testing.

Input Channel	Voltage (V)	Current (A)	RSIL Power (W)
1	28.53	1.53	43.7
2	28.53	1.46	41.7

Table 12. Voltage at DCC disconnect for dual input channel capacitor bus testing.

Test	Input Channel 1 (V)	Input Channel 2 (V)
Low Voltage	20.77	21.15
High voltage	36.37	33.8

B. Supercapacitor bus

Three tests were performed in the RSIL supercapacitor configuration: load step change, voltage limit and short circuit. Table 13 lists the bus voltage and current on each RSIL channel for these tests. Three load channels were each programmed for 2 A. The loads were connected concurrently, thus realizing a step from no load 0 to 6 A. No disturbances were seen in RSIL or RPS. Table 14 shows the results of the voltage limit test.

Table 13. RSIL bus voltage and current for dual input channel supercapacitor bus testing.

Input Channel	Voltage (V)	Current (A)	RSIL Power (W)
1	28.6	2.87	82.1
2	28.6	2.71	77.5

Table 14. Voltage at DCC disconnect for supercapacitor bus testing.

Test	Input Channel 1 (V)	Input Channel 2 (V)
Low Voltage	20.76	21.1
High voltage	36.26	34.2

For the short circuit test, two of the load channels was set to 2 A for a total load of 4A. A short was imitated on channel 1 and the trip was realized in 83 us. This did not impact RPS or RSIL operation.

C. Battery bus

The battery unit was connected as the energy storage for the system with a bus commanded to 30.57 V. The load profile shown in Fig. 28 was run to determine whether there were any negative interactions between the two RPSs during load changes. All systems operated within specifications with no disturbances seen by RSIL or the RPSs.

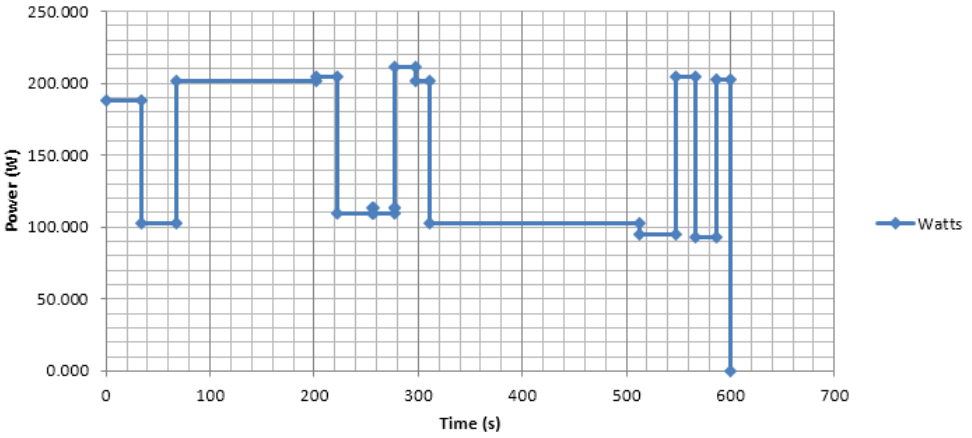

Figure 28. Dual input channel load profile (212 W max).

VI. Conclusion

The results of the tests showed not only the viability of the RPS convertors to act as a source for future planetary exploration missions, but also demonstrate the ability of the RSIL to provide overall electrical power system testing and analysis. The short-circuit, overvoltage, under voltage and load step transients provided by RSIL were effectively managed by the ASCs and associated DCC controller both during single and dual input channel testing. This testing paves the way for future RSIL validation and verification of the next generation of RPS technology.

Acknowledgments

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