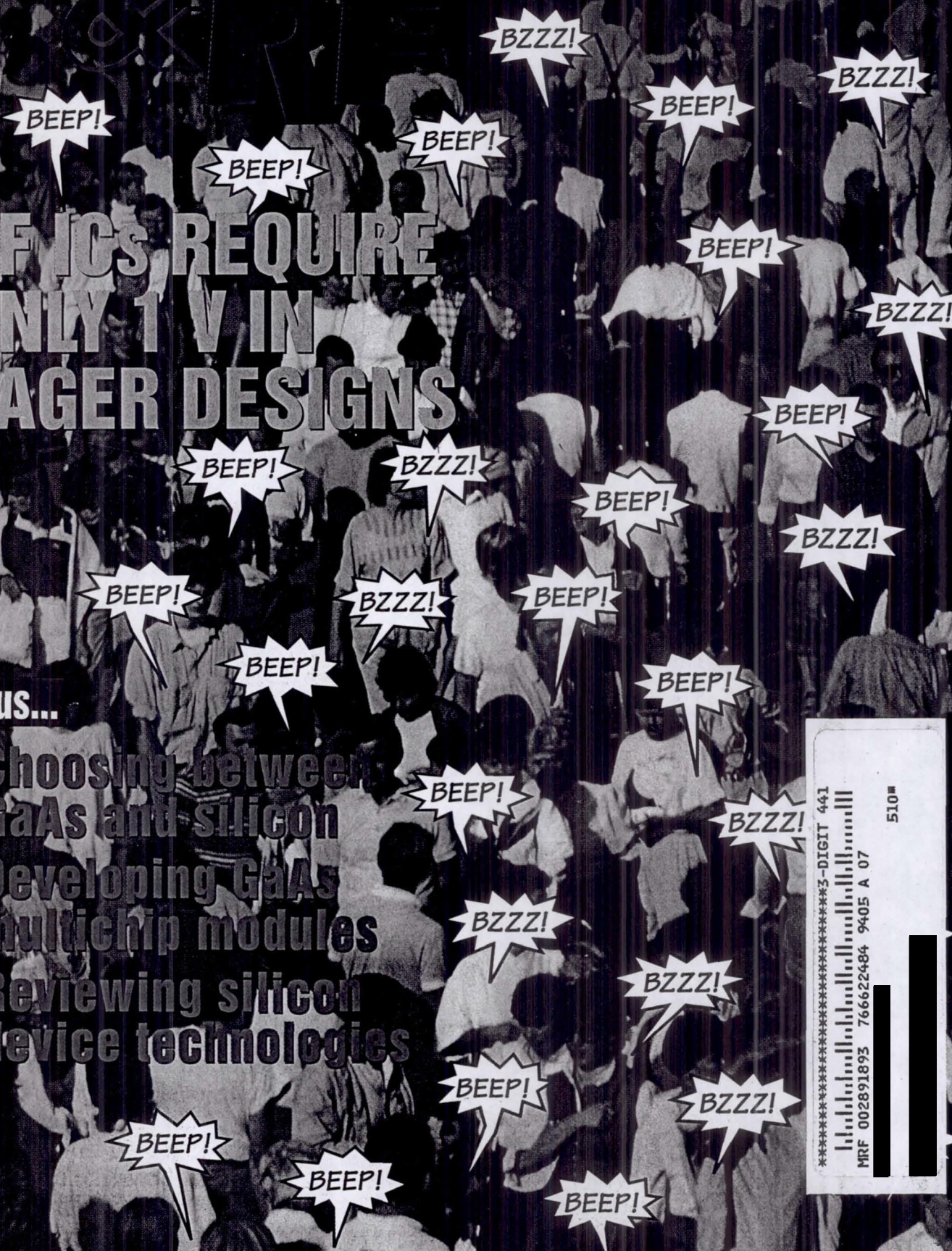


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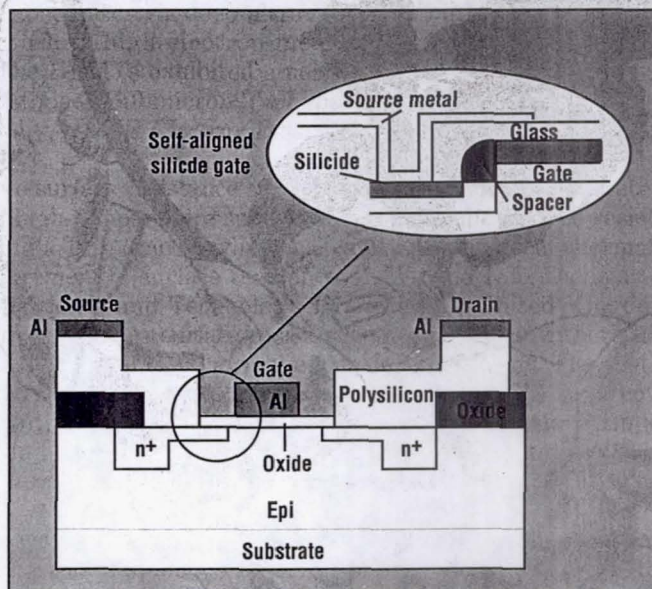
SILICON TECHNOLOGIES ADJUST TO RF APPLICATIONS

Improvements in silicon materials and processing techniques promise higher-frequency performance.

SILICON (Si), although not traditionally the material of choice for RF and microwave applications, has become a serious challenger to other semiconductor technologies for high-frequency applications. Fine-line electron-beam and photolithographic techniques are now capable of fabricating silicon gate sizes as small as $0.1 \mu\text{m}$ while commonly-available high-resistivity silicon wafers support low-loss microwave transmission lines. These advances, coupled with the recent development of silicon-germanium (SiGe), arm silicon integrated circuits (ICs) with the speed required for increasingly higher-frequency applications.

Silicon devices dominate the present-day electronics industry. The material is well characterized (see table) and is available in high-quality wafers.^{1,2} Properties include good

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1. This high-frequency silicon MOSFET uses self-aligned silicide gates.

mechanical strength and thermal conductivity with a reasonable band-gap. High-quality oxides are easily formed on silicon, allowing for the fabrication of field-effect transistors (FETs)—the basis for CMOS technology. High-quality, low-cost silicon wafers are readily available in diameters as large as 8 in.

In spite of its benefits, silicon has several features which limit its high-frequency use. The resistivity of low-cost commercial wafers is orders of magnitude below the intrinsic resistivity, usually on the order of $10 \Omega\text{-cm}$. This low resistance causes exceedingly-high dielectric losses in microwave transmission lines, making it almost impossible to transmit

microwave signals on silicon. Since device speed is dictated by the electron mobility and carrier velocity, silicon is a fundamentally slower material than germanium (Ge) or gallium arsenide (GaAs), both of which have higher electron mobilities than silicon. Germanium also has higher hole mobility and electron velocity than silicon, but because of its extremely-low intrinsic resistivity, it is not appropriate for high-frequency applications. This leaves GaAs as silicon's chief competitor for high-speed applications.

GaAs has its own disadvantages, however. Its low hole mobility severely limits its ability to support complementary circuitry. Also, high-

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quality oxides cannot be formed on GaAs, a shortcoming which has been partially circumvented by the use of modulation-doped FET (MODFET) structures.

The characteristics of an ideal microwave substrate were itemized as far back as 1969.³

- high dielectric constant
- low dissipation factor or loss tangent
- dielectric constant should remain constant over the frequency and temperature ranges of interest
- high purity and constant thickness
- high thermal conductivity

Silicon fulfills most of these requirements. It has a dielectric constant of 11.7, thermal conductivity of 1.5 W/cm K (compared to 0.46 W/cm K for GaAs), well-controlled purity and thickness, and its dielectric constant is fairly stable with frequency. Silicon has a high loss tangent, however. The resistivity of standard sili-

con is extremely low, on the order of 10 Ω -cm. Transmission lines fabricated on standard silicon suffer from very high dielectric losses.

Still, silicon-based substrates have moved to microwave frequencies. High-resistivity silicon (HRS), silicon-on-insulator (SOI) materials, and highly-doped silicon wafers have all been used to fabricate silicon-based microwave circuits.

HRS SUBSTRATES

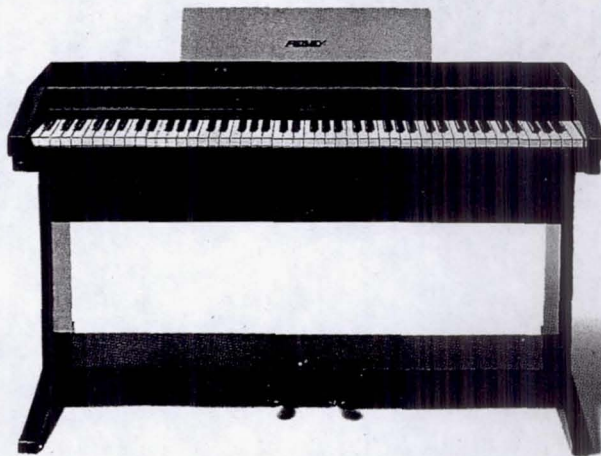
HRS has existed for decades, but with limited availability. The material was of little interest because it was believed that high device-processing temperatures would destroy the material's insulating properties.⁴ Today, HRS substrates are readily available with resistivities in excess of 10,000 Ω -cm and have been shown to withstand significant processing temperatures.⁵

Transmission lines on HRS substrates were demonstrated as early

as 1965.⁶ Microstrip lines on HRS materials with a resistivity of 1500 Ω -cm achieved measured losses of 0.5 dB/cm for temperatures between +5 to +110°C. In 1982, researchers at RCA Laboratories (Princeton, NJ) theorized that if microstrip lines were fabricated on HRS wafers with resistivities of 2000 Ω -cm or greater for applications at frequencies beyond 30 GHz, the losses would rival those of microstrip lines on GaAs.⁷ But it was not until 1993 that this theory was confirmed experimentally by a group at the NASA Lewis Research Center (Cleveland, OH).

These researchers showed that coplanar-waveguide (CPW) transmission lines on HRS substrates with resistivities of 2500 Ω -cm or greater had losses from 5 to 40 GHz that were only slightly higher than those on GaAs. In fact, CPW lines fabricated on HRS substrates with resistivities in excess of 30,000 Ω -cm actually had lower losses than those on

GaAs, temperature loss on HF HR to fabricate antennas have lithic circuits SOI between the oxide between preparation of technology



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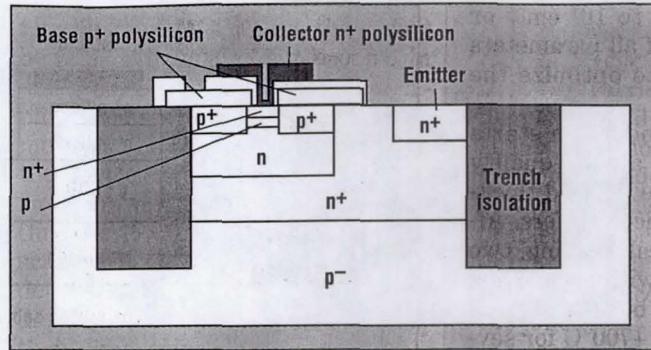
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GaAs, both at cryogenic and room temperatures.^{8,9} The same group at NASA has also demonstrated low-loss slot line and coplanar striplines on HRS substrates.¹⁰

HRS substrates have been used to fabricate a linearly-tapered slot antenna with a CPW feed.¹¹ The antenna achieves 7-dB gain at a center frequency of 7 GHz. HRS substrates have also been used in silicon monolithic millimeter-wave integrated circuits (SiMMWICs) for transmitters operating to 73 GHz.¹²

SOI technology enhances isolation between devices on the same wafer with an oxide layer placed just below the surface of the substrate. The oxide layer blocks current flow between devices, thus improving isolation. SOI wafers are commonly prepared via separation-by-implantation-of-oxygen (SiMOX) and bonded-and-etched-back-SOI (BESOI) processes. SiMOX is the leading technology,¹³ but improvements in



2. This high-frequency silicon bipolar employs a polysilicon base and emitter structure.

BESOI are making this latter approach more competitive. Both techniques can yield high-quality wafers of any size with thin, homogeneous silicon layers of easily-controlled thickness.

To fabricate regular SiMOX wafers, silicon wafers are implanted with oxygen ions (O^+ in doses as high as 10^{18} cm^{-2} and at energies as high as 200 keV. The wafers are held at temperatures that approach $+600^\circ\text{C}$. This procedure creates an amor-

phous oxide layer under a damaged silicon top layer. A subsequent anneal at $+1320$ to $+1350^\circ\text{C}$ for 2 to 6 hours in argon (with roughly 1 percent oxygen) recrystallizes the top silicon layer and makes an abrupt Si-SiO₂ interface. The silicon layer above the oxide is of the order of several thousand Angstroms thick and has 2-percent thickness homogeneity. The silicon can then be etched to the desired thickness. Additional interim steps can reduce the silicon



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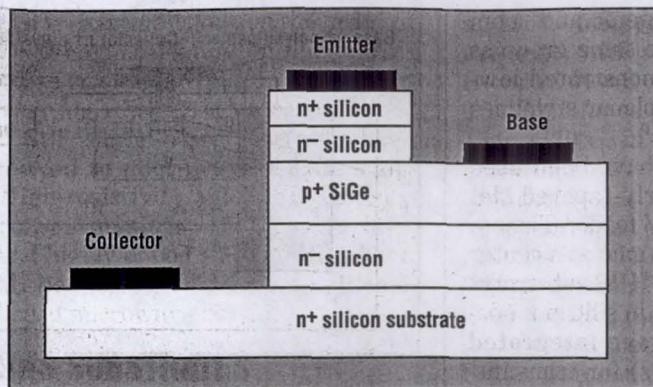


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dislocation density to 10^4 cm^{-2} or lower. A variation of all parameters can be performed to optimize the material quality.¹⁴

BESOI wafer production starts with the growth of a good-quality thermal oxide to the desired thickness on standard silicon wafers. After thorough chemical cleaning, two wafers are bonded with their oxide layers together. The bonded wafer is then heated to over $+700^\circ\text{C}$ for several hours to improve the strength of the bond. One wafer is then etched back and mechanically polished, in several steps, to achieve the required top silicon wafer thickness. Etch "stops" are used in order to ensure uniformity.

The most recent etch-stop technology employs the use of epitaxially-grown etch stops like SiGe,¹⁵ which allows very careful control of the silicon layer homogeneity. For example, when a $1000\text{-}\text{\AA}$ SiGe etch-stop layer was used, the silicon thickness



3. This simplified cross-sectional diagram shows the components of a SiGe/Si heterojunction bipolar transistor (HBT).

was accurate to 70 \AA . The dislocations in the material were below 10^5 , making these wafers very competitive with SiMOX wafers. Other SOI techniques include silicon on glass, silicon on sapphire (SOS), dielectric isolation (DI), and silicon on diamond (SOD).

For lower-frequency applications such as mobile commercial communications, highly-doped conductive silicon is commonly used. As in the case

of SOI, the highly-doped substrate acts as a ground plane just under the active region. Motorola uses this approach for their silicon MOS circuits.¹⁶ Via holes are fabricated using p^+ sinkers that ground the source to the substrate. But unlike SOI technology, this approach can lead to serious leakage problems and, of course, cannot support microwave frequencies.

Recent advances in both materials



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and fabrication techniques are pushing the frequency limit of silicon devices far beyond what was originally thought possible. Because of new techniques in photolithography and x-ray lithography, gate lengths as small as $0.1 \mu\text{m}$ are now possible with silicon. For instance, eximer laser lithography, an extension of optical lithography, is being used for applications below $0.25 \mu\text{m}$.¹⁷ The process is better suited for production than electron-beam or x-ray techniques.

MOSFET STRUCTURES

Traditional MOSFET and bipolar structures are being pushed to higher frequencies by novel scaling techniques. But perhaps the most significant development in high-frequency silicon devices is SiGe. This material enables, for the first time, bandgap engineering and strained layer structures in a silicon-based system.

In order to increase the operating

frequency of MOSFETs, they must be scaled to smaller dimensions. In doing so, the parasitic junction capacitances and series resistance must also be reduced. In addition, if the devices are to be part of an IC, isolation must be preserved. The three basic variables involved in this scaling-down process are junction depth, oxide thickness, and depletion depth, with tradeoffs in choosing their dimensions.

As device dimensions shrink, drain and source junctions must also become smaller. With this reduction in size, however, comes an increase in the series resistance, a decrease in the breakdown voltage, and an increase in the generation of hot carriers. In addition, the shallow channels that result are particularly susceptible to damage during subsequent processing, which can lead to leakage in the device. Therefore, only the portion of the junctions close to the channel are made shallow.

This, however, does not solve the biggest problem; hot-carrier generation. Hot carriers are caused by the increased field concentration in the shallow junction. These carriers can greatly degrade device performance by increasing leakage currents. The problem can be minimized by lightly doping the drain junction, which helps to reduce the electric field at the junction.

Nonetheless, this does not help to reduce the high series resistance of the shallow junctions. One technique used to solve this problem is the self-aligned silicide (salicide) process. When scaling down a MOSFET, the gate oxide becomes thinner (within limits). When an oxide becomes thinner than 40 \AA , carriers begin to tunnel through the oxide, ultimately leading to device failure. Additionally, as the oxide gets thinner, the capacitance between the metal and the substrate increases. This capacitance can be reduced by placing poly-



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silicon between the metal and the contact (Fig. 1). This not only helps to decrease capacitance, but also adds a layer which protects the device against metal spikes during processing.

Depletion regions in MOSFET structures are a result of the drain and source junctions. The width of the depletion region must scale down with the other MOSFET dimensions, particularly in the channel region, to avoid drain-to-source punch-through. This can be achieved by heavily doping the channel, but this can lower the breakdown voltage and increase the threshold voltage. Heavy doping also increases the junction-to-substrate capacitance. An alternative is to lightly dope the area outside the channel to minimize this capacitance. This technique was applied by Bell Laboratories, which developed silicon N- and P-type MOSFETs with f_T 's of 116 and 51 GHz, respectively.¹⁸ These devices

feature 0.1- μm polysilicon gates fabricated with electron-beam lithography.

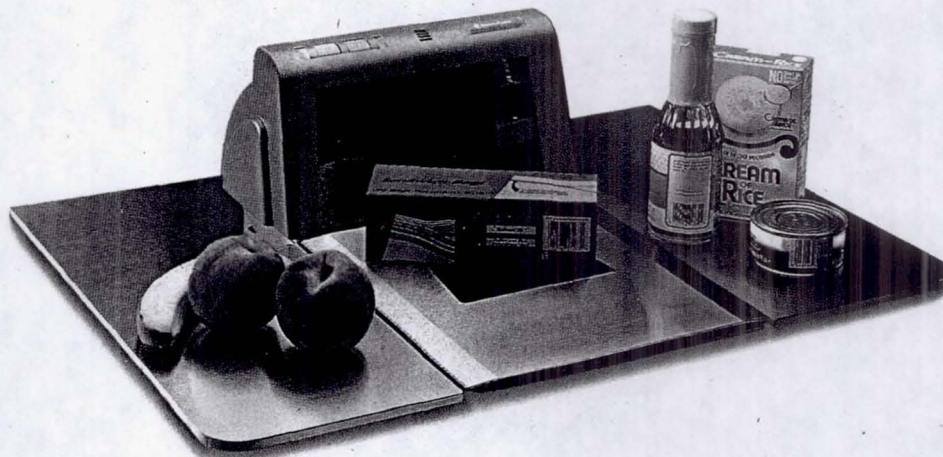
To minimize subthreshold leakage in these devices, vertical doping technology was employed to put a highly-doped region under the channel only. The drain fields terminate on this region instead of on the source, which reduces both leakage and junction-to-substrate capacitances. Since the channel itself is not doped, there is no shift in threshold voltage using this process, which is VLSI-compatible.

Substrates used for high-frequency MOSFETs must either be highly conductive or fairly insulating. Standard silicon acts as a lossy resistor, degrading device performance. As a result, silicon used for high-frequency applications has traditionally been very highly doped. By making the substrate conductive, the entire substrate in essence becomes the ground plane. Unfortunately, this

approach is inherently leaky, with a limited level of integration. Junction and trench isolation techniques have been used to try to limit leakage.

Leakage is the prime motivator for using SOI technologies. SOI adds a layer of oxide just below the active device. Devices can be isolated on all three sides by etching trenches between the devices and back-filling them with polysilicon. Although SOI helps to control leakage, it does not alleviate the loss problem.

SOS technologies, on the other hand, do cut losses. They provide the isolation of SOI and a low-loss substrate for microwave components. Using SOI, both 0.5- μm NMOS and PMOS devices have been demonstrated with f_T 's of 22 and 21 GHz, respectively, and f_{max} 's of 11 and 7 GHz, respectively.¹⁹ Using a T-gate structure, f_T 's greater than 20 GHz and f_{max} 's of 37 and 53 GHz, respectively, were achieved for PMOS-FETs and NMOSFETs.²⁰

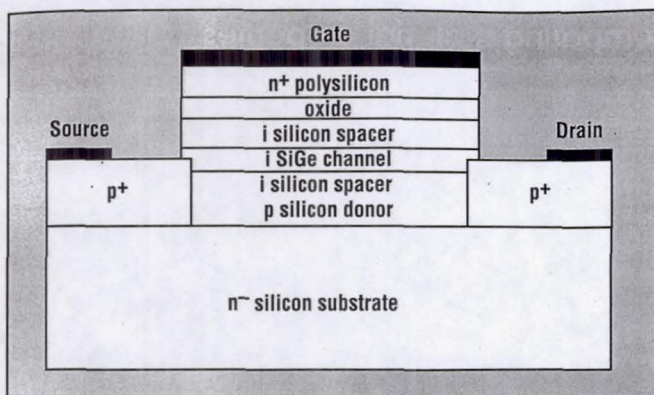


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4. A SiGe/Si PMOSFET device contains several spacer layers.

Unfortunately, SOS is relatively expensive. Its main disadvantage is its anisotropic nature: the dielectric constant changes with the direction of the crystal, varying from 9.3 to 11.5 and making circuit design extremely complicated. In addition, sapphire has a thermal conductivity even lower than that of GaAs (0.42 W/cm-K compared to 0.46 W/cm-K).

Perhaps one of the best ways to minimize leakage and substrate loss-

es is to use HRS substrates. It has been shown that the f_T and f_{max} of MOSFET devices actually increase when fabricated on a high-resistivity substrate.²¹ MICROX technology from Westinghouse combines SIMOX processes with HRS substrates. Substrates with resistivities greater than 10,000 Ω -cm are used and the resistivity can be maintained during processing.²²

Silicon bipolar devices reach high-

er frequency operation in the same way as silicon MOSFETs, via scaling. The scaling rules and relationships are different for bipolars, however. Bipolar devices have effects such as the Kirk effect (base push-out), base punchthrough, and current crowding, in addition to parasitic elements. In a bipolar, the parasitic elements that affect performance the most are the base resistance (R_b), the base-collector capacitance (C_{BC}), emitter resistance (R_E), and the collector-to-substrate capacitance.

For high-frequency bipolars, vertical structures are used since, in this dimension, the layer thicknesses can be easily controlled. Techniques such as polysilicon emitters, self-aligned emitter and base contacts, and trench isolation are commonly used in scaling these devices (Fig. 2).

The use of polysilicon in fabricating bipolars provides many advantages. This material cannot only



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withstand high processing temperatures, but can also be oxidized. Its most important use is in self-alignment of the emitter and base contacts. The polysilicon forms a sidewall spacer to permit the fabrication of devices with very small emitters. When used to form the emitter contact, polysilicon can greatly improve transistor gain. When scaling bipolar devices, the base doping must be increased as the base is made smaller to compensate for the increase in base resistance and to prevent punchthrough. However, because of this increased base doping and other factors, f_T drops. Polysilicon emitters help to compensate for this. Also, polysilicon in the emitter can be extended beyond the contact region to lower the contact resistance.

An example of a high-frequency bipolar is Hitachi's 64-GHz device.²³ It is fabricated with U-groove trench isolation using an in-situ phosphorous-doped polysilicon (IDP) technique to form the ultra-shallow emitter. Low-temperature processing and large-grain-size polysilicon are used to avoid increasing emitter resistance and redistributing the base profile. Hitachi has also fabricated complementary bipolar transistors on the same chip using their SPO-TEC process. The process yields NPN and PNP transistors with cutoff frequencies of 30 and 32 GHz, respectively.²⁴ The fact that the f_T 's of both devices are almost identical helps to avoid high-frequency distortion. In addition to excellent discrete-device performance, bipolar

Comparing material properties			
Property	Silicon	Germanium	GaAs
Intrinsic resistivity ($\Omega\text{-cm}$)	2.3×10^5	47	10^8
Thermal conductivity (W/cm K)	1.5	0.6	0.46
Bandgap at 300 K (eV)	1.12	0.66	1.42
Electron mobility ($\text{cm}^2/\text{V s}$)	1500	3900	8500
Hole mobility ($\text{cm}^2/\text{V s}$)	450	1900	400
Electron velocity at 0.1 μm (cm/s)	1.4×10^7	1.6×10^7	7×10^7
Electron velocity at 0.3 μm (cm/s)	1.2×10^7	1.4×10^7	8.2×10^7
Field for max. overshoot (kV/cm)	40	10	30
Maximum wafer diameter (in.)	12	—	4

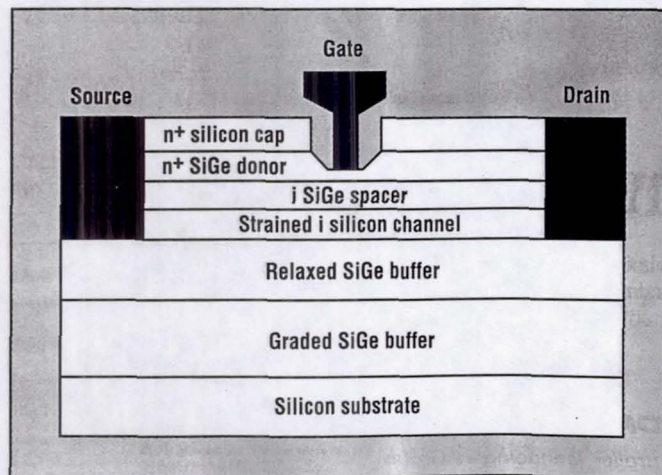
devices have formed the basis for silicon MMICs. Another firm, NEC, has demonstrated a divide-by-16 prescaler that operates in the 12-to-28-GHz range. The circuit incorporates silicon bipolar transistors with 40-GHz cutoff frequency.²⁵

High-frequency BiCMOS technology, which integrated both bipolar transistors and CMOS devices, has the potential to support ICs with both RF and digital functions. IBM has demonstrated a 60-GHz double-polysilicon self-aligned bipolar device integrated with 0.25- μm CMOS. Integration is achieved without degradation of either type of device.²⁶

Active electron devices containing

one or more SiGe layers have shown significantly better performance than their pure silicon counterparts, due to the improved material properties of these structures. Silicon and germanium have a lattice mismatch of 4.2 percent at room temperature. The lattice constant of $\text{Si}_{1-x}\text{Ge}_x$ grows linearly with the germanium concentration, denoted by x in the chemical formula. The $\text{Si}_{1-x}\text{Ge}_x$ starts growing on silicon, epitaxially growing defect-free and unconditionally stable until the critical thickness (h_c) is reached. This critical thickness can be very small. For example, when $x = 0.2$, h_c is only 80 Å. Above h_c , there is a range of thickness where the material is conditionally stable or metastable. Since materials with thicknesses below h_c are extremely difficult to fabricate, many materials are fabricated with metastable structures. This must be done with great care since, under certain conditions, the material will start to relax and develop defects.

Methods used for the epitaxial growth of SiGe include molecular-beam epitaxy (MBE), gas source MBE, and several types of chemical vapor deposition (CVD). The most notable CVD type is ultrahigh-vacuum (UHV) CVD.²⁷ UHV CVD was used to produce the first large-scale



5. A SiGe/Si modulation-doped FET (MODFET) device employs strained silicon on relaxed SiGe.

SILICON TECHNOLOGIES

SiGe application, a digital-to-analog converter (DAC) with 2854 NPN transistors.²⁸ The special equipment used for this process is now commercially available.²⁹ This process employs relatively low temperatures (up to +550°C) to grow the SiGe structure and can process multiple wafers with diameters as large as 8 in. Several large companies are currently involved with SiGe, including IBM (using UHV CVD), Daimler-Benz (using MBE), AT&T (using MBE and rapid thermal CVD), Hewlett-Packard Co. (using low-pressure CVD), NEC (using MBE), and Hitachi (using MBE).

In the fabrication of heterojunction-bipolar-transistor (HBT) devices, SiGe offers the ability to tailor the bandgap and strain effects. At the SiGe/Si interface, there is a step in the valence band equal to the bandgap difference (ΔE_g). This improves the emitter injection efficiency (h_{fe}) of HBT devices compared to bipolars, where ΔE_g is zero. Parameter h_{fe} is related to a change in bandgap as shown by the following relationship:

$$h_{fe} \propto e^{\Delta E_g / kT}$$

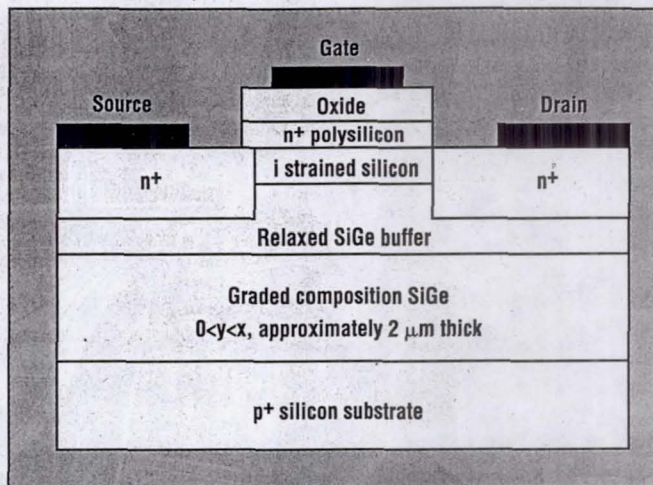
In a typical device material with $x = 0.2$, SiGe has approximately a 175-meV reduction in the bandgap. This results in a large improvement in h_{fe} . For a simple NPN SiGe/Si HBT (Fig. 3), the current gain, as limited by the injection efficiency, is improved by a factor of 1000 compared to an all-silicon bipolar. In addition to the improved injection efficiency, this result enables the device designer to increase doping and reduce the thickness of the base. With lower base resistance and thickness, f_T and f_{max} are markedly improved. The values of the Early voltage (V_a) and βV_a are also increased due to the increased doping concentration. An additional increase in the device speed can be achieved by grading the germanium concentration in the base.³⁰ This gives an accelerating field of 20 to 40 kV/cm.

The introduction of strain into the SiGe/Si material enhances the bandgap change and actually changes the mobility of the material. Relaxed SiGe and silicon have degenerate conduction and valence bands; strain lifts this degeneracy but results in non-constant mobility regarding the type of carrier, direction of conduction, and whether the carriers are

materials (Fig. 4). The hole mobility in the SiGe channel of SiGe/Si PMOS is enhanced versus that of standard silicon PMOS because these holes do not scatter at the Si/SiO₂ interface.³²

The top silicon spacer layer is necessary since there is no ideal oxide for SiGe. Proper design, including a germanium-graded channel to move the holes nearer to the top of the channel, and an n⁺ polysilicon gate allow for proper operation. So far, the actual performance of these devices has only been moderate. A 0.25- μ m-gate PMOS demonstrated a transconductance of 167 mS/mm versus 137 mS/mm for a silicon-only control device.³³ With optimization, the SiGe device could be improved.

Since there is no step in the conduction band in the SiGe/Si interface, electron-conduction FETs or NMOS HBTs can only be fabricated using strained silicon grown on relaxed SiGe. This creates a bandgap discontinuity in the conduction



6. A strained silicon NMOSFET device incorporates both a surface oxide and a strained silicon layer on relaxed SiGe.

majority or minority types. For most of these cases, theory predicts that the mobility will be enhanced. The result of these strain effects, as predicted through simulations of a high-frequency SiGe HBT with a linearly-graded base, is an increase of roughly 50 percent in f_T and 35 percent in f_{max} versus the case where strain was neglected.³¹

MOSFETs on SiGe/Si are desirable, but as of yet have not been fabricated as successfully as HBTs. SiGe technology offers FET enhancements that are much different than those possible with bipolars. In a MOSFET, the surface scattering due to the roughness of the silicon/oxide interface causes a large reduction in the mobility of the carriers. With SiGe technology, it is possible to fabricate quantum-well structures that essentially move the channel of the MOSFET below the surface of the device. For P-type devices, this is achieved using strained SiGe on silicon, since a step in the valence band is formed between the two ma-

band, which allows electron confinement in the thin strained silicon layer adjacent to the relaxed SiGe layers. Moreover, the degeneracy of the silicon conduction band is lifted, resulting in a significant increase in the mobility in the direction of the current flow within the device.³⁴ The NMOS channel is in the silicon as opposed to in the SiGe for the PMOS device. A basic MODFET includes N-doping in the top SiGe donor layer, an undoped SiGe spacer, and an undoped strained silicon channel (Fig. 5).

A mobility of 2830 cm²/Vs has been reported for an N-type MODFET.³⁴ This is an improvement by a factor of 2 versus intrinsic silicon and a factor of 5 over silicon inversion layers in MOS structures. Moreover, the electron velocity reached its saturation value at an applied field of only 25 kV/cm instead of the 50 kV/cm required in bulk silicon. This significant result means that a lower voltage bias can be used in these devices. Even with all its advantages, these

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structures have some drawbacks, however. The requirement of a relaxed SiGe "substrate" is rather demanding. A compositionally-graded buffer (2 to 3 μm or more thick) is used to achieve this. It turns out that these structures usually have large leakages. Several cap layers have been used to solve this problem. A

0.5- μm T-gate MODFET fabricated on this material demonstrated a transconductance of 390 mS/mm at room temperature.³⁵

NMOS devices were also fabricated,³⁶ using a slightly modified standard silicon MOS process (Fig. 6). The actual germanium concentration was 30 percent. The devices made on

strained silicon showed roughly an 80-percent improved effective mobility and transconductance in comparison to similarly made silicon control devices. This procedure can also yield P-type devices, but those fabricated so far have not been optimized and have not shown improvement over standard silicon devices.³⁷

All FET devices (MODFET, MOSFET, N-, and P-types) are still in the early stages of development and no meaningful high-frequency results have been reported. HBTs, however, have been optimized for high-frequency applications with good results. Either f_T or f_{max} for an HBT can be optimized, but to the detriment of the other parameter.³⁸ For example, $f_T = 113 \text{ GHz}$ ³⁹ and $f_T = 116 \text{ GHz}$ ⁴⁰ were reported for NPN HBTs. However, f_{max} of only 48 GHz was reported for the latter example. Still, a device having both a high f_T and f_{max} has been achieved: an NPN HBT structure from Daimler-Benz featuring an f_{max} of 65 GHz and f_T of 91 GHz.⁴¹

A study was performed to compare a SiGe HBT with a similarly processed silicon bipolar (containing a sub-500-Å base width). The SiGe device had an f_T of 113 GHz with βV_A of 48,400, improvements of 40 GHz and 47,770 over the bipolar. Since PNP SiGe HBTs are much harder to fabricate (as the germanium profile must be changed to accommodate the adverse band discontinuity), the best PNP HBT results so far are not as impressive as those for NPN HBTs. For PNP HBTs, some of the best devices have f_T of 55 GHz.⁴² Also, f_{max} of 38 GHz and f_T of 31 GHz have been demonstrated for a single device in an ECL circuit.⁴³ The ability to produce both NPN and PNP HBTs, albeit with different SiGe/Si profiles, opens up the possibility of fabricating complementary circuits with SiGe HBTs.

In addition to f_T and f_{max} , noise and the ability to integrate must be considered in a device process. Low noise figures have been obtained by a collaboration between Daimler-Benz and the University of Ulm (Ulm, Germany) for an NPN HBT. At a low collector current of 1 mA,

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SILICON TECHNOLOGIES

the device had noise figures of 0.9 and 0.5 dB, with associated gains of 6.5 and 12 dB at 10 and 2 GHz, respectively.⁴⁴ These devices had an f_T of 34 GHz and f_{max} of 25 GHz.

Integration of SiGe devices with digital circuitry has been shown in a DAC developed by the collaboration between IBM and Analog Devices (Norwood, MA). The circuit has a sampling rate of 1 GSamples/s, 12-b resolution, and contains 2854 NPN HBT transistors; it consumes just 1-W power. The collaborators claim that this power consumption is lower by a factor of 4 or 5 than any other semiconductor technology.⁴⁵

SiGe technologies, in particular HBTs, are well-suited for many applications, such as low-power, high-speed DACs and analog-to-digital converters (ADCs). In turn, these DACs and ADCs can be incorporated into a variety of systems, including communications networks, radars, medical imaging systems, and high-definition television (HDTV). Analog applications include low-noise and possibly high-efficiency amplifiers. In these cases, monolithic integration on high-resistivity silicon is the next logical step. Digital designers will find that the technologies are suitable for low-voltage digital ICs.

Since silicon is an indirect bandgap material, it has limited use for optical applications. Prognosticators note that optics in silicon will take at least twice as long to reach fruition as hybrid GaAs/AlGaAs and InGaAsP/InP.⁴⁶ Porous silicon has demonstrated photoluminescence,⁴⁷ but devices made from these materials are still in the beginning research stage.

With the development of SiGe materials, the possibility of silicon light emitters has greatly increased. In this material, the bands can be modulated by proper growth of SiGe on silicon. The processing, however, is not trivial and the light-emitting yield is extremely low. Modulation of the bands has been demonstrated by the use of multiple quantum-well (MQW) structures.^{48,49}

Even with increased-speed silicon devices, eventually silicon will reach its frequency limit and an inherently

faster material, such as GaAs, must take over for very high frequencies. It is not a matter of whether silicon will dominate microwave applications, but where it is that silicon will no longer be a practical choice. With the addition of SiGe devices, that boundary will apparently continue to move higher. ●●

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