

## Evidence of Processing Non-Idealities in 4H-SiC Integrated Circuits Fabricated With Two Levels of Metal Interconnect

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**Abstract.** The fabrication and prolonged 500 °C electrical testing of 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) with two levels of metal interconnect is reported in another submission to this conference proceedings. While some circuits functioned more than 1000 hours at 500 °C, the majority of packaged ICs from this wafer electrically failed after less than 200 hours of operation in the same test conditions. This work examines the root physical degradation and failure mechanisms believed responsible for observed large discrepancies in 500 °C operating time. Evidence is presented for four distinct issues that significantly impacted 500 °C IC operational yield and lifetime for this wafer.

### Introduction

Solid state integrated circuits that are capable of prolonged and stable 500 °C operation would enable new applications of sensors in the area of aerospace, aeronautics, energy production, and Venus missions [1]. Increasing the complexity of circuits while also increasing reliability at elevated temperatures has been the focus of on-going work at NASA Glenn. The fabrication and testing of 4H-SiC JFET prototype IC's fabricated on a single 76mm diameter 4H-SiC epitaxial wafer with two levels of metal interconnect capable of prolonged operation at 500 °C is reported in another submission to this conference proceedings [2]. While 500 °C operation in excess of 1000 hours was obtained on a few ICs, other prototype ICs (some nominally identical) failed before 300 hours at 500 °C. Some circuits even failed at temperatures less than 300 °C. This report presents evidence for four physical degradation/failure mechanisms believed responsible for observed large discrepancies in 500 °C operating time and IC yield.

### Results and Discussion

**Crack Formation Induced Fail-Open of Top Metal Interconnect.** The focused ion beam (FIB) cross-section shown in Fig.1, illustrates an example of dielectric and metal cracks that caused topmost metal conductive interconnect traces to electrically fail open. It is important to note that the crack forms only on the right side of Fig. 1 where the patterned edge of a lower TaSi<sub>2</sub> metal trace slightly overlaps (distorting upward) the edge of a SiC mesa feature due to slight misalignment of these two mask features. Devices close to the wafer center (roughly < 1 cm) did not exhibit this problem as the misalignment in this region was insufficient to result in such overlap/distortion. Misalignment and cracking grew more severe with increasing radial distance from the wafer center, consistent with rotational misalignment of the bottom metal mask pattern to the substrate n-mesa pattern during fabrication. Such cracks are not observed on other kinds of topology, such as where the lower TaSi<sub>2</sub> trace edge ends over the flat SiC region on the left side of Fig. 1. Cracking has neither been observed on the large bond pad edge cross-section shown in Fig. 2. If there had been

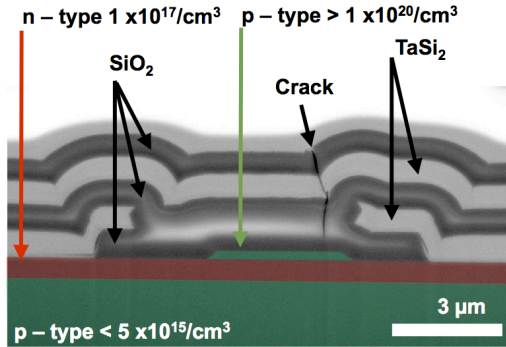


Fig. 1. Cracking sometimes occurs Where metal 1 and metal 2 overlaps the gate.

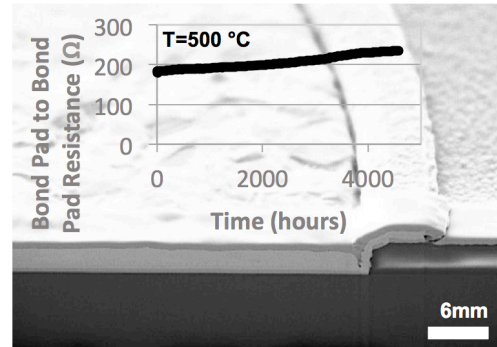


Fig. 2. By design, cracking did not occur around the oxide on bond pads. There was 32% increase in pad to pad resistance over 4800 hours.

cracking at the edge of the bond pad (Fig. 2), previous experiments have shown that the underlying TaSi<sub>2</sub> metal laterally oxidizes causing electrical failure of the bond pad in less than a few hours at 500 °C. The measured resistance vs. time between adjacent connected bond pads plotted in Fig. 2 demonstrates desired minimal change in conduction properties (in part due to absence of crack features) over 4800 hours of 500 °C electrical testing time. Since it is related to misalignment, this cracking problem should be solvable by improved alignment and/or design rules with larger misalignment tolerances so as to prevent overlapping of lower metal edges with mesa features. The SiO<sub>2</sub> where the cracks originated was possibly weakened by water vapor absorption. To inhibit this possible contributing mechanism to the observed cracking, a protective stoichiometric Si<sub>3</sub>N<sub>4</sub> cap is planned for the next wafer run.

**Gate-to-Channel Leakage/Short From Notching of Gate Etch Mask Metal.** As described in [2], the JFET fabrication process starts by patterning a gate etch mask and dry etching ~2000 Å into the SiC to define the p<sup>+</sup> gate. The gate etch mask remains in place for a subsequent self-aligned implant step followed by liftoff patterning of a second metal etch mask that laterally defines the JFET n-channels when an additional ~5000 Å of SiC is dry etched. While the gate etch mask is supposed to prevent removal of any SiC from p<sup>+</sup> gate regions during the second (n-channel) dry etch, this particular JFET IC wafer displayed random notches in the gate mesa pattern. These notches arose from non-uniform oxidation/peeling along the edges of the gate etch mask during a prolonged unplanned storage of the sample in room air. When the second dry (n-mesa) etch was conducted, the notched regions did not sufficiently protect the p<sup>+</sup> SiC from removal, which then exposed underlying n-mesa regions in areas where contacts to p<sup>+</sup> gates were subsequently deposited. Fig. 3 inset shows where a p<sup>+</sup> gate contact overlaps such a notch. This allows the deposited metal p<sup>+</sup> gate contact to also form a parasitic electrical contact to the underlying exposed n-channel epilayer, including along the vertical etched sidewall of the n-epilayer. While both Fig. 3 JFETs demonstrate sufficient turn-off for successful circuit operation at 25 °C, turn-off characteristics of “notched” JFETs are undesirably orders of magnitude larger than notch-free devices. While not directly measured at high T, the leakage mechanisms of metal-semiconductor contacts/diodes are known to increase with anneal time and exponentially with T [3]. Therefore, this parasitic leakage is surmised to contribute to rapid failure of circuits at 500 °C. The degree of notching (and thus the degree of leakage) varied across the wafer. Very few devices with more than 10 gate fingers were free of notches. Notches have not been observed in any process runs before and after this wafer whose processing time between the gate and mesa etches have been a week or less, and were shipped to vendors in vacuum boxes.

**Device Resistance Degradation.** Fig. 4 plots sheet resistance ( $R_{\text{Sheet}}$ ) and specific contact resistance ( $R_{\text{Specific}}$ ) extracted from prolonged measurement of a packaged 500 °C transmission line method (TLM) test device of the source/drain implant for over 1000 hours.  $R_{\text{Sheet}}$  changed less than 1% while  $R_{\text{Specific}}$  changed 50%. This suggests a degradation in the contact area or metal while the

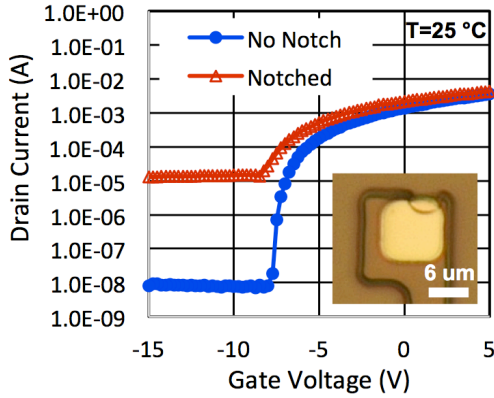


Fig. 3. JFET turn off leakage with and Without a notch in the p-gate mesa.

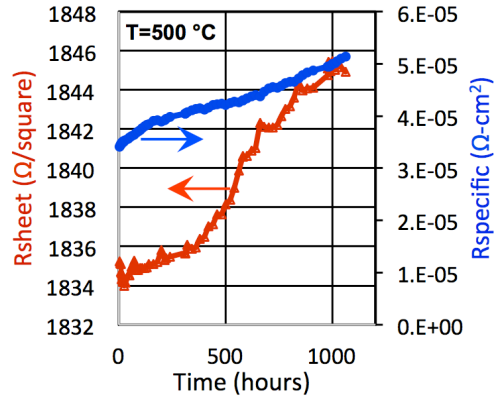


Fig. 4. < 1% variation in  $R_{sheet}$ , but 50% increase in  $R_{specific}$ .

high-dose SiC implanted sheet resistance is stable. The 500 °C testing time evolution of transistor parameters for a JFET in a NOT circuit are shown in Fig. 5. The threshold voltage ( $V_T$ ) changes less than 2% over 2000 hours. Transconductance ( $g_m$ ) and the on-state current ( $I_{DSS}$ ) decrease with time at temperature while on-state resistance  $R_{DS}$  increases, which is qualitatively consistent with the Fig. 4 trend. Data discontinuity shown in Fig. 5 at 1000 hours corresponds to a brief temperature cycle to 25 °C and back. Most of the drift in  $R_{DS}$  recovered during this cycle. It is important to note that the recovery of  $R_{DS}$  seems inconsistent with contact oxidation or metal trace failure mechanisms that would be irrecoverable. Delamination of the contact area has not been seen in focused ion beam (FIB) cut cross-section images of similar devices on the wafer. Therefore, the root physical cause (or causes) of this degradation remains under investigation at this time.

**Parasitic Circuit Imbalance Induced by Mobile Ion Contamination.** Differential amplifier circuits rely on well-balanced circuit legs (i.e., transistors and/or resistors) to operate. Resistive load differential amplifier ICs (including 2-stage op-amps which were also used as sense-amps for test memory ICs) were fabricated and electrically verified as operational at room temperature with expected gains. However, on all ICs custom-packaged for high temperature testing, these differential-based amplifiers all rapidly failed as they were heated past 200 °C. A packaged diff-amp (Fig. 6) underwent bias-temperature stress measurements while directly measuring “balanced” resistors RDD+ and RDD- (highlighted with colored dashed lines) IV characteristics. Fig. 7 shows an example of the resistor IV imbalance measured after +30V 200 °C positive bias stress of the VDD metal trace, while Fig. 8 shows that the imbalance is mostly eliminated following a subsequent -18V 300 °C stress applied to the VDD metal trace. This reversible bias-temperature-time stress behavior is consistent with reversible mobile ion contamination phenomenon well-

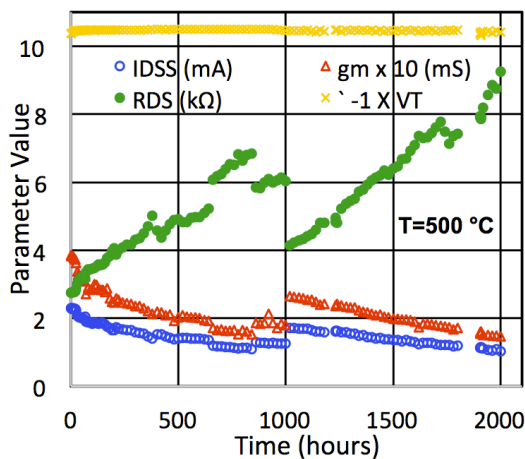


Fig. 5. < 2% variation in  $V_T$ . Note changes from thermal cycle to RT at 1000 hours.

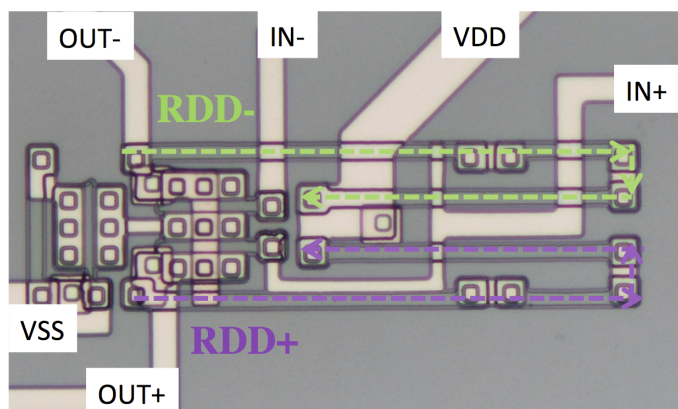


Fig. 6. Optical image of the differential amplifier shows the two balanced resistors with one having a VDD trace pass over top.

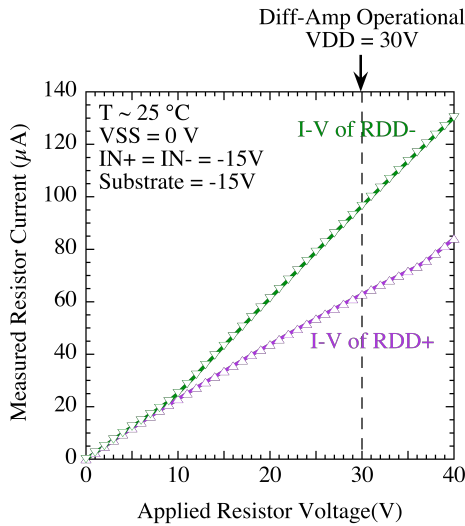


Fig. 7. Diff-amp resistor IV imbalance observed following biased heating (VDD=+30V) to 200 °C and cool down.

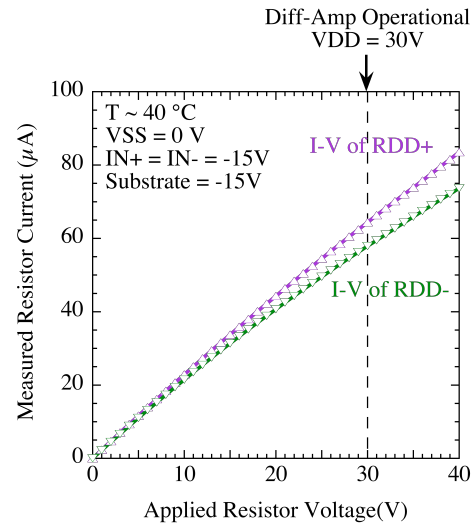


Fig. 8. Observed restoration of diff-amp resistor IV balance following 2 hour 300 °C VDD stress of -18V and cool down.

known to be detrimental to metal-oxide-semiconductor (MOS) devices [4]. In this particular case, positive ions in the oxide become mobile at elevated temperature and are repelled by positive VDD bias, piling up near the SiC-oxide interface beneath the VDD metal. The resulting positive ion charge buildup near the SiC-insulator interface produces a parasitic surface inversion channel of electrons (supplied by the n-mesa resistor), causing turn-on of a parasitic n-MOSFET under the VDD trace which substantially imbalances current flow of RDD- relative to RDD+. Application of negative VDD terminal bias at temperature drives positive ions back towards the gate, turning off the parasitic MOSFET, restoring post-cool down resistor balance (Fig. 8) and experimental room temperature operation of diff-amp and op-amps.

Subsequent surface analysis detected sodium (Na) on the surface of wafer samples. Some sources of sodium contamination in the NASA processing laboratory have been identified and eliminated. Additional processing steps that largely mimic sodium mitigation strategies of the silicon IC industry as well as layout design changes are being implemented for future processing runs [4,5]. However, the effectiveness of these lower-temperature IC strategies to withstand/enable prolonged 500 °C SiC IC circuit operation remains to be proven.

## Summary

Evidence for at least four kinds of device non-idealities (cracking, notching, device resistance degradation, and mobile ions) found on a 4H-SiC JFET IC wafer process for 500 °C operation have been described. Elimination/mitigation of the three most rapid failure mechanisms (cracking, notching, and mobile ions) is believed possible in future wafers with relatively straightforward process improvements.

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