Long-Term Reliability of a Hard-Switched Boost Power Processing Unit Utilizing SiC Power MOSFETs

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***Abstract* - Silicon carbide (SiC) power devices have demonstrated many performance advantages over their silicon (Si) counterparts. As the inherent material limitations of Si devices are being swiftly realized, wide-bandgap (WBG) materials such as SiC have become increasingly attractive for high power applications. In particular, SiC power metal oxide semiconductor field effect transistors' (MOSFETs) high breakdown field tolerance, superior thermal conductivity and low-resistivity drift regions make these devices an excellent candidate for power dense, low loss, high frequency switching applications in extreme environment conditions. In this paper, a novel power processing unit (PPU) architecture is proposed utilizing commercially available 4H-SiC power MOSFETs from CREE Inc. A multiphase straight boost converter topology is implemented to supply up to 10 kW full-scale. High Temperature Gate Bias (HTGB) and High Temperature Reverse Bias (HTRB) characterization is performed to evaluate the long-term reliability of both the gate oxide and the body diode of the SiC components. Finally, susceptibility of the CREE SiC MOSFETs to damaging effects from heavy-ion radiation representative of the on-orbit galactic cosmic ray environment are explored. The results provide the baseline performance metrics of operation as well as demonstrate the feasibility of a hard-switched PPU in harsh environments.**

Keywords – SiC, Power MOSFETs, Boost, PPU, high temperature, HTGB, HTRB, SEE, radiation, SEB, SEGR

I. INTRODUCTION

With the expedient maturation of silicon-carbide (SiC) device technology, a great deal of interest has been generated in the development of switching power applications capable of harnessing the inherent wide-bandgap (WBG) properties of the material. SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) in particular offer significant benefit over their silicon counterparts. The potential for lower total switching loss, higher breakdown field tolerance and superior thermal performance make SiC devices highly attractive for high temperature and extreme environment applications [1]. Though successful power conversion implementations show promise [2-6], these noteworthy device innovations have yet to directly translate into pragmatic power conversion systems for extreme environments. Therefore, it is still necessary to evaluate the application-specific performance of these devices to fully understand thermal limitations as well as estimate the overall device reliability. This paper describes a design-for-reliability approach to an innovative power processing architecture intended for in-space solar electric propulsion systems. The work herein also presents reliability data on CREE's commercially available generation I and generation II N-channel enhancement mode SiC MOSFETs.

Figure 1 depicts a schematic representation of the proposed SiC High Temperature Boost (HTB) Power Processing Unit (PPU) architecture for in-space solar electric propulsion (SEP) [1]. A large solar array converts available solar energy into electrical energy that is distributed throughout the system by a central power management and distribution (PMAD) interface. Input power provided from the PMAD drives a power scalable (10-80 kW) HTB-PPU architecture responsible for powering the subsequent propulsion stages. This work focuses primarily on the operational performance of the Anode (Boost) Power Assembly of the PPU. A multiphase straight boost topology is employed using CREE's 1.2kV C2M family SiC Power MOSFETs and Schottky Barrier Diodes [6-8]. This novel system implementation takes full advantage of the emerging SiC technology and high temperature device packaging to produce a thermally robust, scalable, power dense design capable of maintaining favorable operation in harsh environmental conditions. However, in order to more gainfully

utilize these SiC device technologies, a great deal of emphasis must still be placed on evaluating the devices' static and high frequency switching performances. In this work, an application-specific model is developed to gauge the overall system efficiency and stability as well as forecast the long-term reliability of SiC MOSFETs in a hard-switched boost implementation operating at baseline temperature of 100 °C. In addition, susceptibility of the MOSFETs to damaging effects from heavy-ion radiation representative of the galactic cosmic rays to which the in-space HTB-PPU system will be exposed are explored.

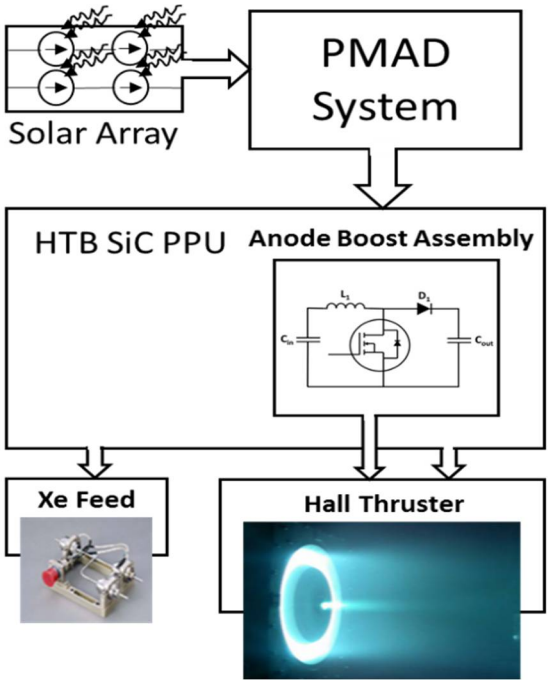

Figure 1 *Schematic diagram of proposed in-space solar electric propulsion (SEP) architecture for deep space application. An integrated High Temperature Boost (HTB) Power Processing Unit (PPU). Photonic energy is converted to electricity by the solar array and the resultant energy is regulated and distributed by the Power Management and Distribution (PMAD) system providing an unregulated output power to the PPU. The anode power assembly module is composed of a typical straight boost design utilizing commercially available SiC MOSFETs and diodes for switching.*

It has been shown that consequential reliability issues preside at the SiO_2/SiC interface in planar MOSFETs structures resulting in volatile gate threshold performance [9-13]. From a systems perspective, it proves critical to account for such variations in the turn-on threshold of the gate drive design to avoid unfavorable behaviors. Therefore, it is imperative to explore the device's reliability due to this common mode of failure. High Temperature Gate Bias (HTGB) and High Temperature Reverse Bias (HTRB) are very common tests performed to characterize the robustness of the gate oxide as well as junction integrity [14]. Both tests are performed in the work herein. The resultant data are interpreted using the cumulative damage model with the Arrhenius relation to estimate the expected device lifetimes at various high temperature conditions. The Eyring model is then used to correlate the device lifetime as a function of the external gate drive voltage and device junction temperature. Device lifetime is then plotted versus the external gate drive voltage at a range of junction temperatures (T_j). Furthermore, it is demonstrated that gate oxide lifetime is highly dependent on the applied external bias.

The overall efficiency for the anode power assembly is assessed using commercial SPICE software. At high temperature, it is initially presumed that the overall system efficiency is dominated by the high frequency switching loss within the MOSFETs and that the loss is then constant at the operational temperature. However, since the on-state resistance is susceptible to increase at elevated temperatures due to the internal junction field-effect transistor (JFET) and drift layer resistance, the system level performance can then be simulated with respect to this increasing conduction loss (on-state resistance). Efficiency as a function of increasing on-state resistance for the generation I and generation II 1.2 kV n-channel SiC MOSFETs from CREE, Inc. are evaluated. It is shown that maintaining a sufficient power efficiency margin is quite feasible due to moderate rise in the MOSFET's on-state resistance. Moreover, process improvements between generation I and generation II devices suggest a higher tolerance due to on-state resistance variability in this particular system. A continuing effort is being placed on studying the effects of switching loss at high temperatures and discovering the nature of its influence on the reduction of system efficiency. This paper presents a more thorough discussion of these results as well as the HTGB and HTRB testing, switching loss behavior, and effects of radiation on the SiC MOSFETs. Additionally, the assumptions presumed in the lifetime model are presented herein.

II. EXPERIMENTAL SETUP

The considered device voltage and current ratings range from 1.2-1.7 kV and 90-4.9 A respectively. Each device is equipped with a standard TO-247-3 plastic package with the devices mounted on a metal plate heat sink. The fundamental MOSFET device characteristics, including threshold voltage, on-state resistance and breakdown voltage, are statically characterized at elevated temperatures to accelerate intrinsic failures. A nominal time to failure is then deduced from the contributing failure mechanism and the device lifetime extrapolated.

HTGB characterization methods are commonly employed to monitor threshold voltage (V_{TH}) and on-state resistance ($R_{DS(on)}$) variations of power MOSFET devices. An external DC bias is continuously applied from gate-to-source on the device under test (DUT) at an elevated temperature in order to induce

failure modes within the oxide. The devices are placed in an industrial oven at a constant temperature ranging from 125-175°C. A sample size of 3-5 devices is selected for each bias condition. The device junction temperature is assumed to be approximately equal to the ambient temperature. A constant gate-to-source voltage (V_{GS}), ranging from 20 – 40 V, is applied during the Stress phase of the measurement using Keithley's 2651A Source Measurement Unit (SMU). The external bias is then briefly removed to evaluate the deviations in the MOSFET characteristics. Figure 2(a) illustrates the measurement circuit.

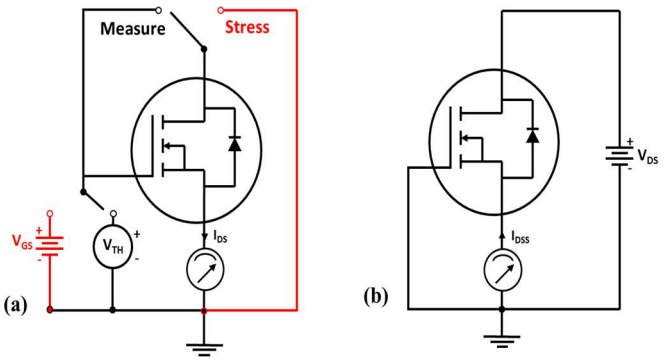

Figure 2 *Experimental setup a) High Temperature Gate Bias (HTGB) b) High Temperature Reverse Bias (HTRB).*

HTRB characterization is used to monitor the drain-source leakage current (I_{DSS}) through the built-in body diode of the power MOSFET. Similarly, a high voltage DC external bias is applied from drain to source of the DUT at elevated temperatures. A constant drain-source bias is applied while I_{DSS} is measured simultaneously using a Keithley 2657A SMU. This test setup is depicted in Figure 2(b).

III. RESULTS AND DISCUSSION

A. SiC MOSFET Reliability

The threshold voltage characteristic of CREE Inc. SiC MOSFETs (Generation I & II) is characterized with HTGB gate-source voltages of 20, 30, and 40 V at ambient temperatures of 125, 135, 145, and 150 °C. Significant threshold voltage drifts are observed and are associated with the tunneling of electrons at the oxide/semiconductor interface due to the applied gate stress [10]. The failure criterion associated with oxide failures is the rise in threshold voltage corresponding to >200% increase in threshold voltage. The failure criterion is arbitrarily chosen to corresponding to a percentage reduction in system efficiency. To conserve time in each experiment, a logarithmic approximation is used to estimate ΔV_{TH} when a linear trend emerges (Figure 3). The linear trend suggests a positive threshold shift with increasing gate bias stress. Extrapolating the linear trend in Figure 3 out to later stress times we can estimate the gate bias induced threshold drift after long periods of stress.

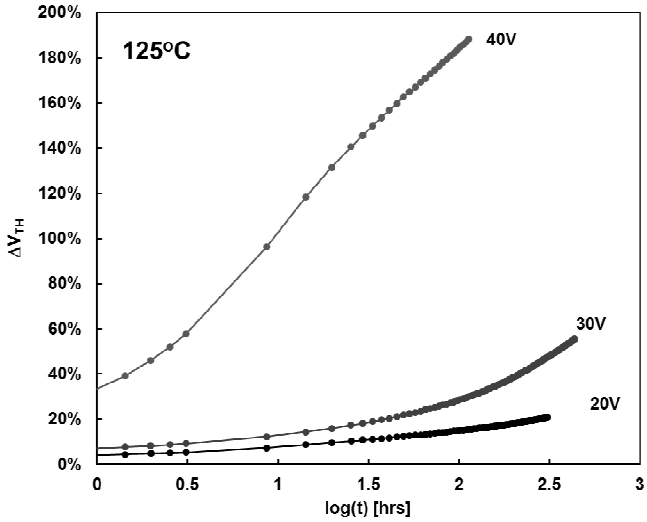

Figure 3 *Threshold voltage drift due to increasing gate-source stress at 125 °C.*

The threshold voltage drift is significantly intensified with an increasing electric field across the gate oxide. Figure 3 illustrates the effect of increased gate oxide electric field strength on threshold voltage. The increasing distribution of hot electrons entering the oxide through the oxide/semiconductor interface significantly increases the threshold voltage. This effect is noticeably intensified beyond 30V applied from gate to source and is likely due increasing gate overstress.

Fowler-Nordheim (FN) tunneling is typically acknowledged as the primary cause of this form of oxide degradation. Unfortunately, FN tunneling drastically reduces the oxide reliability at high gate-source bias conditions. This mechanism has been observed in the first generation devices from CREE Inc. Second generation devices are also considered and show considerable reduction in electron tunneling through the oxide/semiconductor barrier. The reduction of this effect is attributed to device level and process level improvements made by the manufacturer. Figure 4 shows the variation in threshold voltage for both generation I (CMF20120D) and generation II (C2M0025120D) devices. A reduction in the electron tunneling mechanism is concluded from the decreased threshold voltage shift across device families. It is also observed that the threshold shift due to increasing temperature at constant gate stress is greatly reduced. Moreover, the threshold shift at constant temperature between gen. I and gen. II devices is also significantly diminished. It is noteworthy to mention that the 2nd generation MOSFET devices have a more subtle stress induced threshold voltage drift than its predecessor. The threshold drift in the 1st generation devices exhibit an exponential change with temperature and applied stress time. The minimum gate bias condition to which the reduction in threshold drift can be observed among these devices currently unknown.

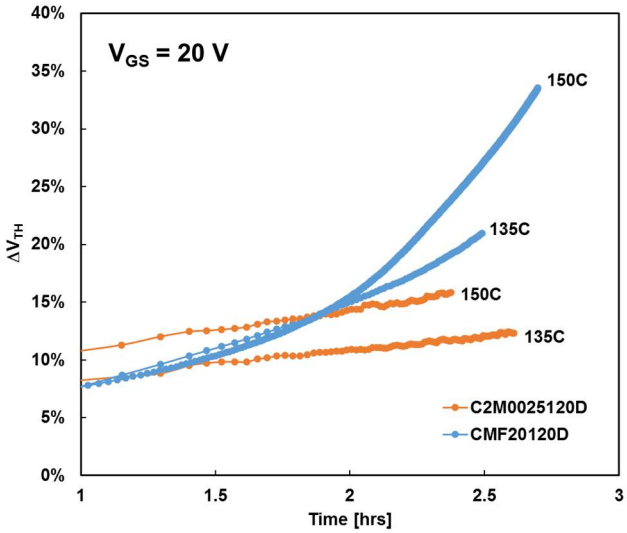

Figure 4 *Threshold voltage drift due to 20V gate-source bias for generation I (CMF20120D) and generation II (C2M0025120D) from CREE.*

Since this work is predominantly concerned with the on-state current performance of the power MOSFETs, only positive gate bias conditions are considered in this work. Therefore, positive bias, HTGB characterization is sufficient to evaluate the effects of electron tunneling and trapping in the gate oxide. These mechanisms contribute to cumulative degradation failure modes, which are used to project oxide reliability due to these effects. A lognormal distribution is assumed to describe device failure. It is expected that lognormal statistics is an adequate representation of the threshold-voltage of MOS devices when low number sample sizes are considered. The resultant characteristic lifetimes are shown in Figure 5.

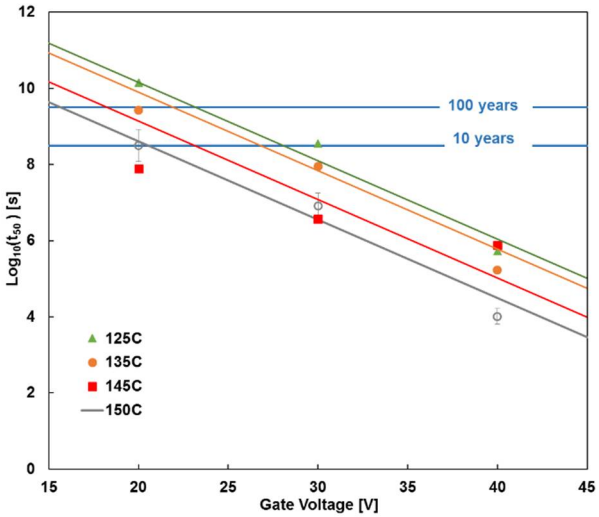

Figure 5 *Projected lifetimes using measured median values with constant applied gate-source bias. The lifetime is based on experimental HTGB data measured at 20V, 30V and 40V V_{GS}.*

The E model is applied to estimate oxide lifetime at low gate-source stress. This approach offers a worst-case estimation of lifetime since the devices are characterized at constant stress levels greater than the intended operational range. From the projected lifetimes, it is evident that the voltage acceleration factor is fairly independent of temperature and thus, a nominal lifetime can be deduced for devices operating within the temperature range. Table I summarizes the estimated median lifetimes as a function of applied gate bias at each particular junction temperature. Since the oxide is believed to be the primary mode of failure in power MOSFET devices, the overall device lifetime is also inversely proportional to the applied gate bias. Increasing the applied field across the oxide, effectively increases the rate of hot-electron injection across the oxide/semiconductor interface and reduces the overall reliability substantially. Many studies have highlighted this susceptibility in MOS devices [9-15].

TABLE I
MAXIMUM GATE BIAS CONDITIONS

Temp.	**10 yrs.**	**15 yrs.**	**20 yrs.**	**100 yrs.**
125 C	28.068 V	27.214 V	26.607 V	23.214 V
135 C	26.821 V	25.966 V	25.360 V	21.966 V
145 C	23.132 V	22.277 V	21.670 V	18.277 V
150 C	20.588 V	19.733 V	19.127 V	15.733 V

The Arrhenius relation is commonly used to describe accumulation failure rates in semiconductor material due to thermal stress. The failure rate is inversely proportional to the device lifetime and is described by $1/r = \tau \propto e(E_a/kT)$, where τ is the characteristic lifetime, E_a is the activation energy, T is the absolute temperature in Kelvin and k is Boltzmann's constant. Similarly, it is applied to define the device lifetimes temperature dependence over the entire test range. Furthermore, a sufficient level of screening by the manufacturer is assumed to successfully remove weak devices from the sample, therefore no bimodal effects are taking into account. Activation energies between 0.3 and 0.6 eV are observed.

The reliability of the power MOSFET's drain-source body diode is also of great concern when considering a high temperature, high voltage switching applications. HTRB is employed to measure the variation in the zero gate bias drain-source current. This test is used to evaluate junction integrity and degradation effects [14]. The DUTs are evaluated at drain-source voltages greater than rated breakdown voltage (BV_{DSS}) and the body diode reliability is linearly extrapolated at lower bias conditions. The drain-source stress ranges from 1620 to 1720 V. Figure 6 shows the characteristic lifetime of the drain side. Lifetimes of over 100 years are achievable at 150°C with drain-source voltage of 1000V consistent with device specifications from CREE Inc. [16].

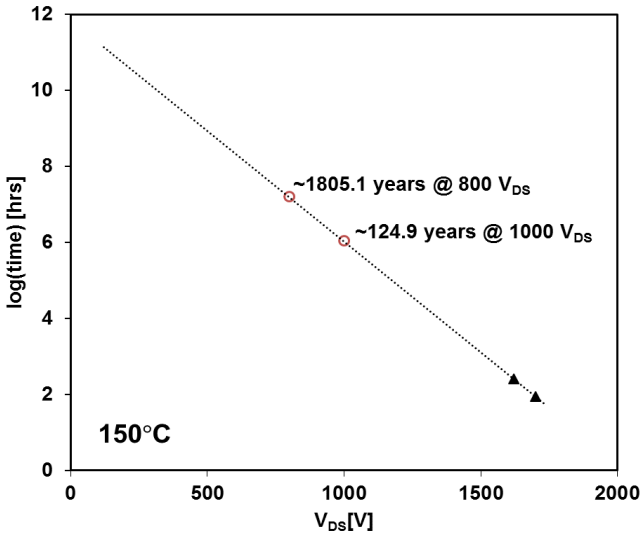

Figure 6 *HTRB voltage accelerated test of drain-source body diode with zero gate bias. Lifetimes greater than 100 years at up to 1000V drain-source bias with zero gate bias are achievable at 150°C*

Drain leakage current is commonly attributed to pn junction and oxide trap induced leakage effects [14]. HTRB offers a more pessimistic estimation of the junction integrity than the use condition and is sufficient for projecting junction lifetime. It should be noted that large drain-source bias may also provide additional gate oxide stress and further contribute to gate oxide degradation. In the study, it is assumed that this effect is minimal. The cumulative degradation effects caused to the gate oxide and the drain-source junction are individually assessed and characterized as such using HTGB and HTRB respectively.

B. Output Power Efficiency Model

The Anode Power Assembly considered in the study implements a multiphase straight boost topology. Figure 7 shows the circuit diagram used to achieve 10kW boost conversion. Each phase of the interleaved design utilizes both 1200V/20A and 1200V/10A SiC power MOSFET and Schottky barrier diode (SBD) respectively. Though the SiC SBDs experience similar junction failure modes as the power MOSFETs, their long-term reliability is not assessed in this work.

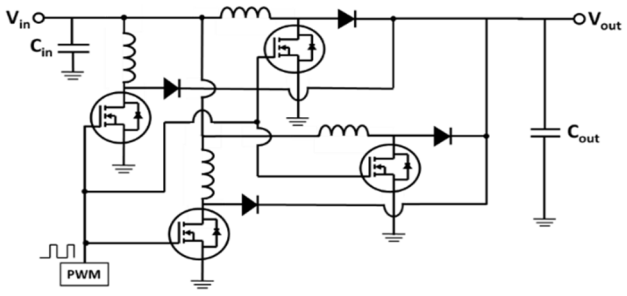

Figure 7 *Multiphase straight boost topology used to achieve 10kW conversion.*

The performance of the power assembly is test to demonstrate feasibility. The figure of merit used to assess the performance is the overall output power efficiency. Through extensive SPICE simulation, it is deduced that minimal power is dissipated through the passive circuit elements and the majority of the performance losses are attributed to switching and conduction loss in the power MOSFET devices. The total switching energy is shown to be reasonably constant at temperatures above 100°C [6][7]. Figure 8 shows the results of clamped inductive switching testing as performed on a power MOSFET device after HTGB characterization.

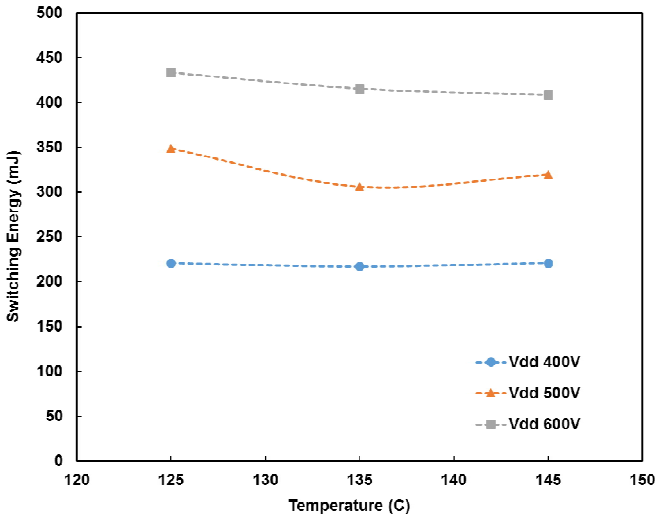

Figure 8 *Total switching loss due to clamped inductive switching at V_{DD} = 400V, 500V and 600V on MOSFET after 125°C HTGB.*

Switching loss testing confirms that the total loss due to switching can be held constant at elevated temperature. This is not the case with the observed conduction loss of the power MOSFETs. Since the on-state resistance is known to significantly increase with temperature, adversely, the conduction loss will increase proportionately. Therefore, extreme changes in the on-state resistance will lead to substantial performance degradation of the power supply. Though negligible variation in the on-state resistance is observed during HTGB characterization, the on-state resistance can be used as a performance metric to assess worst case performance reduction. Figure 9 displays the normalized system efficiency as a function of the normalized MOSFET on-resistance. A tenfold increase in the on-state resistance of the first generation device (*CMF20120D*) is shown to yield a 5% reduction in power efficiency. Similarly, a tenfold increase in on-state resistance of the second generation devices shows a substantial improvement of less than 2% efficiency reduction. Insignificant drift levels in $R_{DS(on)}$ were observed after prolonged periods of HTGB. Therefore, the likelihood of encountering such drastic changes in on-state resistance remain very small.

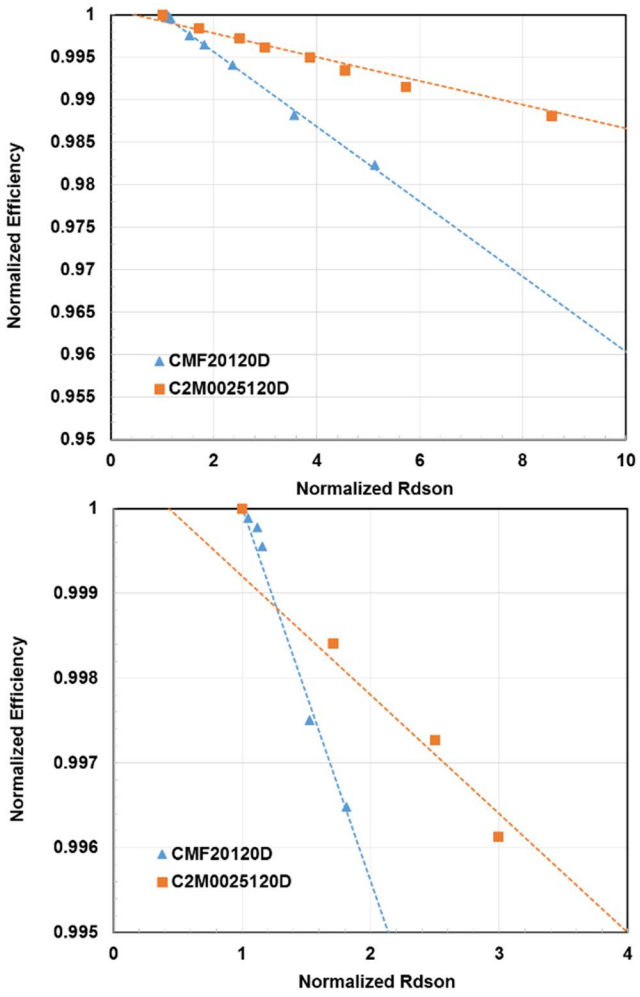

Figure 10 *System efficiency as a function of normalized MOSFET on-resistance. The overall system efficiency is tolerant to very large increases in $R_{DS(on)}$ assuming minimal shifting of total switching loss.*

C. Radiation Effects

Susceptibility to atmospheric cosmic radiation is of major concern for SiC devices [13]. Similarly, SiC power devices have not performed well under heavy-ion irradiation representative of the on-orbit galactic cosmic rays, suffering both degradation and catastrophic single-event effects (SEE) [17-18]. The mechanisms of heavy-ion induced degradation and failure are an active area of research [19-21]. In this work, heavy-ion test data are presented for the CREE C2M 1.2 kV SiC power MOSFET.

Heavy ion SEE tests were conducted at the Lawrence Berkeley National Laboratory (LBNL) [22] in vacuum with 10 MeV/u xenon or argon. Figure 10 shows a diagram of the irradiation test circuit. Bare die (CPM2-1200-0025B) were assembled in TO-3 cans without lids, and a controlled 1-mil parylene-C coating was then deposited to prevent the bond wires from arcing under high voltage. Beam energy at the surface of the die after passing through the coating was determined using the SRIM code [23] to be 966 MeV for xenon, with a linear energy transfer (LET) in SiC of 65 MeV-cm^2/mg and a penetration range of 45 μm; for argon, energy = 361 MeV, LET = 11 MeV-cm^2/mg, and range = 77 μm. Prior to and after each irradiation, the gate-source leakage current (I_{GSS}) and I_{DSS} and/or the BV_{DSS} were measured. During irradiation, V_{GS} was held at 0 V, a positive V_{DS} was applied, and the gate and drain currents were continuously measured and recorded via Keithley 2635A or 2400, and 2657A SMUs.

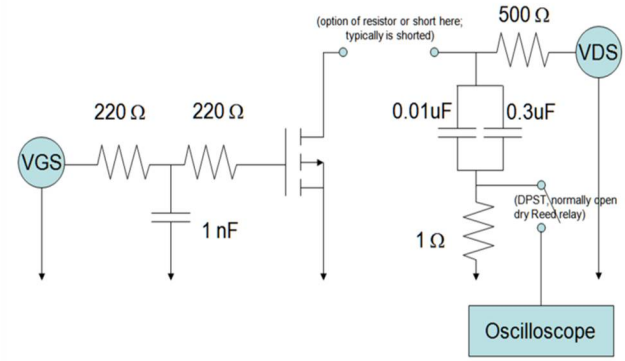

Figure 9 *Diagram of MOSFET irradiation test circuit. (Diagram of diode irradiation test circuit to be included in final paper). DPST = double-pole, single-throw switch.*

At biases suitable for PPU applications, immediate catastrophic failure of the device occurred upon beam exposure. Under xenon irradiation at 600 V_{DS}, gate and drain currents immediately jumped to compliance levels and post-stress tests revealed a shorted drain-source and $I_{GSS} > 1$ mA compliance. At lower voltage, permanent degradation of the drain and/or gate leakage current occurred linearly as a function of fluence. The slope of this degradation increased with increasing temperature, as can be seen in Figure 11 where the change in leakage current during the beam run as a function of fluence is shown for a single part irradiated at 300 V with xenon at 28 °C, 75 °C, and 97 °C case temperature. In silicon power MOSFETs, single-event burnout (SEB) susceptibility during radiation testing is often reduced by elevated temperature due to the decreased charge mobility. SEB in silicon power MOSFETs typically involves the turn-on of the parasitic bipolar junction transistor [22]. The behavior of silicon carbide power MOSFETs differs: in addition to immediate catastrophic failure, there is a voltage range at which permanent substantial degradation of leakage current occurs [18] that worsens with increasing temperature. It is more likely that the mechanisms in SiC MOSFETs are more direct and need not involve the parasitic bipolar transistor. As demonstrated by Mizuta, et al., [20] and Abbate, et al., [21], the electric fields in SiC power devices are much higher than those in Si devices, resulting in more heat generation upon charge ionization that can result directly in local thermal destruction of the lattice.

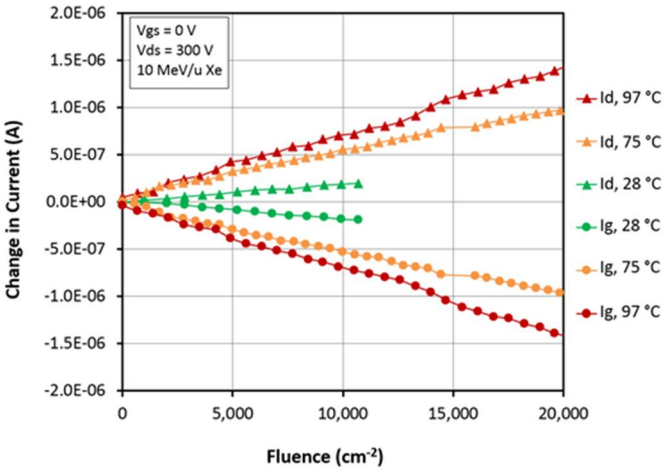

Figure 11 *Degradation of both drain and gate currents during irradiation with xenon while biased at 0 V_{GS} and 300 V_{DS} is very linear with ion fluence. The degradation rate during irradiation increases with increasing case temperature.*

In addition to burnout in the SiC material, the MOSFETs are susceptible to latent damage in the gate oxide. As shown in Figure 12 for the CREE MOSFETs irradiated under 100-V drain-source bias with xenon, this degradation is fluence-dependent, such that no single ion causes the part to go out of specification under these conditions. Irradiation with the much lighter ion, argon, at 100 V_{DS} up to a fluence of $5x10^5$ cm^{-2} resulted in no measurable change in I_{GSS}.

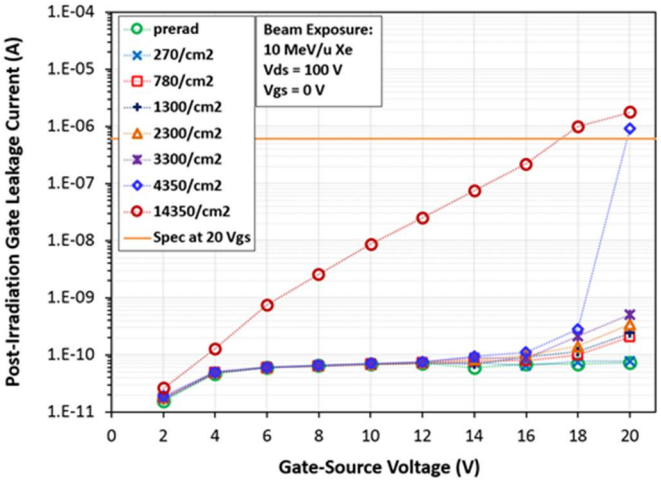

Figure 12 *Upon irradiation with xenon at 100 VDS, only latent damage to the gate leakage current was found. The post-irradiation gate stress test reveals increasing gate leakage current with increasing fluence.*

Clearly, from a radiation hardness assurance perspective, there is work to be done to ruggedize these commercial MOSFETs for space applications. Fortunately, there is growing interest in the manufacturing community to address the susceptibilities in order to achieve SiC power devices that can be operated at a much greater percentage of their electrical ratings.

IV. SUMMARY

In this work, a novel architecture for in-space solar electric propulsion is presented. A multi-phase, hard-switched, straight boost design utilizing commercially available SiC power MOSFET device is proposed to implement a power scalable 10-80kW supply. First and second generation devices from CREE Inc. are evaluated with HTGB and HTRB characterization methods and are shown to exhibit sufficient gate oxide and drain-side junction robustness over the evaluated range of conditions and comply with manufacturer specifications. The overall system performance is then assessed with SPICE simulation and correlated with variation in MOSFET characteristics. Furthermore, it is shown that the SiC power MOSFETs display long-term oxide and junction reliability at elevated temperatures and hold great potential for missions requiring high operational temperatures and long-standing component dependability. With continual device improvements, maturing process technology, and radiation hardening efforts SiC power devices show promise for future high power, high efficiency deep space applications.

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