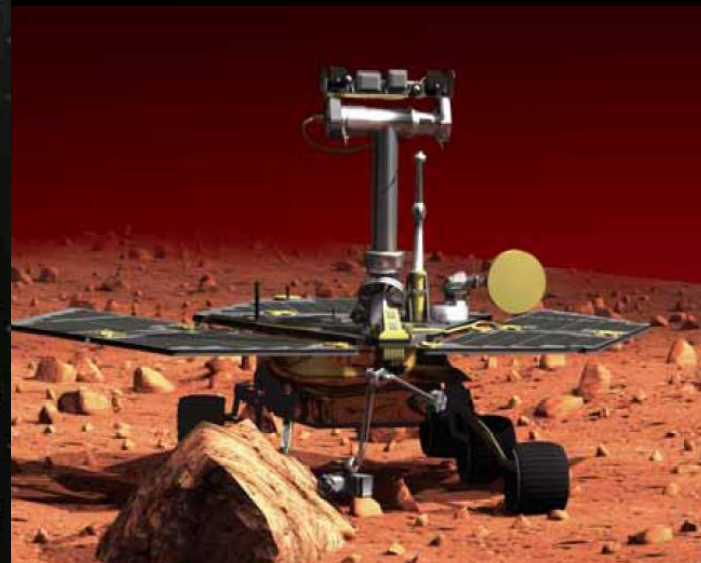
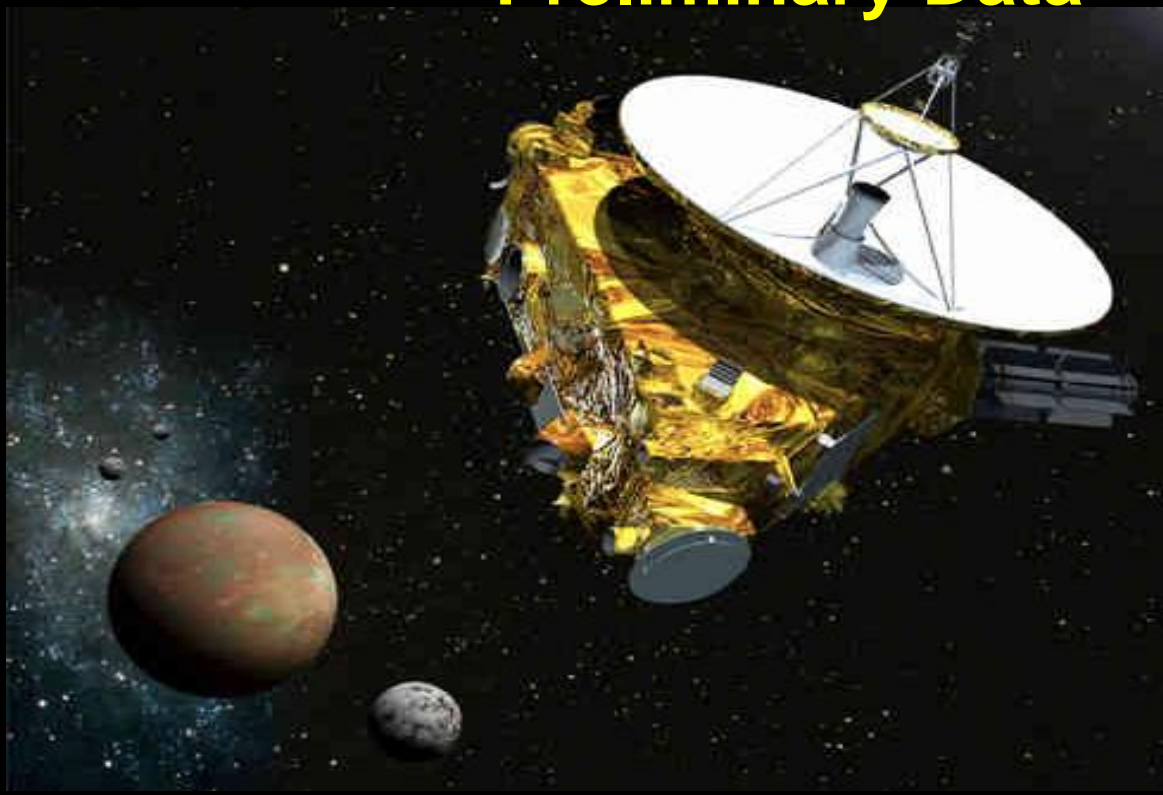




NEPP Independent Single Event Upset Testing of the Microsemi RTG4: Preliminary Data

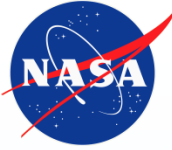


Melanie Berg, AS&D in support of NASA/GSFC

Melanie.D.Berg@NASA.gov

Kenneth LaBel, NASA/GSFC

Jonathan Pellish, NASA/GSFC



Acronyms

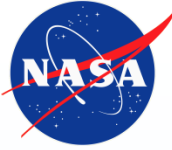
- **Clock conditioning Circuit (CCC)**
- **Combinatorial logic (CL)**
- **Dedicated Global I/O (DGBIO)**
- **Design under analysis (DUA)**
- **Device under test (DUT)**
- **Double data rate (DDR)**
- **Edge-triggered flip-flops (DFFs)**
- **Field programmable gate array (FPGA)**
- **FDDR: Double Data Rate Interface Control;**
- **Global triple modular redundancy (GTMR)**
- **Hardware description language (HDL)**
- **Input – output (I/O)**
- **Linear energy transfer (LET)**
- **Local triple modular redundancy (LTMR)**
- **Low cost digital tester (LCDT)**
- **Look up table (LUT)**
- **NASA Electronics Parts and Packaging (NEPP)**
- **Operational frequency (*fs*)**
- **PLL: Phase locked loop**
- **POR: Power on reset**
- **Radiation Effects and Analysis Group (REAG)**
- **SERDES: Serial-De-serializer**
- **Single Error Correct Double Error Detect**
- **Single event functional interrupt (SEFI)**
- **Single event effects (SEEs)**
- **Single event transient (SET)**
- **Single event upset (SEU)**
- **Single event upset cross-section (σ_{SEU})**
- **Static random access memory (SRAM)**
- **Static timing analysis (STA)**
- **Total ionizing dose (TID)**
- **Triple modular redundancy (TMR)**
- **Windowed shift register (WSR)**



Introduction

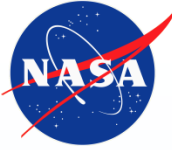
- **This is a NASA Electronics Parts and Packaging (NEPP) independent investigation to determine the single event destructive and transient susceptibility of the Microsemi RTG4 device (DUT).**
- **For evaluation: the DUT is configured to have various test structures that are geared to measure specific potential single event effect (SEE) susceptibilities of the device.**
- **Design/Device susceptibility is determined by monitoring the DUT for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing the DUT to a heavy-ion beam.**
- **Potential Single Event Latch-up (SEL) is checked throughout heavy-ion testing by monitoring device current.**

Preliminary Investigation Objective for DUT Functional SEE Response

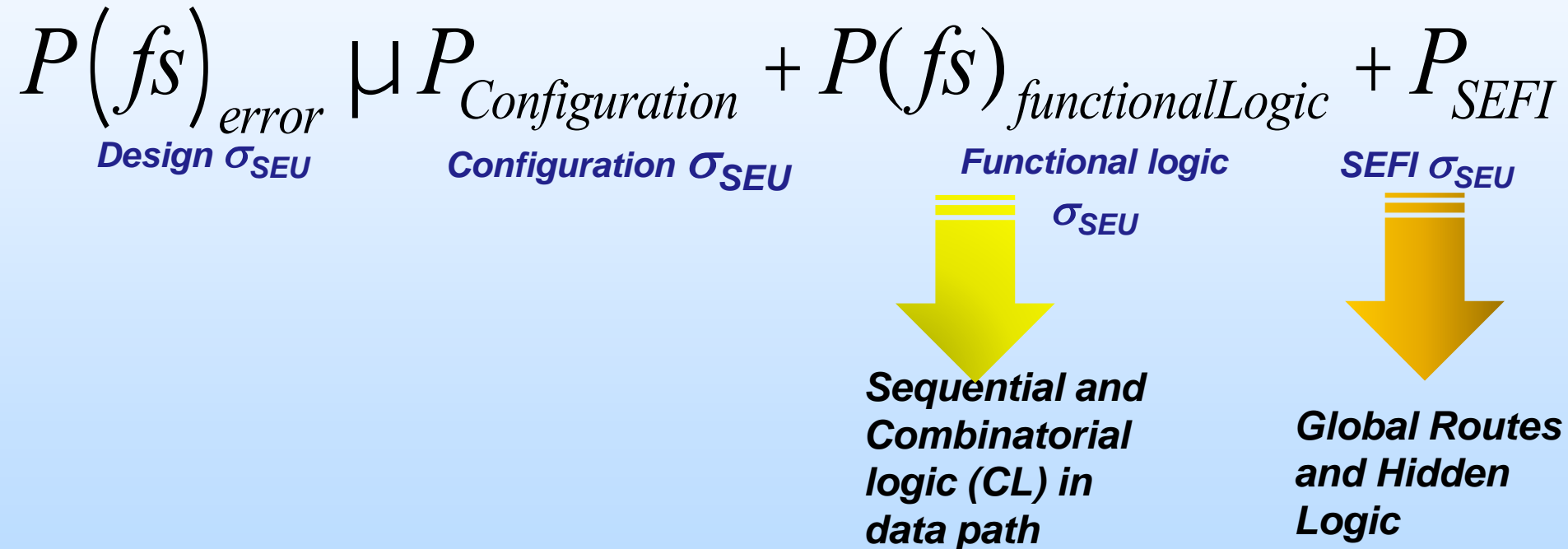


- **The preliminary objective, of this study, is to analyze operational responses while the DUT is exposed to ionizing particles.**
- **Specific analysis considerations:**
 - **Analyze flip-flop (DFF) behavior in simple designs such as shift registers.**
 - **Compare SEU behavior to more complex designs such as counters. Evaluating the data trends will help in extrapolating test data to actual project-designs.**
 - **Analyze global route behavior – clocks, resets.**
 - **Analyze configuration susceptibility. This includes configuration cell upsets and re-programmability susceptibility.**
 - **Analyze potential single event latch-up.**

FPGA SEU Categorization as Defined by NASA Goddard REAG:



SEU cross section: σ_{SEU}

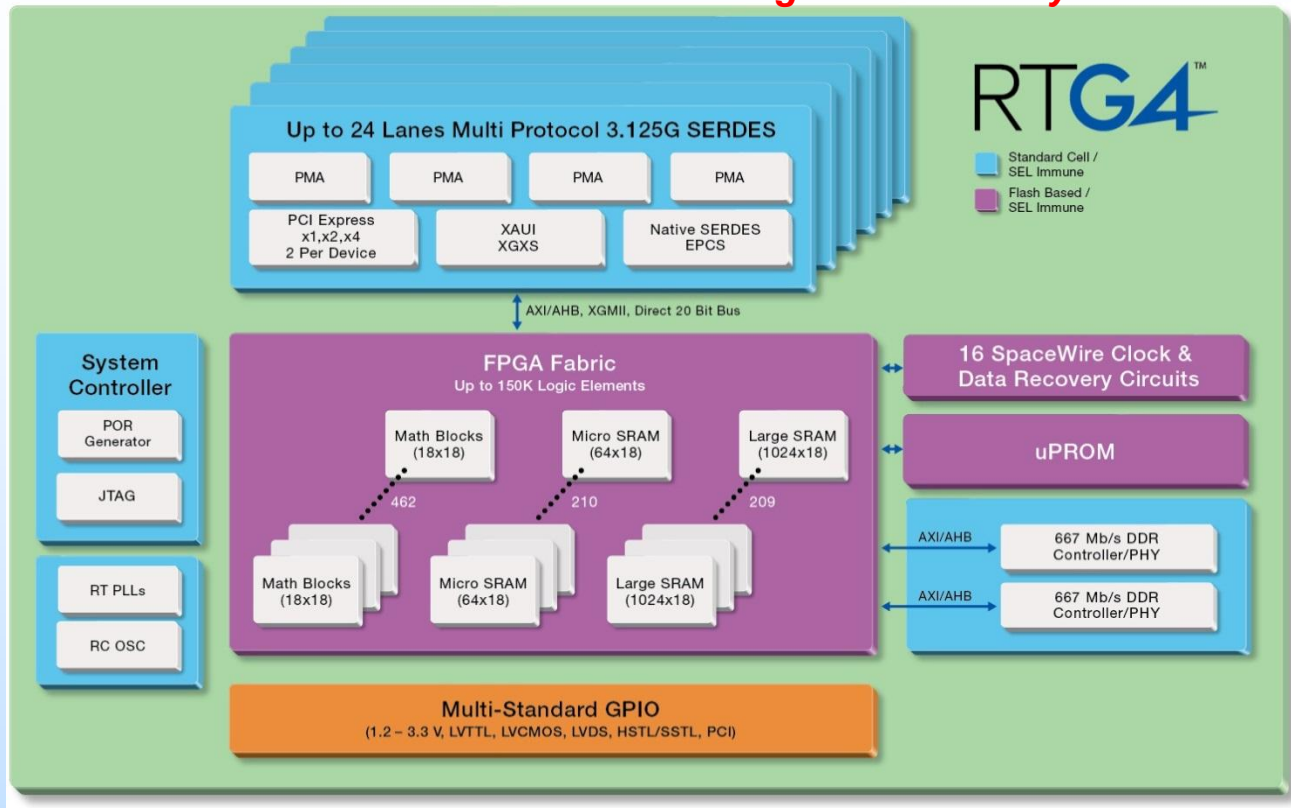


SEU Testing is required in order to characterize the σ_{SEU} s for each of FPGA categories.



RTG4 Radiation-Mitigated Architecture

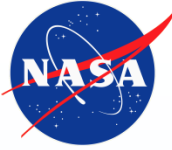
Figure is Courtesy of Microsemi Corporation.



- Total-dose hardening of Flash cells.
- Single-event hardening of registers, SRAM, multipliers, PLLs.

*Comprehensive radiation-mitigated architecture
for signal processing applications*

Microsemi RTG4: Device Under Test (DUT) Details



- The DUT : RT4G150-CG1657M.
- We tested Rev B and Rev C devices.
- The DUT contains:
 - 158214 look up tables (4-input LUTs);
 - 158214 flip-flops (DFFs); 720 user I/O;
 - 210K Micro-SRAM (uSRAM) bits;
 - 209 18Kblocks of Large-SRAM (LSRAM);
 - 462 Math logic blocks (DSP Blocks);
 - 8 PLLs;
 - 48 H-chip global routes (radiation-hardened global routes);

LUT: look up table.

SRAM: sequential random access memory.

DSP: digital signal processing.

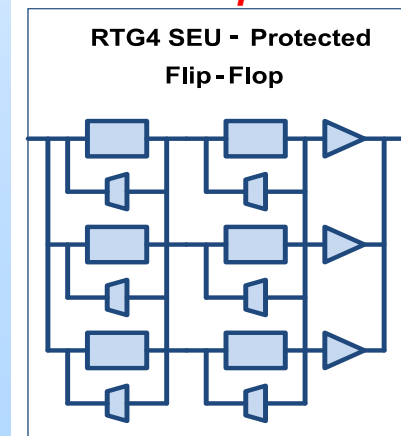
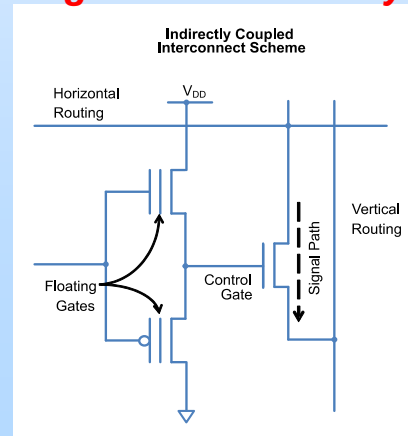
PLL: phase locked loop.

DFFs are radiation hardened using Self-Correcting TMR (STMR) and SET filters placed at the DFF data input.



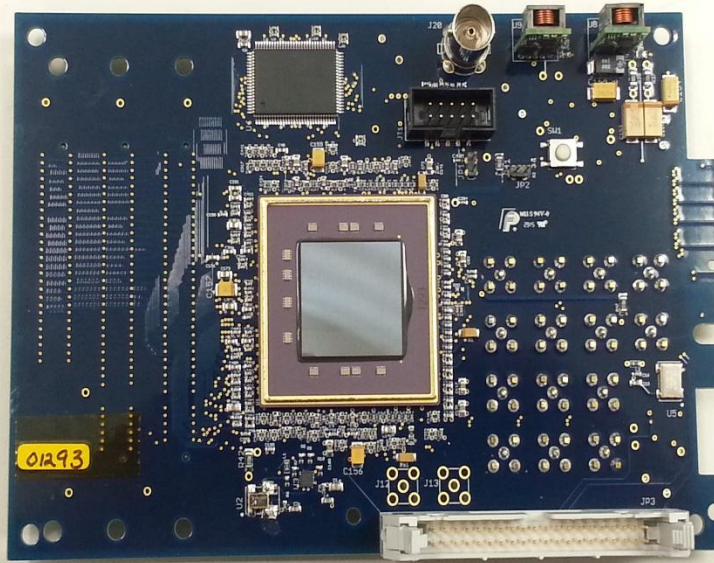
Figures are Courtesy of Microsemi Corporation.

Hardened flash cell →



DUT Preparation

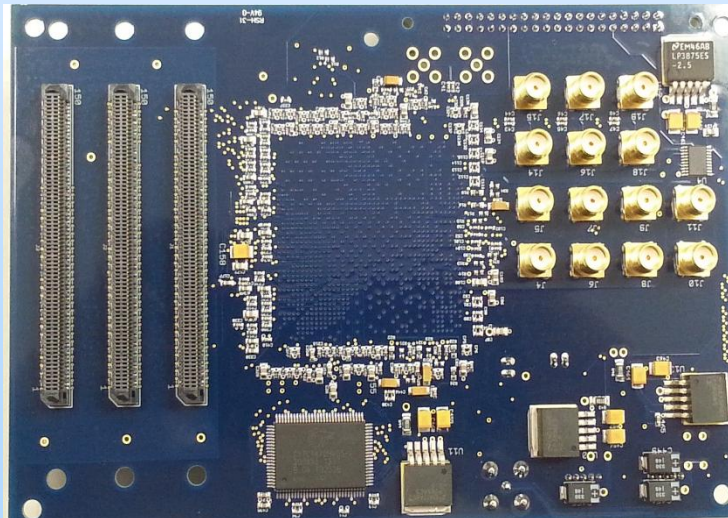
- NEPP has populated two Rev B and one populated Rev C boards with RT4G150-CG1657M devices.
- The parts (DUTs) were thinned using mechanical etching via an Ultra Tec ASAP-1 device preparation system.
- The parts have been successfully thinned to 70um – 90um.



*Top Side
of DUT*



*Ultra Tec
ASAP-1*



*Bottom Side of
DUT*



Challenges for Testing

TID: total ionizing dose

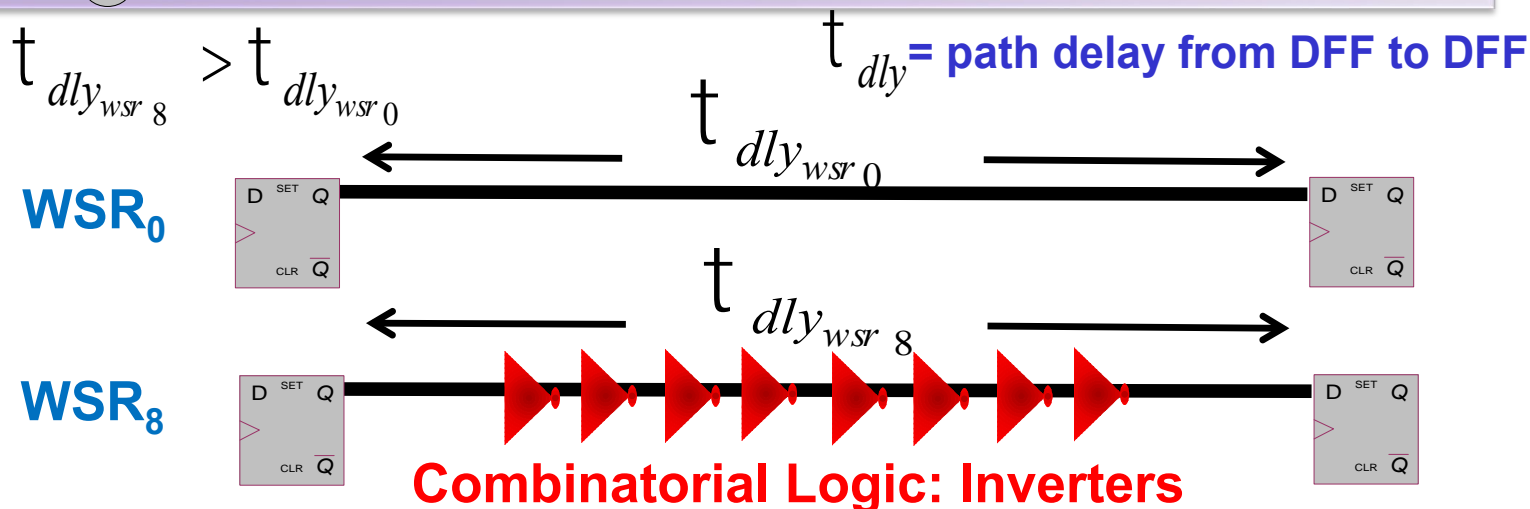
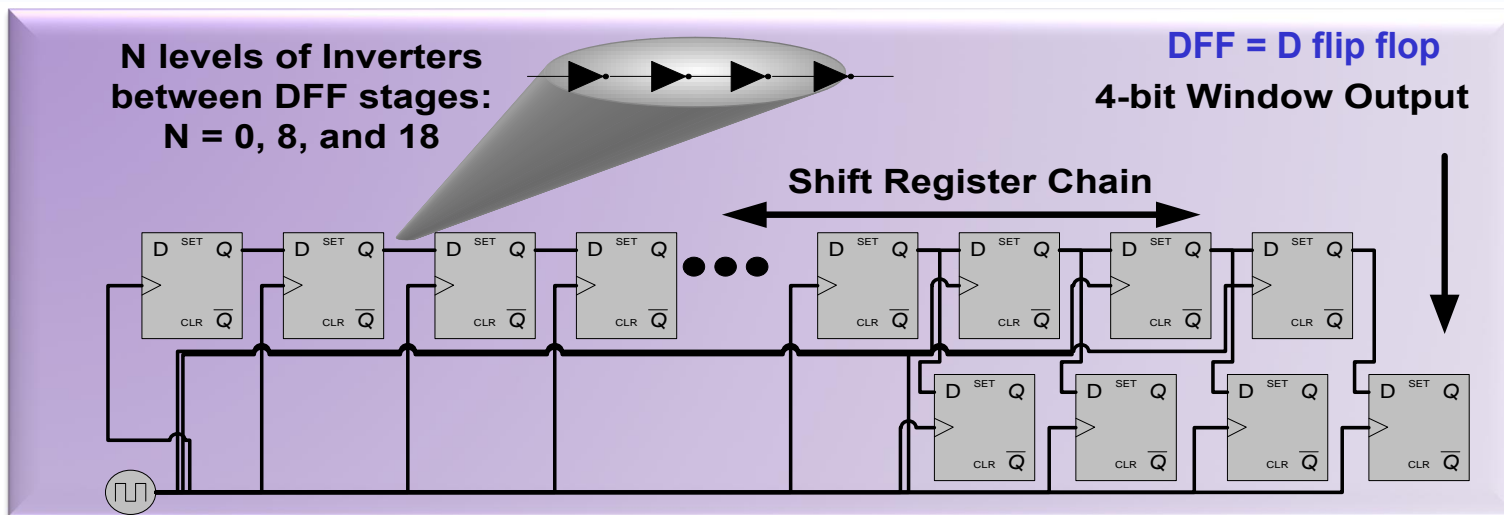
- **Software is new... place and route is not optimal yet. Hence, it is difficult to get high speed without manual placement.**
- **We did not perform manual placement.**
- **Microsemi reports that devices show TID tolerance up to 160Krad.**
 - **Although, when testing with heavy-ions, dose tolerance will be much higher.**
 - **TID limits the amount of testing per device.**
 - **Number of devices are expensive and are limited for radiation testing.**
 - **A large number of tests are required.**
- **We will always need more parts.**
- **Current consortium participants:**
 - **NEPP**
 - **Aerospace**
 - **JPL**
 - **Potential: ESA**

Summary of Test Structures and Operation



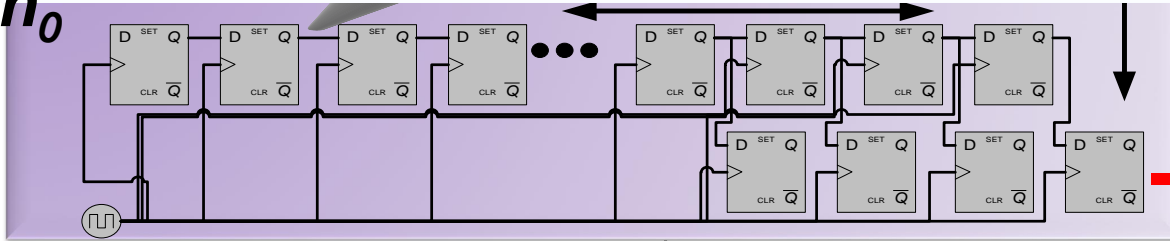
- **Windowed Shift Registers (WSRs):**
 - All designs contained four separate WSR chains.
 - Chains either had 0 inverters, 4 inverters, 8 inverters, or 16 inverters.
 - Resets were either synchronous or asynchronous.
 - Input data patterns varied: checkerboard, all 1's, and all 0's.
- **Counter Arrays:**
 - Resets are synchronous.
 - 200 counters in one array.
 - Two full arrays (400 counters total) in each DUT.
- **Frequency was varied for all designs.**
- **All DFFs were connected to a clock that was routed via RTG4 hard global routes (CLKINT or CLKBUF).**
 - This was verified by CAD summary output and visual schematic-output inspection.

Windowed Shift Registers (WSRs): Test Structure



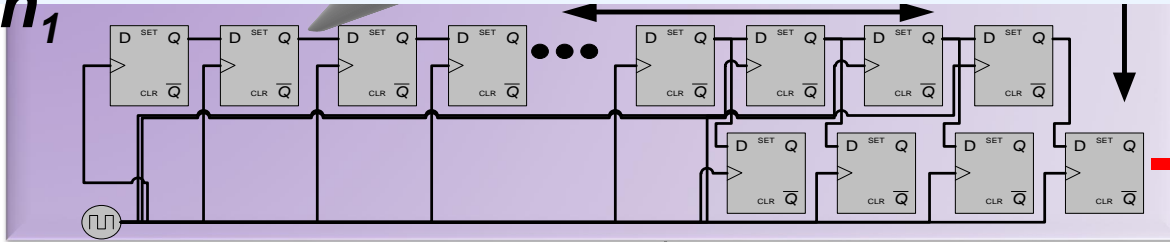
Windowed Shift Registers (WSRs): Each DUT Contains 4 WSR Chains

Chain₀



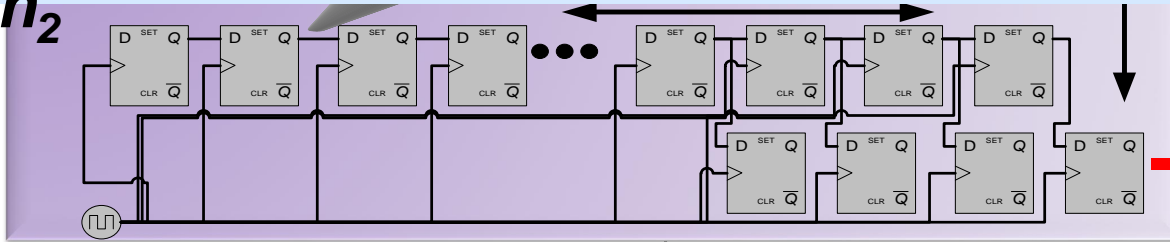
**4-bit
Window**

Chain₁



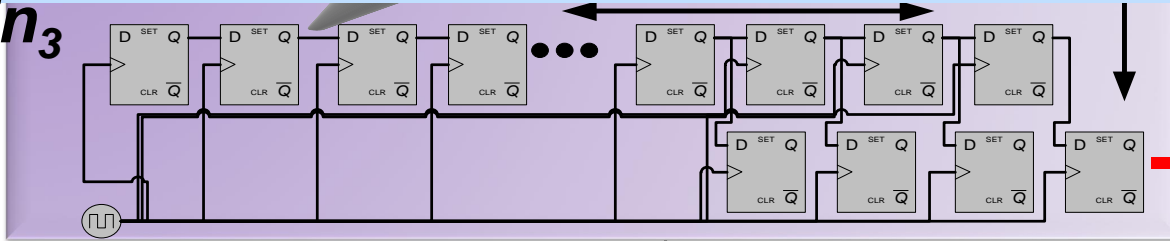
**4-bit
Window**

Chain₂



**4-bit
Window**

Chain₃



**4-bit
Window**

Tester

Microsemi RTG4 Clock Conditioning Circuit (CCC)

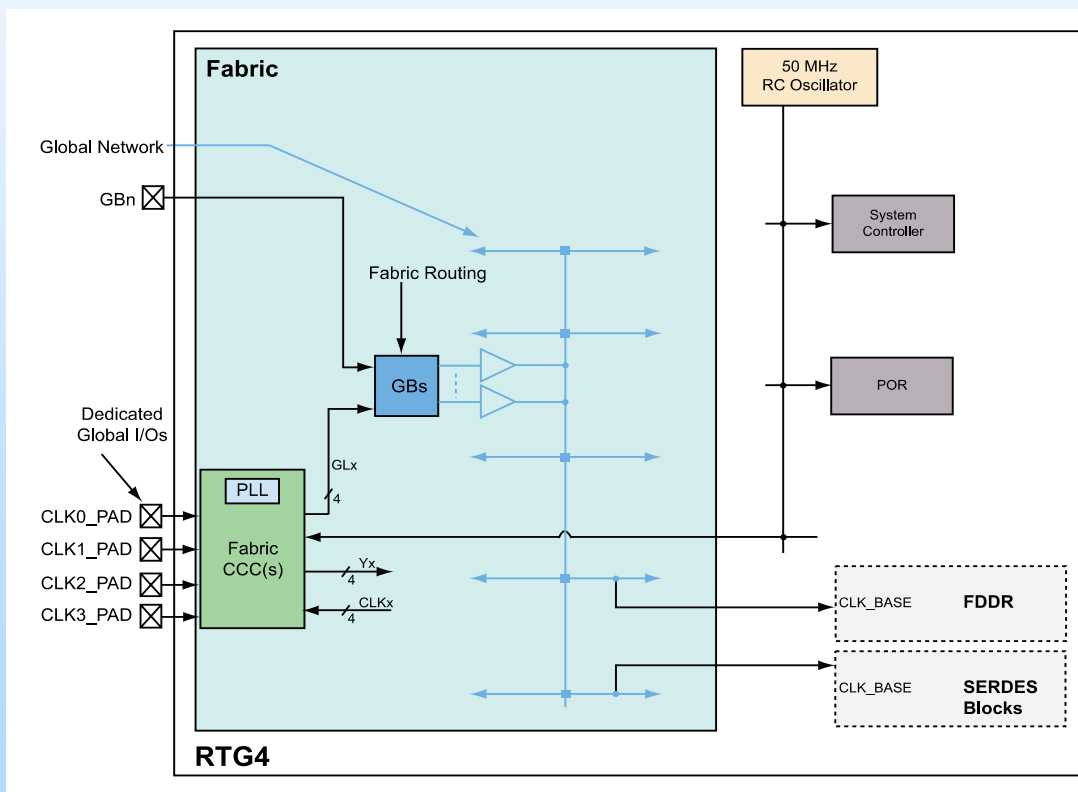


FDDR: Double Data Rate Interface Control;
SERDES: Serial-De-serializer;
POR: Power on reset;
PLL: Phase locked loop;
GBn: global network;
DGBIO: dedicated global I/O pad.

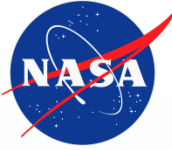
- **CLKBUF:** Hardened global route. Input can only be a DGBIO pad.
- **CLKINT:** Hardened global route. Input can come from fabric or any input.

Figure is Courtesy of Microsemi Corporation.

- **User can connect:**
 - From DGBIO pad to CLKINT,
 - FROM DGBIO pad to CCC-PLL to CLKINT,
 - From DGBIO pad to CLKBUF,
 - From normal input to CLKINT,
 - From normal input to CCC-PLL to CLKINT.

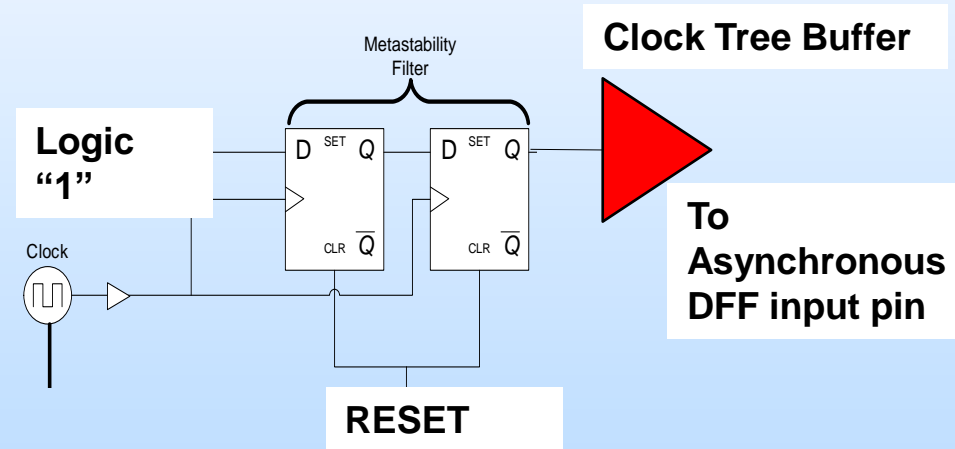


Asynchronous Assert Synchronous De-Assert Resets (AASD)



- AASD is the traditional method of reset implementation in NASA driven systems.
- This is a requirement for the protection of a mission in case of loss-of-clock.
- Synchronization is performed prior to clock tree connection.

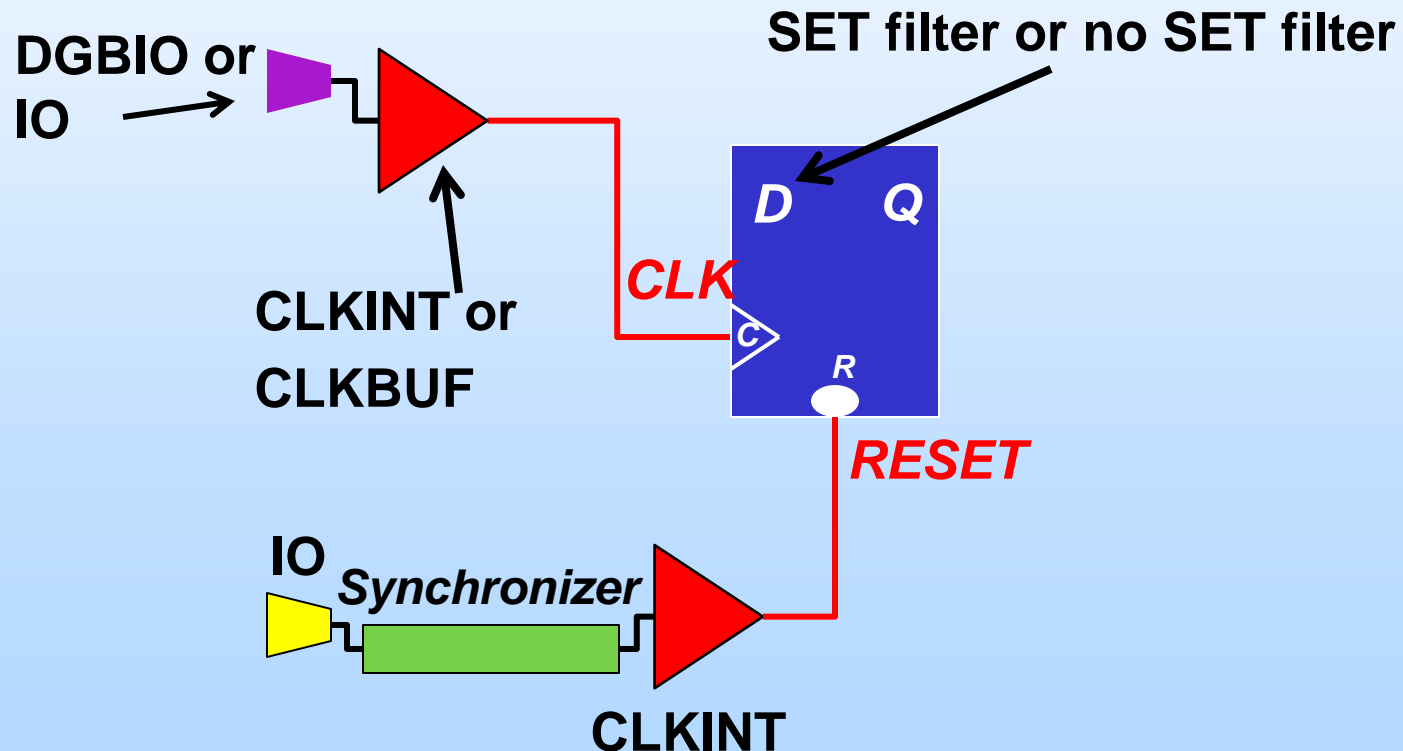
- The AASD global reset is connected to the asynchronous pin of each DFF, however, it is synchronized to the clock and is hence synchronous.



- Rev B tests implemented pure AASD via asynchronous reset tree connections to DFFs.
- AASD was not used in Rev C designs. Rev C designs use a pure synchronous reset.

List of WSR Implementations: Design Variations on the Clock Path

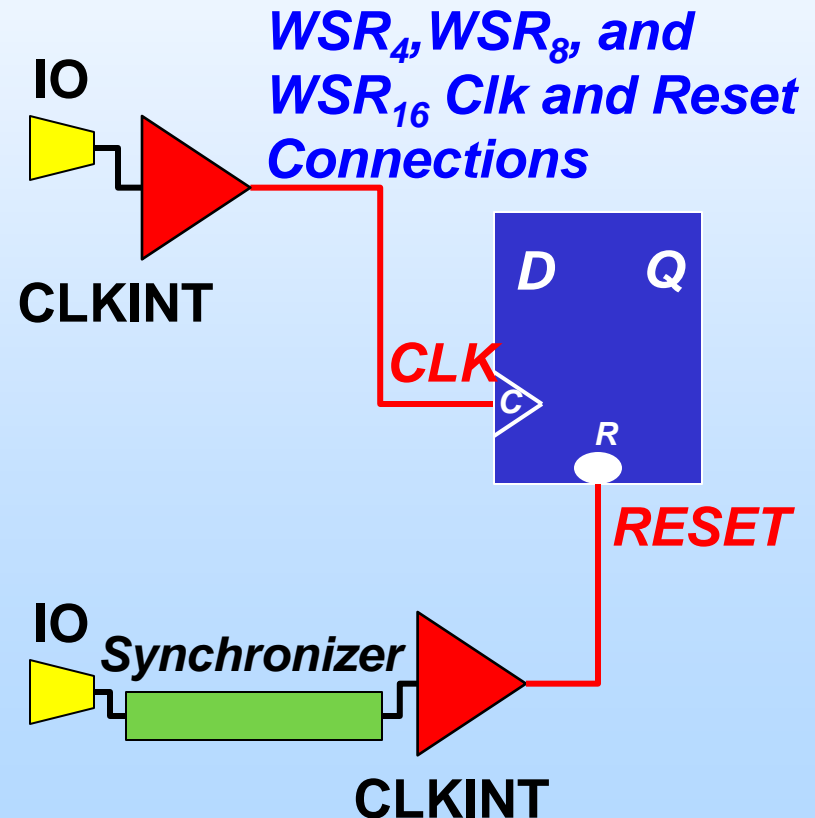
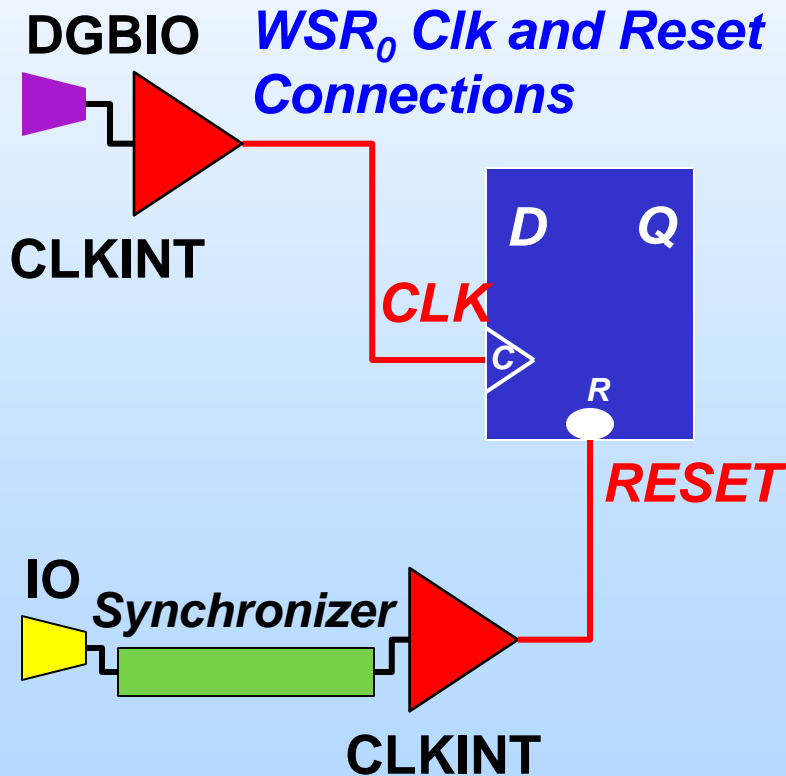
- Clock input to the DUT is either a dedicated clock I/O (DGBIO) or a normal I/O.
- All clocks are placed on a clock tree. The clock tree is either a CLKINT or a CLKBUF.
- All DFF data inputs are either in a normal state or contain an SET filter.



List of WSR Implementations:

Design A: 4 clk 4 rst

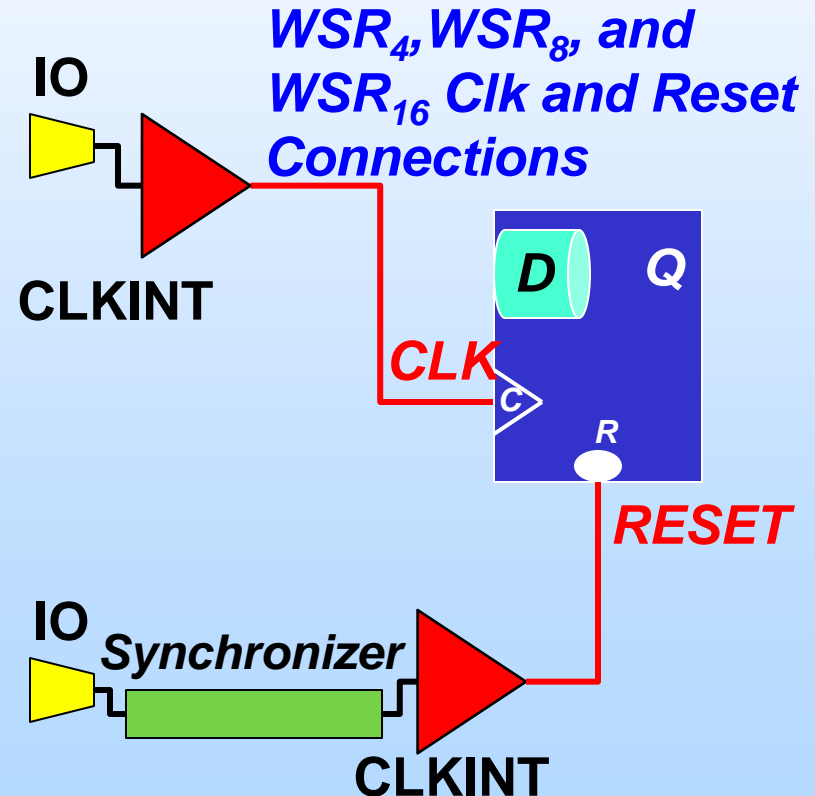
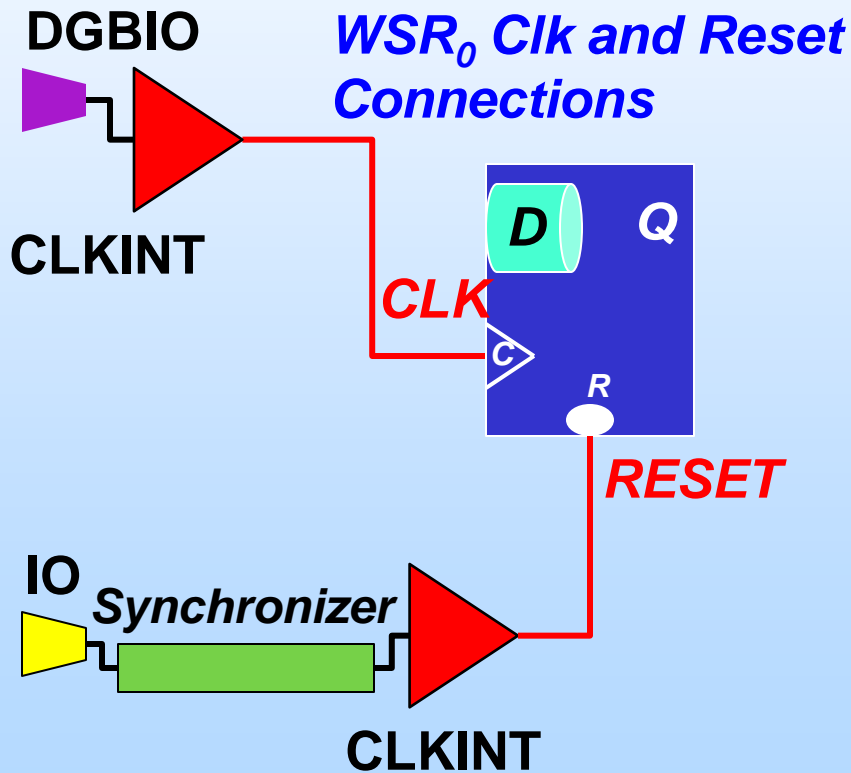
- Design has WSR_0 , WSR_4 , WSR_8 , WSR_{16} with 800 stages each.
- All clocks are connected to **CLKINT**. Only WSR_0 has a DGBIO.
- Each WSR chain has it's own synchronized reset.
- Rev B used a mixture of AASD and pure synchronous resets.
- Rev C used only pure synchronous resets



List of WSR Implementations:

Design B: 4 clk 4 rst FILTER

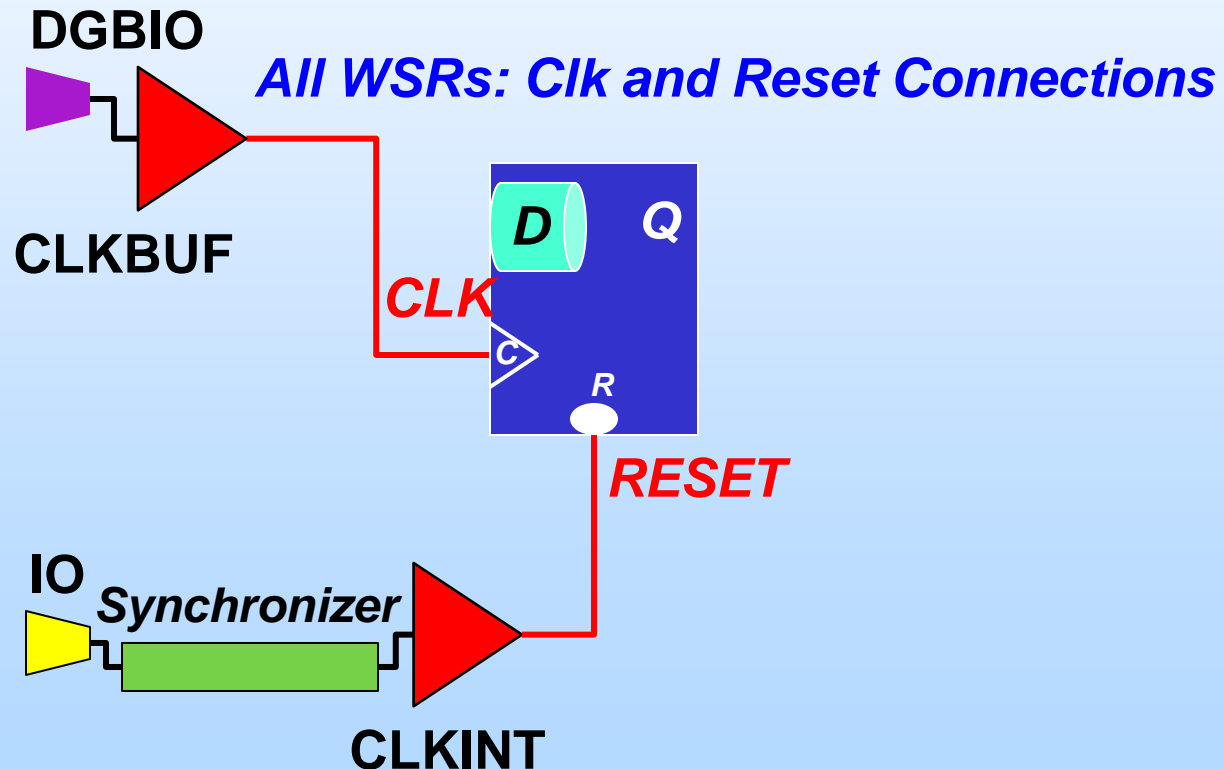
- Design has WSR_0 , WSR_4 , WSR_8 , WSR_{16} with 800 stages each.
- All clocks are connected to **CLKINT**. Only WSR_0 has a DGBIO.
- Each WSR chain has it's own synchronized AASD reset.
- **SET Filter is active** on every DFF in all WSR chains.
- Only implemented in Rev C with synchronous resets.



List of WSR Implementations:

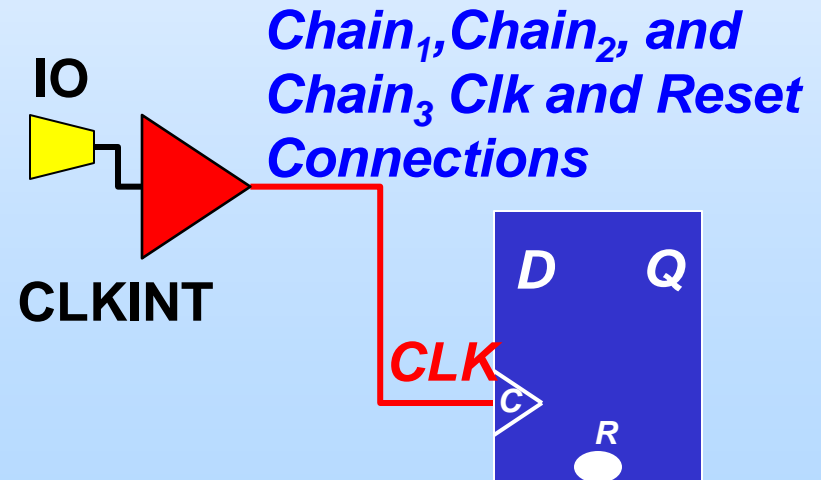
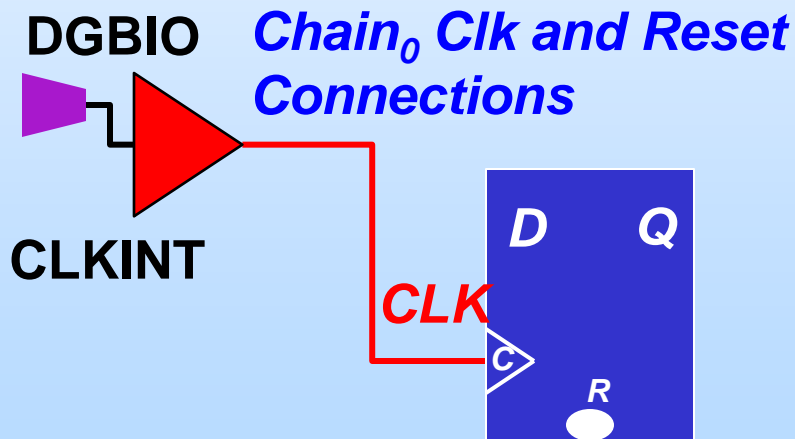
Design C: 4 clk 4 rst Direct CLKBUF

- Design has WSR_0 , WSR_4 , WSR_8 , WSR_{16} with 800 stages each.
- All clocks are connected to **CLKBUF**. All WSR chains have a DGBIO.
- Each WSR chain has it's own synchronized AASD reset.
- **SET Filter is active** on every DFF in all WSR chains.
- Only implemented in Rev C with synchronous resets.



List of WSR Implementations: Design D: Large shift register

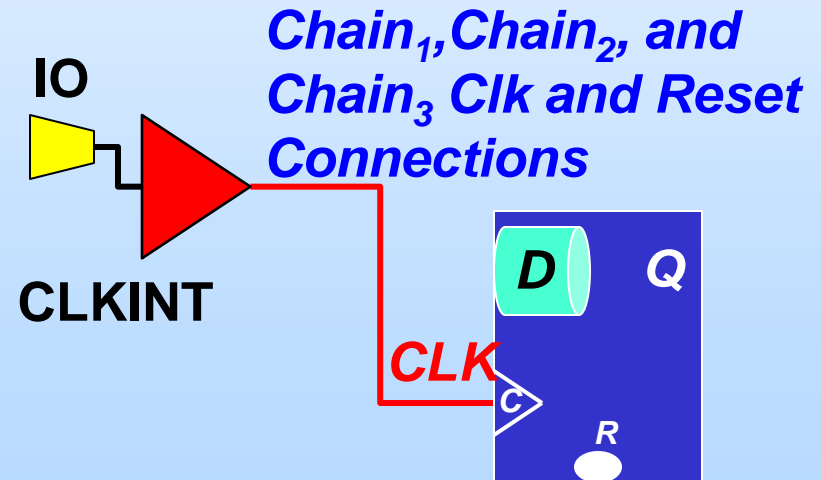
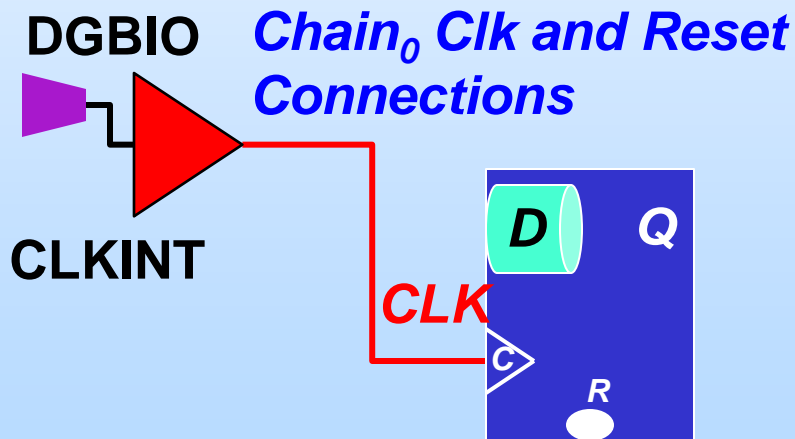
- 20,000 stage WSRs.
- DUT has 4 chains of WSR₀ (i.e., no inverters between DFF stages): Chain₀, Chain₁, Chain₂, Chain₃.
- All clocks are connected to **CLKINT**. Only Chain₀ has a DGBIO.
- No resets are used.



List of WSR Implementations:

Design E: Large shift register FILTER

- 20,000 stage WSRs.
- DUT has 4 chains of WSR₀ (i.e., no inverters between DFF stages): Chain₀, Chain₁, Chain₂, Chain₃.
- All clocks are connected to **CLKINT**. Only Chain₀ has a DGBIO.
- No resets are used.
- **SET Filter is active on every DFF in all WSR chains.**

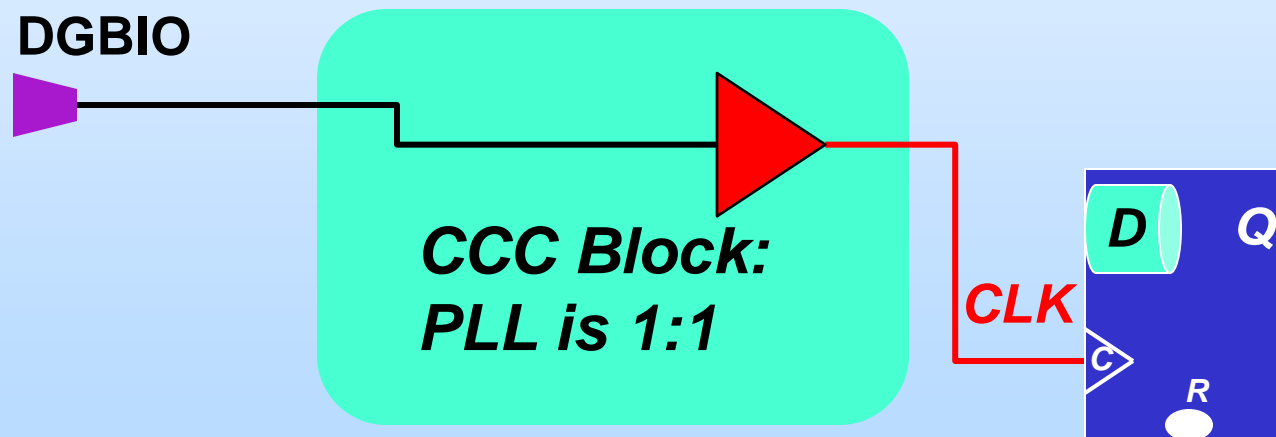


List of WSR Implementations:

Design F: Large shift register CCC

- 20,000 stage WSRs.
- DUT has 4 chains of WSR_0 (i.e., no inverters between DFF stages): $Chain_0$, $Chain_1$, $Chain_2$, $Chain_3$.
- All clocks are connected to output of the CCC block.
- All clock inputs are directly connected to a DGBIO.
- No resets are used.
- **SET Filter is active on every DFF in all WSR chains.**

All Chains: Clk and Reset Connections



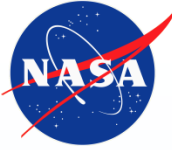


Summary of WSR Designs Under Test

Design	Design Name	CLK I/O Pin	Clock Buffer	Reset	Number of Stages	SET Filter
A	4 CLK 4 RST	WSR ₀ :DGBIO Others: I/O	All CLKINT	All CLKINT	800	OFF
B	4 CLK 4 RSTFILTER	WSR ₀ :DGBIO Others: I/O	All CLKINT	All CLKINT	800	ON
C	4 CLK 4 RST Direct CLKBUF	All DGBIO	All CLKBUF	All CLKINT	800	ON
D	Large Shift Register	Chain ₀ :DGBIO Others: I/O	All CLKINT	None	20,000	OFF
E	Large Shift Register FILTER	Chain ₀ :DGBIO Others: I/O	All CLKINT	None	20,000	ON
F	Large Shift Register CCC	All DGBIO	All Through CCC	None	20,000	ON

Designs D and E are large versions of A and B – implemented with only WSR₀s for statistics.

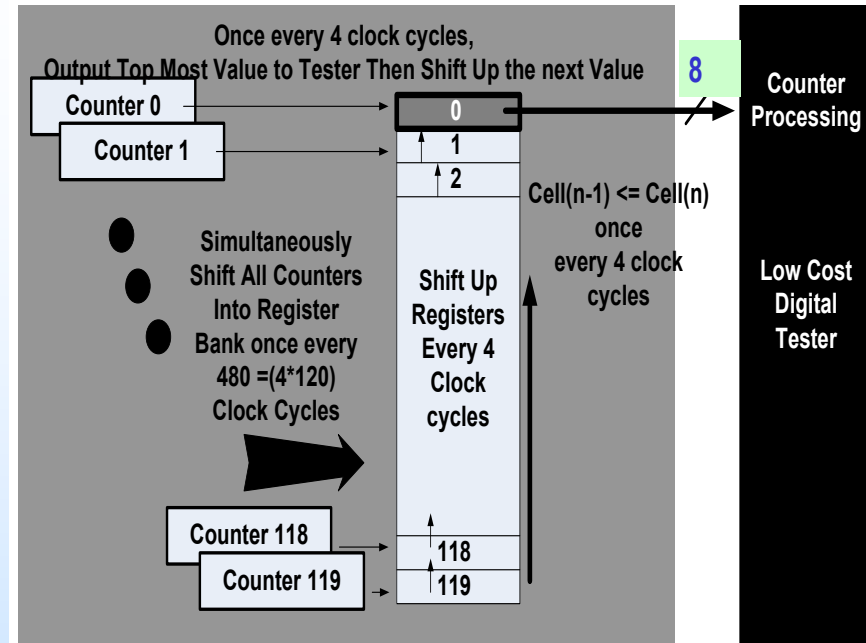
WSRs: Frequency of Operation and Data Patterns



- **Halt Operation:**
 - **Data patterns: checkerboard, all 1's, all 0's.**
 - **Registers are loaded with a data pattern while beam is turned off. Beam is turned on while clocks are static (however, registers are still enabled). Beam is turned off and the tester reads out registers.**
 - **Only performed on shift register test structures.**
- **Dynamic Operation:**
 - **Data patterns: checkerboard, all 1's, all 0's.**
 - **Shift register frequency of operation will be varied from 2KHz to 160MHz.**
 - **Data pattern and frequency are selected and operation is active prior to turning on beam. Beam is turned on; SEUs are collected real-time; and SEU data is time-stamped.**

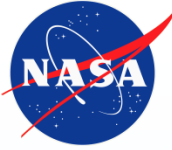
Counter Arrays

- DUT contains two sets of the following:
 - 200 8-bit counters
 - 200 8-bit snapshot registers
- All counters and snapshot registers are connected to the same clock tree and RESET.
- The clock tree is fed by the CLK input from the LCDT.
- DUT CLK is connected to a DGBIO and a CLKBUF.
- The LCDT sends a clock and a reset to the DUT. The controls are set by the user



Counters can still operate after most SEUs. However after an SEU occurs, the tester must recalculate a new expected value for the affected counter.

2 sets of counter arrays are tested simultaneously



Microsemi RTG4 Test Conditions

- **Temperature range: Room temperature**
- **Facility: Texas A&M.**
- **Performed December 2015, March 2016, and May 2016.**
- **NEPP Low Cost Digital Tester (LCDT) and custom DUT board..**
- **LET: 1.8 MeVcm²/mg to 20.6 MeVcm²/mg.**

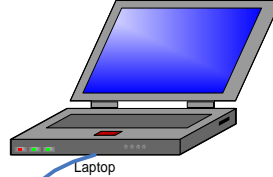
Block Diagram of RTG4 Test Environment



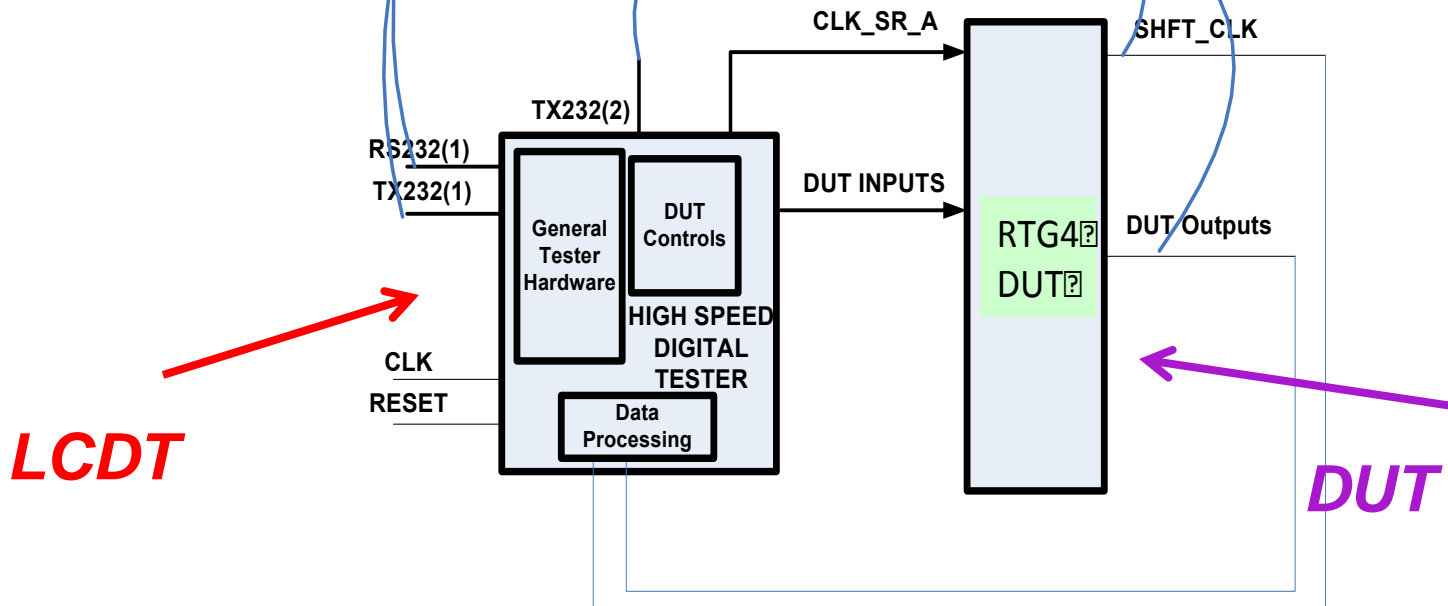
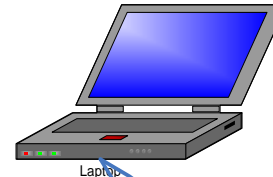
Labview GUI Connected to Memory Processing in HSDT. Commands are also sent (and echoed) to the HSDT through this RS232 interface



Labview GUI connected to WSR or Counter Processing



Logic Analyzer Connected to WSR or Counter Outputs



Characterizing Single Event Upsets (SEUs): Accelerated Radiation Testing and SEU Cross Sections

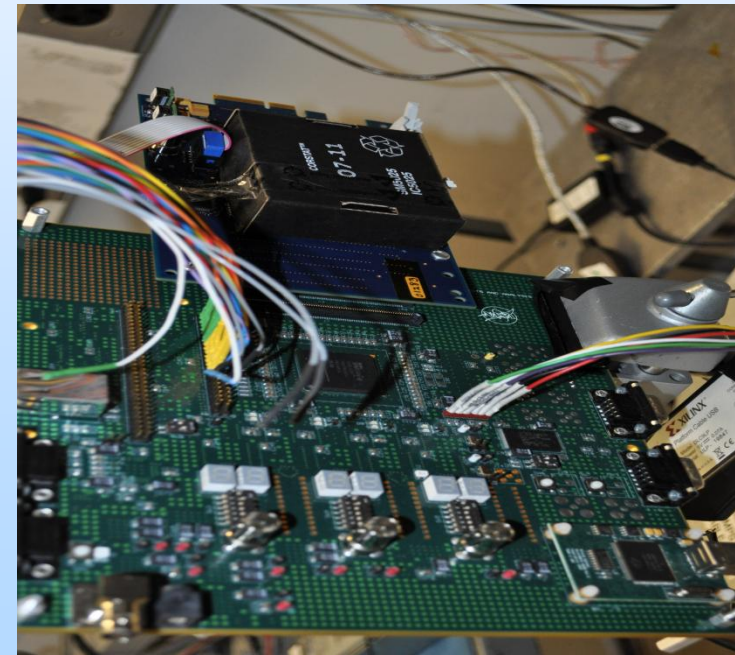
SEU Cross Sections (σ_{seu}) characterize how many upsets will occur based on the number of ionizing particles to which the device is exposed.

$$\sigma_{seu} = \frac{\#errors}{fluence}$$

Terminology:

- Flux: Particles/(sec-cm²)
- Fluence: Particles/cm²

σ_{seu} is calculated at several linear energy transfer (LET) values (particle spectrum)

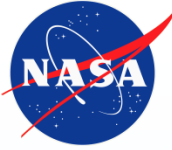




Accelerated Test Results



Configuration



Configuration Re-programmability

- **During this test campaign, tests were only performed up to an LET of 20.6MeVcm²/mg.**
- **Higher LETs will be used during future testing.**
- **No re-programmability failures were observed up to an LET of 20.6MeVcm²/mg when within particle dose limits.**



WSRs



Halt Accelerated Tests

- **LET=20.6 MeV*cm²/mg the test fluence was 1.0e⁷ particles/cm²; and LET=5.0 MeV*cm²/mg the test fluence was 2.0e⁷ particles/cm².**
- **Designs are held in a static state because the clock is suspended.**
- **Upsets are expected to come from a clock tree, reset tree, or an internal DFF SEU.**
 - **Clock SET can capture data that is sitting at a DFF input pin.**
 - **Upsets are not expected to come from the reset tree with Rev C tests.**
 - **Why not Rev C reset SETs? All resets are placed on the synchronous tree. It would take a clock SET and a reset SET for a reset SET to be captured.**
 - **With AASD designs (Rev B), upsets can originate in the reset tree.**

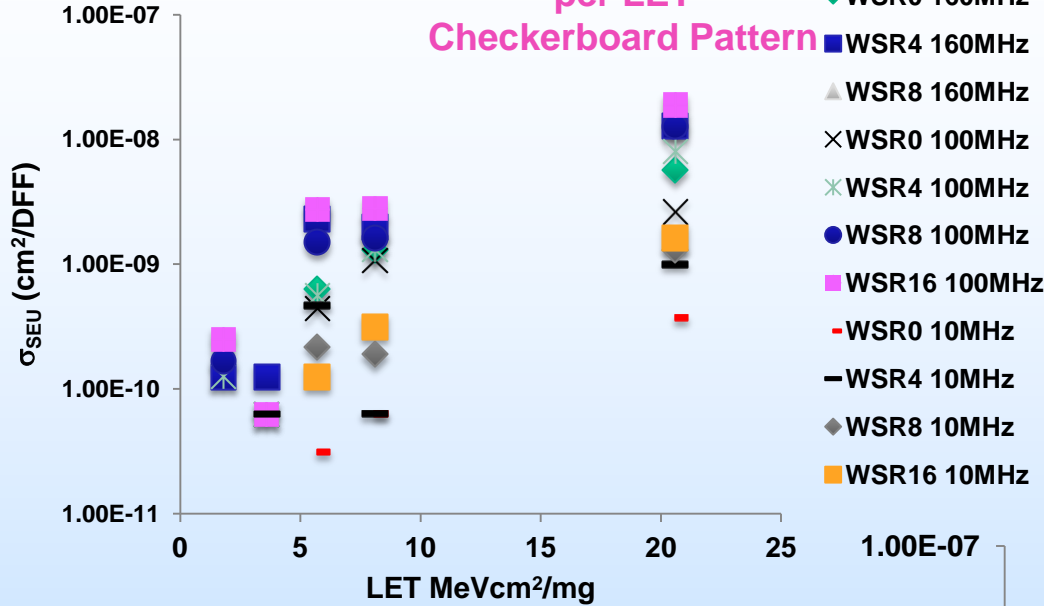


Halt Accelerated Tests: DFFs

- **No internal DFF upsets were observed.**
- **No SEUs were observed on any of the chains that were connected to a DGBIO and a CLKBUF pair.**
- **SET filters did not make a difference.**
 - This is as expected because data-path SETs cannot be captured (DFFs are not clocked).
- **All chains of WSRs:**
 - No SEUs were observed with All 1's and All 0's tests. This is as expected because, when a clock glitches, the same data value is captured.
 - SEUs were not observed until an $LET=20.6 \text{ MeV}^*\text{cm}^2/\text{mg}$ for all 4 clk 4 rst design variations.
 - SEUs were observed at $LET = 5.7 \text{ MeV}^*\text{cm}^2/\text{mg}$ for Long Shift Reg.

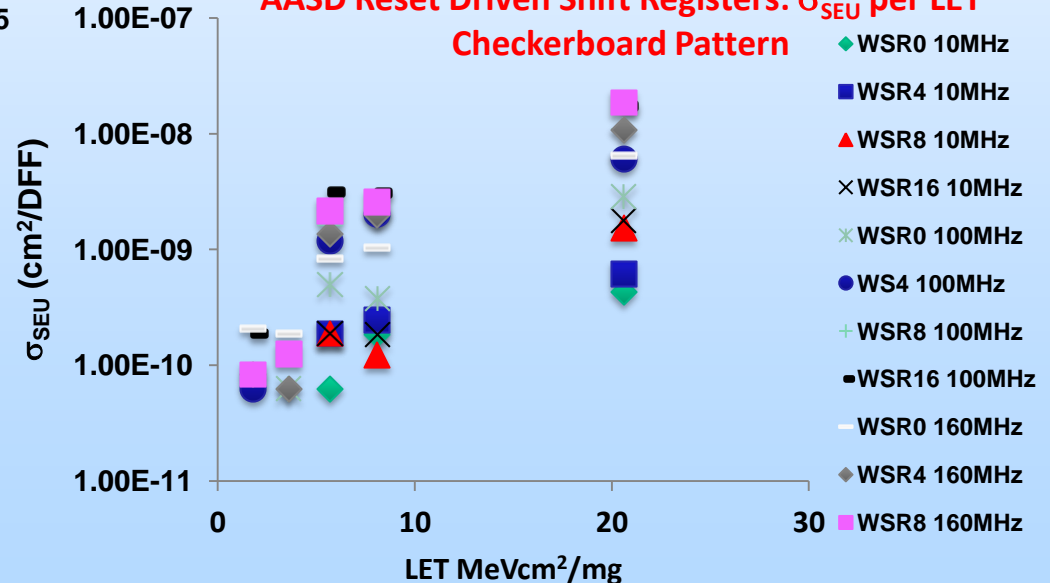
Rev B Reset Evaluation: 4 clk 4 rst

Synchronous Reset Driven Shift Registers: σ_{SEU} per LET
Checkerboard Pattern

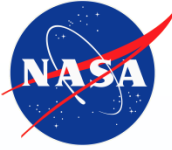


Synchronous versus AASD... Insignificant difference between SEU cross-sections.

AASD Reset Driven Shift Registers: σ_{SEU} per LET
Checkerboard Pattern

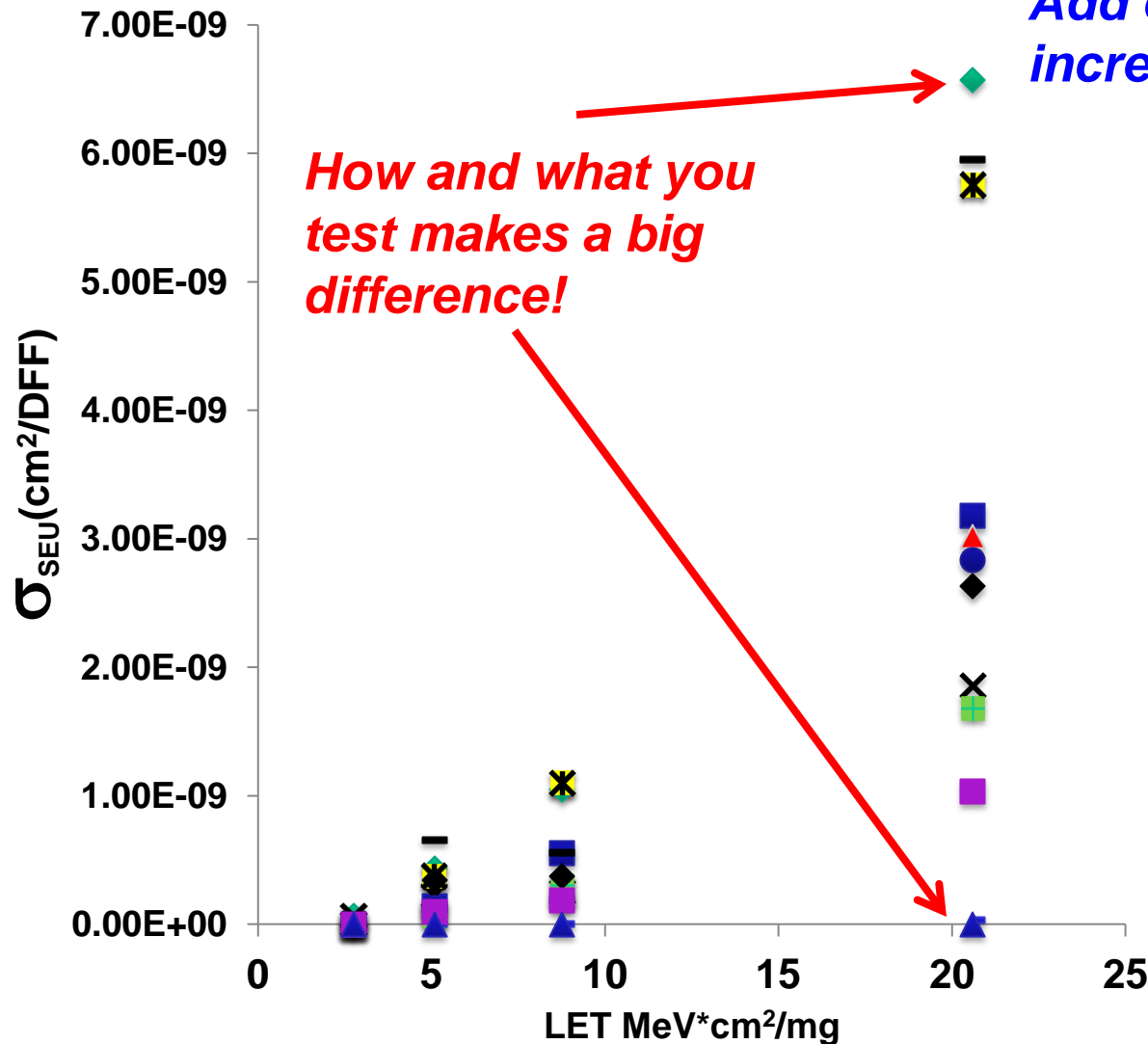


Both AASD and synchronous reset are on hardened clock trees.



Rev C: 4 CLK 4 RST FILTER versus LET at 100MHz

Add combinatorial logic, increase cross section.



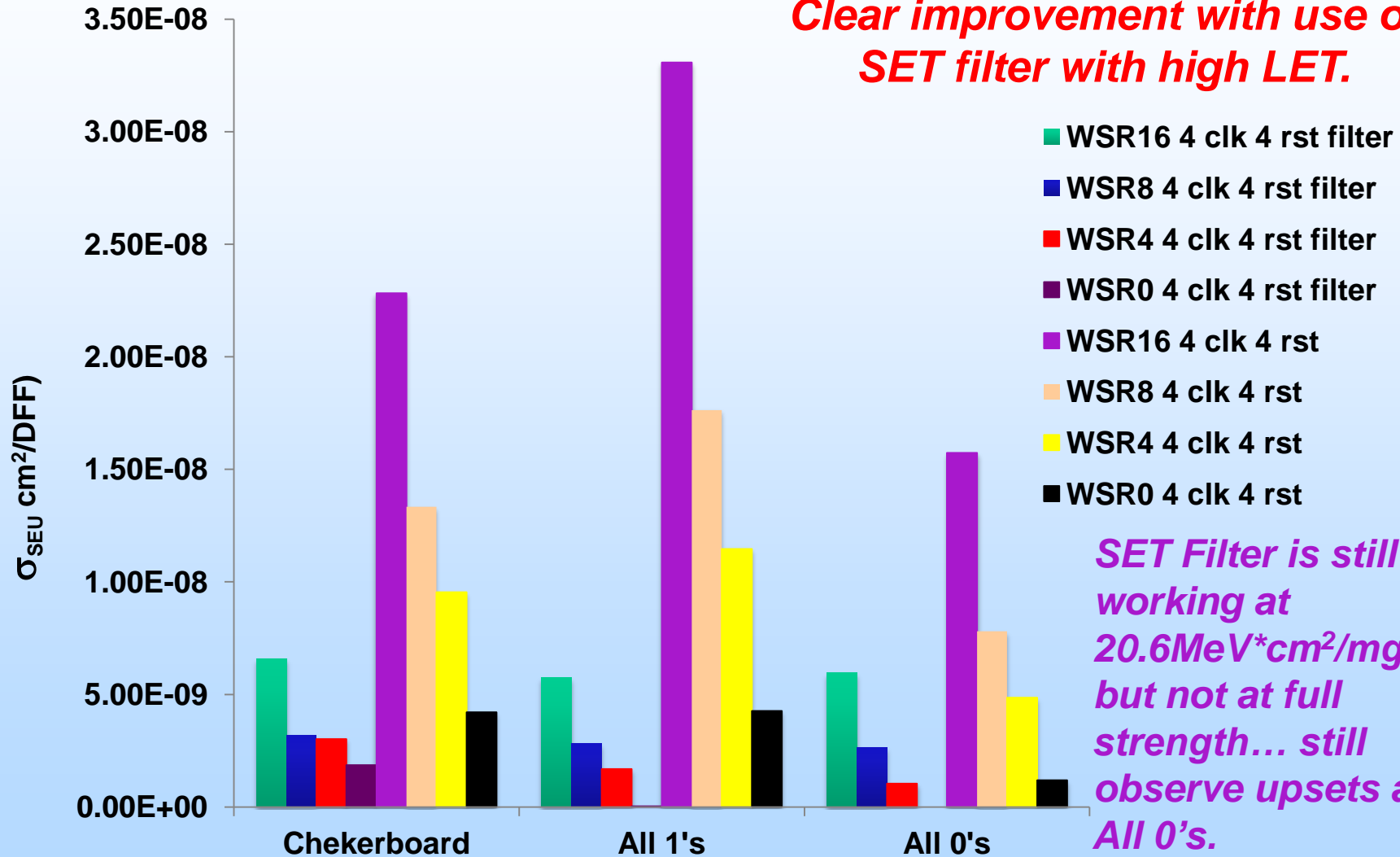
- ◆ WSR16 Checkerboard
- WSR8 Checkerboard
- ▲ WSR4 Checkerboard
- × WSR0 Checkerboard
- ✱ WSR16 All 1's
- WSR8 All 1's
- WSR4 All 1's
- WSR0 All 1's
- WSR16 All 0's
- ◆ WSR8 All 0's
- WSR4 All 0's
- ▲ WSR0 All 0's



Comparing WSR Chains:

4 clk 4 rst with Filter and 4 clk 4 rst ...100MHz with
LET = 20.6MeVcm²/mg

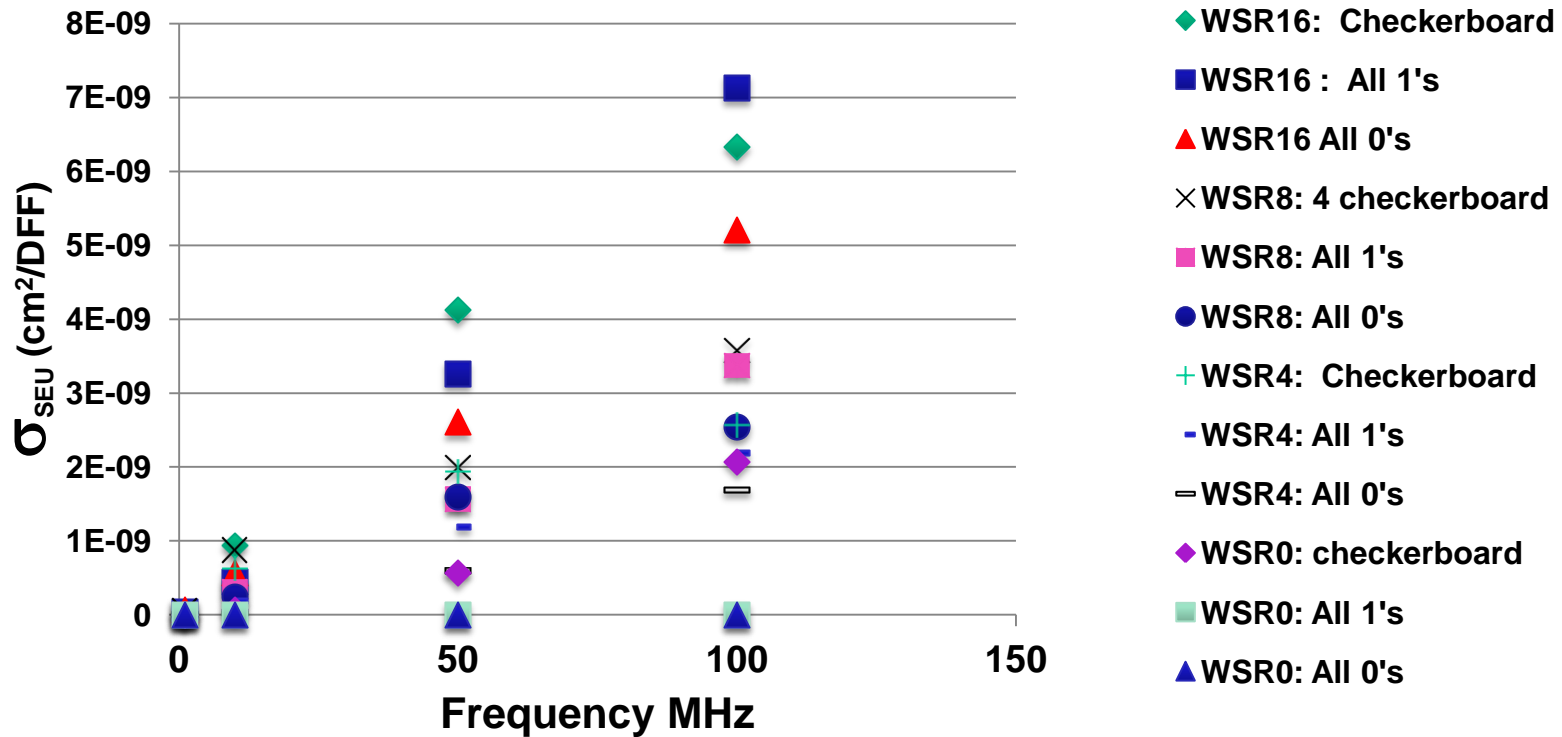
*Clear improvement with use of
SET filter with high LET.*



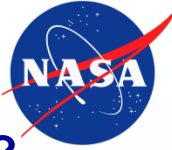
4 Clk 4 rst Direct CLKBUF SEU Cross Sections versus Frequency at LET = 20.6 MeVcm²/mg



Data across LET was not able to be taken because of limited test time with this design.

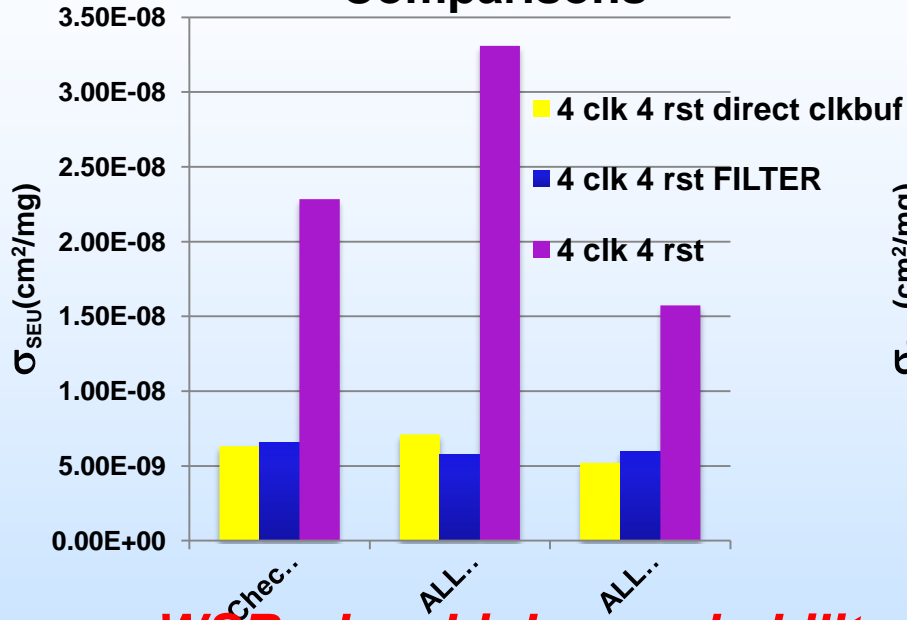


- DFFs are hardened well. SEUs are coming from captured SETs in the data-path.
 - As frequency increases, SEU cross-sections increase.
 - As the number of CL gates increase, SEU cross-sections increase.
 - Upsets occur with All 1's and All 0's. (Can't be from a clock – must be data-path).
- **SET filter works but is not at full strength at LET= 20.6MeV*cm²/mg.**

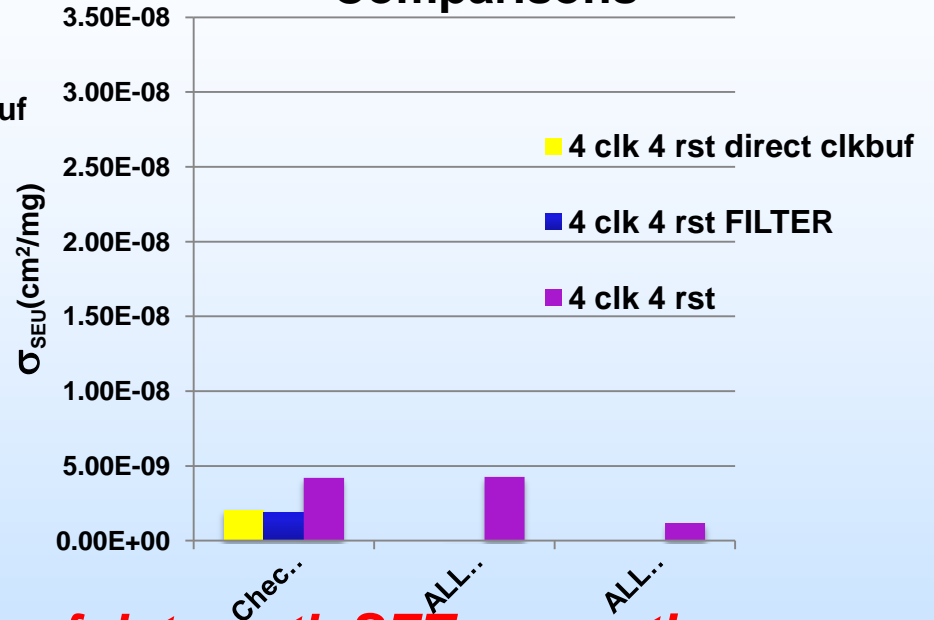


Comparing 4 clk 4 rst DUT Variations: How much Better Is A Direct Connection to CLKBUF and/or A SET Filter?

WSR₁₆ at 100MHz LET=20.6 Comparisons



WSR₀ at 100MHz LET=20.6 Comparisons



WSR₁₆ has higher probability of data-path SET generation.

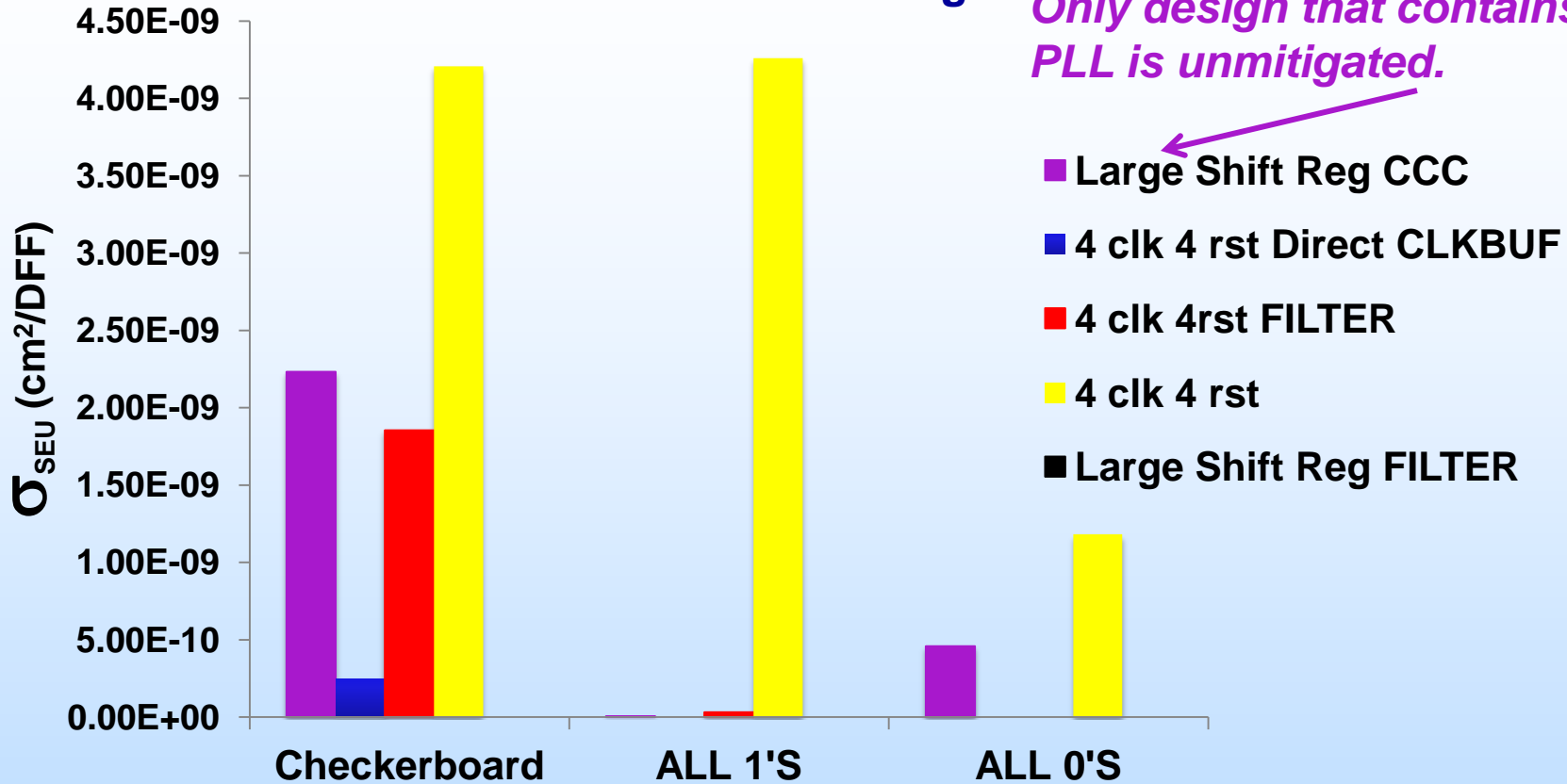
WSR ₁₆ Pattern	Direct/fil ter	Direct/n o filter
Checker	0.96	0.28
All 1's	1.24	0.26
All 0's	0.88	0.33

Tables represent Ratios of SEU cross sections.

WSR ₀ Pattern	Direct/fil ter	Direct/n o filter
Checker	1.1	0.47
All 1's	1.0	0.007
All 0's	1.0	0.025

Introducing Large WSRs (1):

Comparison of WSR_0 SEU Cross Sections at 100MHz at LET = 20MeV*cm²/mg



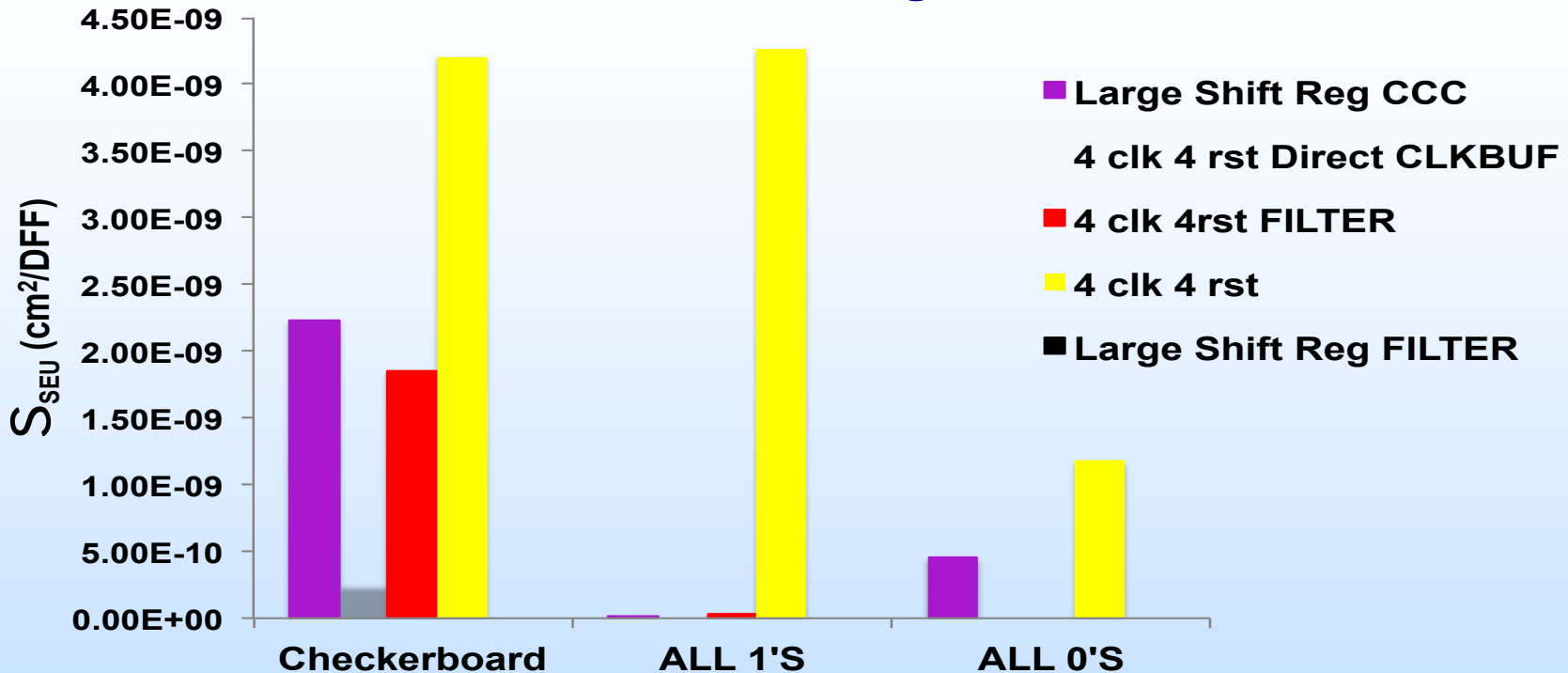
Only design that contains PLL. PLL is unmitigated.

- Large Shift Reg CCC
- 4 clk 4 rst Direct CLKBUF
- 4 clk 4rst FILTER
- 4 clk 4 rst
- Large Shift Reg FILTER

- Can only compare WSR_0 chains because Large Shift Reg only contains WSR_0 s.
- As expected 4 clk 4 rst has the worst SEU performance. It is the only design in this graph with no SET filters.
- 4 clk 4 rst Direct CLKBUF has the best SEU performance. There is a direct connect from the DGBIO to the CLKBUF.

Introducing Large WSRs (2):

Comparison of WSR_0 SEU Cross Sections at 100MHz at LET = $20\text{MeV}\cdot\text{cm}^2/\text{mg}$

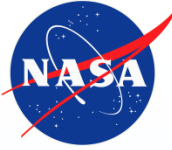


- **Checkerboard pattern:** all designs have observable SEU cross-sections.
- **All 1's:** 4 clk 4 rst Direct CLKBUF and Large Shift Reg FILTER have negligible SEU cross-sections.
- **All 0's:** Only 4 clk 4 rst (no filter) and Large Shift Reg CCC (PLL) have observable SEU cross-sections.

Using the PLL reduces the effectiveness of using an SET filter.

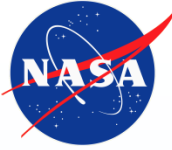
WSR Accelerated Radiation Test Data

Observations



- SEUs can originate in clocks trees, reset trees (not with long shift-regs), and data paths.
- In Rev C, resets are connected via the synchronous tree and reset SETs would require a clock edge capture.
- WSR_0 s:
 - When only analyzing all 1's or all 0's, clock SEUs are masked.
 - With WSR_0 , no SEUs were observed on chains with filters.
 - Only the designs with no filter have observable SEU cross-sections. In addition, there is less probability of SET capture because of little to no CL in the data-path.
 - Adding the analysis of checkerboard, all WSR_0 s have observable SEUs.
 - This suggests, for WSR_0 , that most of the checkerboard upsets are coming from the clock or reset tree (global routes).
- Why does an SET filter make a difference with WSR_0 's?
 - SEUs should not come from the data-path because there are no combinatorial logic between DFF stages.
 - There are probably some hidden connection buffers in the shift register chains.

WSR Accelerated Radiation Test Data Observations



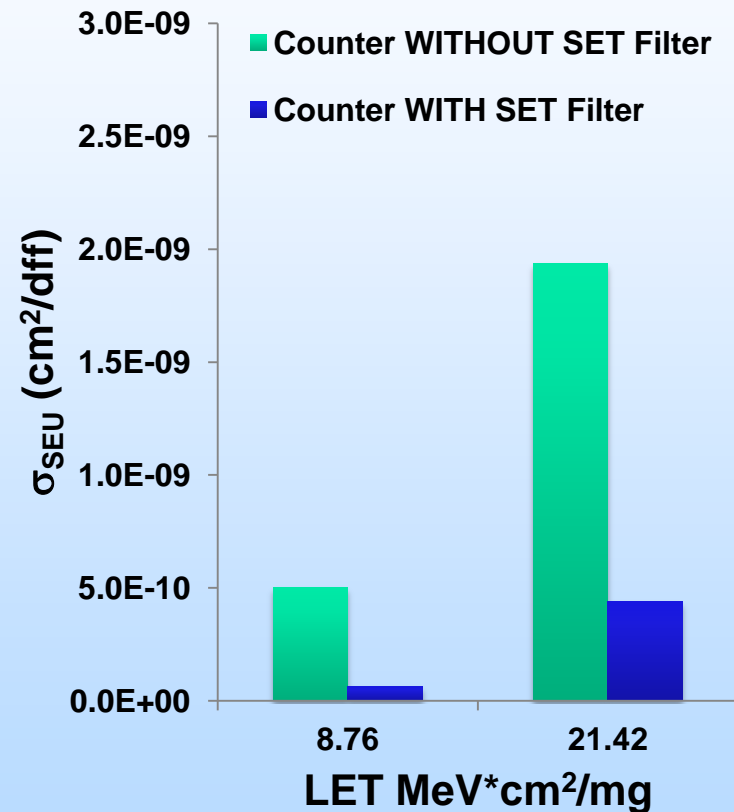
- In some tests, WSR input pattern of All 1's had greater SEU cross sections than WSR input pattern of checkerboard.
 - This only occurred with designs that used resets. Most likely the reset was the cause.
 - **The use of resets in a synchronous design is imperative. This observation must not change the rules for reset implementation.**
- Connecting from a DGBIO to a CLKBUF versus a normal I/O to a CLKINT did not provide significant improvement in SEU cross sections.
- Connecting from a DGBIO to a CCC-PLL into a CLKINT did not improve SEU cross sections. It actually had higher SEU cross sections.
 - However, the performance is most likely acceptable because there is a PLL in the path.



Counters

Rev C Counter Arrays

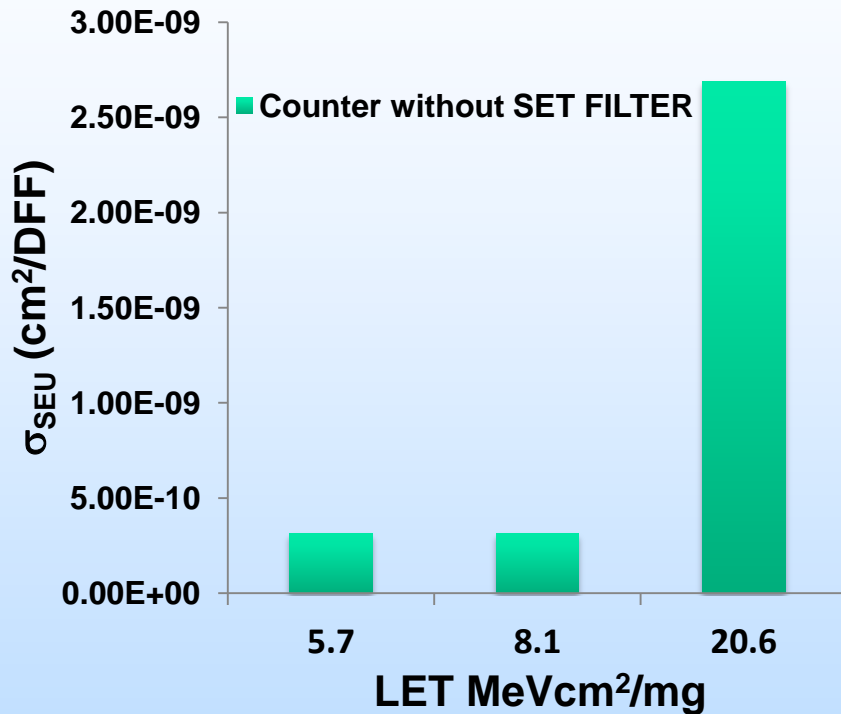
Rev C Counter Arrays Single Bit σ_{SEU} : without SET Filter versus with SET Filter at 50MHz



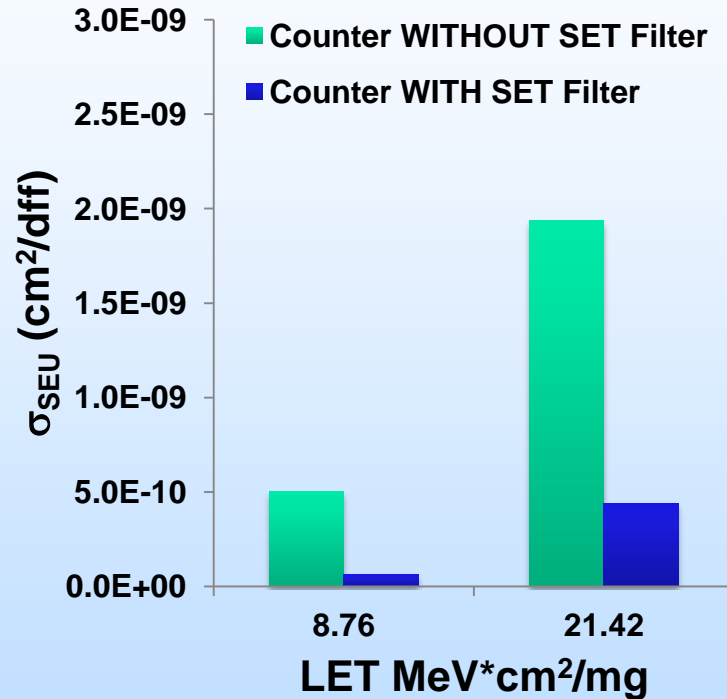
- Counter SEU cross-sections are lower than the corresponding (i.e., with filter or without) WSRs with checkerboard.
 - Only counter-bits that change at the frequency of a checkerboard are bit-0 of each counter.
 - As the bit-number of each counter increases, the bit frequency is decreased by a factor of 2.
- Once again, the SET filter makes a significant difference.
- Counters were tested at 1MHz, 5MHz, 10MHz, and 50MHz.
- Upsets were not observed below 50MHz below an LET of 20MeV*cm²/mg. Additional testing is required.

Rev C versus Rev B Counter Arrays

Rev B Counter Array Single Bit σ_{SEU} s at 50MHz

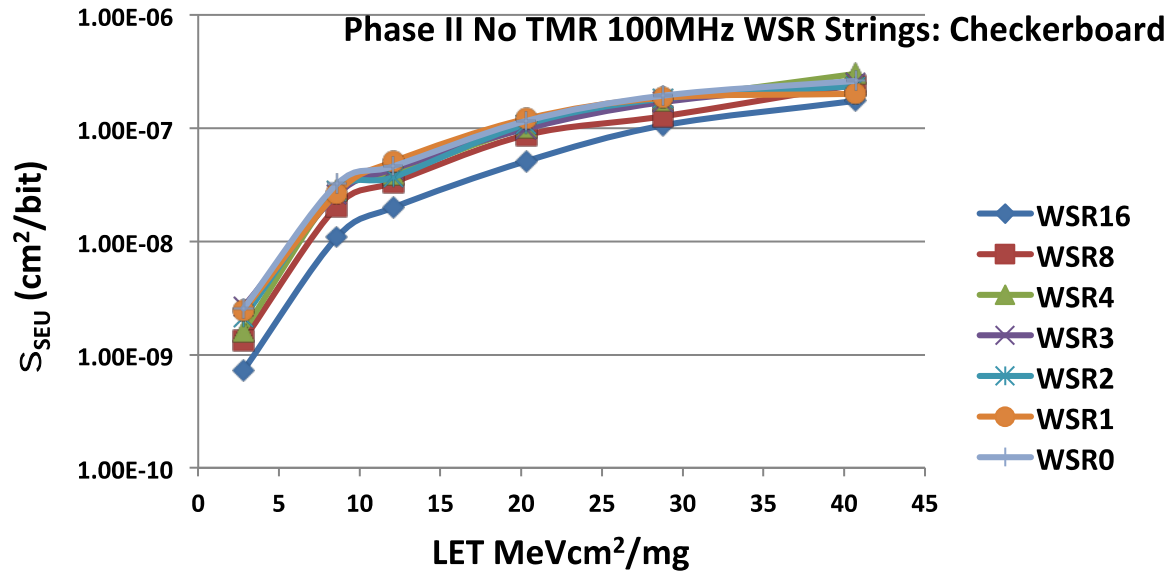
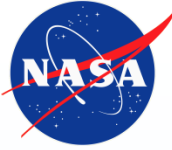


Rev C Counter Arrays Single Bit σ_{SEU} s: without SET Filter versus with SET Filter at 50MHz

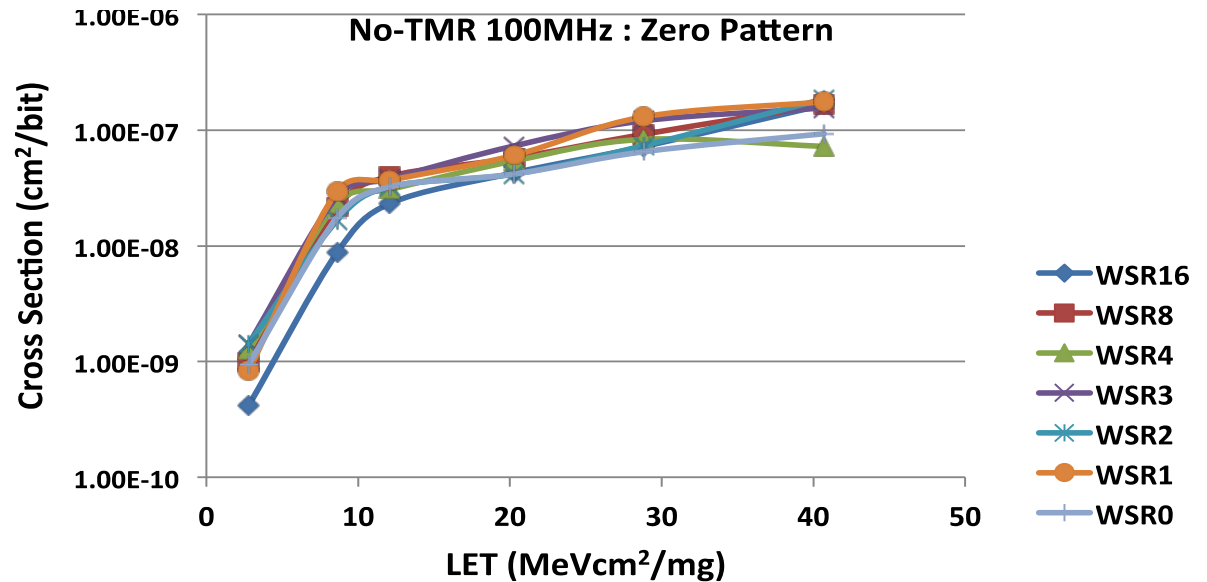


- Rev B counters did not contain SET filters.
- Rev B and Rev C counters with no SET filters have compatible cross-sections.
- Rev C cross-sections are slightly lower because of improvements from Microsemi.

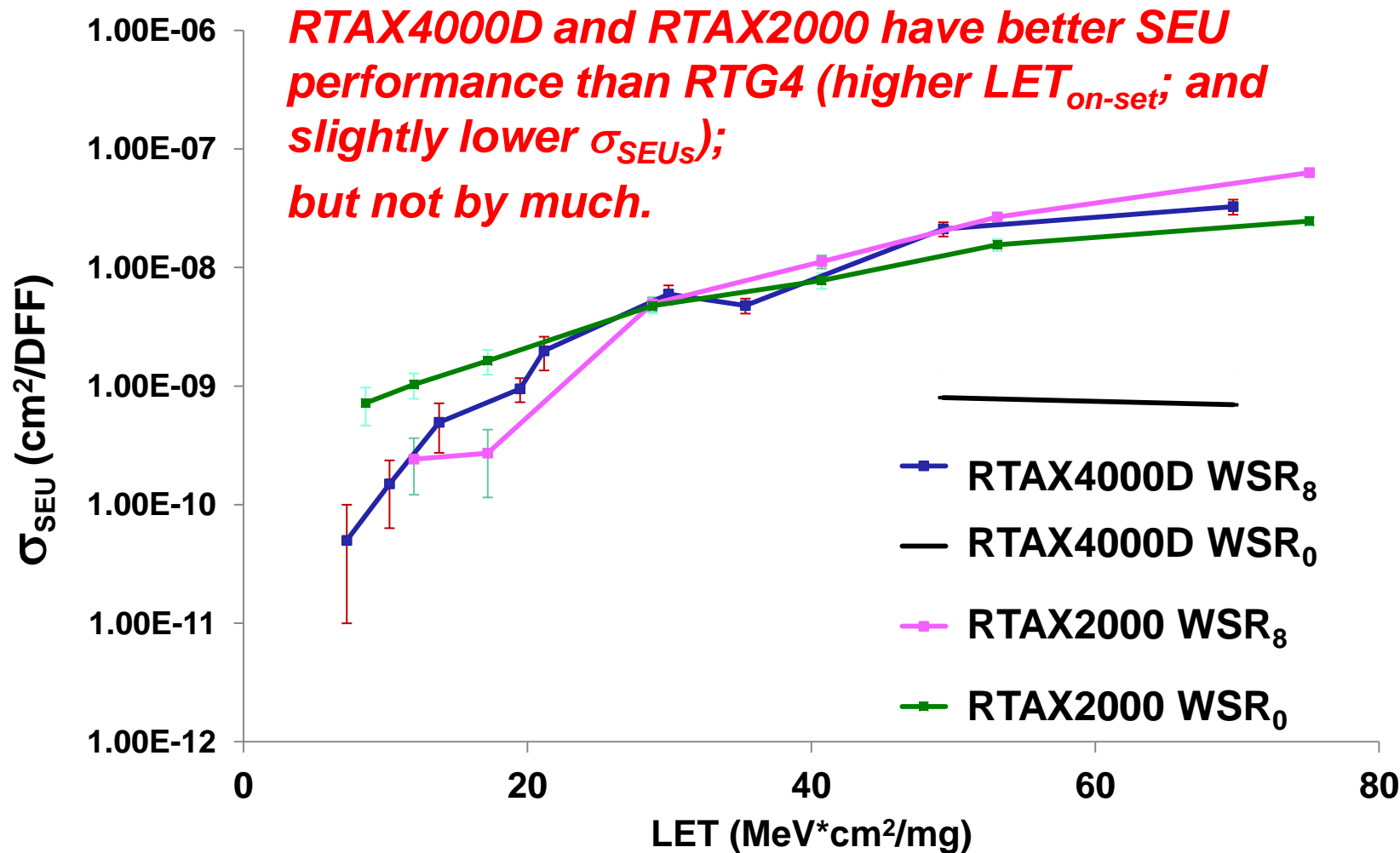
NEPP: ProASIC3 Accelerated Heavy-ion Test Results



RTG4 shows an improvement over ProASIC3 in functional data path.



RTAX4000D and RTAX2000 WSRs at 80MHz with Checkerboard Pattern





Future Work

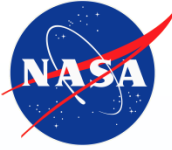
- **DUT Test structures:**
 - Additional counter array tests (will try for higher frequencies).
 - Embedded SRAM (LSRAM and μ SRAM).
 - I/O evaluation:
 - Multiprotocol 3.125Gbit SERDES.
 - Space wire interface block.
 - DDR controllers.
 - Embedded microprocessors.
 - Math logic blocks (DSP blocks).
 - Additional CCC block testing.
- **Multiple test structures will be implemented in a DUT and tested simultaneously.**
 - Saves time.
 - Reduces the number of devices needed for testing.
- **Preliminary Rev B test report is finished.**
- **Preliminary Rev C test report October 2016.**

CCC: Clock Conditioning Circuit

DSP: Digital signal processing

DDR: double data rate memory

SERDES: serial high speed interface



Acknowledgements

- *Some of this work has been sponsored by the NASA Electronic Parts and Packaging (NEPP) Program and the Defense Threat Reduction Agency (DTRA).*
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