Review of DC-DC Converters for Multi-terminal HVDC Transmission Networks

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Abstract: This paper presents a comprehensive review of high-power dc-dc converters for high-voltage direct current (HVDC) transmission systems, with emphasis on the most promising topologies from established and emerging dc-dc converters. Additionally, it highlights the key challenges of dc-dc converter scalability to HVDC applications, and narrows down the desired features for high-voltage dc-dc converters, considering both device and system perspectives. Attributes and limitations of each dc-dc converter considered in this study are explained in detail and supported by time-domain simulations. It is found that the front-to-front quasi two-level operated modular multilevel converter, transition arm modular converter and controlled transition bridge converter offer the best solutions for high-voltage dc-dc converters that do not compromise galvanic isolation and prevention of dc fault propagation within the dc network. Apart from dc fault response, the MMC dc auto transformer and the transformerless hybrid cascaded two-level converter offer the most efficient solutions for tapping and dc voltage matching of multi-terminal HVDC networks.

Key words: High-voltage dc-dc converter; modular multilevel converter; multi-terminal high-voltage dc networks; and prevention of dc faults propagation.

I. INTRODUCTION

For many decades researchers have recognised the possibilities multi-terminal high-voltage dc (HVDC) transmission networks can offer when compared to well-established high-voltage ac (HVAC) systems[1-15]. For the majority of this period, the difficulty of power reversal in complex multi-terminal networks based on line commutating converter high-voltage dc (LCC-HVDC) technology has prevented development of generic dc grids with seamless control over the power flow in any of its branches [16]. Also, the increased dependency of the LCC terminal on the ac network strength has caused significant concerns regarding ac voltage stability of relatively weak ac networks, especially when large power is being exchanged [8, 16-26]. The emergence of voltage source converter high-voltage dc (VSC-HVDC) in the early 1990s [10, 12, 27-46] that can reverse dc power without any difficulty (power reversal is achieved without the need to reverse the dc voltage) has reinvigorated research into generic multi-terminal HVDC networks. Recent consideration of offshore wind farms by many European countries with real possibilities of building offshore multi-terminal HVDC networks and inter-regional dc grids, has encouraged serious research and development effort from major HVDC manufacturers and academia [1, 8, 12, 43-45, 47-59]. These efforts include all technology chains which are necessary for practical realisation of multi-terminal HVDC networks, such as dc switchgear (dc circuit breakers and fast disconnectors) and high-voltage dc-dc converters [44, 47, 60-76]. Besides dc voltage matching, high-voltage dc-dc converters are expected to play a pivotal role of splitting a large dc grid into several protection zones (smaller dc networks, each capable of sustaining itself as an individual network or operating as part of a large network), thus preventing entire system collapse during a severe dc network fault. These dc-dc converters (also known as dc-transformers) are expected to provide galvanic isolation. The majority of the most promising dc-dc converters for HVDC applications known today are developed around the front-to-front (F2F) dual active bridge originally developed by De Doncker for low and medium-voltage applications [65, 77]. The topology is best suited for low and medium transformation ratios. These dc-dc converters deliberately use an intermediate ac link to make a dc fault on one side appears as a controllable ac overcurrent at the healthy side converter. Blocking the healthy converter will therefore be sufficient to isolate the faulty part.

These converters must therefore be seen as an enabling technology for a multi-terminal HVDC network as they minimise the number of dc circuit breakers, and allow dc grids to behave in a similar fashion as ac grids during dc network faults. Because it is not possible to cover all the dc-dc converters proposed in the literature for HVDC applications, this paper focuses on the established and emerging dc-dc converters, which show promise for HVDC applications. A brief discussion of each dc-dc converter will be presented, with broader emphasis on aspects related to power electronic systems. The discussions will be supported by a number of illustrative simulations.

II. CHALLENGES AND REQUIREMENTS FOR HIGH-VOLTAGE DC TRANSFORMERS

To focus investigation, this paper summarises some of the technical issues related to scalability of dc-dc converters for multi-terminal HVDC networks as follows:

a) F2F two-level and neutral-point clamped dc transformers require robust methods for static and dynamic voltage sharing of the series device connection in order to be able to operate with dc voltage suitable for HVDC transmission systems. However experiences from early generations of HVDC links show that the use of series connected IGBTs is limited to ±200 kV [47, 78].
b) Although adoption of a high fundamental frequency (1 kHz to 2 kHz) is attractive for reduced size and weight of magnetic components, switching of large voltage steps (400 kV or higher) at such frequencies impresses extremely high *dv/dt* upon interfacing transformers. This will make transformer design more challenging (that is, insulation and ability to transmit powers associated with dominant low-order harmonics such as the 3^{rd}, 5^{th} and 7^{th}).
c) Benefits of multi-level techniques in dc-dc applications, where fundamental frequencies are much higher than 50Hz may not be significant. This is because the reduction in transformer size will be limited by the minimum clearance between terminals and phases, bushing creepage, and transformer body structure must be mechanically strong to be able to support the weight of long high-voltage bushings, including magnetic forces during normal and abnormal operation. Thus, insulation and isolation within high voltage dc-dc converters will present major volume constraints.

Considering the importance of high-voltage dc-transformers for practical realisation of multi-terminal HVDC network with dc operating voltage of up to 800 kV (pole-to-pole), the most desirable features for high-voltage dc-dc converters are:

1) Scalable to high-voltage, and are likely required to use an interfacing transformer for galvanic isolation [65, 79], and better utilisation of switching devices at the converter with higher dc link voltage. In this manner, circulating reactive power in the ac link is minimized, without de-rating of the switching devices. Besides voltage matching, a dc-dc converter must be able to act as a dc power or dc voltage controller and prevent dc fault propagation within the dc network, without exposing its switching devices to risk of damage.
2) Voltage stresses (*dv/dt*) presented at the primary and secondary windings of the interfacing transformer, and voltage stresses across dc-dc converter switching devices and passive components must be fully controlled.
3) Since the size and weight reduction of the interfacing transformer in a high-voltage dc-dc converter is limited by the level of switching losses and other high-voltage and mechanical considerations as stated previously, the fundamental frequency in the ac link must be constrained to less than 1 kHz [65]. In multi-module dc-dc converters, where each sub-module operates at relatively low dc voltage and contributes a small fraction of the total output power, higher fundamental frequency can be achieved at the ac link [79, 80].
4) The dc-dc converter must be able to perform black-start at the ac link and controlled recharge of the dc link following dc fault isolation on any one of its dc terminals. Thus, modulation index control over a wide (0-1) range is required.

III. REVIEW OF ESTABLISHED AND EMERGING DC-DC CONVERTER TOPOLOGIES

A) *Two-level converter dual active bridge (DAB)*

Fig. 1 shows an example of a dc-dc converter that uses a typical two-level dual active bridge with series connected IGBTs (insulated gate bi-polar transistors) to enable operation at high dc voltage. With the use of a fundamental frequency ranging from 250 Hz to 1 kHz in the ac link, the overall size and weight of the dc-dc converter can be reduced, without significant efficiency sacrifice. Traditionally, such two-level dual active bridges are operated in a square wave mode at the fundamental frequency, where each arm conducts for 180^o (half a fundamental period), with the load angle between v_{ao1} and v_{ao2} (Fig. 1) is traditionally used for power flow control between VSC_1 and VSC_2 [65, 77, 81-83]. In this operating mode, self-commutated semiconductor devices in the DAB tend to turn on and off at zero currents for much of the operating range (while anti-parallel diodes are in conduction); thus, low switching loss is achieved [65]. The use of pulse width modulation can provide an additional degree of freedom, which can be exploited to minimise the circulating reactive power in the ac link between VSC_1 and VSC_2. However, with fundamental frequency range stated, the use of high-frequency pulse width modulation (PWM) must be precluded, because the increase in switching losses is expected to outweigh the gain that will be achieved by increased control flexibility [65, 76, 84, 85]. To avoid this shortcoming of the high frequency PWM, low-frequency modulation schemes such as selective harmonic elimination (SHE) with one notch per quarter cycle can be used to achieve the necessary control flexibility, specifically ac voltage and reactive power control in the ac link between VSC_1 and VSC_2, especially during a dc fault. However, with SHE the range at which inherent soft switching during DAB turn-on and off is achieved will be reduced; hence, switching losses are expected to increase.

Fig. 2 (a) shows switched ac voltages VSC_1 and VSC_2 the two-level DAB in Fig. 1 impress on the primary and secondary windings of the medium-frequency transformer in the ac link. In this illustration, the fundamental frequency is 500 Hz, both VSC_1 and VSC_2 are operated using fundamental frequency switching with 180^o conduction, input and output dc link voltages of VSC_1 and VSC_2 are ±400 kV and ±350 kV respectively, and the power flow direction is from VSC_1 to VSC_2. Fig. 2 (c) shows sampled dc power measured at the dc link of VSC_2 (when VSC_2 ramps the power flow from VSC_1 and VSC_2, from 0 to 800 MW). The switched voltage waveform at the terminal of VSC_1 (v_{ao1} for phase '*a*') leads that of VSC_2 (v_{ao2}) as expected when the power flow direction is from VSC_1 to VSC_2. Theoretically, the switch voltages v_{ao1} and v_{ao2} of the VSC_1 and VSC_2 can be expressed as:

$$
\begin{aligned}
v_{ao1}(t) &= \frac{2V_{dc1}}{\pi}\sum_{n=1,3,5.}^{\infty}\frac{\sin n\omega t}{n} \\
v_{ao2}(t) &= \frac{2V_{dc2}}{\pi}\sum_{n=1,3,5.}^{\infty}\frac{\sin(n\omega t+n\delta)}{n}
\end{aligned} \tag{1}
$$

where δ is the angle of v_{ao2} relative to v_{ao1} and $n=2j+1, \forall j \in \mathbb{Z}$. If the medium-frequency transformer is assumed to be lossless and with L_T transformer leakage inductance referred to primary, the primary instantaneous current can be expressed as:

$$
i_{ao1}(t) = i_{ao1}(0) + \frac{1}{\omega L_T}\left[-\sum_{n=1}^{\infty}\frac{2V_{dc1}}{\pi n^2}\sin(n\omega t+\tfrac{1}{2}\pi) + k\sum_{n=1}^{\infty}\frac{2V_{dc2}}{\pi n^2}\sin(n\omega t+\tfrac{1}{2}\pi+n\delta)\right] \tag{2}
$$

With the instantaneous power at the terminals of the lead converter VSC_1 expressed as $p_1(t)=3v_{ao1}i_{ao1}(t)$, the average power VSC_1 exchanges with VSC_2 is:

$$
P_1 = \frac{1}{T}\int_0^T p_1(t)dt = k\,\frac{6V_{dc1}V_{dc2}}{\pi^2\omega L_T}\sum_{n=1}^{\infty}\frac{\sin n\delta}{n^3} \tag{3}
$$

where k is the turn ratio (primary to secondary).

Equation (3) indicates that the medium-frequency transformer must be designed to transmit all the powers associated with significant low-order harmonics, including that of the fundamental component. Here, the load angle is the only available degree of freedom that can be used to control power flow. When SHE is used as depicted in Fig. 2 (b), expressions for v_{ao1} and v_{ao2} become [86]:

$$
\begin{aligned}
v_{ao1}(t) &= \frac{2V_{dc1}}{\pi}\sum_{n=1,3,5.}^{\infty}\frac{[2\cos n\alpha_1 - 1]}{n}\sin n\omega t \\
v_{ao2}(t) &= \frac{2V_{dc2}}{\pi}\sum_{n=1,3,5.}^{\infty}\frac{1}{n}[2\cos n\alpha_2 - 1]\sin(n\omega t + n\delta)
\end{aligned}
\tag{4}
$$

The average power VSC_1 exchanges with VSC2 is:

$$
P_1 = \frac{1}{T}\int_0^T p_1(t)dt = k\frac{6V_{dc1}V_{dc2}}{\pi^2\omega L_T}\sum_{n=1}^{\infty}[2\cos n\alpha_1 - 1][2\cos n\alpha_2 - 1]\frac{\sin n\delta}{n^3} \tag{5}
$$

Equations (4) and (5) show that with SHE the power flow in the ac link can be controlled using voltage magnitudes at the terminals of VSC_1 and VSC_2, and the phase shift between these voltages (load angle *δ)*. Fig. 2(b) and (d) show ac voltages VSC_1 and VSC_2 present at the primary and secondary windings of the coupling transformer, and dc power measured at the dc link of VSC_2 when power flows from VSC_1 and VSC_2, and VSC_2 ramps its power command from 0 to 800 MW (both VSC_1 and VSC_2 are controlled using SHE). From Fig. 2 (b) and (d), although SHE introduces an additional degree of freedom, the principle of controlling the DAB remains the same.

With continuously increasing dc operating voltage of voltage source converter based high-voltage direct current (VSC-HVDC) transmission systems, the rate of change of voltage *dv/dt* that the two-level DAB in Fig. 1 impresses upon the medium-frequency transformer between VSC_1 and VSC_2 becomes intolerable, and restricts its applications to relatively low power and dc voltages of up to ±200 kV dc, as in early generation two-level and neutral-point clamped based VSC-HVDC links.

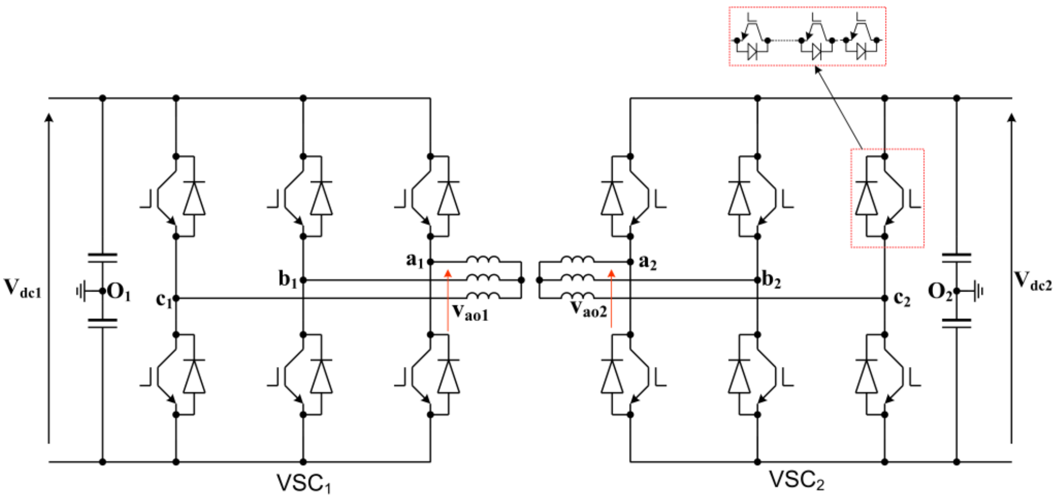
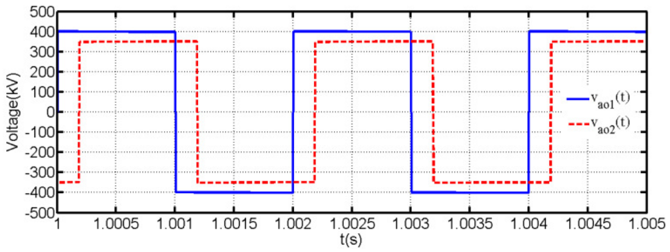
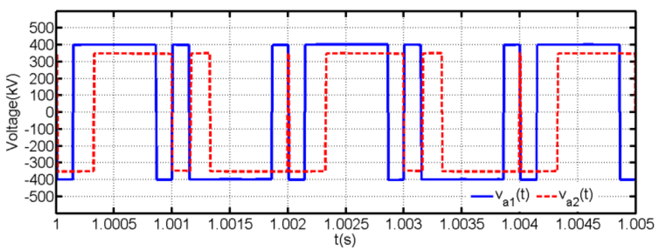


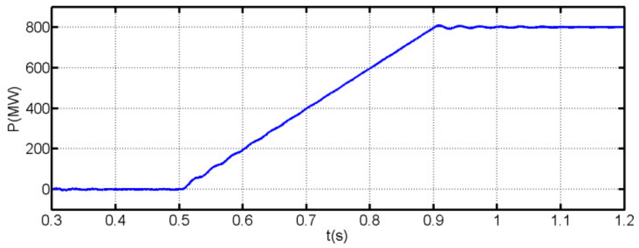
Fig. 1: IGBT based two-level converter dual active bridge (V_{dc1}=800 kV, V_{dc2}=700 kV, 500Hz fundamental frequency and medium frequency transformer rated at 1000 MVA, 500 kV/450 kV with 10% per unit reactance)



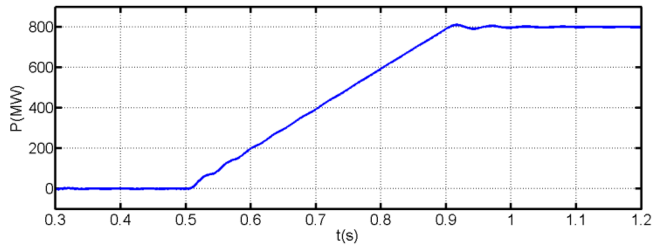
(a) Voltage waveforms at the terminals of VSC_1 and VSC_2 (v_{ao1} and v_{ao2}) when power flow is from VSC_1 to VSC_2 (fundamental frequency switching)



(b) Voltage waveforms at the terminals of VSC_1 and VSC_2 (v_{ao1} and v_{ao2}) when power flow is from VSC_1 to VSC_2 (SHE with active power and ac voltage control in the high frequency ac link)



(c) Power flow in the dc link of VSC_2 (fundamental frequency switching, VSC_2 ramps its power command from 0 to 800 MW)

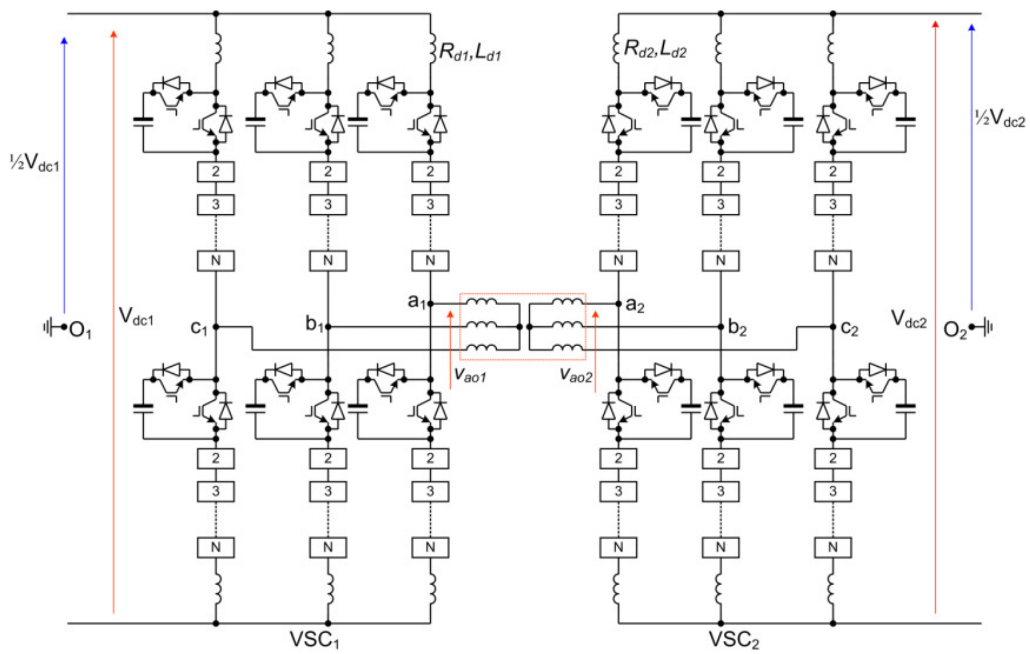


(d) Power flow in the dc link of VSC2 (SHE, VSC_2 ramps its power command from 0 to 800 MW)

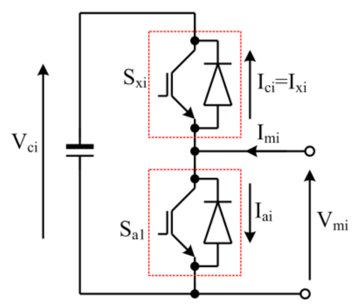
Fig. 2: Waveforms illustrating the basic operation of a two-level converter DAB (fundamental frequency=500 Hz)

B) *Modular multilevel converter dual active bridge*

As power handling and the dc operating voltage of the VSC-HVDC links continue to increase, the modular multilevel converter dual active bridge (MMC-DAB) with a medium-frequency transformer in the ac link in Fig. 3 is more likely to be adopted. The use of a medium-frequency ac link is not only beneficial for compact transformer design, but also leads to overall reduction in the size of the MMC-DAB passive elements such as cell capacitances and arm reactors. Practically, the ac link of an MMC-DAB can be operated using full multilevel modulation with sinusoidal voltage or in a quasi two-level mode with trapezoidal voltage as suggested in [53]. These two possibilities will be explored in the subsequent parts.



(a)



(b)

Fig. 3: Modular multilevel converter dual active bridge

a) Multilevel operation of MMC-DAB with sinusoidal voltage and currents in the ac link

This mode operates the MMC-DAB in Fig. 3 using multilevel modulation similar to that used in the converter terminal of the typical VSC-HVDC link, where the MMC is connected to the ac grid [50]. Basic operating principle of the MMC can be explained using sub-converter VSC_1 in the MMC-DAB Fig. 3(a). Each of phase-leg of the VSC_1 depicted in Fig. 3(a) comprises of upper and lower arms, each consists of N_1 half-bridge cells such as shown in Fig. 3(b). Each MMC arm supports full dc link voltage (V_{dc1}), with the voltage across each cell capacitor must be maintained strictly around $V_{cell}=V_{dc1}/N_1$ or $V_{cell}=V_{cref}/N_1$, depending on the control method to be employed. To control the power flow between MMC ac and dc sides, without unnecessary inrush current in the dc side, the distributed cell capacitors of each MMC phase-leg must be controlled such that the upper and lower arms are operated in complementary manner according to the following insertion functions: $n_{a1}(t) = \frac{1}{2}N_1[\alpha_d - m\sin(\omega t + \delta)]$ and $n_{a2}(t) = \frac{1}{2}N_1[\alpha_d + m\sin(\omega t + \delta)]$; where, $\alpha_d = V_{dc1}/V_{cref}$, m is the modulation index, δ is the VSC_1 load angle measured relative to VSC_2, V_{cref} is the desired set-point for the sum of the cell capacitor voltages of each arm, and n_{a1} and n_{a2} are the number of cells to be selected from the upper and lower arms at each instant. Instantaneous voltage across the upper and lower MMC arms are: $v_{a1} = n_{a1}(t)\times V_{cell} = \frac{1}{2}V_{cref}[\alpha_d - m\sin(\omega t + \delta)]$ and $v_{a2} = n_{a2}(t)\times V_{cell} = \frac{1}{2}V_{cref}[\alpha_d + m\sin(\omega t + \delta)]$ [1, 87]. The ac voltage will be generated at each converter pole such as 'a_1' relative to ground (O_1) represents the different-mode voltage of phase-leg 'a' and it is given by: $v_{ao1} = v_{a2} - v_{a1} = \frac{1}{2}mV_{cref}\sin(\omega t + \delta)$. During normal operation, V_{cref} is regulated aroundV_{dc1}; thus, $\alpha_d \approx 1$. Notice that the aforementioned operation allows each MMC phase leg to present sufficient dc or common-mode voltage ($v_{a1}+v_{a2}\approx\alpha_d V_{cref}$) to counter the input dc link voltage (V_{dc1}), while keeping sufficiently small voltage mismatch between the two voltages to allow the current flow in the dc link as it will be set by the power controller. The arm inductor L_d in Fig. 3(a) is needed to limit the inrush current due to mismatch between common-mode voltage and input dc link voltage. The aforesaid operation makes MMC is the only VSC, where the upper and lower arms of the same phase leg conduct simultaneously, and with co-existence of continuous ac and dc currents in all its arms; with the ac currents are being used to transfer active power from ac side to converter, and dc currents for power transfer from converter to the dc side[88]. When i_{a1} and i_{a2} are assumed to be phase 'a' upper and lower arm currents, with both currents have the same direction, phase 'a' output current (i_{ao}) represents the differential-mode current ($i_{ao}=i_{a1}-i_{a2}$). The current component that circulate between the upper and lower arm of phase 'a', without leaking into output circuit is denoted as common-mode current and it is given by: $i_{com}=\frac{1}{2}(i_{a1}+i_{a2})$. If appropriate measure is not put in place, MMC arm currents may contain some parasitic component such as 2nd order harmonic current that could increase semiconductor losses and cell capacitor voltage ripple. The main features of this mode are:

- Low switching losses and voltage stresses (*dv/dt*) on the isolation transformer of the MMC-DAB compared to its two-level equivalent (this is achieved through sequential switching of small voltage step, with an average switching frequency per device of 3 to 4 times the fundamental frequency).
- Full modulation index range is available for voltage control in the ac link during dc faults and for provision of black start of a dead dc networks following a blackout.
- This mode does not fully exploit the active powers associated with significant low-order harmonic voltages and currents; therefore, MMC-DAB operated in this mode is expected to have lower power density compared to its two-level equivalent [62, 75, 89]. Also, full exploitation of soft switching as in the DAB configuration is not possible (only some of the devices will turn on and off at zero current).

Although the use of a medium-frequency ac link between VSC_1 and VSC_2 of the MMC-DAB may lead to a compact design as previously stated, operation with low modulation index during black start following a dc network fault will increase the loading on the cell capacitors. Thus, cell capacitance must be oversized to keep cell capacitor voltage ripple within tight limits, and avoid exposing switching devices to increased voltage stress.

The average active power exchange between VSC_1 and VSC_2 when the MMC-DAB is operated with sinusoidal currents and voltages in the ac link can be approximated by:

$$P_1 = k \frac{3 m_1 m_2 V_{dc1} V_{dc2}}{8 \omega L_T} \sin \delta \tag{6}$$

where, m_1 and m_2 are the modulation indices of VSC_1 and VSC_2 ($m_1=2V_{m1}/V_{dc1}$ and $m_2=2V_{m2}/V_{dc2}$, and V_{m1} and V_{m2} are peak fundamental voltages at the terminal of VSC_1 and VSC_2). Equation (6) only exploits the active power associated with the fundamental voltage and current (lower power density is expected).

b) Quasi-two-level (Q2L) operation of MMC-DAB

Quasi two-level operation of multilevel converters was initially proposed for diode clamped multilevel inverters [90-93] and later adopted for modular multilevel converters [75]. This mode operates the modular multilevel converter as a two-level converter, except that the cell capacitors of the modular converter are used briefly as a clamping network to facilitate orderly transition of the output phase voltage $v_{ao1}(t)$ from $-½V_{dc}$ to $½V_{dc}$ and vice versa, as shown in Fig. 4. With the time spent (dwell time t_d) at each intermediate voltage level being sufficient small (5µs to 25µs), t_d must be selected taking into account the switching capability of employed semiconductor devices. This mode loads the MMC cell capacitors with fundamental current for a short time during stepped transitions of the output phase voltage $v_{ao1}(t)$ between the positive and negative dc rails as illustrated in Fig. 4. In this way, the energy storage requirement of the cell capacitors (cell capacitance) and overall footprint of the MMC is reduced drastically. This makes the MMC-DAB operated in the Q2L mode well suited, promising candidate for dc-dc converters for multi-terminal HVDC networks. Q2L operation mode bypasses the upper and lower arm cell capacitors of each MMC phase-leg for the majority of the fundamental period when the output phase voltage $v_{ao1}(t)$ is clamped at $-½V_{dc}$ or $½V_{dc}$. Such operation leads to small voltage mismatch between the input dc link voltage and the sum of the cell capacitor voltages in each arm. Thus, small arm inductances suffice to limit the circulating currents as demonstrated in [75, 94]. Practically, dwell time t_d can be pre-defined or varied based on the cell capacitor balancing requirements when the MMC-DAB is operated with fixed voltage magnitudes in the medium-frequency ac link. Alternatively, the dwell time t_d can be varied to vary the magnitude of the ac voltage at the MMC terminals to minimize circulation reactive power and facilitate black-start following blackout in one of the dc or ac sides. However, such variation increases the loading on the cell capacitors by the fundamental current as *Q2L* operation mode converges to typical multilevel operation. This increases the energy storage requirement of the MMC cell capacitors; thus, cell capacitance. The output phase voltages $v_{ao1}(t)$ and $v_{ao2}(t)$ that VSC_1 and VSC_2 of the *Q2L* operated MMC-DAB present to the primary and secondary windings of the transformer in the ac link are:

$$\begin{aligned} v_{ao1}(t) &= \frac{2V_{dc1}}{\pi} \sum_{n=1}^{\infty} \frac{\sin n\alpha_1}{n^2 \alpha_1} \sin n\omega t \\ v_{ao2}(t) &= \frac{2V_{dc2}}{\pi} \sum_{n=1}^{\infty} \frac{\sin n\alpha_2}{n^2 \alpha_2} \sin n(\omega t + n\delta) \end{aligned} \tag{7}$$

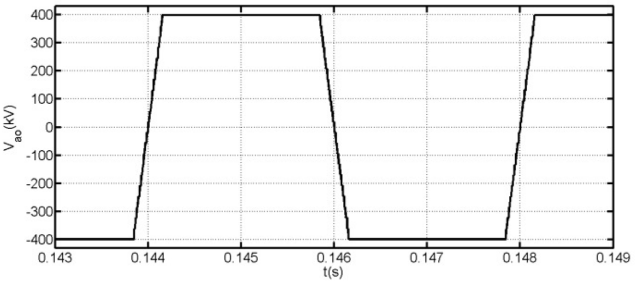
Following similar procedures as with the two-level DAB, active power of the Q2L operated MMC-DAB is:

$$P_1 = k \frac{6V_{dc1} V_{dc2}}{\pi^2} \sum_{n=1}^{\infty} \frac{\sin n\alpha_1 \sin n\alpha_2}{n^4 \alpha_1 \alpha_2} \sin n\delta \tag{8}$$

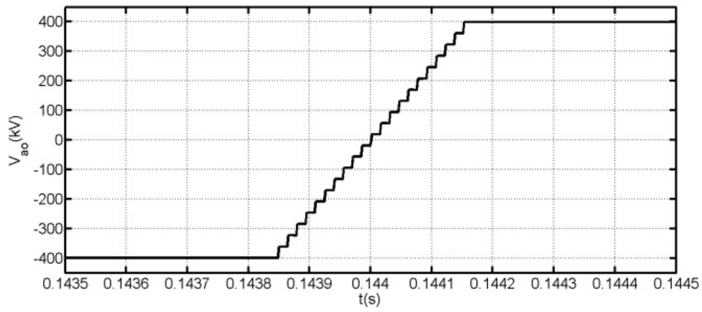
Implementation of MMC Q2L operation as suggested in [94, 95] results in considerable MMC switching loss reduction as each switching device operates at the fundamental frequency, and the upper and lower MMC arms are bypassed alternately every half fundamental cycle. Switching losses has been shown in [53] comparable to those of a two-level DAB. A further soft switching method has been recently proposed in [96].

Trapezoidal operation involves each MMC arm being connected in parallel with the input dc link voltage every 180°, with rapid recharge of the MMC cell capacitors to the input dc link voltage. This makes the current in each arm drop to zero every half fundamental period. The main disadvantage of the implementation suggested in [95] is that modulation index control is only achievable within a narrow range ($0.81<m<1.27$). Auxiliary techniques can be employed to extend this range as detailed in [53].

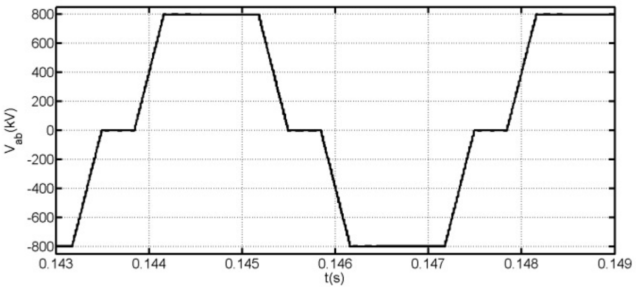
Fig. 4 shows illustrative simulation results from a Q2L operated MMC with the scheme suggested in [95]. Waveforms in Fig. 4 are for a 250Hz fundamental frequency. Fig. 4 (a) and (b) show phase voltage relative to dc ground of a symmetrical monopole and its expanded version during transition from $\frac{1}{2}V_{dc}$ (+400 kV) to -$\frac{1}{2}V_{dc}$ (-400 kV). Fig. 4 (c) shows the line-to-line voltage. Upper and lower arm currents displayed in Fig. 4 (d) show each arm current falls to zero as stated. Fig. 4 (e) shows that despite the significant reduction achieved in the magnitudes of the arm inductance and cell capacitance, the cell capacitor voltages of the Q2L operated MMC are tightly controlled, with voltage ripple well below 10%. This means a further reduction in cell capacitance may be possible from the converter operational point of view. Fig. 4 (f) shows samples of the currents in the switching devices S_x and S_m (S_x is the IGBT connected in series with the cell capacitor, and S_m is the IGBT that bypasses the cell capacitor), and highlights that both switches (S_x and S_m) operate at the fundamental frequency. Additionally, switch S_x of each cell experiences lower current stresses than with full multilevel operation. Switch S_m of each cell experiences higher current stresses than with full multilevel operation (since the total power each phase contributes is being exchanged through one arm at any instant time instead of two arms as in full multilevel operation). Because of the reduce cell capacitance, the dc link current ripple is higher than with full multilevel operation.



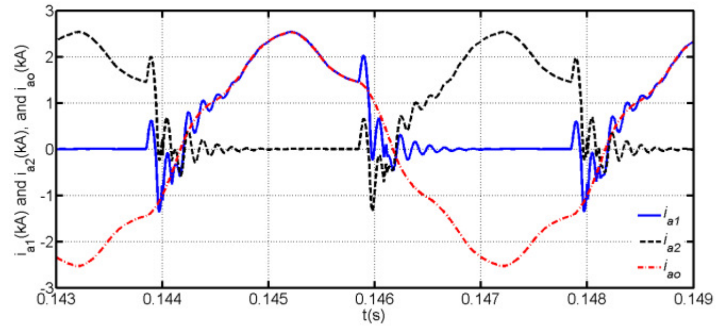
(a) Output voltage (v_{ao1}) that Q2L operated MMC presents to its interfacing transformer



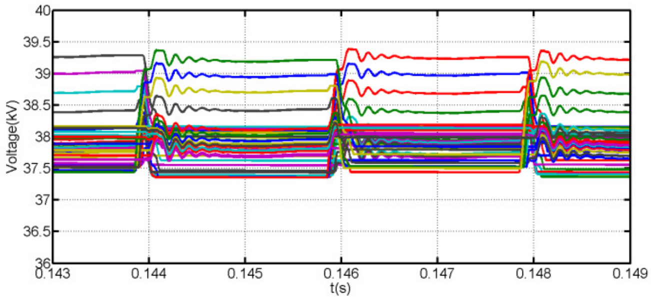
(b) 'v_{ao}' expanded around the transition from $+\frac{1}{2}V_{dc}$ to $-\frac{1}{2}V_{dc}$ illustrating the low dv/dt on the interfacing transformer



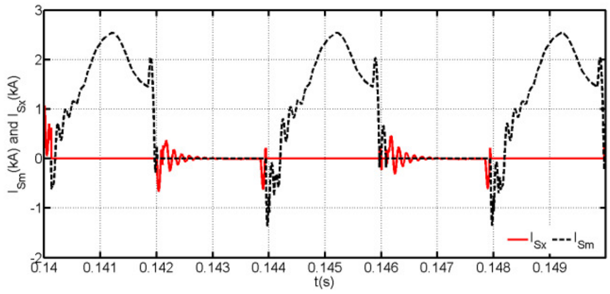
(c) Line-to-line voltage Q2L operated MMC presents to its interfacing transformer



(d) Upper and lower arm currents (i_{a1} and i_{a2}), and output phase 'a' current i_{ao}



(e) Phase ‘*a*’ cell capacitor voltages



(f) Current in switching devices of one cell (I_{Sx} is the current in the device in series with cell capacitor, and I_{Sm} is the current in the main device that bypasses the cell capacitor)

Fig. 4: Waveforms illustrating the suitability of the Q2L operated MMC for dc-dc conversion (21-cell switch model, dc link voltage is 800 kV, arm inductor L_d=50 µH, combined internal resistance of the arm reactor and the on-state resistance of switching devices R_d=0.3 Ω, cell capacitor C_m=50 µF, modulation index m=1.26 and fundamental frequency=250 Hz)

c) Dual active bridge based Controlled Transition Bridge (CTB) converter

Fig. 5 shows a dual active bridge dc-dc converter based on three-phase controlled transition bridge multilevel converter proposed in[97]. Consider converter 1 of DAB in Fig. 5, the circuit structure of CTB is similar to that of the T-type inverter discussed in[98, 99], except the series connected switches of the T-inverter between each output pole (a_1, b_1 and c_1) and the neutral-point (O_1) are replaced by full-bridge (FB) chain links. A CTB multi-level converter with N_1 FB cells per limb can generate ‘$2N_1+1$’ voltage levels per phase, between (a_1, b_1 and c_1) and O_1. When a CTB multilevel converter is operated as suggested in [97], the switching devices of its main two-level bridge operate at the fundamental frequency; thus, negligible switching loss is incurred in this stage. Operationally, the chain link of each limb needs to block only half the input dc link voltage (V_{dc1}); hence, the voltage across each cell capacitor must be maintained at $½V_{dc}/N_1$. This means the number of semiconductor devices in conduction path in each limb is $2N_1$, which is the same as the main two-level bridge and as in a conventional two-level converter. As an example, for a CTB with a 640kV dc link voltage that employs 4.5kV IGBT with 55% device utilization (2.5kV per IGBT at two-level bridge and chain links), the number of IGBT in the conduction path in each instant is 256 and number of full-bridges per limb is 128. This indicates that the CTB converter is expected to have lower on-state losses than a HB-MMC. The chain links and two-level bridge of the CTB converter in Fig. 5 operate in a complementary manner, with the chain links of each phase being used to facilitate controlled transitions between the positive and negative dc buses ($+½V_{dc}$ and $-½V_{dc}$) through intermediate voltage levels.

Generally, the CTB converter can be operated using established modulation strategies, especially when it is used as a converter terminal of the VSC-HVDC link. For dc-dc converter applications, where converter footprint and weight are increasingly important, Q2L operation of the CTB offers several advantages (as presented in [56]):

- Smaller footprint compared to Q2L operated MMC.
- Low semiconductor losses (the number of switching devices in the conduction path is lower than that in an MMC and most he hybrid converters of similar rating).
- Retains most of the attributes of the Q2L operated MMC such as low *dv/dt*, readily scalability to high voltage, and modular structure.

However, its main disadvantage is that the discharge of its concentrated dc capacitor at the input dc link may result in high current stresses in the freewheel diodes of the two-level stage during a dc side fault. But this is not a major issue in dc-dc converters because the ac link between the two CTB converters in Fig. 5 is weak (freewheel diodes of the faulty converter will see only short duration discharge current of the dc link plus cable capacitors).

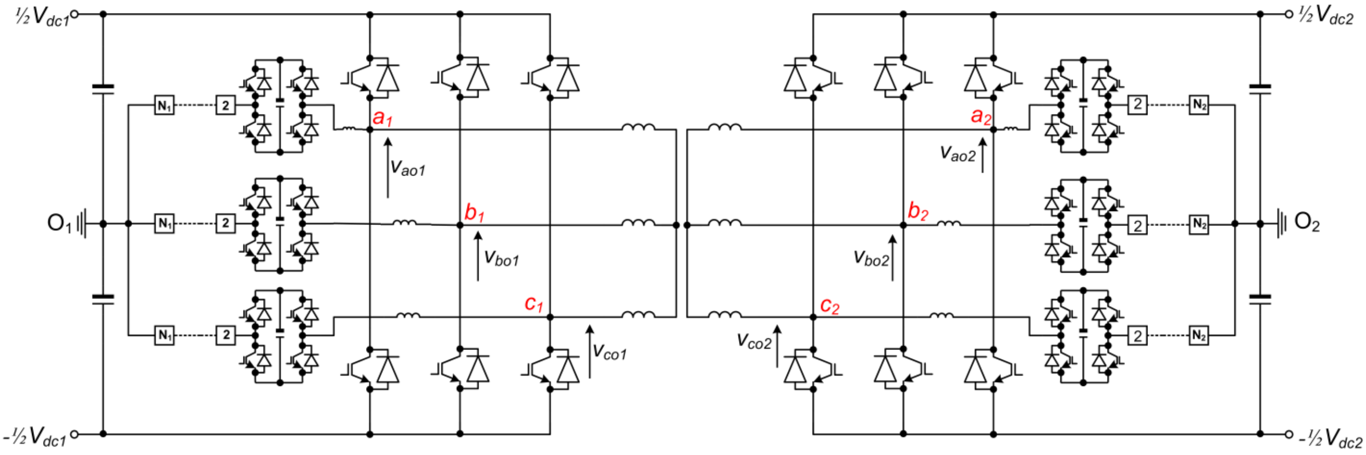
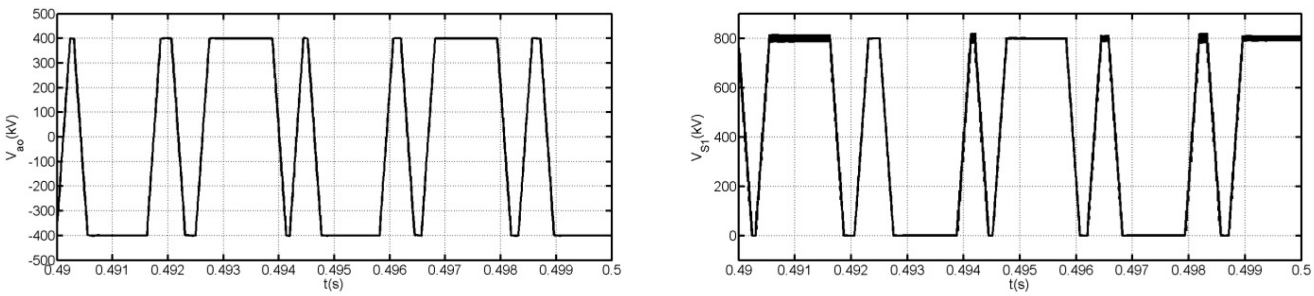


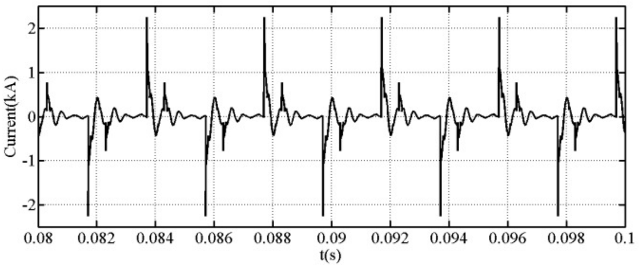
Fig. 5: Two-level Cascaded Transition Bridge (CTB)

To illustrate the suitability of the Q2L operated CTB converter for dc-dc converters, a three-phase 21-cell CTB converter is simulated with a 800 kV input dc voltage, connected to a passive load of 300 Ω with 0.98 power factor lagging per phase. Cell capacitance and current limiting inductance inserted in each limb are 100 µF and 50 µH respectively. In this illustration, SHE is used with 0.9 modulation index, and the results are shown in Fig. 6. Fig. 6 (a) shows the phase output voltage the CTB presents to the load when SHE based Q2L operation is adopted. Fig. 6 (b) shows the voltage stress across phase '*a*' upper switches of the two-level stage. The use of a Q2L operated CTB converter permits gradual increase of the voltage across the series IGBTs of the two-level stage. This offers the possibility of turning on and off the IGBTs (that form the composite switches of the two-level stage) individually and in a sequential manner (snubber circuits are avoided). Fig. 6 (c) shows the current waveform in the converter limb (that is, a series string of FB cells), and it indicates that the FB cascaded cells are recharged when the output phase is clamped to either the positive or negative dc rail, with the limb current dropping to zero when the sum of the voltages across the cascaded FB cells equals the dc link voltage. Also, each limb conducts for a small part of the fundamental period; hence switching devices with relatively low current rating can be used in the FB cells. Fig. 6 (d) shows that the cell capacitor voltages of the CTB converter are maintained around the desired set point, $\frac{1}{2}V_{dc}/N$. The results in Fig. 6 show that the CTB converter is promising as a HVDC dc-dc converter, without the constraints of the conventional two-level converter counterpart in terms of *dv/dt* and losses. However, its input dc link capacitor may increase the magnitude of transient discharge current during dc faults, which may increase the let-through current in the dc circuit breakers and other switchgear connected to the dc side to isolate dc faults.

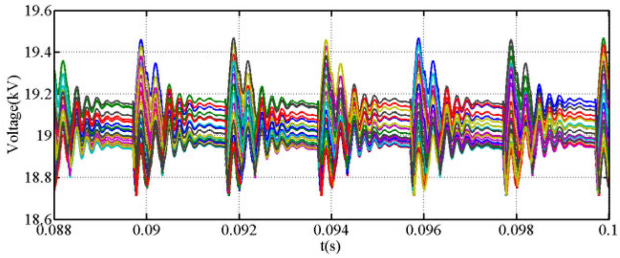


(a) Phase voltage (v_{ao}) measured relative to supply mid-point

(b) Voltage across upper switch of phase '*a*'



(c) Sample current in the limb that connects full-bridge cells of phase '*a*' to neutral –point or dc link mid-point

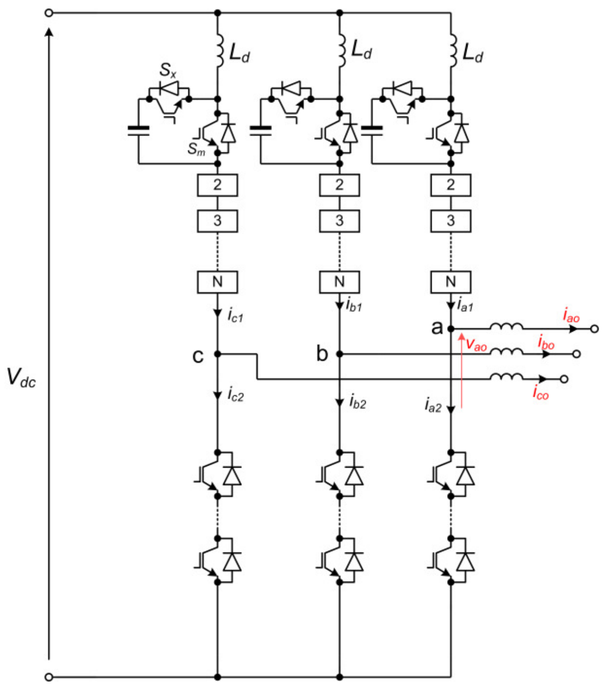


(d) Full-bridge cell capacitor voltages

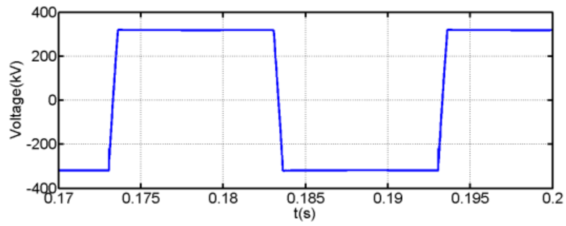
Fig. 6: Waveforms illustrating the suitability of the CTB two-level converter in dc-dc converter application, with modulation index control over the linear range (21-cell detailed switch model, V_{dc}=±400 kV, L_d=50 µH, C_m=100 µF, fundamental frequency=250 Hz, modulation index m=1)

d) Dual active bridge based on Transition arm multilevel converter (TAC)

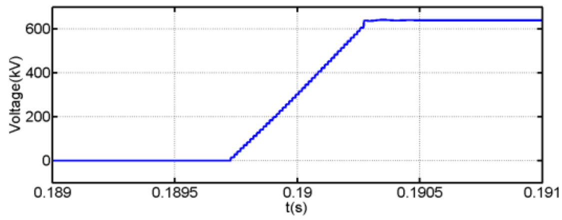
Transition arm multilevel converter (TAC) proposed in [100] offers possibilities for further reduction of footprint and semiconductor area in dc-dc converters for multi-terminal HVDC networks, see Fig. 7a. It is realized by replacing the HB chain links of the upper or lower arm chains in typical MMCs by high-voltage composite switches such as series connected IGBTs. In the TAC, only the upper arms are used to facilitate controlled stepped transitions between the positive and negative dc rails when synthesizing the output ac voltage that will be imposed on the DAB ac transformer, see Fig. 7a and b. The lower arm high-voltage series switch of each phase leg is turned on only when the output voltage of -½*Vdc* needs to be synthesized at the ac output poles '*a*', '*b*' and '*c*'. Otherwise, these high-voltage series switches remain off. For example, when turning on the high-voltage series switch of the phase '*a*', all the cell capacitors of the upper arm of the phase '*a*' are inserted into the power path, in parallel with the input dc link voltage. This causes a common-mode current to flow in both arms (upper and lower) to recharge the cell capacitors of the upper arm to V_{dc}/N_c, where V_{dc} and N_c are input dc link voltage and number of cell capacitors per transition arm (see Fig. 7c, d and e). With such operation, the voltage stress across the high-voltage series switches will be built gradually; thus there is no need for complex snubber circuits to facilitate dynamic voltage sharing between the series connected IGBTs. The upper and lower arm currents of the TAC drop to zero every half fundamental period as in the Q2L operated MMC previously discussed, since the output poles of the TAC are clamped to the positive and negative dc rails alternatively every 180^o, for the majority of the fundamental period. The arm inductance of the TAC operated in this mode is expected to be small, similar to that of the Q2L operated MMC. This discussions show that TAC is promising for high-voltage dc transformer application.



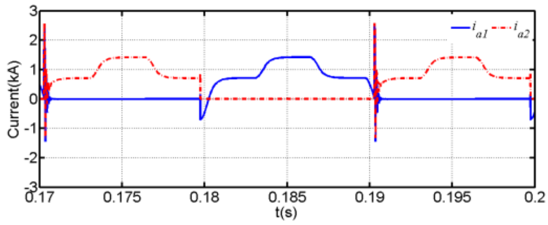
(a) Transition arm modular multilevel converter



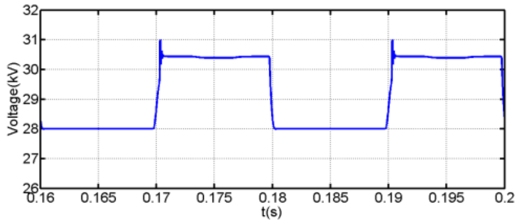
(b) Terminal voltage (v_{ao})



(c) Zoomed voltage across the upper arm



(d) Samples of the upper and lower arm currents



(e) Sample cell capacitor voltage

Fig. 7: Transition arm modular multilevel converter and its selected waveforms that aim to illustrate its operational principle (average model of TAC, V_{dc}=640 kV, L_d=0.1 mH, C_m=60 µF(equivalent cell capacitance $C_e=C_m/21$), 50 Hz fundamental frequency and operated using trapezoidal modulating signals, and equivalent load connected to ac side is 812 MW and 85 MVAr inductive)

e) Dual active bridge dc-dc converter based on alternative arm modular multilevel converter (A2M2C-DAB)

Fig. 8 shows the A2M2C-DAB dc-dc converter proposed in [101] and [63] that reduces the number of full-bridge cells required per arm when compared with the FB-MMC. By altering the basic operation of the FB-MMC, each arm of the A2M2C operates for 180^{o}, while a director switch is used to ensure that each arm is able to block the full dc link voltage. With the aid of a brief overlap time (where the upper and lower arms of the A2M2C conduct simultaneously), the director switches of each phase are able to facilitate a relatively smooth current commutation between the upper and lower arms over a limited power factor range. This modification allows the A2M2C to achieve dc fault blocking capability with reduced semiconductor losses when compared to the FB-MMC and hybrid cascaded two-level converter [53, 102-104], and a modest reduction in footprint. Operation of the A2M2C in the Q2L mode further reduces its footprint (size of cell capacitors and arm inductor), hence it is a suitable HVDC dc-dc converter. However, its overall efficiency remains lower than that of the Q2L operated half-bridge MMC due to the large number of switching devices it inserts in the conduction path. Additionally, the A2M2C-DAB is less likely to be adopted for high-voltage high-power dc-dc converters as dc fault blocking is not necessary and its concentrated input dc link capacitor may increase the peak of transient component of the dc fault current.

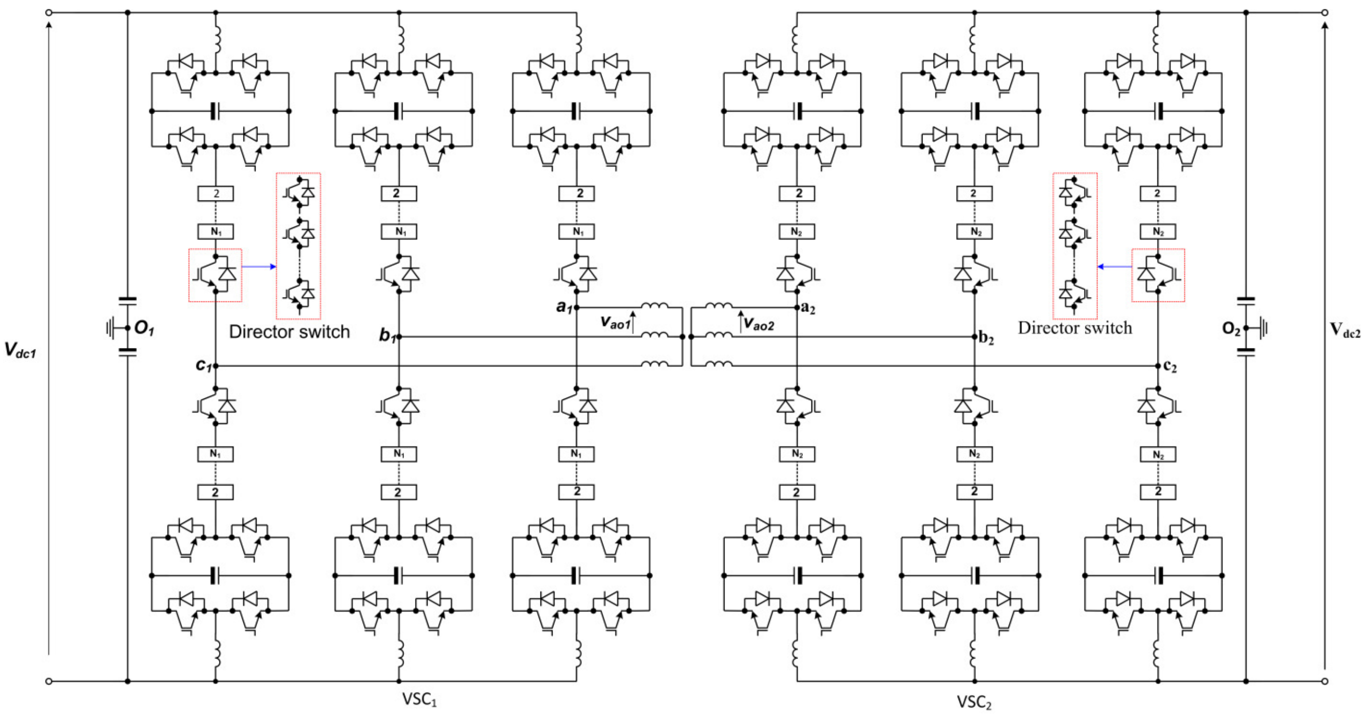


Fig. 8: Alternative arm modular multilevel converter dual active bridge (A2M2C-DAB)]

f) Dual active bridge based on hybrid cascaded two-level converter

Fig. 9 shows a dc-dc converter configuration that employs hybrid cascaded two-level converters with ac side FB cells [53, 105-107]. Although the numbers of switching devices and cell capacitors in the hybrid cascaded two-level converter shown in Fig. 9 are the same as in the CTB converter in Fig. 6, it offers reverse blocking capability during a dc fault. However, its main disadvantages are: it has a large number of switching devices (4*N*) in conduction path when compared to the CTB converter (2*N*), thus, higher semiconductor losses are expected even with Q2L operation; and its input dc link capacitor increases the magnitude of the dc fault currents experienced by the switchgear in the dc side as stated with CTB and A2M2C based DABs. Based on this discussion, the cascaded two-level converter is unlikely to be used for high-voltage dc-dc converters.

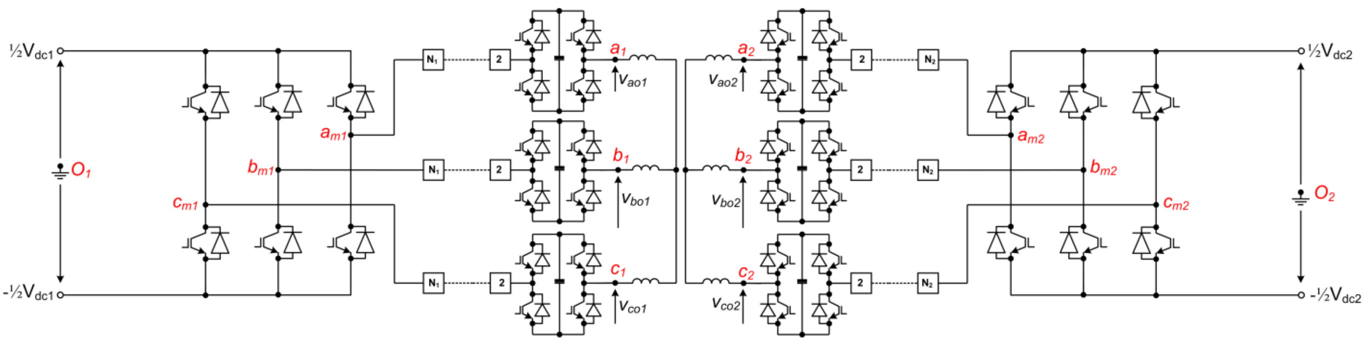


Fig. 9: Hybrid cascaded two-level converter

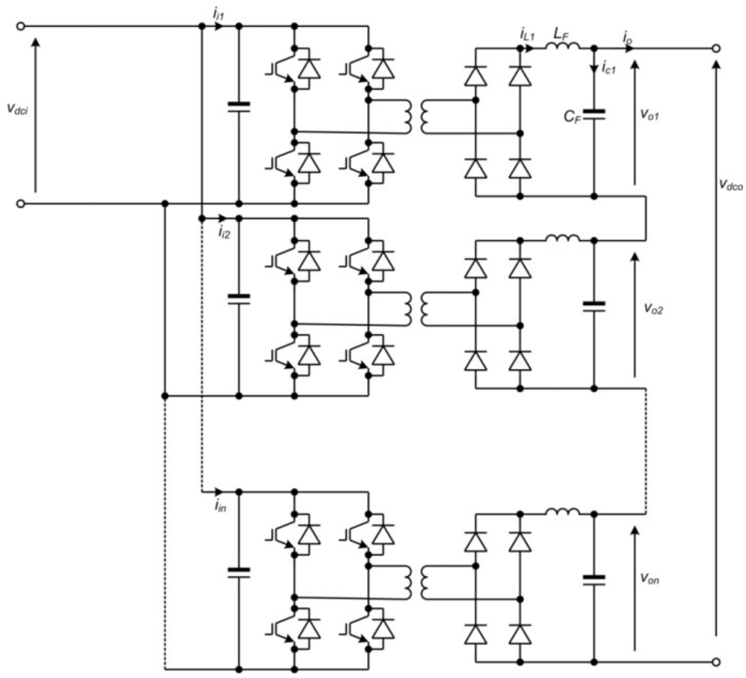
C) *Multi-module dc-dc converters*

Fig. 10a shows a flexible multi-module dc-dc converter with unidirectional power flow capability that can be used in medium-voltage high-power applications. In this arrangement, each sub-module operates at the rated voltage of a single device and contributes a fraction of the total output power; thus, operation with higher switching frequencies (>1 kHz) is achievable without significant design challenge or efficiency sacrifice. This type of dc-dc converter is also suited for applications where bi-directional power flow capability is not needed. Normally, the active front-end converter of each individual sub-module regulates that sub-module's output voltage with inner loop control that regulates the inductor current i_{Lj} (where j=1 to N, and N

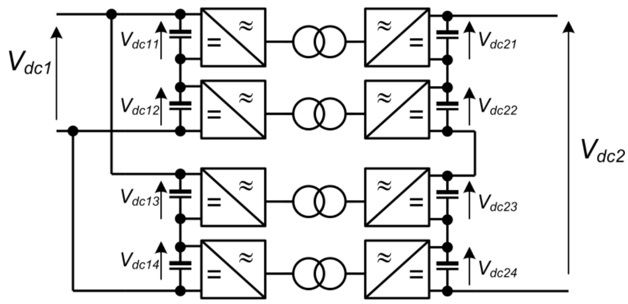
is the sub-module number) and constraints the sub-module current contribution during dc network transients. Additional control is needed to ensure equal output voltage and input current sharing between the sub-modules, and to facilitate extra functionality such as black-start of the dc network, etc. At high fundamental frequency, the leakage inductance of the ac link transformer must be designed carefully in order to avoid exacerbating the reverse recovery problem at each diode bridge, which is connected to the secondary side of each high-frequency transformer [77, 108]. In high-power applications, the rectifier diodes suffer from high reverse recovery currents, a limited zero voltage switching range of the front end converter FB, and duty cycle loss [65, 77, 83, 108-111]. Several solutions to the reverse recovery current problem of the rectifier diodes, high-voltage ringing and circulating reactive power have been suggested [65, 77, 79, 108].

Fig. 10b shows a generic version of a multi-module dc-dc converter with bi-directional power flow, where any of the submodules in Fig. 10 (c), (d) and (e) can be used. In the resonant version, the FB converters are used to adjust their operating frequencies to the resonant frequency of the ac link, thereby presenting near sinusoidal voltages to the primary and secondary windings of the high-frequency transformer, enabling switching devices of both bridges to operate at nearly zero current switching. However, the main disadvantage of this approach is that the voltage across the series resonant capacitor tends to be extremely high. As a result the resonant capacitor of each submodule tends to be relatively large and heavy. This makes the non-resonant version in Fig. 10c lighter and smaller than its resonant counterpart in Fig. 10d [79].

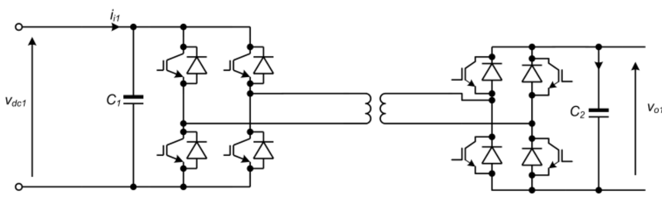
The half-bridge multi-module dc-dc converter with a split capacitor has been proposed in [80], see Fig. 10e. However, the topology in Fig. 10e has lower power density than the full-bridge version, Fig. 10c (should both topologies be fed from the same dc link voltage) and requires a larger filter capacitor to attenuate the large current ripple of the half-bridge cells (thus, larger footprint is expected). The multi-module dc-dc converters discussed in this section, and their derivatives, are expected to offer better solutions at medium-voltage when compared to the single large dc-dc converters discussed (over a wide range of operating frequencies). The main disadvantage associated with all multi-module dc-dc converters when employed beyond medium-voltage is the use of multiple transformers and their requirement for varying and high insulation from real ground.



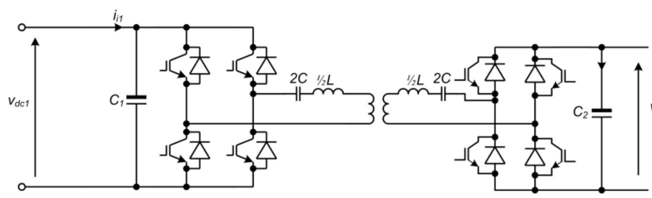
(a) Unidirectional power flow



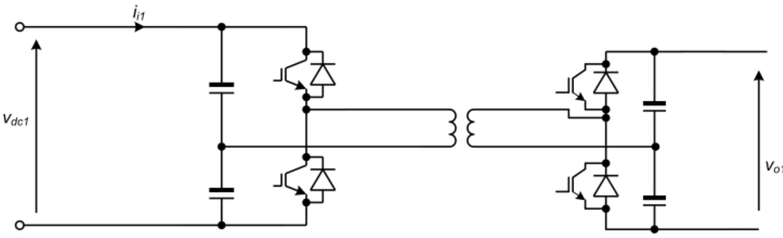
(b) Bi-directional power flow



(c) Bidirectional based on full-bridge bridge sub-module



(d) Bidirectional based on series resonant single-phase full-bridge module



(e) Bidirectional based on half-bridge single-phase module

Fig. 10: Generic schematic diagram of dc-dc modular multilevel converter [112]

D) *Non-isolated dc-dc converters*

a) Resonant based transformerless dc-dc converters

Fig. 11 shows a non-isolated resonant based dc-dc converter with bi-directional power flow capability [113, 114]. It was originally proposed as a high stepping voltage ratio (V_2/V_1) multi-functional unit for use in multi-terminal HVDC transmission systems, with the ability to control power flow in both directions and to limit the impact of a dc fault to within well-defined sections of the HVDC network. The claimed advantage of high stepping voltage ratio [113] may not be viable practically because the series-connected thyristors of the low-voltage side converter must be rated to withstand the peak voltage across the resonant tank capacitor, which is 1.2 to 1.4 times the nominal rated voltage of the high-voltage side (V_2). Although transformer-less operation is attractive, it may lead to poor device utilization at the high-voltage side and low efficiency with circulating reactive power in the ac link. The utilisation shortcoming is not only limited to this dc-dc converter, Fig. 11, but to all non-isolated dc-dc converter based DAB configurations. Being based on single phase concepts, the power ripple on both dc link sides at twice the resonant frequency and must be filtered, which adds to the dc fault current levels. Pre-existing grounding and filtering arrangements may preclude its connection to established dc links. Switch transient voltage sharing mechanisms have to be addressed, making a Q2L MMC approach attractive provided the link inductances are transferred to the ac sides.

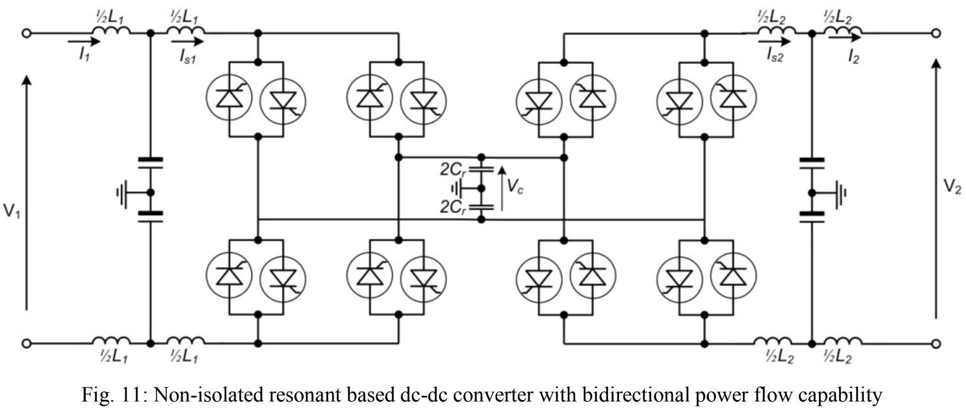


Fig. 11: Non-isolated resonant based dc-dc converter with bidirectional power flow capability

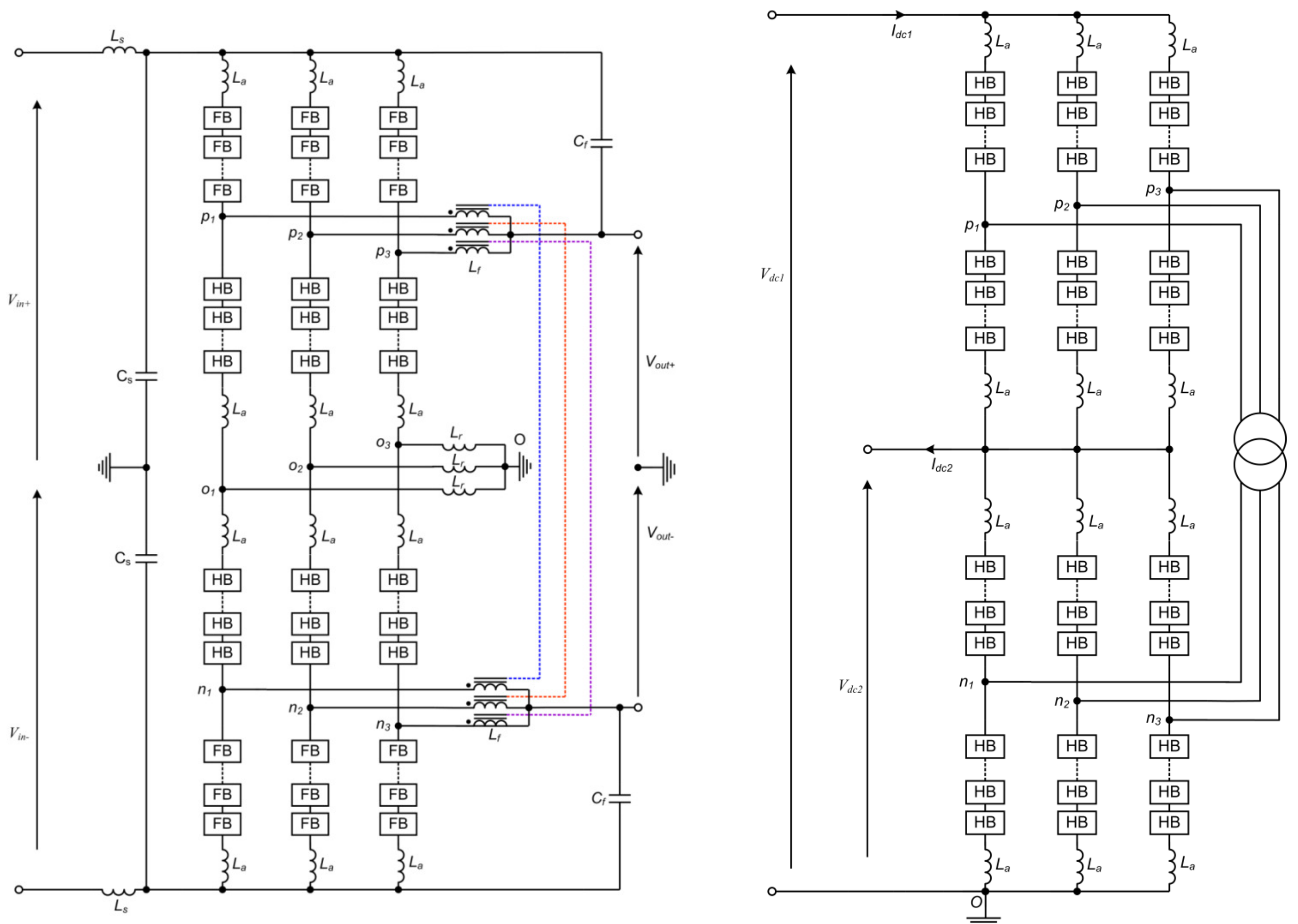
b) MMC transformerless dc converter topologies

Recently, the modular dc/dc converter topology of Fig. 12a was proposed [115, 116]. It generates output voltages that contain ac plus dc bias at the nodes (p_1, p_2 and p_3) and (n_1, n_2 and n_3) relative to ground. Therefore, it requires extremely large output filter inductance and capacitance to attenuate the fundamental ac voltage components from each phase voltage when measured relative to ground (L_f=990 mH is used for the ±17.6 kV, 40 MW system in [115]); otherwise, pole-to-ground dc voltage of the low-voltage side will be modulated at the fundamental frequency used to exchange power between converter arms. The claim that this dc-dc converter offers dc blocking capability is correct only when the dc fault occurs at the high-voltage side; but during pole-to-pole and pole-to-ground dc faults at the low-voltage side, sub-modules of the innermost arms are exposed to excessive current stresses. However, reverse blocking capability can be achieved if the inner and outer arms adopt mixed cells (combination of HB and FB cells).

Two versions of the non-isolated dc-dc converter, known as the tuned filter and the push-pull modular multilevel dc converter are presented in [89, 117]. Again both converter versions require significant filtering at the output dc port, with the tuned filter version reported to require more filtering than the push-pull version[89] . In [89] detailed design of the push-pull version concluded that filtering the ac components necessitate a similar amount of magnetics as in an equivalent multi-module DAB dc-dc converter. Therefore, they may not be competitive in medium and high-voltage applications..

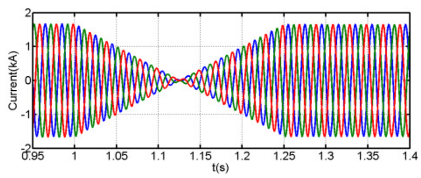
The auto dc transformer proposed in [118] and shown in Fig. 12b only converts part of the total dc power exchange between the two dc sides into ac power to be transferred to the lower converter through the coupling transformer in the ac link. The dc power converted into ac power is $P_{ac}=(V_{dc1}-V_{dc2})I_{dc1}=I_{dc1}V_{dc1}(1-V_{dc2}/V_{dc1})=P_{dc1}(n-1)/n$ and is fed to the dc side of the lower converter (where, $P_{dc1}=V_{dc1}I_{dc1}$ and $n=V_{dc1}/V_{dc2}$). The remaining part of the dc power will be transferred directly to the lower converter dc side, using the common mode currents of the upper converter (dc component of the arm currents), and this amount of power can be expressed as $P_{dc12}=P_{ac}/n$. Thus, the MVA rating of the coupling transformer in the ac link is reduced or even halved when $V_{dc1}:V_{dc2}=2:1$ or $(V_{dc1}-V_{dc2}):V_{dc2}=1:1$. With power flow shown by the direction of the dc currents in Fig. 12(b) and I_{d1} and I_{d2} being the magnitudes of the common mode currents in the arms of the upper and lower converters, respectively, the dc link current of the lower converter (I_{dc2}) is: $I_{dc2}=3(I_{d1}+I_{d2})$, where $I_{d1}=⅓I_{dc1}$ and $I_{d2}=⅓(V_{dc1}-V_{dc2})I_{dc1}/V_{dc2}=P_{dc1}(n-1)/n\times 1/V_{dc2}=P_{ac}/V_{dc2}$ (I_{d2} is set by the ac power transferred through the ac link). For example, when $V_{dc1}=2V_{dc2}$, $I_{d1}=I_{d2}=⅓I_{dc1}$ and $I_{dc2}=2I_{dc1}$, and these indicate that the auto dc transformer in Fig. 12b is expected to have higher efficiency than the F2F equivalent. This is because the semiconductor switches of the low-voltage side converter experience half the current stresses relative to that of an equivalent F2F connection (at a conversion ratio of 2). However, insertion of large number of FB cells in some of its arms in order to be able to cope with dc network faults at either dc side represents a limitation as it will jeopardize the high efficiency that could be achieved when only HB cells are employed. An additional problem of the asymmetric auto dc transformer in Fig. 12(b) is that it exposes both windings of the coupling transformers to high dc voltage stresses. This situation could be avoided should the auto dc transformer is rearranged to be symmetrical configuration so that both transformer windings avoid dc voltage stress. To support this discussion, the auto dc transformer of Fig. 12(b) is simulated using an average model, with the operating conditions shown in the caption of Fig. 13. Fig. 13 (a), (b) and (c) show current waveforms in the ac link and in the arms of the upper and lower converters of the auto dc transformer. The total power of 1400 MW is exchanged between the two dc sides, and the switching devices of the upper and lower converters experience equal current stresses (because $V_{dc1}=2V_{dc2}$). Fig. 13 (d) and (e) show the dc link currents at the high and low voltage side, and dc current components in the arms of the upper and lower converters. The dc currents components in the arms of the upper and lower converters in Fig. 13 (e) are equal, and this supports the results in Fig. 13 (b) and (c). Fig. 13 (f) shows dc powers at the terminal of the upper and lower converters and the ac power measured at the ac terminal of the lower converter. These results confirm this discussion regarding the internal power distribution in the auto dc transformer.

A multiport topology auto dc transformer has been recently presented in [119], which exhibits the same operating principles as the two port auto dc transformer explained but uses multiple ac transformers.

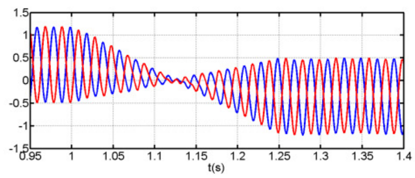


(a) (b)

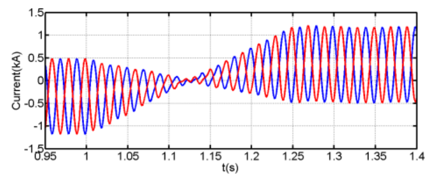
Fig. 12: (a) and (b) are possible configurations of symmetrical and asymmetrical auto dc transformer (dc-dc converter) [112, 118]



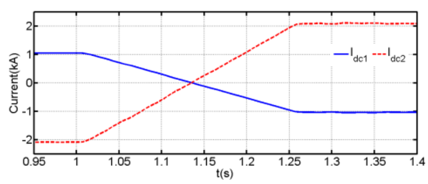
(a) Current waveforms in the ac link measured at the terminal of the lower converter



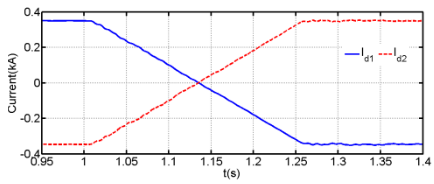
(b) Arm currents of the upper converter



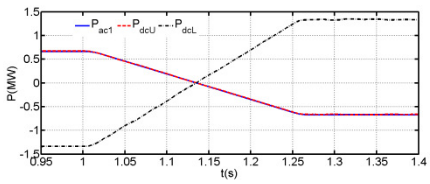
(c) Arm currents of the lower converter



(d) DC link currents of the high and low voltage sides (I_{dc1} and I_{dc2})



(e) DC current components of the arm currents of the upper and lower converters (I_{d1} and I_{d2})



(f) P_{dcU} and P_{dcL} are dc power measured at the terminal of the upper and lower converters and P_{ac} is the ac power measured at the terminal of the lower converter

Fig. 13: Selected waveforms obtained when 2600 MVA auto dc transformer in Fig. 12b is simulated with $V_{dc1}=2V_{dc2}$, $V_{dc2}=640\ kV$, 320 kV/320 kV ac transformer rated at 1300 MVA (initial power flow is 1400 MW from upper converter to lower converter and reverse at t=1s). Although 50Hz is used in the ac link for illustration and for faster simulation speed, a fundamental frequency in order of 250 Hz to 1 kHz could be adopted (high fundamental frequency requires small time-step).

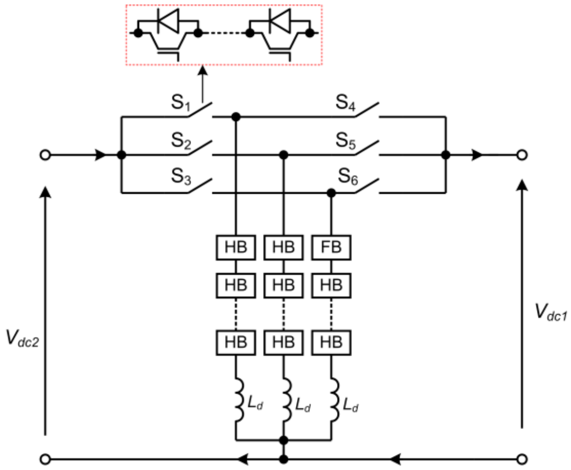
c) The hybrid cascaded transformerless dc converter

Fig. 14 shows possible high-voltage transformer-less dc transformers recently proposed in [120], which are developed around the hybrid cascaded two-level converter. Fig. 14 (a) shows the so called hybrid cascaded parallel two-level auto dc transformers. The six-pulse bridge of the two-level converter stage is connected in series with the positive pole of the dc line, while its ac side chain links are tied to ground or the negative pole of the dc line through current limiting inductors L_d. In this dc transformer, the HB chain links of each limb are rated at the full dc voltage of the high-voltage side so as to be able to switch alternatively between V_{dc1} and V_{dc2} using the series connected IGBTs of the two-level converter stage (for example, S_1 and S_4 for phase '*a*') without exposing the cell capacitor and switching devices of individual HB cells to excessive voltage stresses. When $V_{dc2}>V_{dc1}$, the series device IGBTs of the high and low voltage sides must be rated to withstand V_{dc2}-V_{dc1}, which is attractive from a semiconductor loss point of view. In the proposed dc transformer, the HB cell capacitors are clamped by the voltage across the submodule switching devices during abrupt switching between V_{dc2} and V_{dc1} in one large voltage step of V_{dc2}-V_{dc1}. The main weakness of the dc transformer topology of Fig. 14 (a) is that during a dc fault on its high-voltage side, the freewheel diodes of the two-level stage and main switches of the HB cells that bypass the cell capacitors will be exposed to high current stresses (unable to prevent fault propagation as in F2F topologies).

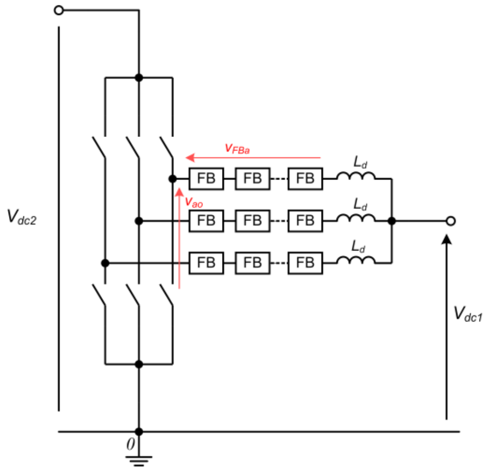
Fig. 14 (b) shows a type 1 hybrid cascaded series two-level dc transformer. When the dc link of the two-level stage is designated as the high-voltage side ($V_{dc2}>V_{dc1}$), the submodules of the cascaded chain links at the low-voltage side must be of the full-bridge type. In this arrangement, the FB chain link of each limb generates a bipolar ac voltage waveform that can be described by $V^*_{dc1} - \frac{1}{2}V_{dc}\left[1 + \mathrm{Sign}(\pi - \omega t)\right]$ in order to generate a ripple free dc voltage with magnitude V_{dc1} at the low-voltage side. This means the series connected switching devices of the two-level stage must be rated to block the full dc voltage of the high-voltage side (V_{dc2}). To prevent propagation of dc fault from one side to the other independent of fault location, the FB cascaded cells of each limb must be capable of supporting the full dc voltage of the high-voltage side, V_{dc2}. This feature is achieved with more semiconductor devices in the conduction path (thus, higher conversion loss is expected) compared to that in Fig. 14 (a), but losses remain lower than F2F dc transformer topologies.

Fig. 14 (c) shows a type 2 hybrid cascaded series two-level converter where the dc link of the two-level converter stage is designated as the low-voltage side. In this arrangement, the HB cells can be used in the chain link instead of the FB cells as each limb only needs to generate a unipolar voltage waveform to boost the output dc voltage. In this scenario, the chain link of each limb must be able to support the full dc voltage of the high-voltage side.

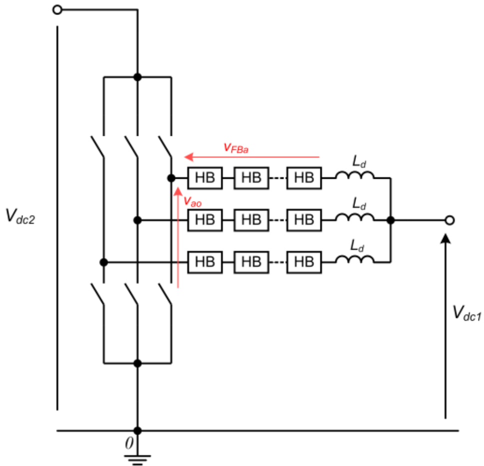
To support this discussion, a type 1 hybrid cascaded series two-level dc transformer, Fig. 14(b), is simulation with the high-voltage side connected to an active dc link voltage of V_{dc2}=800 kV and the low-voltage side is connected to a 500Ω passive load. The modulating function of the dc transformer in Fig. 14(b) is set so that it generates $V_{dc1}=560kV$ across the passive load at its low-voltage side. Fig. 15(a), (b) and (c) show the voltage across the FB chain link (V_{FBa}) and voltage waveforms at one terminal of the two-level converter stage (v_{ao}), and ripple-free dc voltage (V_{dc1}) converter in Fig. 14(b) presents across the passive load, which is connected to the low-voltage side. Fig. 15(a) shows the cascaded FB cells of each limb operates as an active series power filter that attenuates the ac voltage components generated at the terminals of the two-level converter stage (v_{ao}), see Fig. 15(a) and (b). Plot of the voltages across the cell capacitors shows that the voltage stresses on the cell capacitors and switching devices of the FB submodules are regulated (see Fig. 15(d)). Fig. 15(e) displays current waveforms in the three limbs of the active power filter stage that removes the ac voltage component from the v_{a0}, v_{b0} and v_{c0} in order to generate a ripple-free dc voltage (V_{dc1}) at the low-voltage side of hybrid cascaded converter Fig. 14(b). Observe that the fundamental current components of the three limbs cancel at the star point of the output dc node; thus, a ripple-free dc current is observed in the passive load connected to the low-voltage side, with each limb contributes approximately one third of the output dc current in the low-voltage side, Fig. 15(e) and (f).



(a) Hybrid cascaded parallel two-level dc-dc converter

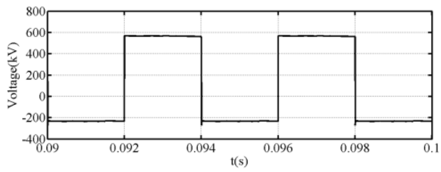


(b) Hybrid cascaded series two-level dc-dc converter-type 1 (full-bridge cells)

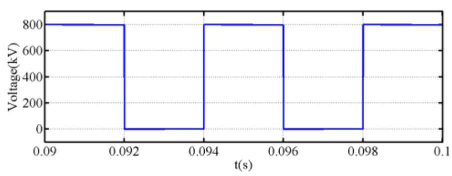


(c) Hybrid cascaded series two-level converter type 2 (half-bridge cells)

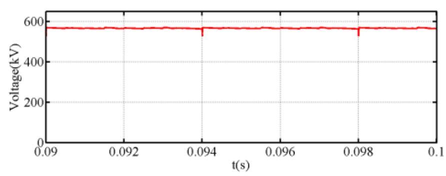
Fig. 14: Some of the transformer-less arrangement of dc-dc converter proposed in [120]



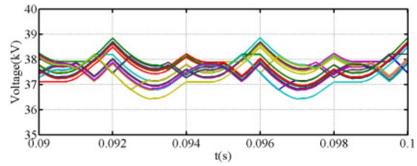
(a) Sample of the voltage waveform across the FB chain link



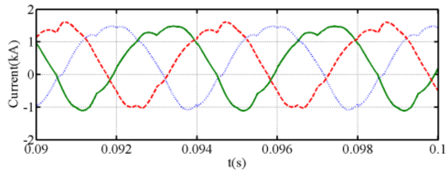
(b) Sample of the pole voltage (v_{ao}) at the terminal of the two-level converter stage



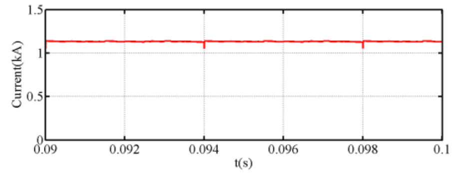
(c) DC Voltage generated at the low-voltage side (V_{dc1})



(d) Samples of the cell capacitor voltages



(e) Current waveforms in the three limbs of the low-voltage side



(f) DC current of the low-voltage side

Fig. 15: Waveforms for type 1 hybrid cascaded series two-level converter dc transformer simulated with 800 kV at high-voltage side and 560 kV imposed on the low-voltage side (detailed switched model with 21 cells per limb, Cell capacitance C_m=1 mF, L_d=4 mH, 250 Hz fundamental frequency, and 500 Ω load resistance)

IV. Conclusions and Summary of main Observations

This paper presented a review of a number of dc-dc converters which are scalable and applicable to multi-terminal HVDC networks. It has defined a set of general desirable features for high-voltage dc-dc converters to be used when judging the applicability of each dc-dc converters being considered in this study. Based on the discussion presented in this paper and desirable features defined in section II, the following conclusions are drawn:

1) Semiconductor losses, footprint and initial cost are expected to be decisive factors that determine the viability of all high-voltage dc-dc converters, especially in F2F topologies where semiconductor losses resemble that of the back-to-back HVDC link. On this basis, the Q2L operated CTB-DAB offers the best solution for HVDC applications, because it satisfies the majority of the desirable features drawn in section II.**Error! Reference source not found.** However, its concentrated dc link capacitors are expected to contribute significantly to any dc fault current and this may expose the freewheeling diodes of the converter connected to faulty side and dc switchgears to excessive current stresses.
2) Holistically, the Q2L operated MMC and TAC offer better overall performance during normal and fault conditions (reduced footprint, low losses, and reduced risk to freewheel diodes in the converter connected to a faulty dc side as the distributed cell capacitance in the MMC do not contribute to the dc fault current). This latter dc fault current weakness could be mitigated if their arm inductances be slightly oversized to limit the magnitude of the common-mode currents during dc faults, and their rate of rise. Also, the cell capacitors must be slightly oversized to accommodate short duration active power sinking or sourcing due to mismatch between ac and dc powers as expected during ac network faults, without creating significant overcharge or discharge of the cell capacitors. Additionally, it has been shown the MMC and TAC with trapezoidal modulation increases the power density since most of the significant low-order harmonics contribute to dc power transfer. Also, the main switching devices that bypass the cell capacitors are rated for full load current, but the auxiliary switches (those in series with the cell capacitors) are rated at a fraction of the load current. A Q2L operated MMC, TAC, and CTB DAB present controllable *dv/dt* to both windings of the medium-frequency transformer in the ac link. However the Q2L operated TAC-DAB has smaller semiconductor area than in MMC and CTB DABs, and this may be advantageous in terms of initial cost.
3) Based on the features outlined in section II, it is concluded that both the A2M2C and cascaded two-level converters are less competitive for F2F high-voltage dc-dc converters, because they suffer from relatively high semiconductor losses, and their large concentrated input dc link capacitors tend to increase the current stresses in the dc side switchgear during dc network faults. Also, achieving dc fault blocking at the expense of extra semiconductor losses as in the A2M2C and cascaded two-level converters, is not necessary in F2F dc-dc converters, although it is for the terminal converters of the VSC-HVDC link.
4) Most of the resonant topologies of the dc-dc converters tend to either increase current or voltage stresses of the switching devices. Although this may be tolerable in low-voltage applications, it is not acceptable in high-voltage applications. Generally they are single phase hence introduce large current ripple on both dc links (and possibly discontinuous link current). Thus it is concluded that resonant based dc-dc converters are less likely to be adopted in high-voltage applications.
5) A transformer is necessary for galvanic isolation in F2F dc-dc converter topologies for the following reasons: better switching device utilisation of both converters, and minimises the circulating reactive power in the ac link when the input and output dc link voltages are significantly different (by keeping the per-unit ac voltages VSC_1 and VSC_2 presented to both transformer windings, similar). Without such an isolating transformer, a dc-dc converter with different input and output dc link voltages may suffer from high losses due to excessive reactive power circulation. To avoid this scenario

without using isolation transformer, the converter with higher dc voltage must be under-modulated to keep the magnitudes of the ac voltages applied at both ends of the power transfer inductor between the F2F converters near equal. Such a solution results in poor device utilisation in the converter connected to the higher dc link voltage and higher current in its switches, hence more losses. A transformer may be necessary when connecting to existing HVDC links where established filter grounding arrangement dictate connection isolation.

6) Among the auto dc transformer topologies considered in this study, the asymmetrical partially isolated dc modular auto transformer proposed in [118] offers an efficient solution for dc voltage matching and tapping in multi-terminal HVDC networks (reduced transformer MVA rating and better switching device utilization). However, it requires FB cells in the outer arms, instead of HB cells, to prevent dc fault propagation from one side to the other, and it exposes both windings of the coupling transformer to high voltage stresses of $\frac{1}{2}(V_{dc1}+V_{dc2})$ and $\frac{1}{2}\ V_{dc2}$ respectively. Type 2 of non-isolated hybrid cascaded series two-level auto-dc transformer proposed in [120] provides an interesting method for voltage matching and tapping in multi-terminal HVDC networks without the use of coupling transformer. Its main weaknesses are: requires a large number of semiconductor valves in a conduction path (indication of high losses); and discharge of the dc link capacitor at the dc terminal of the two-level converter stage during a dc fault (at the two-level converter side) may expose freewheeling diodes of the two-level converter stage to high current stresses.

V. Acknowledgment

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VI. References

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