Low-inductance snubber arrays for high-power, high-bandwidth switch-mode amplifiers

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Abstract—This paper presents a low inductance snubber design incorporating a damped DC bus capacitance and multiple RC-RCD cells arranged in two arrays. The design suppresses transient over-voltage peaks seen at the switching transitions in hard-switched, high-frequency switch-mode circuits which are created by an unavoidable interaction between circuit parasitic inductances, IGBT turn-off current slopes and free-wheeling diode reverse recovery currents. The array arrangement allows the use of small surface-mount, ultrafast diodes by enforcing current sharing between many devices. An industrial application example is presented where the snubber design enables an increase in DC bus voltage from 200V to 400V when using 600V Si IGBTs operated at a switching frequency of 75 kHz. Simulation results are presented and compared to experimental measurements to illustrate the operating principle and effectiveness of the array design.

Index Terms—IGBT modules, snubbers, parasitic inductances, switching transients, switched mode power supplies, surface mounting, RC circuits.

I. INTRODUCTION

Some applications of switch-mode power electronic converters are constrained to operate at very high switching frequencies beyond that which is normally considered optimal for power conversion or machine-drive applications. In these applications, the inevitably higher semiconductor device switching losses are accepted in order to obtain other benefits resulting from high switching frequencies, for example high signal bandwidth or a minimum passive component size [1], [2]. The upper limit on switching frequency depends typically on one of two considerations: Hard-switched circuits suffer significant switching loss which scales linearly with switching frequency, therefore, as switching frequency is increased, the thermal dissipation capability of the semiconductor devices may be exceeded, or some minimum acceptable system efficiency figure will be reached. Alternatively, and especially for switch-mode power electronic circuits rated above a few kilowatts and targeting switching frequencies >50 kHz, circuit parasitic inductances can create large over-voltage stress across the switching devices [3]. This is because high switching frequencies imply high $V = L \frac{di}{dt}$ switching transitions, and this must be factored into the device voltage headroom to ensure circuit reliability. Parasitic inductances may be minimized through careful bus bar design [4], [5] and the use of low ESL DC bus capacitors but can never be entirely eliminated. The simple engineering solutions of employing devices with a higher voltage rating and/or of deliberately slowing down the switching process to limit $di/dt$ both tend to increase losses. This is because higher voltage devices incur increased conduction losses (due to a higher on-state voltage drop) and artificially slow switching speeds increase switching losses. In addition, higher voltage devices are more expensive and may require a specialized power module design. In conclusion, designs intended to operate at very high switching frequencies, parasitic inductances can become a major limiting factor preventing economic increases in power output.

Application examples that require operation at very high switching frequencies are the high-bandwidth high-power industrial amplifiers used in vibration testing systems and current control systems for MRI scanners. Such systems must typically be capable of providing a flat frequency response from DC to 5 kHz, at an output of around 20kVA. Switch-mode designs are preferred due to their high efficiency, however, to satisfy THD limits and accurately reproduce the reference waveform, switching frequencies approaching 100 kHz are typically employed which is at the edge of that achievable using current standard large silicon IGBT devices. At the switching transitions, current transfer rates of over 1000 A/µs is common. This is necessary to reduce IGBT switching losses by limiting the time the IGBTs spend in the partially-on state. However, the resultant voltage transients produced across circuit parasitic inductance can necessitate a very significant DC bus voltage derating to stay within the safe operating area of all devices. Voltage stress is often most severe across the opposing freewheel diode at IGBT turn-on. This is due to the $di/dt$ of the decaying reverse recovery current just after voltage is recovered across the diode. This so-called ‘snap’ of the diode can produce a large voltage across the DC bus interconnection inductance which constructively adds to the static DC bus voltage. If large enough, this voltage will cause the power devices to break down and result in an uncontrolled short circuit current and the destruction of the diode and IGBT.

Snubbers are a class of circuit that are used to control and reduce over-voltages seen by a switching device at turn-on and turn-off. Careful application of snubber circuits can effectively increase the maximum usable current and voltage of the IGBTs, particularly in hard-switched circuits. Snubbers can...
allow the use of a lower device voltage rating than would otherwise be possible, or allow a retrofit opportunity to increase the operating voltage of an existing design. Snubbers also tend to limit the occurrence of sustained high-frequency current and voltage oscillations at the switching transitions, resulting in reduced EMI potential [6].

Snubber circuits can be classified as active or passive types. Active snubber circuits [7] need additional auxiliary switch and complex control mechanisms to perform the snubber action. Passive snubber circuits [8] use resistors, capacitors and diodes only and require no external control mechanism. Passive snubbers are often preferred due to their simple and reliable operation. The use of diode clamps and basic series and shunt snubber action are described in [9] and the design methods for selecting optimum component values in RC (Resistor-Capacitor) snubber circuits with an aim to minimize the device peak voltage and power losses are discussed in [10]. RCD (Resistor-Capacitor-Diode) snubbers with snubber capacitor energy recovery schemes are reported in [11], [12] and two different configurations of RCD snubbers for high current IGBTs are described in [13]. The work [14] reports a dynamic current sharing snubber for parallel connected IGBTs in high power applications.

II. A LOW-INDUCTANCE SNUBBER ARRAY DESIGN

The snubber circuit proposed in this paper and its intended placement between the supply and power module is shown in Fig. 1. The corresponding physical layout of the snubber and its mounting on the power module is shown in Fig. 2. The snubber design is a combination of a damped DC bus capacitance, a passive RC snubber and a passive RCD clamp. The RC snubbers and RCD clamps are referred to as snubber arrays composed of cells in which the corresponding cell components are labeled with the subscript suffix 1-6 in Fig. 1.

![Fig. 1. Schematic diagram of proposed array-based snubber connected to a power module showing major parasitic inductances](image1)

![Fig. 2a. Array-based snubber mounted on the power module. The top of the snubber PCB is visible, showing R_x and C_{DC}](image2a)

![Fig. 2b. Bottom side of the array-based snubber PCB showing two RC +RCD snubber arrays composed of six cells each](image2b)
A. PCB layout and component selection

A snubber must be of very low inductance itself in order to have a maximum effect in reducing peak voltages generated by other circuit parasitic inductances [15], [16]. This may be illustrated by noting that an inductance of only 50 nH will cause a voltage drop of 125 V when exposed to a 40 ns, 100 A switching edge. Given that a standard TO220 package lead has an inductance of about 10 nH alone, it is clear that a snubber composed of multiple leaded components is fundamentally limited in the clamping effect it can achieve. To obtain the lowest possible inductance and maximum clamping effect, a snubber should employ surface mount devices (SMD) and be mounted as close as physically possible to the semiconductor devices to be protected. Assuming a typical IGBT power module which is cooled on one side with electrical connections made on the opposing side, a snubber constructed on a PCB of the same footprint as the module and using the same connection pattern allows a close connection directly to the module, thus minimizing the parasitic inductance appearing between the snubber and the IGBT and providing maximum voltage clamping efficacy. This type of arrangement is shown in Fig. 2.a.

The use of multiple physically small diodes in the RCD clamps is advantageous for four reasons. Firstly, small surface mount diodes in the 3-10 A range are commonly available and are low-cost due to their small silicon area and high manufacturing yields. Secondly, the effective ‘spreading’ of a total silicon area over many parallel paths leads to a reduction in overall interconnection inductance below that achievable for a single large-area device. Thirdly, the spreading effect is also advantageous in terms of the thermal design as system heat output is dissipated over a larger heatsink area. Fourthly, physically small devices can be expected to have good internal current density uniformity when compared to larger devices. This may be expected to improve overall robustness as long as current sharing between diodes can be ensured. However, it cannot be assumed that direct-connected paralleled diodes will share current equally due to variations between individual diode die and in path resistances and inductances. For this reason the snubber array arrangement of Fig. 1 and Fig. 2.b is introduced to enforce current sharing between several separate diode paths. Current sharing between cells of the array is discussed in Section III.B.

B. Damped DC bus capacitance

High power switch-mode circuits normally employ a low-inductance laminated bus bar design connecting the power module to a large electrolytic or film capacitor bank. However, the physical separation between the power module and the main DC bus capacitors produce an unavoidable parasitic inductance of the order 70 nH (this is represented by $L_{\text{pdc}}$ and $L_{\text{n dc}}$ in Fig. 1). This is enough inductance to cause significant over voltages and ringing at turn-on and turn-off for many cycles when no snubber is in place. To counter this effect, a small localized DC bus capacitance $C_{\text{DC}}$ may be incorporated on one side of the snubber PCB, along with a damping resistance $R_{\text{DC}}$, which should be tuned to provide critical damping of the resulting resonant LC circuit now formed by the loop composed of the main DC bus capacitance ($C_{\text{DC}}$ in Fig. 1) and $L_{\text{pdc}}$, $L_{\text{n dc}}$ and $C_{\text{DC}}$. The parasitic inductance ($L_p$ and $L_n$ in Fig. 1) present between the power module and the snubber should be minimized to ensure effectiveness of this additional DC bus capacitance. The internal parasitic inductance of the snubber may be minimized by constructing the bulk capacitance from many surface mount devices connected in parallel as shown in Fig. 2.a. The peak power dissipation of the damping resistance can be very high (approaching the system VA rating) and, especially for high switching frequencies, the average power dissipation will be significant. Again, the use of many SMD resistors in parallel will keep parasitic inductance low and will also provide a large surface area for heat removal, keeping component temperatures within limits.

C. RC+RCD snubber cells

The voltage oscillations seen at the center terminal of the half-bridge at turn-on and turn-off can be controlled by an RC snubber or RCD clamp [13]. For a given capacitance value, the RCD clamp produces much lower power losses when compared to the RC snubber because the snubber capacitance is not fully charged and discharged on every switching cycle. At high switching frequencies the power dissipation of an RC snubber quickly becomes prohibitive. The additional IGBT stresses caused by the discharge current of the RC snubber at switch-on are also unwelcome. However, the RC snubber has the advantage of virtually instantaneous operation because there is no turn-on delay associated with a diode (as there is in the RCD clamp). This is particularly relevant when considering very high switching frequencies because the turn on delay of the snubber diode can approach that of the current commutation time, making the RCD clamp ineffective at controlling peak voltages.

A parallel combination of a small-value RC snubber and an RCD clamp can serve to combine the advantages of both types, allowing to the control of the initial overvoltage without incurring excessive power losses [17]. Effectively, the RC snubber provides the initial current path while the RCD clamp transitions into conduction to provide the main current path for the remainder of the commutation time. In the circuit of Fig. 1, the RC snubber is formed by the series connection of $C_{\text{Snr}}$ and $C_{\text{Ln}}$, where $x=A$ or $B$ (depending on placement with respect to the lower or upper device of the power module) and $1 \leq x \leq 6$ (corresponding to the cell number). The capacitances are sized such that $C_{\text{Sn}} >> C_{\text{Snr}}$ and so the effective capacitance of each cell of the RC snubber can be approximated as $C_{\text{Snr}}$. The RCD clamp is formed by the series connection of $D_{\text{on}}$ and $C_{\text{Ldar}}$. The charge transferred to $C_{\text{Ln}}$ and $C_{\text{Sn}}$ during a switching transition is discharged by $R_{\text{Sn}}$ during the time before the next transition.

III. SIMULATION RESULTS

In order to study the operation of the proposed snubber a simplified version of the circuit of Fig. 1 was simulated using the PLECS block set for MATLAB [18]. The PLECS block set uses a behavioral model of IGBTs and diodes (including reverse recovery) which overcomes some of the limitations of standard SPICE models when used in power electronic applications [19]. The simplified circuit used in the simulation to analyse the turn-on and turn-off transients is shown in...
The expanded transition waveforms of the simulated turn-on and turn-off transients are shown in Fig. 4. A step by step discussion of snubber operation with reference to Fig. 4 now follows. Note that $S_A$ refers to the lower RC+RCD snubber array ($D_{DA}, C_{AL}, R_{A}, C_{AS}$) and $S_B$ refers to the upper snubber array ($D_{DB}, C_{BL}, R_{B}, C_{BS}$).

### A. Snubber operation during turn-on and turn-off

The gate pulse turns $Q_A$ on. Current increases approximately linearly in $Q_A$ at the rate of $\frac{dI_{QA}}{dt}$ and so the voltage across $Q_A$ falls by $(\frac{dI_{QA}}{dt})(L_n + L_p)$.

**A to B:** $D_{FB}$ is conducting and so the voltage across $L_c$ is equal to $(\frac{dI_{QA}}{dt})L_p$ causing a current to build in $L_c$. This current flows in the snubber ($I_{SA}$ and $I_{SB}$) and causes the voltage $V_{SA}$ to fall.

**B:** Once $D_{FB}$ reaches peak reverse recovery current, it appears as a current source with a decaying reverse recovery current and the voltage across $Q_A$ rapidly collapses to near-zero.

**B to C:** $C_{AS}$ discharges and $C_{BS}$ charges through $Q_A$ which builds a further current in $L_c$.

**C:** Once the voltage across $C_{AS}$ falls to zero, $S_A$ is forward biased and $C_{AL}$ appears as a virtual short circuit (as it is large).

**C onwards:** Current in $S_B$ rapidly transfers to $S_A$ as $C_{AL} >> C_{BS}$. The reverse recovery current of $D_{FB}$ finishes decaying. The current in $L_n$ and $L_c$ decays to steady state value $I_0$ via $S_A$ (some oscillations occur as stored energy is dissipated in $R_A$ and $R_B$).

**D:** Gate pulse turns $Q_A$ off. Current falls in $Q_A$. As $D_{FB}$ is reverse biased it does not conduct.

**D to E:** Current $I_0 - I_{QA}$ flows in $S_A$ and $S_B$ capacitors, causing the voltage $V_{SA}$ to rise.

**E:** The voltages across $D_{FB}$ and $S_B$ fall to near-zero, $D_{FB}$ and $S_B$ are forward biased.

**E onwards:** Current in $S_A$ rapidly transfers to $S_B$ as $C_{BL} >> C_{AS}$. Current in $D_{FB}$ builds as result of the small positive voltage across $S_B$. The current in $L_p$ and $L_c$ decays to steady state value $I_0$ via $S_A$ (some oscillations occur as stored energy is dissipated in $R_A$ and $R_B$).

### B. Current sharing between snubber array cells

In the preceding discussion, at the instant at which the snubber diode $D_S$ becomes forward biased, current initially flows in $C_{AS}$ and $C_{AL}$. As $C_{AS} << C_{AL}$, the majority of the...
mismatched diodes. For the case where $R_{An}=0$ (effectively $C_{ALn} = \infty$), the effect is demonstrated in Fig. 5 showing two different cases, one representing the designed value of $C_{ALn} = 100 \text{nF}$ and the other case where $R_{An}=0$ (effectively $C_{ALn} = \infty$). The differential cell capacitor voltage is used to illustrate the current sharing arrangement between the cells with mismatched diodes ($\Delta V_{cd} = V_{CAL2} - V_{CAL1}$). For the diode currents $I_{DA1}$ and $I_{DA2}$ corresponding to the case of $C_{ALn} = 100 \text{nF}$, it can be seen that $\Delta V_{cd}$ rapidly builds to approximately 0.63 V to compensate for the different V-I characteristics of the two diodes. As a result of this, the snubber current is shared almost equally between the lower sniper arrays respectively (see Fig. 4. B-C). The losses in the freewheeling diode $D_{IB}$ are lower when the snubber is present because the voltage across the diode is better controlled (i.e. lower) and so the charge transferred during the reverse recovery of the freewheeling diode. When the snubber is present, the apparent DC bus inductance is reduced and so this effect is less pronounced and the losses are higher. In addition, the peak turn-on current carried by $Q_A$ is roughly doubled due to the charging and discharging currents of the upper and lower snubber arrays respectively. The voltage across $Q_A$ rises instantaneously before the current in $Q_A$ begins to fall. With the snubber present, the apparent DC bus inductance is reduced and so this effect is less pronounced and the losses are higher. In conclusion, the array-cell balancing arrangement insures that all diodes conduct a nearly-equal share of the snubber current allowing the snubber to be operated at a total current near to the sum of the forward current ratings of the individual diodes.

C. Circuit losses

A circuit model of Fig. 1 was simulated with a DC bus voltage of 400 V and a load current of 100 A. The peak and average power losses were calculated using the simulated voltage and current waveforms of the power devices and snubber components. The simulation was repeated for the same power circuit operated without a snubber and the resulting power losses are compared in Table II.

Without the snubber, the turn-on losses in $Q_A$ are remarkably low because during the turn-on period a large fraction of the DC bus voltage is dropped across the DC bus parasitic inductance (note that it is this same inductance which causes the large over-voltage peak seen during the reverse recovery of the freewheeling diode). When the snubber is present, the apparent DC bus inductance is reduced and so this effect is less pronounced and the losses are higher. In addition, the peak turn-on current carried by $Q_A$ is roughly doubled due to the charging and discharging currents of the upper and lower snubber arrays respectively. The losses in the freewheeling diode $D_{IB}$ are lower when the snubber is present because the voltage across the diode is better controlled (i.e. lower) and so the charge transferred during the reverse recovery of the diode dissipates less energy.

At turn-off, in the case without the snubber, the voltage across $Q_A$ rises instantaneously before the current in $Q_A$ begins to fall. With the snubber present, the voltage across $Q_A$ rises slowly during the period in which the current rises leading to reduction in the energy dissipated by two thirds. In both cases the switching loss associated with $D_{IB}$ is very small (the forward recovery voltage is below 20 V). Fundamentally, the RC snubbers and RCD clamps are dissipative. $R_{DC}$ provides damping of the LC circuit formed by the DC bus inductance $L_{DC}$, $C_{DC}$ and $C_{DC}$ and therefore the majority of the energy stored in the DC bus inductances is dissipated in $R_{DC}$ at turn-on and turn-off giving rise to a significant power dissipation in $R_{DC}$. Moreover, at $Q_A$ turn-on, the $D_{IB}$ reverse recovery current flows in the DC bus resulting in additional energy dissipated in $R_{DC}$. Dissipation in $R_{A}$ and $R_{B}$ is

<table>
<thead>
<tr>
<th>Components</th>
<th>Without Snubber</th>
<th>With Snubber</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Average (W)</td>
<td>Peak (kW)</td>
</tr>
<tr>
<td>$Q_A$</td>
<td>Turn-on 2.90</td>
<td>1.42</td>
</tr>
<tr>
<td></td>
<td>Turn-off 395</td>
<td>42.4</td>
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<tr>
<td>Conduction</td>
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<td>150</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>548</strong></td>
<td><strong>351</strong></td>
</tr>
<tr>
<td>$D_{IB}$</td>
<td>Turn-on 92.9</td>
<td>80.7</td>
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<tr>
<td>Conduction</td>
<td>103</td>
<td>103</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>196</strong></td>
<td><strong>168</strong></td>
</tr>
<tr>
<td>Snubber</td>
<td>$R_{DC}$</td>
<td>79.3</td>
</tr>
<tr>
<td></td>
<td>$R_A$</td>
<td>50.6</td>
</tr>
<tr>
<td></td>
<td>$R_D$</td>
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</tr>
<tr>
<td></td>
<td>$D_{A}$</td>
<td>6.86</td>
</tr>
<tr>
<td></td>
<td>$D_{B}$</td>
<td>1.83</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>148</td>
<td></td>
</tr>
<tr>
<td>All components total</td>
<td>744</td>
<td>667</td>
</tr>
</tbody>
</table>
R_B is due to the charge transferred to C_{AS}, C_{AL}, C_{BS} and C_{BL} as a result of the voltage clamping action of the snubber. The clamp energy is dissipated slowly in R_A and R_B after the turn-on and turn-off events have occurred. The charge transfer is greatest in the snubber arrays connected across the conducting IGBT and so for the direction of current flow studied here, R_A dissipates significantly more power than R_B. Snubber diode losses are small in comparison to losses elsewhere due to the very low average forward current experienced by these devices.

Although there is significant power dissipation in the snubber components, the total loss figures show that overall losses with the snubber are about 10% lower than without the snubber, principally due to the large reduction in Q_A turn-off losses. The overall power loss occurring in the power module (IGBT plus diode) is reduced by about 30%. In addition, IGBT peak power stress is reduced by about 25% and diode peak power stress is reduced by about 50% which may be advantageous in terms of device reliability. It is clear from the power dissipation figures that the snubber will require thermal management solution itself (the snubber accounts for 22% of overall dissipation). Although overall losses are slightly lower and therefore the complete thermal management solution overall may be of lower capacity, the additional complexity required to manage the snubber dissipation is potentially costly.

IV. EXPERIMENTAL RESULTS

A. Experimental snubber construction details

The physical arrangement of both sides of the snubber PCB and its attachment to the power module is shown in Fig. 2. In the experimental set-up, C_DC was composed of 12 parallel connected 500 V X7R dielectric ceramic capacitors in an 1812 SMD package of 100 nF each (1.2 μF in total). R_DC was composed of 38, 3.3 Ω thick film resistors in a 1218 SMD package, connected as two series banks of 19 resistors in parallel (0.347 Ω in total).

The RC+RCD snubber arrays were composed of six cells for each device (i.e. 12 cells for each half-bridge power module). The cell diodes are STTH3R06S, SMC package, rated at 600V, 3A with t_{tr}=35ns. R_m is constructed from two 10 Ω, 1218 package resistors connected in parallel. Values for other components are given in Table I.

The large number of individual components serves two purposes, it reduces the effective inductance (roughly proportional to 1/N, where N is the number of paralleled devices), but also limits the current density and therefore the power loss density to within acceptable limits. This is particularly important in the case of R_DC which suffers both high average losses and high peak losses.

B. Comparison with simulation

Fig. 6 shows a comparison of experimental and simulation results for the operation at a DC bus voltage of 400 V rms current of 100 A. Note that the voltages measured correspond to the ‘external’ voltages at the terminals of the snubber, i.e. V_{SA} and V_{DC} in Fig. 3. There is generally good agreement between the voltages waveforms, with the exception of pulse

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**Fig. 6.** Comparison of simulation and experimental results for the array snubber (400 V/100 A) clamp employing leaded (through-hole) components to damp radio-frequency oscillations that were otherwise observed to persist for several tens of cycles at each switching edge. Although somewhat effective at damping these oscillations, initial peak device voltages of 340 V were observed at the terminal of the device when delivering 100 A load current from a 200 Vdc supply. Internal device voltages are likely to be 10-20% higher due to additional internal parasitic inductances, but these voltages cannot be measured routinely due to the module encapsulation. When increasing the DC bus voltage to 350 Vdc, intermittent failure of the IGBT modules was observed. For long-term reliable operation, a DC bus...
voltage of about 300 Vdc proved to be the upper limit for these IGBT modules operated with the leaded RCD clamp. This is a typical example of the large derating necessary to ensure safe operation of a semiconductor device operating at very high switching speeds (a 600 V device used in a 200 Vdc bus equates to a voltage derating of 67%).

A design challenge was set to extend the amplifier supply voltage to 400 Vdc at the same current ratings, allowing a 100% increase in the rated power output of system. This was to be achieved without changing the design of the power module or power circuit design but instead by improving on the existing snubber design so that the peak overvoltage experienced by the module was kept below the rating of 600 V.

D. Comparison with alternative circuit options

To investigate the comparative effectiveness of the proposed snubber design, additional experiments were performed for three different cases, the first corresponding to operation with no snubber, the second to the existing snubber design based on Through Hole (TH) components and the third case to the proposed low inductance array snubber.

A comparison using a DC bus voltage of 200 V with a load current of 100 A is shown in Fig. 7. In the ‘without snubber’ case, the bridge output voltage (V_{SA}) has very large over-voltages and ringing at both switch on and switch off for many cycles due to the interaction of the power device and circuit parasitic inductances. The presence of a large DC bus parasitic inductance can be observed indirectly via the large voltage drop at the power module terminals at turn-on. An increase in DC bus voltage is not possible as the peak device voltage is over 550 V (the rated voltage of the power module is 600 V). The through-hole snubber suppresses the peak over-voltage but still shows oscillations for many cycles, largely as a result of the inherent inductances of the leaded components used in its construction. This is particularly evident at the instant of freewheeling diode recovery at QA turn-on where a large peak voltage of about 40% of the DC bus voltage is developed. It would be problematic to increase DC bus voltage beyond approximately 300 V due to the magnitude of the over-voltage developed. In the SMA snubber case, the localized DC bus capacitance and action of the RC+RCD snubber is effective at suppressing the over voltage peak at turn-on to less than 10% of the DC bus voltage.

In addition, the clamping effect of the RCD clamp and the damping effect of RDC are effective in suppressing oscillations, resulting in an improved EMI performance.

A further experiment was conducted to observe the effect of the snubber when the system is subject to transient overload conditions. In this case, the load current was increased to 200 A at a DC bus voltage of 400 V, representing a 100% overload condition. The results are shown in Fig. 8 where it can be seen that although there is a significant voltage drop across the power module terminals at turn-on, the overvoltage at turn-off is controlled to within 25% of the DC bus voltage, ensuring the power module continues to operate within its voltage rating.

V. CONCLUSION

The operation of a low-inductance combined RC+RCD snubber has been explored through simulation and verified experimentally. A localized damped DC bus capacitance is used to suppress DC bus over-voltage peaks in combination with an array design concept which enforces current sharing between multiple small SMD diodes, allowing the low parasitic inductance and fast switching performance of these devices to be fully utilized for fast voltage clamping action.

In a practical retrofit industrial application, the snubber design has been shown to be highly effective at suppressing transient over-voltages and sustained oscillations that otherwise occur due to the interaction of fast switching transitions and circuit parasitic inductances. The design is specifically suited to applications requiring very high switching frequencies and therefore subject to fast switching transitions. As an example of what may be achieved, when applied to an existing high-bandwidth amplifier the snubber has allowed the DC bus voltage to be increased from 200 V to 400 V when using a 600 V power module, resulting in a...
doubling in amplifier power handling capability subject only to the relatively low additional cost of the snubber.

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