Advanced Photonic Routing Sub-systems with Efficient Routing Control

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ABSTRACT

In recent years, there has been much interest in the development of optical switches which can route optical signals from different input guides to different outputs based on thermo-optic and electro-optic technologies. Such switches, which can be reconfigured on millisecond and microsecond timescales, have already attracted commercial interest. However switches which are able to reconfigure on the nanosecond timescales required for packet switching have been more challenging and only in recent years, have router concepts been devised to allow lossless routers to be constructed able to switch on nanosecond timescales with more than 16×16 ports. This paper will therefore review the advances that have occurred to allow such operation and then describe recent studies that have begun to determine the electronic control and functionality required to enable full and practical operation of such switches in high performance networks.

Keywords: optical switching, packet switches, photonic integrated circuits, routing algorithm

1. INTRODUCTION

The ever-increasing network traffic in both data centres and internet cores is leading to increased demands on network switching capacity and energy consumption. Developing electronic switch technologies to cope with this continually growing bandwidth demand has become increasingly difficult and has led to increasing thermal dissipation [1]. Optical switching circuits, which have been studied in recent years by a number of research groups, are regarded as potential key components to meet future communication routing requirements

Optical switches with millisecond and microsecond reconfiguration time, such as micro-electro-mechanical systems (MEMs) [2] and thermo-optic switches, can be used to route large blocks of data in parallel. 320×320 three-dimensional (3D) MEMs switches with low loss and energy consumption have been reported [3]. Silica-based MZI using thermal-optic effects switches with port counts of up to 32×32 have been demonstrated with very high extinction ratios (55 dB) [4]. However, these devices cannot meet the requirement of packet switches which are able to redirect data in very short packet time-scales.

Semiconductor optical amplifier (SOA) based switches, which are capable of nanosecond-response times, have been the subject of much research. They are able to meet the time response requirement for packet switching. SOAs are now mature gating elements for switching and offer ease of control, low operating voltage, large-scale integration and high ON/OFF extinction ratio. Additionally, forward-biased SOAs offer inherent gain which compensate for the loss caused by passive components. For example, a monolithic active-passive 4×4 switch with booster SOAs has been fabricated with a 3dB gain bandwidth of 25nm [5]. Larger-scale SOA-based switches can be achieved by using multiple-stage architectures. For instance recently, a monolithic 16×16 SOA-based switch has been fabricated using all-active InP/InGaAsP epitaxy with shuffle networks being pumped electrically to avoid loss [6]. The long optically-active paths limit the optical signal-to-noise ratio (OSNR) to 14.5 dB in a 0.1 nm bandwidth and lead to high energy consumption of 1W/path. A further monolithic 16×16 SOA-based switch has been reported by integrating active SOA gates with passive shuffle networks [7]. The shorter active paths involved improve OSNR to 28.3 dB in a 0.1 nm bandwidth and reduce energy consumption to 0.55W/path. This device, however, suffers from around 30dB insertion loss, even with the gain of the three cascading SOAs integral to the switch. Lossless optical switches are regarded as key enabling building blocks for large-scale optical switches. Therefore, this paper focuses on a lossless 8×8 SOA-based switch using active-passive integration.

Small-scale optical switches developed in integrated form are typically implemented using a strictly non-blocking architecture which uses a straightforward control method. However, large-scale optical switches with more than 8x8 ports tend to adopt a rearrangeably non-blocking multi-stage architecture to minimize the number of components required at the expense of needing a more sophisticated routing algorithm. In addition, the path loss in such switches can be significant, requiring SOAs not only to act as gating elements but also compensate with gain for the optical path loss so that overall the switch can be lossless. As a wide variation in path-dependent loss can be present, the path selection of optical signal through the device is thus important. Non-optimized selections of long paths through the switch inevitably lead to unnecessarily large optical losses which require to be compensated by increasing optical gain, at the expense of increased ASE noise and saturation induced patterning which in turn reduces the input power dynamic range (IPDR). The IPDR can thus be minimised by choosing optimised paths through the switch. Several routing algorithms have been developed to set up non-blocking routes [8], reduce the time taken for set-up process [9], and minimise the crosstalk within

the devices [10]. However, to our knowledge, no algorithm has been developed to avoid the unnecessary long paths and improve the IPDR. Therefore, this paper presents a path-selection algorithm which minimises the path-dependent loss and improves the IPDR performance for the worst-case path.

2. LOSSLESS 8X8 SOA SWITCH

A schematic of the 8x8 SOA switch is shown in Fig. 1(a). The device is designed with a three-stage Clos architecture which offers rearrangeably non-blocking connectivity. The input and output switching stages are implemented with 2×2 switching elements while the central stage has two 4×4 switching elements. All switching elements are implemented with a broadcast-and-select configuration using SOA gates. Pre-defined standard building blocks are used to enable the reliable design and fabrication. The switch circuit is fabricated on a multi-project wafer where each photonic integrated circuit (PIC) has a maximum sector size of 4 mm x 6 mm. The limit of chip size requires the layout shown in Fig. 1(a) to be folded to fabricate all elements on the chip. The switch has been fabricated using a generic foundry within the EU FP7 PARADIGM project as shown by the photograph in Fig. 1(b) [11].
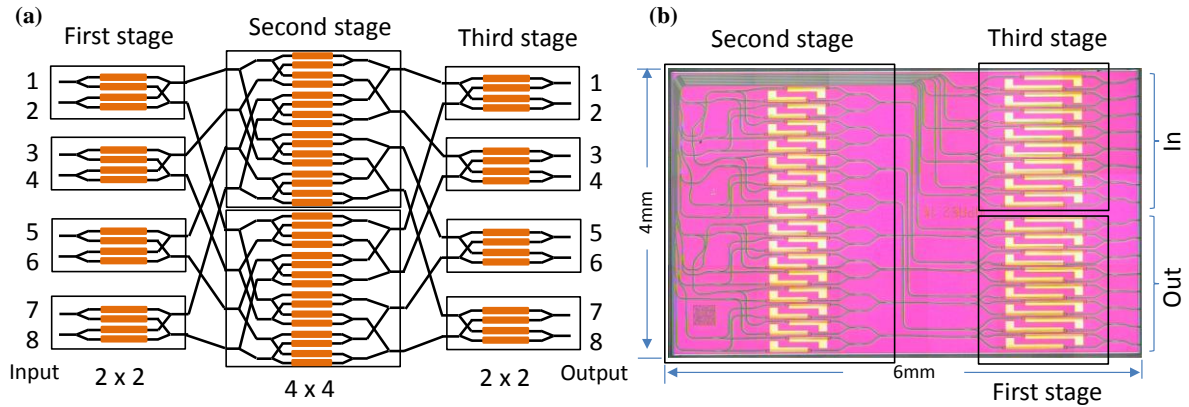

Figure 1: (a) Schematic layout of an 8x8 SOA switch; (b) Photograph of the fabricated 8x8 SOA switch [12]

The input and output ports are placed at the same edge using deep etched passive waveguides with a width of 1.5 µm and pitch of 250 µm. The bend radius of the S-bends and circular bends within the shuffle network is chosen to be 150 µm as a trade-off between bend size and excess loss. The waveguide width is tapered out to 2 µm at the MMI power splitters/combiners and waveguide crossings in order to minimize component excess loss and crosstalk. Shallow-etched 2 µm wide waveguides are used for the SOA sections. A transition element is used between the shuffle networks and the SOAs to match the modes between the deep- and shallow-etched components to minimize reflection. 500 µm long SOAs are chosen for central stage while longer 750 µm SOA gates are used at the input and output stages to compensate the losses from the shuffle networks.
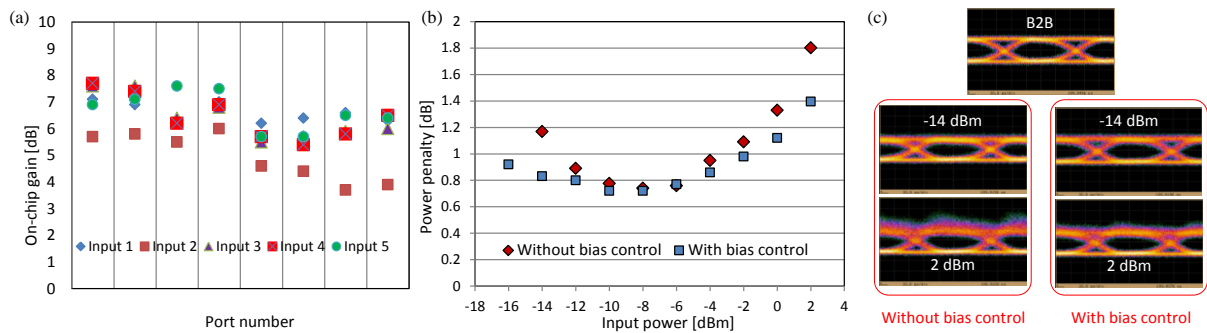

Figure 2: (a) Measured on-chip gain for 40 optical paths; (b) Power penalty vs. optical input powers with and without bias control; (c) Eye diagrams of -14 and 2 dBm with and without bias control

The integrated switch is mounted on a thermo-electric cooler and operated at 20 ºC. Lensed fibres are used to couple light in and out the chip, with an estimated coupling loss of 8dB. By determining the material transparency current of the 500 µm and 750 µm long SOAs (7.5 mA and 10 mA), the gain/absorption is found as a function of current. Operating bias currents of 40, 35 and 30 mA for the first-, second- and third-stage SOAs are chosen to achieve an optimum OSNR of 32.9 dB in a 0.1 nm bandwidth for an input power of -6 dBm. The device exhibits on-chip gain for 40 measured paths (input 1-5 to all) as shown in Fig. 2 (a). The gain values for all 40 paths are within 4 dB. Because of that, if we assume the SOA elements offer uniform gain, the variation of the path-dependent loss is also within a range of 4 dB. The differences in length of the passive waveguides and number of bends and crossings contribute to the path-dependent loss.

Dynamic characterization of the switch has been performed with an optical input generated by a tuneable laser which is modulated by a Mach-Zehnder modulator driven by a 10 Gb/s 2^{31}-1 pattern length PRBS. Figure 2(a) [red diamonds] shows an IPDR of 9.5 dB for a 1 dB power penalty on the path Input 1 – Output 8. The active power monitoring and bias control can be implemented to extend the IPDR for multi-stage SOA networks [13]. With optimum bias current in the range from 30 – 50 mA applied to the first-stage SOA, the IPDR is extended to 14.5 dB within 1dB penalty as shown in Fig. 2(b) [blue diamonds]. The eye diagrams for measurements with and without bias control are shown in Fig. 2(b).

3. PATH-SELECTION ROUTING ALGORITHM

The path-dependent loss and IPDR can be improved by adopting a routing algorithm to choose optimized paths through the switch. In this paper, an 8x8 port Clos-tree is used as an illustrative example as shown in Fig. 3. When all inputs of the switch map to distinct outputs (a fully connected state), each path can be set up via one of two centre-stage 4x4 switching element using the classical looping algorithm [8], as shown in Fig. 3(a). The bold path suffers the greatest unamplified path loss of 34.5 dB owing to the long passive waveguide, bends, crossings and splitters/combiners [11]. The high-level path loss thus must be compensated by an increased optical gain from cascaded SOAs, at the expense of increased ASE noise and increased saturation induced patterning which in turn reduces the IPDR. A better choice of routes can improve the IPDR.
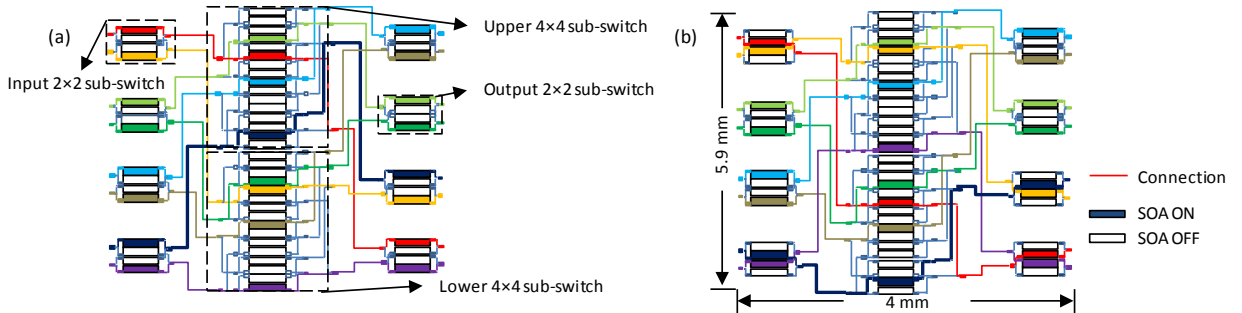

Figure 3: Fully utilized 8x8 switch set-up. Path allocations are shown adopting (a) the classical looping algorithm (the connection shown by the bold line suffers the greatest path loss) (b) the path-selection algorithm (the maximum loss is much reduced)

The connection between each input and output is set up via either the upper or lower centre-stage 4x4 switching elements. The looping algorithm attempts to first connect a path via the upper switching element; if not available it chooses the lower switching element [8]. This process continues looping until all paths are assigned with centre-stage switching elements. The looping algorithm was designed in this way because it was developed for setting up electronic switches which assumes the loss for all pathsis equal. However, it produces paths with unnecessarily large loss variation in optical switches as well as the possibility of a large loss path being chosen.

Here we modify the looping algorithm to attempt both upper and lower centre-stage switching when available to generate all possible permutations for a given fully connected state. The best setup is selected from these permutations according to a specific weighting mechanism. It is possible to consider a number of different options, such as accepting an outcome if the maximum unamplified path loss is below a threshold value, computing the root mean square path loss for all permutations and selecting the lowest outcome, or examining the maximum individual path loss in each permutation and selecting the outcome which has the lower overall individual maximum path loss. The last mechanism has been adopted to avoid paths with unnecessarily large loss, as shown in Fig. 3(b).

The number of total permutations that must be considered and compared for a fully connected state is 2^L, where L is the number of loops to establish the connections. Therefore, the routing control plane would require a high-speed processor if on-the-fly computing were used. If we compute the path selection algorithm once for each possible state and store its outcome in a look-up table, the fast switch reconfiguration can be enabled but a significant large-size look-up table is required as 8! = 40320 possible states are needed for an 8x8 switch. However, there are only 282 unique connected states between the outer-bank 2×2 switching elements and the centre-bank 4×4 switching elements [14]. Therefore, the look-up table can be reduced to a practical size.

Figure 4(a) shows the loss improvement of maximum individual path loss for all 282 fully connected states. Although most states do not exhibit a significant loss improvement, eight states have a significant loss reduction of 2.7 dB. The IPDR improvement is simulated by using one of the eight examples [Fig. 3] with photonic simulation software VPI. 10 Gb/s PRBS optical input signal and a 30 mA bias current for each SOA gate are simulated. The loss and IPDR for each path with and without the algorithm are shown in Fig. 4(b). The IPDR of the path with overall individual maximum loss increases by 1.9 dB for penalties less than 1.5 dB. The variation of IPDRs for all paths is within 0.4 dB.
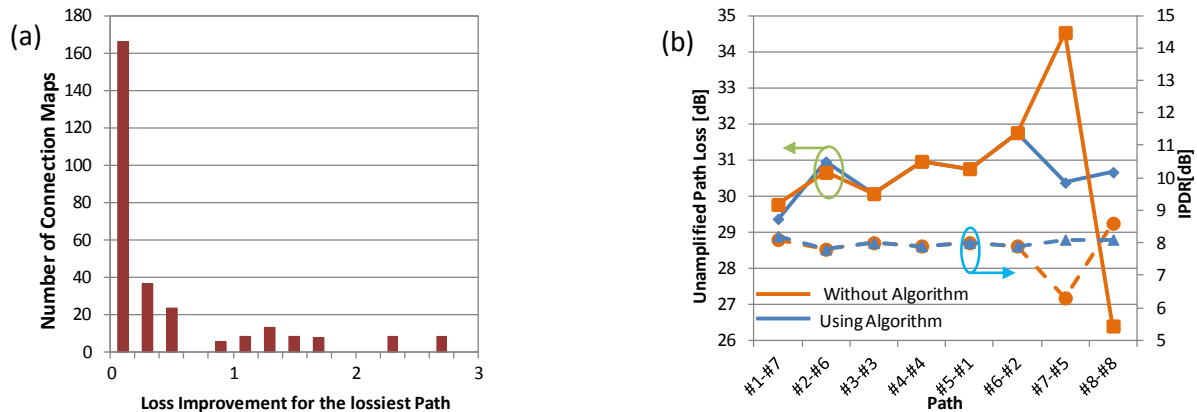
Figure 4 (a) Loss Improvement of the lossiest path by using the path selection algorithm for all fully connected states (b) Loss and IPDR of each path for the set of connections shown in Fig.3

4. CONCLUSIONS

After reviewing the field, this paper describes a lossless 8×8 SOA switch using active-passive integration. An IPDR of 14.5 dB for 1 dB power penalty is achieved with the bias control techniques. An intelligent path-selection algorithm is also presented to optimise path-dependent loss and IPDR performance. The modelling of a general 8x8 Clos-tree switch shows a loss reduction of 2.7 dB and IPDR extension of 1.9 dB for the worst case. The algorithm can be run once and its outcome is stored in a compact look-up table to realise fast switch reconfiguration. The large-scale rearrangeably non-blocking switches with more than 16×16 ports can be constructed recursively using Clos-tree architecture. This algorithm can be implemented recursively from the outer stages of switches to central sub-networks to set-up the optimised routes which is very promising for the future networks with large-scale optical switches.

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