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Enhanced Phase-Shifted PWM Carrier Disposition for Interleaved Voltage Source Inverters

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***Abstract*—This letter presents a novel implementation of pulse-width modulation (PWM) that improves the quality of the line-to-line output voltages in interleaved multi-phase voltage source inverters (VSIs). In multi-phase VSIs with *n* interleaved parallel-connected legs, the best single-phase output voltage is achieved when the carriers are evenly phase shifted. However, switching among non adjacent levels can be observed at regular intervals in the line-to-line voltages, causing bad harmonic performance. With the proposed method, switching in the line-to-line voltages happens exclusively between adjacent levels. The modulator utilizes two sets of *n* evenly phase-shifted carriers that are dynamically allocated. Because of its generality, the proposed implementation is valid for any number of phases and any number of legs in parallel. A Matlab/Simulink model has been set up for simulation purposes. Selected experimental results obtained from a three-phase VSI made up with two and three legs in parallel per phase are reported, confirming the enhancement attained with the proposed implementation.**

***Index Terms*—Voltage-source inverter, legs connected in parallel, interleaving, pulsewidth modulation.**

I. Introduction

VOLTAGE source inverters (VSI) with legs connected in parallel (see Fig. 1) are widely used when high output currents are to be achieved, thus increasing the overall output power [1]–[3]. Inductors are the passive components used to connect several phase legs in parallel [4]–[7]. They not only limit circulating currents among the phase legs but also qualify for averaging the voltage from the legs to form the output voltage. If interleaving is used, the Thevenin equivalent output voltage of a phase with *n* legs connected in parallel has *n*+1 levels, because of the averaging effect.

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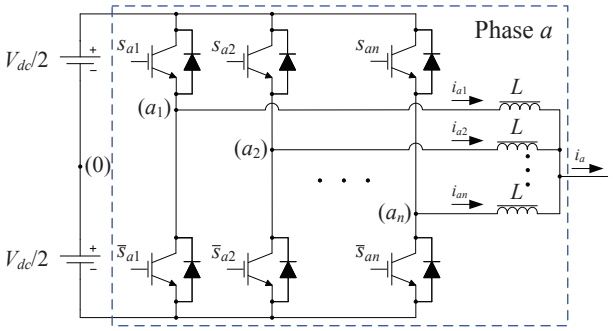

Fig. 1. One phase of a VSI incorporating *n* legs connected in parallel.

Different methods to set the instantaneous output voltage level can be used, including space vector modulation (SVM) or carrier-based pulse-width modulation (CB-PWM). The effect on their harmonic spectra has been largely investigated [8]–[12]. In CB-PWM, the use of as many carriers as legs are connected in parallel is the standard procedure if interleaving is to be implemented. In an interleaved phase-shifted PWM (PS-PWM) scheme, all the carriers have the same frequency and amplitude (usually ranging from -1 to +1 per unit) and are evenly phase-shifted within a switching period. Each carrier is associated with a specific leg. In level-shifted PWM (LS-PWM) schemes, *n* triangular carriers with the same frequency and $2/n$ peak-to-peak value are arranged in contiguous zones to fully occupy the range from -1 to +1. Depending on the relative phase relationship among the carriers, different PWM strategies are commonly referenced. The most popular one is phase-disposition PWM (PD-PWM) [9].

In multilevel inverters, a PD-PWM scheme provides line-to-line voltages where switching happens only between adjacent levels. However, LS-PWM techniques, such as PD-PWM, cannot be applied without modification in converters with legs connected in parallel. If each carrier were associated with one leg, only the leg associated with the carrier in the zone where the reference signal was, would be switching. The remaining *n*-1 legs would be clamped to either the positive or the negative dc-link voltage, depending on the relative position of their reference signal. This process would create dc-voltage components across the inductors and produce extremely large circulating currents.

This paper proposes a new PS-PWM implementation for interleaved multi-phase VSIs where switching in the line-to-line voltages happens exclusively between adjacent levels. As a consequence, the proposed modulator improves the quality

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of the line-to-line output voltages when compared to the conventional PS-PWM implementation. For a VSI with *n* legs in parallel, the modulator utilizes two sets of *n* evenly phase-shifted carriers that are dynamically allocated. Because of its generality, the proposed implementation can be applied to VSIs with any number of phases and any number of legs connected in parallel.

The rest of the letter is organized as follows. First, the concept of interleaved PS-PWM is reviewed in Section II. Then, the implementation of the proposed modulation scheme is presented in Section III. Simulation and experimental results that illustrate the improvements achieved in terms of total harmonic distortion (THD) and waveform quality in the line-to-line voltages are given in Section IV. Finally, conclusions from this work are presented in Section V.

II. Interleaved Phase-Shifted PWM

The interleaving technique is applied to VSIs with legs in parallel to achieve an apparent switching frequency *n* times higher than the individual switching frequency of each leg [6]. When operating with a CB-PWM this is achieved by using *n* evenly phase-shifted carriers. Since there are *n* legs connected in parallel per phase, the Thevenin-equivalent output voltage of the *y*-phase becomes

$$v_y = \frac{1}{n}\sum_{x=1}^{n} v_{yx}, \tag{1}$$

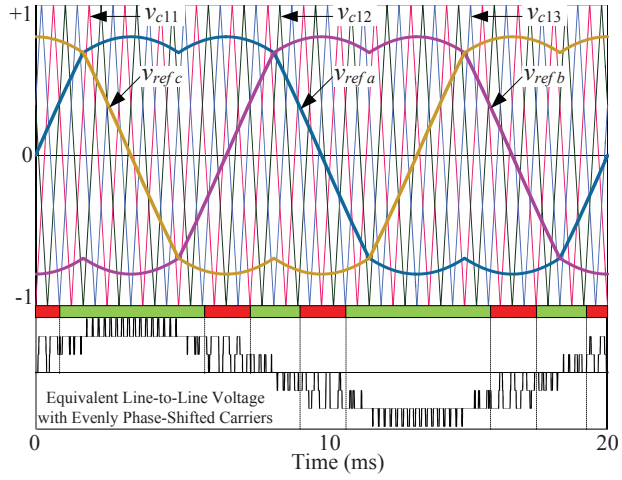
due to the averaging effect of the parallel connection. The equivalent line-to-line voltage is the difference between the equivalent output voltage of two phases.

Fig. 2(a) illustrates the case of a three-phase VSI with three legs in parallel per phase. The phase angles for the three carriers used (v_{c11}, v_{c12}, and v_{c13}) are 0°, 120°, and 240°, respectively. The reference signals (v_{refa}, v_{refb}, and v_{refc}) are compared to their respective carrier signal to set the on-off state of the switches. In order to further extend the range of the linear modulation index (m_a) up to 1.15, the offset voltage

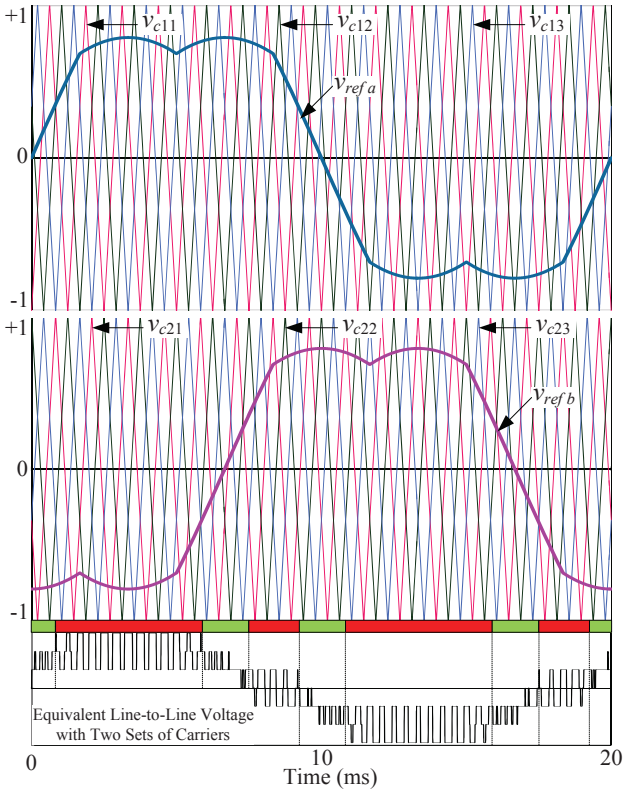
$$v_{offset} = -\frac{max(v_{refa}, v_{refb}, v_{refc}) + min(v_{refa}, v_{refb}, v_{refc})}{2} \tag{2}$$

is added as a zero sequence component to the three-phase references. The same equivalent output voltages as if centered SVM was used are obtained [13].

Although the use of a set of evenly shifted carriers yields the best attainable single-phase output voltage in terms of THD, that is not the case for line-to-line output voltages [8]. From the equivalent line-to-line voltage in Fig. 2(a), it can be observed that during certain intervals there is switching among three adjacent levels, thus worsening the overall THD and with negative implications in terms of electromagnetic interference on account of bigger voltage steps. The use of a different, but also evenly phase-shifted, set of carriers does not fix that. But if two different sets of carriers are used to modulate two different phases, the periods of time where three-level switching in the line-to-line voltages is observed, vary. Fig. 2(b) depicts the results obtained for the aforementioned VSI if v_{refa} is modulated by means of the first set of carriers,



(a)



(b)

Fig. 2. Voltage references, set of carriers, and Thevenin-equivalent line-to-line output voltage (v_{ab}) for a three-phase VSI with three legs connected in parallel for m_a= 0.8 and f_c= 800Hz: (a) one set of carriers and (b) two sets of carriers.

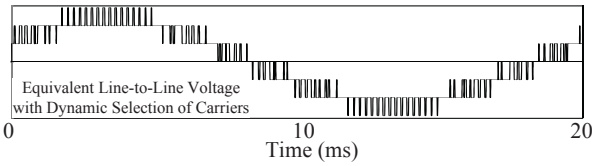


Fig. 3. Line-to-line voltage waveform for a three-phase VSI with three legs in parallel per phase achieved when using a dynamic assignment of carriers.

i.e. v_{c11}, v_{c12}, and v_{c13}, and v_{refb} is modulated by means

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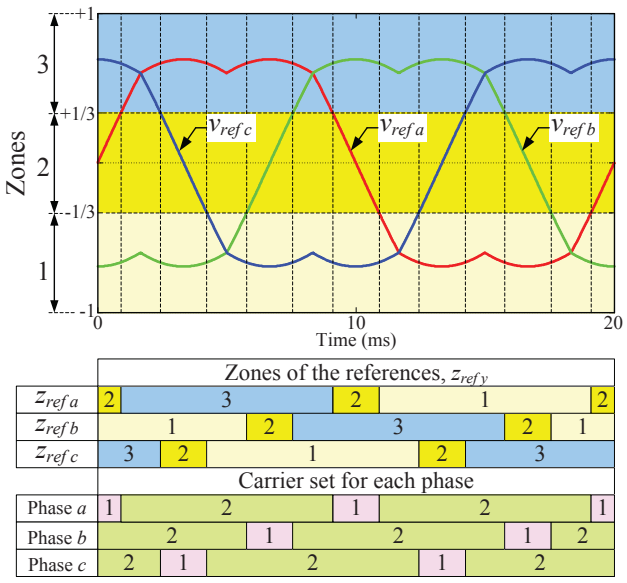

Fig. 4. Single-phase voltage reference zones and carrier set allocation for a three-phase three-paralleled-leg VSI.

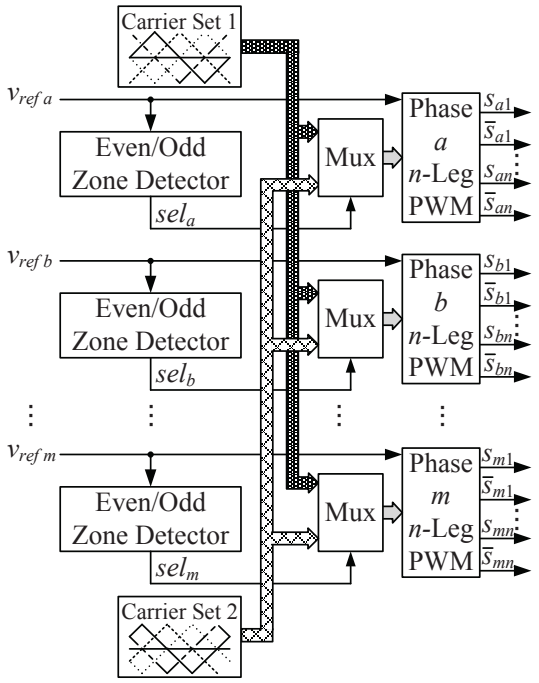

Fig. 5. Generalized *m*-phase *n*-leg modulator diagram.

of a second set of carriers, i.e. v_{c21}, v_{c22}, and v_{c23}, whose respective angle phases are 60°, 180°, and 300°.

Upon scrutinizing the examples shown in Fig. 2, one can conclude that those intervals of two-level and three-level switching, when using one or another set of carriers, are fully complementary. As a consequence, line-to-line output voltages with switching only happening between adjacent levels are achievable with a dynamic selection of the appropriate set of carriers, as can be seen in Fig. 3. The proposed implementation is described in Section III.

III. Enhanced Modulator

The new modulator requires the use of two sets of carriers. For the general case of *n* legs connected in parallel per phase, carrier Set 1 is made up of *n* phase-shifted carriers (v_{c11}, v_{c12}, ..., and v_{c1n}) with a relative phase shift of $360°/n$. A second set of carriers (v_{c21}, v_{c22}, ..., and v_{c2n}) —Set 2— is also evenly phase shifted, but the whole set is phase-shifted by $360°/(2n)$ with regards to Set 1. Table I shows the relative phase-shifting among the carriers. The phase shift depends on the number of carriers, i.e. the number of legs in parallel.

The carrier set selection is dynamically assessed depending on the instantaneous value of the modulating reference signals ($v_{ref\,a}$, $v_{ref\,b}$, ..., and $v_{ref\,m}$). For that purpose, and considering linear modulation, the carrier/reference signal domain (which ranges from -1 to +1) is broken down into *n* equally sized zones of $2/n$ peak-to-peak value that are numbered upwards as it is shown in Fig. 4. In order to quantize them, the following expression is used:

$$z_{ref\,y} = 1 + \left\lfloor \frac{1 + v_{ref\,y}}{\frac{2}{n}} \right\rfloor \quad \text{for} \quad y = \{a, b, ..., m\}, \qquad (3)$$

where $z_{ref\,y}$ variables can take values from 1 to *n*.

Fig. 5 shows a block diagram of the proposed modulator for m phases and *n* legs per phase. The modulators for each phase

TABLE I
Phase Shift of the Two Sets of Carriers

Number of carriers	Carriers' Phase Shift (°)	
	Set 1	Set 2
2	0, 180	90, 270
3	0, 120, 240	60, 180, 300
4	0, 90, 180, 270	45, 135, 225, 315
n	$360\left(0, \frac{1}{n}, \ldots, \frac{n-1}{n}\right)$	$360\left(\frac{1}{2n}, \frac{3}{2n}, \ldots, \frac{2n-1}{2n}\right)$

use either Set 1 or Set 2 depending on the position of their reference signals. The Even/Odd Zone Detectors pinpoint the zones where the reference signals are, and generate the $z_{ref\,a}$, $z_{ref\,b}$, ..., and $z_{ref\,m}$ signals. The Even/Odd Zone Detectors also assess the parity of the $z_{ref\,y}$ signals and generate the sel_y selection signals according to:

$$sel_y = mod[z_{ref\,y}, 2] \quad \text{for} \quad y = \{a, b, ..., m\}. \qquad (4)$$

Depending whether a phase reference signal lies within an even or an odd zone, its modulation is carried out by means of one or another set of carriers, respectively. For the example considered in Fig. 4, Set 1 is assigned to even zones and Set 2 to odd zones. Those sel_y signals control the multiplexers that route one or another set of carriers to the PWM blocks that, ultimately, set the on-off state of the VSI switches.

IV. Simulation and Experimental Results

A. Simulation Results

The proposed modulator has been simulated on three- and four-phase Matlab-Simulink models with up to five legs in parallel per phase. Fig. 3 depicts the line-to-line voltage waveform for a three-phase three-leg VSI. The THD values for a three-phase inverter, with a switching frequency of 3 kHz, and considering the first 2000 harmonics have been computed

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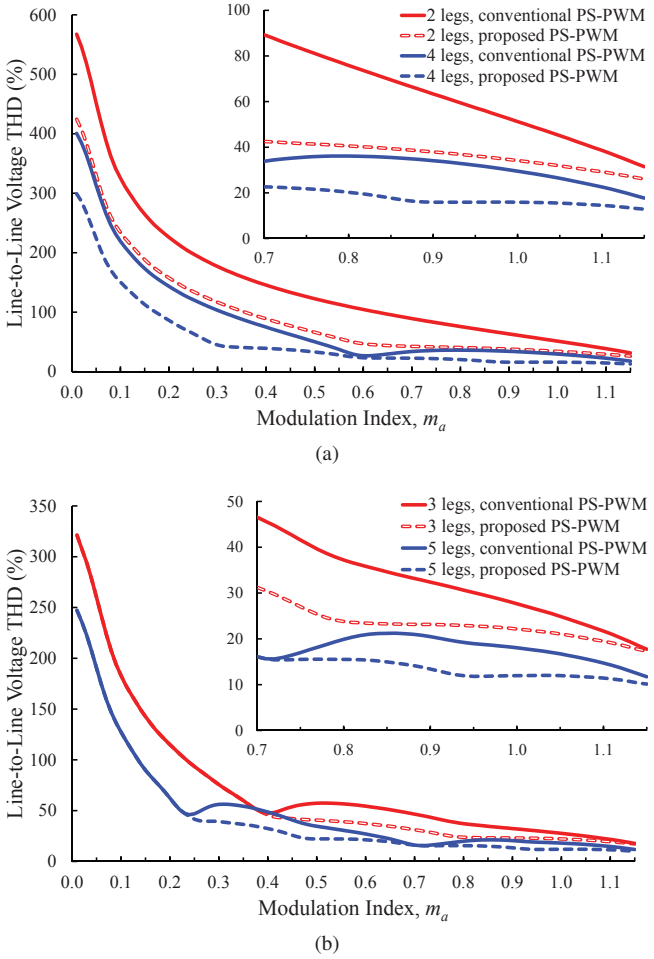

Fig. 6. Line-to-line THD vs. modulation index for: (a) 2 and 4 legs in parallel, and (b) 3 and 5 legs in parallel.

and plotted in Fig. 6. It can be seen that for an odd number of legs, i.e. an odd number of zones, the improvement in the THD is only achieved if the reference signal exceeds the central zone, e.g. $m_a > 1/n$.

B. Experimental Results

A three-phase modulator has been implemented on a dSpace DS1103 PPC Controller board and tested on a laboratory prototype. There are two three-phase VSIs in the lab, which leaves up to six legs available for different connections. Two different configurations have been studied: (i) a full three-phase VSI with two legs in parallel per phase, and (ii) the implementation of phases *a* and *b* of a VSI with three legs per phase. Nevertheless, those two phases are modulated as if a full three-phase system had been implemented. The parameters that are common for both configurations are: dc bus voltage V_{dc}= 48V, carrier frequency f_c= 2kHz, inductors L= 6mH, and Wye-connected load resistors R= 10Ω. In order to be able to visualize the Thevenin output voltage, two (or three, depending on the configuration) 10-kΩ Wye-connected resistors have been connected to the mid point of each leg.

Fig. 7 corresponds to the case of two-legs per phase with m_a= 0.8. It shows the phase voltage (v_a), the line-to-line voltage (v_{ab}), the phase current (i_a), and the leg currents (i_{a1} and i_{a2}) for that phase. At the beginning of the figure the modulation is carried out with only one set of carriers, i.e. using conventional PS-PWM. From t= 50 ms on, the proposed PS-PWM method is used. Although the waveform of the phase voltage is not visually affected, the improvement in the line-to-line voltage is significant. There is also a perceptible reduction in the current ripple. It can be seen that the change from

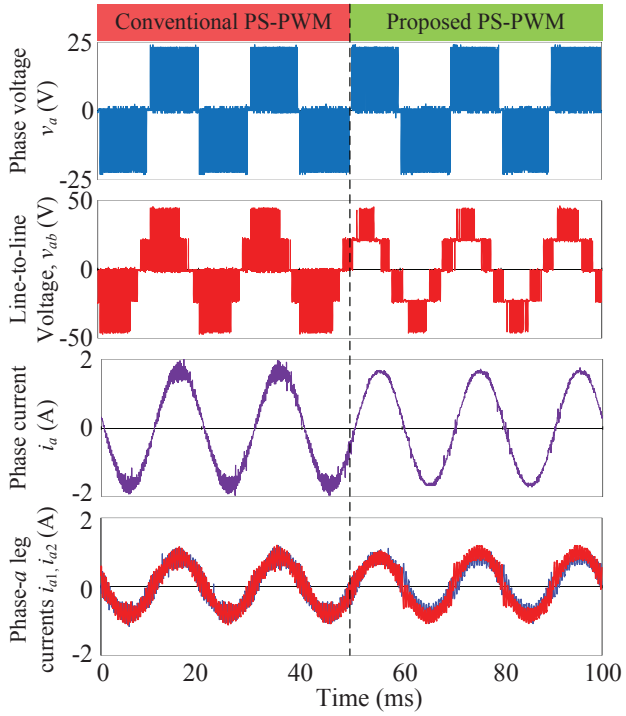

Fig. 7. Experimental results with two legs connected in parallel. Transient from conventional PS-PWM to proposed PS-PWM with a modulation index m_a= 0.8. From top to bottom: phase voltage, line-to-line voltage, phase current, and leg currents.

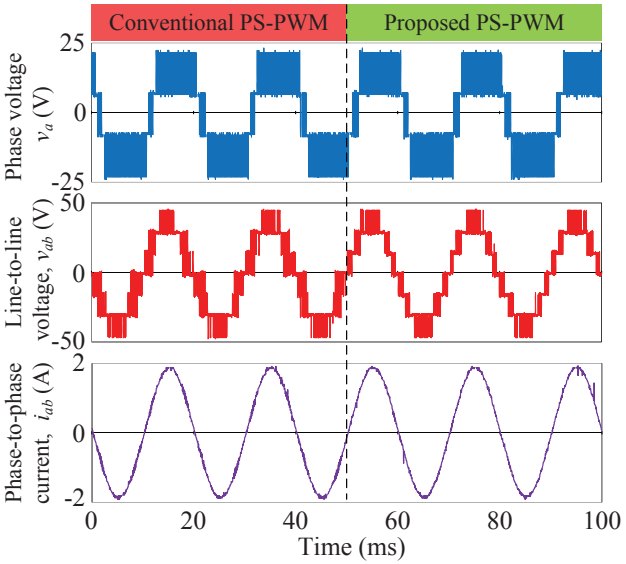

Fig. 8. Experimental results with three legs connected in parallel. Transient from conventional PS-PWM to proposed PS-PWM with a modulation index m_a= 1.0. From top to bottom: phase voltage, line-to-line voltage, and phase-to-phase current.

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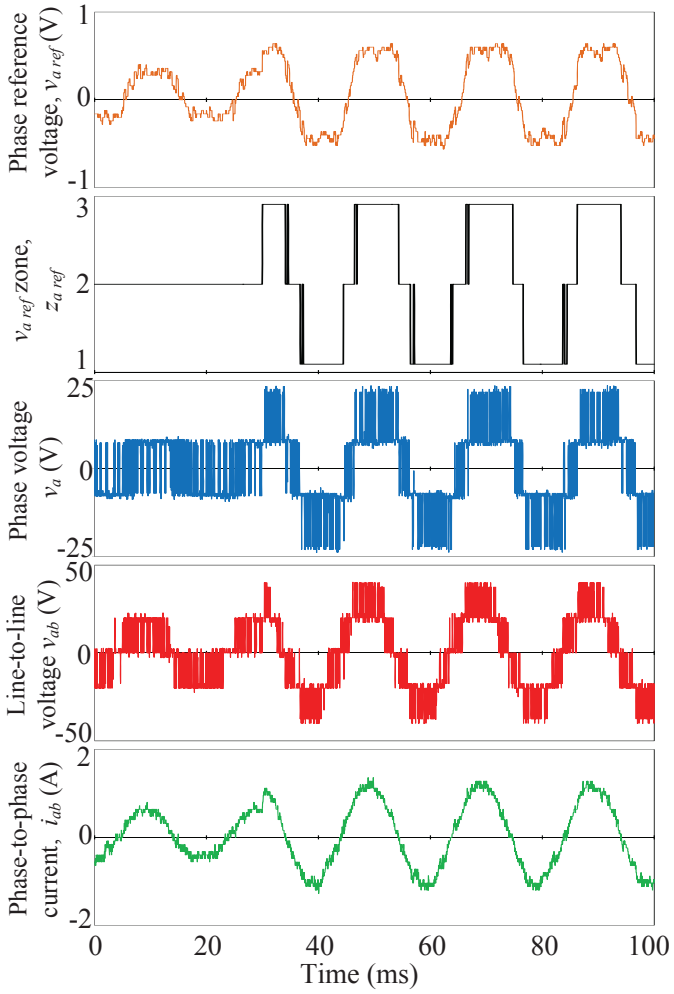

Fig. 9. Experimental results with three legs connected in parallel showing a step in the modulation index m_a from 0.3 to 0.6. The reference signal includes random noise to represent a control action. From top to bottom: phase-*a* reference voltage, reference zone, phase voltage, line-to-line voltage, and phase-to-phase current.

the conventional to the proposed PS-PWM causes a slight imbalance in the leg currents that is not significant.

The experimental results obtained with three legs per phase, can be seen in Figs. 8 and 9. As phase *c* is not implemented in this configuration, the resistor load between phases *a* and *b* is $R = 20\Omega$. Fig. 8 shows the phase voltage (v_a), the line-to-line voltage (v_{ab}) and the phase-to-phase current (i_{ab}) for m_a= 1.0. The current ripple reduction and the improvement in the quality of the line-to-line voltage can be noticed here too, although to a lesser extent than in the previous case, with two legs connected in parallel. In order to emulate the behavior of the modulator in a close-loop control system, a randomly shaped signal has been added to the reference signals. Fig. 9 displays such a reference signal for phase-*a* (v_{refa}), the internal signal generated by the even/odd zone detector (z_{refa}), the equivalent phase voltage (v_a), the equivalent line-to-line voltage (v_{ab}), and the phase-to-phase output current (i_{ab}). When at first m_a is 0.3, the reference signal is confined to Zone 2 and only one set of carriers is used. At t= 30 ms, there is a step change to m_a= 0.6 and, as all the zones are used, the dynamic selection of the carriers begins. Although the shape of the reference signal causes some additional zone transitions that imply changes in the set of carriers to be used, neither the equivalent phase voltage nor the output current is apparently affected.

V. Conclusion

This letter has presented a new interleaved PWM implementation for VSIs with legs connected in parallel. With the proposed implementation, the quality of the line-to-line output voltages is improved owing to the fact that switching occurs exclusively between adjacent levels. The modulator makes use of two sets of *n* evenly phase-shifted carriers that are dynamically allocated. The implementation is presented in a general way so that it can be applied to multi-phase converters with any number of phases and any number of legs in parallel per phase. It is, therefore, appropriate for modular parallel converters. Because of the improvement in terms of line-to-line voltages, better THD values are achieved, which can lead to a reduction in the output filtering requirements.

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