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Survey of Robustness Enhancement Techniques for Wireless Systems-on-a-Chip and Study of Temperature as Observable for Process Variations

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Abstract Built-in test and on-chip calibration features are becoming essential for reliable wireless connectivity of next generation devices suffering from increasing process variations in CMOS technologies. This paper contains an overview of contemporary self-test and performance enhancement strategies for single-chip transceivers. In general, a trend has emerged to combine several techniques involving process variability monitoring, digital calibration, and tuning of analog circuits. Special attention is directed towards the investigation of temperature as an observable for process variations, given that thermal coupling through the silicon substrate has recently been demonstrated as mechanism to monitor the performances of analog circuits. Both Monte Carlo simulations and experimental results are presented in this paper to show that circuit-level specifications exhibit correlations with silicon surface temperature changes. Since temperature changes can be measured with efficient on-chip differential temperature sensors, a conceptual outline is given for the use of temperature sensors as alternative process variation monitors.

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1 Introduction

Many semiconductor product improvements are direct or indirect consequences of the perpetual shrinking of devices. A paralleling trend is that process variations and intra-die variability increase with each technology node. Since most high-performance analog circuits depend on matched devices and differential signal paths, this trend has begun to diminish yields and reliabilities of system-on-a-chip (SoC) designs. Fundamentally, the problem is that parameters of devices on the same die show increasing intra-die variations, thereby exhibiting different characteristics. For example, Table 1 lists the evolution of the typical transistor threshold voltage standard deviation $\sigma\{V_{Th}\}$ normalized by the threshold voltage (V_{Th}) for several technology nodes, as reported in [10]. In addition to higher percent errors for small fabrication dimensions, the threshold voltage mismatch worsens even for neighboring transistors due to the increasing effect of dopant fluctuations in modern CMOS processes [2].

A direct consequence of device parameter variations is a decrease in production yields because block-level and system-level parameters will show a corresponding increase in variations. This relationship between variations and yield can be inferred from the visualization in Fig. 1, where the Gaussian distribution of a specification with a standard deviation σ around the mean value μ is shown together with the specification limits (±3σ in this example). For standalone analog circuits, parameters such as gain may

Table 1 Intra-die variability vs. CMOS technology node (from [10])

Technology Node	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm
$\sigma\{V_{Th}\}/V_{Th}$	4.7%	5.8%	8.2%	9.3%	10.7%	16%

have an upper and/or lower specification limit, and the samples that exceed the limit(s) during production testing must be discarded. Guardbands are often defined to account for measurement uncertainties by following procedures such as repeating the same test or performing other more comprehensive tests to determine whether the part can be sold to customers, which incurs additional test cost in a manufacturing environment. An important observation from Fig. 1 is that an increase of variation (σ) widens the Gaussian distribution, which leads to a higher percentage of parts falling within the highlighted ranges that require them to be scrapped or retested. Clearly, there is a direct relationship between the amount of production cost and yield reduction attributable to process variations. In the case of wireless mixed-signal integrated systems, the trend towards increasing integration and complexity has also been paralleled by technical challenges and rising cost of testing, which can amount up to 40–50% of the total manufacturing cost [37, 49].

System complexities and process variations raise the importance of considering testability early in the design phase to avoid technical complications and time-to-market delays in the pre-production phase as well as test cost reduction during the production phase. Worst-case process corner models have been used extensively to account for variations during the design of analog circuits. But more recently, a paradigm shift is towards the use of statistical models and Monte Carlo simulations. One of the main reasons for this development is that a corner-based design approach easily results in too pessimistic designs [20]. Normally, leaving excessive margins for process variations through overdesign should be avoided because it involves costly performance or parameter trade-offs. This economic reason and the availability of more efficient on-chip computational resources is an incentive to equip wireless SoCs with more self-calibration features. Along these lines,

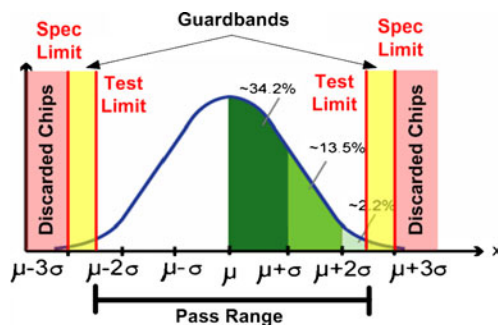

Fig. 1 Specification variation impact on the fraction of discarded chips

a production test strategy for SoCs has recently been proposed in [17] to address cost savings through the use of soft specification limits based on statistical parameter distributions in combination with a defect-oriented test approach that enables low-cost testing with less accurate equipment or built-in circuitry.

In addition to the underlying variation issues on the device level, several system-level and technology trends impair the testability and manufacturability of integrated circuits for mobile applications. Developments over the past decades have resulted in low-power handheld devices with multi-purpose functionality such as video, voice, pictures, and internet access. Most relevant services for wireless devices range from 470 MHz to almost 11 GHz, resulting in signal interference issues. This concern can be partially solved if more linear high-performance analog receiver front-ends are available to tolerate and filter out interference signals without saturation of the analog blocks due to the high signal power levels. Further filtering and channel selection can be performed in the digital domain when the signal integrity is maintained during the processing in unsaturated highly-linear analog and analog-to-digital conversion blocks. Nonetheless, the processing of broadband signals in radio frequency (RF) front-ends mandates high-performance analog circuits, which in many cases requires continued circuit-level innovations for on-chip self-calibration to tune for optimum performance. Support of multiple communication standards requires chips with more circuitry and complexity, making them less testable in the production stage because of limited access to internal nodes, interactions between blocks, and a higher number of test cases to verify functionality. Additionally, systems with more subcomponents are more likely to fail. The main advantages of device scaling with CMOS technology are improved high frequency response, reduced power consumption, and increased levels of integration. With regards to analog circuits, deep-submicron technology scaling progress comes together with adverse effects such as reduced gains from lower transistor output impedances, limited voltage headroom, higher flicker noise levels, and reduced transistor linearity. Additional reliability concerns arise from the restricted power that transistors can supply to their loads without exceeding the low breakdown voltage of the deep-submicron devices.

As a consequence of the abovementioned issues, built-in self-test, design-for-test, and design-for-manufacturability methods for analog and mixed-signal circuits have received growing interest [25]. The purpose of this paper is twofold:

on the one hand, to present a survey of existing built-in testing and calibration strategies that cope with performance shifts in transceiver SoC circuitry due to process variations, which is covered in Section 2. On the other hand, to show that process variations not only affect performance specifications of circuit blocks, but also influence the temperature profile on the silicon die. This part is covered in Section 3. Section 4 describes how the correlation between circuit-level performance parameters and on-die temperature changes can be exploited to monitor process variations with on-chip differential temperature sensors. Experimental results are also presented in Section 4, which were obtained with a 0.25 µm CMOS test chip that contains a narrow-band low-noise amplifier (LNA) operating around 1 GHz and a compact on-chip temperature sensor for built-in test purposes. Lastly, conclusions are given in Section 5.

2 Transceiver Self-Calibration and Built-In Test Approaches

While equipping circuit blocks with built-in test (BIT) and self-calibration features to compensate for variations, it is important to keep their role as part of the system in mind because of the interaction between blocks and the overall goal to optimize system-level performance specifications such as bit error rate (BER) or error vector magnitude (EVM). In general, the self-calibration challenge can be divided into two parts: one is to add tunability and controllability capabilities in the individual blocks, and the other one is to devise comprehensive system-level calibration algorithms in a digital signal processing unit. BIT strategies for transceivers vary depending on the transceiver architecture, communication standard, available on-chip measurement and computation resources, the production volume, and whether the BIT is designed for production testing (quality control) or on-line self-calibration (reliability) during the life time of the chip. Consequently, most BITs involve a mix of analog and digital blocks, on-chip and off-chip components, long calibration routines at start-up, and shorter periodic or on-line calibration. Generally, a trend has emerged to combine techniques for the verification of complex mixed-signal SoC transceivers. Despite of the diversity, BIT approaches can be grouped into a few broad categories. In the following overview, a few example cases will be discussed to highlight the distinctive characteristics of the methods.

2.1 Digital Correction and Calibration

Digital BIT approaches involve measurements and compensation techniques that are realized in the digital baseband processor of the transceiver. They have the advantage of high precision when sufficient computational resources are available. Furthermore, they are suitable for parameters that are observable and correctable in the digital domain, such as slowly drifting DC offsets or mismatch between the in-phase (I) and quadrature-phase (Q) paths of receivers. They are also very attractive for on-line calibration schemes that run in the background.

Digital I/Q mismatch compensation involves digital measurement and compensation of the I/Q gain and phase mismatches in the analog circuitry of a receiver. For example, the work in [21] presents a scheme that runs during start-up or in a dedicated calibration mode to ensure acceptable performance of a low-IF receiver even with up to 10% gain and 10° phase imbalance in the analog front-end. On-line digital I/Q compensation techniques have also been reported, such as [15], in which training symbols in orthogonal frequency-division multiplexing (OFDM) transmissions are exploited for background I/Q calibration. It was also demonstrated in [15] how digital I/Q compensation relaxes the overall signal-to-noise ratio (SNR) requirements in the receiver chain because I/Q imbalance directly affects the SNR and thereby degrades the BER. In the OFDM receiver example presented in [15], the digital calibration allowed to improve the tolerance to I/Q imbalances from (1%-gain)/(1º-phase) to (10%-gain)/(10º-phase). Digital I/Q calibration is widely used. An example is the work in [16] describing a low-IF GSM receiver in 90 nm CMOS technology. This receiver utilizes an adaptive digital filter that obtains the mismatch information from on-line I/Q correlations, for which the adapted block diagram from [16] is displayed in Fig. 2. The interesting section of this block diagram involves the adaptive digital decorrelator

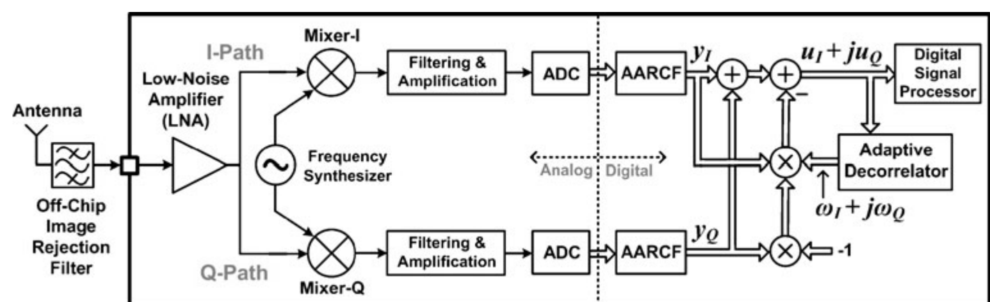

Fig. 2 Receiver with digital I/Q mismatch compensation [16], where ω_I/ω_Q are the correction coefficients and u_I/u_Q are the compensated outputs

after the analog-to-digital converter (ADC) and anti-aliasing rate change filter (AARCF). In the digital domain, gain mismatch appears as difference in the auto-correlation between I and Q paths, while phase mismatch appears as nonzero cross-correlation between I and Q. The authors use an algorithm that takes advantage of these relationships by implementing an adaptive decorrelator which attempts to minimize the auto-correlation and the cross-correlation between I and Q outputs (y_I, y_Q). This is done by updating the correction coefficients until the error is within the allowed tolerance:

$$\omega_{I(n+1)} = \omega_{I(n)} + \mu \cdot [u_{I(n)} \cdot u_{I(n)} - u_{Q(n)} \cdot u_{Q(n)}], \quad \omega_{Q(n+1)} = \omega_{Q(n)} + 2\mu \cdot u_{I(n)} \cdot u_{Q(n)}; \tag{1}$$

where $u_{I(n)}$ and $u_{Q(n)}$ are the compensated I and Q outputs at the nth iteration, and μ is the adaptation step size which is inversely proportional to the signal energy. Thus, periodic training sequences are required with this scheme. Depending on process-voltage-temperature (PVT) variations, 15–30 dB image rejection ratio (IRR) improvement has been demonstrated in practice with phase mismatch <1°, amplitude mismatch <10%, and a settling time between 3–4 milliseconds [16].

The incentive for using a digital BIT technique is high when the circuit under test itself has digital features. An example is the BIT in [42] for a transmitter that includes an all-digital phase-locked loop (ADPLL). In that case, the error signal of the ADPLL is already in the digital domain, allowing to monitor failures and the center frequency drift of the digitally controlled oscillator. Furthermore, the authors of [42] state that digital filtering and spectral estimation can be used to observe and adjust the phase noise transfer function.

2.2 Analog Measurements and Tuning

Analog I/Q imbalance calibration has been proposed and demonstrated for image-reject receiver (IRRX) architectures. A simplified block diagram of such a scheme is displayed in Fig. 3, which is representing the work from [32]. In an IRRX, the down-conversion scheme with two mixing stages suppresses the image signal at the second intermediate frequency output Out(f_{IF2}), which avoids the need for an external image-rejection filter. The quality of the image-rejection is typically expressed with the image-rejection ratio (IRR) that depends on the I/Q amplitude mismatch (ΔA) and phase mismatch ($\Delta\theta$):

$$IRR_{(dB)} \approx 10 \log \left(\frac{(\Delta\theta)^2 + (\Delta A/A)^2}{4} \right) \tag{2}$$

In practice, the IRR is often limited to 25 dB–40 dB due to mismatches, even though almost 60 dB are frequently required for acceptable BER performance. In [32], a purely analog calibration scheme was implemented with the auxiliary path shown in Fig. 3. This path contains duplicate mixing operations as in the main path with the exception that the output signal at the second intermediate frequency (f_{IF2}) can be of the form $\cos(2\pi f_{IF2} t)$ or $\sin(2\pi f_{IF2} t)$, depending on which phases of the two local oscillators (LO_1, LO_2) are routed to the auxiliary mixers. Finally, $mixer_3$ correlates the signals from the two paths to extract the I/Q mismatch information contained in the DC component after the lowpass filter (LPF). The resulting analog DC voltage (V_{cal}) can be directly used to tune the bias voltages of analog circuits for mismatch compensation, resulting in high IRR (e.g. 57 dB in [32]). A similar automatic on-line IRR calibration using analog mixers, a

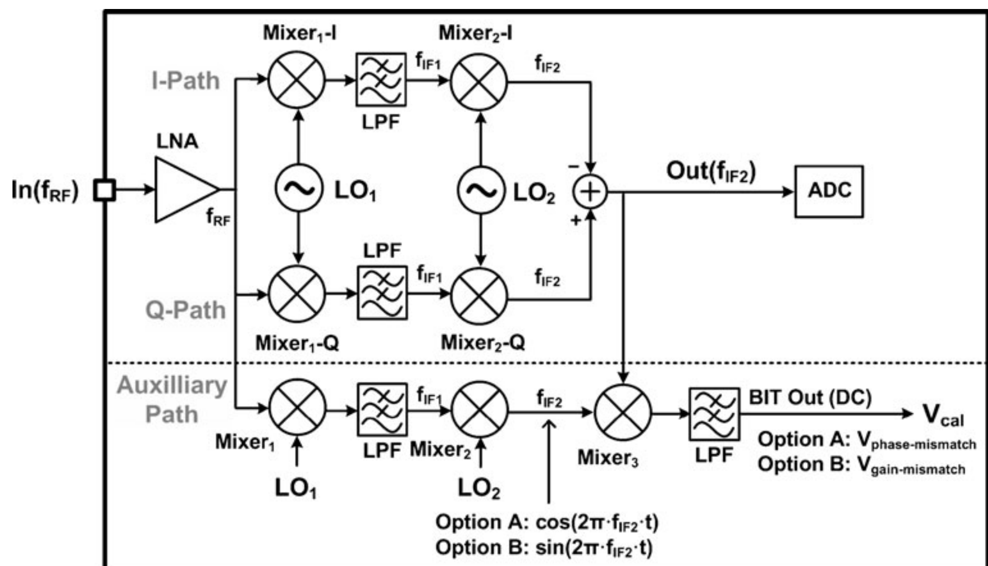

Fig. 3 Analog I/Q calibration for image-rejection receivers [32]

variable phase shifter, and gain tuning has been realized in [18] with an IRR of 59 dB.

A benefit with analog tuning is that the bias conditions of the analog blocks under calibration are controlled and are more robust to PVT variations due to the correcting actions of the feedback loops. This enables higher yields as a result of automatic correction in the analog front-end blocks. However, the power and area consumption of the BIT circuitry is the main trade-off. Furthermore, the BIT circuits themselves have to be designed robustly to avoid failures, making the implementation more challenging and invasive than digital schemes. Efforts for the analog approach are typically more justified for transceivers that have few on-chip digital resources and in scenarios that require fast automatic correction (e.g. in the microseconds regime as in [39]).

Instead of using a system-level test strategy, it has also been popular to extract information from each block in the analog front-end for characterization or tuning of the individual blocks, which is visualized in Fig. 4. The circuit under test (CUT) represents a block in the RF front-end or analog baseband that can be connected to a BIT circuit in test mode by closing the two switches S_1 and S_2. In [38] for instance, a low-noise amplifier (LNA) was tested with a BIT block containing a test amplifier and two precise power detectors to measure input impedance, gain, noise figure, input return loss, and output SNR of the LNA. This approach has the advantages that the fault locations/causes can be identified clearly, and that the DC or digital outputs of the BIT circuits can be used to recover from certain failure modes. High-frequency RF front-ends have been targeted in particular with dedicated design of BIT circuits because their gain, impedance matching, and linearity performances are very sensitive to variations. Also, direct signal digitization is not feasible at high frequencies, eliminating many digital compensation schemes. Hence, several RF block-level measurement approaches involve power or amplitude detectors along the signal path [8, 19, 45, 47, 48].

Self-calibration of impedance matching for an LNA at the input of the receiver chain as done in [14] also requires on-chip analog sensing circuitry, especially to achieve a short calibration time such as the 30 μs reported in [14]. Another alternative proposition to monitor individual blocks in the signal path was made in [43], in which the transient supply current of the CUT is sensed with the BIT circuitry by placing a small series resistor in the power supply line. However, a disadvantage with any block-level measurement is that the BIT circuitry is connected to the CUT and therefore must be designed carefully to avoid impact on performance. But even with careful design, some degradation due to loading effects from BIT circuitry must usually be tolerated. Furthermore, switches in or along the signal path are undesired because of their insertion losses and signal feedthrough due to finite isolation, particularly at RF frequencies.

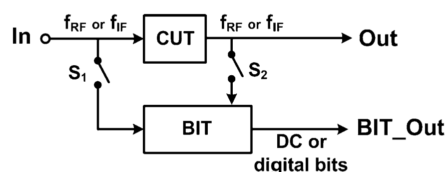

Fig. 4 BIT with analog instrumentation along the signal path

Although with less accuracy than off-chip measurement equipment, efforts have also been made to mimic conventional instrumentation such as spectrum analyzers [26, 44] on the chip with sufficient accuracy for BIT applications. In [26] for example, the analyzer with a frequency range of 33 MHz to 3 GHz can cover the entire signal paths of many wireless transceivers in handheld consumer products. A multiplexor could be used to selectively route a test input at a time to one spectrum analyzer, but the on-chip measurement circuitry still uses up large area and significant power which might not be permissible in certain applications. For example the analyzer in [26] consumes 0.384 mm^2 and more than 20 mW.

2.3 Loopback Testing

Loopback testing is a system-level BIT technique in which the BER is monitored in the digital baseband [12]. It allows simultaneous verification of the analog and digital transceiver blocks with a low-frequency digital input signal applied to the baseband subsection of the transmitter. As indicated in Fig. 5, this up-converted signal is routed from the transmitter (TX) output to the receiver (RX) input via a loopback connection [35]. After down-conversion and digitization in the RX, the received bitstream is analyzed in the digital baseband processor to determine the BER. Attenuation and frequency translation with a mixer are required in the loopback block to provide a suitable signal at the RX input. If the communication standard does not require frequency translation between TX and RX, then only the attenuator is needed. In any case, the overhead of the BIT circuitry is below 10% of the complete transceiver [35], which is efficient. However, the loopback BIT cannot be executed on-line; it requires a dedicated test mode during production testing or self-checks during times when the transceiver is idle.

The main benefit of the loopback technique is that a BER test is the most important metric, which only passes when all components function properly. This property makes loopback very attractive for fast pass/fail production testing and quick self-checks during in-field use, especially when few or no off-chip test resources are available. For instance, a loopback test for the on-wafer production test stage was presented in [41]. A drawback of early loopback

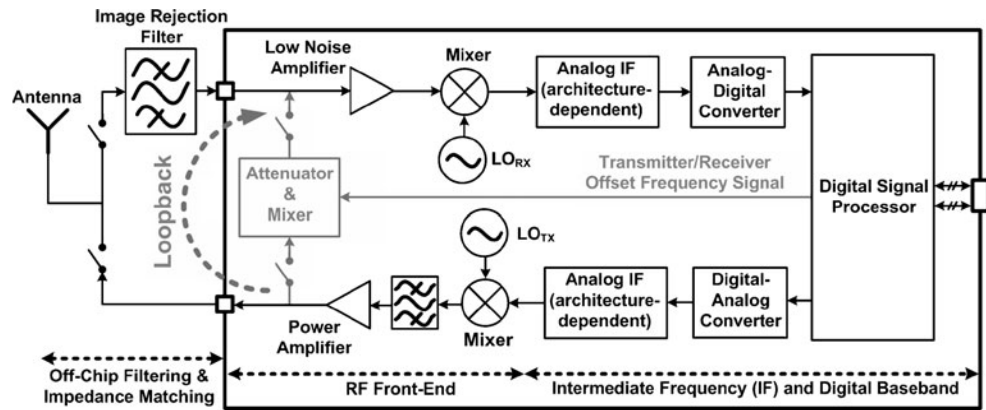

Fig. 5 Generalized transceiver block diagram with loopback

implementations is the lack of information regarding failure causes and fault locations. In response, one proposed variant [23] involves more computations in the digital baseband processor to determine the spectral content of the receiver output bits and to use the data for estimation of receiver/transmitter nonlinearity specifications. Alternatively, power detectors can be placed at critical nodes to extract block-level gain and 1-dB compression point measurements. Or, similarly, statistical sampling blocks were placed along the signal path in [33] to produce digital bitstreams for analysis of fault locations. In brief, inclusion of auxiliary circuitry during a loopback test increases the observability of faults, but with the associated trade-offs that have been discussed for on-chip measurement circuitry in Section 2.2. Another method to reduce fault masking in a production test setup encompasses an off-chip analog filter and adder in the loopback path [40].

2.4 Combined Digital Performance Monitoring and Analog Tuning

A BIT approach for complex transceiver chips that has become increasingly popular in recent years is depicted in Fig. 6. It incorporates accurate digital monitoring and I/Q mismatch correction in the baseband processors after the analog-to-digital converter (ADC) as well as analog observables such as outputs from received signal strength indicators or DC control voltages of blocks that give some insights into their operating conditions. A significant aspect is that many analog bias voltages for RF front-end and baseband circuits are generated by digital-to-analog converters (DACs). These DACs are utilized for coarse adjustments at start-up in order to compensate for PVT variations. They also reduce DC offsets in the analog circuits to prevent saturation of internal nodes due to large gains in the receiver chain. Thus, more mismatches can be tolerated because of the capability to counteract them. Digital monitoring and calibration combined with analog compensation DACs has been reported in publications describing industrial transceivers [13, 24, 27, 46].

One goal that can be defined to improve the combined self-calibration approach is to enhance fault observability and calibration effectiveness by adding more measurement circuitry in the analog segments. This would provide additional data that can become part of the system-level calibration routine. Information from on-chip measurements can be used for block-level tuning prioritizations and optimizations, leading to shorter start-up routines and convergence times of algorithms. As shown in Fig. 6, on-chip power detectors (PD) can be included to measure gains

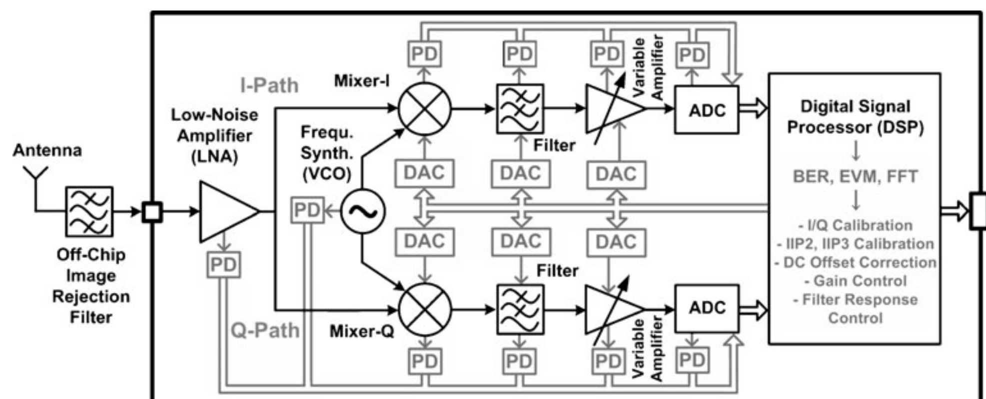

Fig. 6 Transceiver with digital monitoring, analog measurements, and tuning; where the PD and DAC blocks represent on-chip power detectors and digital-to-analog converters, respectively

along the analog chain, providing enhanced analog measurement capability as described in [8, 45, 47, 48]. Alternatively, on-chip differential temperature sensors [4, 34] could be used for that purpose without connecting circuitry to the signal path: the activity of the CUT (power dissipation) can be observed thanks to the inherent substrate thermal coupling. This approach avoids the loading effects from finite input impedances of electrical detectors. Moreover, the integration of more functionality and transistors into SoCs leads to higher power densities on the chips, which causes more pronounced temperature gradients and interference between circuits due to thermal coupling. This has motivated investigations into the feasibility of on-chip temperature measurements to monitor PVT variations. Due to the novelty of the approach, the relationships between temperature and circuit variations are discussed with more detail in the following sections.

2.5 Circuit-Level Performance Tuning

Individual blocks are tuned as part of the system-level calibrations described in the previous section, for which diverse mechanisms can be used depending on the specific circuit and its application. For instance, the gain of the RF transconductor in [27] has 5-bit digital gain programmability by selectively activating a number of transconductance elements that are connected in parallel. Alternatively, the transconductance values of the baseband filter in [46] are tuned by adjusting bias voltages with 8-bit DACs. Additionally, the receiver path in [46] contains 8-bit current-steering DACs to cancel DC offsets at the output of the mixing stage. Digital correction of I/Q gain mismatches can also be carried out immediately after the down-conversion by generating the bias currents for the mixers in the I and Q paths with separate current sources consisting of multiple elements [28]. This is visualized for a single-balanced mixer in Fig. 7a, where control bits B_1–B_0 set the conversion gain. Second-order nonlinearities due to mismatches in the mixer can be reduced as well with load resistors that are comprised of multiple parts and switches [28], which enables mismatch compensation by setting the optimum resistor value for each branch at the mixer output with digital control bits D_1–D_N. Digitally programmable resistors have also been employed for enhancement of third-order nonlinearities in transconductance-capacitor baseband filters, provided that a linearization scheme with dependence on resistors is applied such as the one proposed in [31].

Circuit-level tuning methods have been reported to recover from process variations of passive components that influence the frequency response in the RF front-end. For instance, Fig. 7b shows how, as proposed in [14], the input impedance matching network of a conventional inductively degenerated common-source LNA can be digitally tuned by designing it with a gate inductor L_g that is tapped at several

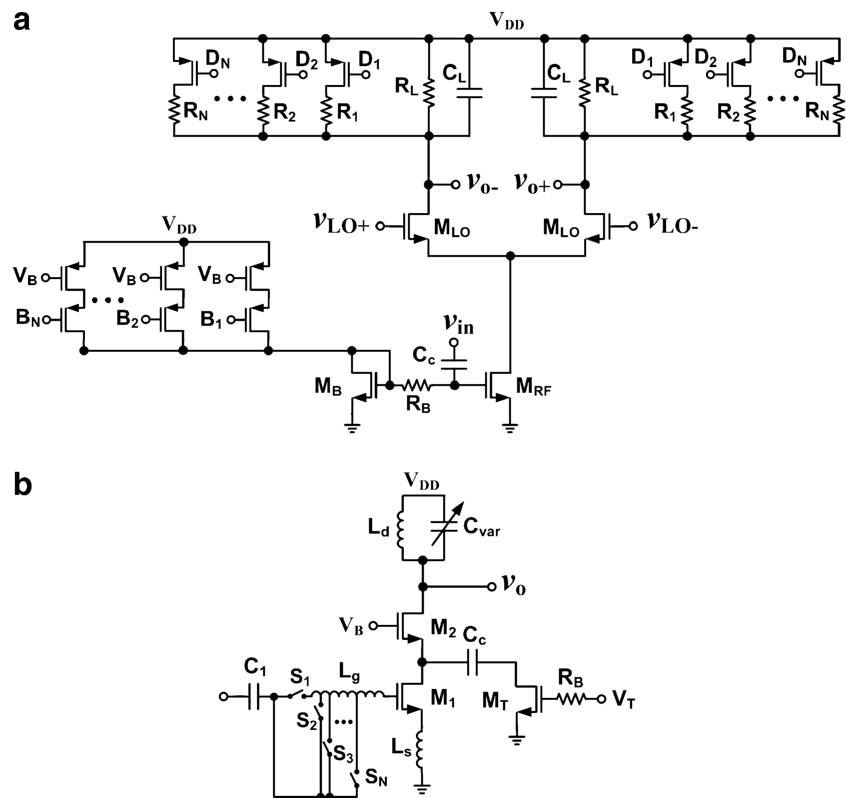

Fig. 7 Examples for tuning knobs: **a** mixer gain (B_1…B_N) and second-order nonlinearity (D_1…D_N) from [28], **b** LNA with input impedance matching correction (S_1…S_N) from [14], center frequency tuning (C_{var}) from [3], and gain adjustment (V_T) from [29]

points by closing one of the switches $S_1 \ldots S_N$. However, the on-resistance of the switch in the signal path must be carefully considered during the design in order to minimize its effect on the quality factor of the input matching network as well as on the noise and linearity performance. An additional tuning feature is the varactor C_{var} in the inductor-capacitor tank, which can be used to adjust the self-resonant frequency according to [3]. Finally, Fig. 7b also displays the gain adjustment method from [29]: the auxiliary transistor M_T is employed as variable resistor that diverts signal current to the AC ground instead of the output, modifying the LNA gain while the LNA DC bias remains unaffected thanks to the capacitor C_c.

3 Process Parameter Variations and Silicon Temperature

Various process variation monitoring approaches circumvent direct measurements of functionality or specifications to reduce the complexity of the on-die monitors and the time required to extract data, but also to avoid degrading the CUT performance by electrically connecting to the signal path. Some examples are methods that entail sensing supply current [11], sensing timing slack [36], measuring the frequency of ring oscillators [9], or measuring the characteristics of dummy circuits that resemble the CUT [1]. It has also been observed that thermal coupling through the semiconductor substrate generates a temperature gradient in the vicinity of a circuit/device that depends on its power dissipation [6]. Since many process variation effects manifest themselves in a change of the power dissipation associated with devices in the circuit, sensing the corresponding local temperature changes offers a non-invasive opportunity to monitor relevant parameter variations. The relationship between CUT performance variations and device-level power dissipation is explained next, and the measurement of power dissipation using differential temperature sensors is discussed in Section 4.

3.1 Impact of DC and RF Power Dissipation on Local Temperature

The diagram in Fig. 8 illustrates how due to the Joule effect, the temperature near a device is a down-converted physical magnitude that contains information of the high-frequency electrical signals. The Joule effect is modeled as a frequency mixer; and as a consequence of its quadratic nature, the spectral components of the power dissipated by the CUT's devices are frequency-shifted relative to the spectral components of the electrical signals that drive the CUT. The shifted low-frequency power components enable the device temperature to be an observable of the high-

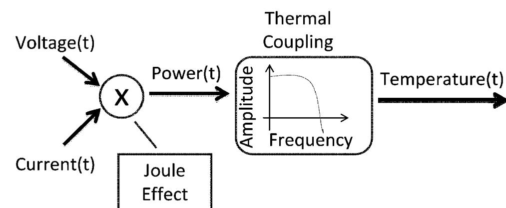

Fig. 8 Down-conversion from high-frequency electrical signals to low-frequency temperature changes

frequency figures of merit. The relationship between the power dissipation and temperature increase at the silicon surface can be modeled by a lowpass filter with a typical cut-off frequency below hundreds of kHz [7]. As a matter of a fact, the equivalent block diagram is very similar to the one of a conventional receiver. Therefore, from a frequency-shifting point of view, the temperature increase can either be a direct-converted magnitude of the high-frequency electrical signals processed by the CUT (i. e., a DC temperature increase generated by mixing of electrical signals at the same frequency f) or it can be generated at an intermediate frequency (i. e., the CUT is driven with two electrical signals of frequencies f_1 and $f_1+\Delta f$, and the temperature increase is generated and sensed at Δf; where Δf must be below the cut-off frequency of the thermal coupling transfer function). The first approach is defined in [5] as homodyne thermal testing, and the second as heterodyne thermal testing.

Thermal testing strategies involve both electrical (voltage and current) and physical (temperature) magnitudes. Simulation of such phenomena requires an electrical model of the electro-thermal coupling. An example is shown in Fig. 9. It contains an amplifier, a basic temperature sensor [4, 34] (i.e., a parasitic bipolar transistor with a constant DC bias and an amplification stage that monitors the changes of the emitter current due to local temperature changes), and a resistor-capacitor (RC) network modeling the thermal

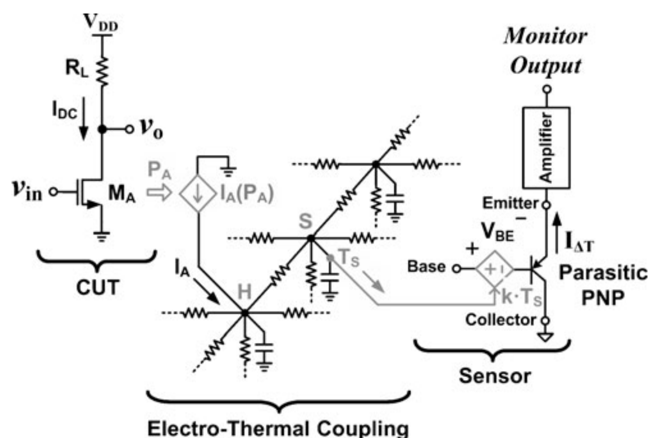

Fig. 9 Simplified electro-thermal coupling model between a transistor M_A and a PNP sensing device

coupling (details can be found in [34] and [30] for example). The error of the electro-thermal coupling simulations can be maintained within 10% by selecting the proper resolution for the RC network components based on the dimensions of the silicon die and the embedded devices [34]. The power dissipation of active devices influences the local surface temperature, which can be measured with the sensor. Considering the amplifying transistor M_A as the CUT, the following expression for the DC power P_A that M_A dissipates can be derived when a sinusoidal signal with amplitude A is applied at v_{in} [5]:

$$P_A = (I_{DC} \cdot V_{DD} - R_L \cdot I_{DC}^2) - \tfrac{1}{2}(g_m \cdot A)^2 R_L, \quad (3)$$

where g_m is the transconductance of M_A. First, notice that this DC power dissipation depends on both the biasing of the circuit and on the RF signal processed by the amplifier. Second, the AC terms of the power have been dropped from expression (3) under the assumption that only the DC component is measured with the homodyne approach. Each node in the RC network represents a unit volume of the silicon die, at which the injected current I_A models the power dissipation of transistor M_A at location H. Each voltage node in the grid models a temperature change with respect to the ambient die temperature. The parasitic bipolar device (PNP) used as temperature transducer is at location S. Since the amount of coupling between locations H and S reduces rapidly with distance [6], the sensor should be placed close to the CUT (< 20 μm) to ensure that the locally measured temperature change T_S predominantly reflects the power dissipation of nearby transistor M_A. Finally, the factor k (≈ −2 mV/°C) in Fig. 9 is the sensitivity of the base-emitter junction to temperature, which causes the output current of the bipolar transistor to change, allowing the DC output voltage of the following amplifier to be used as a process monitor. The two main advantages of this testing strategy can be identified from Figs. 8 and 9: first, the sensor circuit does not electrically load the CUT. Second, measurements are performed at low frequencies, regardless of the CUT's operating frequency.

3.2 Direct Relationship Between Temperature and Specifications

Figure 10 shows the schematic of a common-source LNA used as CUT in this section. The preferred temperature observation points are near devices with relatively high signal power. For example, the cascode transistor M_C has a larger drain-source voltage swing than transistor M_M, but the same DC and AC current flows through both devices. Hence, M_C is the better candidate for observation of its higher power dissipation with a nearby temperature sensor. Table 2 summarizes the relevant simulation results for the LNA designed in 65 nm CMOS technology. Statistical process models were used for active and passive devices, and 1000 Monte Carlo simulations were performed to gain insights into the observability of parameter variations through the average power dissipation at the cascode transistor. In these simulations, a −25 dBm input tone at 2.45 GHz was applied to determine the average power from the current through M_C and its drain-source voltage drop during the simulation [22] for comparison with several key parameters. Considering the homodyne thermal testing approach, only the DC component of the dissipated RF power will generate a measurable DC temperature change after application of the RF test tone. Figs. 11 and 12 show the correlations of the DC power dissipated due to the RF electrical signal [second term in eq. (3)] with the voltage gain and the 1-dB compression point, respectively. Both of these specifications show high correlation since they are direct reflections of the dynamic power dissipated at transistor M_C. Notice from the correlation plots that the DC power difference to be monitored with temperature sensors is in the 5–80 μW range, which is feasible with the sensor topologies reported in [4, 34] as will be shown in the following section. These results indicate that temperature sensing is a suitable method to identify whether a detrimental performance shift has occurred with regards to one of these two parameters. As it can be observed in Fig. 13, there is also some correlation between the power dissipation and the noise figure, but this relationship is less pronounced. Nonetheless, the corresponding production test approach derived from this result would not involve direct

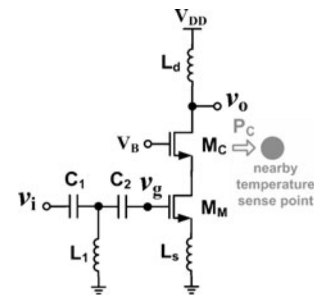

Fig. 10 Common-source LNA with T-matching network

Table 2 Simulated LNA performance (mean values at 27°C)

Specification	Value at 2.45 GHz
Voltage Gain (v_o/v_i)	25.9 dB
1-dB Compression Point	−15.4 dBm
IIP3	−3.2 dBm
S_{11}	−17.6 dB
NF	4.5 dB
Power	0.42 mW
Technology/V_{DD}	65 nm CMOS/1.2 V

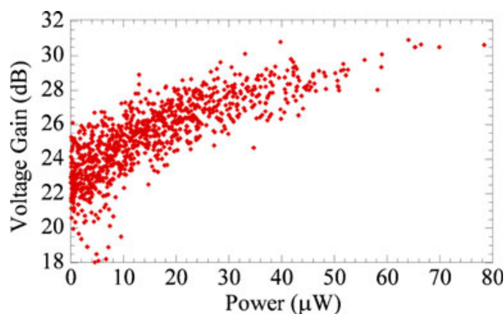

Fig. 11 Gain vs. DC power dissipation at M_C in the LNA due to the RF test signal. The power due to DC bias is not included

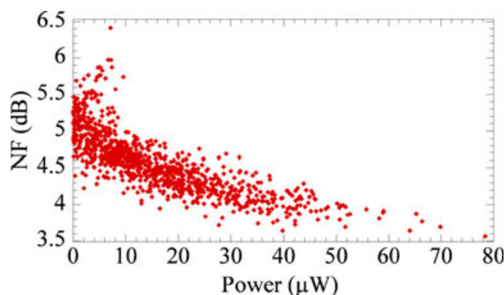

Fig. 13 Noise figure vs. DC power dissipation difference at M_C in the LNA due to the RF test signal. The power due to DC bias is not included

measurements of small noise quantities. Instead, faulty devices can be screened out based on the correlation between noise figure and power, since a low DC power (temperature) difference measurement is an indicator for poor noise figure.

3.3 Thermal Tendencies and Center Frequency Measurement

Equation (3) can be rewritten as [5]

$$P_A = (I_{DC} \cdot V_{DD} - R_L \cdot I_{DC}^2) + \tfrac{1}{2} g_m \cdot A^2 \cdot G_V(f), \tag{4}$$

where $G_v(f)$ is the voltage gain of the amplifier at the frequency f, which is negative for an inverting amplifier. If the frequency of the input tone is swept over the inverting amplifier's band of operation, then the frequency at which the DC temperature reaches a minimum corresponds to the frequency at which the CUT has its maximum gain (i.e., the center frequency of a narrow-band amplifier). Here, observation of a thermal tendency is defined as the observation of the temperature evolution when a parameter such as the frequency of the input tone is swept. The advantage of monitoring thermal tendencies is that it relaxes the design requirements for the built-in temperature sensors: when a relative minimum or maximum temperature point is extracted through multiple measurements, then the exact value of the sensor sensitivity (which is also affected by process variations) does not have to be known. Thus, the calibration prior to the built-in test does not have to include the measurement of the sensor's sensitivity. Figure 14 displays the result of 1000 Monte Carlo simulations, where the LNA's center frequency (at which the maximum voltage gain occurs) is plotted as a function of the frequency at which the minimum DC power (DC temperature) point is observed during a frequency sweep. As it can be seen, there is very good agreement between both frequency values, suggesting that DC temperature measurements can be used to monitor the frequency response of amplifiers.

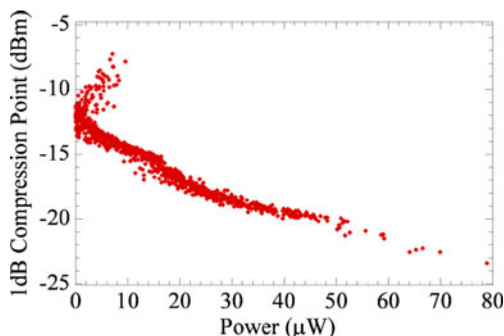

Fig. 12 1-dB compression point vs. DC power dissipation difference at M_C in the LNA due to the RF test signal. The power due to DC bias is not included

4 Incorporation of Temperature Sensing: Concepts and Examples

4.1 Differential Temperature Sensing

The use of a differential temperature sensor (DTS) provides high sensitivity to small temperature changes generated by the CUT's power dissipation and low sensitivity to ambient

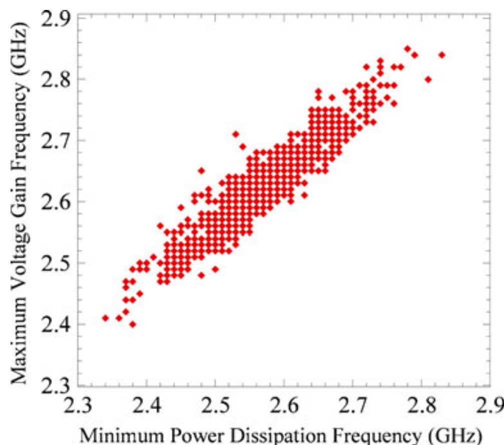

Fig. 14 Thermal tendency analysis: simulated LNA center frequency vs. frequency at which the minimum DC power dissipation is observed

temperature changes [4, 6]. Such a sensor has two transducer devices (e. g. parasitic bipolar transistors), and its output voltage (or current) depends only on the difference of temperature between these transducers. Figure 15 shows a simplified representation of a DTS: the two transducers Q_1 and Q_2 sense the temperatures T_1 and T_2 respectively. The DTS output voltage can be written as

$$\Delta V_{OUT} = S_{DT} \cdot (\Delta T_2 - \Delta T_1) = S_{DP} \cdot P_{CUT}, \quad (5)$$

where S_{DT} is the differential temperature sensitivity of the sensor, and ΔT_1 and ΔT_2 are the temperature increases above the ambient temperature at the transducer locations due to the power dissipated by the CUT after activating it with a fixed ambient temperature near the sensing points. The impact of other on-chip power sources can be removed through a calibration step prior to the measurement [34]. Since the temperature change at the transducer's locations linearly depends on the CUT's dissipated power, S_{DP} corresponds to the sensitivity of the sensor to the power dissipated by the CUT [4]. As foreseen from Fig. 9, S_{DP} depends on the placement of the CUT and the DTS in the chip layout, and it is maximized when one of the transducers is at a faraway reference location that experiences a negligible differential temperature change while the other transducer is located close to the CUT. As an example, Fig. 16 shows the output voltage change of the DTS from [4] implemented in a 0.35 µm CMOS technology as a function of the distance *x* between the temperature transducer and an NMOS transistor acting as CUT. In this test configuration, the two temperature sensing devices are separated by 400 µm (distance transducer Q_1–CUT=*x*, whereas distance transducer Q_2–CUT=400 µm+*x*). Measurements are shown for two different DC CUT power dissipation magnitudes. As it can be seen, these sensors provide enough sensitivity to detect temperature increases generated by power dissipations in the µW range. The settling times of differential temperature measurements depend on the distance between the transducer and the CUT as well as the bandwidth of the sensor's amplifier configuration. As elaborated in [34], a short settling time below 10 µs is achievable when the sensing device is within 10 µm of the CUT.

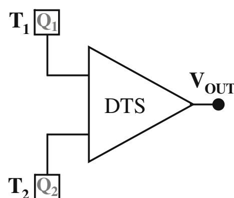

Fig. 15 Symbol of a differential temperature sensor (DTS). T_1 and T_2 are the temperatures of the transducers Q_1 and Q_2, respectively. V_{OUT} is proportional to T_2–T_1

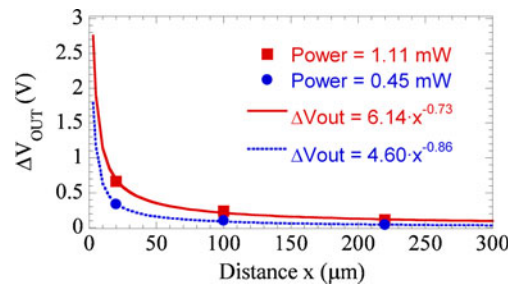

Fig. 16 Output voltage change of the DTS in [4] as a function of the distance between the temperature transducer 1 and an NMOS transistor for two different bias conditions. The distance between both temperature transducers is 400 µm

4.2 Observing DC and RF Power with Temperature Sensors

Figure 17 shows the layout of a chip fabricated in a standard 0.25 µm CMOS technology. It contains a narrow-band LNA as CUT and a differential temperature sensor whose schematics are displayed in Fig. 18. The LNA is a classical single-ended cascode type with inductive source degeneration, and the differential temperature sensor is based on a conventional operational transconductance amplifier topology. The differential pair (bipolar transistors Q_1 and Q_2) is imbalanced when the temperatures of Q_1 and Q_2 are different, causing the output voltage to change. The zoom in Fig. 17 shows two resistors named R_1 and R_2 that

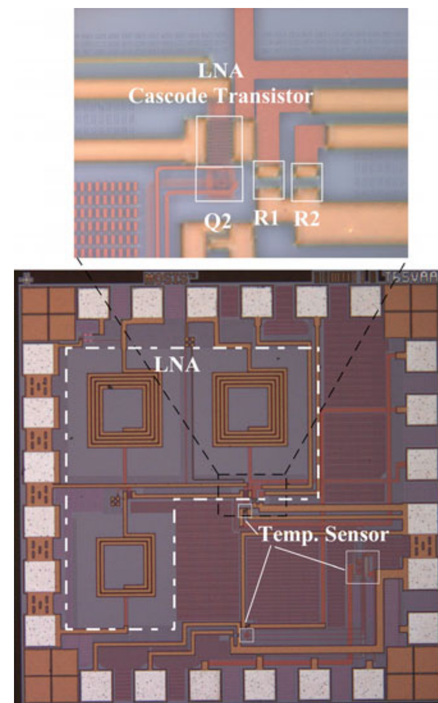

Fig. 17 Chip containing an LNA used as CUT and a differential temperature sensor. The small squares of the sensor indicate the locations of the temperature sensing devices, and the large square surrounds the bias/amplification circuitry. Technology: 0.25 µm CMOS

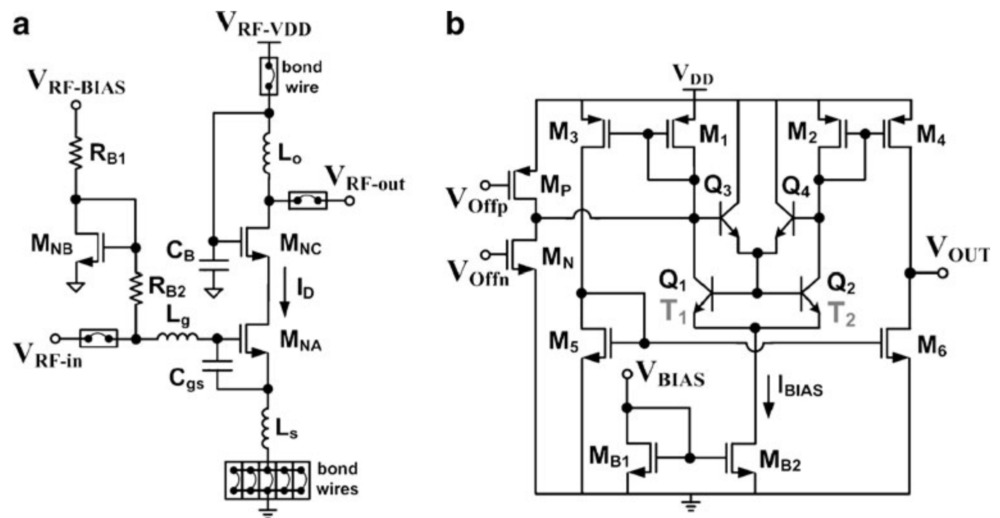

Fig. 18 **a** Schematic of the LNA used as CUT, **b** schematic of the DTS. Q_1 and Q_2 are the temperature sensing devices

are located 25 μm and 45 μm away from one temperature sensing device (Q_2). The plots in Fig. 19 were obtained by individually activating these two resistive devices. In both cases, the power dissipated by one resistor was swept while measuring the associated sensor output voltage change, showing that the sensor is able to track the power dissipated by R_1 with a sensitivity of 117 V/W and the power dissipated by R_2 with a sensitivity of 64 V/W. The linear range is approximately 8.5 mW and 16 mW, respectively. More details about the operation of both circuits can be found in [5], whereas the remainder of this section introduces new measurements obtained with this test chip by inducing CUT performance variations while observing the sensor output.

The CUT has two controllable inputs: $V_{RF\text{-}in}$ (RF signal input) and $V_{RF\text{-}BIAS}$ (DC bias of the LNA). A change of the DC value applied to $V_{RF\text{-}BIAS}$ varies the LNA bias current and therefore its performance parameters such as gain. Thus, dispersion of the LNA gain can be emulated by altering $V_{RF\text{-}BIAS}$. In this section, the different bias conditions for the circuit in Fig. 18a are named A ($V_{RF\text{-}BIAS}$=3.3V, I_D= 10.59 mA, Gain=9.79 dB@850 MHz), B ($V_{RF\text{-}BIAS}$=2.6 V, I_D=8.05 mA, Gain=8.56 dB@850 MHz), and C ($V_{RF\text{-}BIAS}$= 2.0 V, I_D=5.80 mA, Gain=6.58 dB@850 MHz). Figure 20 shows the electrically-measured frequency responses of the LNA for the aforementioned conditions. As expected, the lower the bias current, the lower the LNA's gain is. Thermal tendencies are plotted in Figs. 21 and 22 for comparison. Figure 21 shows the measured DC sensor output voltage as a function of the frequency of a −10 dBm input tone applied to the LNA. It can be seen that the DC value provided by the temperature sensor depends on the LNA bias condition and on the frequency-dependent LNA gain. Notice that the minimum of the sensor output matches with the maximum of the LNA's frequency response. Figure 22 shows the sensor's

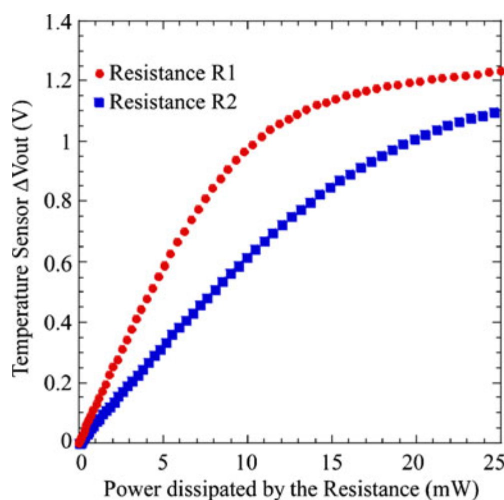

Fig. 19 Sensor DC response as function of the DC power dissipated by the resistors R_1 and R_2 located at distances of 25 μm and 45 μm from the temperature sensing device, respectively

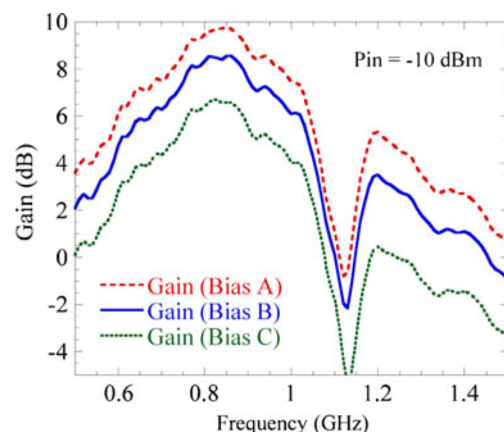

Fig. 20 Frequency response of the LNA for three different voltage levels applied to V_{RF_BIAS} : A=3.3 V, B=2.6 V, C=2.0 V

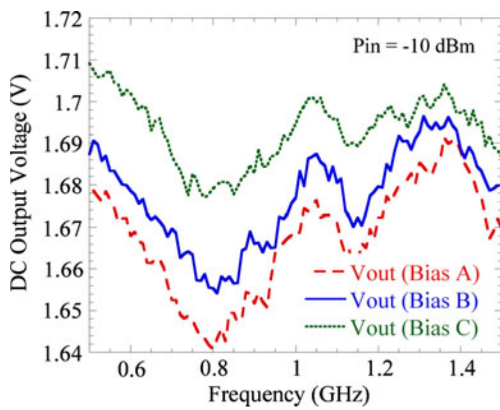

Fig. 21 DC output voltage of the temperature sensor vs. frequency of the RF input tone applied to the LNA

DC output voltage as a function of the RF power of a single input tone at 800 MHz. The different slopes of the linear approximations through the measured temperature data points indicate the different gains of the LNA for each bias condition. However, noise is observed in the form of data point scattering in Fig. 22 because the measurements have been extracted at DC. The measurement's immunity to noise can be reduced by increasing the power levels of the test signal or by using the heterodyne approach involving two test tones. The heterodyne measurement results in [5] show that the presented temperature sensor is able to track the temperature changes generated by input power levels as low as −35 dBm. These results reveal that performance variations can be monitored with a temperature sensor without contacting the CUT.

4.3 Potential Role of Temperature Sensors in the Calibration Process

The presented simulation results and measurements for the DC temperature sensing approach with low power levels indicate that the sensors are suitable to detect gross variations and faults. For the circuit discussed in the previous section, the voltage gain prediction accuracy in the DC domain is roughly ±2 dB. Being a thermal tendency, the 1-dB compression point prediction exhibits less spread (around ±1 dB). In a practical test approach with these fluctuations, the outputs of the sensors should be correlated to the actual specifications with statistical data from simulations or a number of measured samples. Alternate test methods based on embedded sensors are described in [8] and [1]. In general, it is essential to extract the statistical error between the sensor output and the specific CUT performance parameter through correlations prior to relying solely on the sensor outputs. From a system-level calibration point of view, the temperature sensors would aid by quickly providing fault identification information based on which tuning prioritizations can be made in the DSP (Fig. 6). Once the faulty block is known, the accuracy and effectiveness of the tuning mainly depends on the digital fine tuning resolution of the DACs or programmable elements in the block under calibration. Notice that the final performance evaluation in the DSP can be a system-level metric such as BER and EVM in order to determine the optimum control bits for a block that has been identified as deficient based on temperature measurements. To optimize for fault coverage and performance monitoring accuracy in the analog front-end, the combination of different sensors or the selection of the appropriate sensor for each block under test could be explored based on comparisons such as in [1]. One possibility that can be envisioned for such a combination is to employ temperature sensors for coarse measurements of the actual signal power at critical elements in the signal path while including dummy circuits [1] at blocks for which finer resolution is required to monitor variations due to fluctuations of the doping concentration in the proximity of the CUT.

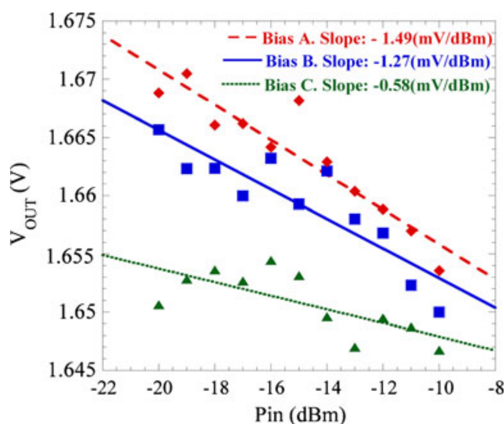

Fig. 22 DC output voltage of the temperature sensor vs. power of the input tone applied to the LNA. Input tone frequency=800 MHz

5 Conclusion

Increasing complexity of wireless SoCs together with rising CMOS process variations have led to numerous built-in test and self-calibration strategies. An outline of different approaches and trends was given in this paper, representing various design philosophies in academia and the industry. It has become increasingly popular to combine digital and analog techniques to tune for optimum system-level performance. Usually, better observability of faults and variations improves the accuracy or execution time of test and calibration routines, for which electrical detectors and process monitoring circuits are utilized. Towards this end, a temperature sensing approach has been assessed in this paper. Using an LNA as example, Monte Carlo simulations

and CMOS test chip measurements revealed that performance variations can be observed with an on-chip temperature sensor. Since this alternative technique does not require a connection to the CUT or signal path, it provides a non-influential method for monitoring variations.

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