

Exact Linearization Nonlinear Neutral-Point Voltage Control for Single-Phase Three-Level NPC Converters

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Abstract—This letter proposes a new control scheme for the neutral-point (NP) balance in single-phase three-level NP-clamped converters. The control is addressed considering the plant under study, a nonlinear time-variant system. A quasi-exact linearization is applied allowing the application of classic control techniques. The described method is simple, general, and suitable for buck and boost topologies, as well as for inverter or rectifier operating modes under either linear or nonlinear loading. Correct operation is verified under simulated and experimental operation.

Index Terms—Multilevel converters, neutral-point control, nonlinear control.

I. INTRODUCTION

PULSEWIDTH modulation (PWM) converters guarantee good harmonic quality on the ac side and excellent dc voltage regulation. Diode-clamped multilevel topologies introduced in [1] represent a straightforward way to increase dc-side voltage and nominal power levels while further reducing harmonic distortion [2]. Using these kinds of topologies comes at the cost of increasing control complexity, particularly through extra control loops for voltage equalization across the dc-link capacitors. An imbalance in intermediate dc-voltage levels would produce distorted ac voltage and current waveforms and might cause possible over-voltage damage in any of the power-switching devices.

Multilevel equalization in three-phase converters has been an active research topic for the last several years. Several approaches, such as special modulations, modification of PWM signals, etc., have been proposed and their effectiveness assessed [3]–[5]. Neutral-point (NP) voltage control in single-phase multilevel converters presents different features from the three-phase multilevel case. Probably, the most important is the fact that the nonlinearities in the single-phase case are located in isolated points, whereas in the three-phase case there are singular regions. This facility

makes possible an easier application of feedback linearization techniques. However, the problem has not attracted much attention, although multilevel single-phase converters continue being considered useful devices for several important applications such as powerfactor correction [6], traction [2], photovoltaics [7], audio amplifiers [8], etc. Several approaches have been developed to achieve dc-link capacitor charge balance. They may be categorized as linear and nonlinear control approaches.

Given the nonlinear time-varying nature of the control problem, the former approach approximates the process by first averaging the NP current over a line period and linearizing the expression for the NP voltage by differentiating it around a nominal operating point [9]–[11]. This model is used to design a standard proportional–integral controller feedback loop. The input is the difference between both dc-link capacitor voltages, and the output is either an offset to be added to the modulating wave [9], [10] or the difference between the transistor dead times [11] in each modulation period.

Nonlinear methods are based on the dual behavior of two pairs of switching combinations. In a combination, both members in each pair yield the same voltage level on the converter ac side but have an opposite effect on the state of charge of the dc-link capacitors [3], [12], [13]. The duration of each modulation period is shared by a switching combination coming from one of these pairs and another that has no effect on the dc-link voltage balance.

This letter describes a new control method based on a simple feedback linearization procedure to obtain a linear time-invariant model for the NP voltage. The feedback linearization process takes almost no time, is direct, and yields a linear, time-invariant model. With this linear model, well-known and easy-to-implement classic control techniques for obtaining the desired system response and disturbance rejection can be applied with greater accuracy than in previous approaches. The strategy benefits from design facilities of linear methods, while achieving convergence times similar to nonlinear ones. In other words, the linearization opens the possibility of choosing whichever linear controller the application demands. This feature is useful in situations where the NP voltage must get a concrete value different from a perfect equilibrium, as, for example, maximum power point tracking (MPPT) in photovoltaic (PV) applications with NP-clamped interfaces. The algorithm can be straightforwardly extended to other rectifier or inverter topologies and is very simple to apply to existing structures.

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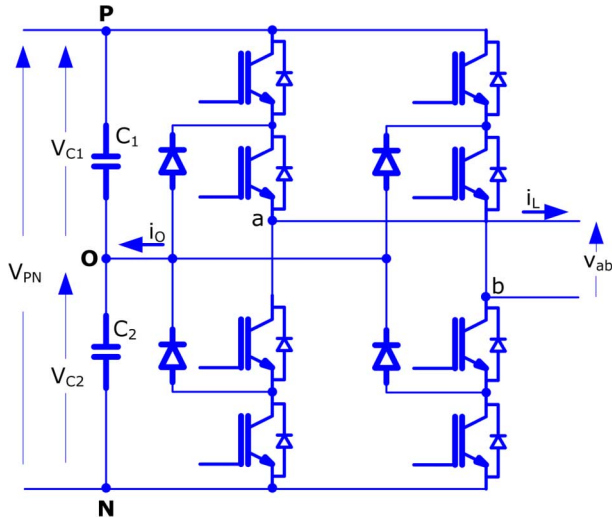


Fig. 1. Converter under study.

Section II of this letter briefly describes the switching scheme and converter operation considered herein. Section III focuses on an accurate mathematical description of the system. Starting from the electrical schematic of the converter, a nonlinear time-varying differential equation that models the system is extracted. Section IV focuses on the linearization process itself. Once the problem has been transformed to a linear time-invariant control design problem, a simple classic zero-pole network is assessed as an example control scheme to test the correct operation of the proposal by means of experimental testing in Section V.

II. CONVERTER OPERATION AND SWITCHING SCHEME

During normal operation, the converter function is to generate an ac voltage (v_{ab}) from a dc voltage (V_{PN}) by driving the insulated gate bipolar transistors (IGBTs) of Fig. 1 to a correct state. A more intuitive switching model of the system under study is shown in Fig. 2, where V_{PN} is the dc-side voltage, which for convenience will be called *output voltage*, v_{ab} is the ac-side voltage which will be called *input voltage*, and i_L denotes the ac-side current usually called *input current*. The variables V_{C1} , I_{C1} , V_{C2} , and I_{C2} represent the voltages and currents related to the dc-side capacitors. i_o represents the current entering the NP. This will play an important role in the control scheme.

In typical configurations, a converter outer control loop calculates the voltage v_{ab} , which should be generated by PWM signals using appropriate switches, S_a and S_b . Switches S_a and S_b can be placed in any of three positions, called *p*, *o*, or *n*, which correspond to the three voltage levels of the dc bus: V_{PN} , $V_{PN}/2$ (assuming a balanced dc-bus), and 0, respectively.

Given the input voltage value v_{ab} that must be synthesized, the converter operation can be segmented into four different zones.

- 1) *Zone 1.* ($V_{PN} \geq v_{ab} \geq V_{PN}/2$): The input voltage (v_{ab}) is generated from a PWM signal with voltage levels of V_{PN} and $V_{PN}/2$. This is accomplished by the use of switch-

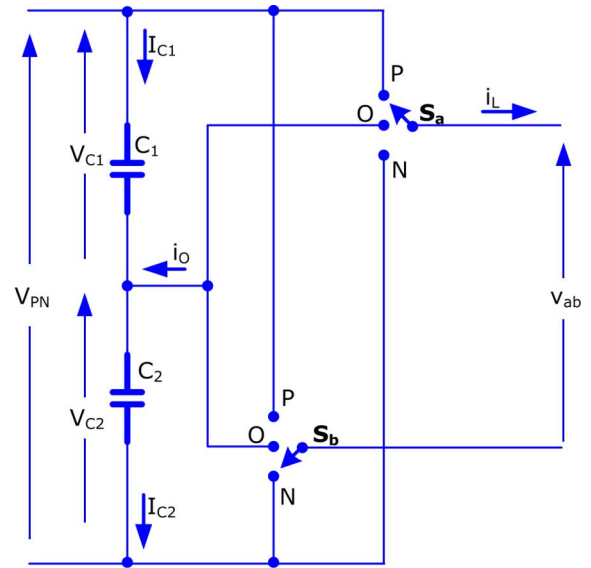


Fig. 2. Switching model of the converter under study.

ing states **PN** ($i_o = 0$) and either **PO** ($i_o = i_L$) or **ON** ($i_o = -i_L$).

- 2) *Zone 2.* ($V_{PN}/2 \geq v_{ab} \geq 0$): The input voltage is generated from a PWM signal with voltage levels $V_{PN}/2$ and 0. This is accomplished by the use of switching states **PO** ($i_o = i_L$) or **ON** ($i_o = -i_L$) and a zero-voltage switching state that is produced by any the states **PP**, **NN**, or **OO** ($i_o = 0$ for all of them).
- 3) *Zone 3.* ($0 \geq v_{ab} \geq -V_{PN}/2$): The input voltage is generated from a PWM signal with voltage levels 0 and $-V_{PN}/2$. This is accomplished by the use of a zero-voltage switching state, produced by states **PP**, **NN**, or **OO** ($i_o = 0$ for all of them), and either **OP** ($i_o = -i_L$) or **NO** ($i_o = i_L$).
- 4) *Zone 4.* ($-V_{PN}/2 \geq v_{ab} \geq -V_{PN}$): The input voltage is generated from a PWM signal with voltage levels $-V_{PN}/2$ and $-V_{PN}$. This is accomplished by the use of switching states **OP** ($i_o = -i_L$) or **NO** ($i_o = i_L$) and **NP** ($i_o = 0$).

Each switching state induces a different effect over the NP current i_o . It is clear that the NP current is null for maximum module input voltage (states **PN** and **NP**) and for the zero-input voltage switching position. In such positions, the NP voltage will remain invariant. When the converter has to be switched to an intermediate input voltage (states **PO**, **ON**, **NO**, or **OP**), two equivalent switching combinations may be chosen for the same voltage value: one will produce $i_o = i_L$ and the other will make $i_o = -i_L$. This well-known property will give an extra degree of freedom that may be used to control the NP voltage.

III. PHYSICAL SYSTEM MODELING

The objective of this section is to obtain an analytic expression of the plant transfer function that relates the capacitor voltage difference ($V_{C1} - V_{C2}$) with the current across the NP (i_o). The influence of the modulation is considered as well.

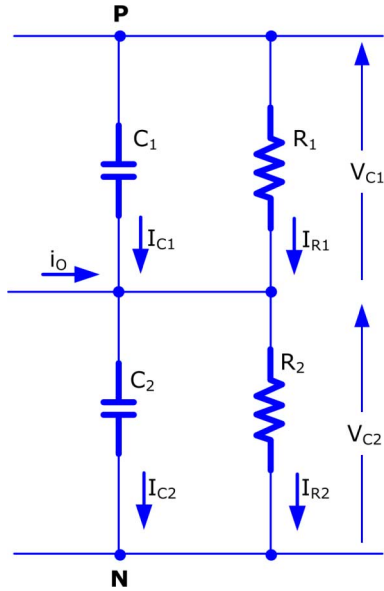


Fig. 3. Multilevel dc-bus physical model.

Fig. 3 represents an electrical schematic of the plant being modeled. Two resistors (R_1 and R_2) have been added to the diagram. These resistors model the dc-bus discharge resistors, placed in most power converters for security reasons. Applying Kirchhoff's law to the NP

$$i_o(t) + i_{C_1}(t) + i_{R_1}(t) - i_{C_2}(t) - i_{R_2}(t) = 0 \quad (1)$$

$$i_o(t) + C_1 \frac{dV_{C_1}(t)}{dt} + \frac{V_{C_1}(t)}{R_1} - C_2 \frac{dV_{C_2}(t)}{dt} - \frac{V_{C_2}(t)}{R_2} = 0. \quad (2)$$

Assuming device symmetry ($C_1 = C_2 = C$ and $R_1 = R_2 = R$) and defining $V_{\text{diff}}(t) = V_{C_1}(t) - V_{C_2}(t)$

$$\frac{dV_{\text{diff}}(t)}{dt} + \frac{1}{RC} V_{\text{diff}}(t) = -\frac{1}{C} i_o(t). \quad (3)$$

Equation (3) describes a linear time-invariant system. The control should be trivial, if $i_o(t)$ was the control variable. Unfortunately, it is not. Actually, the NP current value i_o is dependent on several factors: state scheduling producing same voltage and an opposite current, the instantaneous i_L current value, the converter operation zone and, in general, is a function of time.

From this point of view, the system in Fig. 3 can be considered a nonlinear time-variant system. For purposes of illustration, let us consider as an example the PWM period (T_{PWM}) represented in Fig. 4 and corresponding to the second operating zone. During the first part of the period, the PWM signal value is $V_{\text{PN}}/2$. This voltage level can be generated by two different switching states: PO , which is active during $t_{\text{on}1}$ will produce $i_o(t) = i_L(t)$, and ON , active during $t_{\text{on}2}$, will induce a current, $i_o(t) = -i_L(t)$. The average NP current over the PWM period will have a value of $\langle i_o(t) \rangle_{T_{\text{PWM}}} = ((t_{\text{on}1} - t_{\text{on}2})/T_{\text{PWM}}) \langle i_L(t) \rangle_{T_{\text{PWM}}}$, where $\langle i_L(t) \rangle_{T_{\text{PWM}}}$ is, also, the average value of $i_L(t)$ over the PWM signal period under study.

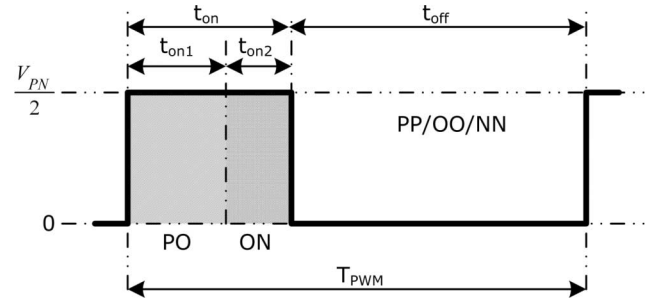
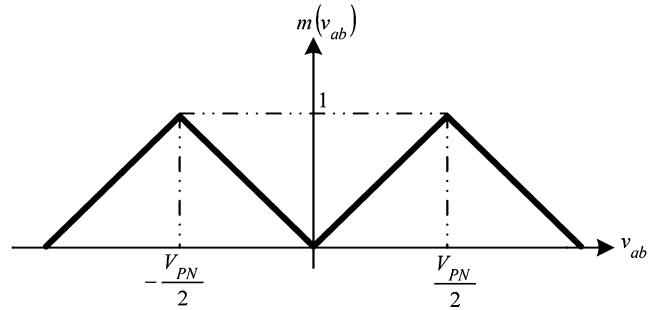


Fig. 4. Example PWM period for the NP balance with the converter in the second operating zone.


 Fig. 5. $m(v_{ab})$ function.

More generally, the average value of $i_o(t)$ over a PWM period can be expressed in the following way:

$$\langle i_o(t) \rangle_{T_{\text{PWM}}} = m(v_{ab}) \langle i_L(t) \rangle_{T_{\text{PWM}}} n(t) \quad (4)$$

where

- 1) $m(v_{ab})$ is a piecewise-defined function of the input value $v_{ab}(t)$ and of the switching scheme that is being used in the converter. It represents the part of the PWM period where the switching state is either PO , OP , ON , or NO , and therefore, where the i_o current can be controlled. It can be calculated as

$$m(v_{ab}) = \frac{t_{po} + t_{op} + t_{on} + t_{no}}{T_{\text{PWM}}}. \quad (5)$$

The function $m(v_{ab})$ defines the ratio $t_{\text{on}}/T_{\text{PWM}}$ in Fig. 4. This is a general way to introduce the influence of the modulation in the model. Assuming a switching scheme as the one shown in Section II, $m(v_{ab})$ is a piecewise function defined as follows:

$$m(v_{ab}) = \begin{cases} 2 - v_{ab} \frac{1}{(V_{\text{PN}}/2)}, & \frac{V_{\text{PN}}}{2} < v_{ab} \leq V_{\text{PN}} \\ v_{ab} \frac{1}{(V_{\text{PN}}/2)}, & 0 < v_{ab} \leq \frac{V_{\text{PN}}}{2} \\ -v_{ab} \frac{1}{(V_{\text{PN}}/2)}, & -\frac{V_{\text{PN}}}{2} < v_{ab} \leq 0 \\ 2 + v_{ab} \frac{1}{(V_{\text{PN}}/2)}, & -V_{\text{PN}} < v_{ab} \leq -\frac{V_{\text{PN}}}{2}. \end{cases} \quad (6)$$

A graphical representation of this function can be found in Fig. 5.

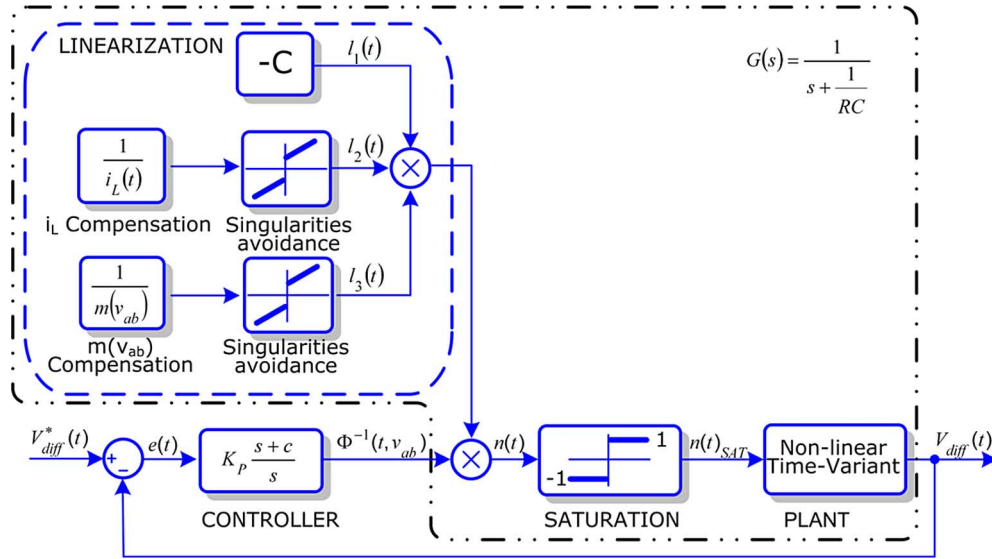


Fig. 6. Control system block diagram.

- 2) $n(t)$ is the actual control variable of the system. It is a function whose output is defined over the interval $[-1, 1]$. Its value is

$$n(t) = \frac{t_{po} + t_{no}}{t_{po} + t_{no} + t_{on} + t_{op}} - \frac{t_{on} + t_{op}}{t_{po} + t_{no} + t_{on} + t_{op}} \quad (7)$$

The function $n(t)$ defines the ratio $(t_{on1} - t_{on2})/t_{on}$ in the example of Fig. 4. This variable is a measure of the net charge injected or taken from one capacitor of the dc link to the other. Intuitively, a null $n(t)$ value implies that during the part of the PWM period where i_o is different from 0, each of the states that produces the same voltage and opposite currents are used for the same amount of time, and thus, $\langle i_o(t) \rangle_{T_{PWM}} = 0$ and the net charge transfer would be, consequently, null.

The differential equation that models the system may now be rewritten as

$$\frac{dV_{diff}(t)}{dt} + \frac{1}{RC}V_{diff}(t) = -\frac{1}{C}m(v_{ab})\langle i_L(t) \rangle_{T_{PWM}} n(t) \quad (8)$$

which can be considered a nonlinear time-variant system.

IV. SYSTEM LINEARIZATION

Equation (8) represents a nonlinear time-variant system. Fortunately, nonlinearities only affect the nonhomogeneous part of the differential equation. As the homogeneous part of (8) is linear and time-invariant, a feedback linearization procedure can be easily applied.

Consider a new function, namely $\phi(t, v_{ab})$ defined as

$$\phi(t, v_{ab}) = -\frac{1}{C}m(v_{ab})\langle i_L(t) \rangle_{T_{PWM}} \quad (9)$$

Introducing the inverse of the function described in (9) as a multiplicative term in the input of the nonlinear controlled plant, the resulting dynamics of the system under study become linear as if the actuated variable were $I_o(t)$. The new system dynamics are then linear and equal to those shown in (3).

TABLE I
POWER CONVERTER PARAMETERS

Parameter	Value
Grid Voltage	110 V_{rms}
L	6.6 mH
C	1000 μ F
R	12 k Ω
Load Resistance	132 Ω
DC Bus voltage	250 V
Switching frequency	8.2kHz

This linearization procedure is graphically described in Fig. 6. The introduction of the control algorithm inside the whole converter control is quite straightforward. Consider, for instance, a typical scenario where an outer voltage-control loop calculates a certain current reference to be followed by an inner current-control loop. The output of the current controller would be a certain average voltage to be created by means of the PWM signal, v_{ab} . At this point, the control algorithm described in this article would synthesize the switching signals for the switches (IGBT in this case) such that, in addition to obtaining the desired average voltage, the NP voltage is also properly controlled.

Regarding the extra measurements of the variables involved in linearization, it should be noted that the output voltage v_{ab} does not need to be measured as long as this value is fixed by the converter and, consequently, the algorithm already knows it. On the other hand, the output current measurement, in most cases, is already measured for current-control purposes, so usually no more sensors are needed.

V. EXPERIMENTAL RESULTS

Correct operation of this proposal has been verified under experimental testing. The algorithm has been tested on a 1 kW converter, with an inductance of 10 mH, dc-bus capacitors of 100 μ F, parallel resistors of 12 k Ω , and a load resistance of

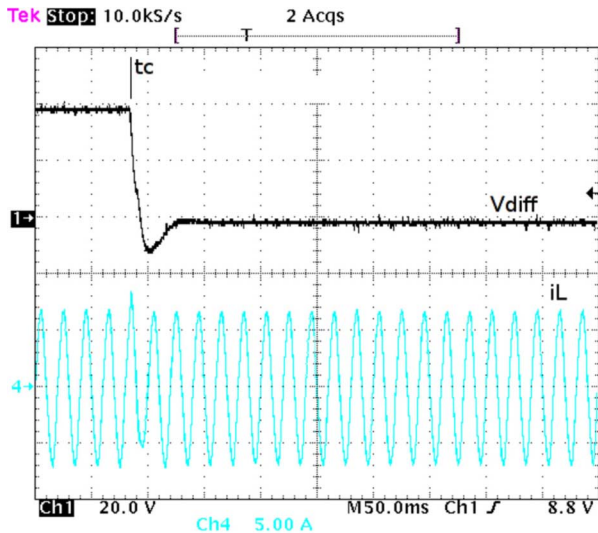
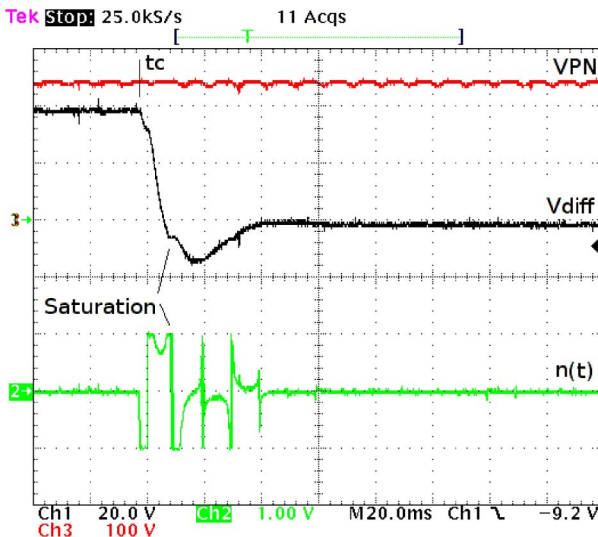
Fig. 7. Time response and effect over i_L current of the control algorithm.

Fig. 8. Time response and associated actuation variable of the control algorithm.

132 Ω . A statement of the experiment parameters is displayed in Table I.

Fig. 7 shows the time response of the system (V_{diff}) at the connection time of the control algorithm (t_c). The previous imbalance between capacitor voltages was 40 V. The bottom half of the scope shows the distortion effect over current $i_L(t)$. The variable V_{diff} reaches the null value successfully.

Fig. 8 focuses on the effect of the control algorithm over the dc-bus voltage, the resulting actuation variable $n(t)$ in Fig. 6, and the effects of plant saturation over the time response of the system. A 250 V dc-bus V_{PN} voltage has been configured. The initial voltage capacitor difference was 40 V. Influence over the dc-bus voltage is undetectable, and although the control is saturated several times, the system reaches a null value successfully.

Finally, Fig. 9 shows the algorithm behavior when a nonlinear load is connected to the converter. In this case, the load periodically changes its value between 264 and 132 Ω with a frequency

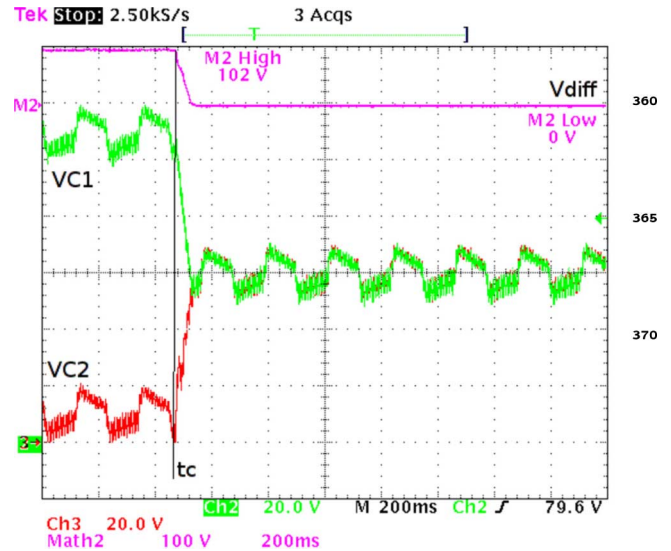


Fig. 9. Control system behavior under nonlinear load operation.

of 5 Hz. The initial difference before the control algorithm connection time (t_c) between capacitor voltages was 102 V. A scope capture shows the evolution of V_{diff} at the top and at the bottom the variables V_{C1} and V_{C2} . The control algorithm is not affected by the connection of this kind of load and the result is again successful.

VI. CONCLUSION

This letter has presented a novel control algorithm to balance the capacitors' voltage of a three-level NPC single-phase rectifier. The proposed algorithm is a simple and easy-to-implement linearization. The algorithm makes possible further analytical approaches to NP equalization control. The procedure demonstrates a successful behavior by means of experimental testing under different operating conditions, such as linear and nonlinear loading under a transient regime. The proposed algorithm can be easily extended to buck rectifiers, buck and boost inverters, and to other switching strategies and is independent of the converter's outer control loops. For these reasons, it can be easily applied to existing converters.

REFERENCES

- [1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.
- [2] S. Dieckerhoff, S. Bernet, and D. Krug, "Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1328–1336, Nov. 2005.
- [3] N. Celanovic, D.-H. Lee, D. Peng, D. Boroyevic, and F. Lee, "Control design of three-level voltage source inverter for SMES power conditioning system," in *Proc. 30th Annu. IEEE Power Electron. Spec. Conf.*, 1999, pp. 613–618.
- [4] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM—a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," *IEEE Power Electron. Lett.*, vol. 2, no. 1, pp. 11–15, Mar. 2004.
- [5] W.-S. Oh, S.-K. Han, S.-W. Choi, and G.-W. Moon, "Three phase three-level PWM switched voltage source inverter with zero neutral point po-

- tential," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1320–1327, Sep. 2006.
- [6] P. Barbosa, F. Canales, J. Burdio, and F. Lee, "A three-level converter and its application to power factor correction," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1319–1327, Nov. 2005.
- [7] P. Barbosa, H. Braga, M. Rodrigues, and E. Teixeira, "Boost current multilevel inverter and its application on single-phase grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1116–1124, Jul. 2006.
- [8] V. Antunes, V. Pires, and J. Silva, "Narrow pulse elimination PWM for multilevel digital audio power amplifiers using two cascaded H-bridges as a nine-level converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 425–434, Mar. 2007.
- [9] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: theory, design and operational limitations," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet., Record*, 1997, pp. 1336–1343.
- [10] B.-R. Lin and T.-L. Hung, "Novel single-phase ac/dc converter with two PWM control schemes," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, no. 3, pp. 1000–1010, Jul. 2002.
- [11] C. Osawa, Y. Matsumoto, T. Mizukami, and S. Ozaki, "A state-space modeling and a neutral point voltage control for an NPC power converter," in *Proc. Power Convers. Conf.*, 1997, pp. 225–230.
- [12] J. Carter, C. Goodman, H. Zelaya, and S. Tran, "Capacitor voltage control in single-phase three-level PWM converters," in *Proc. Record 5th Eur. Conf. Power Electron. Appl.*, 1993, pp. 149–154.
- [13] J.-H. Song, S.-J. Cho, I. Choy, and J.-Y. Choi, "New PWM method for single-phase three-level PWM rectifiers," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1997, pp. 283–287.
- [14] J. Salaet, A. Gilabert, J. Bordonau, S. Alepuz, A. Cano, and L. Gimeno, "Nonlinear control of neutral point in three-level single-phase converter by means of switching redundant states," *Inst. Electr. Eng. Electron. Lett.*, vol. 42, pp. 304–306, Mar. 2006.
- [15] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. Gimenez, "A new simplified multilevel inverter topology for DC–AC conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1311–1319, Sep. 2006.
- [16] R. Ghosh and G. Narayanan, "A simple analog controller for single-phase half-bridge rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 186–198, Jan. 2007.
- [17] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted pwm control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 178–185, Jan. 2007.
- [18] W. Levine, *The Control Handbook*. Boca Raton, FL: CRC Press, 1996.