Some experiments on chattering suppression in power converters

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Abstract— **This paper contains some experiments based on the paper *Chattering Suppression in Multiphase Power Systems* by Hoon Lee, Andrey Malinin, and Vadim I. Utkin that will appear in *International Journal of Control*. In that paper, the use of multi-phase converters and an appropriated phase shift allows reducing chattering to desired level under given switching frequency in the so called "ripple cancelation" or "harmonic cancelation". Additionally this strategy would consider sliding mode as a suitable substitute over the Pulse Width Modulation because of the benefits in sliding mode control, e.g. the ability to achieve desired system responses regardless of a certain level of parameter changes.**

A half-bridge buck converter prototype was built and the chattering suppression reported in the Hoon Lee at al. paper has been checked comparing the power converter performances operating with 1-phase and 4-phases respectively.

I. INTRODUCTION

Switched mode power converters lie at the heart of DC power supplies, bringing the advantages of high efficiency and low mass. The converters can be represented mathematically as nonlinear time-varying dynamical systems. They can be modelled as variable structure systems because of the abrupt topological changes that the circuit, commanded by a discontinuous control action, undergoes. Traditionally, controls using Pulse Width Modulation(PWM) are common for controlling DC-DC converter systems, but Sliding Mode Control (SMC) has come to attention as suitable substitute over the PWM control because of the benefits it involves, e.g. the ability to achieve desired system responses regardless of a certain level of parameter changes. Many papers can be found in the literature about SMC amd power converters, for example [1], [2], [3], [4]. However, the main drawback of the SMC is the appearance of undesirable oscillations having finite amplitude and frequency due to the presence of unmodelled dynamics or discrete time implementation. This phenomenon, so-called chattering, may lower control accuracy or incur unwanted wear of mechanical components. An additional obstruction of sliding mode implementation in power converters is the fact that SMC yields to variable switching frequencies, which is not accepted in many applications.

Several solutions to reduce the chattering have been studied. In [5] a solution to totally eliminate chattering utilize

observers. Another way to decrease the chattering without designing any asymptotic observers is to implement a state-dependent switching gain for the discontinuous control [6]. However, for sliding mode control of power converter systems with "on/off" as the only admissible switching operation mode, any of the above methodologies cannot be applicable, and a natural way to reduce chattering is increasing switching frequency. This is not always possible due to the limitation of switching frequency or to the switching losses. As for fixed switching frequency, there are several strategies reported in the literature. For example, in [7] the duty cycle is defined as the equivalent control evaluated at the beginning of the control period:

$$d_k = \frac{u_{eq}(kT) - u^-}{u^+ - u^-}.$$

The weak point of this strategy lies in the need to know system parameters, which results in a loss of system robustness. Authors in [1], [8] and [9] propose the addition of a hysteresis cycle to the sliding mode control comparator. Several approaches, [10], [11], consider a variable bandwidth hysteresis cycle, which implementation depends on system parameters and is complex. Other electronic implementations of quasi-sliding controls are reported in [12], [13] where the fixed switching frequency is synchronized by an external signal d defined by a T_d-periodic bipolar pulses train. Finally, in [14] and [15] the duty cycle is defined so that the average of the sliding surface is zero in each commutation period.

V. Utkin and co-workers proposed a new challenge in multi-phase converter systems that allows reducing chattering to desired level under any given switching frequency. This can be achieved by providing an appropriate phase shift to implement the so-called "ripple cancelation" or "harmonic cancelation" method. In this paper this new challenge is implemented on a 4-phases, half-bridge Buck converter prototype. Power converter performance is compared to the 1-phase system. The paper is organized as follows: main results of Hoon Lee et al. are summarized in Section 2. The 4-phases Buck converter is described in Section 3 that also reports several experiments which, in turn, are compared to the 1-phase system. Conclusions are in Section 4.

II. MAIN RESULTS BY HOON LEE ET AL. [16]

Let us consider a system with an inner loop which is in charge of regulating an inner output y by means of a relay as in Figure 1 where the Phase-1 block corresponds to a relative degree 1, first order transfer function. Hence,

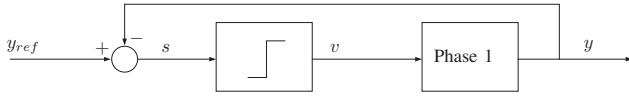$$\frac{ds}{dt} = \frac{dy_{ref}}{dt} - \frac{dy}{dt} = a - M\text{sign}(s) \qquad (1)$$

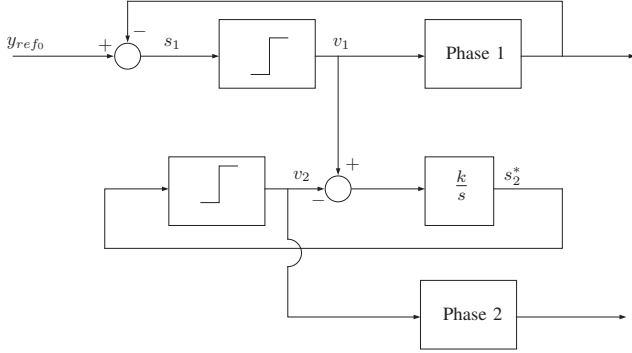Fig. 1. Inner loop in a 1-phase system.

Fig. 2. A 2-phase master-slave system.

Fig. 3. Periodic s_1 dynamics.

Fig. 4. Periodic (s_1, s_2^*) dynamics

where $a = \frac{dy_{ref}}{dt} + \frac{y}{\tau}$ and $M = \frac{k_0}{\tau}$. Note that there is sliding motion on $s = 0$ provided that $|a| < M$.

The chattering reduction method proposed in [16] is based on:

- a multiphase inner loop instead of a 1-phase one,
- modifying the reference appropriately, *i.e.* taking as a new reference $y_{ref_0} = \frac{y_{ref}}{m}$,
- taking benefit of some properties of the Fourier expansions.

They show two possible schemes called m-phase interconnected system and m-phase master-slave system. The experiments reported in this paper were performed in a 4-phase master-slave DC-DC buck converter. However, for simplicity, the main results in [16] are summarized here in the basis of a 2-phase master-slave model as in Figure 2.

As in the single phase case,

$$\frac{ds_1}{dt} = a - M\text{sign}(s_1) \tag{2}$$

$$\frac{ds_2^*}{dt} = kM\left[\text{sign}(s_1) - \text{sign}(s_2^*)\right] \tag{3}$$

where now

$$s_1 = y_{ref_0} - y_1 \tag{4}$$

$$s_2^* = k \int M\left[\text{sign}(s_1) - \text{sign}(s_2^*)\right] dt, \tag{5}$$

presumed that the relay gains and the dynamics in the two phases are identical.

In figure 3 s_1 dynamics is sketched close to $s_1 = 0$. Computing the period T from the figure yields

$$T = T_1 + T_2 = \frac{\Delta}{M - a} + \frac{\Delta}{M + a} = \frac{2\Delta M}{M^2 - a^2} \tag{6}$$

It is presumed that $\frac{dy_{ref_0}}{dt}$, and state variables are practically constant; *i.e.* the dominant term in $\dot{s}_1$ is $M\text{sign}(s_1)$.
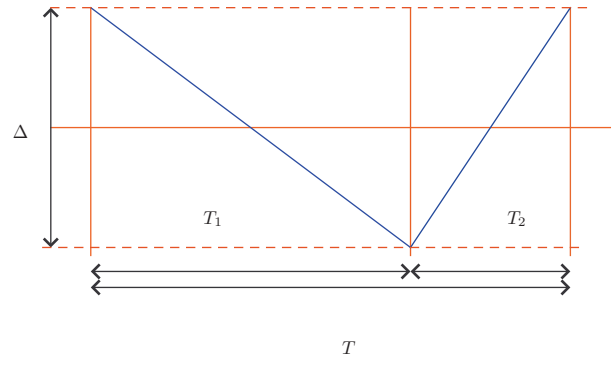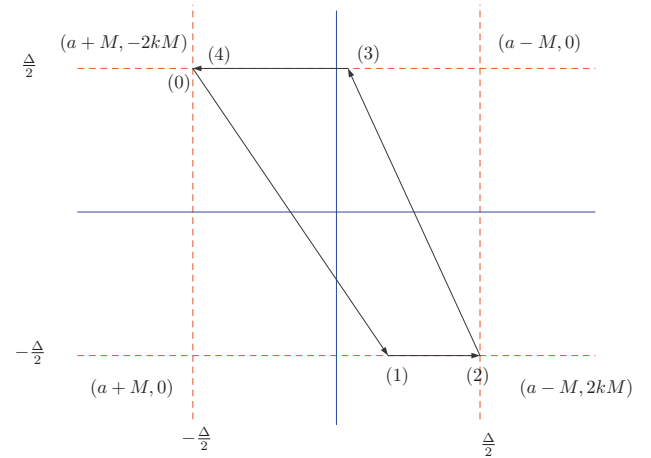
In figure 4, (s_1, s_2^*)-plane is sketched for $a > 0$, the vector fields values are written in the corners. From this figure, it can be seen that the phase shift becomes

$$T_\phi = \frac{\Delta}{2kM} \tag{7}$$

which is equal to the time from changing s_2^* from (2) to (3).

The scheme sketched in Figure 2 allows implementing a phase shift between phases 1 and 2 while the following inequalities hold

$$\frac{\Delta}{2kM}(M + |a|) < \Delta, \tag{8}$$

that is equivalent to

$$M + |a| < 2kM. \tag{9}$$

where Δ is the hysteresis width and k and M are the integral and relay gains respectively. See [16] for details.

The ideal sliding dynamics in the interconnected system results in $y_1 = y_2 = y_{ref_0}$.

A. Selection of Phase Number

Suppose that a master-slave m-phases linear system is to be designed so that the period chattering is the same in each

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phase, and two consecutive phases have the same phase-shift $\frac{T}{m}$. Since chattering is a periodic function, it can be represented using Fourier series with frequencies

$$\omega_n = \frac{2\pi n}{T}, \quad n = 1, 2, \ldots, \infty \quad (10)$$

Lemma

1) Let $f_1(t)$ be a periodic function, $f_2(t) \triangleq f_1(t + \tau)$ and $\mathcal{F}_1(t) = a_0 + \sum_n (a_n \cos(\omega_n t) + b_n \sin(\omega_n t))$, the Fourier series of f_1, then $\mathcal{F}_2(t) = \mathcal{F}_1(t + \tau)$.
2) Let a_n, b_n the cosine and sine coefficients respectively. Then if $\frac{n}{m}$ is not an integer, $a_n = b_n = 0$.

As a consequence of the lemma, all harmonics except for $n = lm$, $l \in \mathbb{Z}$ are suppressed in the output signal. As a result, the amplitude of chattering can be deduced to desired level by increasing the number of phases. Additionally, since the sliding surface $T-$average is zero, there is no continuous component in the Fourier expansion.

III. A 4-PHASES PARALLEL BUCK CONVERTER

A. The System Model

The results just reported will be applied here to a parallel buck converter. It is modelled by the next ODE

$$L\frac{di_1}{dt} = -R_L i_1 - v_C + E u_1 \quad (11)$$

$$\vdots \quad \vdots \quad \vdots \quad (12)$$

$$L\frac{di_m}{dt} = -R_L i_m - v_C + E u_m \quad (13)$$

$$C\frac{dv_C}{dt} = i_1 + \cdots + i_m - \frac{v_C}{R} \quad (14)$$

where i_k refers to the current in the k-th phase inductor, v_C refers to the output voltage and $u_k \in \{0, 1\}$ are the switches. Note that inductances L and losses resistors R_L are presumed to be the same for all phases.

Let us assume we deal with a m-phase buck converter which phases are shifted $T_\phi = \frac{T}{m}$. Then from equations (6) and (7),

$$\frac{\Delta}{2kM} = \frac{1}{m}\frac{2\Delta M}{M^2 - a^2}, \quad (15)$$

hence

$$k = \frac{m(M^2 - a^2)}{4M^2}. \quad (16)$$

Finally, equation (9) results in

$$|a| < M\left(1 - \frac{2}{m}\right), \quad (17)$$

Particularizing it for the half-bridge DC-DC buck converter gives

$$\frac{1}{L}\left|\frac{E}{2} - \left(\frac{R_L}{mR} + 1\right)v_C^*\right| < \frac{E}{2L}\left(1 - \frac{2}{m}\right) \quad (18)$$

which, in turn, taking $v_C^* = \alpha E$ and defining $\hat{\alpha} = \alpha\left(\frac{R_L}{mR} + 1\right)$ yields to the necessary and sufficient conditions

$$\hat{\alpha} > \frac{1}{m} \quad \text{if } \hat{\alpha} < 0.5, \quad (19)$$

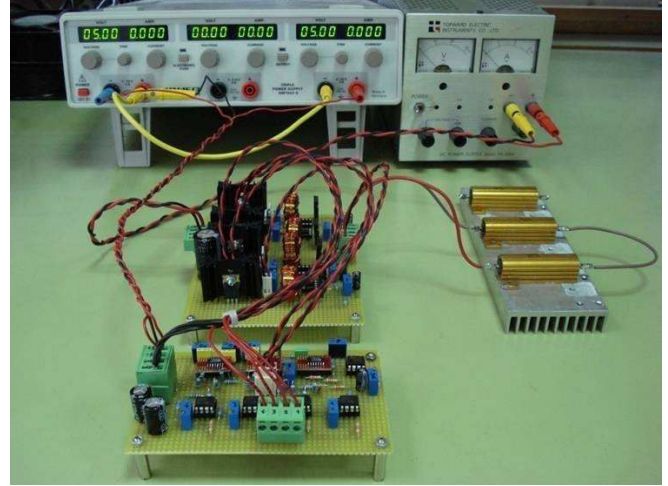| m	$\hat{\alpha} < 0.5$	$0.5 < \hat{\alpha}$
3	0.3333	0.6666
4	0.25	0.75
5	0.20	0.8
6	0.1666	0.8333

Fig. 5.   The full prototype

and

$$\hat{\alpha} < 1 - \frac{1}{m} \quad \text{if } \hat{\alpha} > 0.5. \quad (20)$$

Table I shows the minimum and maximum $\hat{\alpha}$ values for $m = 3, 4, 5, 6$

Remarks

1) It is not necessary to exactly set the switching period. Taking Δ sufficiently small will be enough.
2) T is linear with respect Δ.
3) Defining k properly yields the desired phase shift between consecutive currents.
4) k depends on the input voltage and on the current reference .
5) Differences in the load losses between phases will result in differences in the current averaged values.

B. The Plant

The electronic prototype is shown in Figure 5. Apart from the voltage source, back in the picture, the figure contains three boards corresponding to the 4-phase converter (in the middle), the control board (in front) and the loads (on the right-hand side).

The four phases converter can be seen in Figure 6. Each phase, in vertical in the picture (see Figure 7) contains, from right to left, a shunt and a current sensor, a coil and a mosfet transistor.

The system is controlled using two loops. A current inner loop, sliding mode controlled with an hysteresis band, and a
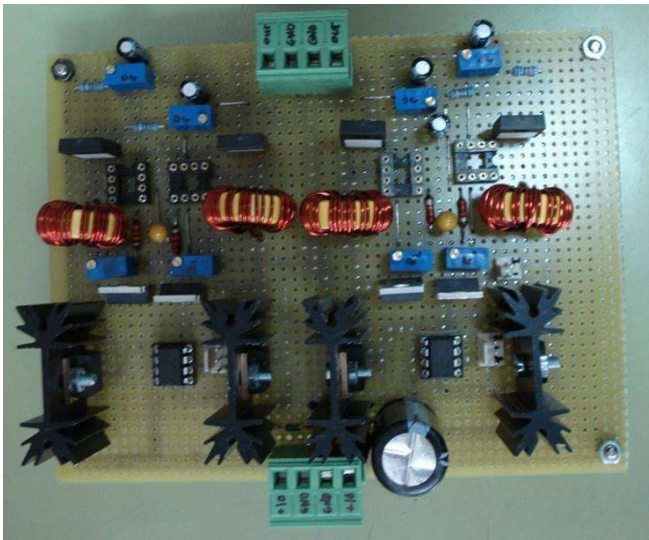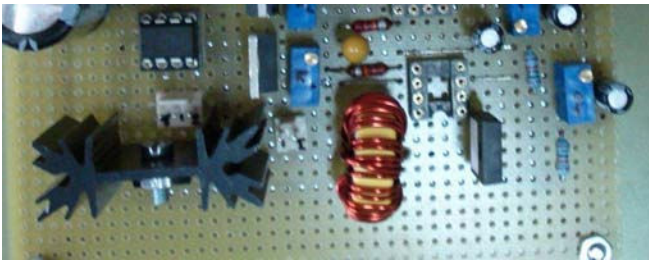
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Fig. 6.   The 4-phases power converter

Fig. 7.   Detail of one phase

Fig. 8.   Control signal board

Fig. 9.   Oscilloscope signals. 1 phase, 5 V

voltage outer loop that defines the current reference through a PI controller.

The control signal board, shown in Figure 8 consists of

- two connectors (on the left and at bottom). The first is connected to a ± 5 V. voltage, the second one sends the control signals to the converter,
- four comparators (integrated circuits very close to four potentiometers),
- four potentiometers labeled 1, 2, 3, 4 that are in charge of tuning the hysteresis cycle width,
- other three potentiometers, at the top of the picture, labeled I_2, I_3 and I_4, which are in charge of tuning the delay between phases,
- two more ones labeled P and I that are in charge of adjusting the PI voltage controller, and
- a last potentiometer on the right-hand side in the middle of the picture, which is in charge of adjusting the reference voltage.

Note that the control board were designed to support the four feedback inductor currents but only the first one will be used in the experiments.

The converter parameter values are $E = 10$ V, $L = 22\,\mu$H, $C = 10\,\mu$F and $R_L = 0.7\Omega$ (this includes 300 mΩ corresponding to semiconductor losses and 400 mΩ corresponding to inductor losses). The mosfet approximately

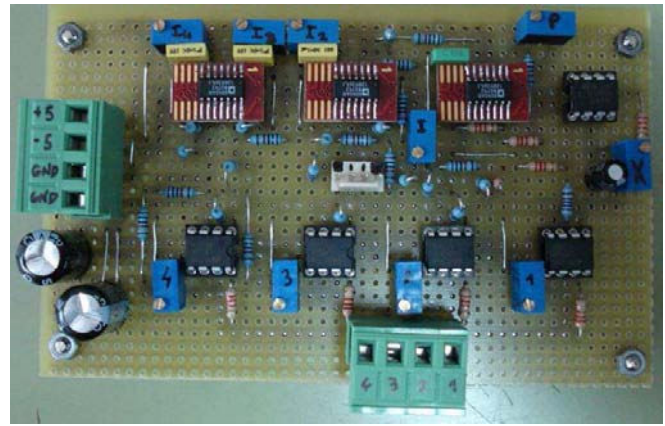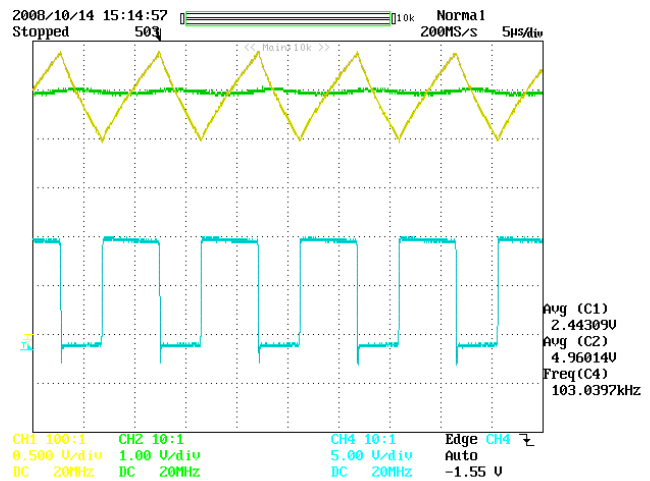works at a frequency of 100 kHertz.

IV. EXPERIMENTS

The power converter feeds a $2\,\Omega$ load providing several output voltages, namely 3, 5, 7 V. Also, the specific output voltage value $v_o = 4.59$ V is selected so that the relation T_{on}/T (*i.e.* the resulting duty cycle) equals to 50%. This case is particularly interesting because the Fourier coefficients corresponding to the harmonics that are multiples of four cancel. Thus the chattering reduction is really important. The cases $v_o = 3$ V, $v_o = 7$ V show that the system does not work properly, as it is stated by the theory.

Figure 9 shows the oscilloscope signals when the half-bridge, 1-phase DC-DC converter provides an output voltage of 5 V. The triangular signal corresponds to the input current, the rectangular one corresponds to the control signal while the third one is the output voltage. The average current value is 2.44 A and the chattering width is 0.47 A. The output voltage average is 4.96 V.

Let us consider now the half-bridge, 4-phases DC-DC converter. The four shifted currents are depicted in Figure 10 and the mosfet drain voltages in Figure 11. Both figures show
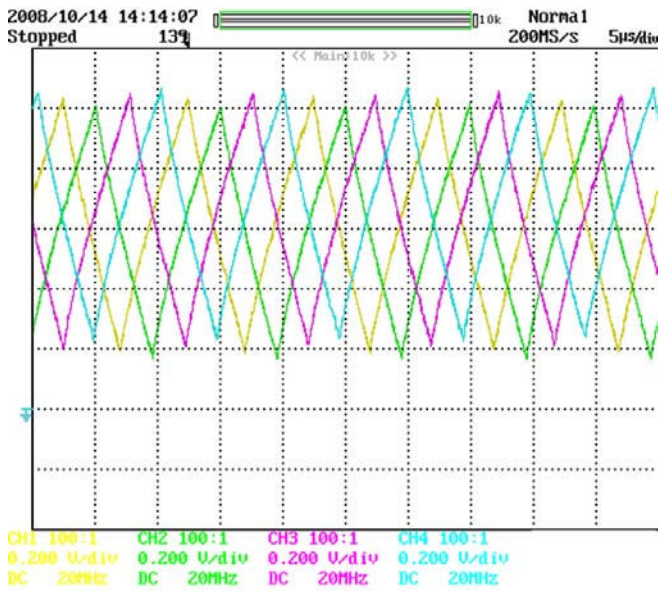
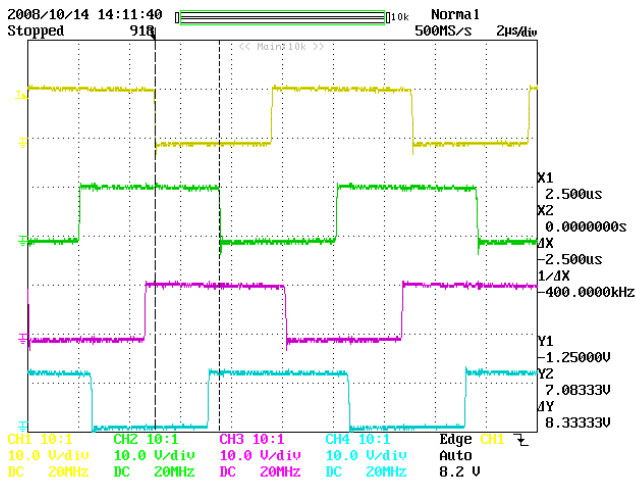**1526**

Fig. 10. Oscilloscope signals. 4 currents

Fig. 11. Oscilloscope signals. Mosfet drain voltages

Fig. 12. Oscilloscope signals. 4 phases, 5 V

Fig. 13. Oscilloscope signals. Voltage ripple and current chattering

that the master-slave algorithm operates properly with respect to current shifting. The current values of each phase are $i_{L_1} = 0.62 \pm 0.43$ A, $i_{L_2} = 0.6 \pm 0.42$ A, $i_{L_3} = 0.63 \pm 0.43$ A and $i_{L_4} = 0.66 \pm 0.42$ A. The output current, one of the duty cycles and the output voltage are depicted in Figure 12, which is zoomed in Figure 13 to show the voltage ripple and the current chattering. The average value of the output current is 2.48 A, with a chattering width of 0.095 A. Note the reduction in the current chattering from 0.47 to 0.095 A.

Chattering reduction in the case of 4.59 V output voltage is amazing. This is because the four duty cycles are equal to 0.5 and the Fourier coefficients corresponding to the harmonics that are multiples of four cancel.

In this case, output current and voltage are shown in Figure 14 and zoomed in Figure 15. The average value of the output current is 2.28 A, with a chattering width of 0.033
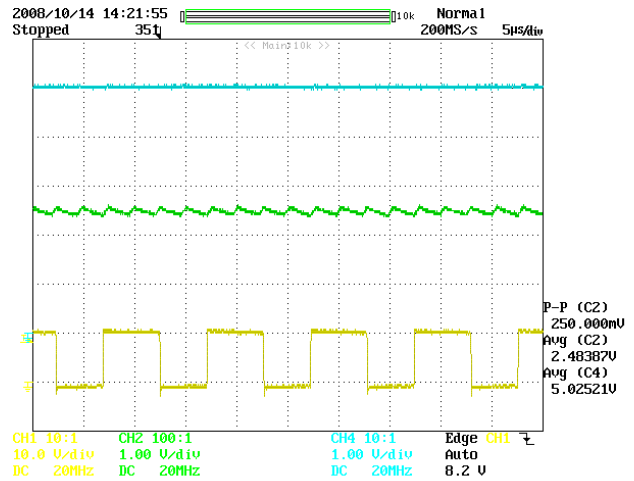
A. It is difficult to distinguish this chattering from measure noise. Note the reduction in the current chattering from 0.47 to 0.033 A.

Finally, Figure 16 shows the output current and voltage for the 4-phase, master-slave, DC-DC converter when a 7 V output voltage is demanded. Note that the system does not work properly. This is because our demand yields an $\hat{\alpha}$ which is not in the interval available using four phases as shown in Table I. Actually, the $\hat{\alpha}$ value for $\alpha = 0.7$ is $0.76 \notin (0.25, 0.75)$.

V. CONCLUSIONS AND FURTHER RESEARCH

The experiments carried out on a small power buck converter prototype are in agreement with the theoretical results about chattering suppression reported in "CHATTERING SUPPRESSION IN MULTIPHASE POWER CONVERTER" by Hoon Lee, Andrey Malinin, and Vadim I. Utkin. Although the controlled circuit results in a variable frequency system when the input or the reference voltage vary, the chattering suppression procedure prevents from
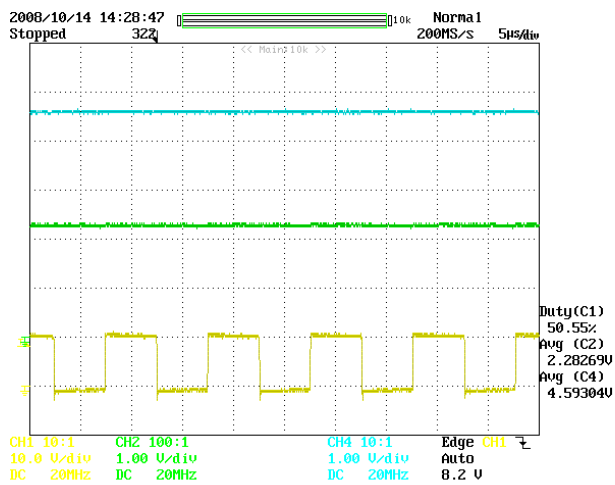
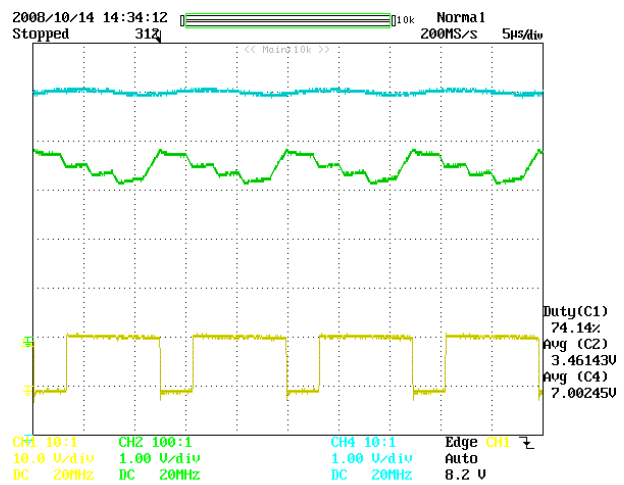Fig. 14. Oscilloscope signals. 4 phases, 4.59 V

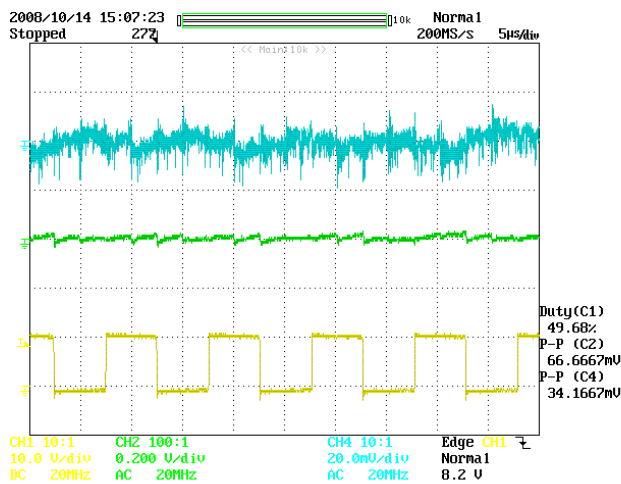
Fig. 16. Oscilloscope signals. 4 phases, 7 V

Fig. 15. Oscilloscope signals. Voltage ripple and current chattering

unexpected harmonics in the output voltage.

A key parameter in the chattering suppression procedure is the integral gain k which, in turn, depends on system parameters. The obtention of a robust procedure for getting the appropriate k value is left as a further research.

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