

A Novel Fully Differential Biopotential Amplifier With DC Suppression

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Abstract—Fully differential amplifiers yield large differential gains and also high common mode rejection ratio (CMRR), provided they do not include any unmatched grounded component. In biopotential measurements, however, the admissible gain of amplification stages located before dc suppression is usually limited by electrode offset voltage, which can saturate amplifier outputs. The standard solution is to first convert the differential input voltage to a single-ended voltage and then implement any other required functions, such as dc suppression and dc level restoring. This approach, however, yields a limited CMRR and may result in a relatively large equivalent input noise. This paper describes a novel fully differential biopotential amplifier based on a fully differential dc-suppression circuit that does not rely on any matched passive components, yet provides large CMRR and fast recovery from dc level transients. The proposed solution is particularly convenient for low supply voltage systems. An example implementation, based on standard low-power op amps and a single 5-V power supply, accepts input offset voltages up to ± 500 mV, yields a CMRR of 102 dB at 50 Hz, and provides, in accordance with the AAMI EC38 standard, a reset behavior for recovering from overloads or artifacts.

Index Terms—AC coupling, biopotential amplifiers, electrode offset potential.

I. INTRODUCTION

HIGH common mode rejection ratio (CMRR) and low-input voltage noise are two of the most desirable features for biopotential amplifiers in order to, respectively, reject external interference and enable high-resolution measurements. High common mode input impedance is also desirable in order to achieve a high CMRR despite the electrode's impedance mismatch. All these objectives are easy to achieve by using a high-gain fully differential front end. This approach, however, is usually not feasible in dc-coupled biopotential amplifiers because electrode offset potential can saturate input stages, hence limiting their admissible gains. An ac-coupled input stage is required.

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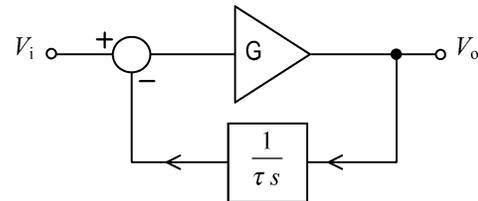


Fig. 1. Subtracting the output dc component from the amplifier input yields a dc suppression (or ac coupling) circuit.

There are two basic ac coupling methods: passive circuits that use serial blocking capacitors [1]–[3] and active circuits based on closed-loop control of the dc level [4]–[6]. Methods relying on serial blocking capacitors need additional high-pass filtering to remove the offset voltage of amplifier stages following the ac coupling network [7]. That offset arises from op amps offset voltages and also from dc voltage drops across bias resistors.

The active circuit approach is especially attractive because it yields a precise control of dc levels (thus rejecting any unwanted dc voltage and ensuring a proper dc level) and, additionally, simplifies the design of fast-recovery circuits, which quickly reset the proper dc levels after input overload.

Active ac coupling techniques reject dc input voltages (electrode and op amp offset) by negative feedback of the amplifier dc output voltage [4]–[6]. Usually, the feedback loop includes an integrator (see Fig. 1), which results in a high-pass first-order response

$$T(s) = \frac{s\tau}{1 + \frac{s\tau}{G}} \quad (1)$$

where G is the amplifier gain.

The lower cutoff frequency $f_L = G/2\pi\tau$ can be controlled through the integrator time constant τ . Decreasing τ allows the amplifier to quickly reach a proper dc level after an artifact saturates its output. To avoid low-frequency distortion, the nominal τ value must be restored once the artifact disappears.

Usually, the dc component is subtracted in a single-ended stage following the dc-coupled front end, whose gain must be limited to moderate values (say, ten) to prevent output saturation. As a result, the CMRR is quite limited and the second amplification stage contributes to the amplifier equivalent input noise. Furthermore, this solution cannot be applied to systems with differential analog-to-digital converters (ADC), which are quite convenient in electronic circuit design.

The alternative approach herein presented is a fully differential dc-suppression circuit (Fig. 2). It involves a fully differential integrator and also a fully differential feedback network which

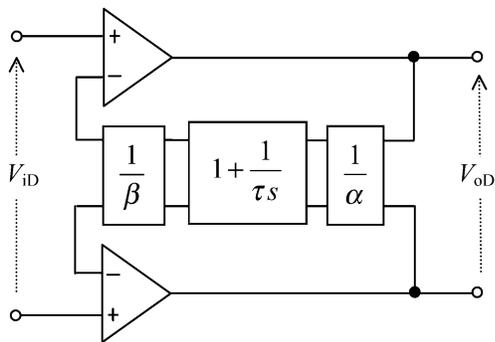


Fig. 2. Fully differential circuit for dc suppression implemented by feeding back the dc output voltage using a fully differential network.

preserves the balanced structure of the fully differential input amplifier. This approach can be considered a balanced extension of that presented in [6], which is based on the two-op-amp instrumentation amplifier. The proposed circuit inherits its good dc input range and low noise, whereas the CMRR becomes independent from passive component mismatch.

II. PROPOSED CIRCUIT

Fig. 2 shows a simplified model of the proposed biopotential amplifier. It includes a fully differential feedback network with two attenuators, one located at the input of the integrator stage and the other at its output. Assuming a negligible error voltage at the op amps inputs (this implies infinite gain op-amps), the ratio between differential-mode input and output voltages ($= G_{DD}$, differential input to differential output gain) is

$$A(s) = \frac{V_{oD}}{V_{iD}} = \frac{\alpha\beta s\tau}{1+s\tau}. \quad (2)$$

Midfrequency (nominal) gain A_{Dn} and high-pass cutoff frequency f_L are

$$A_{Dn} = \alpha\beta \quad (3)$$

$$f_L = \frac{1}{2\pi\tau}. \quad (4)$$

A. Circuit Implementation

Fig. 3 shows a possible implementation of the circuit in Fig. 2. If initially we assume $R_1 = R'_1$, $R_2 = R'_2$, $R_4 = R'_4$, $R_T = R'_T$, and $C_T = C'_T$, we have

$$\alpha = 1 + \frac{2R_4}{R_3} \quad (5a)$$

$$\beta = 1 + \frac{2R_2}{R_1} \quad (5b)$$

$$\tau = R_T C_T. \quad (5c)$$

As will be shown later, passive component mismatches do not degrade the CMRR.

B. DC Input Voltage Range

Assuming rail-to-rail output op amps and a single power supply, the maximal differential-mode dc-input voltage makes the integrator output reach V_{CC} . Because the integrator output

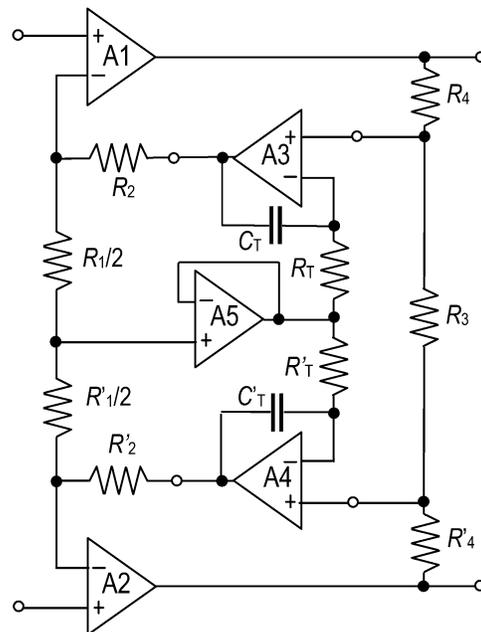


Fig. 3. Implementation of the method in Fig. 2. Because the proposed topology does not include any grounded component, its CMRR is ideally infinite.

is attenuated by β before being applied to the input, the admissible dc input voltage V_{idc} is

$$V_{idc} = \frac{V_{CC}}{\beta}. \quad (6)$$

C. Equivalent Input Noise

The equivalent input amplifier noise is mainly due to the op amps. Noise of R_1 and R'_1 appear directly to the amplifier's input but, adopting low value resistors, this noise can be neglected against the op-amps' noise contribution. The noise voltage of A1 and A2 also appears directly at the input, and the noise from A3 and A4 is attenuated by β . A5 contributes only common mode noise. The resulting equivalent input voltage noise power is approximately

$$E_{in}^2 = E_{A1}^2 + E_{A2}^2 + \frac{(E_{A3}^2 + E_{A4}^2)}{\beta^2}. \quad (7)$$

Usually, β is large enough to allow us to neglect the last term and the equivalent input noise is due only to A1 and A2. Resistors R_T also contribute to the overall noise but only for frequencies below f_L , that is, outside the bandwidth of interest. This contribution is similar to that of the biasing resistors in the passive circuit ac-coupling approach.

D. Common Mode Rejection Ratio

Given that the proposed circuit has no connections to ground, and disregarding stray capacitances, no current flows when applying a common-mode input voltage V_{iC} . In fact, all circuit nodes reach a potential V_{iC} , regardless of eventual mismatches in passive components due to their tolerance. Hence, the differential output is zero, which means $G_{DC} = 0$ (common mode input to differential output gain), and the CMRR ($= G_{DD}/G_{DC}$) is infinite. In practice, however, mismatches in differential and common-mode op amp open loop gain limit the global CMRR [8]. A good choice to minimize op amp

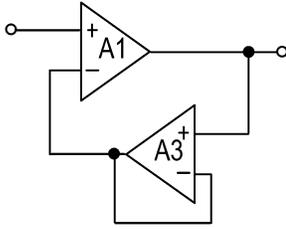


Fig. 4. Simplified model of the proposed amplifier for common mode voltages, useful for stability analysis. This model is valid for frequencies around the 0-dB gain frequency.

mismatches is to use dual IC models. This yields typical CMRR values greater than 100 dB at 50 Hz, even for general-purpose op amps. Because $G_{CC} = 1$ (common mode input to common mode output gain), a limited CMRR for subsequent stages would convert V_{iC} into a differential output, thus degrading the overall CMRR, but designing G_{DD} large enough minimizes that degradation [9].

E. Output dc Offset

The dc output voltage is due to the input offset voltage of the op amps composing the differential integrator in the feedback loop. The difference between the offset voltages of A3 and A4, amplified by α , appears as a differential mode output voltage V_{OS}

$$V_{OS} = \alpha(V_{OS_{A3}} - V_{OS_{A4}}) \quad (8)$$

which can be expressed as a function of β

$$V_{OS} = \frac{A_{Dn}}{\beta} (V_{OS_{A3}} - V_{OS_{A4}}). \quad (9)$$

F. Stability Considerations

The circuit in Fig. 3 is unconditionally stable for differential-mode voltages because the feedback gain attenuates them by $1/(\alpha\beta)$.

Stability problems could arise for common mode voltages because attenuators α and β amplify them by 1. Fig. 4 shows a simplified model to analyze this behavior at frequencies around the 0-dB gain frequency. If unity-gain-compensated op amps are used, A1 usually has a phase margin smaller than 60° which, when considering the additional phase shift introduced by the unity gain buffer A3, could lead to instability.

A possible solution that does not degrade the CMRR is to select for A3 (integrator stage) an op amp with a gain-bandwidth product GBP larger than the GBP of A1. By so doing, if the phase shift contributed by A3 at the unity gain frequency of A1 is negligible, the circuit is stable also for common mode voltages.

The unity gain buffer A5 propagates the common mode input voltage to the integrator stage. In this way, a common mode reference is provided to the full-differential integrator without any connection to ground, thus preserving the CMRR.

G. Design Example

As a design example, and in order to validate the previous analysis, an ECG amplifier has been designed, built, and experimentally tested according to the following specifications:

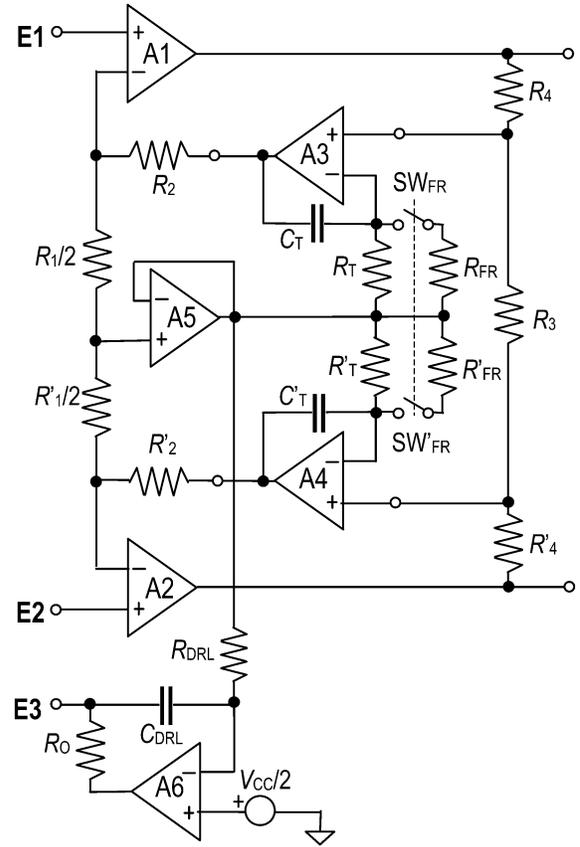


Fig. 5. Implemented ECG amplifier based on the topology proposed in Fig. 3.

$V_{idc} > \pm 500$ mV, $f_L = 0.05$ Hz, $V_{CC} = 5$ V and differential-mode gain $A_{Dn} \cong 500$.

For a dc input range of ± 500 mV, from (6) we obtain

$$\beta = \frac{V_{CC}}{V_{idc}} = 10 \quad (10)$$

and, from (3), the value of α necessary to achieve the required overall gain is

$$\alpha = \frac{A_{Dn}}{\beta} = 50. \quad (11)$$

Finally, the time constant $\tau = R_T C_T$ must be designed to obtain the desired cutoff frequency.

From (4)

$$R_T C_T = \frac{1}{2\pi f_L} = 3.18 \text{ s}. \quad (12)$$

Selecting standard components: $R_T = 3.3$ M Ω , $C_T = 1$ μ F, $R_{1/2} = 910$ Ω , $R_2 = 7.5$ k Ω , $R_3 = 2.2$ k Ω , and $R_4 = 56$ k Ω , results in

$$\alpha = 51.9, \quad \beta = 9.24, \quad A_{Dn} = \alpha\beta = 480,$$

and

$$f_L = 0.048 \text{ Hz}.$$

The complete circuit is shown in Fig. 5. A DRL circuit [10] was added to obtain a closed loop control of common mode input voltages and also to shift its dc value in order to allow single-supply operation [11]. The implementation uses

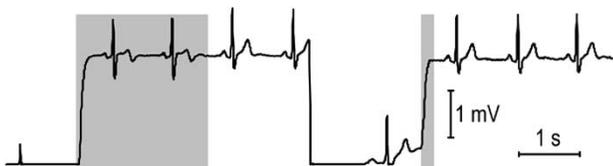


Fig. 6. ECG records obtained with the amplifier in Fig. 5 when operating the “fast-recovery” switches. Gray segments correspond to switches SW_{FR} , SW'_{FR} closed (see Fig. 5). In the first segment, the switches were manually operated to simulate an equipment startup. In the second segment, the switches were shortly closed, corresponding to a lead commutation. ECG amplitude is input referenced.

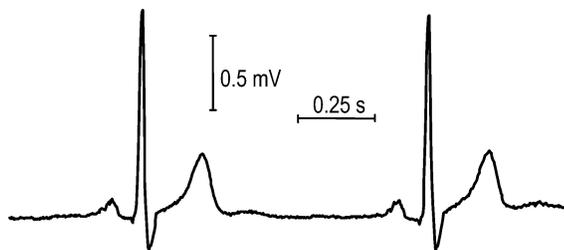


Fig. 7. ECG record acquired using the proposed amplifier. No further signal processing other than a band limiting to 128 Hz was performed. ECG amplitude is input referenced.

TLV2454 op amps in the input stage ($GBP = 220$ kHz) and TLV2474 ($GBP = 2.8$ MHz) for the integrator. Switches SW_{FR} and SW'_{FR} provide fast recovery by switching from the nominal R_T (3.3 M Ω) to $R_T/100$ (33 k Ω).

III. EXPERIMENTAL RESULTS AND DISCUSSION

The amplifier has been built by using metal-film resistors with 1% tolerance for R_1 to R_4 , 10% tolerance for R_T , and 10% tolerance capacitors (C_T). The measured CMRR of the amplifier without the DRL circuit is 107 dB at low frequency (1 Hz) and 102 dB at 50 Hz. Adding the DRL circuit, the CMRR theoretically increases by 30 dB at 50 Hz.

The fast recovery feature has been tested with real ECG signals (Fig. 6). When the outputs of A1 and A2 are saturated, switches SW_{FR} and SW'_{FR} close and the circuit quickly reaches its dc base level. In the first segment displayed, the switches were operated simulating a “manual reset” controlled by the operator according to [12, Sec. 3.2.13.1]. In this test, the switches remained closed during a “long” time, which resulted in a frequency distortion of the T wave of the ECG. In the second segment, the switches were closed during a “short” time, yet large enough to quickly reach the dc level. This could correspond to a base line reset performed automatically by the ECG equipment after an electrode commutation, as recommended in [12, Sec. 3.2.13.2]. Finally, Fig. 7 shows the acquired ECG signal in detail, showing that power-line interference is below the data acquisition card resolution (12 bit).

The proposed amplifier has a simple structure and is straightforward to design. The design procedure basically involves the proper selection of attenuation factors α and β . To achieve a large dc input range, from (10) β should be small; but, according to (7), this increases the noise contributions from A3 and A4. Therefore, a convenient strategy for low-noise design is to select the highest value of β compatible with the required dc input

range and then select the α value to achieve the desired gain in (3).

If a 3-V power supply is available, $\beta = 10$ yields a dc input range of ± 300 mV, which is the minimum required by the AAMI standard [12]. For this β value, the contribution of A3 and A4 to the equivalent input noise is small.

IV. CONCLUSION

Data acquisition systems that use differential ADCs are increasingly common because of both their improved interference-rejection capability and their larger dynamic range in low-voltage circuits, such as those in portable systems.

Differential ADCs, large CMRR, and low-noise design need fully differential biopotential amplifiers, whose design does not directly follow from that of amplifiers with single-ended output. Specifically, ac coupling and dc restoring, which are often performed on single-ended voltages, ask for novel solutions if they are to be performed on differential voltages.

This paper has proposed a dc suppression circuit that, in addition to ac coupling, provides a simple method for fast restoring the dc level of biopotentials. The proposed circuit does not include any grounded passive component, which makes the CMRR of the amplifier insensitive to the tolerance of passive components. Because the proposed circuit allows us to design a large differential gain for the first amplifiers stage, the CMRR and voltage noise are optimal. A circuit implementation with a single 5-V power supply yields 102-dB CMRR at 50 Hz, rejects up to ± 500 mV electrode offset, and quickly recovers from saturation with minimal ECG distortion.

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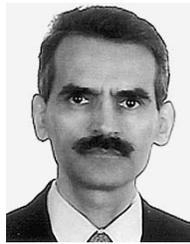
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