UNIVERSITÀ DEGLI STUDI DI PARMA

Dottorato di Ricerca in Tecnologie dell'Informazione

XXVI Ciclo

ACTIVE COMMON-MODE FILTER FOR PV TRANSFORMERLESS GRID-CONNECTED INVERTERS

Coordinatore:

Chiar.mo Prof. Marco Locatelli

Tutor:

Chiar.mo Prof. Carlo Concari

Dottorando: *Davide Barater*

Marzo 2014

Alla mia famiglia

Summary

List of Figures

List of Tables

Introduction

During the last years, it has been possible to witness a steady and progressive increase of energy production from renewable resources. In particular, the greatest increment has been registered for photovoltaic applications, due to the possibility to install low power implants easily integrated in the urban ambient, the so-called domestic photovoltaic.

Furthermore, the use of photovoltaic has been strongly encouraged by national governments through various forms of subsidies, in order to reduce the level of CO_2 emission, as established by the Kyoto Protocol. This, combined to a decrease in the cost for installed kW of the photovoltaic systems, has led to a real industrial boom in that sector in the years between 2008 and 2011.

In the last two years, due to a substantial downsizing of government grants, the growth rate has decreased, but it still continues to rise. In Europe, for instance, Germany claims a total solar capacity of 34.7 GW at the end of August 2013, with 7.6 GW of implants installed only in 2012, and 7.5 GW in 2011.

Considering that for European Union the target is to cover with renewable resources the 20% of the internal energy demands by 2020, it is likely to assume that the contribution of photovoltaic on the European energy mix is destined to rise again in the coming years.

To support the integration of new plants at the current growth rate it is necessary to achieve a further improving in the efficiency and a lowering for the installation costs of the implants.

A photovoltaic system can be islanded, when the energy is extracted from the

panels for supplying local loads, as in the case of remote agricultural areas where the electricity mains is not present, or grid-connected, where the energy recovered from the panels is directly injected into the mains.

Until now, where there was the possibility, grid-connected system has been considered the easiest and most efficient solution for photovoltaic plants. In fact, it allows extracting the maximum achievable power from the photovoltaic field in any situation, considering the mains as an infinite accumulator in which it is possible to inject, without restriction, all the energy harvested. Conversely, an islanded system is limited by the status of the battery pack and the presence of connected loads. It could happen that, in presence of a strong solar radiation, with the battery pack full charged and no load connected, the system would not work at all, wasting the total producible energy.

Following these considerations, in recent years there has been a remarkable proliferation, in both academic and industrial field, of new solutions for grid-connected inverters that were designed to maximize efficiency and reliability.

Initially, grid-connected inverters were realized employing a line frequency transformer, which, establishing a galvanic insulation between the photovoltaic source and the grid, facilitated the design issues. Nevertheless, because of its bulky dimension, costs, and additional power losses, the use of line frequency transformers was progressively abandoned.

A solution was represented by inverters that use a high frequency transformer, which, keeping the advantages of galvanic insulation, partially mitigate the losses due to the presence of the transformer. Actually, in high frequency transformer inverters there is an increment of the power stages, since the DC electric variables from the panels have to be modulated at high frequency and, after that, returned in output at line frequency, increasing the total complexity of the converter.

Moreover, the necessity to eliminate all additional power losses to obtain higher efficiency values has led to the complete abandon of the transformer, and transformerless inverters have gained their share of the market. Nowadays transformerless inverters are the most efficient grid-connected converters commercialized and some companies arrive to claim values of 98% of efficiency for their products.

Nevertheless, as the penetration into the structure of the mains of distributed energy sources began to become massive, new problems have arisen about the stability and power quality of the mains itself.

When the number of solar inverters connected to the same low voltage area becomes substantial, it is no longer possible to consider the mains as independent from the behavior of the inverters. Thus new regulations were established, and the inverters are not only required to provide the highest possible power to the grid, but to participate to the stability mechanism of the mains itself, for keeping the amplitude and frequency of the grid voltage under safety limits set by standards.

Obviously, this opens the way to new areas of research for the control of converters connected to the mains, enabling a smart management of resources, the so-called smart grid.

In this context the development of more efficient, reliable and long-lasting transformerless grid-connected inverters is of primary importance and also represents the topic of this work.

Chapter 1

Overview of requirements for Photovoltaic inverters

1.1 Introduction

A photovoltaic system consists of two fundamental elements: the photovoltaic field and the converter. Converters have to accomplish two tasks: extracting the maximum available power from the photovoltaic panels, and interfacing with the mains, injecting a sinusoidal current compliant with the norms that govern the connection to the grid of distributed energy sources.

Several algorithms have been proposed to make the panels work at the maximum power point of their characteristic (MPP), they are known as maximum power point tracking (MPPT) methods. The effectiveness and rapidity of these methods affect the overall performance of the converter and are therefore object of several studies [1].

However, the connection of the inverter to the mains represents the major issue, in particular for transformerless topologies.

The inverters have to obey to the standards given by the utilities companies about power quality, islanding detection, grounding, etc., that are analysed in details in the following.

1.2 Grid Interfacing

The requirements for the connection to the mains of low power distributed resources vary depending on the country considered. In Table 1.1 three different standards regarding grid connection were summarized: the US code IEEE 1547 [2], the German regulation VDE0126-1 [3] and the Italian rules CEI 0-21 [4].

In term of power quality, inverters have to inject a sinusoidal current at the grid frequency with a total harmonic distortion ratio THD less than 5% for the US code. Otherwise, German and Italian regulations specified a maximum value for both even and odd harmonics, in particular CEI 0-21 refers to European Union directive IEC 61000-3-2 [5] for devices with current rating till 16 A (the case reported in table 1), and IEC61000-3-12 [6] for current values between 16 and 75 A.

Besides harmonic distortion, the presence of a DC component in the output current is a major issue that must to be addressed. Considering the absence of galvanic insulation, it is possible to inject into the grid a DC current. The DC component has to be limited at less than 0.5% of the rated output current according to IEEE 1547.

The Italian regulation is even more severe. It considers two limit values: when the inverter is supplying less than 50% of its nominal power it is not allowed to inject a DC component higher than 0.5% of the nominal output current for more than 1 second, however, as in VDE0126-1 code, in any case if the DC current is greater than 1 A the inverter must disconnect from the grid within 200 ms.

The DC component is particularly detrimental because it can cause the saturation of the medium to low voltage MV/LV grid transformers. The saturation can rapidly lead to overheating, causing degradation in the insulation layer of the phase windings of the transformer itself and, in the worst case, to irreversible damages. Cases of

MV/LV transformers that ignite spontaneously, due to short circuits in the windings, are commonly reported by utilities companies.

The DC current problem is exacerbated in case of cascade multilevel topologies, where the total rejection of an offset value at the inverter output results more difficult to achieve than in conventional architectures. However this issue was deeply investigated and can be mitigated by improved measuring systems and control techniques [7].

Every standard provides regulations for the recognition of state of islanding operation, i.e. when the mains is not connected and the inverter is supplying only the local loads. The inverter must be able to detect when the grid is removed on purpose, by accident, or by damage, and take the appropriate countermeasures.

Typical case is when the mains is disconnected for maintenance work of the grid. In this situation it is mandatory that the inverter detects the event and stops working to guarantee the safety of people and equipment. The detection of islanding situation can be obtained through the monitoring of the grid voltage. Limit values and disconnection times are established for both amplitude and frequency of the grid voltage.

The available detection schemes are normally divided into two groups: active and passive. The passive methods just monitor grid parameters, using a digital PLL to control the variation of the grid frequency or line impedance estimator [8].

It could happen that in presence of resonant loads, when the mains is disconnected, the inverter continues erroneously to inject current into the grid with no variation of the frequency and amplitude of the measured voltage. In that case the total system, constituted by the inverter itself and the local loads, operates in a working point of relative stability, and the islanding situation becomes very difficult to detect [9].

The active schemes introduce a disturbance into the grid and monitor the effects. The disturbance causes a deviation from the working point and a variation of the grid voltage parameters that can be detected. Nevertheless, during the normal operation of the inverter, active methods introduce undesired disturbances, with a degradation of power quality. Moreover problems when multiple inverters are connected in parallel to the grid are also known to exist [10], [11].

In general passive methods are sufficient to comply to the regulations.

1.3 Active and Reactive Power Management

Initially, grid-connected inverters were required only to inject into the grid the maximum available power from the distributed sources, with unity power factor and a clean sinusoidal waveform. The policy of injecting all the available power to the grid is a good one, as long as distributed renewable power sources constitute a small part of the grid power capacity.

The fundamental characteristic of renewable power sources, especially photovoltaic, is to provide a variable amount of power depending on the weather condition, with the possible occurrence of severe oscillations of the delivered power. The classical example is the passage of clouds that reduce the solar radiation for a short period.

Until some years ago, it was thought that any random power fluctuation of the renewable sources would be compensated by the controllers associated with the large conventional power generators. Some of these generators would also control the overall power balance of the grid, system stability, and fault ride-through. Nevertheless, when renewable power sources provide the majority of the grid power, this paradigm is not valid anymore, and instability problems can arise in the mains.

For these reasons the new standards, as CEI 0-21 [4] and VDE0126-1 [3], impose to the grid-connected inverters to collaborate at the stability of the mains, requiring them to handle a certain amount of reactive power, and the possibility to modulate the delivered active power in function of the grid parameters.

For better understanding the requirements imposed to grid-connected inverters, it is worth to further analyze the mechanism involved in the process of mains balancing.

The structure of the mains was designed to deliver the power, generated in large power stations, to loads located at long distances from the power sources. Regardless of the type of electric central, the mains interfacing was realized with big synchronous generators (SG). When, in a power system, a generator acts alone, or it is by far the

strongest in an area, its frequency (i.e. the frequency of the grid), may be controlled via generator speed to remain constant in spite of load variations.

On the contrary, when the SG is part of a large power system, and electric generation is shared by two or more SGs, the frequency (speed) cannot be controlled to remain constant because it would forbid generation sharing between the SGs.

Speed droop control is the solution for generation sharing. The Automatic generation control (AGC) in Fig. 1.1 distributes the generation task between SGs and, based on this as input, the speed control system of each SGs controls its speed with an adequate speed droop, in order to achieve the desired power sharing.

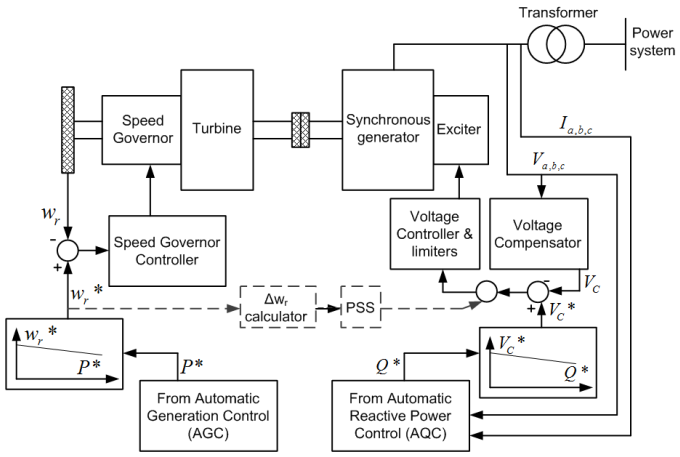


Fig. 1.1: Generic synchronous generator control system.

The motion equation, not considering friction effects, for a synchronous generator is:

$$J\frac{dw_r}{dt} = T_m - T_e \tag{1.1}$$

where T_m is the turbine torque, T_e the SG torque, and J the inertia. Considering small deviations:

$$\begin{aligned} w_r &= w_0 + \Delta w_r \\ T_m &= T_{m0} + \Delta T_m \\ T_e &= T_{e0} + \Delta T_e \end{aligned} \tag{1.2}$$

For a steady state $T_{m0} = T_{e0}$. Using the power instead of torque from (1.1) it is possible to have:

$$J w_0 \frac{d\Delta w_r}{dt} = \Delta P_m - \Delta P_e \tag{1.3}$$

Moreover, considering that P_e is delivered both to frequency independent and frequency dependent loads (such us motor loads), P_e can be expressed as

$$\Delta P_e = \Delta P_L + D\Delta w_r \tag{1.4}$$

leading to the general equation

$$J w_0 \frac{d\Delta w_r}{dt} + D\Delta w_r = \Delta P_m - \Delta P_L \tag{1.5}$$

As can be seen a variation of the load power request P_L results in a variation of the generator speed w_r and hence of the grid frequency. In presence of just one synchronous generator, the turbine torque can be modulated to restore the nominal frequency. As mentioned before in a power system with more than one SGs a certain variation of w_r have to be allowed. In Fig. 1.2 a speed droop governor is described, where ΔX is the variation of the valve position that controls the turbine torque. It is basically a proportional speed controller with R that provide the steady-state speed vs. load power

With two or more generators the frequency variation will be the same for all of them, thus the load sharing depends on their speed-droop characteristics (Fig. 1.3)

$$\begin{aligned} \Delta P_1 &= \frac{-\Delta f}{R_1} \\ \Delta P_2 &= \frac{-\Delta f}{R_2} \end{aligned} \tag{1.6}$$

Varying the w_0 reference speed the power delivered for a synchronous generator at a given frequency can vary as well. The task of determining the correct speed value

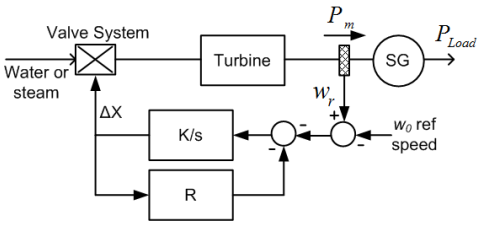


Fig. 1.2: Speed-Droop Governor.

that guarantees the overall balancing is assigned to the AGC. This have also to ensure the grid-frequency remains between the limits set by the legislator.

However, when the oscillations of the active power load P_L become too large or too abrupt they can lead the system to collapse. Cases of large areas black-out, due to the fluctuation of the power delivered by renewable power sources were reported by the Italian grid utility ENEL. To overcome this issue, the new regulation CEI-021 imposed to grid-connected inverters to limit the active power delivered in presence of a variation of the grid frequency. The behavior the inverters must ensure is described in Fig. 1.4.

When the frequency of the grid exceeds the threshold value of 50,3 Hz the inverter output power must linearly decrease, until it reaches the 0% of its nominal value at 51,5 Hz. The trajectory cannot simply be traveled backwards if a lower frequency value is restored, but for avoiding troublesome frequency oscillations, the inverter has to continue to deliver the output power at which it had limited until the frequency was restored to its nominal value for at least 3 min. Subsequently, the inverter can gradually return to inject into the grid all the available power from the renewable source.

Another important task of mains stability mechanism is to take under control the amplitude of the grid-voltage. The overshooting of the maximum grid voltage value can damage equipment connected to the grid, whereas a low voltage value can results in a reduction of the power supplying loads.

In a power system, as small frequency variations are used to regulate the power sharing between the generators, the reactive power flow can be controlled through

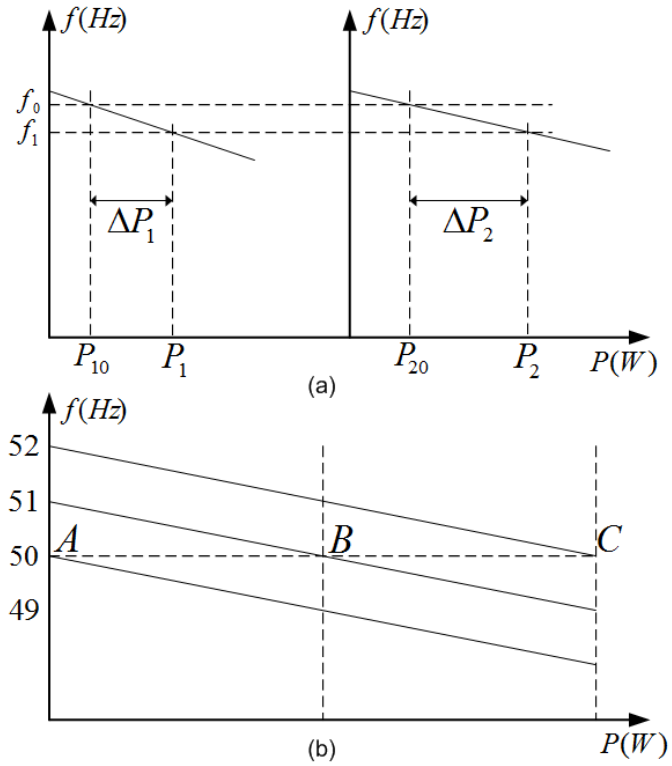


Fig. 1.3: Load sharing between two synchronous generators with speed-droop governor(a), change of the speed power characteristic due to w_0 variations (b).

the amplitude of the grid voltage. The loads require reactive power as well as active power and the power system has to provide for them. Considering the power flowing into a line at the point A of Fig. 1.5, it is possible to express the apparent power S as done in [12].

$$\begin{aligned} P + jQ = \bar{S} \quad &= \bar{U_1}\bar{I^*} = \bar{U_1}(\tfrac{\bar{U_1}-\bar{U_2}}{Z})^* = U_1(\tfrac{U_1 - U_2 e^{j\delta}}{Z e^{-j\theta}}) \\ &= \tfrac{U_1^2}{Z} e^{j\theta} - \tfrac{U_1 U_2}{Z} e^{j(\theta+\delta)} \end{aligned} \tag{1.7}$$

Thus the active and reactive power flowing into the line are

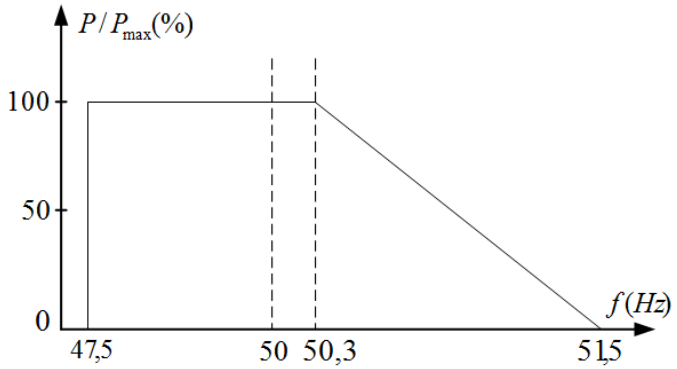


Fig. 1.4: Inverter output power variation in presence of an over-frequency condition.

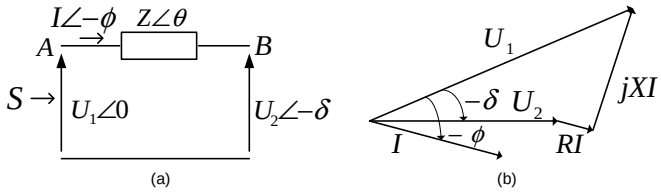


Fig. 1.5: (a) power flow through a line, (b) phasor diagram.

$$P = \frac{U_1^2}{Z}cos\theta - \frac{U_1U_2}{Z}cos(\theta+\delta) \tag{1.8}$$

$$Q = \frac{U_1^2}{Z}sin\theta - \frac{U_1U_2}{Z}sin(\theta+\delta) \tag{1.9}$$

expressing the impedance as $Z = R + jX$, (1.8) and (1.9) can be rewritten as

$$P = \frac{U_1}{R^2+X^2}[R(U_1 - U_2cos\delta) + XU_2sin(\delta)] \tag{1.10}$$

$$Q = \frac{U_1}{R^2+X^2}[X(U_1 - U_2cos\delta) - RU_2sin(\delta)] \tag{1.11}$$

or

$$U_2 sin(\delta) = \frac{XP - RQ}{U_1} \tag{1.12}$$

$$U_1 - U_2 cos(\delta) = \frac{RP + XQ}{U_1} \tag{1.13}$$

for power lines $X >> R$, R can be neglected and, if the power angle δ is small, it is also possible to approximate, $sin\delta = \delta$, $cos\delta = 1$. For this consideration (1.12) and (1.13) become

$$\delta = \frac{XP}{U_1 U_2} \tag{1.14}$$

$$U_1 - U_2 = \frac{XQ}{U_1} \tag{1.15}$$

(1.14) shows that the power angle δ depends on the real power flow P, i.e. the frequency dynamically controls the power angle and, thus, the real power flow, whereas according to (1.15) the voltage difference depends predominantly on reactive power Q, thus the amplitude voltage U_1 is controllable through Q.

However, active and reactive power controls are not totally decoupled. From (1.14) it is possible to note that the active power flowing into the power system affects also the voltage amplitude. Consider the case of a low-voltage area in Fig. 1.6, where several PV generators are presents. During summer days it could happen that, despite a high production of active power by the inverters, the corresponding power demand from electrical customers is low. In this situation the grid voltage can increase over the safety limit (red line in Fig. 1.6).

The grid voltage amplitude can be restored allowing the inverter to absorb a certain amount of reactive power. For these reasons, recent regulations provide reactive power absorption, as well as requiring certain protection relay mechanisms from the inverters regarding the voltage abnormal changes. In Italy, CEI 0-21, requires the capability of the inverters to deliver power with variable power factors (PF). The requested PF can assume any value values between 1 and 0.95 for nominal power plant of 3 kW. If the plant power exceeds 6 kW, power factors variation down to 0.9 must

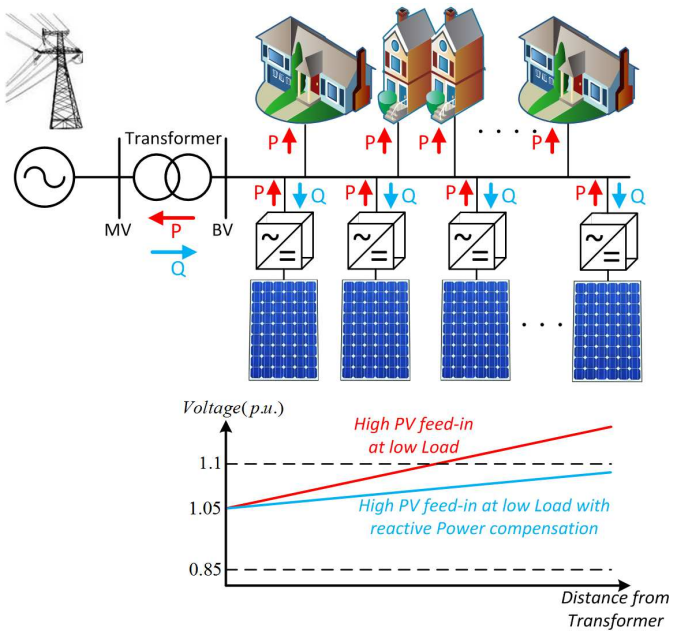


Fig. 1.6: grid voltage amplitude control in case of consistent presence of distributed power sources.

be supported. The reactive power output can be specified either as a fixed value, or as results from the grid parameters, as detailed in a standardized characteristic.

Moreover, demanding the supply of reactive power from distributed generators has a further advantage. Since delivering reactive power to loads results in increased power line currents, it is advantageous to produce the reactive power as close as possible to the place of its utilization. Therefore, grid-connected converters able to supply reactive power can support the reduction of the overall power losses in the power distribution structure.

1.4 Grounding

In transformerless grid-connected converters, there is a direct galvanic connection between the photovoltaic source and the grid, caused by the absence of the transformer.

This could lead to some problems. In fact, the neutral cable of the grid is connected to ground in correspondence of the MV/LV transformer of the mains. Since some regulations, as the US standard, or some particular type of photovoltaic panels, as the amorphous ones, require the grounding of one pole of the panels, without any precautions a short-circuit could occur at the source side of the converter. Specific inverter architectures have been designed for working when one of the two poles of the photovoltaic source is grounded [13].

Furthermore, even the most used technologies, monocrystalline and polycrystalline panels, require, for safety reasons, the grounding of the metallic support system on which they are mounted. Since the frame of photovoltaic modules is made by electrically conductive material, it results grounded as well. For these reasons a stray capacitance is present between the metal support frame of the modules and the photovoltaic cells (see Fig. 1.7) [14].

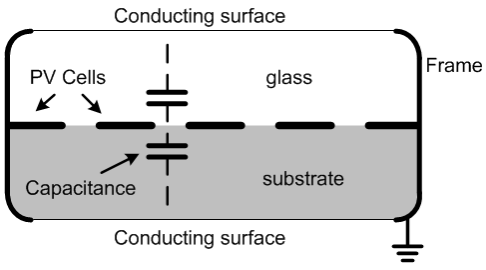


Fig. 1.7: Stray capacitance C_p in PV Module structure.

The value of the capacitance depends on the geometrical structure of the PV plant and on climatic conditions. The presence of moisture or dust on the modules surface can enlarge the dimension of one of the electrodes of the stray capacitance, thus increasing its value.

Hence, a photovoltaic plant can be seen as an array of stray capacitances, connected in series or parallel according to the structure of the PV field. Nevertheless, the phenomenon can be effectively described adding to the schematic of the grid-connected inverter two concentrated capacitors, between the ground reference and both positive and negative poles of the PV source, as depicted in Fig. 1.8.

The value of the considered stray capacitor can vary from 10-100nF for kW installed for mono and polycristalline panels [15].

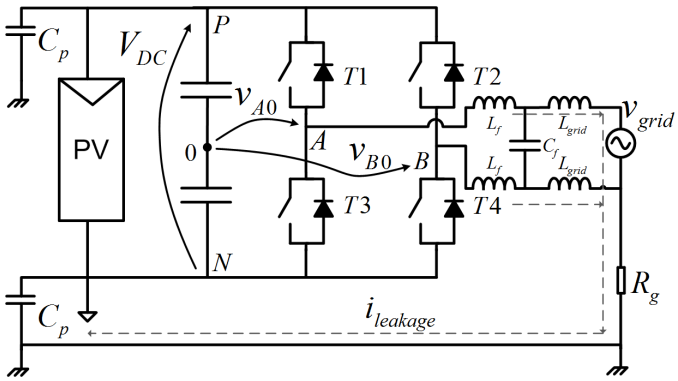


Fig. 1.8: Grid-Connected Transformerless Inverter with stray capacitance C_p.

If the voltage across the capacitors varies, according to (1.16), a ground leakage current can flow through the path (highlighted in Fig. 1.8) constituted by the output filter of the inverter, the grounding impedance of the MV/LV transformer and the capacitors themselves.

$$i_{leakage} = C_p \frac{dv}{dt} \tag{1.16}$$

As the impedance of the capacitor decreases at high frequency, high frequency changes of the voltage across C_p can generate higher current value than low frequency ones. Ideally, keeping the voltage across the capacitor constant results in no leakage current.

Conventional inverters normally do not achieve this goal. Considering the schematic of Fig. 1.8, it is possible to describe the circuit in terms of equivalent differential- (v_d) and common-mode (v_{cm}) components [16].

Taking as reference the mid-point of the DC-Link (marked as 0 in Fig. 1.8), the voltages at the output of the inverter v_{A0} and v_{B0} can be modeled as two pulse width voltage sources. Introducing v_d and v_{cm} as:

$$v_{cm} = \frac{v_{A0} + v_{B0}}{2}, v_d = v_{A0} - v_{B0} \tag{1.17}$$

and considering also the common and differential components of the grid voltage, the resulting equivalent circuit is reported in Fig. 1.9.

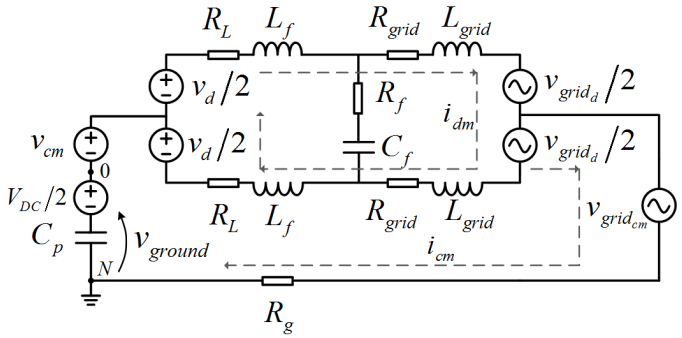


Fig. 1.9: Equivalent Common and Differential Mode circuit for a Grid-Connected Transformerless Inverter.

It is worth to be noted that the differential components do not influence the leakage current, circulating only in the differential path, as reported in Fig. 1.9. On the contrary, the common mode components affect directly the ground leakage current, which is therefore named also common mode current. Analyzing the equivalent circuit only for the common mode components in Fig. 1.9, the voltage across the capacitor C_p can be expressed as in [16]

$$v_{ground} = -v_{cm} - \frac{v_d(L_{f_2} - L_{f_1})}{2(L_{f_2} + L_{f_1})} + v_{grid_{cm}} - \frac{V_{DC}}{2} \tag{1.18}$$

where the first component of (1.18) represents the common mode voltage at the output of the converter. The second is due to mismatching between the value of the inductors of the inveter output filter, and the third, is the common mode component of the grid voltage. The last term of (1.18) is because the reference point 0 in Fig. 1.8 is at $V_{DC}/2$ respect to the negative rail of the DC link. In the case the positive pole of the DC link was considered instead, this component must appear with a positive sign. As V_{DC} is constant it should not contribute to the common mode current. Nevertheless, when the inverter is working, the DC-link is affected by a voltage ripple at twice the frequency of the mains. The amplitude of the ripple depends on the design of the DC-Link capacitor, which is usually dimensioned in order to achieve a low value of it.

Therefore for a more precise definition the expression of v_{ground} should be integrated as in (1.19), where also the component due to the voltage ripple is introduced. For the positive rail of the DC-link the same conclusions are valid, but with a positive offset of $V_{DC}/2$.

$$v_{ground} = -v_{cm} - \frac{v_d(L_{f_2} - L_{f_1})}{2(L_{f_2} + L_{f_1})} + v_{grid_{cm}} - \frac{V_{DC}}{2} - \frac{v_{DC_{ripple}}}{2} \tag{1.19}$$

It is worth to be noted that the second component is usually kept low in case of good converter design, whereas $v_{grid_{cm}}$ results in a sinusoidal common mode current, but with low amplitude due to the fact that $v_{grid_{cm}}$ has half amplitude of the grid voltage, and same frequency.

The most influential component is v_{cm}, since, according to the modulation strategy adopted for the converter, it can have the same amplitude of the DC link voltage and varies at high frequency, i.e. the switching frequency of the inverter, thus generating very high ground leakage current.

For instance, the full-bridge topology driven by a three-level (unipolar) PWM is the most popular solution for single-phase systems due to its simplicity and effectiveness. However, this topology cannot be used in PV transformerless systems because of large variations of the output common-mode voltage.

Fig. 1.10 shows the full-bridge driving signals of the unipolar modulation and the resulting v_{cm}, calculated considering as reference the negative pole of the DC-link. It

presents a peak-to-peak amplitude equal to the DC-Link voltage V_{DC} and a frequency equals to the switching one, and thus high ground leakage current.

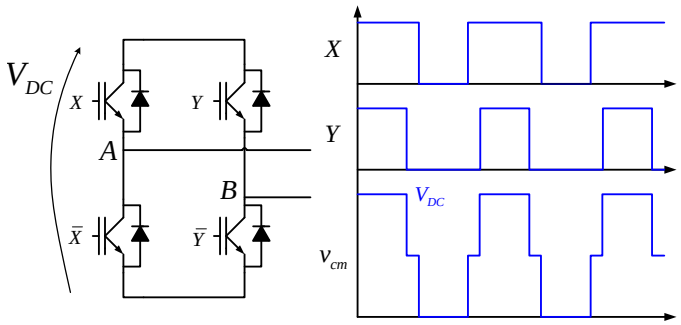


Fig. 1.10: Output common-mode voltage in case of full-bridge driven by unipolar modulation.

On the contrary, the h-bridge converter driven with bipolar PWM, where the two diagonals of the h-bridge commutate complementary, results intrinsically free from common-mode output voltage variations.

Through the support of Fig. 1.8 it is possible to compute the common-mode voltage applied during a switching cycle in case of bipolar PWM. The switching cycle consists of two possible configurations:

1) T1 and T4 On (T2, T3 Off): $v_d = V_{DC}$, $v_{cm} = 0$

2) T2 and T3 On (T1, T4 Off): $v_d = -V_{DC}$, $v_{cm} = 0$

If the turn on and turn off occur at the same time (ideal commutation), there would be no changes on the common-mode voltage and thus no additional ground leakage current would appear.

However, in real converters, a small common-mode high-frequency filter is necessary to avoid an increase of the ground leakage current due to switching mismatch at converter output terminals A and B [17]. Moreover, the bipolar modulation is characterized by a poor efficiency and high output current ripple and it is not widely adopted.

A simple method to mitigate the ground leakage current was proposed in [18], it relies on the use of a passive common mode filter where the common-mode filter

capacitors are connected to the mid-point of the DC source, as shown in Fig. 1.11.

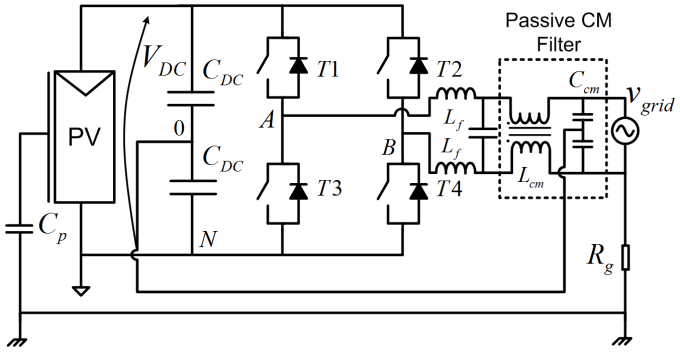


Fig. 1.11: Full-bridge inverter with passive common-mode filter for ground leakage currents.

The equivalent common mode circuit is also reported in Fig. 1.12.

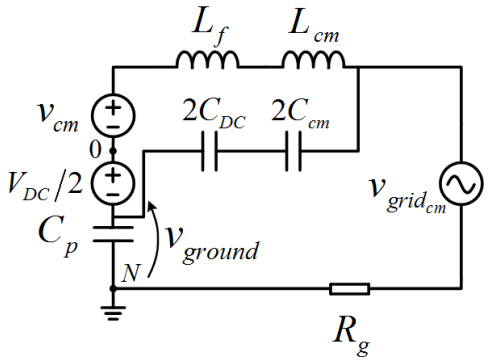


Fig. 1.12: Common-mode equivalent circuit of the Full-bridge inverter with passive common-mode filter

It shows that the split common-mode capacitors C_{cm} and the split dc-link capacitors C_{DC} are included in the circuit. It is also possible to note the presence of an LC low-pass passive filter introduced in the simplified CM circuit. It is constituted by the split dc-link capacitors C_{DC} in series with the split CM capacitors C_{cm} and the inductors L_f and L_{cm}.

Based on Fig. 1.12, the voltage across the stray capacitance can be determined. v_{ground} is obtained as:

$$v_{ground}(\omega) = -\frac{v_{cm} + 0.5V_{DC}}{1 - \omega^2(L_f + L_{cm})(2C_{DC}//2C_{cm})} + v_{grid_{cm}} \tag{1.20}$$

making explicit the resonant frequency of the LC components ω_r, and considering that ω_r is much higher than the frequency of the DC voltage ripple, the only significant component for the the ground voltage is v_{cm}, therefore the solution in (1.20) can be simplified as shown in (1.21).

$$v_{ground}(\omega) = -\frac{v_{cm}}{1 - (\omega/\omega_r)^2} \tag{1.21}$$

As can be seen contribution of the common mode voltage at the inverter output is attenuated by:

$$Atten_{v_{ground}}(w) = 20\log|1 - (\frac{w}{w_r})^2| \tag{1.22}$$

This solution can determine good results in terms of power converter cost and efficiency when the variation of v_{cm} (due to power converter switching) is limited.

Table 1.1: Summary Of The Grid Connection Standards

Issue	**IEEE 1547**		**CEI 0-21**		**VDE0126-1**	
Nominal Power	10kW		6kW		-	
Harmonic Content	order(h)	limit(%)	order(h)	limit(A)	order(h)	limit(A)
	3-9	4.0	3	2.3	3	3
	11-15	2.0	5	1.14	5	1.5
	17-21	1.5	7	0.77	7	1
	23-33	0.6	9	0.4	9	0.7
	even		11	0.33	11	0.5
	harmonics		13	0.21	13	0.4
	are limited		15-39	0.15	17	0.3
	to 25%			x15/h	19	0.25
	of the odd		2	1.08	23	0.2
	harmonic		4	0.43	25	0.15
	litit shown		6	0.3	25-39	3.75/h
	THD $<$ 5%		8-40	0.23	even	1.5/h
				x8/h	$>$40	4.5/h
DC Current Injection	less than 0.5% of rated output current		0.5% $I_n, t < 1s$ and $<$1A trip time 0.2s		$<$1A trip time 0.2s	
Voltage Deviation	range(%)	time(s)	range(%)	time(s)	range(%)	time(s)
	$V < 50$	0.16	$V < 80$	0.4	$V < 85$	0.2
	$50 < V < 88$	2	$V > 120$	0.2	$V > 110$	0.2
	$110 < V < 120$	1				
	$V > 120$	0.16				
Frequency Deviation	range(Hz)	time(s)	range(Hz)	times)	range(Hz)	time(s)
	$59.3 < f < 60.5$	0.16	$47 < f < 52$	0.1	$47.5 < f < 50.2$	0.2
Leakage Current					average current (mA)	time(s)
					30	0.3
					60	0.15
					100	0.04
					300 (peak)	0.3

Chapter 2

State of the art of transformerless PV Inverters

2.1 Introduction

During the last years, several classifications for transformerless inverters were proposed.

In [19] Blaabjerg and Garcia identified three category for step-up transformerless topologies:

- Two-stage topologies
- Pseudo-DC-Link Topologies
- Single-Stage Topologies

The first are those that employ a DC/DC stage for amplifying the voltage from the PV source, while performing the MPPT, and a DC/AC stage to inject current into the grid. Between the two stages a dc-link capacitor ensures the power decoupling from the DC source and the AC load. The dc-link capacitor is designed in order to reduce the amplitude of the voltage ripple at twice the grid frequency thus, electrolytic capacitors are usually employed, affecting the life span of the entire system.

The Pseudo-DC-Link Topologies consists of two power stages as well, but in this case the DC/DC converter generates a rectified sinusoidal current. This current is then unfolded in phase with the grid voltage by means of a line-switched bridge.

The last category includes the converter where the functionalities of stepping-up the voltage from the PV source, executing the MPPT algorithm, and controlling the quality of the injected grid current are performed by a single power stage. This solution permits to increase the overall efficiency and the reliability of the system, simplifying the converter structure and increasing power density as well.

In [20] Blaabjerg again, with Kjaer and Pedersen, classified the converters for PV applications in transformered or transformerless. Furthermore, a more accurate subdivision was developed on the base of the number of power stages, the position of the power decoupling capacitor, and the types of the grid interfaced converters.

In [17] the analysis is more focused on transformerless converters that do not need to step-up the voltage source, since they are connected to PV strings with a sufficient MPP voltage value to allow the inverter to erogate energy into the grid. Grid-connected transformerless topologies were divided into two groups: the half-bridge and the full-bridge families.

In half-bridge converters the neutral wire is connected to the mid-supply voltage point. They intrinsically reject the phenomenon of common-mode current described in section 1.4, since the voltage across the parasitic capacitance C_p is constant. However, these topologies need a double DC bus voltage if compared to a full-bridge one.

In Full-bridge converters avoiding the common-mode current phenomenon is not straightforward. Many solutions were proposed to ensure no common-mode current along with high efficiency levels. The purpose is achieved by means of additional

switches and custom PWM modulations in order to decouple the grid from the DC bus during the freewheeling phases of the output current. As noted in [21] when the PV source is disconnected from the load the potential of the load can be floating, for the so-called inverters with no-clamp methods, or can be set at the mid-point of the DC source for inverters equipped with clamp methods.

It was proved that the latter present better performances in terms of common-mode current rejection capability.

However, all these categorizations were developed focusing on the inverter point of view.

In the last years many different technologies for the photovoltaic panels were studied and marketed. They present different characteristics and require specific concerns for the connection.

In fact, from a practical point of view, the choice of the appropriate inverter for a PV plant is made by the designers in strict dependence on the PV technology installed. For these reasons in this work an alternative classification for grid-connected transformerless PV inverters is proposed, correlating the characteristic of the converters with the needs of the different PV technologies.

Since the two arguments are tied, an overview about the major issues of PV panels is needed.

2.2 Major issues for PV panel technologies

Monocrystalline and polycrystalline panels dominate the PV market for years now, nevertheless, new technologies such as thin film modules, amorphous panels, and tandem solar cells offer high performances and in some case reduced production cost. However, some technologies should be employed only in restricted circumstances and taking certain precautions. The major issues for PV panel technologies are:

- Ground leakage current
- Potential induced degradation
- Transparent Conductive Oxide (TCO) corrosion

2.2.1 Ground leakage current

As analyzed in detail in section 1.4 in transformerless grid-connected converters the absence of galvanic insulation between the PV source and the grid can result in ground leakage currents. These currents are actually common-mode currents circulating in the path that connects the PV cells to the ground through the parasitic capacitance of the panels C_p. If no precautions are taken the leakage currents can reach very high values. Ground leakage currents are particularly detrimental because, not only they can damage the PV panels, but being superimposed to an eventual fault current make difficult to detect the presence of ground faults. To limit ground leakage currents the voltage across the parasitic capacitance C_p must not present high frequency components.

2.2.2 Potential induced degradation (PID)

In several PV plants a degradation in the performances of the PV panels was noticed after a period of operation. Where panels were connected in strings, this phenomenon was particularly observed in the module nearest to the negative pole of the PV array. The degradation was discovered not to be related to the natural aging of the material but to the coulomb effect [22].

The potential of the PV modules' positive or negative poles are biased respect to the metal frame that is grounded for safety standards. The voltage can induce electrons to pass from the silicon active layer through the glass to the grounded module frame.

The phenomenon results in a decrease of the maximum available power from the module. However, competing processes make the effect non-linear and history-dependent [23].

The PID process was initially attributed only to certain types of solar cells. For instance, SunPower company indicates as a remedy for its products to ground the positive pole of the PV string. Nevertheless, cases where it is the negative pole to have to be grounded are registered as well.

2.2.3 TCO corrosion

The Transparent Conductive Oxide layer is an electrically conductive layer employed in thin film PV panels. It is housed on the inside surface of the cover glass. Many studies indicate that the TCO layer is subject to corrosion [24]. The corrosion is the result of the reaction with the sodium that is contained in the cover glass in presence of humidity.

Corrosion depends directly on leakage currents and from the potential of the PV array against ground. Therefore, the damages can be prevented by connecting to the ground the negative pole of the PV array.

2.3 Transformerless Grid-Connected topologies

As seen different PV panel technologies suffer from different types of issues, but in the majority of cases all the problems can be attributed to the presence of a potential difference between the PV cells and the ground.

To limit degradation of PV panels the potential of the positive and negative poles of the PV array against the ground must be controlled.

For these considerations, an alternative classification for Transformerless grid-connected inverters can be developed, taking in consideration the voltages, which can be observed during the inverter operation, between the two poles of the PV source and the ground.

Therefore, it is possible to subdivide single-stage grid-connected transformerless inverters in:

- Full-bridge based topologies
- Half-bridge based topologies
- Doubly grounded topologies

The voltage waveforms between the positive (v_p) and negative (v_n) poles of the PV source and the ground are reported in Fig. 2.1 for each of them. The full-bridge based topologies present sinusoidal waveforms that are symmetrical respect to the

ground potential. The oscillation at the grid frequency is due to the common-mode component of the grid voltage that is intrinsically presents in v_p and v_n for this family of inverters.

In half-bridge based inverters the sinusoidal component in v_p and v_n is totally eliminated, since the neutral wire of the grid, which is grounded in correspondence of the MV/LV transformer of the mains, is directly connected to the mid-point of the DC voltage source. Nevertheless, a symmetrical DC bias equal to half of the DC voltage is still present.

The doubly grounded topologies are those where the negative pole of the PV source is directly connected to the ground. Their name derives from the fact that in transformerless applications also the output of the inverter is grounded, since the neutral wire of the grid is connected to earth at the mains transformer. Therefore, both input and output of the converter are clamped to the ground potential and special architectures are required to prevent short-circuit during the inverter operation.

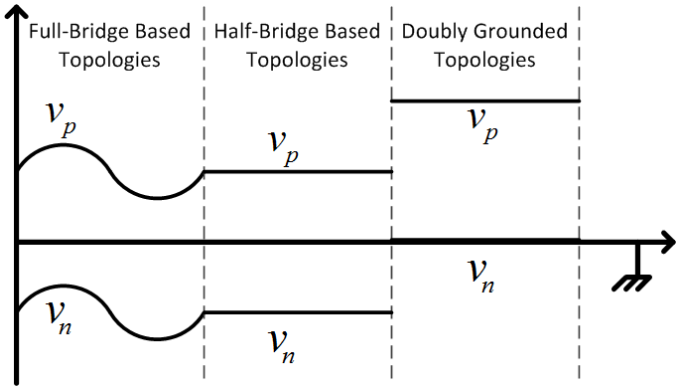


Fig. 2.1: Voltages respect to the ground of the positive and negative poles of the PV source during converter operation for different families of grid-connecetd transformerless inverters.

2.3.1 Full-Bridge Based Topologies

According to what explained in section 1.4 the v_p and v_n voltages for full-bridge based topologies can be expressed with the formula:

$$\begin{aligned} v_n &= -v_{cm} - \frac{v_d(L_{f_2}-L_{f_1})}{2(L_{f_2}+L_{f_1})} + v_{grid_{cm}} - \frac{V_{DC}}{2} \\ v_p &= -v_{cm} - \frac{v_d(L_{f_2}-L_{f_1})}{2(L_{f_2}+L_{f_1})} + v_{grid_{cm}} + \frac{V_{DC}}{2} \end{aligned} \tag{2.1}$$

It is highlighted the presence of a sinusoidal component, which is in fact the common-mode component of the grid voltage, with amplitude equal to half of the grid voltage amplitude. The v_{cm} term represents the common-mode output voltage generated by the converter during the operation. Ideally, if v_{cm} is constant no common-mode currents due to the contribution of the converter operation arise. The only component of the ground leakage current would be at the grid frequency, but with a reduced amplitude thanks to the high impedance of the parasitic capacitance at low frequency.

$$I = \omega C_p \frac{V_{grid}}{2} \tag{2.2}$$

Many inverters able to keep the common-mode voltage at a constant value during the inverter operation were presented both in industry and in academia. They usually disconnect the AC load from the PV source during the free-wheeling phases of the output current, by means of additional power switches.

In Fig. 2.2 two additional blocks used alternatively are presented: the former is inserted in the DC converter side and the latter in the AC converter side, both reducing the ground leakage current [25] [26].

The use of DC or AC decoupling allows the disconnection of the grid voltage from the photovoltaic plant during the grid current free-wheeling phases. The AC decoupling block is employed in the Sunways inverter named Highly Efficient Reliable Inverter Concept (HERIC), whereas the DC decoupling is used in SMA H5 converter. For both cases, the output voltage is a three level one, with ripple at the switching frequency of the converter. Therefore, in the output filter design a current ripple at the same frequency has to be taken into account.

In [27] it was proposed a solution that embeds 6 power switches and 2 diodes. The inverter is named H6 and, as can be seen in Fig. 2.3, in addition to the h-bridge

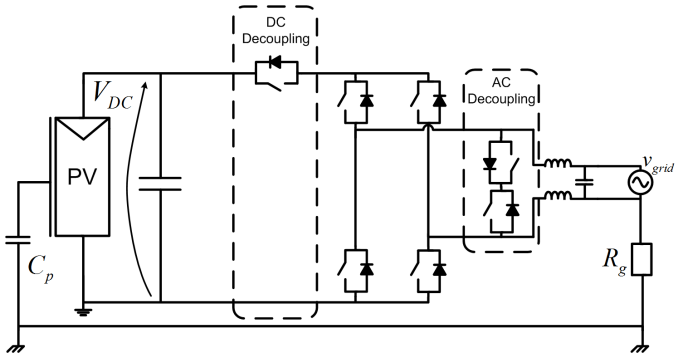


Fig. 2.2: Full-bridge with AC decoupling (HERIC) and DC decoupling (H5) blocks.

structure two switches are inserted in the DC rails, while two diodes are connected between the DC rails and the mid-point of the source voltage.

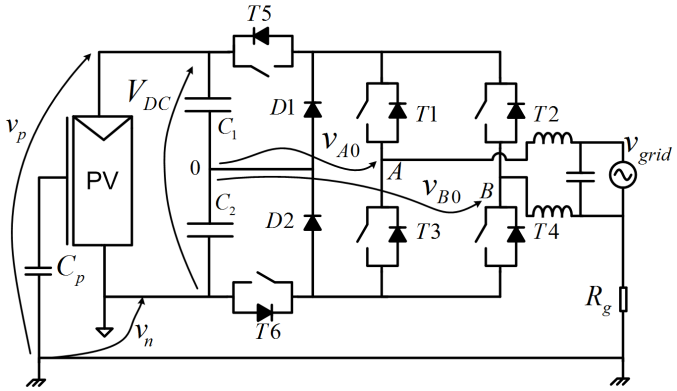


Fig. 2.3: Topology proposed in [27] and [28].

This topology is driven by a particular modulation strategy. A diagonal of the full-bridge is kept on during a whole grid voltage half-wave (for instance T1 and T4 when the grid voltage has positive sign), whereas the DC decoupling transistor, T5 and T6, commutate simultaneously at the switching frequency. During the output current free-wheeling phase, when T5 and T6 are off, all the four full-bridge switches are on; the grid current will then split across the two paths constituted by the transistor T1 and

the free-wheeling diode of T3, and the transistor T4 and the free-wheeling diode of T2. The additional diodes D1 and D2 will fix the common mode voltage to $V_{DC}/2$.

In [28] the same architecture was driven by a different modulation strategy. In this case the 4 switches of the h-bridge are driven as in the case of unipolar PWM modulation, whereas the two DC devices T5 and T6 does not commutate simultaneously, but switch off alternatively when the current free-wheels respectively in the upper or lower part of the h-bridge. The additional diodes do not conduct current but clamp the load potential at $V_{DC}/2$ during the free-wheeling phases.

Differently from [27] in [28] the ripple of the output current is at twice the switching frequency. Therefore, for a given switching frequency of the converter, the size of the filter inductor can be divided by two.

An effective solution presenting the same number of switches and diodes was proposed in [29]. Fig. 2.4 illustrates the scheme for this inverter. The top device in one leg and the bottom device in the other leg are switched simultaneously in the PWM cycle and the middle device operates as a polarity selection switch in the grid cycle. During the grid positive half cycle, for example, switch T4 remains on, whereas T3 is off. If T1, T6, T4 are on, the converter is feeding positive voltage to the load, when T1 and T6 turn off the current free-wheels through the diode D1. Again, the current ripple is at the switching frequency of the converter.

Furthermore, like many other topologies in literature, the solution in [29] was thought for employing MOSFET devices, in order to achieve very high efficiency values. The modulation strategy was studied in order to avoid the conduction of the MOSFET antiparallel body diode, in fact, the free-wheeling phase is realized through the conduction of unidirectional devices, i.e. diodes D1, D2. Thus, the converter can operate only with unity power factor and the capacity to manage reactive power is not addressed.

2.3.2 Half-Bridge Based Topologies

In these topologies, the neutral wire of the grid is directly connected to the mid-point of the DC source, whereas the phase wire is connected through the output filter to the PWM output of the converter. In this way the voltage across the parasitic capacitance

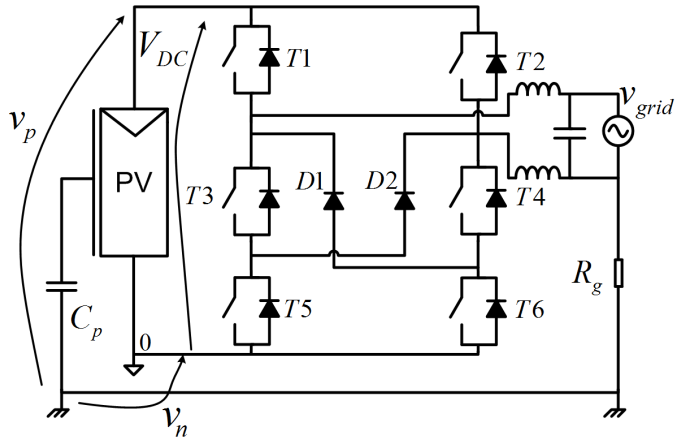


Fig. 2.4: H6-type topology proposed in [29].

is clamped to a constant value, and, as can be observed in (2.3), only the voltage ripple on the DC source affects the leakage currents, although its contribution is negligible.

$$\begin{aligned} v_n &= -\frac{V_{DC}}{2} - \frac{v_{DCripple}}{2} \\ v_p &= \frac{V_{DC}}{2} + \frac{v_{DCripple}}{2} \end{aligned} \tag{2.3}$$

The best known converter in this family is the Neutral Point Clamped (NPC) inverter. It was first proposed in [30] for a three-phase application and subsequently employed also for single-phase solutions [31].

The topology is shown in Fig. 2.5. The DC Link is formed by two series capacitors that share equal voltage, with $V_{DC} = V_{C1} + V_{C2}$. The neutral wire of the grid is connected to the mid-point of the DC voltage source. The NPC embeds four switches (T1-T4) and two clamping diodes (D1 and D2).

During the positive half-wave, T2 is kept on while T1 is switching at the switching frequency, whereas for the negative half-wave, T3 is kept on while T4 is switching at the switching frequency. During the free-wheeling phases the output current circulates through the ON-state IGBT and the diode D1 or D2 depending on the sign of the grid voltage. The three-level output voltage presents a ripple at the same frequency of the PMW carrier.

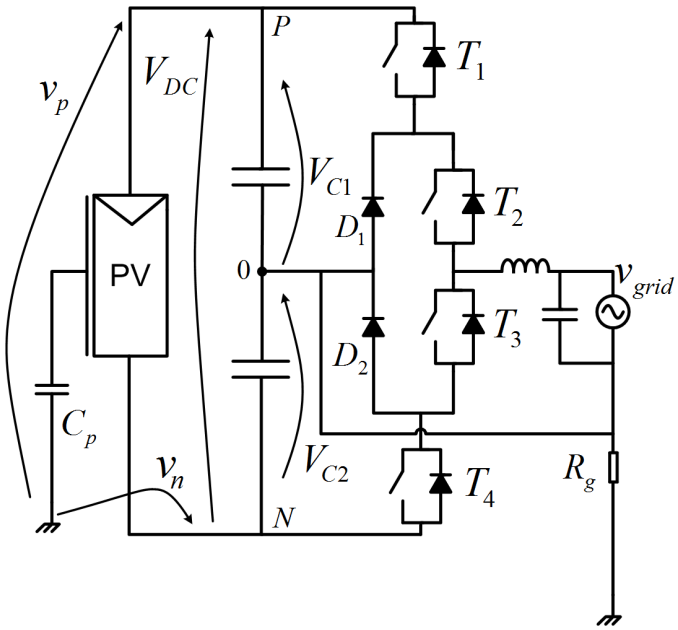


Fig. 2.5: NPC topology.

Also in this case the inverter can deliver only power with unity power factor, for overcoming this drawback an alternative solution, employing 2 IGBTs instead of diodes D1 D2, was proposed as well [32].

Another interesting solution was presented by SMA. It employs 4 SiC MOSFETs as shown in Fig. 2.6.

During the positive half-wave of the grid voltage T1 and T3 commutate at the switching frequency whereas T2 is kept on. On the contrary, during the negative half-wave T2 and T4 switch at high frequency while T3 is kept on. This solution provides very high efficiency since during the active stage, when the inverter output voltage is positive or negative, only one device is conducting, whereas when the output voltage is zero, the current is flowing through two devices. The only disadvantage respect to [31] is that in this case the voltage the devices have to withstand when they are off is equal to the DC voltage source, whereas in [31] it was just $V_{DC}/2$. Therefore, devices with a much higher breakdown voltage have to be used.

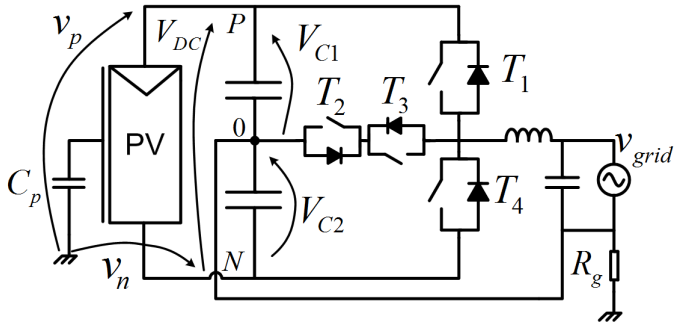


Fig. 2.6: Half-Bridge topology proposed by SMA.

2.3.3 Doubly Grounded Topologies

In doubly grounded inverters the negative pole of the PV source is grounded. The voltage v_n is zero, whereas v_p is equal to the DC source voltage (2.4).

$$\begin{aligned} v_n &= 0 \\ v_p &= V_{DC} + v_{DCripple} \end{aligned} \tag{2.4}$$

Since also the output of the converter is grounded through the neutral wire of the grid, particular inverter configurations have to be considered for avoiding short-circuit conditions.

The topology proposed in [13] is presented in Fig. 2.7. During the positive half-wave, T1 and T3 are on, while T4 and T5 commutate complementary at PWM frequency to synthesize the correct output voltage. The flying capacitor is connected in parallel with the DC Link, so it is charged at the full DC source voltage. During the negative half wave, T5 is kept on, while T1 and T3 switch synchronously and T2 in complement to them in order to generate the negative output voltage.

In particular, when T1 and T3 are on the zero output voltage is provided and the flying capacitor is charged. When T2 switches on, T1 and T3 turn off, and the output voltage is equal to the opposite of the DC voltage.

However the stresses on the devices are not balanced, in fact through T3 flows not only the output current but also the charging current of the flying capacitor. Since

the size of the capacitor is large in order to effectively decouple the AC load power from the DC source, the charging current of the flying capacitor could present high surge, consequently increasing the power losses on the devices.

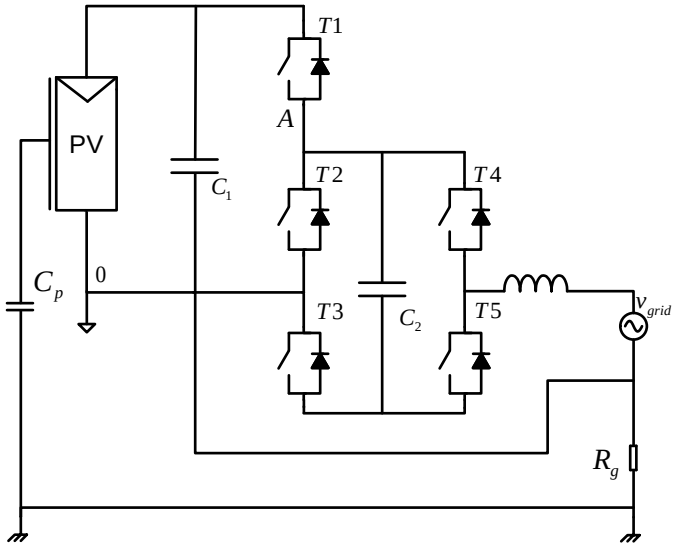


Fig. 2.7: Topology proposed in [13].

An alternative solution was proposed in [33] and depicted in Fig 2.8(a). It belongs to the category of so-called Flying inductor converter. The basic inverter topology is composed of a buck-boost converter that can be shifted according to the positive and negative output of the grid.

During the positive half-wave of the grid voltage T4 T5 are on, T3 is off while T1 T2 switch simultaneously at high frequency. When T1 T2 are on the inductor L is charged, otherwise when T1 T2 turn off the energy stored in the inductor is released to the grid. During the negative half-wave the behavior is similar; T2 T3 are on, T4 and T5 are off, whereas T1 switches at high frequency.

The drawback of such solution is the discontinuous waveform of the output current that requires large filter capacitors. To address this problem, a new circuit, as illustrated in Fig. 2.8(b), was introduced in [34], though the increased amount of switches negatively affects the efficiency and robustness of the total system.

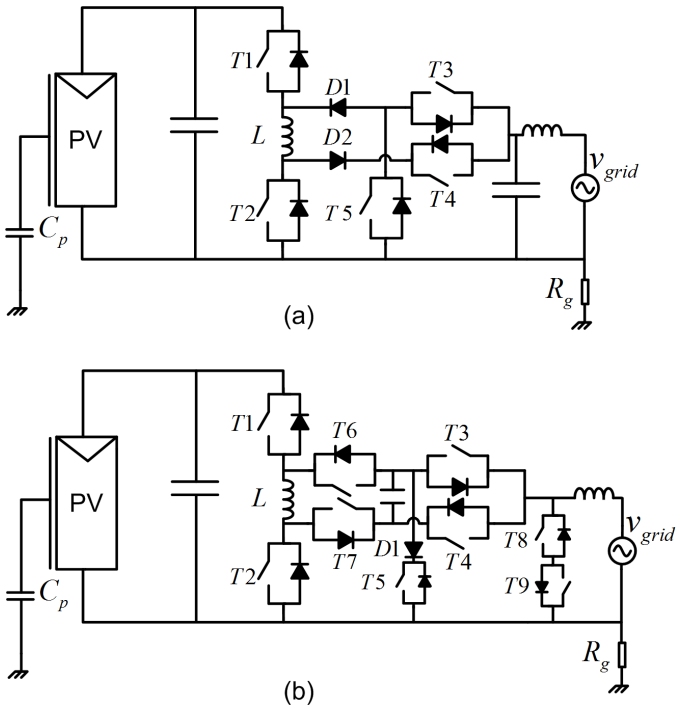


Fig. 2.8: Topology proposed in [33](a) and [34](b).

In [35] a topology derived from the basic Zeta configurations was proposed (Fig. 2.9). During positive half-waves, it transfers the power to the grid on the principle of a buck-boost converter, while during negative half-waves, it uses the boost principle to transfer the power to the grid.

This asymmetrical operation not only makes the control scheme complex, but may also result in asymmetrical current and may inject DC component into the grid.

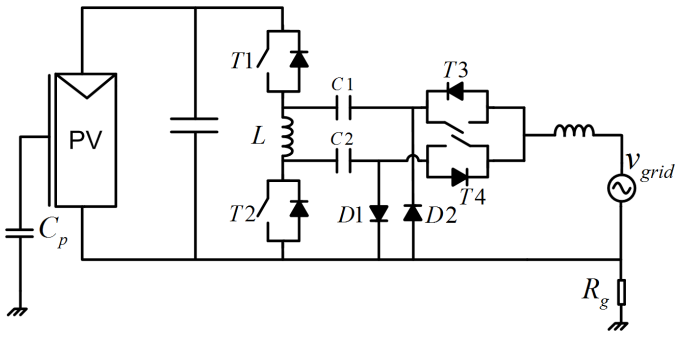


Fig. 2.9: Topology proposed in [35].

Chapter 3

Active Common-Mode Filter

3.1 Introduction

In chapter 2 it was shown as various topologies were proposed in order to avoid the presence of ground leakage currents in transformerless grid-connected converters.

Among all them the most promising and efficient are those belonging to the full-bridge based family (section 2.3). They employ additional power switches with respect to the classic full-bridge structure ensuring, ideally, a constant common-mode voltage at the output of the converter.

This work presents a different principle to solve the problem of the ground leakage currents. Instead of adding devices that complicate the structure of the converter and thus the control strategy, it is possible to employ a simple three-level full-bridge inverter, followed by an additional device able to cancel the v_{cm} variations at the output of the converter.

One of the main advantages of employing the standard three-level full-bridge in grid-connected operation together with the proposed solution is the possibility to operate with any power factor. This characteristic is very important, since new international regulations governing the connection of power converters to the grid require some extent of reactive power handling capability.

Active filters for common-mode voltage have already been studied in literature, although their use in transformerless grid-connected converters has not been yet investigated. In [36, 37, 38] the authors employed linear amplifiers controlled by feedback systems to reduce the electromagnetic interference (EMI) generated by the power converters. Conversely, as the common-mode voltage at the inverter output depends on the PWM strategy, if this is known in advance, a low-power switching converter can be employed to compensate for it without a feedback system. This feed-forward compensation was used in [39, 40] to compensate the common-mode voltage variation of a three-phase voltage-source inverter which supplied an induction motor.

In this work a new feed-forward common-mode voltage compensation system was applied to single-phase grid-connected converters for PV systems.

3.2 Active Common-Mode Filter Concept

As shown in section 1.4, in transformerless full-bridge based converters the ground leakage current is caused by two sources of common-mode voltage variation: the first, and more troublesome, can be introduced by the high-frequency switching of the power converter, while the second is due to the grid generator and it is intrinsically present in this type of topologies. In fact, the common-mode voltage of the grid determines a line frequency sinusoidal voltage, with half the amplitude of the grid voltage, across the parasitic capacitance of the PV string. However, given the low frequency of the grid, the resulting small ground leakage current is acceptable with monocrystalline or polycrystalline PV panels.

On the contrary, the common-mode voltage variation due to the switching of the converter has high frequency spectral content and can generate very high values of

ground leakage current.

The full-bridge topology driven by a three-level (unipolar) PWM is the most popular solution for single-phase power converters due to its simplicity and effectiveness, but it cannot be used in transformerless PV systems because its v_{cm} presents a peak-to-peak amplitude equal to the DC Link voltage V_{DC} at switching frequency (see Fig. 1.10). If a device able to cancel the common-mode voltage variations at the converter output is cascaded to the three-level converter, its application to PV transformerless systems becomes feasible. Obviously, this additional device should be characterized by low power losses, simplicity and low cost.

In fact, every transformerless inverter embeds a common-mode inductor at the output of power converters in order to comply with electromagnetic compatibility (EMC) standards.

By adding another winding to the common-mode choke (Fig. 3.1), it is possible to consider this new magnetic component as a common-mode transformer. If a specific voltage is supplied to its primary winding through an additional low power full-bridge, the secondary voltages (v_s) of the transformer can be used to compensate for the variation of v_{cm}. In this way the total common-mode voltage at the converter output, v_{cmT}, can be effectively kept constant.

The application of the active common-mode filter (composed of the additional low power full-bridge and the common-mode transformer) to a three-level PWM full-bridge is shown in Fig. 3.2. The total common-mode voltage can be expressed as (3.1).

$$v_{cmT} = \frac{v_{A^10} + v_{B^10}}{2} = v_{cm} - v_s \tag{3.1}$$

The common-mode voltage v_{cm} generated by a full-bridge driven by unipolar PWM is shown in Fig. 3.3. The gate signals x and y are also reported. The same figure shows the secondary voltages of the commmon-mode transformer v_s which are used to compensate for v_{cm}. Therefore, v_s must have a shape equal to v_{cm}, but without the DC voltage component. In this way $v_{cmT} = v_{cm} - v_s$ results constant, as shown in Fig. 3.3.

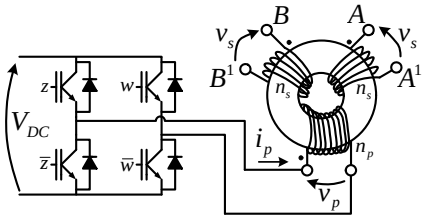


Fig. 3.1: Active common-mode filter topology.

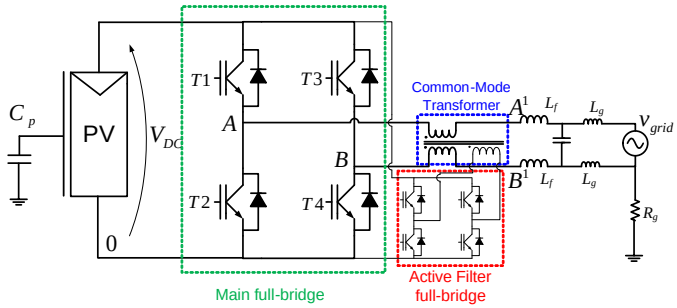


Fig. 3.2: Topology of the proposed solution.

In order to synthesize the desired waveform for v_s, a specific voltage v_p must be fed to the primary winding of the common-mode transformer. Since the additional low-power full-bridge is supplied with the same DC Link voltage of the main full-bridge, fixing the turn ratio at $n_p/n_s = 2$ the PWM driving signals (z and w) can be simply obtained from the PWM signals of the main full-bridge as $z = x$ and $w = \overline{y}$.

It is important to put in evidence that the power losses of the active common-mode filter are very low since the primary current i_p of the common-mode transformer is practically equal to its magnetizing current only. Quantitative considerations will be presented in the following sections.

It is important to note that the proposed active common-mode filter can be adopted also in other power converter topologies, but it results effective in term of cost and size only if the needed compensation voltage v_s (and therefore also v_p) presents a null mean value for each PWM period. In fact, only in this case it is possible to use a small magnetic core for the common-mode transformer, on the contrary the area

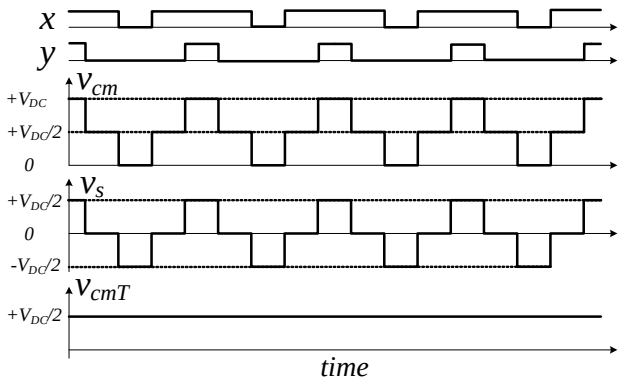


Fig. 3.3: Compensation of v_{cm} variations, operated by the active common-mode filter.

of the magnetic core and/or the turns number must be very large in order to avoid magnetic saturation [41].

3.2.1 Dead Time Compensation Strategy

A possible choice for the driving signals of the active filter full-bridge was proposed in previous section ($z = x$ and $w = \overline{y}$). Nevertheless, this solution works correctly only in the ideal case, where power switches commutate instantaneously. Further considerations are needed in order to properly control the active filter in a real system. As widely known, the transitions between on/off states of a power switch is not instantaneous and, when a commutation occurs, a dead time is inserted in the complementary driving signals controlling each leg of the full-bridge. During this dead time interval the output voltage of the inverter is not actually controlled, and its value depends on the characteristics of the circuit and on the sign of the output current.

For example, Fig. 3.4 reports the typical actual driving signals x, y (with the insertion of the dead time intervals), during a PWM period under conditions of positive half-wave of the grid voltage, and positive value of the injected grid current. All the driving signals are plotted as solid lines together with their complementaries (dotted lines). The following considerations can be extended also to different conditions of grid voltage and current direction.

At first the effect of the dead time is taken into account for the determination of the v_{cm} waveform.

During the time interval t_1 $\overline{x}$ and $\overline{y}$ are high, the current free-wheels in the lower part of the main full-bridge through $T4$ and the anti-parallel diode of $T2$ in Fig. 3.2, and v_{cm} is equal to 0.

When a transition occurs at the end of t_1 a dead time is added and both $\overline{x}$ and x are forced to a low value (interval t_2). Since the anti-parallel diode of $T2$ is still on, the output voltage of the converter does not change till x goes high at the beginning of interval t_3. At this stage $T1$ is switched on and v_{cm} rises to $V_{DC}/2$ (interval t_3). Similarly, when $\overline{y}$ commutates at the end of t_3 a dead time interval is added as well, and y, $\overline{y}$ are driven low (interval t_4). In this case, the inverter output current imposes a switch-on of the anti-parallel diode of $T3$ and v_{cm} quickly reaches V_{DC}.

During t_5 the device $T3$ is on and v_{cm} remains at V_{DC}. At the end of t_5 another transition occurs: y returns to a low value whereas $\overline{y}$ is maintained low for the dead time interval t_6. Since the current is still flowing trough the anti-parallel diode of $T3$, the output common-mode voltage remains at V_{DC}. Only when $\overline{y}$ goes high at the end of t_6, v_{cm} falls to $V_{DC}/2$. Eventually, the common-mode voltage returns to 0 when, at the end of the PWM period, even the x signal switches back to a low value.

Similar behaviors can be deduced for the transitions of the driving signals during the negative half-wave of the grid current.

Since v_s must replicate the waveform of the common-mode voltage, also the behavior of the active filter full-bridge during the dead time intervals has to be taken in to account. In order to investigate that, Fig. 3.4 shows also the waveform of the primary current of common-mode transformer, i_p, which depends on the voltage waveform applied to the transformer primary and on the transformer magnetizing inductance L_m. The sign of i_p determines the output voltage value of the active filter full-bridge during dead time intervals, resulting in a slight difference between v_s and v_{cm} waveforms.

The driving signals of the active filter full-bridge, defined as $z = x$, $w = \overline{y}$, are reported in Fig. 3.4 during a PWM period. When $\overline{z}$ and w are both high (interval t_1) v_s is equal to $-V_{DC}/2$. At the beginning of the time interval t_2 the current of the

active filter full-bridge has a negative value, and therefore, as soon as $\overline{z}$ goes low, the anti-parallel diode of the switch driven by signal z turns on, and v_s raises quickly to 0.

As a matter of fact the rising edge of v_s leads v_{cm} by a time interval equal to the dead time. Otherwise, as can be seen in Fig. 3.4, the dead time interval t_4 is not critical because, when the transition of w occurs, the output current of the active filter full-bridge turns on the anti-parallel diode of the low side device controlled by the signal $\overline{w}$, and v_s is forced to follow the v_{cm} shape. Generally, it can observed that the power switches of the active filter full-bridge are turned on under zero voltage switch condition (ZVS), their anti-parallel diode is always on before their turning on. This behavior contributes to reducing the switching losses, but it also introduces time differences between v_s and v_{cm} (intervals t_2 and t_6 in Fig. 3.4, during the positive half-wave of the injected grid current) that must be compensated.

In particular, during the positive half-wave of the injected grid current, the rising edges of w and z should lag respectively the rising edges of $\overline{y}$ and x by a time equal to the dead time width t_d, as depicted in Fig. 3.5. Likewise, during the negative half-wave of the grid current, the falling edges of w and z should lag the falling edges of $\overline{y}$ and x by the same amount. Employing this control strategy the differences between v_s and v_{cm}, due to the dead time intervals, are strongly reduced.

It is worth to be noted that this compensation strategy does not require any additional sensors, since the only information required is the injected grid current, that is already acquired to implement the current control loop of the power converter.

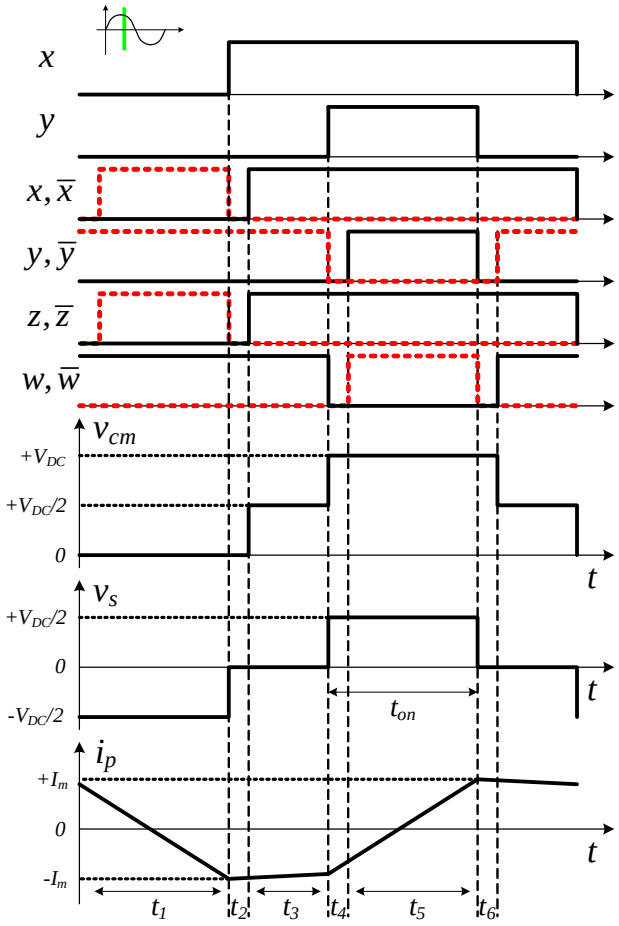


Fig. 3.4: Actual driving signals of the main full-bridge (x,y) and the active filter full-bridge (w,z), without the dead time compensation strategy.

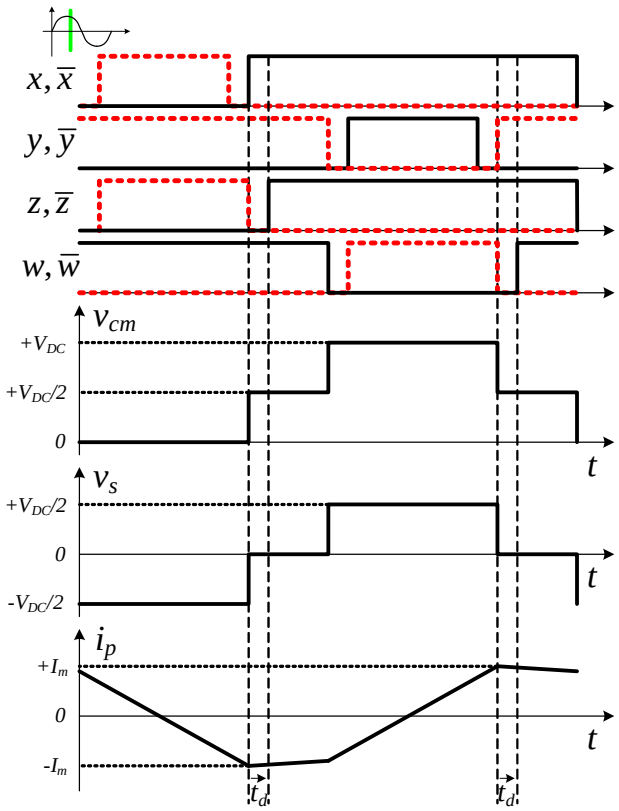


Fig. 3.5: Driving signals of the power converter (x,y) and the active filter full-bridge (w,z) when the dead time compensation strategy is applied.

3.3 Common-Mode Transformer Design

3.3.1 Design Considerations

The design of the common-mode transformer has the primary goal of avoiding the magnetic core saturation. The magnetic flux is generated by the supply of the primary winding and by the common-mode current at the converter output, which flows into the two secondary windings of the common-mode transformer.

Under the hypothesis of no magnetic saturation, the principle of superposition of effects can be used to compute the total magnetic flux.

The first component of the magnetic flux density, B_{VC}, is caused by the primary voltage of the common-mode transformer, whose amplitude changes during a grid voltage period. The worst-case scenario is when the supply of the primary winding is a square wave. This happens at the grid voltage zero crossings, when the the main full-bridge is always providing zero voltage (current freewheeling). Fig. 3.6 shows the primary voltage of the common-mode transformer during the positive semi-period of the grid voltage (a) and around zero-crossing grid voltage (b) with the waveform of B_{VC}.

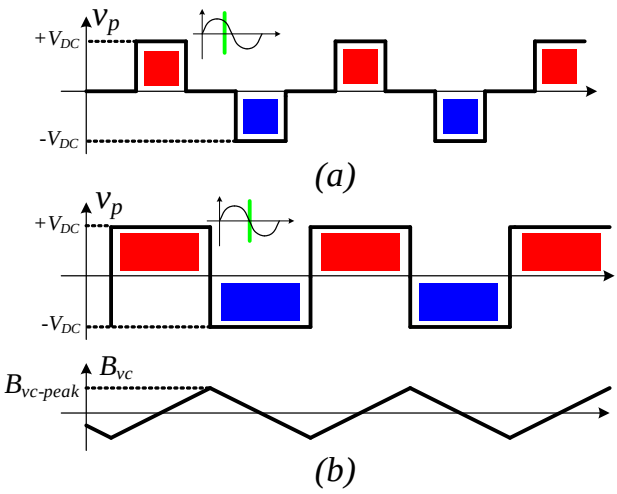


Fig. 3.6: Primary voltage of the common-mode transformer during the positive semi-period (a) and around zero-crossings (b) of the grid voltage with maximum variation of B_{VC} in the latter case.

Eq. (3.2) computes the peak value of B_{VC} which arises around grid voltage zero crossings (f_{sw} represents the switching frequency while S is the effective area of the magnetic core).

$$B_{VC-peak} = \frac{V_{DC}}{4 f_{sw} n_p S} \tag{3.2}$$

The second contribution of the magnetic flux density component, named B_{icm}, is due to the common-mode current at line frequency flowing in the PV system which is not attenuated by the proposed solution, as well as in all transformerless converter solutions based on full-bridge topologies. This component has a sinusoidal waveform with amplitude equal to: $I_{cm-peak} = \sqrt{2}\pi f_{grid} C_p V_{grid-rms}$.

Considering L_{cm} the inductance of each secondary winding of the common-mode transformer, (3.3) allows to calculate the peak value of this second flux density component. In first approximation, neglecting the magnetic saturation, L_{cm} can be computed as $n_s^2/\mathscr{R}_m$, where $\mathscr{R}_m$ indicates the reluctance of the magnetic core.

It is important to note that L_{cm} represents the common-mode inductance of the magnetic component when the primary winding is disconnected and not used. In this way the common-mode transformer becomes a simple common-mode inductor.

$$B_{Icm-peak} = \frac{L_{cm} I_{cm-peak}}{S n_s} \tag{3.3}$$

Since i_{cm} is in quadrature with the grid voltage, the maximum variation of B_{VC} happens when B_{icm} reaches $B_{Icm-peak}$, i.e. during the zero crossings of the grid voltage. Therefore the sum of $B_{Icm-peak}$ and $B_{VC-peak}$ has to be inferior to the maximum flux density, B_{max}, defined for the working conditions of the magnetic core (3.4).

$$B_{Icm-peak} + B_{VC-peak} < B_{max} \tag{3.4}$$

The ferrite material used for this application needs to have a high magnetic flux density and low power losses for frequencies up to 200 kHz. Materials of this kind present a relative magnetic permeability usually lower than 5000, determining for typical PV system parameters a $B_{Icm-peak}$ strongly lower than $B_{VC-peak}$.

3.3.2 Example of Common-mode Transformer Design

The design of the common-mode transformer was realized for a 2000 VA PV grid-connected converter, the grid voltage and frequency are respectively 230 V and 50

Hz. Considering for the secondary winding of the transformer a current density of approximately 4 A/mm^2 (in order to obtain low Joule effect power losses) the winding section area results equal to 2.17 mm^2. This represents the first design constraint.

The magnetic core was built starting from two low cost coated toroids placed side by side. A null air gap was chosen for the ferrite core in order to minimize the magnetizing current. The dimensions of each toroid are the following: outer diameter 51 mm, inner diameter 31.5 mm, effective area S=172 mm^2 and effective length l_e=125 mm. The chosen ferrite material was the low cost 3C90 produced by Ferroxcube, used for general purpose transformers at frequencies up to 200 kHz. The maximum magnetic flux density was fixed at $B_{max} = 0.35$ T in order to operate in absence of magnetic saturation for working temperatures up to 70 °C. The feasibility of this choice in terms of ferrite material and core section area was verified as reported in the following.

The design can be performed by choosing the switching frequency, f_{sw}, the DC-Link voltage V_{DC} and the value of the panels parasitic capacitance, e.g. C_p=600 nF. Given a grid voltage of 230 V rms, the ground leakage current due to the parasitic capacitance amounts to a peak value of I_{cm-max}=30 mA.

Starting from eq. (3.2), $B_{VC-peak} = 0.32$ T was chosen. With f_s=30 kHz and V_{DC}=400 V, the turns number n_p results 30, consequently $n_s = \frac{n_p}{2} = 15$. It was verified that these turns can be easily wound on the chosen core, obtaining a good fill factor.

The relative permeability of the core material can be considered to be $\mu_r = 2000$, consequently the inductance for the secondary windings results $L_{cm} = n_s^2/\mathscr{R}_m = 1.6$ mH. This determines a $B_{Icm-peak} = 0.0091$ T that allows to validate this design since the sum of $B_{VC-peak}$ and $B_{Icm-peak}$ is lower than the maximum working flux density B_{max}.

The primary inductance of the common-mode transformer is approximately $L_m =$ 6.3 mH. The amplitude of the primary current waveform changes during the grid-voltage period but in the worst case (during zero-crossings and with a triangular waveform) has an amplitude equal to 0.52 A. It is important to put in evidence that the primary current of the common-mode transformer is approximately equal to the transformer magnetizing current, therefore the Joule effect power losses are practically

referred only to the secondary windings of the common-mode transformer and result equal to 2.3 W for an injected grid current of 8.7*A*.

As for any electric machine design, the design procedure is iterative up to the achievement of a satisfactory result. A laboratory prototype was built according to the above design.

3.4 Comparison with the state of the art

In this section the proposed topology is compared to the state of the art of transformerless photovoltaic converters. The total number of power devices, the number of power devices in the current path, the commutation voltage and the ground leakage current performance are synthesized in Table 3.1. The full-bridge driven by unipolar PWM is added as a reference, with the remark of high ground leakage current, i.e. not applicable to transformerless applications.

The H5 and H6 transformeless topologies present a lower total number of switches than the proposed topology, but the number of devices in conduction is larger, unlike the HERIC topology which presents the same number of devices in conduction. In order to compare also the switching power losses, Table 3.1 shows the switching voltage across the switches for every topology. It is important to put in evidence that none of these topologies is able to manage reactive power keeping constant the common mode voltage at the output of the converter.

For completeness, Table 3.1 reports also a photovoltaic inverter with HF DC link [42]. This topology features a IGBT full-bridge preceded by a soft-switching DC/DC converter with high-frequency transformer (this topology is able to manage reactive power if the unipolar PWM is used for the DC-AC full-bridge). Each side of the transformer is driven by a full-bridge composed of MOSFETs with very low on-state resistance. As a matter of fact, two half-bridges with capacitor divider could be used instead of the two full-bridges, lowering the power switches count to eight. Although in this case the total component count would be equal to the proposed topology, it must be noted that the devices driving the common-mode transformer are very low-power, small-footprint ones. Solution [42] has the fundamental advantage of ensuring

zero ground leakage current without a bulky line frequency transformer and is suitable for every kind of panel technology. Moreover, the DC/DC converter allows a voltage boost at the secondary. However, the multiple conversion stages and the wide input voltage excursion typical of a photovoltaic field, limit the maximum achievable efficiency with respect to transformerless topologies. In fact, the zero voltage switching and/or zero current switching may not be obtainable for wide ranges of input voltage and power. For this reason, if polycrystalline or monocrystalline silicon panels are employed, transformerless converters are preferable.

The transformerless topologies typically employ boost converters between the PV string and the DC/AC grid-connected converters. In Table 3.1 the additional devices for the DC-DC converters are not considered, except for the HF DC Link topology.

Table 3.1: State of the Art Comparison

Architecture	**Devices Number**	**Devices conducting**	**Switching Voltage**	**Common-mode current**
Full-Bridge Unipolar PWM	4	2	V_{DC}	High
HERIC	6	2	$V_{DC}/2$	Low
H5	5	3	$V_{DC}/2$	Low
H6	6	4	$V_{DC}/2$	Low
Proposed topology	4 Rated Power + 4 Low Power	2	V_{DC}	Low
HF DC Link topology [42]	12(8)	6	V_{DC}	Absent

3.5 Control of a grid-connected Photovoltaic Inverter

As explained in the previous sections of this chapter, the active common-mode filter is cascaded to a three-level full-bridge inverter. It was clarified how the control signals of the h-bridge, that drives the primary of the common-mode transformer, were obtained from the driving signals of the power converter, but the control strategy of the power converter was not yet analyzed.

In grid-connected converters, in order to effectively harvest the energy from the PV field and transfer it to the grid, a specific control system must be implemented. The comprehensive control system is reported in Fig. 3.7.

The control features that the inverter has to realize are basically three, which can be divided in relative control subsystems:

- MPPT algorithm for harvesting the maximum available power from the PV string;
- Grid Synchronization for locking the phase of the grid voltage;
- Current Control for controlling the quality of the current injected into the grid.

Each control subsystem will be further analyzed in the following subsections.

Moreover, it is important to further highlight that these control strategies are just related to the power converter, since the active filter depends only on the driving signals of the power converter and, as long as they are noted, the choice of the adopted current controller or the MPPT method does not affect the active filter control.

3.5.1 Grid Synchronization

Grid synchronization is an important task in grid-connected converter since, as explained in section 1.2, the international regulations impose limits to the frequency and amplitude variations of the grid voltage. Therefore, the mechanism of synchronization with the grid must be very accurate. Different solutions were analyzed in literature, they include from the simple strategy of measuring the time between consecutive zero-crossings of the grid voltage, to more complex solutions such as SOGI

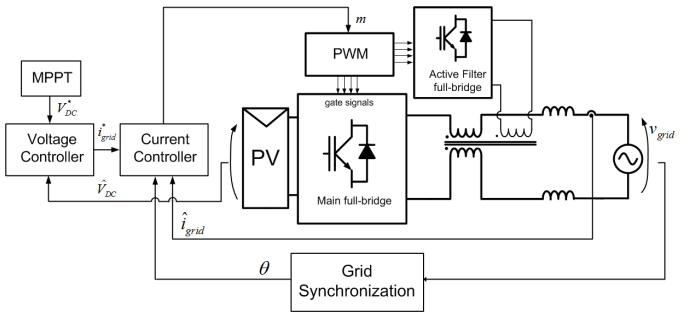


Fig. 3.7: Block scheme of the control of a single-stage PV inverter.

filter and different types of digital PLL. An accurate description of different grid synchronization strategy is realized in [43]. In this work a transport delay PLL was employed to get information about the grid voltage frequency. In a three-phase system, the use of the Clarke transformation allows to create a quadrature system and realize the PLL in a synchronous reference frame (d-q PLL) with the Park transformation. This kind of PLL is very simple to design, allows zero steady state tracking error and very good dynamic performances. However, its application to a single-phase system is not straightforward since the quadrature signal of the grid voltage is not present and it must to be obtained in some way. A possibility is to generate the fictitious quadrature signal by delaying the grid voltage by a quarter of its period. This method permits to achieve a good frequency tracking behavior as long as the frequency of grid remain to a fixed value, i.e. 50 Hz. As the standards allow a slight variations of the grid frequency, when the value of the frequency is not exactly 50 Hz an error in the quadrature signal is introduced by the fixed time delay that was originally calculated for a 50 Hz signal. Therefore, the tracking method gets no longer the correct frequency.

This drawback was solved in [44], where a modified Park transform was employed. Basically, the trigonometric functions of the Park transforms are not computed directly, but the cosine is obtained as a delayed version of the computed sine of the angle, see Fig. 3.8. T_n represents the nominal value of the grid voltage period.

Considering the grid voltage $v_{grid} = V_g \sin\theta_i$ with $\theta_i = \omega_i t + \Phi_0$, the input of the

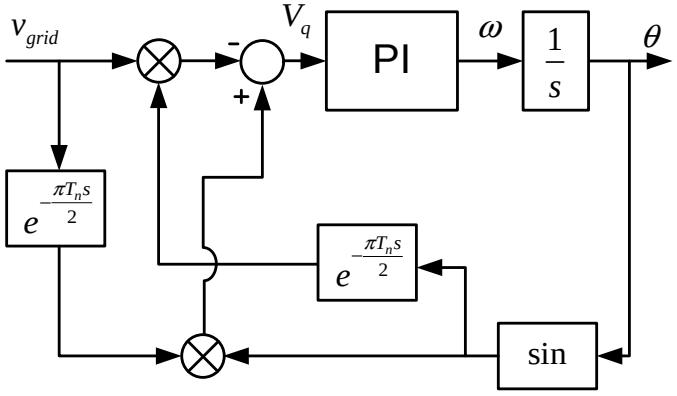


Fig. 3.8: Block scheme of the transport delay PLL.

PI regulator can be written as:

$$\begin{aligned} V_q &= -V_g \sin\theta_i \sin(\theta - \omega_i T_n/4) + V_g \sin\theta \sin(\theta_i - \omega_i T_n/4) \\ &= V_g \sin(\omega_i T_n/4)\,(\sin\theta_i \cos\theta - \sin\theta \cos\theta_i) \\ &= V_g \sin(\omega_i T_n/4) \sin(\theta_i - \theta) \end{aligned} \tag{3.5}$$

Equation (3.5) shows that even if $\omega_i T_n/4 \neq \pi/2$, i.e., the grid frequency varies, the phase error is compensated. Obviously, the presence of a delay line limits the dynamic performances. Moreover, it can be shown that this structure presents two points of stability, one whit $\theta = \theta_i$ and the other with $\theta = -\theta_i$.

This fact must be taken into account and the sign of the grid pulsation must be checked to ensure that the PLL is locked on the stable point with $\omega > 0$.

3.5.2 Control of the current injected into the grid

Voltage source inverters (VSI), as grid-connected converter, synthesize a sinusoidal output waveform through PWM modulation, which introduces a large amount of high frequency components. In order to reduce the switching harmonics, an output filter must be employed. The design of the output filter for grid-connected inverters is well studied in literature [45].

While an inductive L filter represent a simple solution, usually it cannot achieve satisfying performance in term of harmonic reduction unless a large inductance value is chosen. For this reason a LC or LCL filter is generally employed.

For this work an LC filter was employed. Fig. 3.9 represents the schematic of the LC output filter. The output voltage of the converter is represented by the pulse width generator V_{out}, v_{grid} is the grid generator, while v_{PCC} represents the actual voltage at the Point of Common Coupling (PCC), where the converter is connected. Inductor L_{grid} and resistor R_{grid} account for the impedance of the grid, while R_L and L_f are the resistive and inductive values of the filter inductor. In the schematic was also considered the equivalent series resistance ESR of the filter capacitor. It must be noted that R_f could also represent an actual resistor connected in series with the capacitor to damp the resonance of the LC circuit.

In fact, the transfer function $Y(s) = i_{grid}(s)/V_{out}(s)$ presents a marked resonance peak at $\omega_{res} = \sqrt{\frac{1}{C_f L_{eq}}}$, where L_{eq} is due to the parallel of L_f and L_{grid}. The value of the grid inductance is not known and it is affected by a great variability, although it is expected to be less than the filter inductor value. For this reason the resonant frequency of the circuit is greatly affected by the grid impedance and its value cannot be predicted precisely. The presence of a passive damping, as R_f, helps the circuit to prevent instability of the closed-loop system, even if the frequency of resonance may happen to be coincident with a harmonic of the synthesized output voltage of the converter. Nevertheless, since a large value of R_f leads to an increase of power losses also active damping methods were elaborated but they are not taken into account for this work.

The design of the LC filter usually starts by choosing the value of the filter inductor L_f in order to fulfill a first requirement for the output current ripple. The capacitor value is limited by the amount of reactive power that it absorbs, and it is used to further reduce the current ripple.

Depending on the rated power of the converter different filter parameters are chosen in order to comply with the regulations that limit the THD of the output current. The parameters chosen for the LC filter were $C_f = 4.4\mu F$, $R_f = 1\Omega$, $L_f = 1.5mH$, $R_L = 0.1\Omega$, $R_g = 0.25\Omega$ and $L_f = 40\mu H$.

The equations that describe the circuit are:

$$\begin{cases} i_{grid} = i_L - i_C \\ i_L = \dfrac{V_{out} - v_{PCC}}{R_L + sL_f} \\ i_C = \dfrac{sC_f v_{PCC}}{1 + sR_f C_f} \\ v_{PCC} = v_{grid} + i_{grid}(R_{grid} + sL_{grid}) \end{cases} \tag{3.6}$$

For the control, the grid voltage v_{grid} represents a disturbance, while the value v_{PCC} is the actual voltage that is sampled by the converter. Thus, it is possible to extrapolate the block diagram of the system, as shown in Fig. 3.10, where the reported transfer functions are:

$$\begin{cases} G_1(s) = R_{grid} + sL_{grid} \\ G_2(s) = \dfrac{sL_f C_f + sC_f(R_L + R_f) + 1}{1 + sR_f C_f} \\ G_3(s) = \dfrac{1}{R_L + sL_f} \end{cases} \tag{3.7}$$

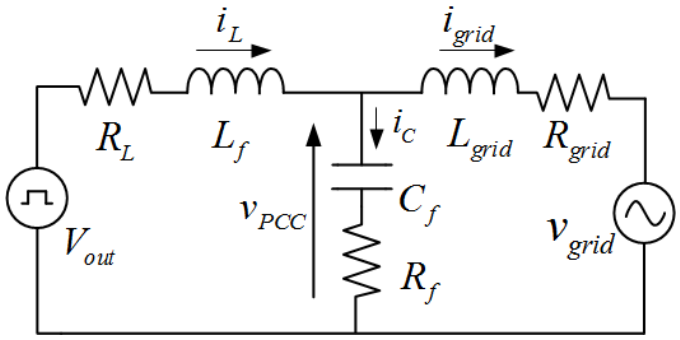


Fig. 3.9: Model of the grid-connected converter with a LC filter.

Since the v_{PCC} is known, and considering the behavior of the system just at low frequencies, the block diagram can be simplified as in Fig. 3.11, where only the transfer function $G_3(s)$ is taken into account. It is worth to note that the previous simplifi-

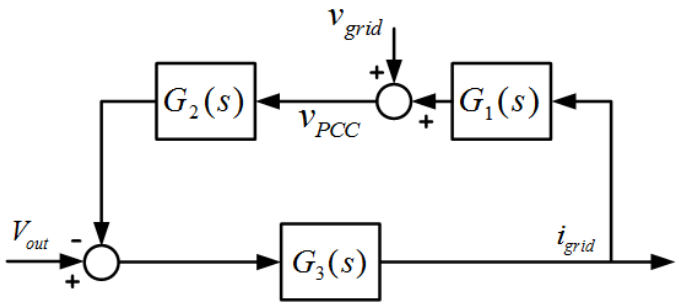


Fig. 3.10: Block diagram of the system.

cation was done considering the resonance frequency of the circuit far form the major low harmonics of the fundamental 50 Hz (i.e. third, fifth, seventh harmonics). With the chosen parameters the resonance frequency $freq_{res}$ is equal to 12.15 kHz, thus, if the band width of the current loop is not too large, the adopted simplification is acceptable at low frequencies.

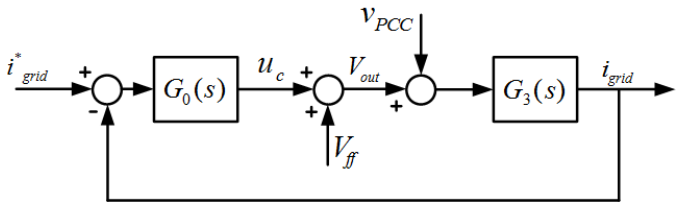


Fig. 3.11: Simplified block diagram of the control.

For the system in Fig. 3.11 the equation is:

$$i_{grid}(R_L + sL_f) = V_{out} - v_{PCC} \tag{3.8}$$

thus the inverter voltage should be controlled as follows:

$$V_{out} = u_c + v_{PCC} \tag{3.9}$$

in which u_c is the signal generated by the current controller. The current loop with the PI regulator is shown in Fig. 3.11, where $G_0(s) = K_p + K_i/s$, and V_{ff} is equal to v_{PCC}.

The Bode diagram of the current loop is reported in Fig. 3.12. As can be seen, the gain at 50 Hz is different from one. This it is due to the fact that the PI controller does not present an infinite gain at the grid frequency, leading to a steady state error.

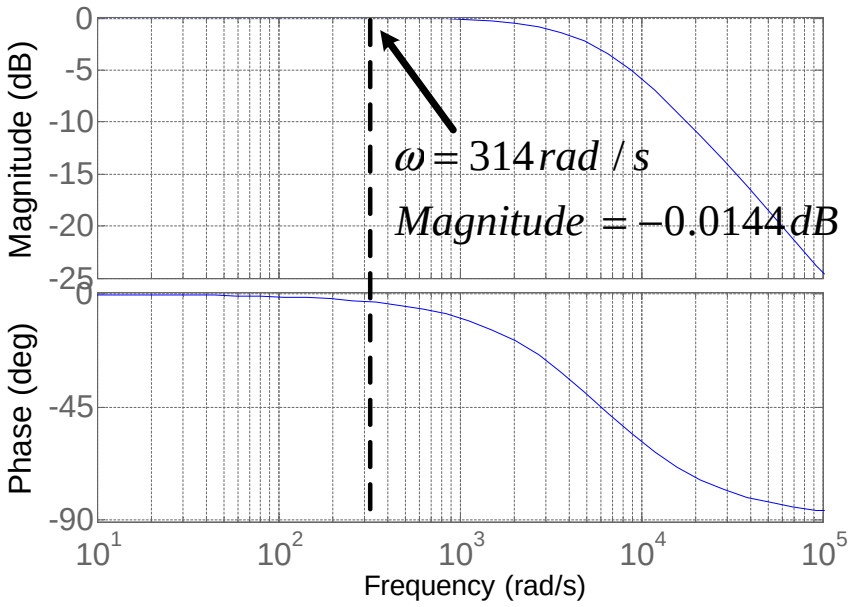


Fig. 3.12: Bode diagram of the current loop.

This problem can be overcome by a Proportional Resonant (PR) controller, which features infinite gain at a desired frequency, or by a PI in a reference frame synchronous with the grid. In the latter case, the variables of the system at 50 Hz can be seen as constants in the rotating reference frame, therefore a simple PI can guarantee the absence of error in steady state.

However, implementing a synchronous control in a single-phase system required the generation of a fictitious quadrature component, as already explained in section

3.5.1.

Fig. 3.13 shows a possible implementation of the d-q grid current control. A delay block is employed to generate the quadrature current signal, and a simple PI for each axis is employed. Obviously, only one output of the Park inverse transform is chosen as output voltage V_{out}. Depending on the convention chosen for the PLL, the active power axis can be either the direct or the quadrature one.

This controller exhibits excellent steady state performance and possibility to control active or reactive power. However, the presence of a delay line negatively affects its dynamic performance.

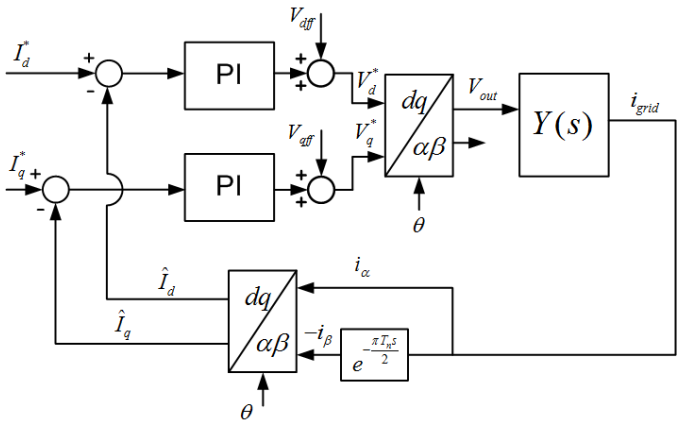


Fig. 3.13: Block scheme of the d-q current control for a single phase VSI.

3.5.3 Maximum Power Point Tracking

In a single-stage PV inverter, the DC Link is directly connected to the photovoltaic field. Controlling the DC-Link voltage, it means to control the operating voltage of the PV field. The control of the DC Link voltage can be realized through the choice of a desired value of the current injected into the grid. The DC Link voltage then follows the well-known characteristic of the photovoltaic cell, which can be derived by the equivalent circuit of a PV cell (Fig. 3.14), where the voltage-current characteristic can be expressed, for silicon PV cells, as:

$$I = I_{pv} - I_0 \left(e^{\frac{q(V+R_S I)}{nkT}} - 1 \right) \tag{3.10}$$

In equation (3.10), I_{pv} represents the current due to the photoelectric effect (variable with the solar irradiance), the diode D models the p-n junction and R_p and R_s the parallel and series resistance of the cell. The current drained by the parasitic resistance was neglected.

The series-parallel connection of multiple PV cells leads to a PV module, and the PV system installers design the connection of multiple PV panels in order to match the requirement of the grid-connected inverter.

For example, Fig. 3.15 represents a typical voltage-current characteristic of a 3.8 kW PV field.

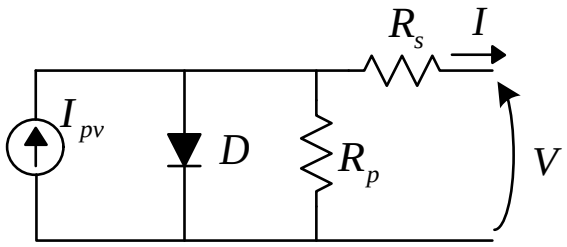


Fig. 3.14: Equivalent circuit of a PV cell.

In order to maximize the energy harvested from the PV field, it is important that the inverter makes the PV field to work at its maximum power point. Fig. 3.16 shows the voltage-power characteristic of the PV field described by Fig. 3.15. It is obvious that the operating point V=400 V corresponds to the maximum available power in these operating conditions.

Therefore, the comprehensive control of a PV inverter must implement, in addition to the basic current controller, also a DC Link controller, whose set-point is generated by a specific algorithm that tries to track the MPP in every working condition. This was depicted in Fig. 3.7.

Different MPPT algorithms were proposed and a review of the different MPPT techniques can be found in [1].

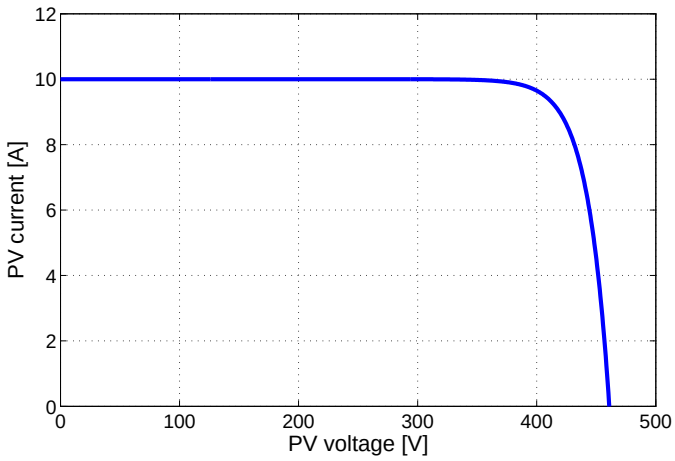


Fig. 3.15: Voltage-Current characteristic of a PV field.

Among the different MPPT technique in this work the **Perturb and Observe (P&O)** algorithm was adopted.

It is based on the continuous perturbation of the system operating point, in the attempt to move the system towards the increasing power. At each step the instantaneous power drained from the PV field is computed and confronted with the memorized value for the previous operating point of the system, then the control pushes the system toward the direction of the positive gradient of the power. In steady-state conditions the algorithm oscillates around the maximum power point, inverting the sign of the perturbation at every sampling interval. This behavior also represents the main drawback of this method, since in order to achieve good MPP tracking the perturbation must be sufficiently high, but the higher the perturbation, the higher the oscillation around the MPP at steady state, and consequently the lower the MPP tracking efficiency.

In order to solve this drawback the magnitude of the perturbation was not fixed but variable in order to obtain good tracking performance with little steady-state oscillation. The width of the perturbation was at its maximum initially and gradually decreased as the gradient of the power becomes less steep.

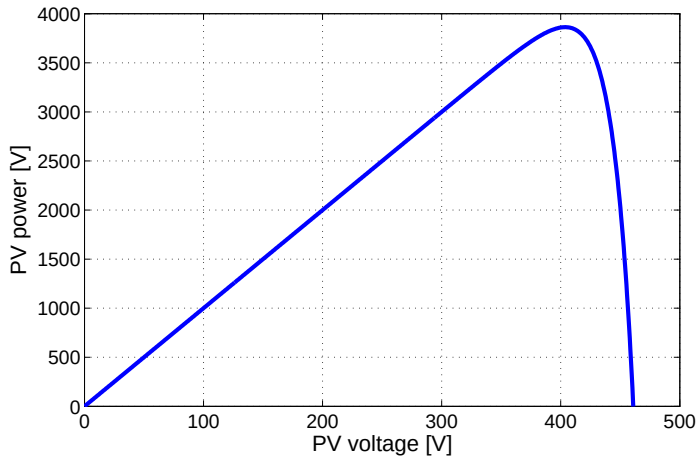


Fig. 3.16: Voltage-Power characteristic of a PV field.

3.6 Simulation results

The proposed solution was simulated using PLECS toolbox in a Simulink/Matlab environment. The schematic used for the simulations is reported in Fig. 3.17. The parameters of the active common-mode transformer designed in the last part of section 3.3.2 were used in the simulations.

A simple PI+feed forward current controller is used to inject 3 kVA of electric power into the grid with variable power factor.

Extensive simulations were performed with the attempt to put in evidence the performance of the proposed solution regarding common-mode voltage and ground leakage current rejection.

The simulations were realized with a DC voltage source of 400 V, a grid voltage of $230V_{RMS}@50Hz$ and a switching frequency f_{sw}= 30 kHz. The output filter was formed by two inductors $L_f = 0.75mH$ and a capacitor $C_f = 4.4\mu F$. The parasitic capacitance of the photovoltaic field was modeled with two equivalent capacitors connected to the positive and negative poles of the DC Link, and their values were fixed equal to $300nF$. For the ground connection, a resistance $R_g = 3\Omega$ was conside-

red. This value is within the limits $(2-5\Omega)$ recommended by IEEE standards. Two inductors $L_{grid} = 40\mu H$ accounted for the distributed inductance of the grid.

Fig. 3.18 shows the common-mode voltage compensation operated by the proposed solution. Fig. 3.19 and Fig. 3.20 show the grid voltage and current, the common-mode current and the primary current of the common-mode transformer in the case of $PF = 1$ and $PF = 0.75$. The common-mode current shown in the two figures presents only the fundamental component due to the common-mode voltage component of the grid and put in evidence the correct behavior of the proposed solution.

Fig. 3.21 shows the common-mode current when the primary of the common-mode transformer was not connected. In this case the common-mode transformer operated as a simple common-mode inductor with a value of $2 * L_{cm} = N_2^2/\mathscr{R}_m = 3.2mH$.

The common-mode current results in this case, as known in literature, very high.

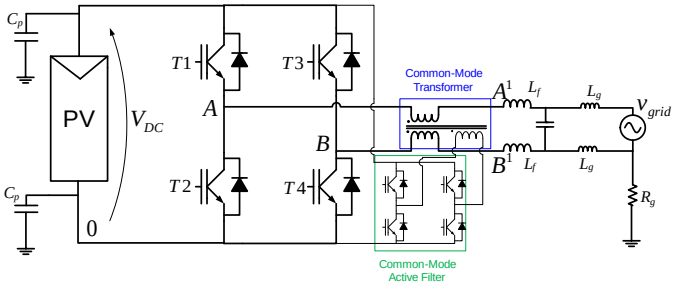


Fig. 3.17: Schematic of the simulation circuit.

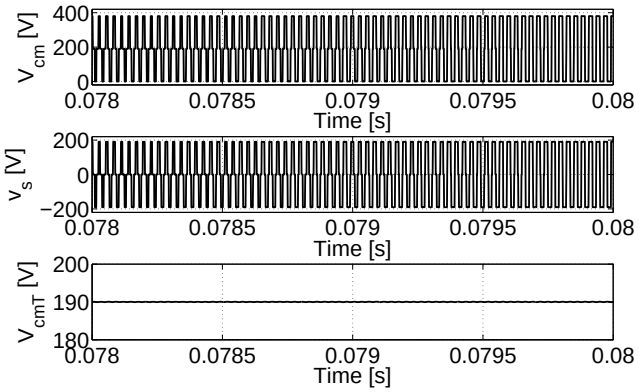


Fig. 3.18: Simulation results. V_{cm}, v_s and V_{cmT} with reference to Fig. 3.2.

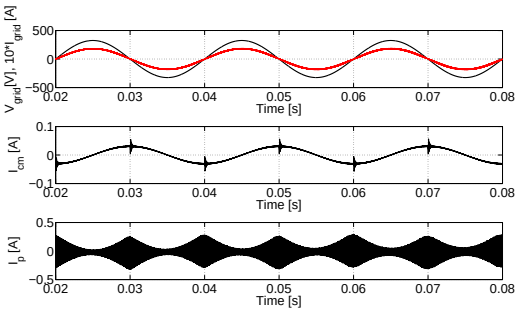


Fig. 3.19: Grid voltage and current, ground leakage current and primary current of the active common-mode inductor in case of PF=1, $2C_p = 600nF$.

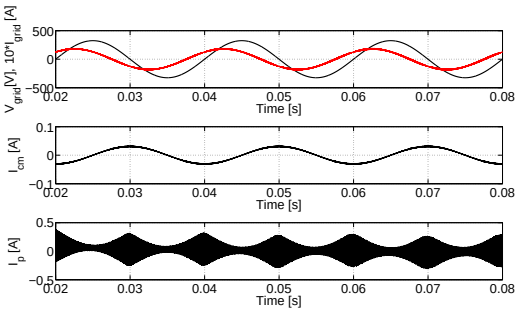


Fig. 3.20: Grid voltage and current, ground leakage current and primary current of active common-mode inductor in case of PF=0.7, $2C_p = 600nF$.

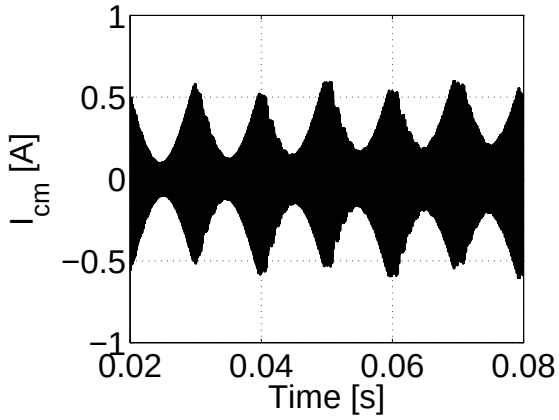


Fig. 3.21: Common-mode current in case of passive common-mode inductor, PF=1, $2C_p = 600nF$.

3.7 Converter Prototype

In order to test the proposed solution, a converter prototype was built. The prototype was obtained rearranging the hardware used for a precedent Ph.D. thesis [43]. The prototype includes the CPU, which implements the control and the modulation strategy, both the full-bridges, for the main and active filter converter, the sensors, the power supply for the logic and analog circuits and the output filter. Due to the complexity of the design and the number of components involved, three boards were employed: the control board, the power board and the output stage board.

3.7.1 Control board

The control board embeds the digital signal controller (DSC) TMS320F28335, a 150MHz, 32bit floating-point processor by Texas Instruments. The high number of PWM channels (12) and Analog to Digital Converter Channels (16) make it particularly suitable for the proposed converter.

The control board also embeds voltage regulators, 3.3 V for the peripherals and 1.9 V for the core of the DSC, and the protection circuit for the ADC.

The complete schematic and PCB are found in Appendices A1.1 and A1.2.

3.7.2 Power board

The power board incorporates the two full-bridge inverters along with their driving circuits and the DC Links filter capacitors, plus additional I/O circuits such as, Digital to Analog Converter (DAC) TLV5631, and a RS485 transceiver SN75LBC182D (appendix A1.3).

Gate drivers

The gate driver circuit is composed of an optocoupler and an insulated power supply for each power device, in order to have a very flexible and independent control on each power device.

The chosen optocoupler is the Allegro ACPL-J313. The insulated power supply is generated by the IC MAX256 that drives a 1:2 transformer followed by a voltage multiplier. The schematic is illustrated in Fig. 3.22.

The PWM signals generated by the DSP are multiplied through logic end gates with the signal generated by the fault circuit. The fault circuit is a latch that, in case of overcurrent, forces to zero its output, consequently disabling all the logic gates.

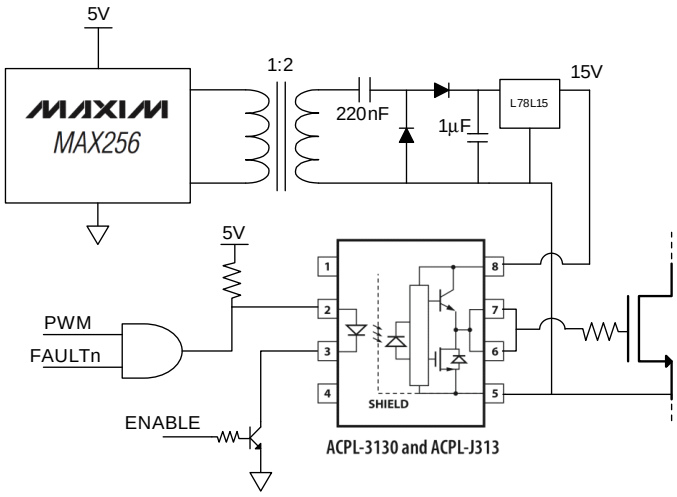


Fig. 3.22: Gate driver circuit with insulated power supply.

The logic gates are in open drain configuration. In this way the current absorbed by the photodiodes is given by the 5 V power supply and not by the logic gates itself. This, however, poses a problem in case of malfunctioning or non-uniform turn on of the devices. In fact, if the logic gate is not powered, every photodiode is conducting due to the pull-up resistor. For this reason, every cathode of the gate drivers is connected to the collector of a BJT. Only if the BJT is polarized it is possible to turn on the gate drivers.

The complete schematic of the gate drivers is reported in appendix A1.4.

Power section

The power section embeds the two full-bridges, realized with discrete power devices. Moreover, in order to prevent overvoltages, turn-off RC snubbers are present in each controlled device.

The DC link voltage is measured by a circuit, reported in Fig. 3.23, that employs a linear optocoupler, the Avago HCNR201. The two operational amplifier acts as a voltage to current and as current to voltage converters. The feedback control of the the LED embedded in the optocoupler forces the photodiode to work in its linear region.

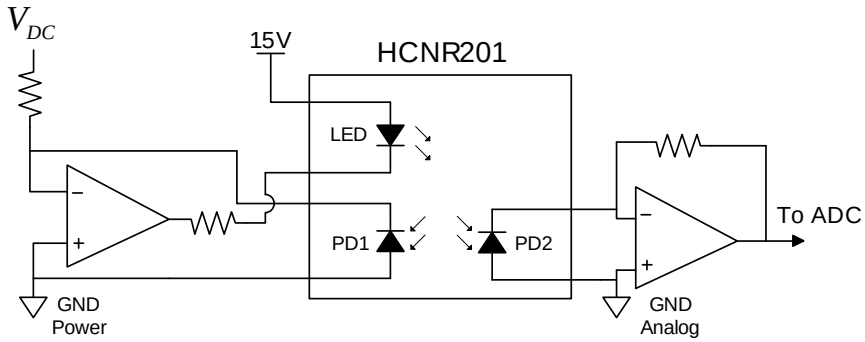


Fig. 3.23: Circuit employed to measure the DC Link voltages with the optolinear coupler.

The complete schematic of the power section is reported in appendix A1.5, and the complete PCB of the power board is shown in appendix A1.6.

3.7.3 Output Stage Board

Power supply

In order to generate all the supply voltages needed for the converter, a flyback based on the IC TOP257-PN was adopted. Fig. 3.24 shows an example of the general flyback circuit. The controller incorporates an active switch used to drive the prima-

ry of the transformer. The DC supply is obtained by a simple diode bridge rectifier, allowing the circuit to be used with DC or AC sources.

A current feedback it used to control the 5V output voltage.

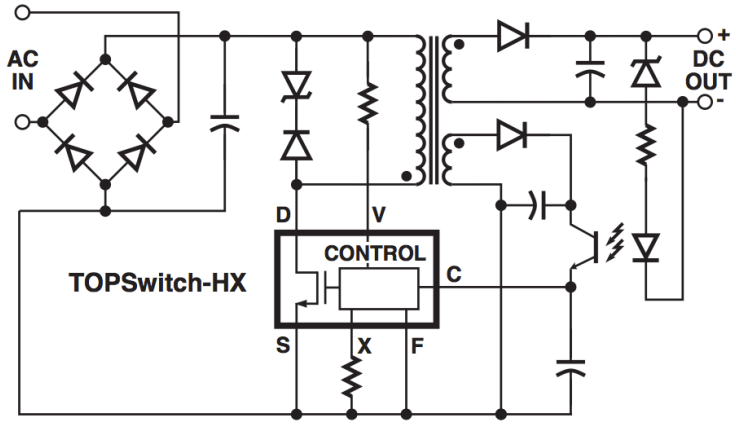


Fig. 3.24: Example circuit of the flyback converter from the TOP257-PN datasheet.

Appendix A1.7 shows the complete schematic of the realized flyback converter. Along with the regulated 5V, additional windings for the +17 V and -17 V (used by the analog circuits) were added to the design. Even an auxiliary winding for the operation of the TOP257-PN and an isolated +15 V are present. It is important to note that the 5 V is the only output regulated by the flyback controller; the other outputs can vary their voltage depending on the duty cycle variations of the IC due to varying load. For this reason, to ensure the stability of the power supplies, the unregulated outputs are followed by linear regulators.

Output filter

The output filter includes all the devices needed for the grid-connection of the system, along with the common-mode transformer and the sensors for the current control and the grid synchronization. Fig. 3.25 shows the basic schematic of the output filter. A couple of relays operate the connection and disconnection of the converter with the

grid. C_x-C_y are the common-mode filter capacitors coupled with the common-mode transformer, while the capacitor C_f is the differential output filter capacitor. An LEM CKSR-25NP is employed as a current transducer and a voltage transformer is used to measure the grid voltage.

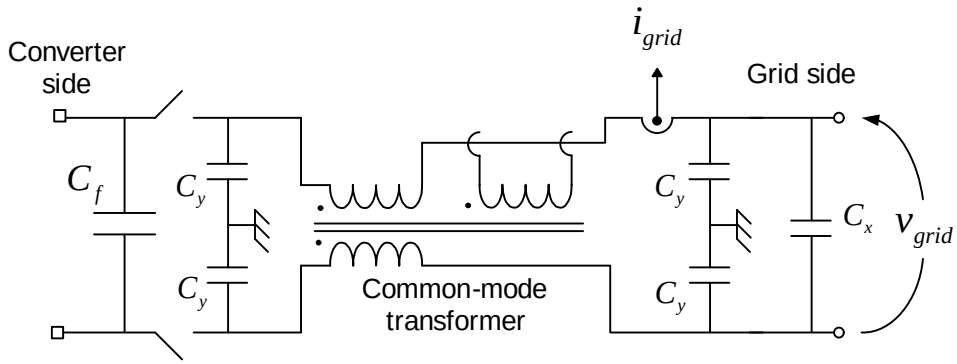


Fig. 3.25: Schematic of the output filter.

In order to comply with the regulations that supervise the grid connection of photovoltaic inverters, the prototype embedded the so-called intrinsic safety circuit. In other words, a hardware solution, which prevents the connection of the converter to the mains when the grid voltage is absent, was realized. A diode bridge rectifier was added at the output of the voltage transformer employed to sense the grid voltage. The rectified voltage was directly connected to the base of a BJT that is in series to the winding of the relays. If the grid voltage is absent the BJT is off, preventing current flowing in the relays' winding, and consequently the connection to the grid of the converter.

The complete schematics of the output filter are reported in appendix A1.8, and the PCB is reported in appendix A1.9.

Fig. 3.27 presents a picture of the boards. The layout of the screws was realized to stack the output board on the top of the power board. Fig. 3.28 shows a detail of the common-mode transformer.

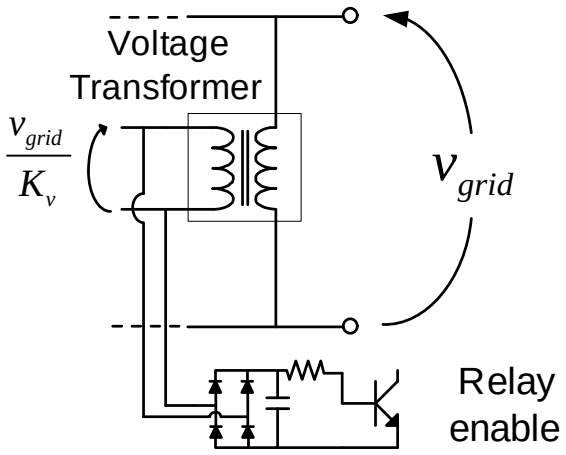


Fig. 3.26: Intrinsic safety circuit.

3.8 Experimental results

A specific test bed was realized in order to test the performance of the inverter prototype in terms of power quality and ground leakage current. In Fig. 3.29 a schematic diagram of the test bed is shown. The converter was supplied by a DC source and directly connected to the grid. Since an existing converter was adapted to realize the proposed solution, as explained in section 3.7, the common-mode transformer in this case is located after the filter inductors, differently from what it was done in simulations (Fig. 3.17). Despite the difference in the schematic the results are consistent with the simulations, as the common-mode path results not affected by the position of the common-mode transformer.

The Texas Instruments TMS320F28335 DSP generates the PWM control signals for both full-bridges, elaborating the current control and all the digital calculations. The current loop operates at the switching frequency. Table 3.2 lists the parameters of the setup.

The performance of the prototype will be discussed in the following with a series of oscilloscope captures.

Fig. 3.30 and Fig. 3.31 show the grid voltage and the injected grid current with the

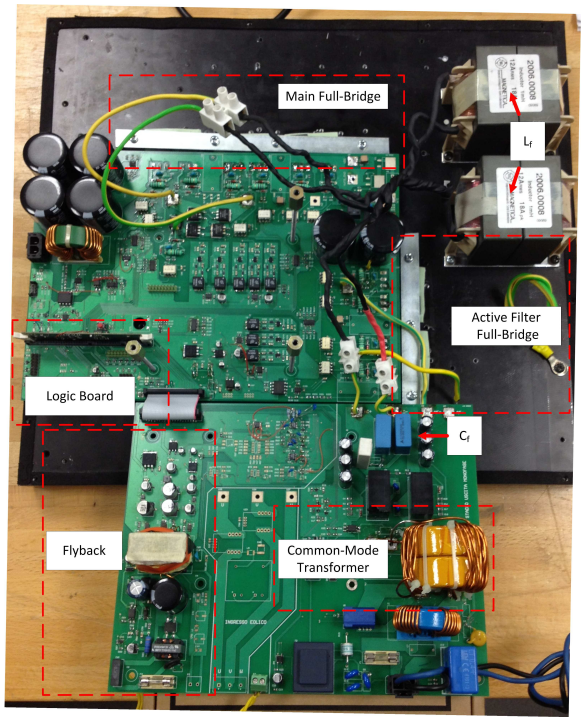


Fig. 3.27: Picture of the prototype with the boards separated.

active filter enabled and with different power factors. The THD of the grid current is equal to 3.4% in case of unity power factor. The behavior is almost unaffected when reactive power is supplied to the grid, and the THD of the grid current rises to 4.6%.

Fig. 3.32 and Fig. 3.33 report the common-mode voltage at the output of the full-bridge, v_{cm}, the voltage at the secondary winding of the common-mode transformer, v_s, and the resulting total common-mode voltage v_{cmT} respectively without and with the dead-time compensation strategy described in section 3.2.1.

The figures refer to the positive half-wave of the grid current. It is possible to recognize the system behavior described in Section 3.2.1. When the dead-time compensation strategy is not applied (Fig. 3.32) the v_{cm} and v_s waveforms do not match perfectly and the small differences result in the generation of pulses, with width equal to the dead-time interval (i.e. 600 ns) in the v_{cmT} waveform. The differences between

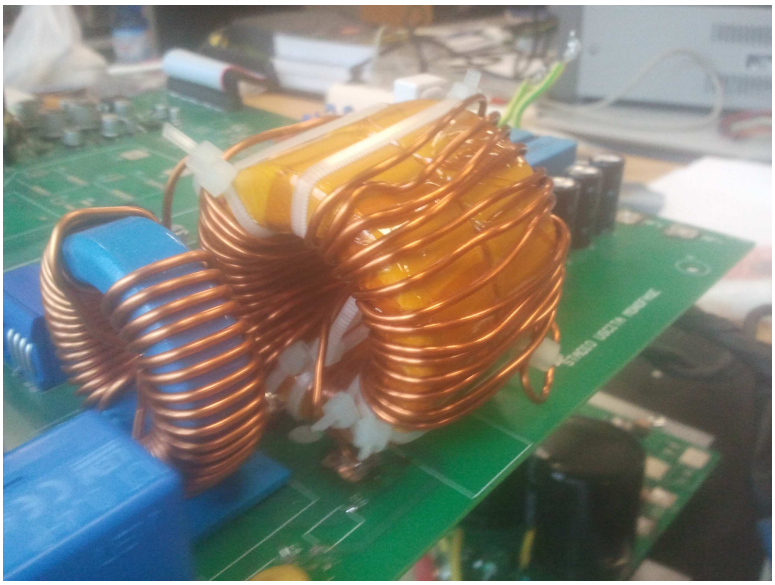


Fig. 3.28: Picture of the common-mode transformer.

v_{cm} and v_s are strongly reduced when the dead-time compensation strategy is applied, as in Fig. 3.33, allowing to mitigate v_{cmT} variations (in this case the maximum width of the pulses resulted equal to 20 ns, the maximum amplitude does not change and is equal to 200 V).

Fig. 3.34 and Fig. 3.35 show the ground voltage and leakage current when a 200 nF capacitor simulates the parasitic capacitance of the photovoltaic field respectively without and with the dead-time compensation enabled.

In the first case the resulting current is $i_{cm} = 22$ mA rms, while in the second case the current is reduced to $i_{cm} = 15$ mA rms.

As a comparison term, Fig. 3.36 shows the same waveforms of Fig. 3.35 when the active filter is disabled. It is important to highlight that in this experiment the primary winding of the common-mode transformer was disconnected and therefore the magnetic component operated as a standard common-mode inductor.

Due to unacceptable levels of ground leakage current, in this case a capacitor of only 6.6 nF was used to simulate the parasitic capacitance. It is evident that the

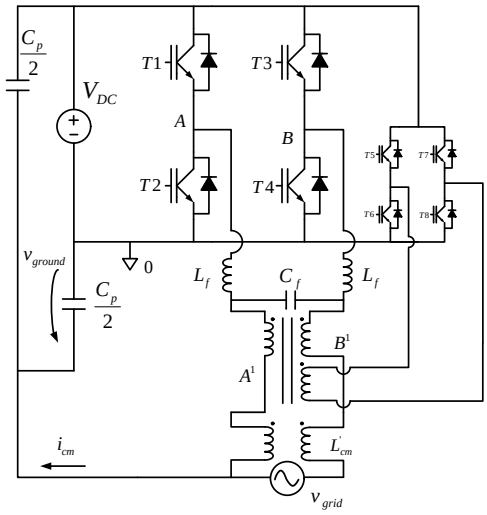


Fig. 3.29: Schematic of the test bed.

ground voltage was also heavily distorted, due to the superposition of a marked high-frequency component. Despite the small 6.6 nF capacitor, the resulting ground leakage current is $i_{cm} = 169$ mA rms. This value is well beyond the limits enforced by international regulations. The quality of the injected grid current also decreased, the THD increased to 3.9% and 5.0% respectively in case of power factor equal to 1 or 0.8. This behavior is due to the presence of several harmonic components in the injected grid current, centered at 30 kHz, introduced by the common-mode current.

Fig. 3.37 and Fig. 3.38 show the common-mode transformer primary voltage and current waveforms far from the grid voltage zero crossing, respectively at no-load (i.e., zero grid current, open secondaries) and during normal operation. The expected behavior of Fig. 3.4 and Fig. 3.5 can be recognized. The rms value of the primary current over a grid voltage period is i_p=200 mA. The difference between no-load and normal operation is due to the grid current flowing into the common-mode transformer secondaries. The grid current should not ideally modify the common-mode transformer flux, but in actual applications a very small perturbation may appear due to unavoidable asymmetries. The oscillating behavior during the commutations of

Table 3.2: Parameters for the experimental setup

Name	Description	Value
V_{DC}	input DC voltage	$400V$
v_{grid}	grid voltage	$230V_{RMS}$
f_{grid}	grid frequency	$50Hz$
f_{sw}	Switching frequency	$30kHz$
L_f	AC inductor filter	$0.75mH$
C_f	AC capacitor filter	$4.4\mu F$
C_p	equivalent PV parasitic capacitances	$200nF$
		or $6.6nF$
n_P	primary turns common-mode transformer	30
n_S	secondary turns common-mode transformer	15
L_m	primary inductance common-mode transformer	$6.3mH$
L'_{cm}	inductance of the additional	$1mH$
	common-mode inductor	

the switches is due to the large output capacitance of the high-power devices used to drive the common-mode transformer primary. If proper low-power devices were used, the lower output capacitance would have resulted in limited ringing during the commutations.

Eventually, tests of the system efficiency were performed with a power meter. The total efficiency of the converter was measured in both cases of active common-mode filter enabled and disabled. With the common-mode active filter disabled, the primary winding was disconnected from the additional low power full-bridge, which was not driven by PWM signals. Fig. 3.39 shows the efficiency as a function of the converter output power.

The additional loss due to the active filter is equal to 4 W and it is independent from the power supplied to the grid by the converter. For this reason, the presence of the active filter does not significantly affect the total system efficiency at output power values close to the rated power of the converter. It should be noted that the choice

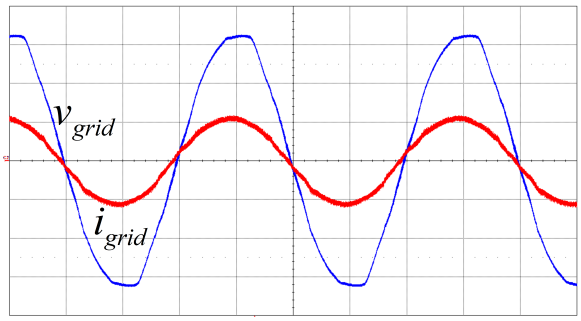


Fig. 3.30: v_{grid} 100 V/div, i_{grid} 10 A/div. Time base 5 ms/div. Unity Power factor operation.

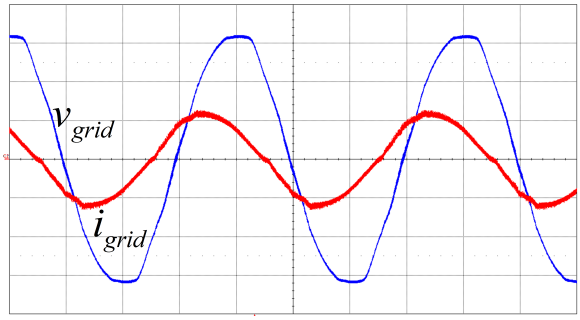


Fig. 3.31: v_{grid} 100 V/div, i_{grid} 10 A/div. Time base 5 ms/div. Power factor equal to 0.8.

of the same devices for the two full-bridge structures benefits the efficiency measures with the adopted test bed. As low-power devices with limited current capability (and higher on-state resistance) would be adopted in an actual application, the power losses of the full-bridge driving the common-mode transformer would increase. However, considering the very small rms value of the common-mode transformer primary current, the increased losses should not have a significant impact on the efficiency even considering a much higher on-state resistance of the devices.

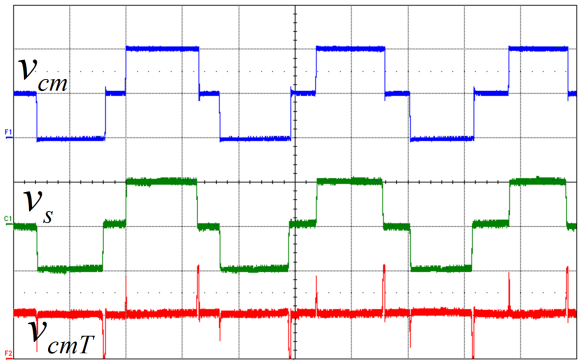


Fig. 3.32: v_{cm} 200 V/div, v_s 200 V/div, v_{cmT} 200 V/div. Time base 10 µs/div.

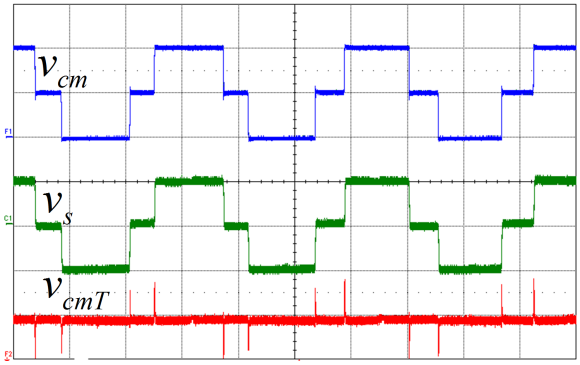


Fig. 3.33: v_{cm} 200 V/div, v_s 200 V/div, v_{cmT} 200 V/div. Time base 10 µs/div. Deadtime compensation enabled.

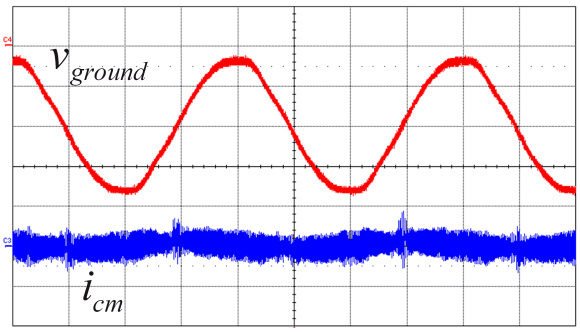


Fig. 3.34: v_{ground} 200 V/div, i_{cm} 100 mA/div. Time base 5 ms/div. Dead time compensation disabled. $C_p = 200nF$

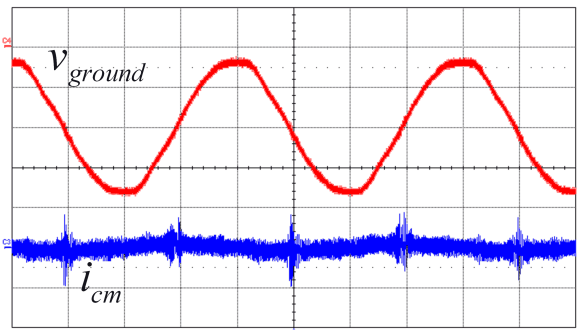


Fig. 3.35: v_{ground} 200 V/div, i_{cm} 100 mA/div. Time base 5 ms/div. Deadtime compensation enabled. $C_p = 200nF$

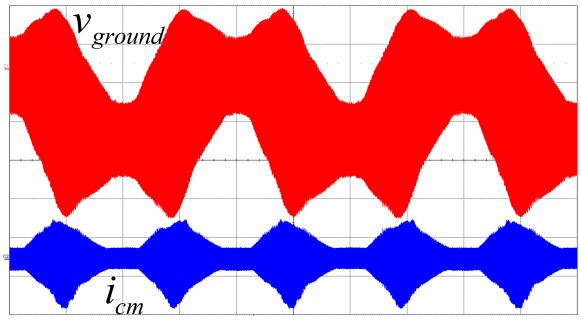


Fig. 3.36: v_{ground} 200 V/div, i_{cm} 500 mA/div. Time base 5 ms/div. Active filter disabled. $C_p = 6.6nF$

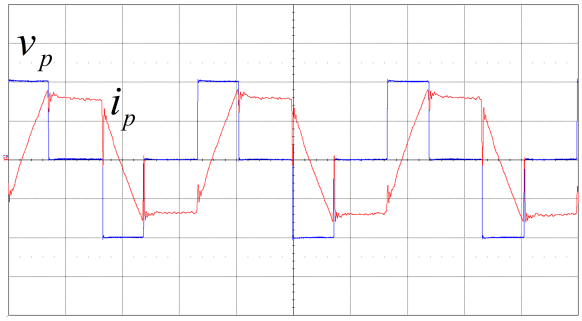


Fig. 3.37: v_p 200 V/div, i_p 100 mA/div at no load. Time base 10 µs/div.

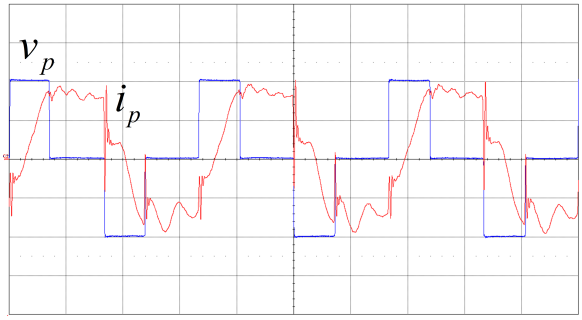


Fig. 3.38: v_p 200 V/div, i_p 100 mA/div during normal operation. Time base 10 µs/div.

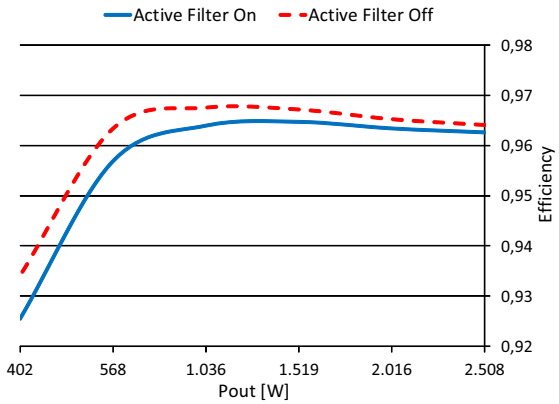


Fig. 3.39: Converter efficiency when the active filter is enabled (solid line) and disabled (dotted line).

Chapter 4

Conclusions

In this work, the issue of ground leakage current in PV trasformerless grid-connected converters was investigated and analyzed. The ground leakage current phenomenon was proven to be due to the presence of a parasitic capacitance between the PV cells and the metal structure of the panels. A survey of the actual solutions to avoid the arising of ground leakage current in transformerless single-phase systems was also elaborated, and a novel classification for transformerless inverters was proposed as well.

The principal causes of ground leakage current were highlighted, and the contribution to the phenomenon of the common-mode voltage generated at the output of the grid-connected inverters during their operation was analyzed. As investigated, the common-mode voltage at the output of the converters v_{cm} generates currents that flow in the parasitic capacitance throughout the connection to the ground of the neutral wire of the grid at the MV/LV transformer. For this reason the ground leakage current is also known as common-mode current.

A novel approach to cancel the common-mode voltage variations at the output

of a transformerless grid-connected converter was proposed. This solution relies on an active common-mode filter connected at the output of the power converter. It is constituted by a common-mode transformer properly supplied by an additional low-power full-bridge.

The proposed solution is applicable to both stand-alone and grid-connected converters. In particular in this work the active filter was applied to a full-bridge power converter topology driven by the efficient 3-level (unipolar) PWM.

The feasibility of the proposed solution and the capacity to operate with power factor different from one was proven through extensive simulations in Simulink/Plecs environment, and confirmed with experimental results.

On this purpose, a converter prototype was designed and built. It embeds all the components for enabling the connection to the mains in accordance to the Italian legislation CEI 0-21.

The experimental results were in accordance with the simulations. In particular, in real converters slight variations in the total common-mode voltage are introduced by the dead time intervals of the PWM modulation strategy. For this reason a dead-time compensation strategy able to minimize the v_{cm} variations, and therefore the common-mode current was elaborated.

Simple design guidelines for the active common-mode filter were presented in order to minimize the size of passive components and in particular the core of the common-mode transformer employed.

A fair comparison with the state of the art was elaborated for the proposed solution in terms of number of power devices employed, efficiency and reliability.

It was highlighted that the proposed solution requires four additional power switches with respect to a full-bridge solar inverter, but as they need to provide only the magnetizing current of the common-mode transformer, the additional losses resulted to be very low. In particular, in the prototype the additional power losses introduced by the active common-mode filter resulted equal to 4 W compared to 2000 VA of injected power. It is important to put in evidence that only standard and low-cost power switches were used in the laboratory prototype. With a more accurate choice of the power devices, employing SiC or GaN devices, the power losses could be even lower.

Furthermore, it is also possible to oversize, without a significant increase of cost, the power size of the 4 additional power switches in order to avoid an overall reliability reduction of the power converter due to the increased number of power switches.

Bibliografia

[1] B. Subudhi and R. Pradhan. A Comparative Study on Maximum Power Point Tracking Techniques for Photovoltaic Power Systems. *IEEE Transactions on Sustainable Energy - In press, available on IEEE Early Access.*

[2] IEEE Application Guide for IEEE Std 1547, IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems. In *IEEE Standard 1547.2-2008*, pages 1–207, :Apr. 2009 2009.

[3] Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid. In *VDE V 0126-1-1,* :2006-02 2006.

[4] Reference technical rules for the connection of active and passive users to the LV electrical Utilities. In *CEI 0-21,* : 2012-06 2012.

[5] Electromagnetic Compatibility (EMC) - Part 3-2: Limits - Limits for Harmonic Current Emissions (Equipment Input Current Under 16 A Per Phase). In *EN 61000-3-2:2006,* 2006.

[6] Electromagnetic compatibility (EMC) - Part 3-12: Limits - Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current >16 A and <75 A per phase . In *IEC 61000-3-12 ed2.0,* :2011-05 20011.

[7] F. Berba, David Atkinson, and M. Armstrong. A review of minimisation of output dc current component methods in single-phase grid-connected inverters

pv applications. In *Environment Friendly Energies and Applications (EFEA), 2012 2nd International Symposium on*, pages 296–301, 2012.

[8] F. De Mango, M. Liserre, A.D. Aquila, and A. Pigazo. Overview of anti-islanding algorithms for pv systems. part i: Passive methods. In *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, pages 1878–1883, 2006.

[9] Zhihong Ye, A. Kolwalkar, Y. Zhang, Pengwei Du, and R. Walling. Evaluation of anti-islanding schemes based on nondetection zone concept. *Power Electronics, IEEE Transactions on*, 19(5):1171–1176, 2004.

[10] B. Verhoeven et al.. Utility Aspects of Grid Connected Photovoltaic Power Systems. In *International Energy Agency Photovoltaic Power Systems IEA PVPS T5-01*, 1998.

[11] J. H R Enslin and Peter J M Heskes. Harmonic interaction between a large number of distributed power inverters and the distribution network. *IEEE Transactions on Power Electronics*, 19(6):1586–1593, 2004.

[12] K.. De Brabandere, Bruno Bolsens, J.. Van den Keybus, A. Woyte, J. Driesen, and R. Belmans. A voltage and frequency droop control method for parallel inverters. *IEEE Transactions on Power Electronics*, 22(4):1107–1115, 2007.

[13] Yunjie Gu, Wuhua Li, Yi Zhao, Bo Yang, Chushan Li, and Xiangning He. Transformerless inverter with virtual dc bus concept for cost-effective grid-connected pv power systems. *IEEE Transactions on Power Electronics*, 28(2):793–805, 2013.

[14] S.V. Araujo, P. Zacharias, and B. Sahan. Novel grid-connected non-isolated converters for photovoltaic systems with grounded generator. In *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pages 58–65, 2008.

[15] D. Barater, G. Buticchi, A.S. Crinto, G. Franceschini, and E. Lorenzani. A new proposal for ground leakage current reduction in transformerless grid-connected converters for photovoltaic plants. In *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, pages 4531–4536, 2009.

[16] Bo Yang, Wuhua Li, Yunjie Gu, Wenfeng Cui, and Xiangning He. Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system. *IEEE Transactions on Power Electronics*, 27(2):752–762, 2012.

[17] G. Buticchi, D. Barater, E. Lorenzani, and G. Franceschini. Digital control of actual grid-connected converters for ground leakage current reduction in pv transformerless systems. *IEEE Transactions on Industrial Informatics*, 8(3):563–572, 2012.

[18] Dong Dong, Fang Luo, D. Boroyevich, and P. Mattavelli. Leakage current reduction in a single-phase bidirectional ac-dc full-bridge inverter. *IEEE Transactions on Power Electronics*, 27(10):4281–4291, 2012.

[19] D. Meneses, F. Blaabjerg, O. Garcia, and J.A. Cobos. Review and comparison of step-up transformerless topologies for photovoltaic ac-module application. *IEEE Transactions on Power Electronics*, 28(6):2649–2663, 2013.

[20] S.B. Kjaer, J.K. Pedersen, and F. Blaabjerg. A review of single-phase grid-connected inverters for photovoltaic modules. *IEEE Transactions on Industry Applications*, 41(5):1292–1306, 2005.

[21] Jianhua Wang, Baojian Ji, Jianfeng Zhao, and Jie Yu. From h4, h5 to h6 - standardization of full-bridge single phase photovoltaic inverter topologies without ground leakage current issue. In *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, pages 2419–2425, 2012.

[22] P. Hacke, K. Terwilliger, R. Smith, S. Glick, J. Pankow, M. Kempe, S.K.I. Bennett, and M. Kloos. System voltage potential-induced degradation mechanisms

in pv modules and methods for test. In *Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE*, pages 000814–000820, 2011.

[23] P. Hacke, R. Smith, K. Terwilliger, S. Glick, D. Jordan, S. Johnston, M. Kempe, and S. Kurtz. Testing and analysis for lifetime prediction of crystalline silicon pv modules undergoing degradation by system voltage stress. *IEEE Journal of Photovoltaics*, 3(1):246–253, 2013.

[24] Mei Wen and P. Ricou. Evaluating tco long-term performance by electrochemical corrosion test and residual film stress analysis. In *Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE*, pages 001332–001335, 2012.

[25] T. Kerekes, R. Teodorescu, and U. Borup. Transformerless photovoltaic inverters connected to the grid. In *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, pages 1733–1737, 2007.

[26] Baojian Ji, Jianhua Wang, and Jianfeng Zhao. High-efficiency single-phase transformerless pv h6 inverter with hybrid modulation method. *IEEE Transactions on Industrial Electronics*, 60(5):2104–2115, 2013.

[27] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo. Transformerless Inverter for Single-Phase Photovoltaic Systems. *IEEE Transactions on Power Electronics*, 22(2):693 –697, March 2007.

[28] D. Barater, G. Buticchi, A.S. Crinto, G. Franceschini, and E. Lorenzani. Unipolar pwm strategy for transformerless pv grid-connected converters. *IEEE Transactions on Energy Conversion*, 27(4):835–843, 2012.

[29] Wensong Yu, Jih-Sheng Lai, Hao Qian, and C. Hutchens. High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Nonisolated AC-Module Applications. *IEEE Transactions on Power Electronics*, 26(4):1253 –1260, April 2011.

[30] A. Nabae, I. Takahashi, and H. Akagi. A new neutral-point-clamped pwm inverter. *IEEE Transactions on Industry Applications*, IA-17(5):518–523, 1981.

[31] O. Lopez, R. Teodorescu, and J. Doval-Gandoy. Multilevel transformerless topologies for single-phase grid-connected converters. In *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, pages 5191–5196, 2006.

[32] Li Zhang, Kai Sun, Lanlan Feng, Hongfei Wu, and Yan Xing. A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters. *IEEE Transactions on Power Electronics*, 28(2):730–739, 2013.

[33] German Patent. Wechselrichter. In *DE19642522C1*, 23 Apr 1998.

[34] German Patent. Transformerless ac. inverter circuit, for coupling photovoltaic systems or wind generator systems, esp. in the low power range, to current networks. In *DE19732218C1*.

[35] K. Kamisako M. Kusakawa, H. Nagayoshi and K. Kurokawa. Further improvement of a transformerless, voltage-boosting inverter for ac modules. In *Sol. Energy Mater. Sol. Cells*, page 379âĂŞ387, Mar. 2001.

[36] Y.-C. Son and Seung-Ki Sul. A new active common-mode emi filter for pwm inverter. *IEEE Transactions on Power Electronics*, 18(6):1309 – 1314, Nov. 2003.

[37] M.C. Di Piazza, A. Ragusa, and G. Vitale. An optimized feedback common mode active filter for vehicular induction motor drives. *IEEE Transactions on Power Electronics*, 26(11):3153 – 3162, Nov. 2011.

[38] M.L. Heldwein, H. Ertl, J. Biela, and J.W. Kolar. Implementation of a transformerless common-mode active filter for offline converter systems. *IEEE Transactions on Industrial Electronics*, 57(5):1772 – 1786, May 2010.

[39] M.C. Di Piazza, A. Ragusa, and G. Vitale. Common mode active filtering effects in induction motor drives for application in electric vehicles. In *In Proc. of IEEE*

VPPC '09 Vehicle Power and Propulsion Conference 2009, pages 1421–1427, 2009.

[40] Jiang Yanshu, Xu Dianguo, and Chen Xiyou. Analysis and design of a feed-forward-type active filter to eliminate common-mode voltage generated by a pwm inverter. In *in Proc. of IEEE IECON 2002 28th Annual Conference of the Industrial Electronics Society*, volume 1, pages 771–775 vol.1, 2002.

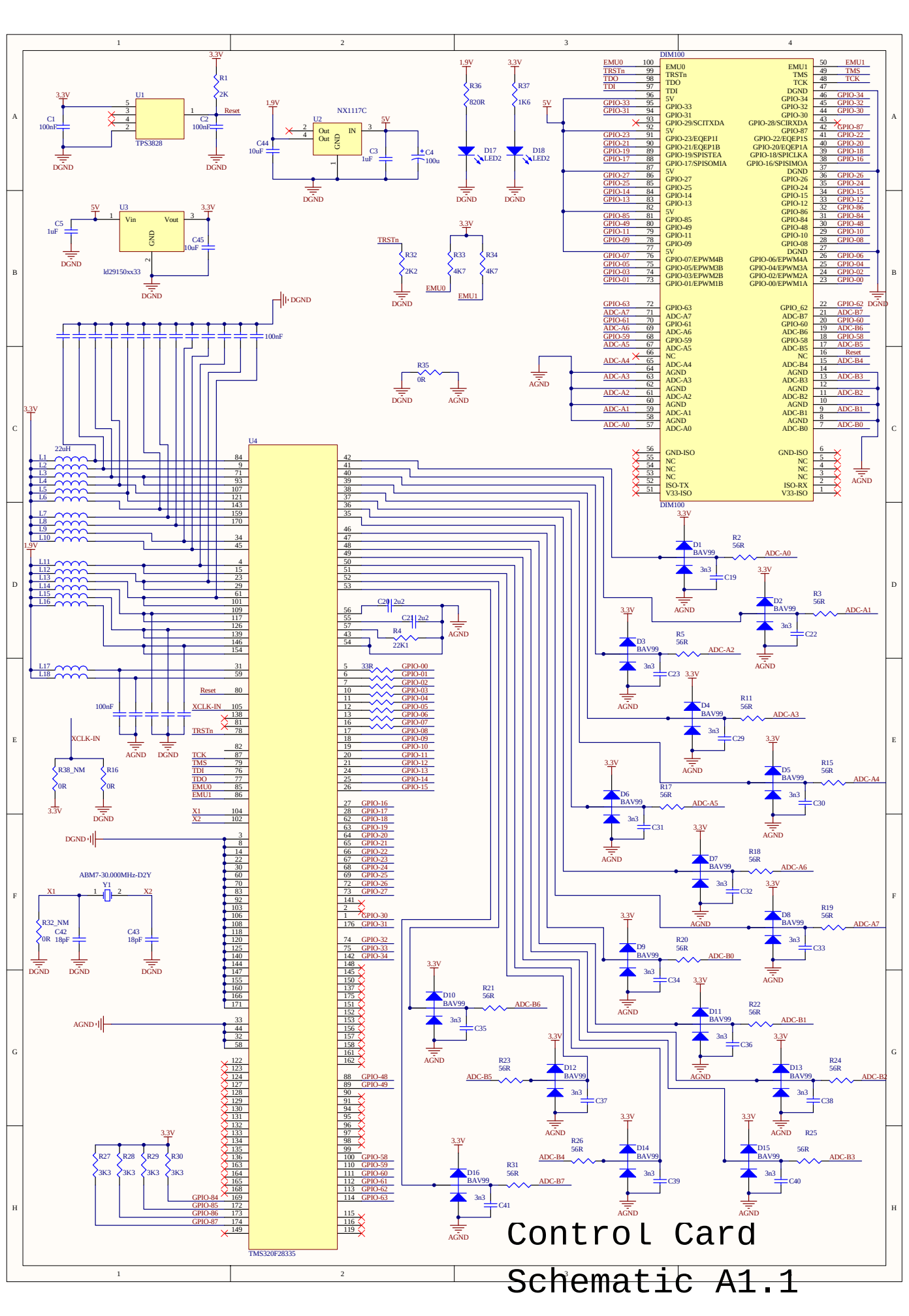
[41] D. Barater, G. Buticchi, E. Lorenzani, and C. Concari. Active common-mode filter for ground leakage current reduction in grid-connected pv converters operating with arbitrary power factor, 2013.

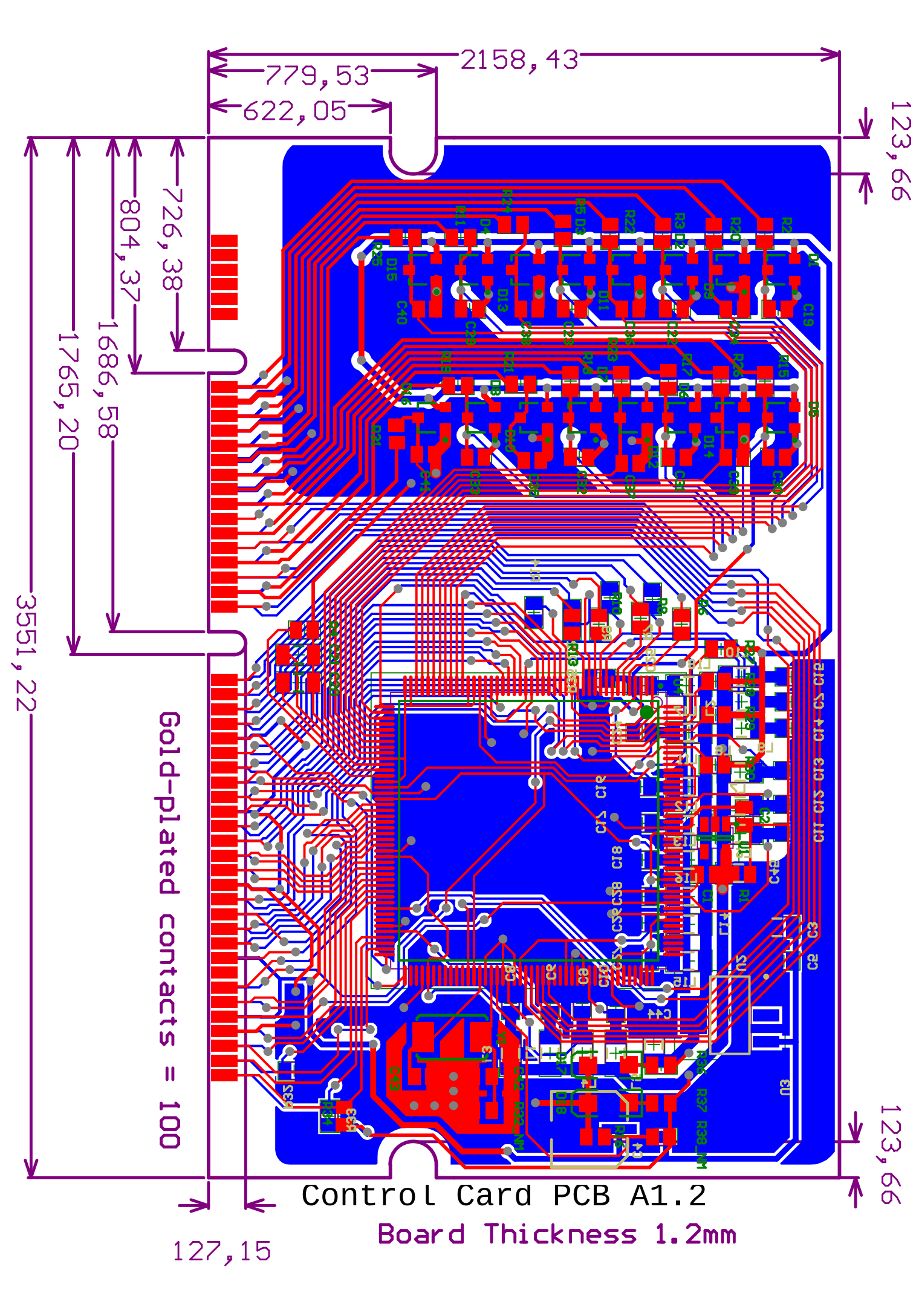
[42] M. Cacciato, A. Consoli, R. Attanasio, and F. Gennaro. Soft-switching converter with hf transformer for grid-connected photovoltaic systems. *IEEE Transactions on Industrial Electronics*, 57(5):1678–1686, 2010.

[43] G. Buticchi. Transformerless Grid-Connected Inverters for Photovoltaic Systems. In *Dottorato di Ricerca in Tecnologie dell'Informazione XXV Ciclo*, March 2013.

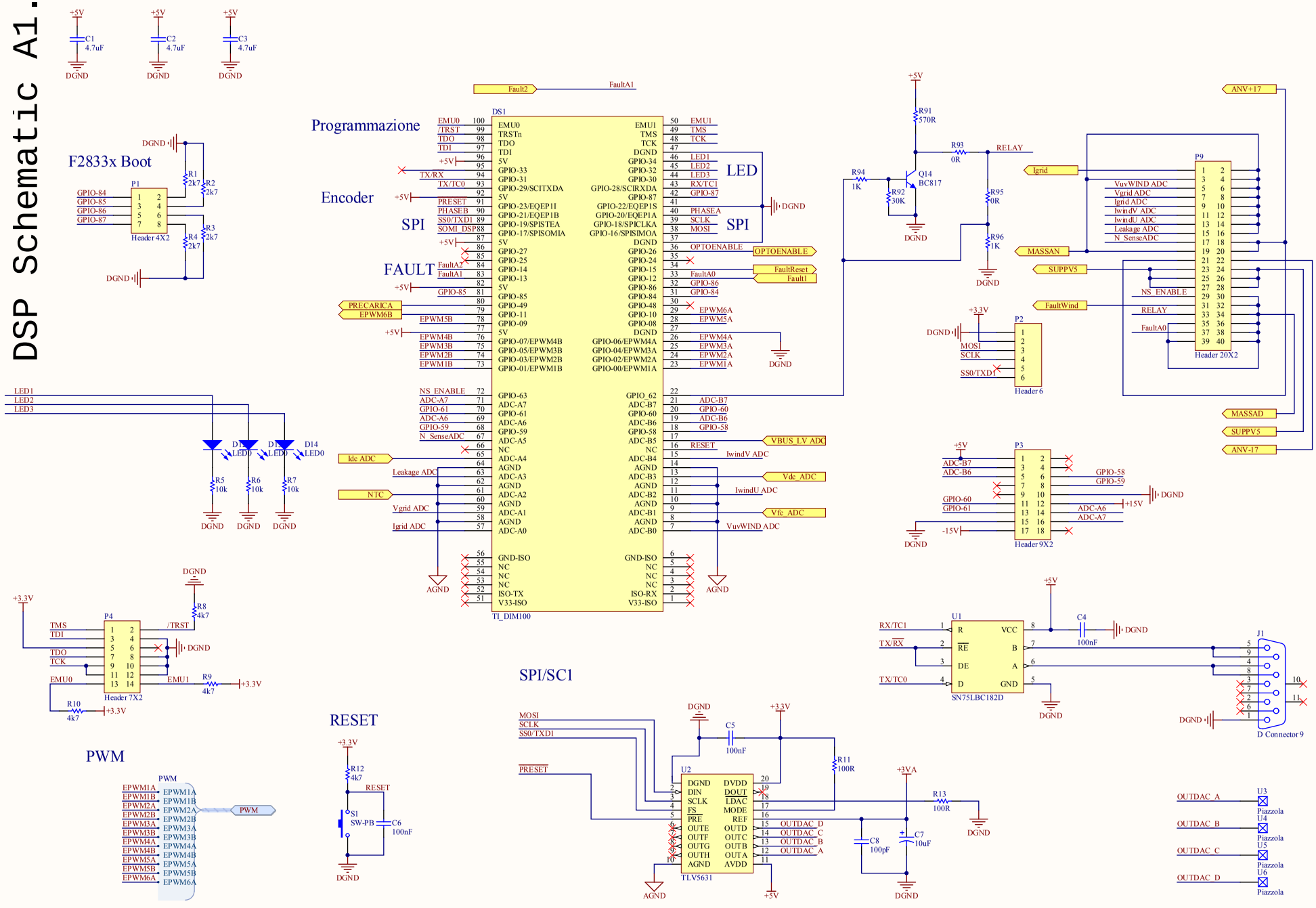
[44] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg. Control of single-stage single-phase PV inverter. In *European Conference on Power Electronics and Applications*, September 2005.

[45] M. Liserre, F. Blaabjerg, and S. Hansen. Design and control of an LCL-filter-based three-phase active rectifier. *IEEE Transactions on Industry Applications*, 41(5):1281 – 1291, September 2005.

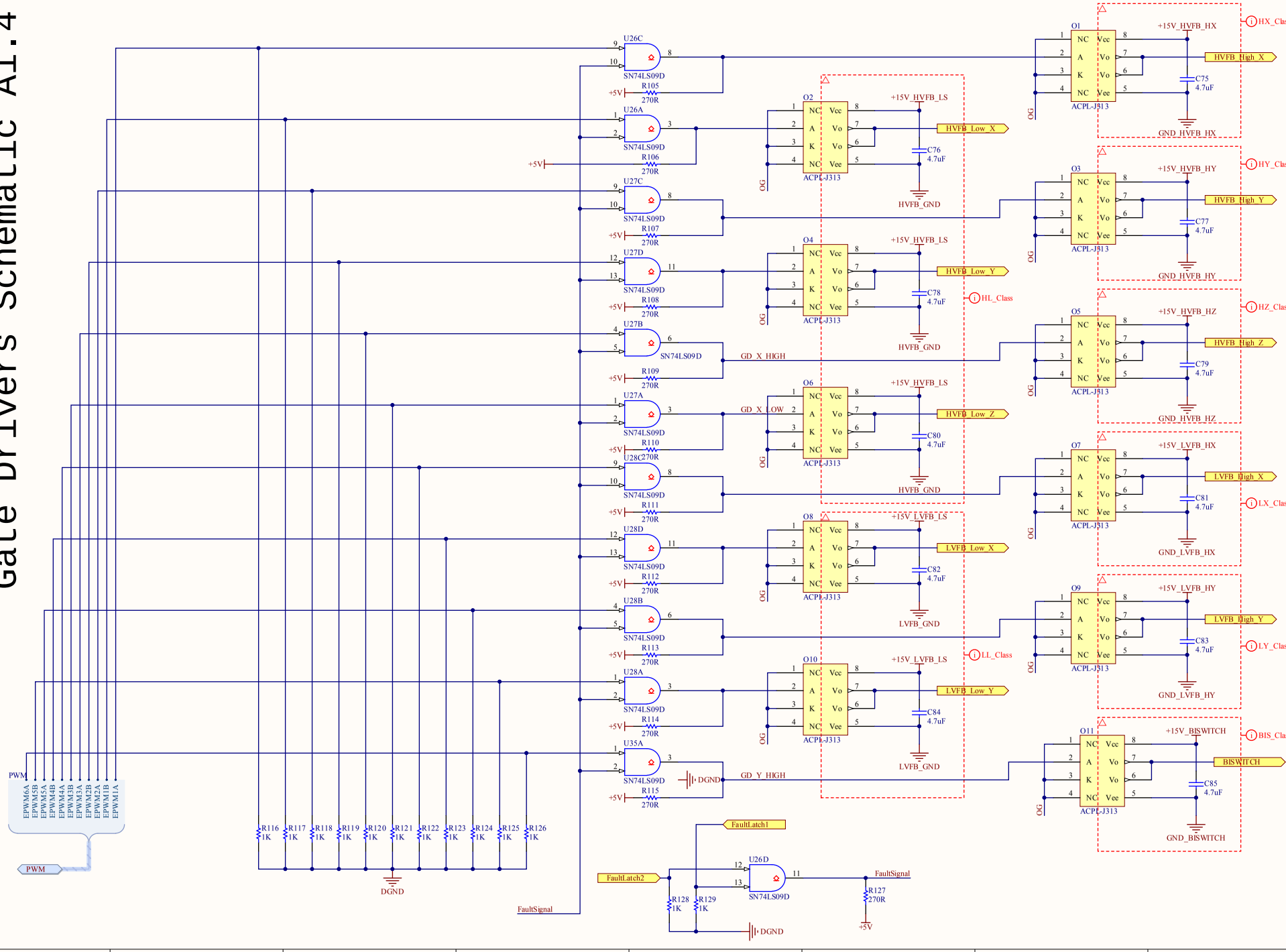

Control Card
Schematic A1.1

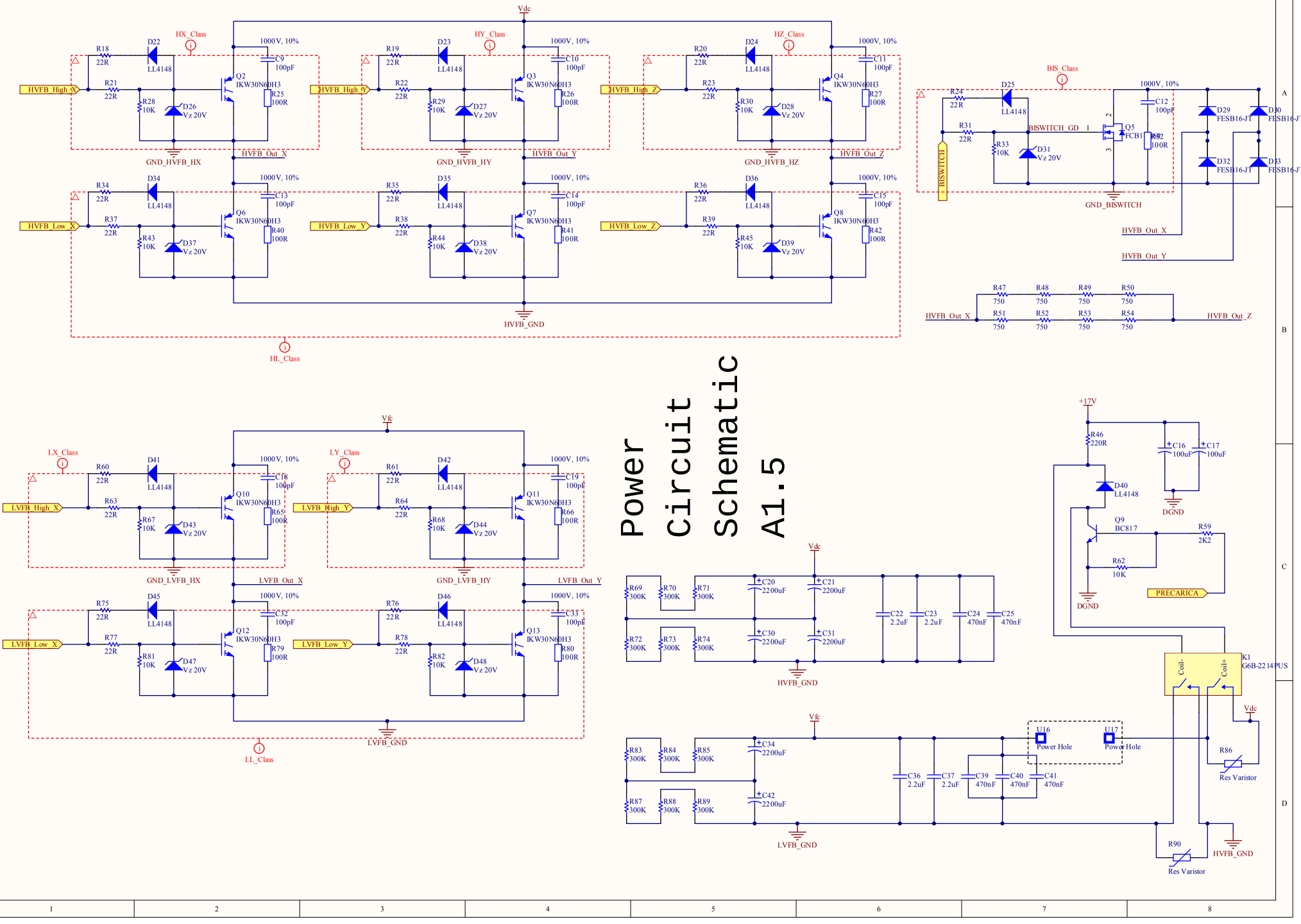

2158,43
779,53
622,05
123,66
804,37
726,38
1765,20
1686,58
3551,22
Gold-plated contacts = 100
123,66
Control Card PCB A1.2
Board Thickness 1.2mm
127,15

DSP Schematic A1.3

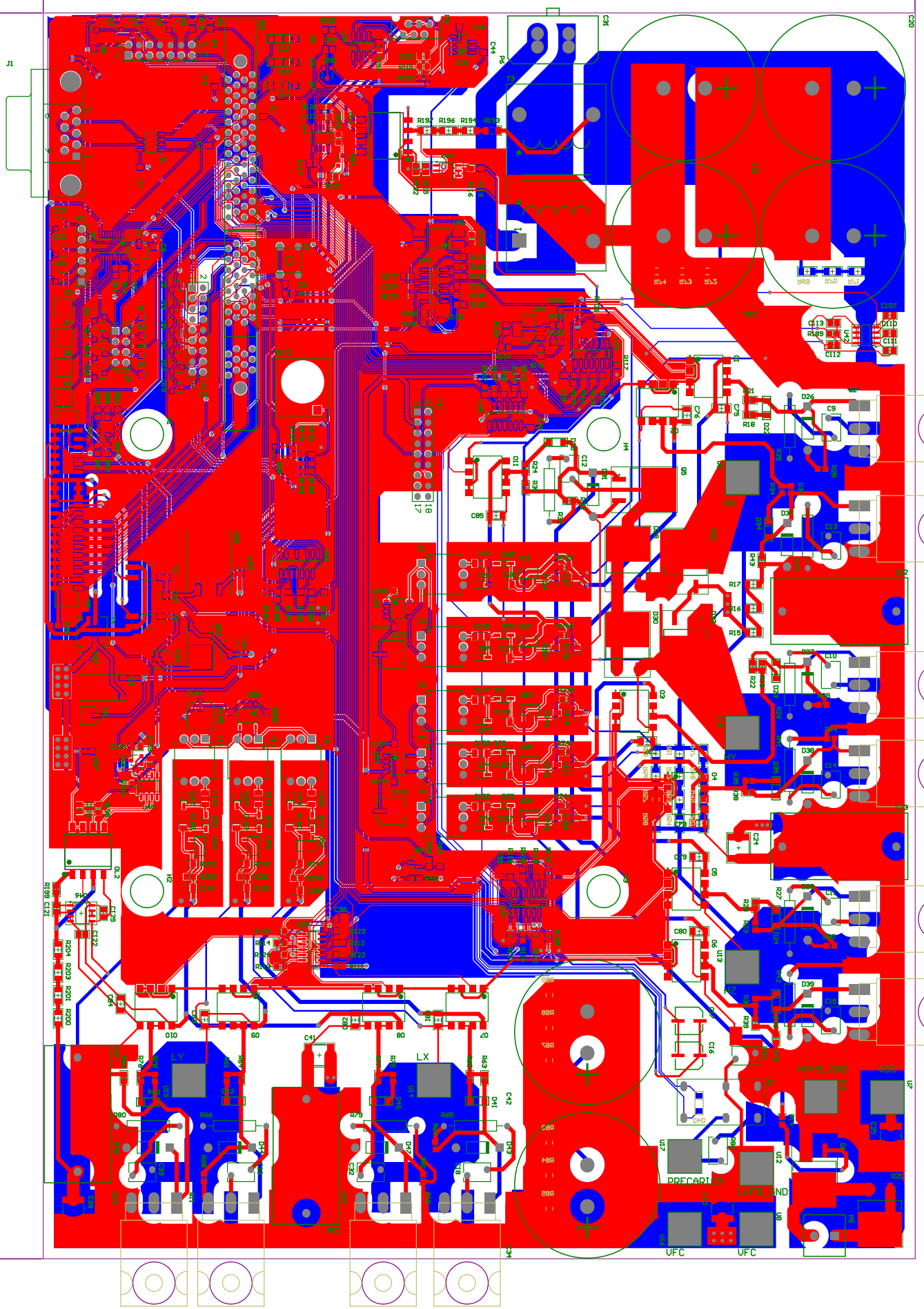


Gate Drivers Schematic A1.4

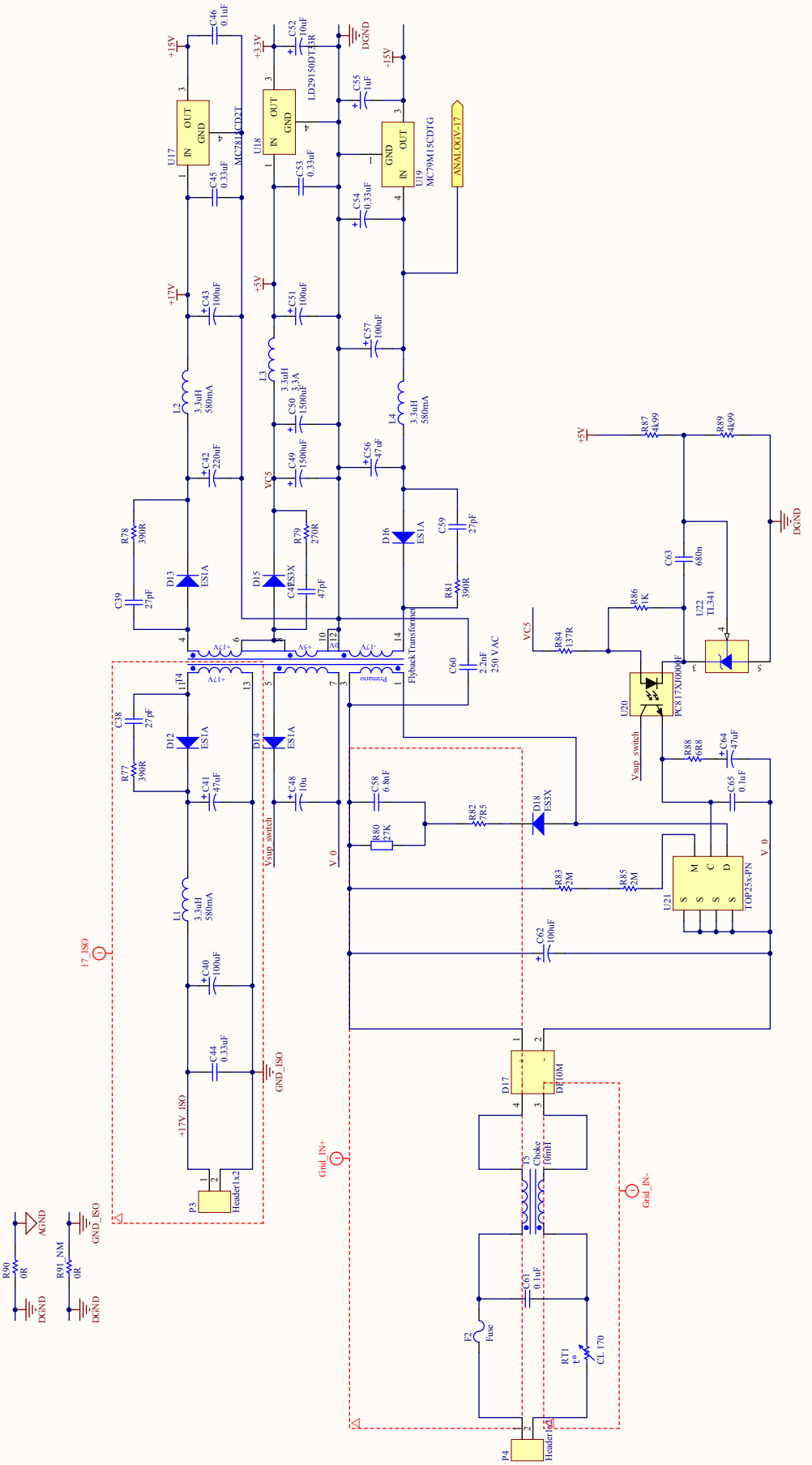


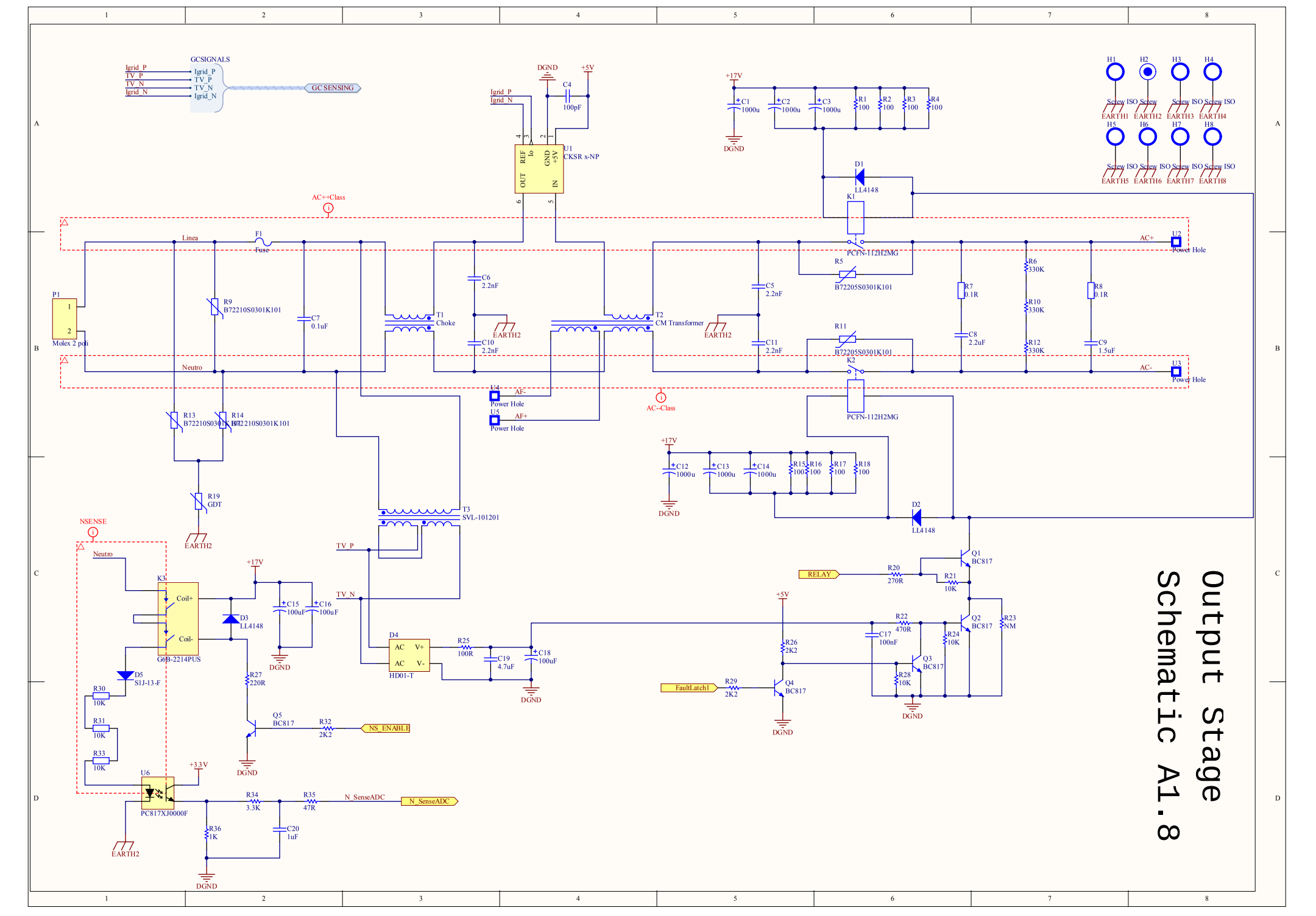

Power Circuit Schematic A1.5
Vdc
HX_Class
HY_Class
HZ_Class
HVFB_High_X
HVFB_High_Y
HVFB_High_Z
HVFB_Low_X
HVFB_Low_Y
HVFB_Low_Z
1000V, 10%
LL4148
IKW30N60H3
Vz 20V
GND_HVFB_HX
GND_HVFB_HY
GND_HVFB_HZ
HVFB_Out_X
HVFB_Out_Y
HVFB_Out_Z
HVFB_GND
HL_Class
BIS_Class
BISWITCH
BISWITCH_GD
FCB1
FESB16-JT
GND_BISWITCH
R47
R48
R49
R50
R51
R52
R53
R54
750
Vfc
LX_Class
LY_Class
LVFB_High_X
LVFB_High_Y
LVFB_Low_X
LVFB_Low_Y
GND_LVFB_HX
GND_LVFB_HY
LVFB_Out_X
LVFB_Out_Y
LVFB_GND
LL_Class
+17V
DGND
PRECARICA
BC817
2K2
K1
G6B-2214PUS
Coil-
Coil+
U16
U17
Power Hole
Res Varistor
R86
R90
HVFB_GND

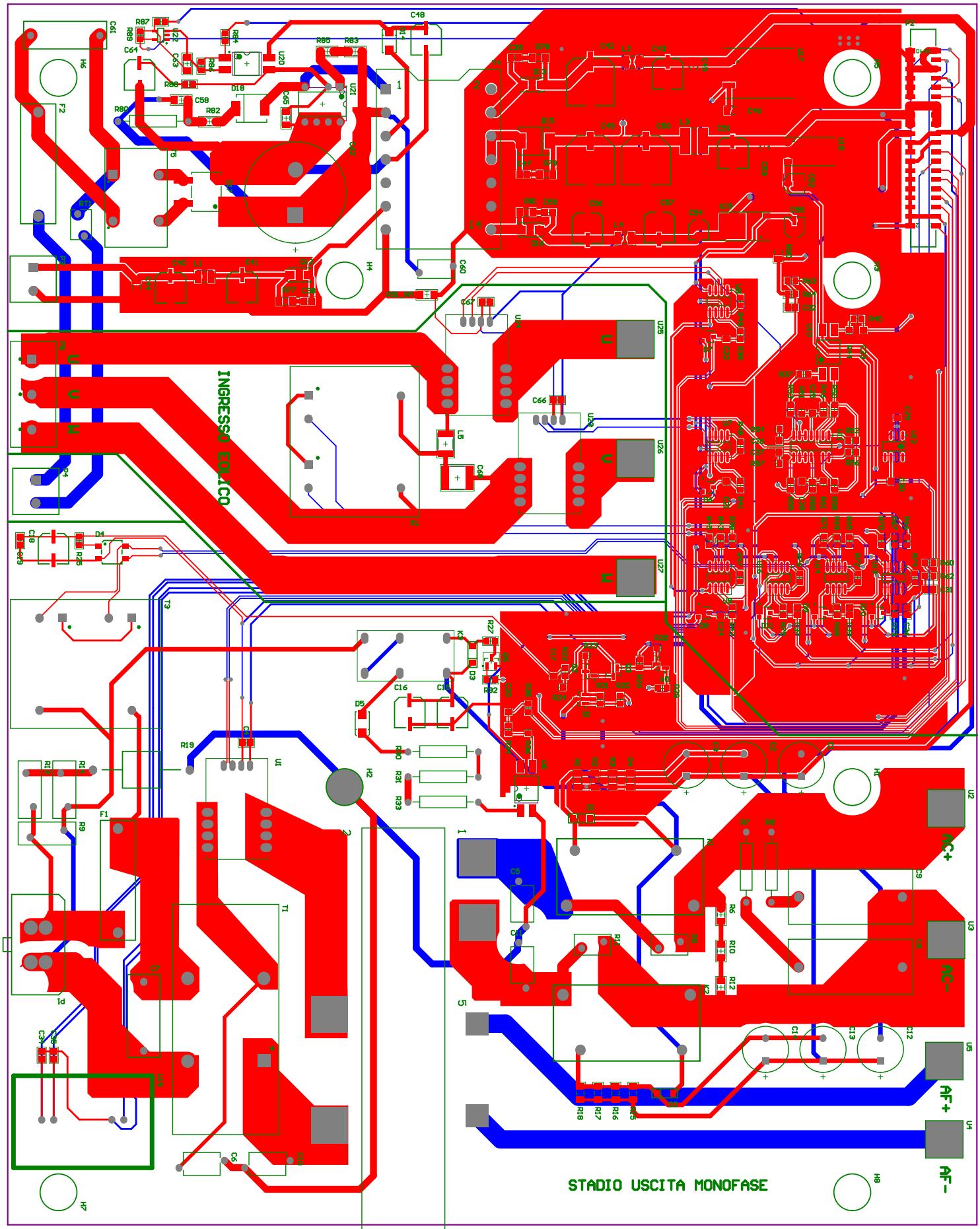
Power Card PCB A1.6



Flyback Schematic A1.7




GCSIGNALS
Igrid_P
TV_P
TV_N
Igrid_N
GC SENSING
DGND
+5V
C4
100pF
U1
CKSR x-NP
REF
Io
GND
+5V
OUT
IN
+17V
C1 1000u
C2 1000u
C3 1000u
R1 100
R2 100
R3 100
R4 100
DGND
H1 H2 H3 H4
Screw ISO
EARTH1 EARTH2 EARTH3 EARTH4
H5 H6 H7 H8
EARTH5 EARTH6 EARTH7 EARTH8
D1
LL4148
K1
PCFN-112H2MG
AC++Class
Linea
F1
Fuse
AC+
U2
Power Hole
R5
B72205S0301K101
R6 330K
R10 330K
R12 330K
R7 0.1R
R8 0.1R
C5 2.2nF
C8 2.2uF
C9 1.5uF
C11 2.2nF
P1
Molex 2 poli
R9
B72210S0301K101
C7 0.1uF
T1
Choke
C6 2.2nF
C10 2.2nF
EARTH2
T2
CM Transformer
R11
B72205S0301K101
Neutro
K2
PCFN-112H2MG
AC-
U3
Power Hole
U4
Power Hole
AF-
U5
Power Hole
AF+
AC--Class
R13
B72210S0301K101
R14
B72210S0301K101
R19
GDT
EARTH2
+17V
C12 1000u
C13 1000u
C14 1000u
R15 100
R16 100
R17 100
R18 100
DGND
D2
LL4148
T3
SVL-101201
NSENSE
Neutro
K3
Coil+
Coil-
G6B-2214PUS
+17V
C15 100uF
C16 100uF
D3
LL4148
DGND
TV_P
TV_N
D4
AC V+
AC V-
HD01-T
R25 100R
C19 4.7uF
C18 100uF
DGND
RELAY
R20 270R
R21 10K
Q1
BC817
+5V
R22 470R
Q2
BC817
R23 NM
C17 100nF
R24 10K
R26 2K2
Q3
BC817
R28 10K
DGND
FaultLatch1
R29 2K2
Q4
BC817
DGND
D5
S1J-13-F
R30 10K
R31 10K
R33 10K
R27 220R
Q5
BC817
R32 2K2
NS_ENABLE
DGND
U6
PC817XJ0000F
+3.3V
R34 3.3K
R35 47R
N_SenseADC
N_SenseADC
R36 1K
C20 1uF
EARTH2
DGND
Output Stage
Schematic A1.8



Output Stage PCB A1.9