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XXV Ciclo

TRANSFORMERLESS GRID-CONNECTED INVERTERS FOR PHOTOVOLTAIC SYSTEMS

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Alla mia famiglia

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Overview of Photovoltaic systems

1.1 Introduction

The increasing demand for electrical power, along with the decreasing stock of traditional energy sources, has caused a growing interest towards microgeneration from renewable power sources.

In particular, photovoltaic energy (PV) has witnessed an increasing attention and the scientific community has concentrated its efforts in order to develop innovative solutions for the integration of PV systems into the existing distribution grid.

PV systems can be mainly classified into two categories: stand-alone or grid-connected. The first topology is suited for remote locations where the PV panels power a local load, while grid-connected systems work in conjunction with the existing electrical grid.

Obviously, considering the highly discontinuous output of a PV field during a day, in a stand-alone system suitable electric energy storage must be provided. Moreover, when the accumulators are fully charged, no more power can be extracted from the panels. A grid-connected system does not suffer from these drawbacks, as the maximum power available from the field can be continuously transferred to the grid. Considering that the majority of the systems is of the grid-connected kind, a lot of research was done in this field. For this reason, this thesis is focused on grid-connected

converters for PV systems.

1.2 Grid-connected PV systems

The earlier designs of PV grid-connected inverters featured a full-bridge topology coupled to the mains with a line frequency transformer (Fig. 1.1a). The transformer guarantees the galvanic isolation between the PV field and the grid, simplifies the output filter design and the compliance with the electromagnetic interference (EMI) international regulations. However, converters embedding a line frequency transformer are bulky and the transformer accounts for 1-2% of the power losses.

For these reasons, researchers have been active in studying solutions for the removal of the line frequency transformer, in order to pursue the maximum efficiency without increasing the converter cost.

The main issue that arises when the line frequency transformer is removed is due to the presence of a parasitic capacitance between the metal frame of the panel and the photovoltaic cells. The value of the capacitance varies with the ambient conditions and with the panel technology. The typical value can range from 100 nF/kWp for crystalline silicon to 1 μF/kWp for thin-film panels. This implies that a common mode current (i.e., ground leakage current) can flow into the resonant circuit composed of the line conductors, the earth connection of the MV/LV distribution transformer and the parasitic capacitance of the PV field [1].

If a simple full-bridge is employed without any transformer coupling or specific modulation strategy, the high-frequency common mode voltage variations at the converter output cause unacceptable levels of ground leakage current, that generate EMI, reduce the safety of the system and cause the disconnection of the converter due to the Residual Current Device (RCD) [2].

In order to solve the problem, two approaches were pursued: the transformerless (Fig. 1.1b) converter and the high-frequency transformer (Fig. 1.2) converter. In the latter kind of topology, a high-frequency transformer is employed to transfer the power from the PV panels to a DC/AC converter. Different choices for the converter are possible: in [3] a soft-switching DC/DC converter feeds a full-bridge VSI and in

[4] a resonant DC/DC converter is followed by a current source inverter.

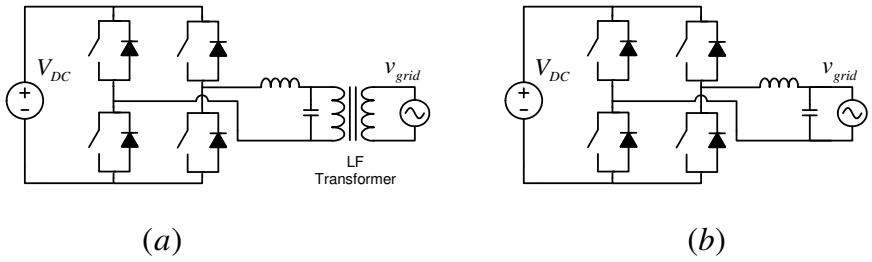


Figure 1.1: Line-frequency transformer (a) and transformerless (b) inverter.

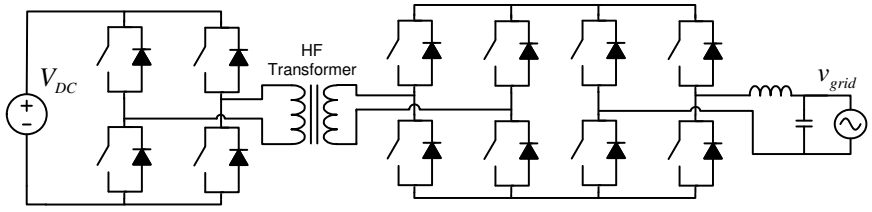


Figure 1.2: High-frequency transformer inverter architecture [3].

While the high-frequency transformer converter still guarantees the galvanic isolation and is suitable for every kind of PV source, even for those panels that require the grounding of the positive or the negative terminal, the transformerless approach does not feature any transformer nor the galvanic isolation.

Transformerless inverters are usually designed for a precise panel technology. For crystal and polycrystalline silicon, the main issue is the common mode voltage variations at the converter output. In any case, for thin-film photovoltaic panels, it is almost mandatory to employ insulated topologies, due to specific requirement of the panel technology. In the following chapters several solutions are presented and analyzed.

1.3 Control of a grid-connected Photovoltaic Inverter

A grid-connected converter is a complex system and the power electronics topology represents only the front-end with the electrical grid. In order to effectively harvest the energy from the PV field and transfer it to the grid, a specific control system must be implemented.

The comprehensive control system is reported in Fig. 1.3 and each component of the subsystem will be analyzed in the following section.

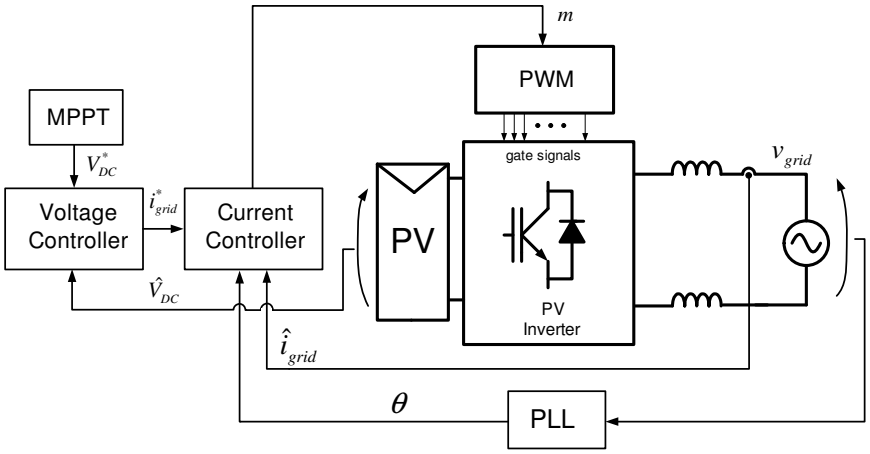


Figure 1.3: Block scheme of the control of a single-stage PV inverter.

1.3.1 Grid synchronization

The main task to be performed by a grid-connected PV inverter is to inject active power into the grid. In order to complete this task, a synchronization mechanism must be implemented. While the simple strategy of measuring the time between consecutive zero-crossings of the grid voltage may be theoretically sufficient, more complex solutions must be employed to comply with the international regulations.

PLL in a stationary reference frame

The first approach to detect the grid voltage angle is to employ a simple Phase Locked Loop (PLL), presented in the scheme of Fig. 1.4. The basic principle is that the difference between the input and output angle can be estimated by the multiplication and subsequent filtering of two sinusoidal signals. Considering $v_{grid} = V_g \sin\theta_i$, it follows that the input of the Low Pass Filter (LPF) is $V_g \sin\theta_i \cos\theta$, that equals to $0.5V_g\,(sin(\theta_i - \theta) + \sin(\theta_i + \theta))$ by applying the Werner formulas.

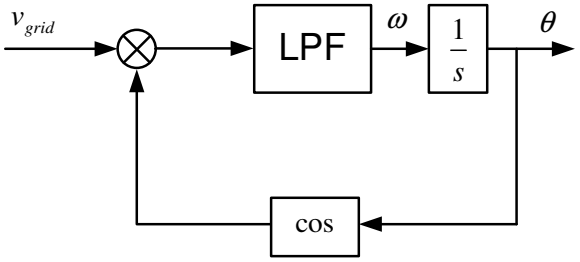


Figure 1.4: Block scheme of the PLL in stationary reference frame.

As a matter of fact $\sin(\theta_i - \theta)$ can be linearized as $\theta_i - \theta$, and the integrator followed by the trigonometric function can be considered the model of a Voltage Controlled Oscillator (VCO), leading back to the scheme of the well-known PLL.

The main drawback of this topology is the design of the LPF in order to achieve good tracking performance. In fact, a first order LPF would lead to a marked phase error, for this reason different structures of PLL are chosen.

Transport delay PLL

In a three-phase system, the use of the Clarke transformation allows to create a quadrature system and realize the PLL in a synchronous reference frame (d-q PLL) with the Park transformation. This kind of PLL is very simple to design, allows zero steady state tracking error and very good dynamic performances. However, its application to a single phase system is not straightforward. While it is true that a fictitious quadrature signal can be generated by delaying the grid voltage by a quarter of period,

this remains true only for a specific frequency, i.e., in case of frequency deviations a tracking error appears.

This drawback was solved in [5], where a modified Park transform was employed. Basically, the trigonometric functions of the Park transforms are not computed directly, but the cosine is obtained as a delayed version of the computed sine of the angle, see Fig. 1.5. T_n represents the nominal value of the grid voltage period.

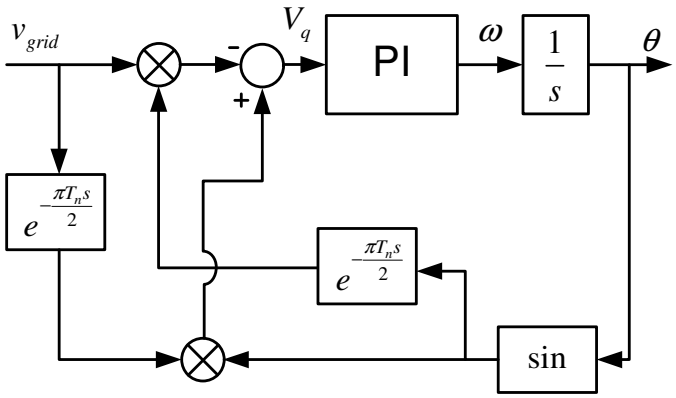


Figure 1.5: Block scheme of the transport delay PLL.

Considering the grid voltage $v_{grid} = V_g \sin\theta_i$, with $\theta_i = \omega_i t + \Phi_0$ the input of the PI regulator can be written as:

$$\begin{aligned} V_q &= -V_g \sin\theta_i \sin(\theta - \omega_i T_n/4) + V_g \sin\theta \sin(\theta_i - \omega_i T_n/4) \\ &= V_g \sin(\omega_i T_n/4)\,(\sin\theta_i \cos\theta - \sin\theta \cos\theta_i) \\ &= V_g \sin(\omega_i T_n/4) \sin(\theta_i - \theta) \end{aligned} \tag{1.1}$$

Equation (1.1) shows that even if $\omega_i T_n/4 \neq \pi/2$, i.e., the grid frequency varies, the phase error is compensated. Obviously, the presence of a delay line limits the dynamic performances. Moreover, it can be shown that this structures presents two points of stability, the one where $\theta = \theta_i$ and the one where $\theta = -\theta_i$.

This fact must be taken into account and the sign of the grid pulsation must be checked to ensure that the PLL is locked on the stable point with $\omega > 0$.

SOGI-FLL

A possible solution to employ a standard d-q PLL in a single phase grid was presented in [6]. The basic idea is to realize a system able to generate the quadrature version of a given input signal while tracking the frequency.

The core of the system is the Second Order Generalized Integrator (SOGI), that is a second order transfer function with a resonance peak tuned to a specific frequency. The block scheme is presented in Fig. 1.6.

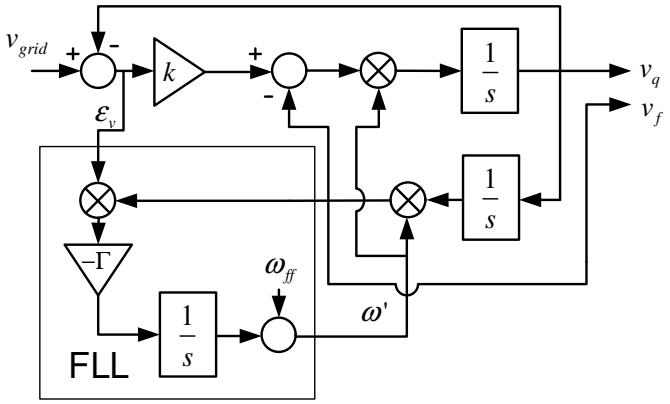


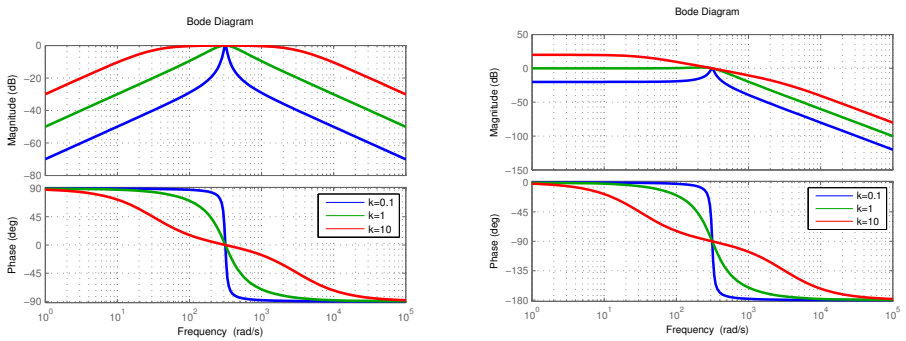
Figure 1.6: Block scheme of the SOGI-FLL.

Neglecting the Frequency-Locked-Loop (FLL) and considering a fixed ω', the transfer function between the outputs v_f, v_q and the input v_{grid} can be expressed as:

$$\begin{cases} D(s) = \frac{v_f(s)}{v_{grid}(s)} = \frac{k\omega' s}{s^2+2k\omega' s+\omega'^2} \\ Q(s) = \frac{v_q(s)}{v_{grid}(s)} = \frac{k\omega'^2}{s^2+2k\omega' s+\omega'^2} \end{cases} \tag{1.2}$$

As it can be seen from the transfer functions (Fig. 1.7), v_f represents a filtered version of the input signal, while v_q lags the input signal by $\pi/2$. The value ω' represents the resonance frequency, while the bandwidth of the filter is determined by the value k.

The Frequency Locked Loop (FLL) dynamically tunes the resonance frequency ω' of the SOGI. The mechanism resides in the transfer functions $\varepsilon_v(s)/v_{grid}(s)$ and



(a) $D(s)$ (b) $Q(s)$

Figure 1.7: Frequency response of the SOGI filters.

$Q(s)$. It can be shown from the magnitude and phase responses that these two latter signals are in phase only when ω' matches the input frequency. For this reason, a simple integrative controller of gain $-\Gamma$ is used to track the frequency.

This topology implies an increase in the computational load, as a d-q PLL must be cascaded to the SOGI in order to reconstruct the grid voltage angle. Moreover, the bandwidth of the system can not be selected too narrow, as it would delay the dynamic response.

1.3.2 Control of the current injected into the grid

Independently from the hardware architecture, a VSI can synthesize a fundamental output voltage by high frequency switching. In order to reduce the switching harmonics, an output filter must be employed. The design of the output filter for grid-connected inverters is well studied in literature [7].

While an inductive (L) filter represent a simple solution, usually it cannot achieve satisfying performance in term of harmonic reduction unless a large inductance value is chosen. For this reason a LC or LCL filter is generally employed.

Fig. 1.8 represents the model of the VSI (with output voltage V_{out}) coupled to the grid with a LCL filter. The inductor L_{grid} represents the lumped inductance of the grid for a LC filter, but it could also include the inductance of the additional inductor

in case of a LCL filter. In the model also the wire resistances and the ESR of the filter capacitor are considered. It must be said that R_f could also represent an actual resistor connected in series with the capacitor to dampen the resonance.

For the control, the grid voltage v_{grid} represents a disturbance, while the value v_{PCC} represents the actual voltage at the Point of Common Coupling (PCC), where the VSI is connected.

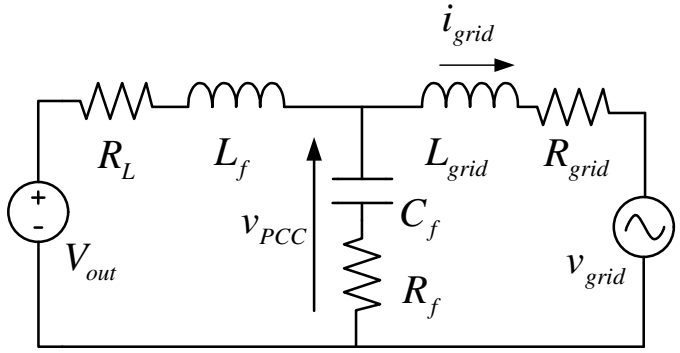


Figure 1.8: Model of the grid-connected converter with a LC filter.

Depending on the rated power of the converter different filter parameters are chosen in order to comply with the regulations that limit the THD of the output current. The Bode response of the plant is shown in Fig. 1.9. The parameters were $C_f = 1\mu F$, $R_f = 1\Omega$, $L_f = 1mH$, $R_l = 0.1\Omega$, $R_g = 0.25\Omega$ and $L_f = [20, 1000]\mu H$. A wide variation of the grid impedance is considered, as this value is affected by a great variability.

The transfer function $Y(s) = i_{grid}(s)/V_{out}(s)$ can be expressed as:

$$Y(s) = \frac{sC_fR_f+1}{C_fL_fL_gs^3+C_f\left(L_fR_f+L_fR_g+L_gR_f+L_gR_L\right)s^2+\left(L_f+L_g+C_f\left(R_fR_g+R_fR_L+R_gR_L\right)\right)s+R_g+R_L} \tag{1.3}$$

This transfer function presents a marked resonance peak at $\omega_{res} = \sqrt{\frac{L_f+L_{grid}}{C_fL_fL_{grid}}}$. The design of the LCL filter usually starts by choosing the value of the filter inductor L_f in order to fulfill a first requirement for the output current ripple. The capacitor value is limited by the amount of reactive power that it absorbs, and it is used to further

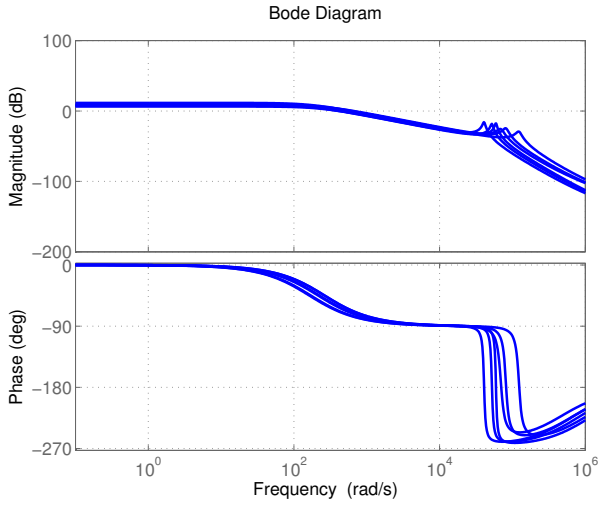


Figure 1.9: Bode response of the Plant with different values of the parameters.

reduce the current ripple. The resonance peak should be located between the grid frequency and half the sampling frequency. While it is true that the damping resistor R_f can be adopted to prevent the instability of the closed-loop system, a large value increases the power losses.

Several solutions for grid current controllers are analyzed [8].

Proportional Integral (PI)

A simple solution is to employ a standard PI regulator, in the form:

$$G_{PI}(s) = K_P + \frac{K_I}{s} \tag{1.4}$$

The main issue of this current regulator is the finite gain at the grid frequency. In fact, the use of a simple PI regulator cannot guarantee a good tracking of the reference signal. As a consequence, errors in the grid current magnitude and phase will appear. This problem can be reduced by increasing the gain of the regulator, obviously reducing the control phase margin and rendering the system potentially

unstable.

Proportional Resonant (PR)

The steady state error at the grid frequency of the simple PI regulator is a serious issue, as also the power factor of the output current cannot be controlled with precision.

The Proportional Resonant (PR) controller can overcome this problem, by designing a second order controller with infinite gain at the grid frequency, as in (1.5). In an actual implementation, some degree of damping must be introduced in the system. This damping factor, k, regulates the gain of the resonant filter, as shown in Fig. 1.10.

$$G_{PR}(s) = K_I \frac{\omega_{grid}^2}{s^2 + \omega_{grid}^2} \simeq K_I \frac{\omega_{grid}^2}{s^2 + 2k\omega_{grid}s + \omega_{grid}^2} \tag{1.5}$$

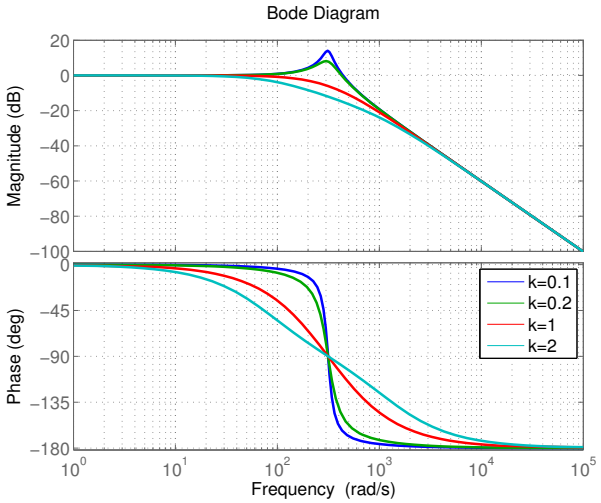


Figure 1.10: Bode response of the PR controller with different damping factors.

The steady state performance of this controller depends on the choice of the damping factor, that cannot be chosen too low in order to avoid system instability.

Despite this problem, this controller is widely adopted when harmonic compensation is needed, as multiple PR controllers tuned to the fundamental harmonics can be added together.

In the field of resonant controllers, the repetitive control was also considered for actual implementations in grid-connected VSI [9]. The repetitive controller can be viewed as positive feedback system with a delay line, that leads to the expression:

$$G_{rep}(s) = \frac{K_{rep}}{1 - e^{-T_n s}} \tag{1.6}$$

This controller shows infinite gain at the frequency $1/(T_n)$, i.e., the nominal grid frequency, and its harmonics. Obviously, a specific compensator must be designed in order to ensure the system stability.

PI in synchronous reference frame

In a three phase system the synchronous current control in the d-q reference frame is widely adopted. However, its application to a single phase system needs the generation of a fictitious quadrature system, as already explained in section 1.3.1.

Fig. 1.11 shows a possible implementation of the d-q grid current control. A delay block is employed to generate the quadrature current signal, and a simple PI for each axis is employed. Obviously, only one output of the Park inverse transform is chosen as output voltage V_{out}. Depending on the convention chosen for the PLL, the active power axis can be either the direct or the quadrature one.

This controller exhibits excellent steady state performance and possibility to control active or reactive power. However, the presence of a delay line negatively affects its dynamic performance.

Deadbeat controller

The deadbeat controller is a model-based discrete control which aims at obtaining zero steady state error in a finite number of sampling intervals.

The basic idea is to write the difference equation that governs the system's dynamics, and to calculate the exact value of the controlled variable which allows to

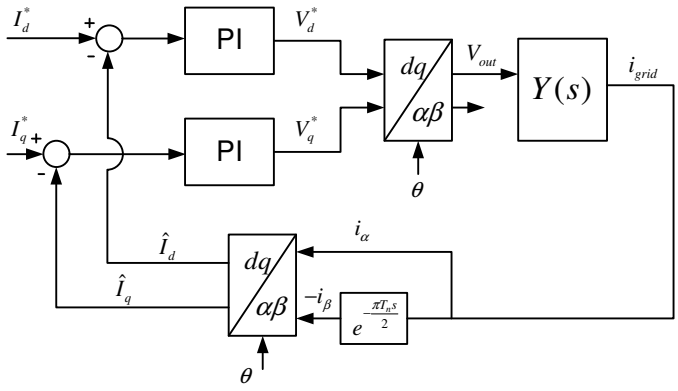


Figure 1.11: Block scheme of the d-q current control for a single phase VSI.

reach the given set-point.

For example, considering the system in Fig. 1.8, the equations that characterize the system are:

$$\begin{cases} R_L i_{L_f} + L_f \frac{di_{L_f}}{dt} &= V_{out} - v_{PCC} \\ v_{PCC} &= v_{C_f} + R_f C_f \frac{dv_{C_f}}{dt} \\ i_{grid} &= i_{L_f} - C_f \frac{dv_{C_f}}{dt} \end{cases} \tag{1.7}$$

The simplest form of the deadbeat control is to control the filter inductor current i_{L_f}, considering only the first equation. In this case discretizing the derivative with a sampling time T_s the following equation can be obtained:

$$R_L i_{L_f}[k] + L_f \frac{i_{L_f}[k+1] - i_{L_f}[k]}{T_s} = V_{out}[k] - v_{PCC}[k] \tag{1.8}$$

This means that, in order to control the inductor current so that $i_{L_f}[k+1] = i^*[k+1]$, where $i^*[k+1]$ is the current set-point at the sampling instant $k+1$, the inverter needs to output the voltage:

$$V_{out}[k] = v_{PCC}[k] + R_L i_{L_f}[k] + L_f \frac{i^*[k+1] - i_{L_f}[k]}{T_s} \tag{1.9}$$

From (1.9) the control needs to know the desired current one sample time ahead: $i^*[k+1]$.

However, the control is complicated by the fact that a PWM inverter operates intrinsically with a time delay of one step, so it is not possible to control the inductor current at the next sample time. An additional sampling interval is needed to take into account this delay and all the variables at the next sampling interval must be predicted.

In fact, $V_{out}[k]$ at the instant k was decided at the previous step, so the control must calculate the value $V_{out}[k+1]$, that can be obtained shifting into the future equation (1.9). The same equation can be employed to predict $i_{L_f}[k+1]$.

The final form of the deadbeat controller, including the delay in the PWM inverter is given by (1.10)

$$\begin{cases} i_{L_f}[k+1] &= \frac{T_s}{L_f}\left(V_{out}[k] - v_{PCC}[k] - R_L i_{L_f}[k]\right) + i_{L_f}[k] \\ V_{out}[k+1] &= v_{PCC}[k+1] + R_L i_{L_f}[k+1] + L_f \frac{i^*[k+2] - i_{L_f}[k+1]}{T_s} \end{cases} \tag{1.10}$$

To implement the control in (1.10) it is necessary to predict the values $v_{PCC}[k+1]$ and $i^*[k+2]$. Different approaches are feasible, i.e. circular buffers to predict periodic signals or data interpolations. The way the predictions are calculated affects in a marked way the performance of the control [10].

Moreover, the deadbeat control needs a good knowledge of the system model, and errors in the system parameters affect the set-point tracking and can also lead to the instability of the control.

Robust control

The robust control theory is applied in order to guarantee the stability of feedback controls with uncertain systems.

As a matter of fact, as shown in Fig. 1.9, the current control is affected by a certain amount of uncertainty, so the robust control theory appears to be an attractive solution. In [11] a robust controller for a grid-connected inverter with a LCL filter was designed with the Robust Control Toolbox of MATLAB.

The first step to design a robust controller is to model the uncertainty of the system, modeling the system as an average model with a multiplicative uncertainty , i.e. (1.11).

$$Y(s) = \overline{Y}(s)\,(1+\Delta(s)) \tag{1.11}$$

In fact, several controllers can be designed for a reference plant, but in order for the system to be stable with respect to parameters variation, specific characteristics of the controller must be considered.

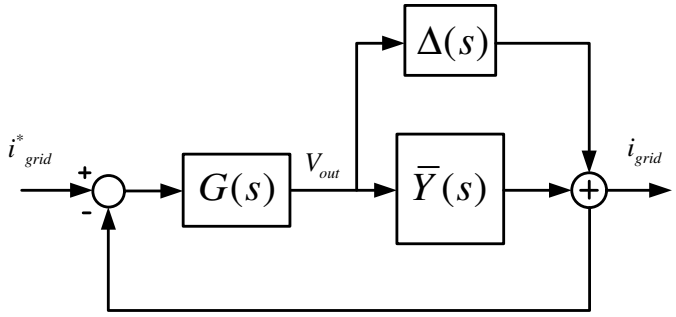


Figure 1.12: Scheme of the controller with the system affected by multiplicative uncertainty.

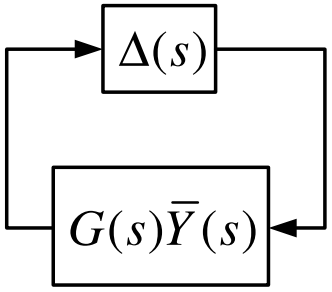


Figure 1.13: Autonomous system employed to study the asymptotic stability.

Considering 1.12, the stability problem can be assessed considering the autonomous system (with null setpoint) of 1.13. The **Small gain theorem** states that: *If* $G(s)\overline{Y}(s)$

and $\Delta(s)$ are stable, system of 1.13 is asymptotically stable if:

$$\| G\overline{Y}\Delta \| < 1 \tag{1.12}$$

That is equivalent to say:

$$\overline{\sigma}\left(G(j\omega)\overline{Y}(j\omega)\Delta(j\omega)\right) < 1 \tag{1.13}$$

where $\overline{\sigma}$ represents the singular value for a multivariable transfer function. In the case of Single-Input Single-Output system the singular value is equivalent to the maximum absolute value of the transfer function over the frequency range.

It follows that the robust stability is guaranteed if

$$\overline{\sigma}\left(G(j\omega)\overline{Y}(j\omega)\right) < \frac{1}{\Delta(j\omega)} \tag{1.14}$$

In other words, the maximum amount of uncertainty of the system limits the maximum gain (therefore the performance) of the feedback system. Usually it is important to shape the robust controller in order to guarantee specific characteristic, i.e. high gain in the frequency range of interest. In fact, the transfer function can incorporate specific weighing filters.

For this reason a mixed sensitivity problem is generally formulated and controllers with fairly good characteristics can be designed [11].

The main drawback of this kind of design is that too wide variations of the parameters compromise excessively the performance of the designed controller.

1.3.3 Maximum Power Point Tracking

The current control represents the basic functionality of the grid-connected inverter. In fact, depending on the system architecture, one or more control loops are needed in order to achieve the full functionality.

In particular, for a single-stage DC/AC inverter, the DC Link is directly connected to the photovoltaic field, and it is mandatory to control the DC Link voltage.

The control of the DC Link voltage can be realized controlling the current injected into the grid. The DC Link voltage then follows the well-known characteristic of the

photovoltaic cell, that can be derived by the equivalent circuit of a PV cell (Fig. 1.14), where the voltage-current characteristic can be expressed, for silicon PV cells, as:

$$I = I_{pv} - I_0 \left(e^{\frac{q(V+R_s I)}{nkT}} - 1 \right) \tag{1.15}$$

In equation (1.15), I_{pv} represents the current due to the photoelectric effect (variable with the solar irradiance), the diode D models the p-n junction and R_p and R_s the parallel and series resistance of the cell. The current drained by the parasitic resistance was neglected.

The series-parallel connection of multiple PV cells leads to a PV module, and the PV system installers design the connection of multiple PV panels in order to match the requirement of the grid-connected inverter.

For example, Fig. 1.15 represents a typical voltage-current characteristic of a 3.8 kW PV field.

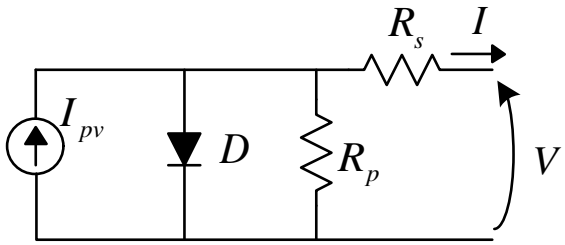


Figure 1.14: Equivalent circuit of a PV cell.

In order to maximize the energy harvested from the PV field, it is important that the inverter makes the PV field to work at its maximum power point. Fig. 1.16 shows the voltage-power characteristic of the PV field described by Fig. 1.15. It is obvious that the operating point V=400 V corresponds to the maximum available power in these operating conditions.

So, the comprehensive control of a PV inverter must implement, in addition to the basic current controller, also a DC Link controller, whose set-point is generated by a specific algorithm that tries to track the MPP in every working condition. This was depicted in Fig. 1.3.

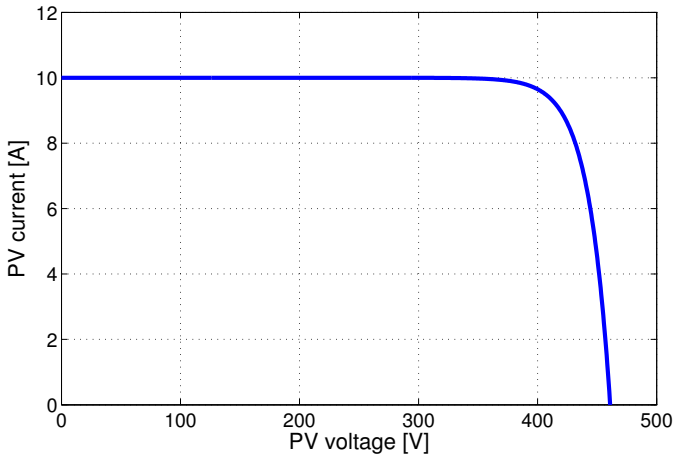


Figure 1.15: Voltage-Current characteristic of a PV field.

The situation is complicated by the fact that the solar irradiance is always varying, due to the variable weather conditions or partial shading of the PV field.

In order to work in the optimum point, a Maximum Power Point Tracking (MPPT) [12], [13] algorithm must be implemented in the inverter.

In the following some MPPT algorithms are shown, a review of the different MPPT techniques can be found in [14].

Off-line MPPT methods

These methods rely on the off-line calculation of the optimum control law. Generally, they can achieve good dynamic performance in terms of system response, but they rely on the good knowledge of the system parameters and usually do not take into account the cases where multiple local maxima are present in the PV characteristic (typically during partial shading of the PV field).

The **Curve Fitting Method** is based on the observation that the maximum power points at different irradiance conditions can be calculated (or mapped) in order to obtain an optimum curve which links the PV voltage and the power that must be drawn from the field.

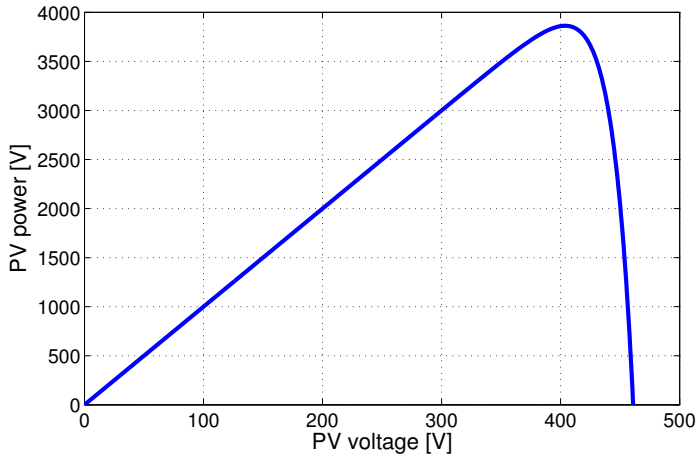


Figure 1.16: Voltage-Power characteristic of a PV field.

The **Fractional Short Circuit Current/Fractional Open Circuit Voltage** method relies on the fact that the MPP current or voltage follows in first approximation a linear law. By measuring at different time instants the open circuit voltage or short circuit current the MPP law can be updated.

On-line MPPT methods

These algorithms search for the optimum operating point continuously and they do not rely only on precalculated characteristics.

The **Perturb and Observe (P&O)** algorithm is one of the most employed due to the ease of implementation and the fact that it requires very little tuning. It is based on the continuous perturbation of the system operating point in the attempt to move the system towards the increasing power. In steady-state conditions, the algorithm oscillates around the maximum power point, inverting the sign of the perturbation at every sampling interval. This behavior also represents the main drawback of this method, as in order to achieve good MPP tracking the perturbation must be sufficiently high, but the higher the perturbation, the higher the oscillation around the MPP at steady state, and consequently the lower the MPP tracking efficiency.

In order to solve the drawback of the P&O method various approaches where investigated, where basically the magnitude of the perturbation is adapted in order to obtain good tracking performance with little steady-state oscillation.

Chapter 2

State of the art of transformerless PV Inverters

2.1 Transformerless Full-Bridge topologies

In this section the full-bridge solutions that address the problem of high-frequency common mode voltage variations are analyzed.

Fig. 2.1 shows a full-bridge converter powered by a PV source. Assuming the negative side of the DC Link as the reference potential, v_{A0} and v_{B0} can be defined as the outputs of the full-bridge. The common mode voltage can be expressed as (2.1), while the differential voltage is the difference between the two potentials (2.2).

$$v_{cm} = \frac{v_{A0} + v_{B0}}{2} \tag{2.1}$$

$$v_d = v_{A0} - v_{B0} \tag{2.2}$$

In order to explain the cause of the common mode current, the full-bridge can be modeled as a differential and a common mode voltage sources, as in Fig. 2.2. In the same figure also the grid impedance is shown (R_{grid} and L_{grid}), along with the parasitic resistance R_L of the filter inductor L_f and the filter capacitor (C_f with a

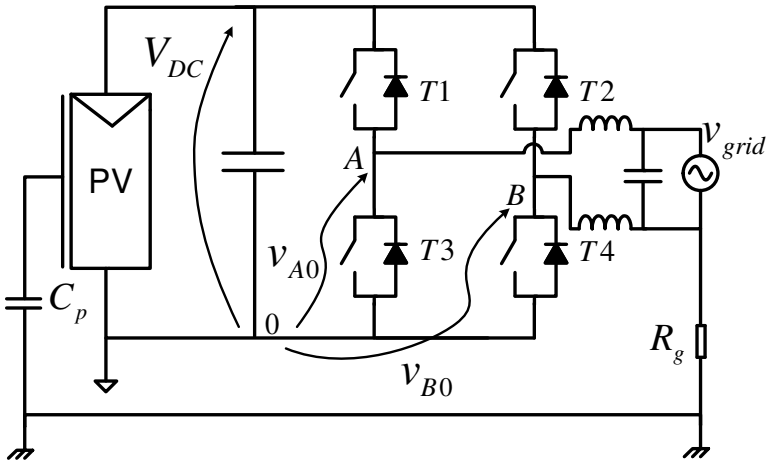


Figure 2.1: Full-bridge inverter with PV DC source.

series resistance R_f, usually employed to damp the resonance of the differential mode circuit).

For completeness, if the filter inductors are not of equal value, another component of the ground leakage current appears. Usually this contribution is lower than the one due to the common mode variations at the converter output.

This schematic leads to the conclusion that the parasitic capacitance of the photovoltaic filed forms a resonant common mode circuit, with a resonant frequency equal to:

$$f_r = \frac{1}{2\pi\sqrt{\left(L_f + L_{grid}\right) C_p}} \tag{2.3}$$

As L_f is usually much greater than the grid inductance, the resonance frequency depends on the filter inductance and on the parasitic capacitance value. However, even for a particular PV field, the value of capacitance depends on ambient conditions, so the result is that the resonance frequency can present very wide variations.

As a matter of fact, when the differential output voltage of the full-bridge, v_d, is not zero, one of the output voltages of the full-bridge will be connected to the DC Link voltage, V_{DC}, while the other will be connected at the negative side of the DC

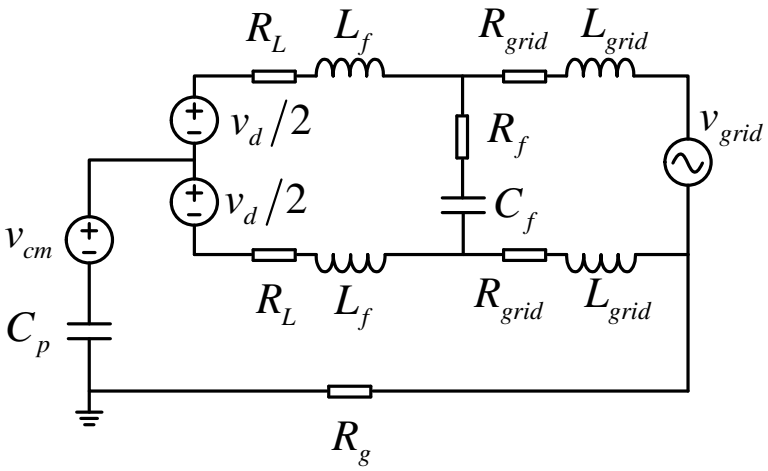


Figure 2.2: Model of the full-bridge converter.

Link. The common mode voltage at the output will simply be equal to $v_{cm} = V_{DC}/2$.

During the current freewheeling, depending on the sign of the current, the differential voltage can be either zero (three level PWM) or $\pm V_{DC}$ (bipolar modulation). While with the bipolar modulation the common mode voltage is always $v_{cm} = V_{DC}/2$, in the three level PWM it can be either V_{DC} or $0V$ depending on the configuration of the transistors.

With this premise, it is obvious that the bipolar modulation strategy (two level output voltage) is ideally suitable for PV inverters. However, its poorer energy efficiency, high output current ripple and common mode voltage variations (during the mandatory dead-times between the commutations) make its application very limited. For this reason, three level inverters are nowadays the most widely adopted solution, although they require specific strategies for the common mode output voltage.

In the following different three level inverters are analyzed. All of them employ different strategies to keep the common mode voltage to a constant level $v_{cm} = V_{DC}/2$. They can be further divided into two kinds: the ones that fix the output of the full-bridge to a known potential with active clamping, and the ones that rely on the transient behavior to achieve the same objective.

It must be said that the reduction of the common mode output voltage is not the only way that can be pursued to reduce the ground leakage currents. In fact, it is sufficient to ensure that high-frequency voltage variations do not happen over the photovoltaic field parasitic capacitance, such as with Neutral Point Clamped (NPC) architectures. Some recent advances are reported in the last part of the chapter as well.

For completeness, it must be said that the common mode current at the output of a three level (unipolar PWM) inverter can be addressed also with a specific output filter, as in [15], see Fig. 2.3.

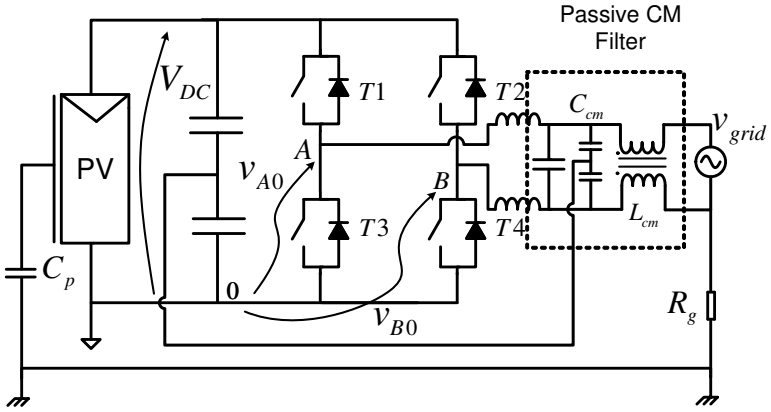


Figure 2.3: Passive filter for ground leakage current reduction in a full-bridge inverter.

However, as it was widely shown, controlling the common mode voltage with a proper topology and PWM strategy allows to strongly reduce the switching losses of the power devices. The solution proposed in [15] is very simple and effective, but its energy efficiency will be similar to a standard three-level full-bridge.

2.1.1 Topologies that do not fix v_{A0} and v_{B0} during freewheeling

In Fig. 2.4 a full-bridge is shown along with two additional blocks that perform the disconnection from the grid during the freewheeling phases. These solutions differ in the way they provide the zero voltage at the output of the full-bridge.

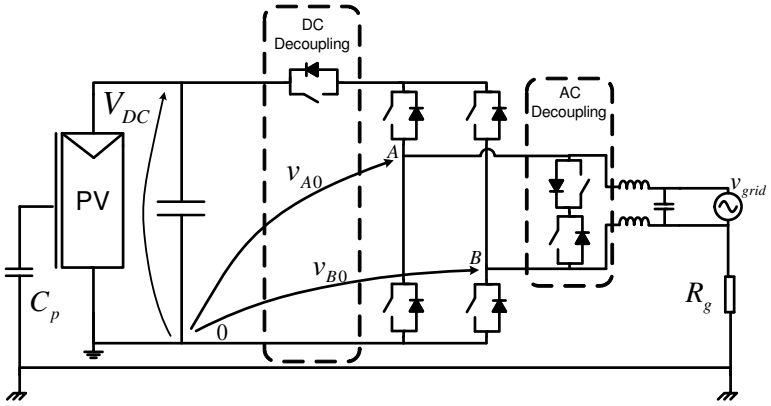


Figure 2.4: Full-bridge with AC decoupling (HERIC) and DC decoupling (H5) blocks.

With the DC decoupling, called H5 topology and employed in converters sold by SMA, the turn on of the upper full-bridge switches provide the zero voltage, while the additional switch disconnects the converter from the grid. The peculiarity of this solution is that the freewheeling takes places only in the upper part of the full-bridge, so only one additional transistor is necessary to realize the decoupling.

The AC decoupling is called Highly Efficient Reliable Inverter Concept (HERIC) and is employed in Sunways converters. The zero voltage output is obtained by turning on the additional devices in the AC-side, short circuiting the grid, while all the devices of the full-bridge are turned off.

In fact, when supplying the zero output voltages, in both solutions the voltages v_{A0} and v_{B0} remain floating and the correct operation relies on the symmetry of the commutations. In unbalanced conditions, v_{cm} drifts from the desired value and higher leakage currents arise.

A modification of the standard full-bridge topology was proposed in [16]. Fig. 2.5 illustrates the scheme for this inverter. The upper (T1 and T2) and the lower (T5 and T6) devices are commutated in order to supply the DC link voltage. In particular, T1 and T6 share the same PWM signal, as T2 and T5.

The middle devices (T3 and T4) select the polarity of the output voltage. Consid-

ering the positive half cycle, T4 is kept on, T1 and T6 commutate at high frequency while the other devices are off.

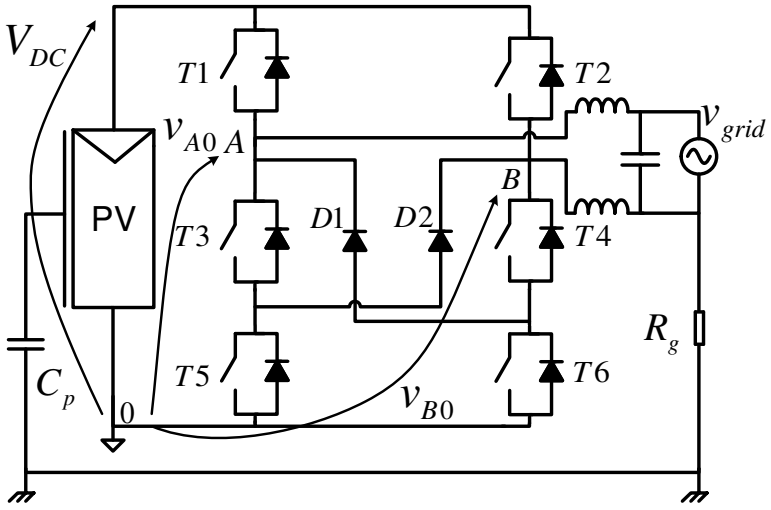


Figure 2.5: H6-type topology proposed in [16]

In the case of positive half cycle two configurations are possible:

1. T1 and T6 on (D1 off): $v_{A0} = V_{DC}$, $v_{B0} = 0$, $v_{cm} = V_{DC}/2$.
2. T1 and T6 off (D1 on): $v_{A0} = v_{B0} = V_{DC}/2$, $v_{cm} = V_{DC}/2$.

During the grid negative half cycle the circuit behavior is dual: T3 on, T4 off, whereas T2, T5 and D2 commutate at the PWM switching frequency.

It is important to highlight that this topology, as in the case of H5 and HERIC, does not actively control the common mode voltage during the freewheeling, so high leakage current can arise in asymmetric conditions.

A novel topology was recently presented in [17] and its architecture is reported in Fig. 2.6. This topology is studied in order to avoid the conduction of the antiparallel diodes of the devices.

For example during the positive half cycle two configurations are possible:

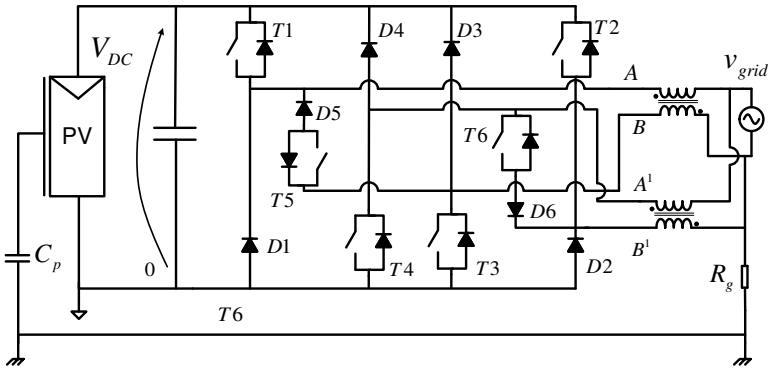


Figure 2.6: Topology proposed in [17].

1. T1 and T3 on (T5 off): $v_{A0} = V_{DC}$, $v_{B0} = 0$, $v_{cm} = V_{DC}/2$.

2. T1 and T3 off (T5 on): $v_{A0} = v_{B0} = V_{DC}/2$, $v_{cm} = V_{DC}/2$.

The drawback of this topology is the increased number of devices, the need for two inductors and the inability to handle reactive power. However, as MOSFETs with slow body diode can be employed, this solution can lead to very high efficiencies.

2.1.2 Topologies that fix v_{A0} and v_{B0} during freewheeling

An immediate approach to control the common mode voltage during the freewheeling was to modify the H5 topology, by adding a diode connected between the midpoint of the DC Link and the high-side of the full-bridge. This topology was proposed in [18] and is reported in Fig. 2.7. The PWM scheme is exactly the same of H5.

The main drawback of this solution is that the DC Link voltage must be equally divided between the capacitors C_1 and C_2, otherwise the ground leakage current increases. As a matter of fact, if a diode is added to the midpoint, the unidirectional current flow will cause a drift in the mid-point voltage, unless countermeasures are employed, i.e. a resistive divider or an additional converter in order to balance the mid-point. Moreover, an uncontrolled drift of the mid-point voltage poses a serious threat to safety, as usually if the DC-Link is composed of series capacitors, the volt-

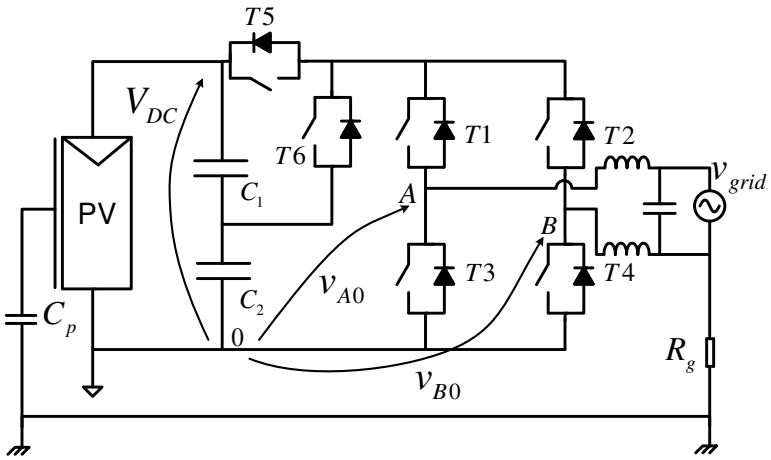


Figure 2.7: Topology proposed in [18]

age rating of the single capacitor is lower than the maximum DC-Link voltage. These solutions obviously deteriorate the efficiency of the converter and add complexity.

Another solution based on a modification of an existing topology was proposed in [19], see Fig. 2.8. In this topology, the bidirectional switch in addition to the full-bridge was realized with a diode bridge rectifier and an additional device, hence the name HB-ZVR (H-Bridge Zero Voltage Rectifier).

The modulation strategy is very similar to HERIC. Considering the positive half cycle, T1 and T4 commutate at high frequency supplying the DC-Link voltage to the output, while T5 switches complementary to supply the zero voltage.

By connecting the source of the additional device to the mid-point it is ensured that v_{A0} and v_{B0} are clamped to $V_{DC}/2$ when supplying the zero voltage. An additional diode is inserted in the current path to prevent the short circuit of the capacitors.

As in the previous case, it is extremely important to control the mid-point voltage, otherwise high ground leakage current will arise. This task is made difficult by the presence of the diode, that present the same problem as in [18]. The balancing of the voltage across the DC Link capacitors was not addressed in [19].

A full-bridge topology with a modified DC Decoupling block was proposed in [20], where two devices are added in series to the DC Link rails. Two diodes are con-

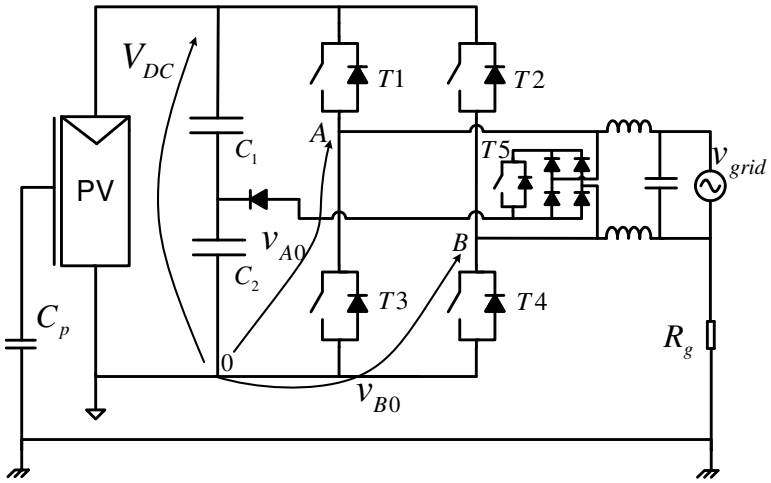


Figure 2.8: Topology proposed in [19]

nected between the high and low sides of the full-bridge and the mid-point voltage, see Fig. 2.9.

This particular topology employs the decoupling transistors, T5 and T6, to supply the DC Link voltage to the output, while the full-bridge devices are used to select the polarity and to give a freewheeling path for the grid current. For example, during the positive half cycle, T1 and T4 are always on. During the active phase T5 and T6 are switched on, while during the freewheeling the DC decoupling is turned off, and the zero voltage is provided by the turn on of T2 and T3. As a matter of fact, during the freewheeling phase the full-bridge is completely short-circuited, and the grid current should divide into the two possible paths given by the high and low side freewheeling.

The additional diodes clamp the common mode voltage to $V_{DC}/2$. Again, the balance of the DC Link capacitors is not addressed in [20].

Based on the same topology, the Unipolar Transformerless (UniTL) PWM was proposed in [21]. In this solution, the full-bridge is driven by a standard three-level unipolar PWM with the freewheeling that happens in both the high and low sides of the full-bridge. The DC decoupling transistors are switched off alternately to detach the converter from the grid during both freewheeling phases. In this way it is pos-

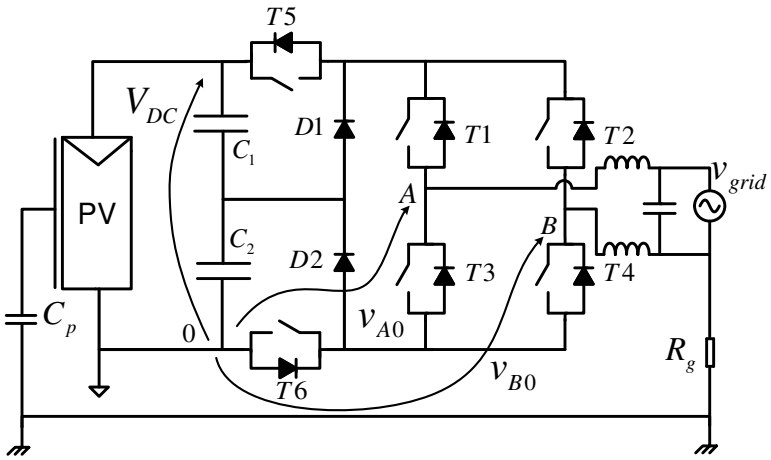


Figure 2.9: The H6 topology

sible to obtain an output voltage main harmonic at twice the switching frequency, differently from all the other topologies previously analyzed.

2.1.3 Topologies that employ the ground connection

As anticipated, if the earth potential is connected to a fixed voltage with respect to the PV cell, no high frequency voltage variations happen over the parasitic capacitance.

In [22] a particular structure of parallel buck converters is employed to ensure that, during each half cycle of the grid voltage, the neutral conductor is connected either to the high or low side of the DC Link, see Fig. 2.10. While this can reduce greatly the ground leakage current, special care must be taken at the zero-crossing of the grid voltage.

Another topology which exploits the ground connection to reduce the ground leakage current was proposed in [23] and is presented in Fig. 2.11. The principle of operation resides in the fact that during the whole grid voltage period the neutral conductor is connected to the negative side of the DC Link, ensuring low values of ground leakage current.

During the positive half wave, T1 and T3 are on, while T4 and T5 commutate

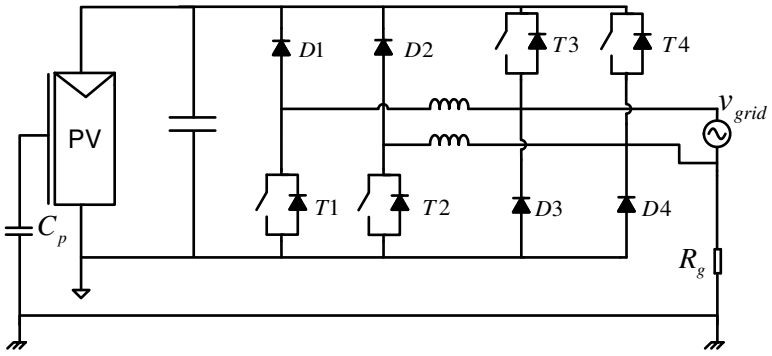


Figure 2.10: Topology proposed in [22].

at high frequency to synthesize the correct output voltage. The flying capacitor is connected in parallel with the DC Link. During the negative half wave, T5 is kept on, while T1, T2 and T3 realize the high frequency switching. In particular, when T1 and T3 are on, the configuration is the same as the positive half wave, and the zero voltage is provided. When T2 switches on, T1 and T3 turn off, and the output voltage is equal to the opposite of the DC voltage of the flying capacitor.

In [23] the aspect regarding the current stress of the flying capacitor is also taken into account, and some guidelines are provided to choose the capacitance values.

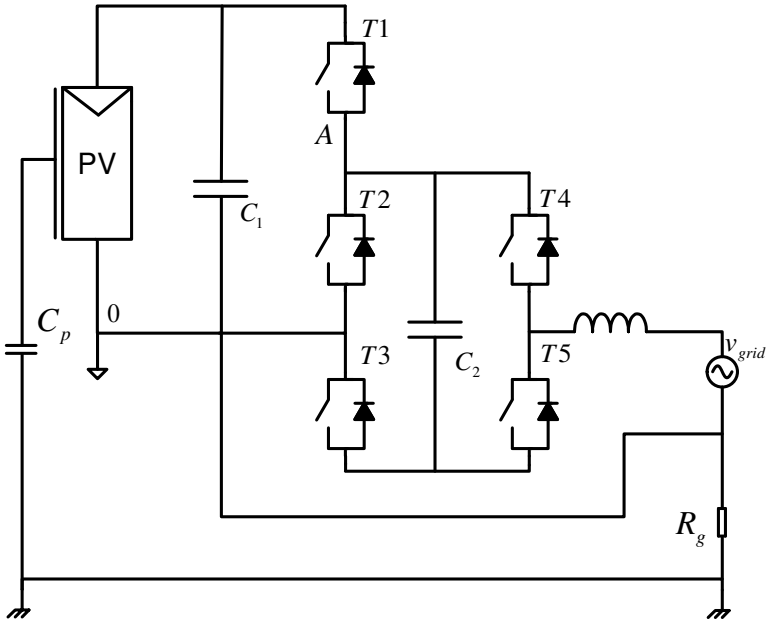


Figure 2.11: Topology proposed in [23].

Chapter 3

State of the art of Multilevel Inverter topologies

3.1 Introduction

Multilevel converters ensure a better reconstruction of the output waveform, allow to reduce the size of output filters and increase the converter efficiency. Research on multilevel converters has been going on for several years [24], but only recently they have been applied to PV converters [25, 26, 27].

The basic idea is that the DC Link voltage can be split across different capacitors, that can provide intermediate voltage levels between the reference potential and the DC Link voltage [28]. Numerous solutions for multilevel inverters are present in literature; in the following a review of the state of the art is reported, with reference to a five-level output voltage. However, most of the topologies could be extended to a greater number of output voltage levels.

As the focus of this work is on single phase (i.e. not high voltage) photovoltaic systems, only some of the numerous ideas presented in literature are reported.

3.2 Half-bridge Neutral Point Clamped (NPC)

This topology consists of a NPC leg composed of eight transistors in series. The diodes provide the clamping of the DC Link capacitors, synthesizing multiple output voltage levels [28].

The diode-clamped solution (Fig. 3.1a) needs several components (series diodes), and presents serious issues with the balancing of the DC Link capacitors, limiting practically its applications to reactive power compensators [29]. Even in this latter application, this kind of converter presents the need of a balancing system for the DC Link capacitors i.e., external circuitry [30], that increases the complexity of the converter, or modified PWM strategies, which present various drawbacks [31, 32].

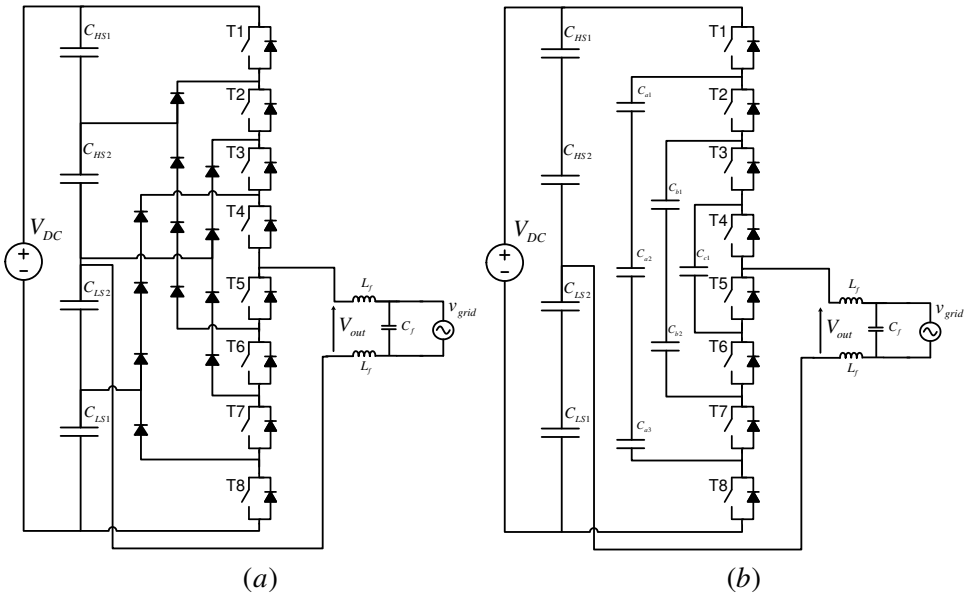


Figure 3.1: Five-level NPC Inverters: diode clamped (a) and flying capacitor (b).

The flying capacitor solution (Fig. 3.1b) allows to exchange even active power and it is suitable for grid-connected inverters. Anyway, a balancing system for the DC Link capacitors is mandatory.

These converters offer multiple switches configurations which can supply the

same voltage to the load, allowing the development of strategies that balance the charge between the DC Link capacitors [33]. Even for a five-level converter, multiple voltages need to be monitored and the balancing strategy is not trivial.

Moreover, with this kind of topologies (diode-clamped or flying capacitors), the frequency of the output current ripple is at the switching frequency. Despite the need for twice the DC Link voltage, if compared to full-bridge topologies, the half-bridge NPC is ideal for transformerless photovoltaic converters, as it allows to obtain very low ground leakage currents. In [34] a NPC half-bridge was applied to a three-level photovoltaic inverter, but the principle remains valid even for a greater number of voltage levels.

3.3 Cascaded full-bridge

Multilevel output voltage can be provided by connecting in series multiple full-bridge structures [28], as in Fig. 3.2.

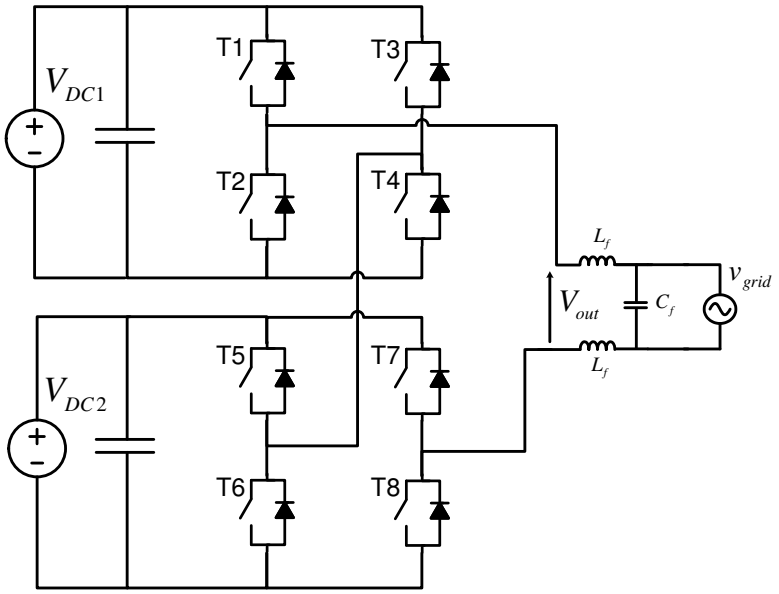


Figure 3.2: Cascaded full-bridge with independent power supplies.

Several independent DC sources are needed for the correct operation i.e., multiple PV strings [35] or transformers followed by diode rectifiers. Another approach is to employ the transformer not to create the DC supplies but to connect same full-bridge structures with the same DC supply [36]. Indeed, this represents the major drawback of this topology [37].

Multiple PWM strategies are available for the cascaded full-bridge: carrier based modulations [38] or space-vector approaches [39, 40].

Anyway, eight devices are needed, and there are always four devices conducting.

3.4 NPC full-bridge

The NPC single-phase full-bridge converter of Fig. 3.3 allows to obtain a multilevel output voltage with a reduced complexity with respect to the NPC half-bridge, as it can be employed as a substitute of the full-bridge. A strong point of this architecture is that multiple DC sources are not needed.

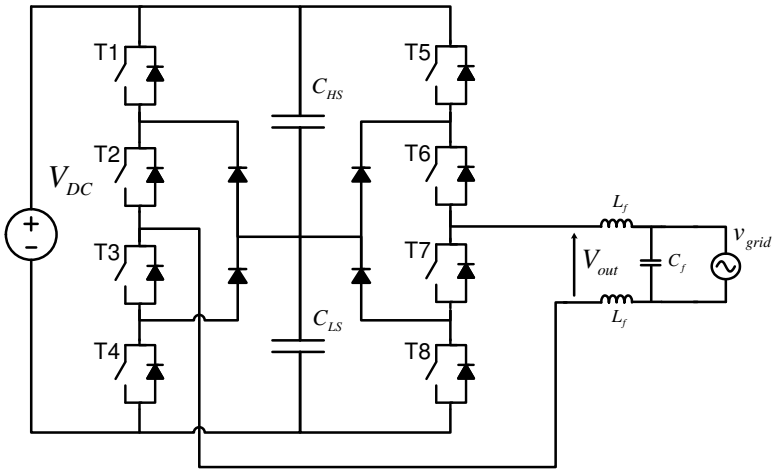


Figure 3.3: NPC full-bridge five-level inverter.

However, for more than five-level output voltage this topology would encounter the same limits described in section 3.2.

3.5 Hybrid five-level topologies

In a hybrid topology, the DC Link voltage is not distributed between multiple structures. Usually, a simple two level half-bridge is employed to change the polarity of the output voltage, while a multilevel structure synthesizes the multiple output voltage levels. In this way, the devices of the two level half-bridge must sustain the whole DC Link voltage. Some hybrid topologies for five-level converters were presented in [41, 42], but only the one presented in [43] (Fig. 3.4) was applied to a photovoltaic source [44, 45].

In this proposal, a bidirectional switch (realized with an IGBT and four diodes) is added to a standard full-bridge topology. The additional switch connects the midpoint of the DC Link to the converter output. The same topology was also extended to a seven-level output voltage in [46].

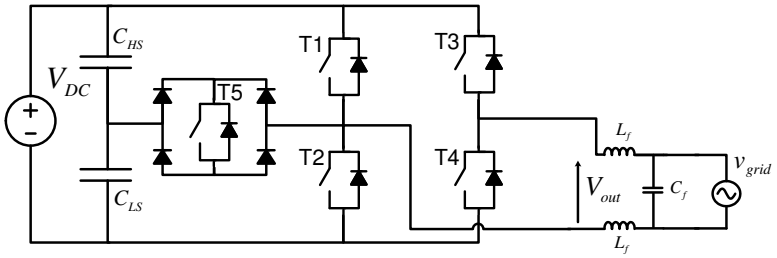


Figure 3.4: Five-level full-bridge topology proposed in [43].

Chapter 4

Novel Nine Level transformerless Inverter

4.1 Introduction

As described in chapter 3.3, cascaded full-bridge solutions need a separate power supply for each full-bridge section [47]. The way these supply are generated and the voltage ratio between them lead to different solutions: [48, 49, 50, 51].

The purpose of this chapter is to describe the development of a nine level cascaded full-bridge converter suitable for PV transformerless systems.

4.2 Architecture of the converter

The basic structure is composed of two cascaded full-bridges, the former supplied by the PV generator and the latter supplied by a flying capacitor. Since there are no particular constraints on the ratio between the two voltages, for the sake of simplicity it is assumed that the voltage on the flying capacitor is always lower than the DC source. For this reason, the PV-fed full-bridge is named High-Voltage Full-Bridge (HVFB), while the other full-bridge is named Low-Voltage Full-Bridge (LVFB), see Fig. 4.1.

Cascading full-bridge structure is often employed in high-voltage converters, as the DC Link voltage can be equally divided upon each full-bridge structure, and devices with lower breakdown voltage requirement can be chosen. However, if the same DC voltage is chosen for each full-bridge, only a five-level output voltage can be achieved.

A way to increase the number of voltage levels and to reduce the switching harmonic distortion is to choose a different voltage for each DC supply. In [52] different choices are proposed, in particular, if the DC voltage supplies are chosen in a geometric progression of ratio 3, 3^n equally-spaced output voltage levels can be achieved with n full-bridge structures.

If the minimum switching harmonics are pursued, the best choice is to chose the voltage across the flying capacitor equal to one-third of the DC Link voltage, i.e., $V_{fc} = V_{DC}/3$. With this first approach, different zones can be identified depending on the output voltage demand: $\overline{V_{out}}$, that represents the average of V_{out} in a switching period.

There are several possible ways to provide the same $\overline{V_{out}}$ with the available voltages, in this work it was chosen to switch between adjacent voltage levels, to minimize the switching ripple and reduce the switching loss. In this way, the zones of Fig. 4.2 are identified. In the zones identified by the $+$ sign the flying capacitor voltage is added to the HVFB output, while in the zones identified by the $-$ sign it is subtracted.

Fig. 4.2 is realized under the assumption that $V_{fc} < 0.5V_{DC}$, otherwise the levels are positioned in a different way, see Fig. 4.3 for reference. It is important to note that the operating zones are the same as the previous case, only the voltage order is changed. This choice allows to switch between non-adjacent level, and in the following it will be explained that this choice has certain benefits.

The PWM strategy is shown in TABLE 4.1. In particular, one leg of the HVFB commutates at line frequency, while the other presents high-frequency switching behavior only in Zone 2, where the flying capacitor voltage is regulated (see section 4.3). Most of the switching is condensed in one leg of the LVFB, while the other operates at a multiple of the line frequency.

The fact that no high-frequency switching is required in one leg of each full-

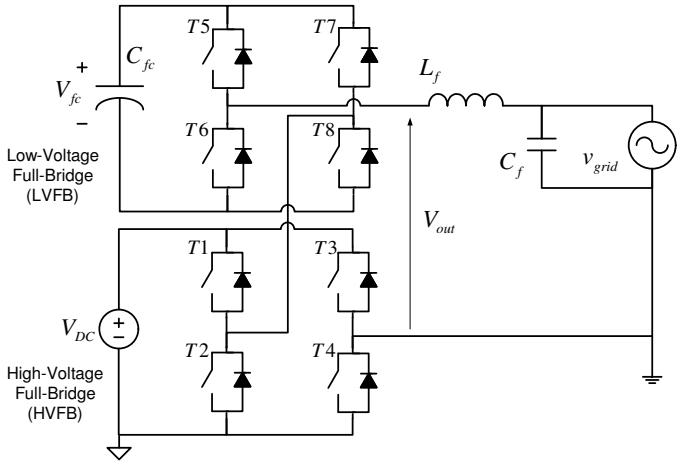


Figure 4.1: Cascaded full-bridge with flying capacitor.

bridge makes possible to employ MOSFETs with a very low on-state resistance, in order to increase the converter efficiency. In fact, the intrinsic body diode of the power MOSFET does not offer good dynamic performance, as a trade-off exists between the on-state resistance and the reverse recovery time. The power IGBTs do not suffer from this problem, as they do not present an intrinsic body diode, and a high performance diode can be embedded in the same package. For this reason, while it is true that MOSFETs offer low on-state resistance, their application should be avoided for hard-switching converters.

4.3 Flying Capacitor Voltage Regulation

While the balancing of the flying capacitor in a converter that does not need to transfer active power, such as shunt active filters, is an easy task, and can be realized by controlling small amounts of active power [53], this is not the case of a PV inverter.

In fact, although the recent international regulation impose that new designs of grid-connected inverters must be able to provide specific amount of reactive power,

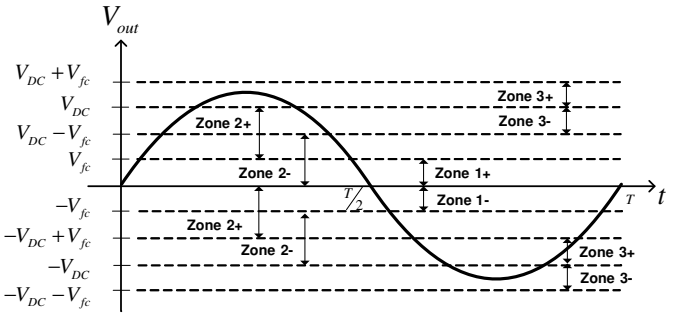


Figure 4.2: Operating zones of the proposed PWM modulation when $V_{fc} < 0.5V_{DC}$.

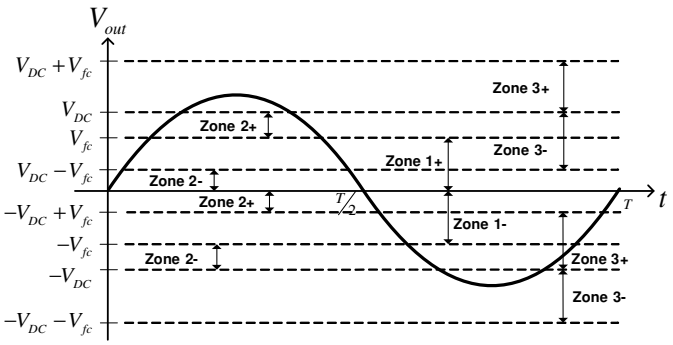


Figure 4.3: Operating zones of the proposed PWM modulation when $V_{fc} > 0.5V_{DC}$.

the main task remains to transfer power into the grid with unity power factor. The situation becomes more critical considering that the DC Link voltage is always changing due to the variable weather condition and the MPPT algorithm, thus a reliable control of the flying capacitor voltage is mandatory.

The balancing of the flying capacitor is possible by using different switching patterns that lead to the same averaged output voltage. As it is evident, with the the choice $V_{fc} = V_{DC}/3$, there are no redundant states that can output the same voltage level with a different switch configuration. As a consequence, switching between non-adjacent level must occur (level skipping) to achieve the balancing of V_{fc}.

The voltage control happens during Zones 2. Fig. 4.4 and Fig. 4.5 show the choice

Table 4.1: Description of the converter operating zones

Zone	Output Voltage	On Devices	Off Devices	Switching Devices
Zone 3-	$-V_{DC}-V_{fc} \leftrightarrow -V_{DC}$	T2, T3, T7	T1, T4, T8	T5, T6
Zone 3+	$-V_{DC} \leftrightarrow -V_{DC}+V_{fc}$	T2, T3, T8	T1, T4, T7	T5, T6
Zone 2+	$-V_{DC}+V_{fc} \leftrightarrow 0$	T3, T7	T4, T8	T1, T2, T5, T6
Zone 2-	$-V_{DC} \leftrightarrow -V_{fc}$	T3, T7	T4, T8	T1, T2, T5, T6
Zone 1-	$-V_{fc} \leftrightarrow 0$	T1, T3, T7	T2, T4, T8	T5, T6
Zone 1+	$0 \leftrightarrow V_{fc}$	T2, T4, T8	T1, T3, T7	T5, T6
Zone 2+	$V_{fc} \leftrightarrow V_{DC}$	T4, T8	T3, T7	T1, T2, T5, T6
Zone 2-	$0 \leftrightarrow V_{DC}-V_{fc}$	T4, T7	T3, T8	T1, T2, T5, T6
Zone 3-	$V_{DC}-V_{fc} \leftrightarrow V_{DC}$	T1, T4, T7	T2, T3, T8	T5, T6
Zone 3+	$V_{DC} \leftrightarrow V_{DC}+V_{fc}$	T1, T4, T8	T2, T3, T7	T5, T6

of the operating zones under the hypothesis of positive grid current. In fact, if V_{fc} is added to the output voltage, the result will be a discharge of the flying capacitor, on the contrary, if V_{fc} is subtracted, the output current will charge the capacitor. In these latter figures a solid line accounts for a low-frequency devices in on-state, no line in case of off-state.

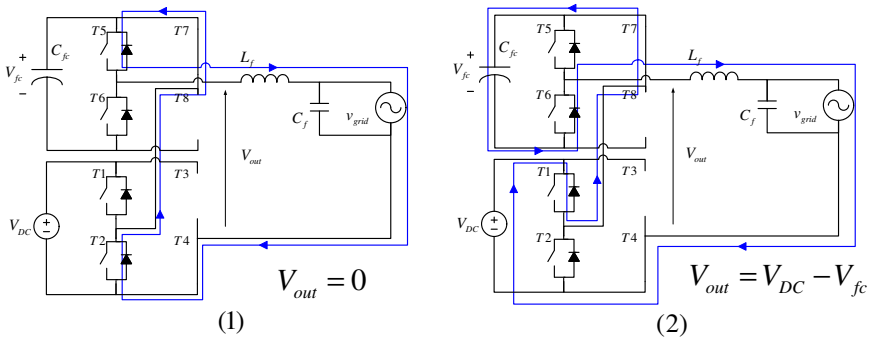


Figure 4.4: Flying capacitor charge.

The strategy previously described allows to charge or discharge the flying capacitor during operation in Zone 2. However, this fact does not imply that the cumulative effect of the other zones allows the long-time control of the flying capacitor voltage.

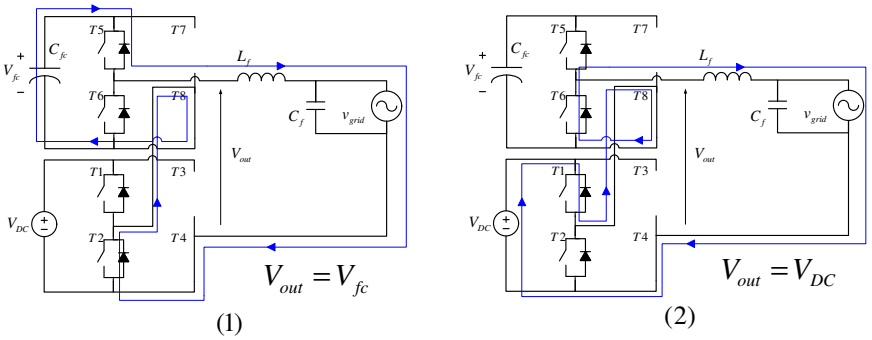


Figure 4.5: Flying capacitor discharge.

To this aim, extensive simulations regarding the theoretical behavior of the power converter operating under different supply voltage conditions were performed. Depending on the operating zone and on the current magnitude, the average current charging the flying capacitor during a grid voltage period can be evaluated. In the following analysis a sinusoidal voltage of amplitude $v_{grid} = 230\sqrt{2}$ was considered. A voltage sweep of both the DC Link and flying capacitor voltages was performed and the average current of the flying capacitor was evaluated in the following cases:

1. The configurations that lead to a charge of the flying capacitor (Fig. 4.4) are always chosen, and the average charging current I_{fc}^{+} is evaluated.

2. The configurations that lead to a discharge of the flying capacitor (Fig. 4.5) are always chosen and the average charging current I_{fc}^{-} is evaluated.

If I_{fc}^{+} is positive and I_{fc}^{-} is negative it means that with the combination (V_{DC}, V_{fc}) the flying capacitor voltage is fully controllable. Otherwise it can happen $I_{fc}^{+} < 0$ (the flying capacitor cannot be charged) or $I_{fc}^{-} > 0$ (the flying capacitor cannot be discharged). As $I_{fc}^{+} > I_{fc}^{-}$, the cases above cover all the possibilities.

It is important to note that the magnitude of the grid current is not important, as it affects only the absolute value of I_{fc}^{+} and I_{fc}^{-} and not the sign. Moreover, the analysis is based on the duty cycles, so the results hold for every pair $(V_{DC}/v_{grid}, V_{fc}/v_{grid})$.

Fig. 4.6 reports the results of the simulations. Only the points where $V_{DC} > V_{fc}$

(as hypothesized) and $V_{DC} + V_{fc} > v_{grid}$ (the converter can control the grid current) are significant.

The white area delimited by the bottom and right edges of the plot and the grey area represents the condition of full controllability of V_{fc}, the black area represents the condition $I_{fc}^{-} > 0$ and the grey area $I_{fc}^{+} < 0$. For this set of simulations a sinusoidal grid current with unity power factor was considered.

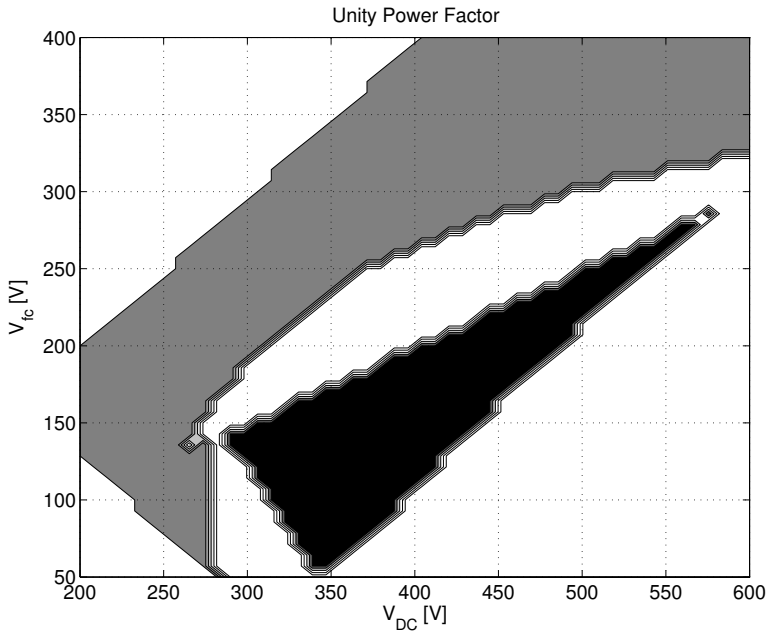


Figure 4.6: Flying capacitor control behavior with unity power factor.

From the results of Fig. 4.6 these consideration can be done:

- If the converter enters the black area, V_{fc} will rapidly rise (the point of operation will move upwards in the graph) until entering the white area.
- If the converter enters the grey area, V_{fc} will decrease (the point of operation will move downwards in the graph) until entering the white area.

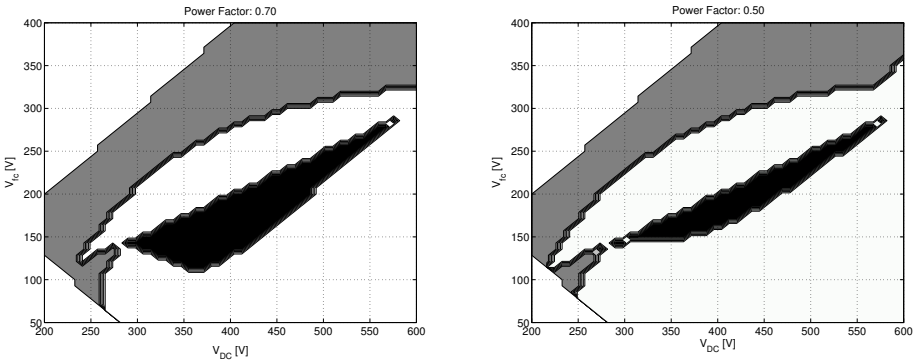


Figure 4.7: Flying capacitor control behavior with different values of power factor.

- Even if the balancing control fails, V_{fc} is limited by the grey area.
- The white area between the black and the grey one represents a stable operating condition of the converter.

4.4 Application to transformerless photovoltaic converters

A peculiar characteristic of the modulation strategy is that particular care must be taken when commutating T3 and T4. In fact, the leg formed by T3 and T4 is directly connected to the neutral conductor. This means that during the commutation high currents will circulate in the neutral conductor due to the panels' parasitic capacitance.

For this reason, a specific transient circuit (TC) was developed to aid the commutation of the grid-frequency leg. The comprehensive schematic of the proposed converter, including the parasitic capacitance, is shown in Fig. 4.8.

Considering for example a transition from the positive half-cycle to the negative one, it means that the transistor T4 must open while T3 must be closed. In order to prevent high surge currents, the current is deviated from the full-bridge transistors T1-T4, and the bidirectional switch T9 is closed. In this situation, the full-bridge is completely switched off, and the HVFB acts as a short-circuit due to T9. The

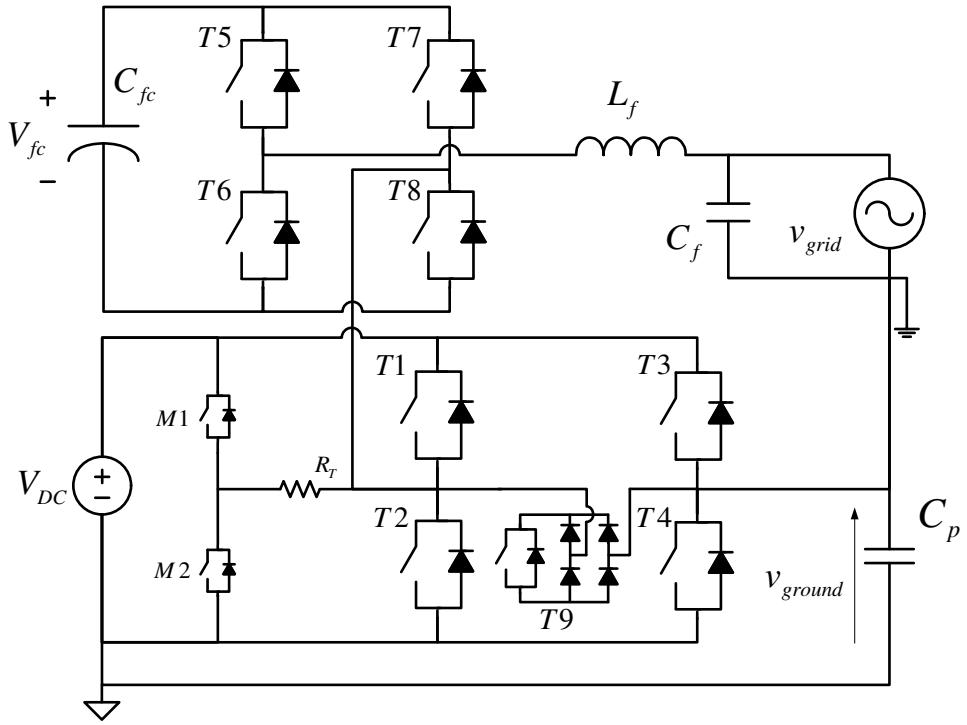


Figure 4.8: Proposed topology.

potential of the parasitic capacitor remains floating, and is still at the previous value $v_{ground} = 0V$.

Then, the low-power MOSFET M1 is switched on, charging with a first order transient the parasitic capacitance C_p through the resistance R_T, see Fig. 4.9 and Fig. 4.10.

When the transient ends, it is safe to switch on the transistors T4 and T2 and to switch off the bidirectional switch T9.

In other words, the parasitic capacitance is always charged through R_T, and the current peaks are acceptable. This can be done because while the HVFB supplies the zero voltage, the current can be controlled with the switching of the LVFB.

The power loss of the transient circuit can be evaluated with the well-known for-

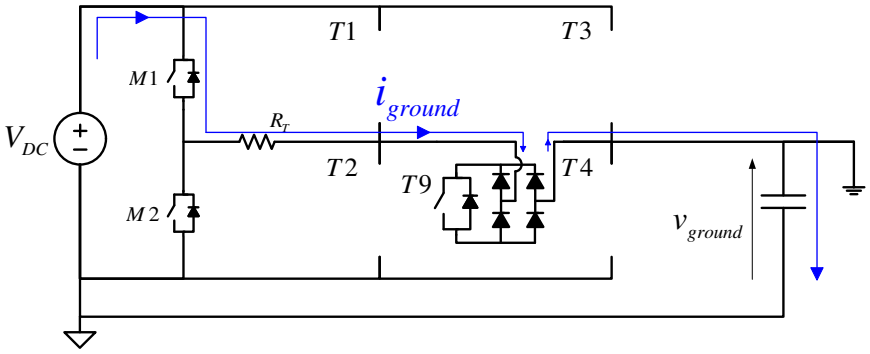


Figure 4.9: Transient Circuit (TC)

mula $P_{tc} = C_p V_{DC}^2 f_{grid}$, which amounts to 1-2 W with the usual values of the parasitic capacitance (100-200 nF). It is important to note that the transient circuit does not increase the power losses, as the power P_{tc} would be dissipated by the transistors T3 or T4 with high current peaks.

Since in grid-connected operation the modulation index is always very similar to the grid voltage even with power factor different from unity, the same switching strategy works even when the current is not in phase with the grid voltage.

Considering TABLE 4.1, the relationship between the output voltage and the duty cycle d is:

$$\overline{V_{out}} = dV_{out}^1 + (1-d)V_{out}^2 \tag{4.1}$$

Where V_{out}^1 and V_{out}^2 represent the output voltage values depending on the operating zone, considering $V_{out}^1 < V_{out}^2$. This means that is possible to synthesize the desired voltage by selecting a duty cycle

$$d = \frac{V_{out}^2 - \overline{V_{out}}}{V_{out}^2 - V_{out}^1} \tag{4.2}$$

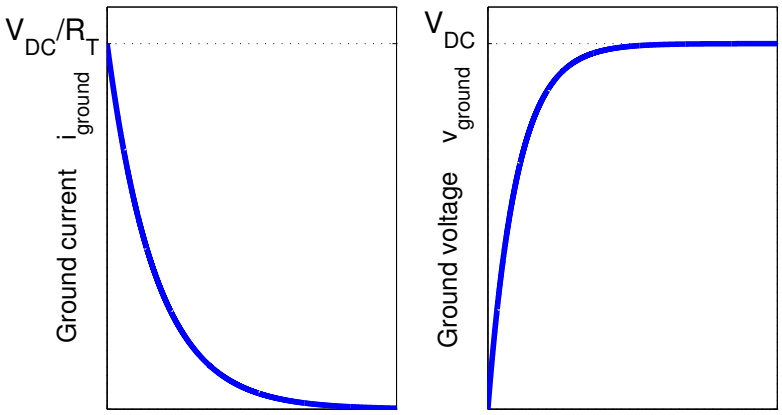


Figure 4.10: Transient Circuit example waveforms.

4.5 DC Voltage independent modulation

As the DC Link voltage changes due to the variability of the solar irradiance, the operation of the converter must not be affected. In fact, it is easy to derive the duty cycles in case of fixed voltage ratio between V_{DC} and V_{fc}, otherwise the computation has to be done on-line.

This kind of approach employs the measurement of the DC voltage in order to synthesize, in the next PWM cycle, the desired value. The on-line calculation of the duty cycle was already explored in [40], and in this thesis it is customized to the modulation strategy.

4.6 Simulation Results

Extensive simulation results concerning grid current distortion and ground leakage current were performed in order to highlight the characteristic of the proposed converter and modulation strategy.

The tool employed for the simulation was the PLECS toolbox in a Simulink en-

vironment.

The first set of simulations aimed at evaluating the quality of the grid current under different conditions of DC voltage ratio. For the simulations it was chosen $V_{DC} = 300V$, $L_f = 1.5mH$, $v_{grid} = 230V_{RMS}$, $f_{grid} = 50Hz$, $C_{fc} = 1mF$. The injected grid current was $8.5A_{RMS}$ (corresponding to 2 kW of electric power). The switching frequency was $f_{sw} = 20kHz$. A simple PI regulator was employed as the current controller, and for the flying capacitor voltage a hysteresis controller with a window of $\pm 5V$ was chosen.

Fig. 4.11 and Fig. 4.12 show the behavior of the converter when the setpoint of V_{fc} is regulated at 180 V. Fig. 4.11 show the grid voltage and current. The resulting current THD is 3.2%. Fig. 4.12 highlights some aspect of the operation of the converter, in particular the output voltage and the separate voltages of the full-bridges and the flying capacitor voltages. It is clear that the high-frequency switching of the HVFB is limited to zone 2, and that the hysteresis controller is able to regulate the voltage of the flying capacitor.

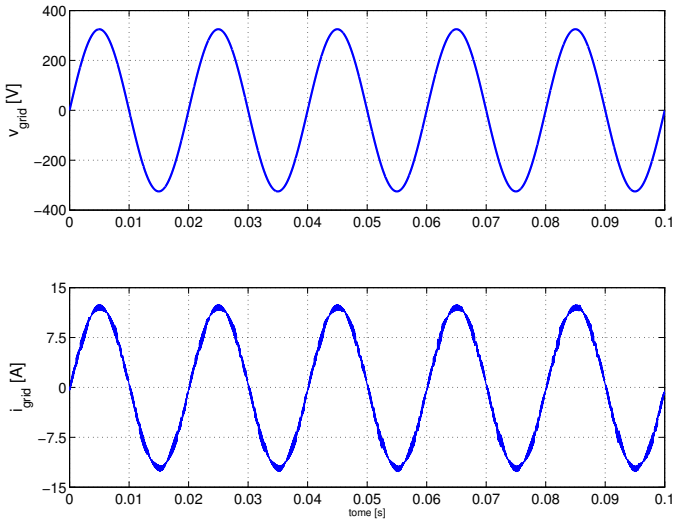


Figure 4.11: Grid voltage and current with $V_{fc} = 180V$.

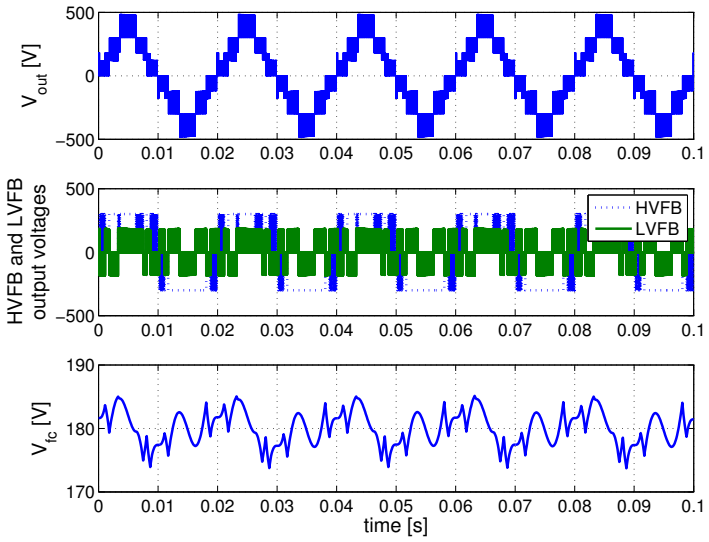


Figure 4.12: Converter output voltage, HVFB and LVFB output voltages and Flying capacitor voltage with $V_{fc} = 180V$.

In the following simulations, the same waveforms of Fig. 4.11 and Fig. 4.12 are reported for different values of V_{fc}. It is important to note that the THD gradually decreases with the flying capacitor voltage, due to the reduced output voltage ripple. In fact, with $V_{fc} = 150V$ (Fig. 4.13 and Fig. 4.14) the THD is 2.9%, while with $V_{fc} = 100V$ (Fig. 4.15 and Fig. 4.16) the THD is 2.6%.

During these simulations only a first order filter and a rather low switching frequency were employed. In fact, the THD could be further reduced by modifying these two design parameters.

The performance of the proposed modulation strategy and TC were evaluated by simulating the PV parasitic capacitor with a capacitance connected between the neutral conductor and the negative side of the DC Link. It is worth noting that the parasitic capacitance is distributed between the positive and negative poles of the DC Link, but it is irrelevant to the analysis, as in the equivalent common mode circuit the DC Link is short-circuited.

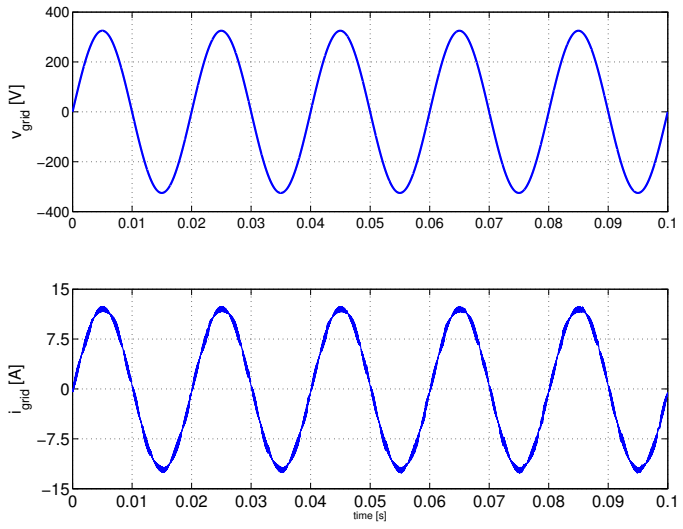


Figure 4.13: Grid voltage and current with $V_{fc} = 150V$.

Fig. 4.17 shows the voltage and current across the parasitic capacitance ($C_p = 200nF$, with $R_{ground} = 2\Omega$, that represents the worst case scenario for a 2kWp system) in the ideal case of grid with zero impedance. The current spikes are due to the TC (with $R_T = 750\Omega$), the additional current spikes are due to the commutations of the grid frequency leg before the end of the transient. As a matter of fact, with ideal devices and ideal grid, even a small voltage transient across a capacitance leads to high current spikes.

In these conditions no common mode filters are used, and the output filter consists only of a single inductance on the phase conductor. The ground leakage current is $i_{ground} = 25mA_{RMS}$.

If the grid is not ideal, a ground leakage current appears due to the common mode voltage variations. In Fig. 4.18 a grid impedance of $R_{grid} = 0.1\Omega$ and $L_{grid} = 10\mu H$ was considered. The ground leakage current is $i_{ground} = 47mA_{RMS}$.

As a matter of fact the proposed topology suffers from the same drawback of

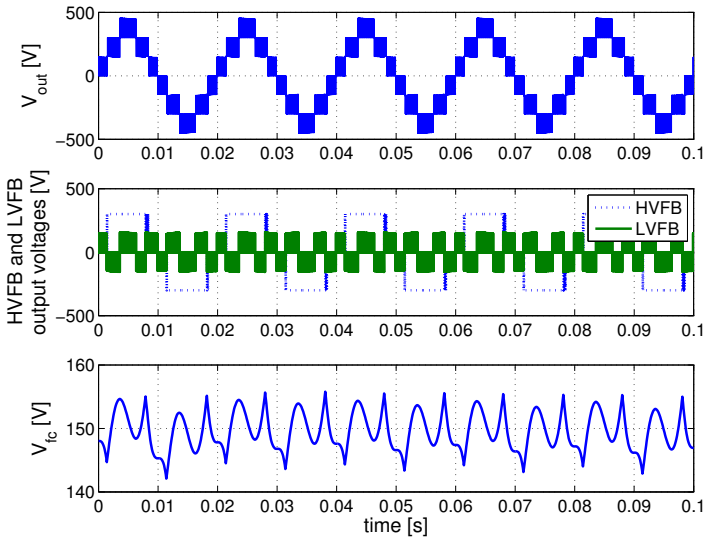


Figure 4.14: Converter output voltage, HVFB and LVFB output voltages and Flying capacitor voltage with $V_{fc} = 150V$.

the NPC solutions, with the increase of ground leakage current due to the transient circuit operation. This means that the problem of the ground leakage current can be addressed by using the same solutions applicable to the NPC converters, i.e. common mode filters.

In the example of Fig. 4.19 a small common mode filter (with $L_{cm} = 2mH$) was employed and the TC resistor was increased $R_T = 1.5k\Omega$. In these conditions, the ground leakage current is reduced to $i_{ground} = 30mA_{RMS}$.

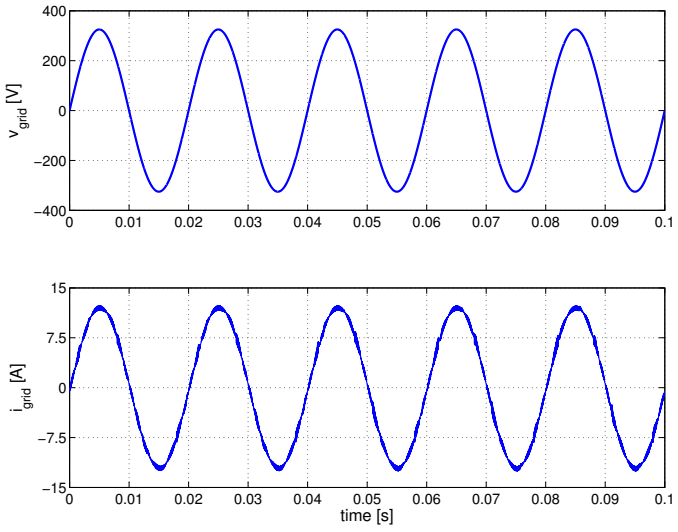


Figure 4.15: Grid voltage and current with $V_{fc} = 100V$.

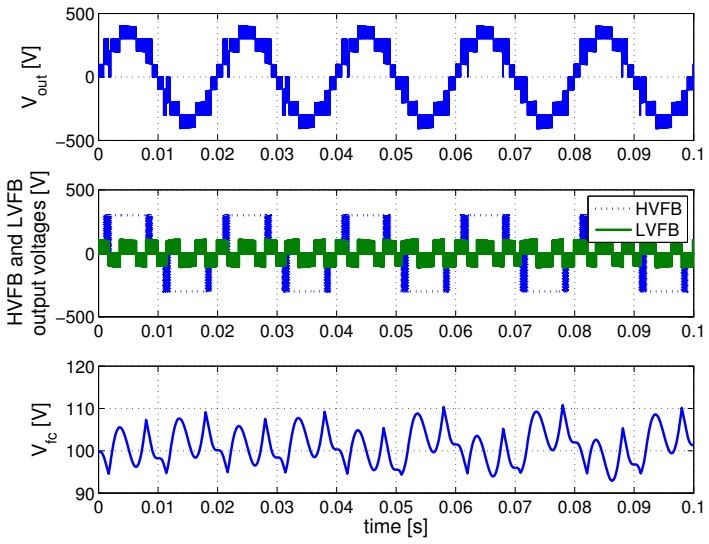


Figure 4.16: Converter output voltage, HVFB and LVFB output voltages and Flying capacitor voltage with $V_{fc} = 100V$.

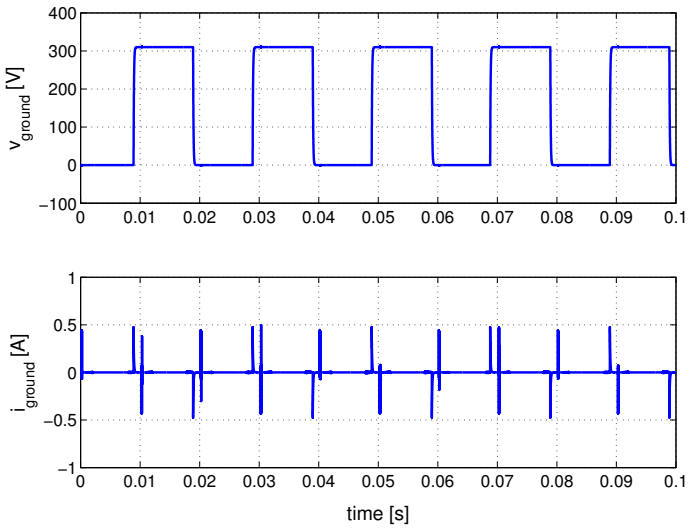


Figure 4.17: Ground voltage and current with ideal grid, $i_{ground} = 25mA_{RMS}$.

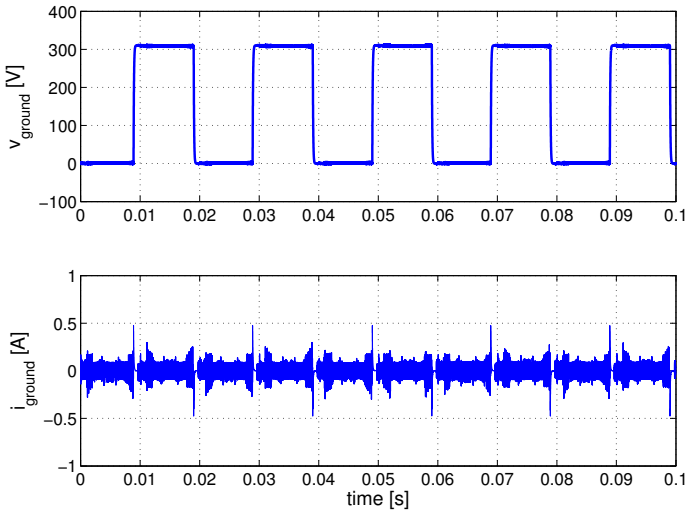


Figure 4.18: Ground voltage and current with non ideal grid, $i_{ground} = 47mA_{RMS}$.

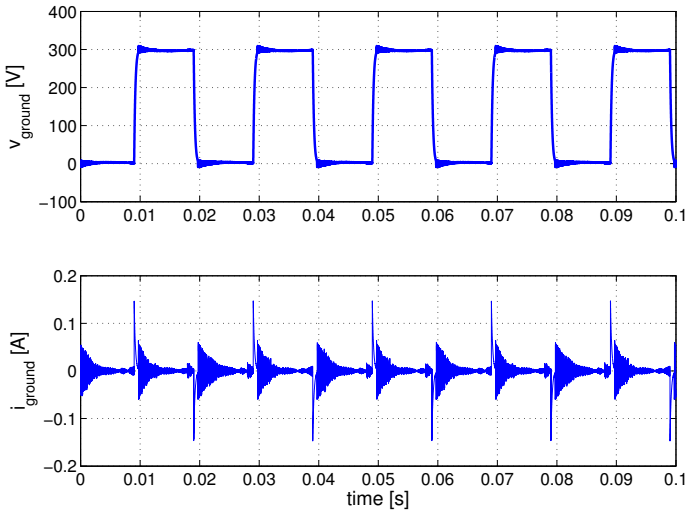


Figure 4.19: Ground voltage and current with non ideal grid and simple common mode filter, $i_{ground} = 30mA_{RMS}$.

4.7 Nine Level converter prototype

In order to test the proposed converter, a prototype was designed and built. The prototype must be completely stand-alone, it includes the CPU, that implements the control and the modulation, both full-bridges and the transient circuit, the sensors, the power supply for the logic and analog circuits and the output filter. Due to the complexity of the design and the number of components involved, three boards were designed: the control board, the power board and the output stage board.

4.7.1 Control board

The control board is a daughter board for the Power one. It was designed to fit in a DIM100 socket in order to change the CPU without redesigning the power circuits. The control board embeds the DSC TMS320F28335, a 150MHz, 32bit processor by Texas Instruments. The high number of PWM channels (12) and Analog to Digital Converter Channels (16) along with the floating point unit make it possible to implement complex algorithms.

Along with the CPU, the control board embeds the voltage regulator (3.3V for the peripherals and 1.9V for the core) and the protection circuit for the ADC.

The complete schematic and PCB are found in Appendices A1.1 and A1.2.

4.7.2 Power board

The power board incorporates the active devices, the DC Links, the driving circuits and the DSP socket with I/O circuitry.

DSP Socket

The Power card embeds the DSP socket with additional I/O circuits. The socket conveys to the DSP the analog signals, the 5V power supply and the various I/O and PWM ports that operate the converter.

As I/O interfaces, the Power board embeds a 10 bit Digital to Analog Converter (DAC) TLV5631, a RS485 transciever SN75LBC182D and various general purpose

connectors. The complete schematic is found in appendix A1.3.

Gate drivers

In order to have a very flexible control on every power device, the gate driver circuit is composed of an optocoupler and an insulated power supply for every power device.

The chosen optocoupler is the Allegro ACPL-J313. The insulated power supply is generated by the IC MAX256 that drives a 1:2 transformer followed by a voltage multiplier. The schematic is illustrated in Fig. 4.20. The PWM signal is generated by the DSP and it enters in a AND gate with the signal generated by the fault circuit. The fault circuit is a latch that, in case of overcurrent, forces to zero its output, consequently disabling all the logic gates.

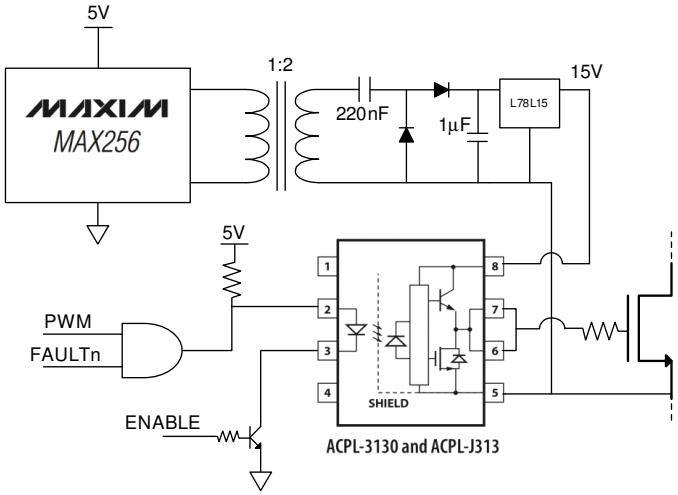


Figure 4.20: Gate driver circuit with insulated power supply.

The logic gates are in open drain configuration. In this way the current absorbed by the photodiodes is given by the 5V power supply and not by the logic gates itself. This, however, poses a problem in case of malfunctioning or non-uniform turn on of the devices. As a matter of fact, if the logic gate is not powered, every photodiode is conducting due to the pull-up resistor. For this reason, every cathode of the gate

drivers is connected to the collector of a BJT. Only if the BJT is polarized it is possible to turn on the gate drivers.

The complete schematic of the 11 gate drivers is reported in appendix A1.4.

Power section

The power section embeds the two full-bridges and the transient circuit. In order to prevent overvoltages, turn-off RC snubbers are present in every controlled device.

The power section features also a relay that connects the flying capacitor to the DC link through a power resistor. In this way it is possible to charge the flying capacitor to a particular voltage, as the chosen power resistor allows a fairly slow charge.

The DC link voltages are measured by a circuit (reported in Fig. 4.21) that employs a linear optocoupler, the Avago HCNR201. The two operational amplifiers act as a voltage to current and as current to voltage converters. The feedback controls the LED embedded in the optocoupler to force the photodiodes to work in the linear region.

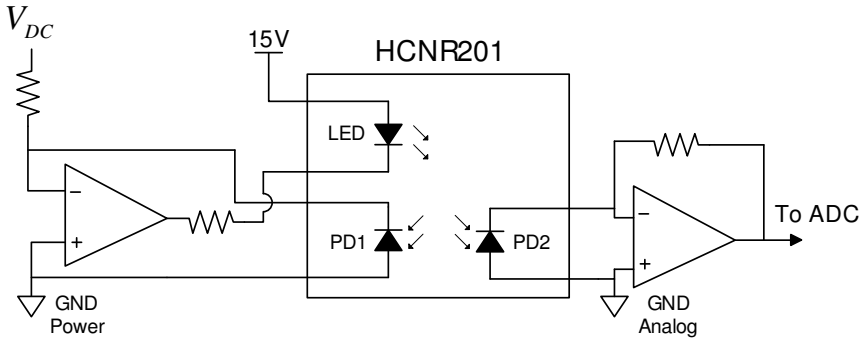


Figure 4.21: Circuit employed to measure the DC Link voltages with the optolinear coupler.

The complete schematic of the power section is reported in appendix A1.5, and the complete PCB of the power board is shown in appendix A1.6.

4.7.3 Output Stage Board

Power supply

In order to generate all the supply voltages needed for the converter, a flyback based on the IC TOP257-PN was designed. Fig. 4.22 shows an example of the general flyback circuit. The controller incorporates an active switch used to drive the primary of the transformer. The DC supply is obtained by a simple diode bridge rectifier, allowing it to be used with DC or AC sources.

An optocoupler carries the feedback signal of the controlled output voltage (5V) to the TOP257-PN.

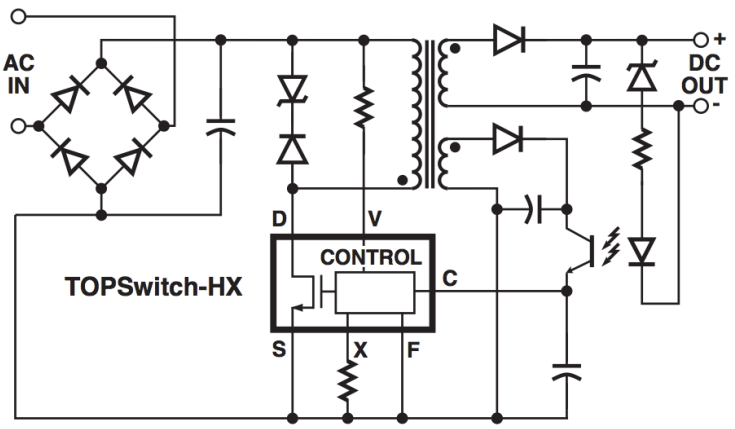


Figure 4.22: Example circuit of the flyback converter from the TOP257-PN datasheet.

Appendix A1.7 shows the complete shcematic of the realized flyback converter. Along with the regulated 5V, additional windings for the +17V and -17V (used by the analog circuits) were added to the design. Also an auxiliary winding for the operation of the TOP257-PN and an isolated +15V are present. It is important to note that the 5V is the only output regulated by the flyback controller, the other outputs can vary their voltage depending on the duty cycle variations of the IC due to varying load. For this reason, to ensure the stability of the power supplies, the unregulated outputs are followed by linear regulators.

Output filter

The output filter connects the active devices to the grid and includes the sensors needed for the grid current control. Fig. 4.23 shows the basic schematic of the output filter. The capacitor C_f is the grid current filter capacitor. A couple of relays insulate the converter from the grid which is coupled to the converter with a filter composed of a two stage common mode inductor and C_x-C_y capacitors. An LEM CKSR-25NP is employed as a current transducer and a voltage transformer is used to measure the grid voltage.

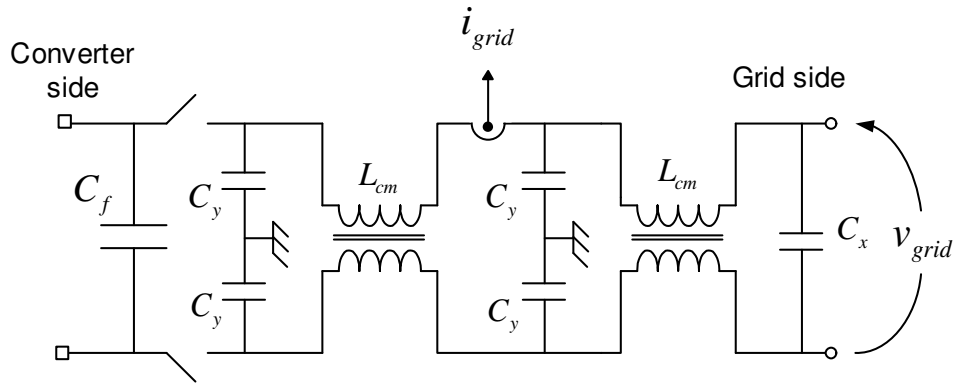


Figure 4.23: Schematic of the output filter.

In order to comply with the regulations that supervise the grid connection of photovoltaic inverters, the so called "intrinsic safety" is needed. In other words, the connection of the converter to the grid must be prevented if the grid voltage is absent. In this way, it is impossible for the grid to be energized even in case of a malfunction of the converter logic.

In this project a specific circuit was developed. A diode bridge rectifier is added at the output of the voltage transformer employed to sense the grid voltage, and the rectified voltage is connected to the base of a BJT. This latter transistor is connected in series to the winding of the relay, and if kept off, it prevents the energization of the relay winding, and consequently the connection to the grid.

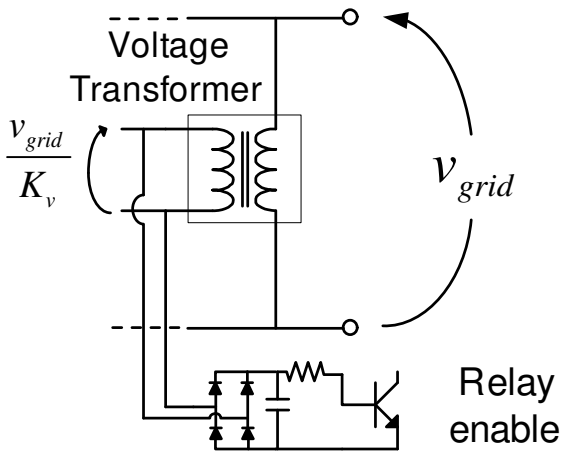


Figure 4.24: Intrinsic safety circuit.

As explained in 4.2 it is mandatory for the correct operation of the converter that the line-switching frequency leg of the HVFB is connected to the neutral conductor. For this reason the converter must check if the grid is correctly connected before starting the operation.

In fact, the correct connection can be checked by measuring the difference of potential between the presumed neutral conductor and earth, as in the MV/LV transformer the neutral conductor is earth-connected. This operation, however, is not trivial, as, in order to be compliant with the international regulations, the converter must pass the electric safety tests. One of these consists in applying a 3kV DC voltage between earth and the line conductors. For this reason a simple transformer cannot be employed to measure the voltage difference.

In the converter developed for this thesis, a relay was employed to connect an optocoupler between the presumed neutral and earth. If enough current is circulating, it means that the phase and neutral conductor are swapped, and the phototransistor will conduct. The output of the phototransistor is connected with a low pass filter to the ADC of the DSP, which will prevent the converter from starting if the wrong connection is detected.

The complete schematics of the output filter are reported in appendix A1.8, and

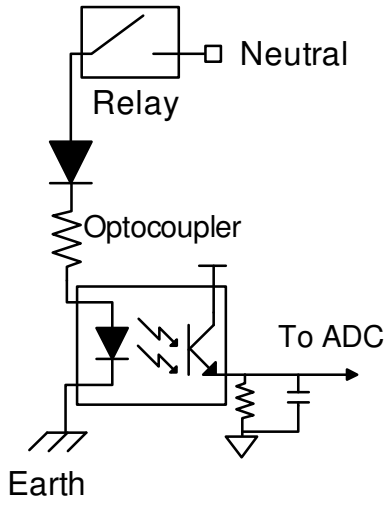


Figure 4.25: Circuit for the phase-neutral detection.

the PCB is reported in appendix A1.9.

Fig. 4.26 presents a picture of the boards. The layout of the screws was realized to stack the output board on the top of the power board. Fig. 4.27 shows the completed result.

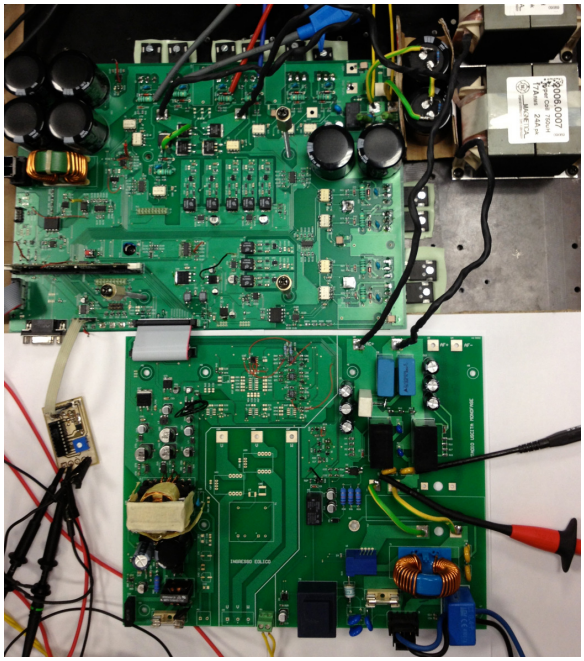


Figure 4.26: Picture of the prototype with the boards separated.

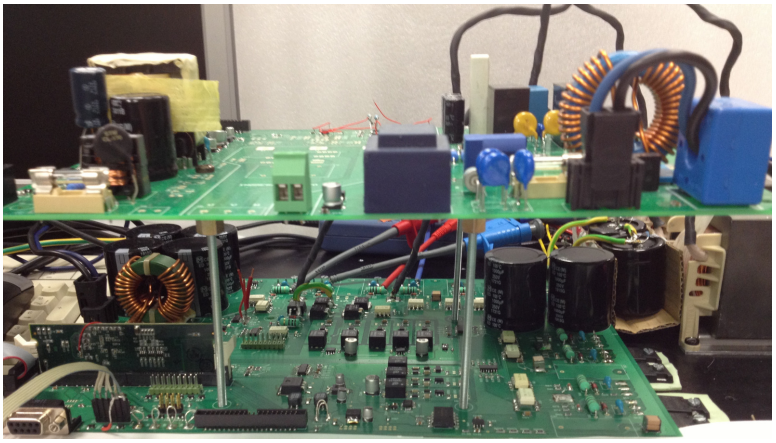


Figure 4.27: Picture of the prototype with the stacked boards.

4.8 Experimental results

A specific test bed was realized in order to test the performance of the realized inverter in terms of ground leakage current and current distortion. Fig. 4.28 shows a scheme of this test bed. The nine level inverter was connected to a DC source and directly connected to the grid.

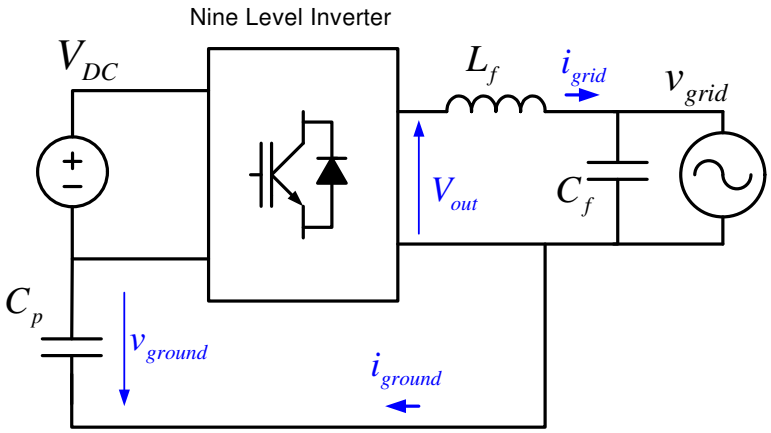


Figure 4.28: Experimental test bed.

Different tests were performed with different values of power factor to show the correct operation regardless the phase displacement of the output current with respect to the grid voltage. For these tests, 2kW output ($i_{grid} = 8.5A_{RMS}$) power was chosen. The grid voltage was $v_{grid} = 230V_{RMS}$. The current control chosen was the PI in synchronous reference frame, due to the very low steady state error. The control is executed at $f_s = 20kHz$, as in the simulations. Even the other parameters remain the same.

Fig. 4.29 and Fig. 4.30 show the output voltage and current of the converter when $V_{fc} = 0.5V_{DC}$. As a matter of fact, seven output voltage levels are correctly synthesized with unity power factor or PF=0.85 (Fig. 4.31 and Fig. 4.32).

In Fig. 4.33 and Fig. 4.34 the previous tests were repeated with $V_{fc} = 0.33V_{DC}$, allowing to obtain a nine level output voltage.

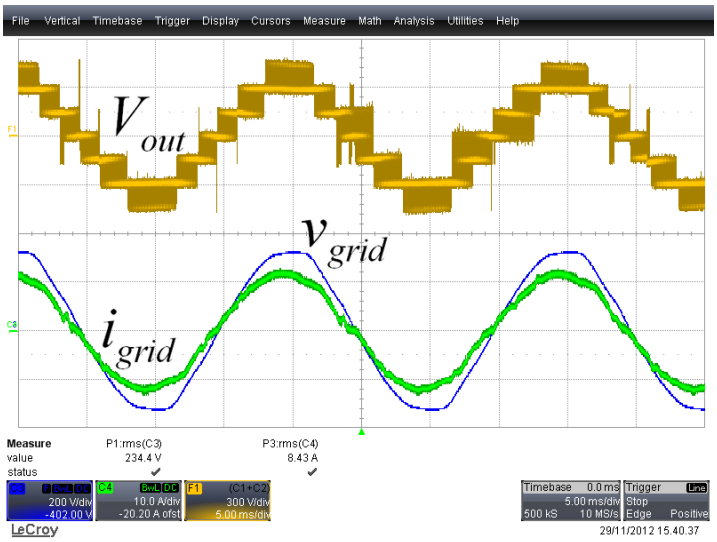


Figure 4.29: Converter output voltage and current with $V_{fc} = 0.5V_{DC}$ and unity power factor.

Nine level output voltages can also be realized when $V_{fc} = 0.66V_{DC}$. Fig. 4.35, 4.36, 4.37, 4.38 show the behavior of the converter with different power factors.

From the analysis of the experimental results, it is clear that the balancing mechanism of the DC voltages allows to control very well the flying capacitor voltage. Also several points of the controllability area of Fig. 4.6 were experimentally tested. A very good agreement of the simulations and the experiments was witnessed, although differences appear due to the distortion in the grid voltage.

The distortion of the grid voltage, that is clear in the above oscilloscope captures, is one of the main causes of the grid current distortion. In fact, the d-q current control presents infinite gain only at the grid frequency. As the grid voltage presents a marked third harmonic content, low frequency oscillation happens due to the finite bandwidth.

Moreover, it can be said that the current distortion when $V_{fc} = 0.33V_{DC}$ is greater than the case when $V_{fc} = 0.66V_{DC}$. This is due to the effect of the dead times between the commutation of the full-bridge legs. As it was shown in literature, narrow pulses

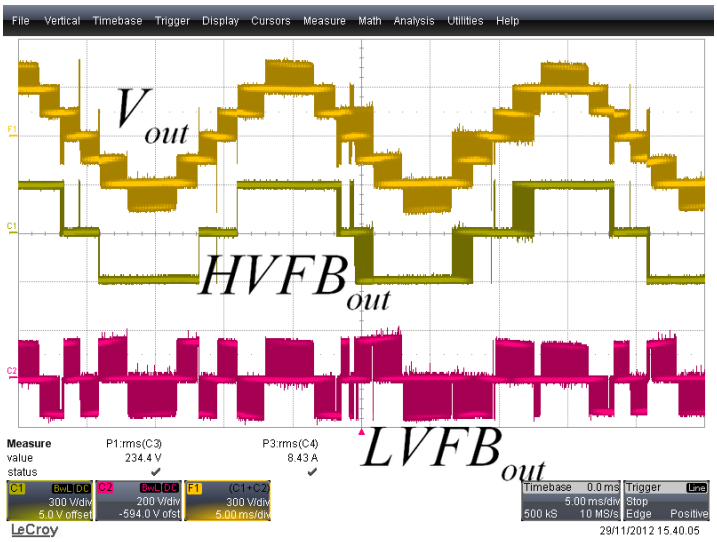


Figure 4.30: HVFB and LVFB output voltages with $V_{fc} = 0.5V_{DC}$ and unity power factor.

lead to a greater current distortion. When operating at $V_{fc} = 0.33V_{DC}$, the output is represented by nine level adjacent level, i.e. the maximum energy efficiency and the minimum high-frequency current distortion. However, for each operating zone, the duty cycles reach the 0% or 100% when entering and exiting the zone. As a consequence, crossover distortion appears.

When operating at $V_{fc} = 0.66V_{DC}$, the zone choice allows to never employ extreme values of duty cycles and the crossover distortion is greatly reduced.

As a comparison, the same waveforms of the previous test are reported in the case of a unipolar three-level converter in Fig. 4.39. For this test, the DC Link was $V_{DC} = 400V$ and all the other parameters were kept the same (i.e., switching frequency, output filter, current controller).

Finally, the operation of the transient circuit was evaluated with a parasitic capacitance of 200nF connected between the virtual earth and the negative pole of the DC Link, as shown in Fig. 4.28. The same parameters of the simulation were chosen, except for the impedance of the neutral conductor. The results of Fig. 4.40 are

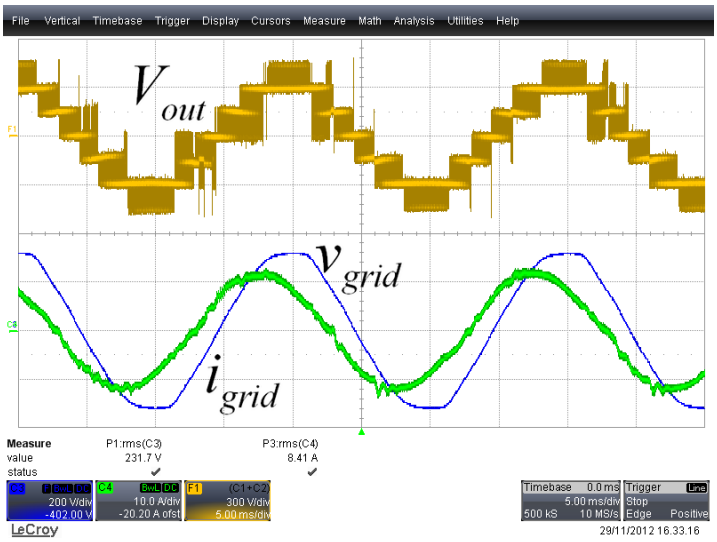


Figure 4.31: Converter output voltage and current with $V_{fc} = 0.5V_{DC}$ and PF=0.85.

in agreement with the simulations of Fig. 4.19, leading to a ground leakage current of about 31 mA. Although the waveform of i_{ground} appears with higher values than the simulations, in fact it is the disturbances linked with the probe when the HVFB is switching. If the waveform was magnified, it would be clear that that disturbance has a negligible RMS. Anyway, further tuning and common mode filter design can reduce the ground leakage current.

As reference, Fig. 4.41 shows the common mode voltage in the case of unipolar PWM. As expected, v_{cm} presents high frequency common mode voltage variations, that render impossible its straightforward application to transformerless inverters.

Finally, some efficiency and THD results are reported in TABLE 4.2. For the proposed topology it was chosen the case $V_{DC} = 300V$ and $V_{fc} = 150V$, while for the unipolar PWM it was $V_{DC} = 400V$. As a matter of fact, although the unipolar PWM test conditions are advantageous (inferior total DC Link voltage and frequency of the output current ripple twice the switching one), the THD performance are lower with respect to the proposed topology.

While the high-frequency content is similar due to the particular test conditions,

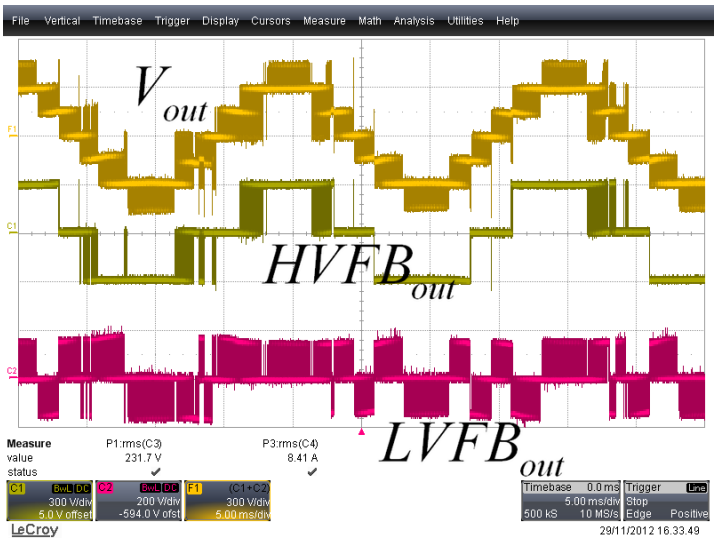


Figure 4.32: HVFB and LVFB output voltages with $V_{fc} = 0.5V_{DC}$ and PF=0.85.

the mandatory dead times have a greater effect, as the voltage at which the commutations happen is greater and the voltage loss due to dead times is higher. This leads to more low frequency distortion.

The efficiency of the proposed architecture is higher than the unipolar solution, despite having four devices always in conduction. In these tests even for the proposed converter all IGBTs were chosen as power devices. If MOSFETs with slow body diode were to be employed, it is estimated that the efficiency could grow by 1 %.

Table 4.2: Efficiency η and THD experimental measures

Architecture	**1 kW η**	**2 kW η**	**2 kW THD**
Proposed Topology	0.975	0.968	4.17 %
Unipolar PWM	0.969	0.966	6.91 %

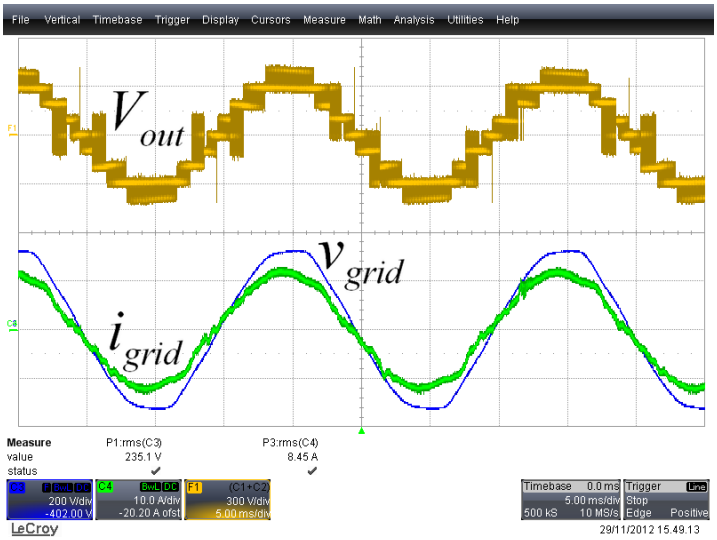


Figure 4.33: Converter output voltage and current with $V_{fc} = 0.33V_{DC}$ and unity power factor.

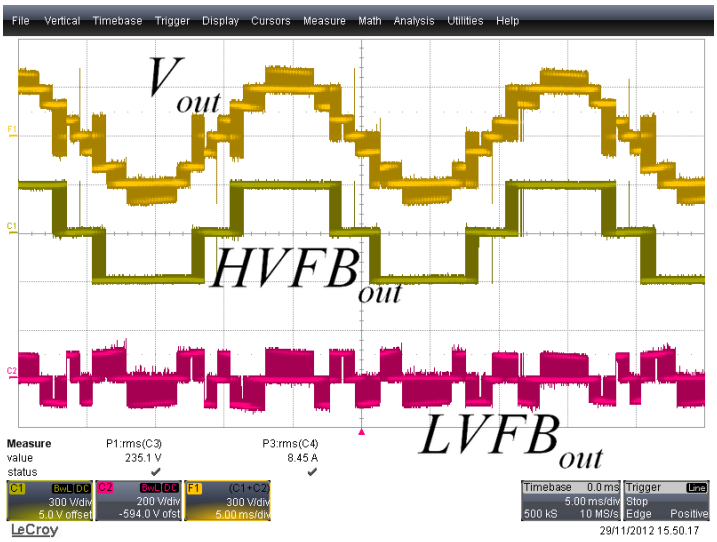


Figure 4.34: HVFB and LVFB output voltages with $V_{fc} = 0.33V_{DC}$ and unity power factor.

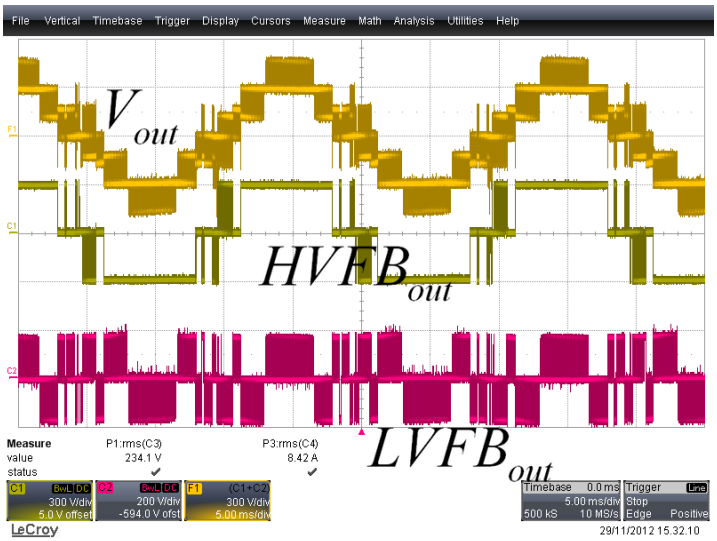


Figure 4.35: Converter output voltage and current with $V_{fc} = 0.66V_{DC}$ and unity power factor.

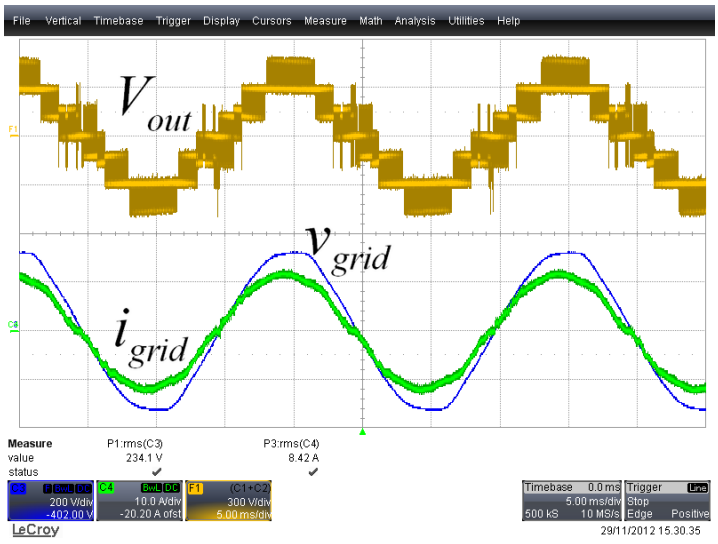


Figure 4.36: HVFB and LVFB output voltages with $V_{fc} = 0.66V_{DC}$ and unity power factor.

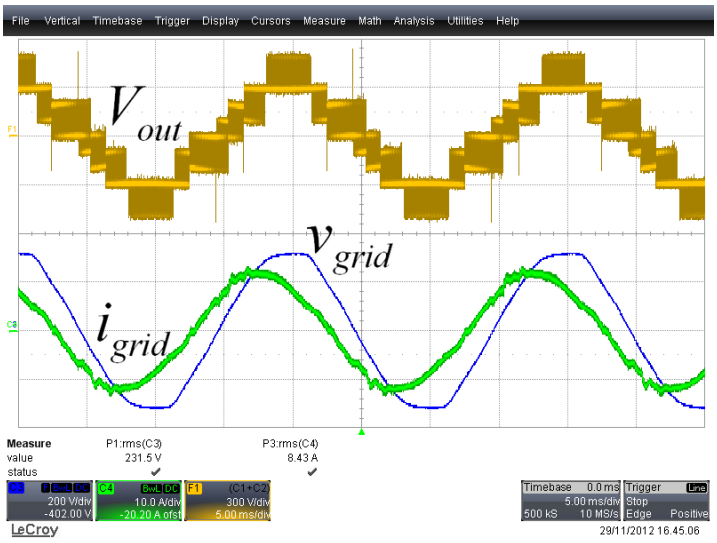


Figure 4.37: Converter output voltage and current with $V_{fc} = 0.66V_{DC}$ and PF=0.85.

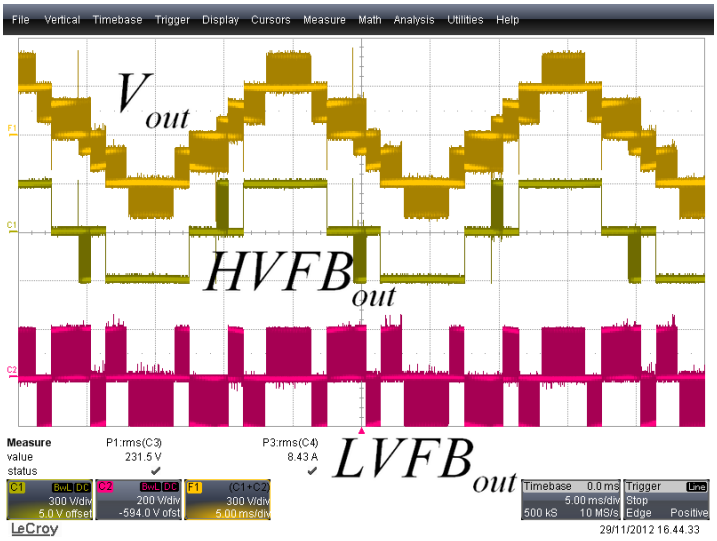


Figure 4.38: HVFB and LVFB output voltages with $V_{fc} = 0.66V_{DC}$ and PF=0.85.

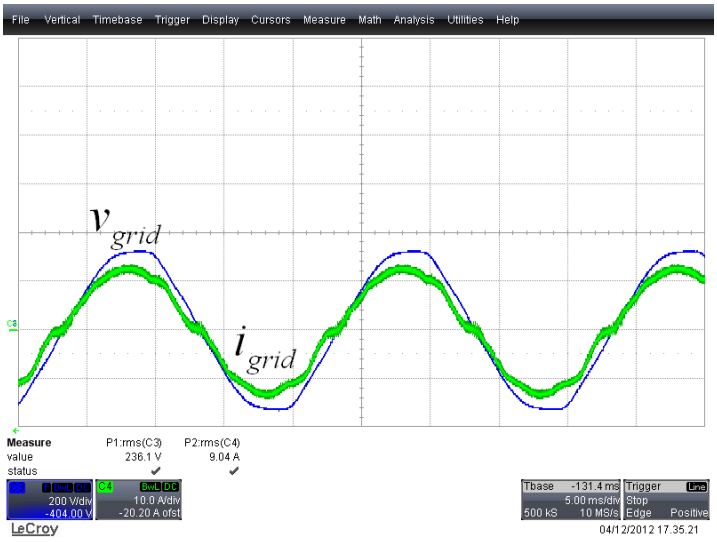


Figure 4.39: Grid current and voltage in case of unipolar PWM and PF=0.1.

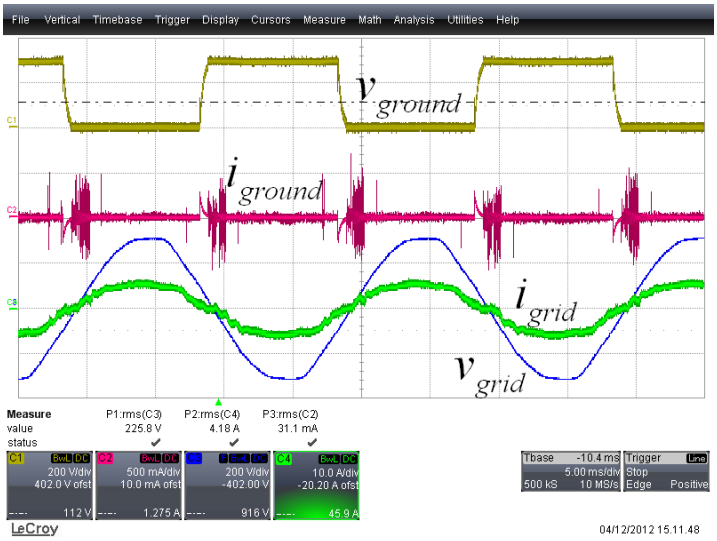


Figure 4.40: Common mode voltage at the output of the converter in case of unipolar PWM.

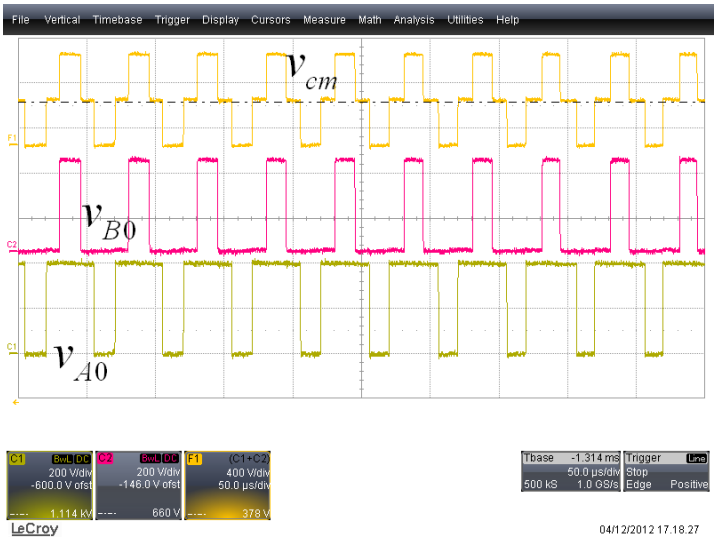


Figure 4.41: Common mode voltage at the output of the converter in case of unipolar PWM.

Chapter 5

Conclusions

In this thesis several topologies of transformerless grid-connected inverters and multilevel converters were analyzed, highlighting drawbacks and strengths. A novel converter was proposed and evaluated in terms of grid current quality and ground leakage current.

The proposed converter relies on the well known cascaded full-bridge topology, where one of the full-bridges is supplied by a flying capacitor. An appropriate PWM strategy was developed to reduce the switching losses and the ground leakage current, that represent a problem of paramount importance in PV-fed grid-connected power converters.

The key characteristics of the realized inverter are:

- Up to nine level output voltage waveform, that allows to reduce the output current ripple due to the switching.
- Extended power factor operations.
- Arbitrary DC voltage ratio with unaffected ability to synthesize the desired output voltage. In fact, even when during a transient the converter enters an unstable flying capacitor voltage area, the output voltage generation is unaffected.

- Intrinsic boost capabilities, as the charging of the flying capacitor extends the input voltage sufficient to control the grid current.
- Possibility to employ MOSFETs with slow body diode to reduce the conduction losses.
- The Transient Circuit allows to keep low levels of ground leakage current.

The proposed solution presents some drawbacks:

- The topology presents an increased component count with respect to the state of the art.
- During the active phase, there are always four devices conducting, limiting the maximum obtainable efficiency.
- The continuous power transfer between the HVFB and LVFB can reduce the lifetime of the flying capacitor.

Simulations and experimental results show that the proposed converter allows to obtain very good performance regarding grid current distortion and can represent a feasible solution for PV-fed inverter systems.

Bibliography

[1] Xiao Huafeng and Xie Shaojun. Leakage Current Analytical Model and Application in Single-Phase Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Transactions on Electromagnetic Compatibility*, 52(4):902 –913, November 2010.

[2] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy. Eliminating Ground Current in a Transformerless Photovoltaic Application. *IEEE Transactions on Energy Conversion*, 25(1):140 –147, March 2010.

[3] M. Cacciato, A. Consoli, R. Attanasio, and F. Gennaro. Soft-Switching Converter With HF Transformer for Grid-Connected Photovoltaic Systems. *IEEE Transactions on Industrial Electronics*, 57(5):1678 –1686, May 2010.

[4] C. Rodriguez and G.A.J. Amaratunga. Long-Lifetime Power Inverter for Photovoltaic AC Modules. *IEEE Transactions on Industrial Electronics*, 55(7):2593 –2601, July 2008.

[5] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg. Control of single-stage single-phase PV inverter. In *European Conference on Power Electronics and Applications*, September 2005.

[6] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg. Multiresonant Frequency-Locked Loop for Grid Synchronization of Power

Converters Under Distorted Grid Conditions. *IEEE Transactions on Industrial Electronics*, 58(1):127 –138, January 2011.

[7] M. Liserre, F. Blaabjerg, and S. Hansen. Design and control of an LCL-filter-based three-phase active rectifier. *IEEE Transactions on Industry Applications*, 41(5):1281 – 1291, September 2005.

[8] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg. Evaluation of Current Controllers for Distributed Power Generation Systems. *IEEE Transactions on Power Electronics*, 24(3):654 –664, March 2009.

[9] T. Hornik and Q. C. Zhong. H infinite repetitive voltage control of grid connected inverters with a frequency adaptive mechanism. *IET Power Electronics*, 3(6):925–935, November 2010.

[10] M. Odavic, V. Biagini, P. Zanchetta, M. Sumner, and M. Degano. One-sample-period-ahead predictive current control for high-performance active shunt power filters. *IET Power Electronics*, 4(4):414 –423, April 2011.

[11] Shuitao Yang, Qin Lei, F.Z. Peng, and Zhaoming Qian. A Robust Control Scheme for Grid-Connected Voltage-Source Inverters. *IEEE Transactions on Industrial Electronics*, 58(1):202 –212, January 2011.

[12] Mei Qiang, Shan Mingwei, Liu Liying, and J. M. Guerrero. A Novel Improved Variable Step-Size Incremental-Resistance MPPT Method for PV Systems. *IEEE Transactions on Industrial Electronics*, 58(6):2427 –2434, June 2011.

[13] R. Kadri, J. P. Gaubert, and G. Champenois. An Improved Maximum Power Point Tracking for Photovoltaic Grid-Connected Inverter Based on Voltage-Oriented Control. *IEEE Transactions on Industrial Electronics*, 58(1):66 –75, January 2011.

[14] B. Subudhi and R. Pradhan. A Comparative Study on Maximum Power Point Tracking Techniques for Photovoltaic Power Systems. *IEEE Transactions on Sustainable Energy - In press, available on IEEE Early Access*.

[15] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli. Leakage Current Reduction in a Single-Phase Bidirectional AC/DC Full-Bridge Inverter. *IEEE Transactions on Power Electronics*, 27(10):4281 –4291, October 2012.

[16] Wensong Yu, Jih-Sheng Lai, Hao Qian, and C. Hutchens. High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Nonisolated AC-Module Applications. *IEEE Transactions on Power Electronics*, 26(4):1253 –1260, April 2011.

[17] B. Gu, J. Dominic, J. Lai, C. Chen, and B. Chen. High Reliability and Efficiency Single-Phase Transformerless Inverter for Grid-Connected Photovoltaic Systems. *IEEE Transactions on Power Electronics*, 57(9):3118 –3128, May 2013.

[18] Xiao Huafeng, Xie Shaojun, Chen Yang, and Ruhai Huang. An Optimized Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Transactions on Industrial Electronics*, 58(5):1887 –1895, May 2011.

[19] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas. A New High-Efficiency Single-Phase Transformerless PV Inverter Topology. *IEEE Transactions on Industrial Electronics*, 58(1):184 –191, January 2011.

[20] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo. Transformerless Inverter for Single-Phase Photovoltaic Systems. *IEEE Transactions on Power Electronics*, 22(2):693 –697, March 2007.

[21] G. Buticchi, D. Barater, E. Lorenzani, and G. Franceschini. Digital Control of Actual Grid-Connected Converters for Ground Leakage Current Reduction in PV Transformerless Systems. *IEEE Transactions on Industrial Informatics*, 8(3):563–572, August 2012.

[22] S. V. Araujo, P. Zacharias, and R. Mallwitz. Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems. *IEEE Transactions on Industrial Electronics*, 28(5):2235–2245, September 2010.

[23] Yunjie Gu, Wuhua Li, Yi Zhao, Bo Yang, Chushan Li, and Xiangning He. Transformerless Inverter With Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems. *IEEE Transactions on Power Electronics*, 28(2):973–805, February 2013.

[24] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, Wu Bin, J. Rodriguez, M. A. Perez, and J. I. Leon. Recent Advances and Industrial Applications of Multilevel Converters. *IEEE Transactions on Industrial Electronics*, 57(8):2553 –2580, August 2010.

[25] S. Daher, J. Schmid, and F. L. M. Antunes. Multilevel Inverter Topologies for Stand-Alone PV Systems. *IEEE Transactions on Industrial Electronics*, 55(7):2703–2712, July 2008.

[26] Liao Yi-Hung and Lai Ching-Ming. Newly-Constructed Simplified Single-Phase Multistring Multilevel Inverter Topology for Distributed Energy Resources. *IEEE Transactions on Power Electronics*, 26(9):2386–2392, September 2011.

[27] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas. Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems. *IEEE Transactions on Industrial Electronics*, 56(11):4399–4406, November 2009.

[28] Jih-Sheng Lai and Fang Zheng Peng. Multilevel converters-a new breed of power converters. *IEEE Transactions on Industry Applications*, 32(3):509 – 517, May 1996.

[29] J. Pou, R. Pindado, and D. Boroyevich. Voltage-balance limits in four-level diode-clamped converters with passive front ends. *IEEE Transactions Industrial Electronics*, 52(1):190 – 196, February 2005.

[30] A. Shukla, A. Ghosh, and A. Joshi. Control Schemes for DC Capacitor Voltages Equalization in Diode-Clamped Multilevel Inverter-Based DSTATCOM. *IEEE Transactions on Power Delivery*, 23(2):1139 –1149, April 2008.

[31] N. Celanovic and D. Boroyevich. A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. *IEEE Transactions on Power Electronics*, 15(2):242 –249, March 2000.

[32] A. Bendre, G. Venkataramanan, D. Rosene, and V. Srinivasan. Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation. *IEEE Transactions Industrial Electronics*, 53(3):718 – 726, June 2006.

[33] L. Zhang and S.J. Watkins. Capacitor voltage balancing in multilevel flying capacitor inverters by rule-based switching pattern selection. *IET Electric Power Applications*, 1(3):339 –347, May 2007.

[34] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo. Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter. *IEEE Transactions on Industrial Electronics*, 55(7):2694 –2702, July 2008.

[35] C. Cecati, F. Ciancetta, and P. Siano. A Multilevel Inverter for Photovoltaic Systems With Fuzzy Logic Control. *IEEE Transactions Industrial Electronics*, 57(12):4115 –4125, December 2010.

[36] Sung Geun Song, Feel Soon Kang, and Sung-Jun Park. Cascaded Multilevel Inverter Employing Three-Phase Transformers and Single DC Input. *IEEE Transactions Industrial Electronics*, 56(6):2005 –2014, June 2009.

[37] M. Malinowski, K. Gopakumar, J. Rodriguez, and M.A. Perez. A Survey on Cascaded Multilevel Inverters. *IEEE Transactions Industrial Electronics*, 57(7):2197 –2206, July 2010.

[38] Yiqiao Liang and C.O. Nwankpa. A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM. *IEEE Transactions on Industry Applications*, 35(5):1118 –1123, September 1999.

[39] J.I. Leon, R. Portillo, S. Vazquez, J.J. Padilla, L.G. Franquelo, and J.M. Carrasco. Simple Unified Approach to Develop a Time-Domain Modulation Strategy for Single-Phase Multilevel Converters. *IEEE Transactions Industrial Electronics*, 55(9):3239 –3248, September 2008.

[40] J.I. Leon, S. Vazquez, A.J. Watson, L.G. Franquelo, P.W. Wheeler, and J.M. Carrasco. Feed-Forward Space Vector Modulation for Single-Phase Multilevel Cascaded Converters With Any DC Voltage Ratio. *IEEE Transactions Industrial Electronics*, 56(2):315 –325, February 2009.

[41] Yun Zhang and Li Sun. An Efficient Control Strategy for a Five-Level Inverter Comprising Flying-Capacitor Asymmetric H-Bridge. *IEEE Transactions Industrial Electronics*, 58(9):4000 –4009, September 2011.

[42] D.A. Ruiz-Caballero, R.M. Ramos-Astudillo, S.A. Mussa, and M.L. Heldwein. Symmetrical Hybrid Multilevel DC-AC Converters With Reduced Number of Insulated DC Supplies. *IEEE Transactions Industrial Electronics*, 57(7):2307 –2314, July 2010.

[43] Sung-Jun Park, Feel-Soon Kang, Man Hyung Lee, and Cheul-U Kim. A new single-phase five-level PWM inverter employing a deadbeat control scheme. *IEEE Transactions on Power Electronics*, 18(3):831 – 843, May 2003.

[44] J. Selvaraj and N.A. Rahim. Multilevel Inverter For Grid-Connected PV System Employing Digital PI Controller. *IEEE Transactions Industrial Electronics*, 56(1):149 –158, January 2009.

[45] N.A. Rahim and J. Selvaraj. Multistring Five-Level Inverter With Novel PWM Control Scheme for PV Application. *IEEE Transactions Industrial Electronics*, 57(6):2111 –2123, June 2010.

[46] N.A. Rahim, K. Chaniago, and J. Selvaraj. Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System. *IEEE Transactions Industrial Electronics*, 58(6):2435 –2443, June 2011.

[47] S. S. Fazel, S Bernet, D. Krug, and K. Jalili. Design and Comparison of 4-kV Neutral-Point-Clamped, Flying-Capacitor, and Series-Connected H-Bridge Multilevel Converters. *IEEE Transactions on Industry Applications*, 43(4):1032 –1040, July 2007.

[48] A. Varschavsky, J. Dixon, M. Rotella, and L. Moran. Cascaded Nine-Level Inverter for Hybrid-Series Active Power Filter, Using Industrial Controller. *IEEE Transactions on Industrial Electronics*, 57(8):2761 –2767, August 2010.

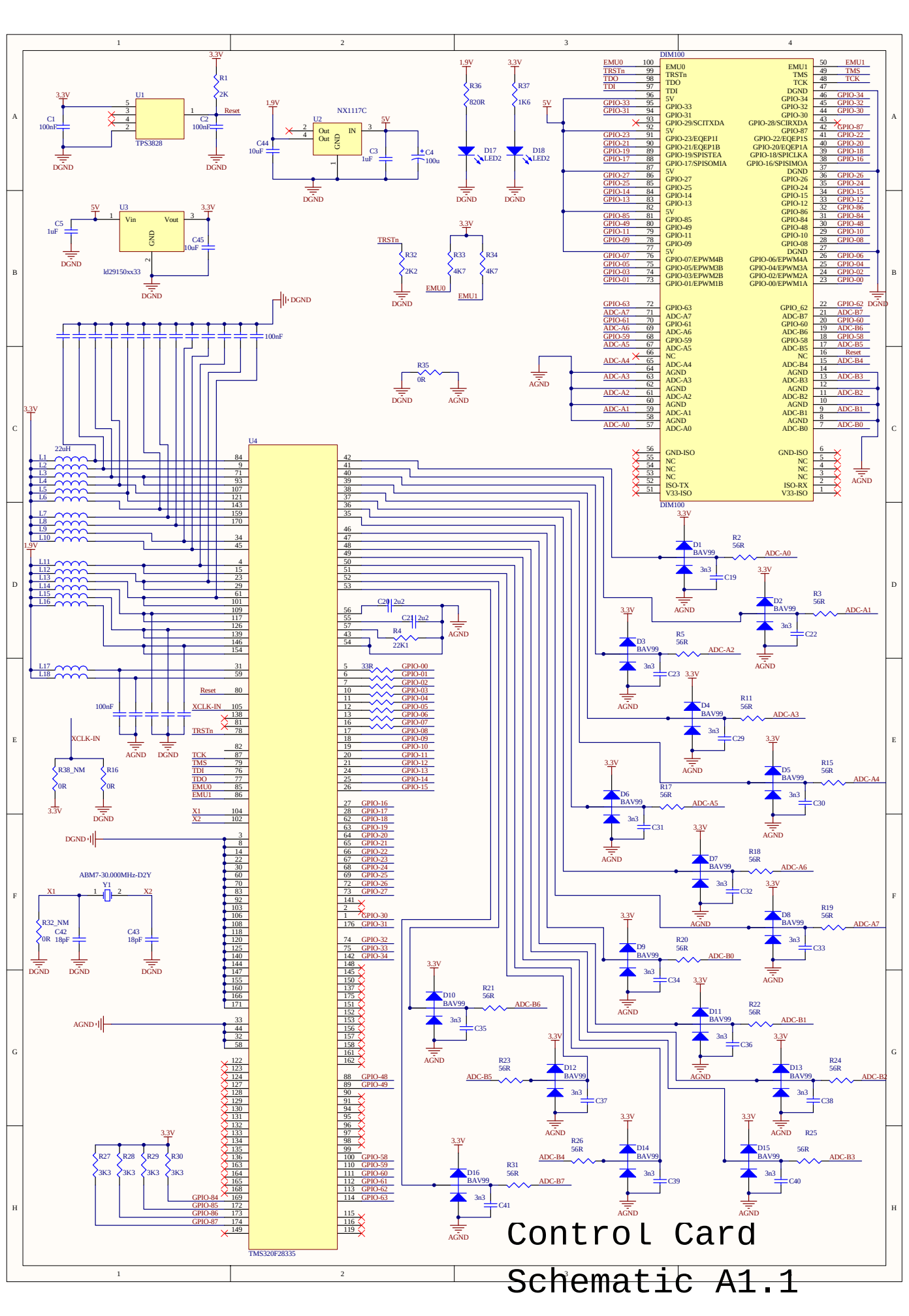
[49] V.M.E. Antunes, V.F. Pires, and J.F.A. Silva. Narrow Pulse Elimination PWM for Multilevel Digital Audio Power Amplifiers Using Two Cascaded H-Bridges as a Nine-Level Converter. *IEEE Transactions on Power Electronics*, 22(2):425 –434, March 2007.

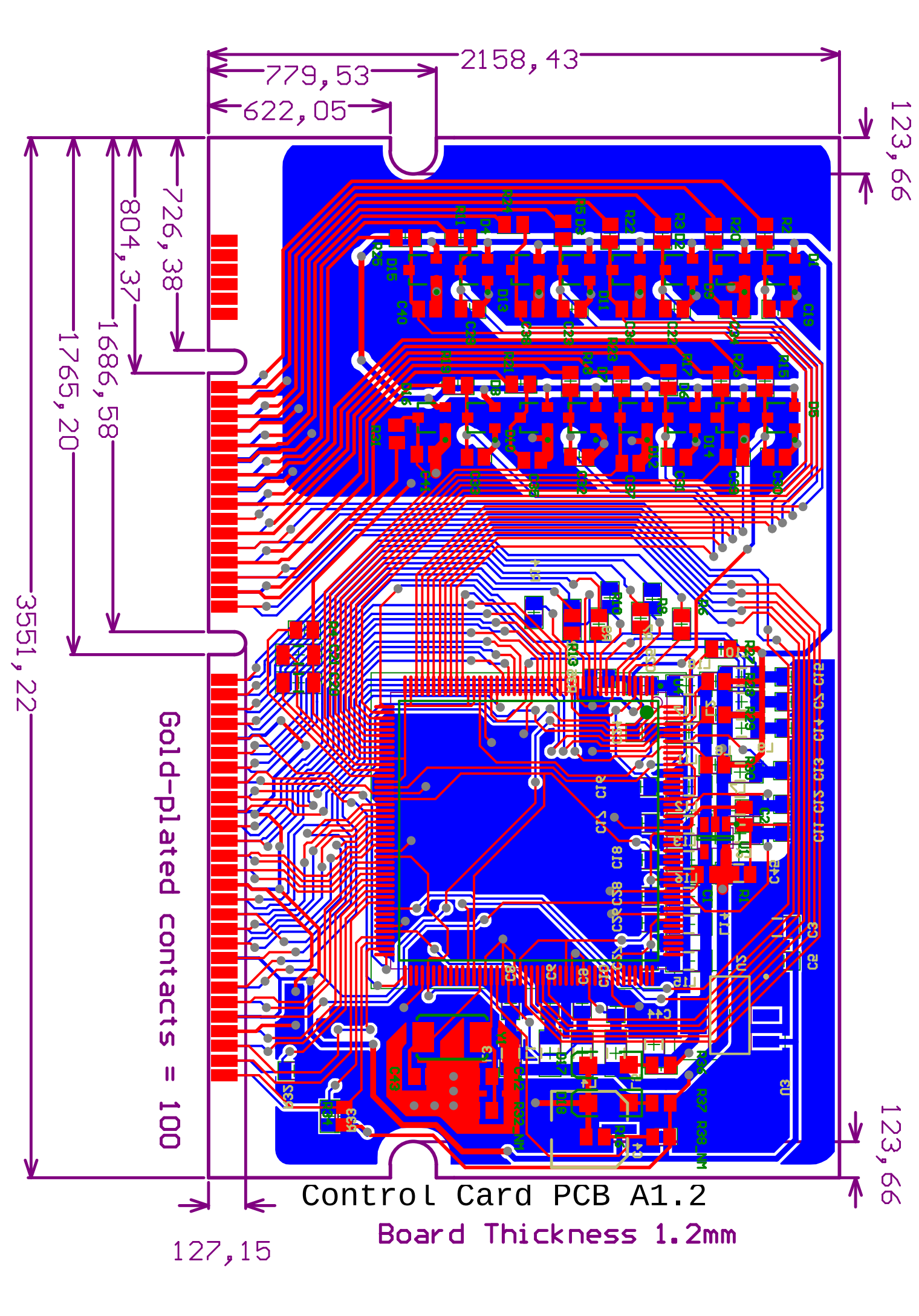
[50] D. A. B. Zambra, C. Rech, and J. R. Pinheiro. Comparison of Neutral-Point-Clamped, Symmetrical, and Hybrid Asymmetrical Multilevel Inverters. *IEEE Transactions on Industrial Electronics*, 57(7):2297 –2306, July 2010.

[51] S. P. Pimentel and J. A. Pomilio. Asynchronous distributed generation system based on asymmetrical cascaded multilevel inverter. In *IEEE IECON'08*, pages 3227 –3232, November 2008.

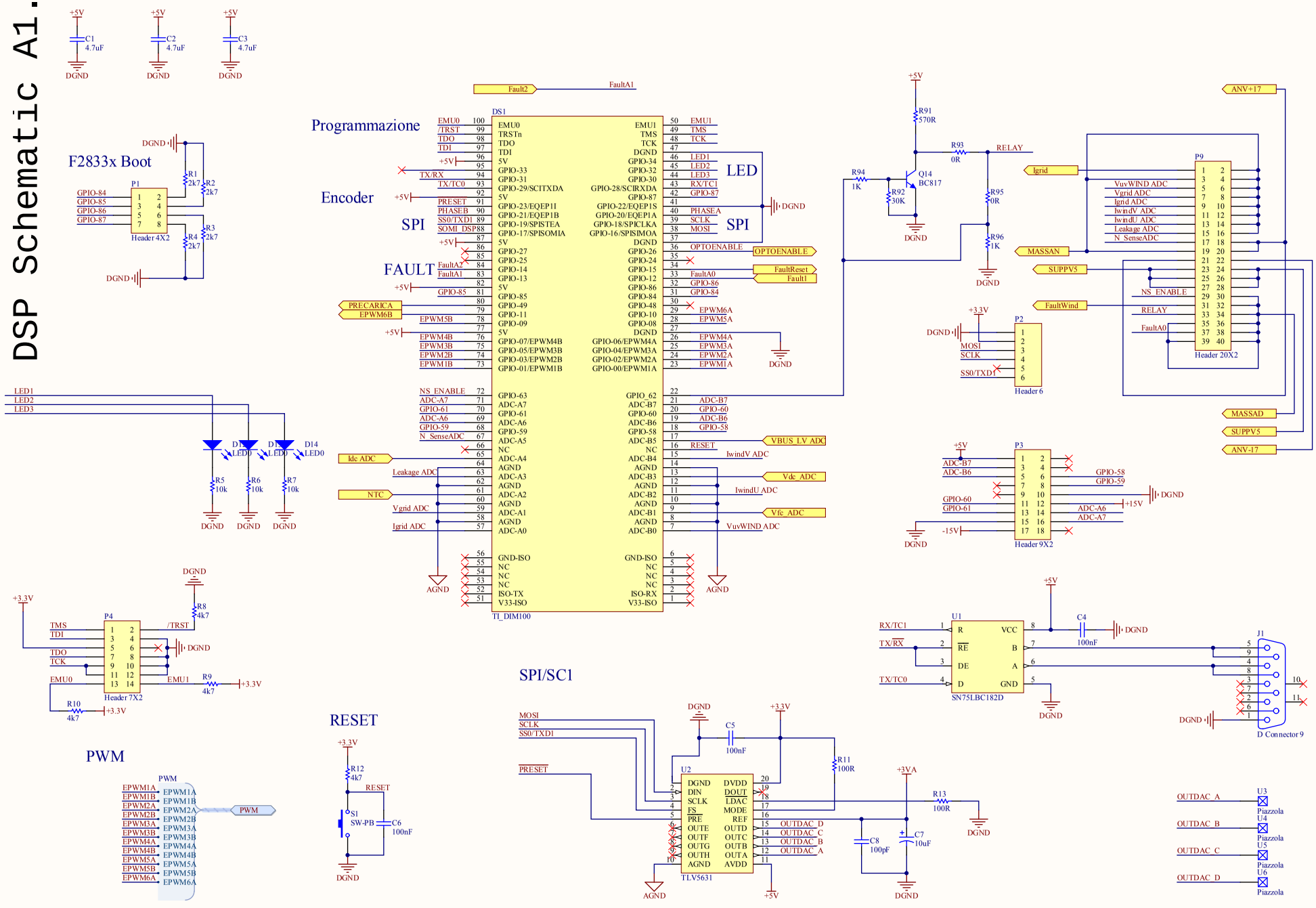
[52] Ebrahim Babaei and Seyed Hossein Hosseini. New cascaded multilevel inverter topology with minimum number of switches. *Energy Conversion and Management*, 50(11):2761 – 2767, November 2009.

[53] L. A. Silva, S. P. Pimentel, and J. A. Pomilio. Nineteen-level Active Filter System using Asymmetrical Cascaded Converter with DC Voltages Control. In *IEEE 36th Power Electronics Specialists Conference, PESC '05.*, pages 303 – 308, June 2005.

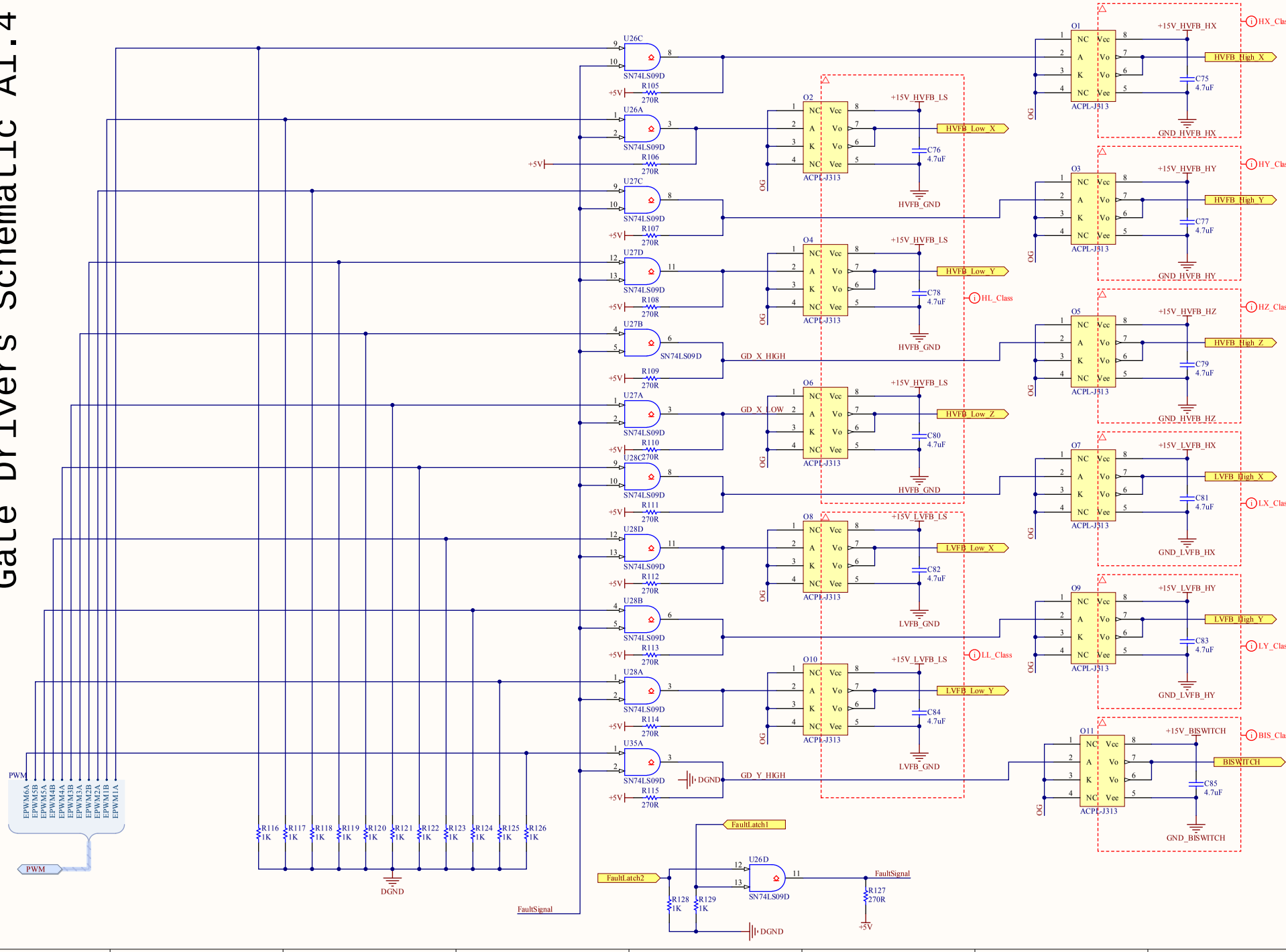

Control Card
Schematic A1.1

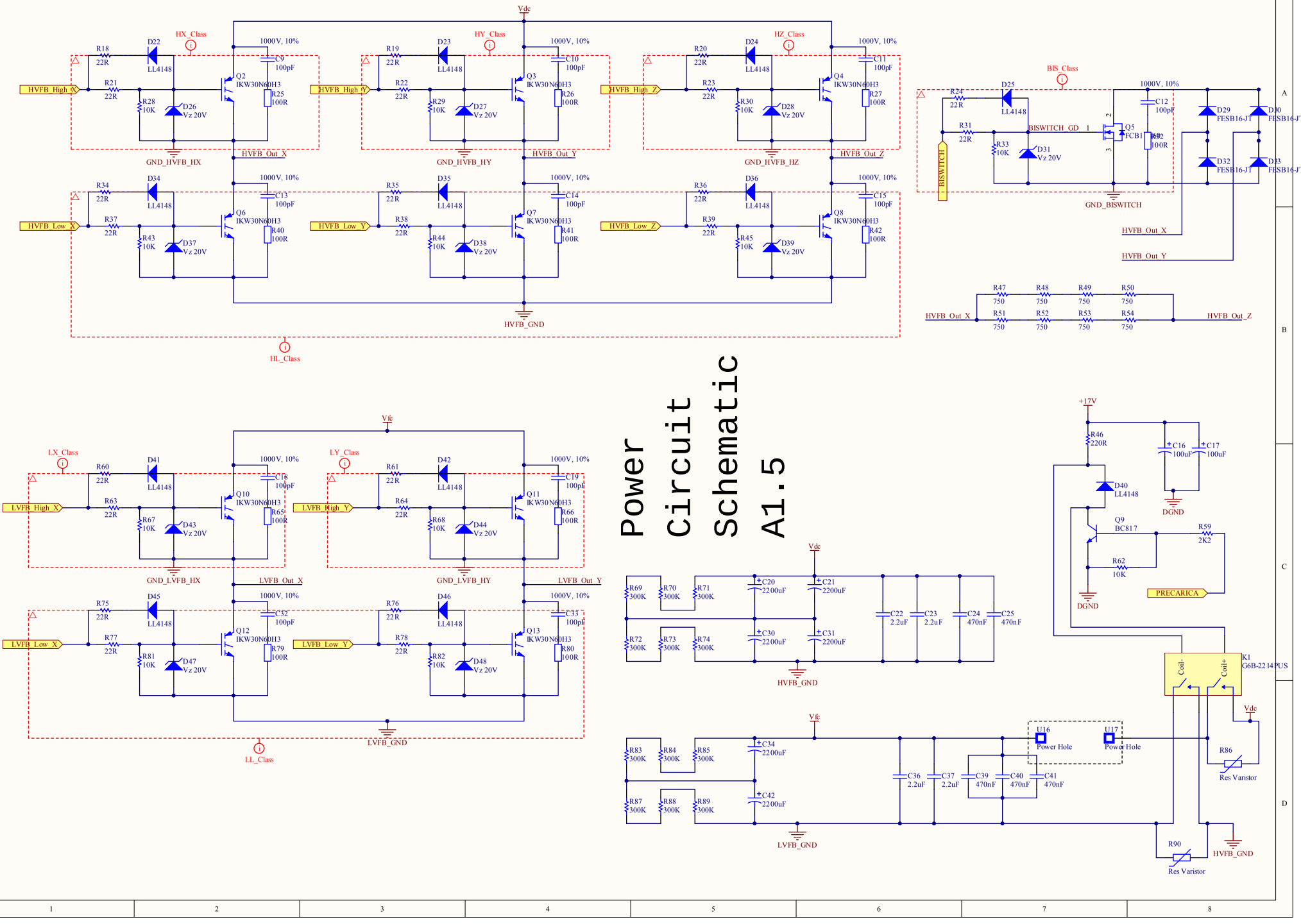

2158,43
779,53
622,05
123,66
804,37
726,38
1765,20
1686,58
3551,22
Gold-plated contacts = 100
123,66
Control Card PCB A1.2
Board Thickness 1.2mm
127,15

DSP Schematic A1.3

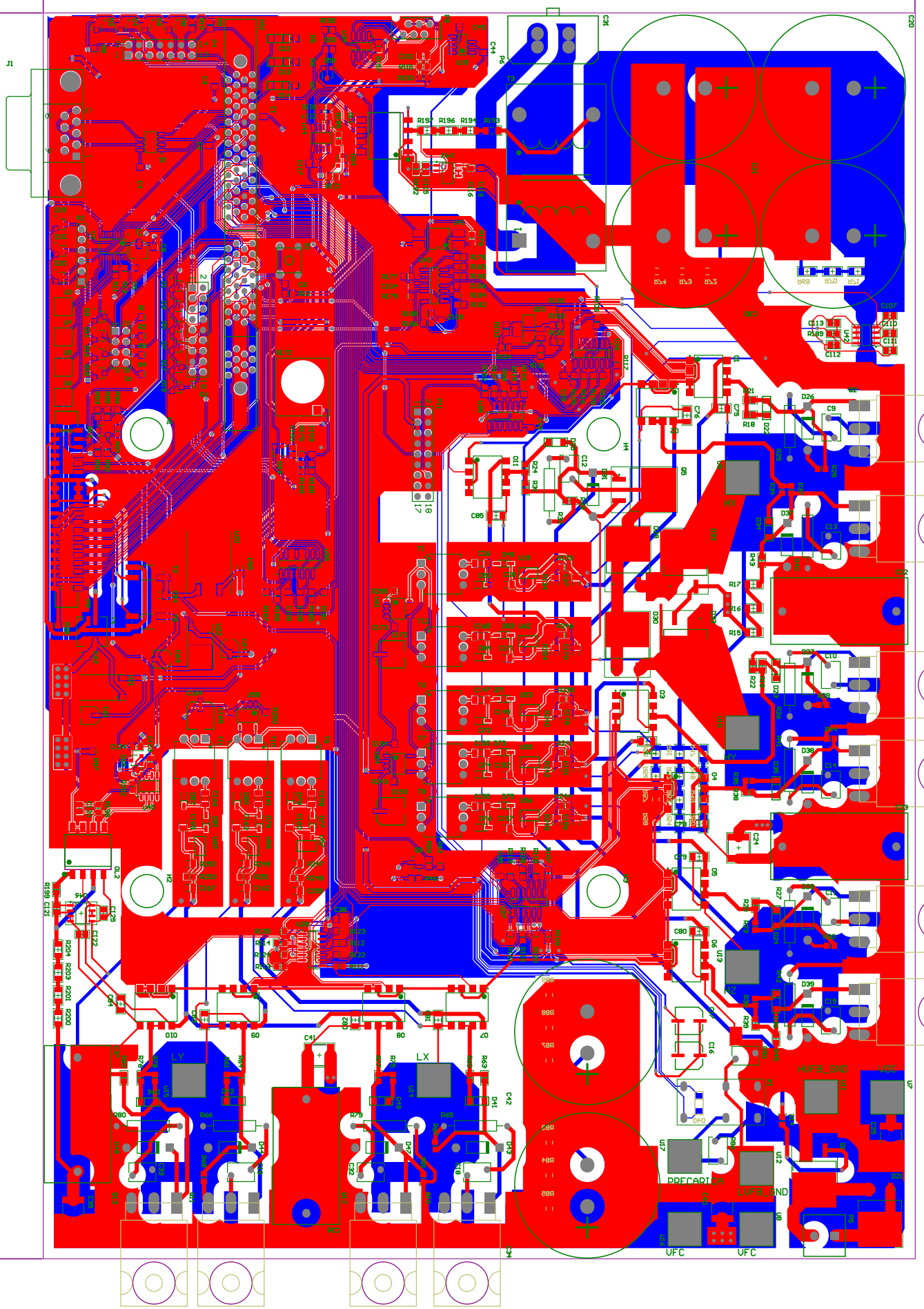


Gate Drivers Schematic A1.4

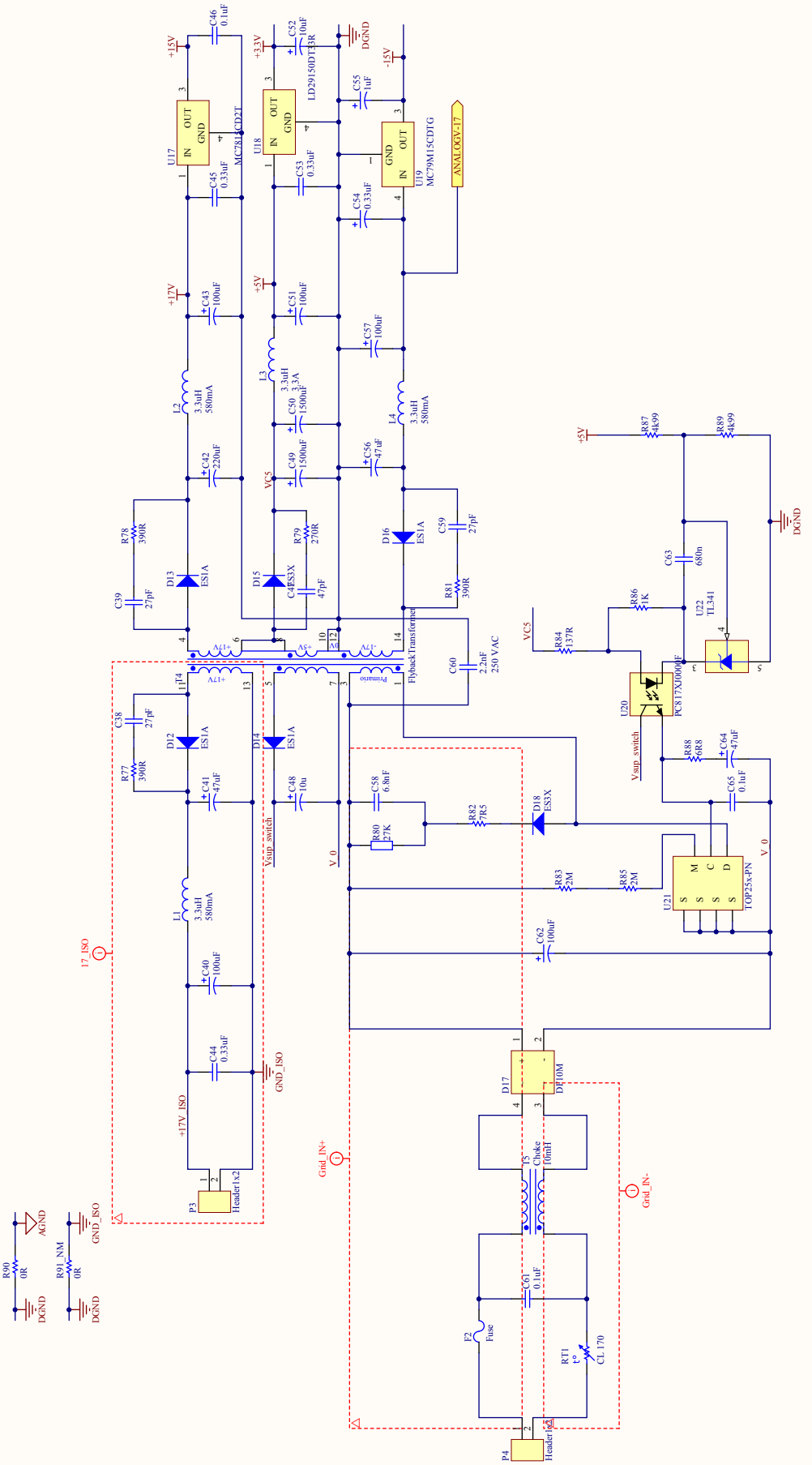


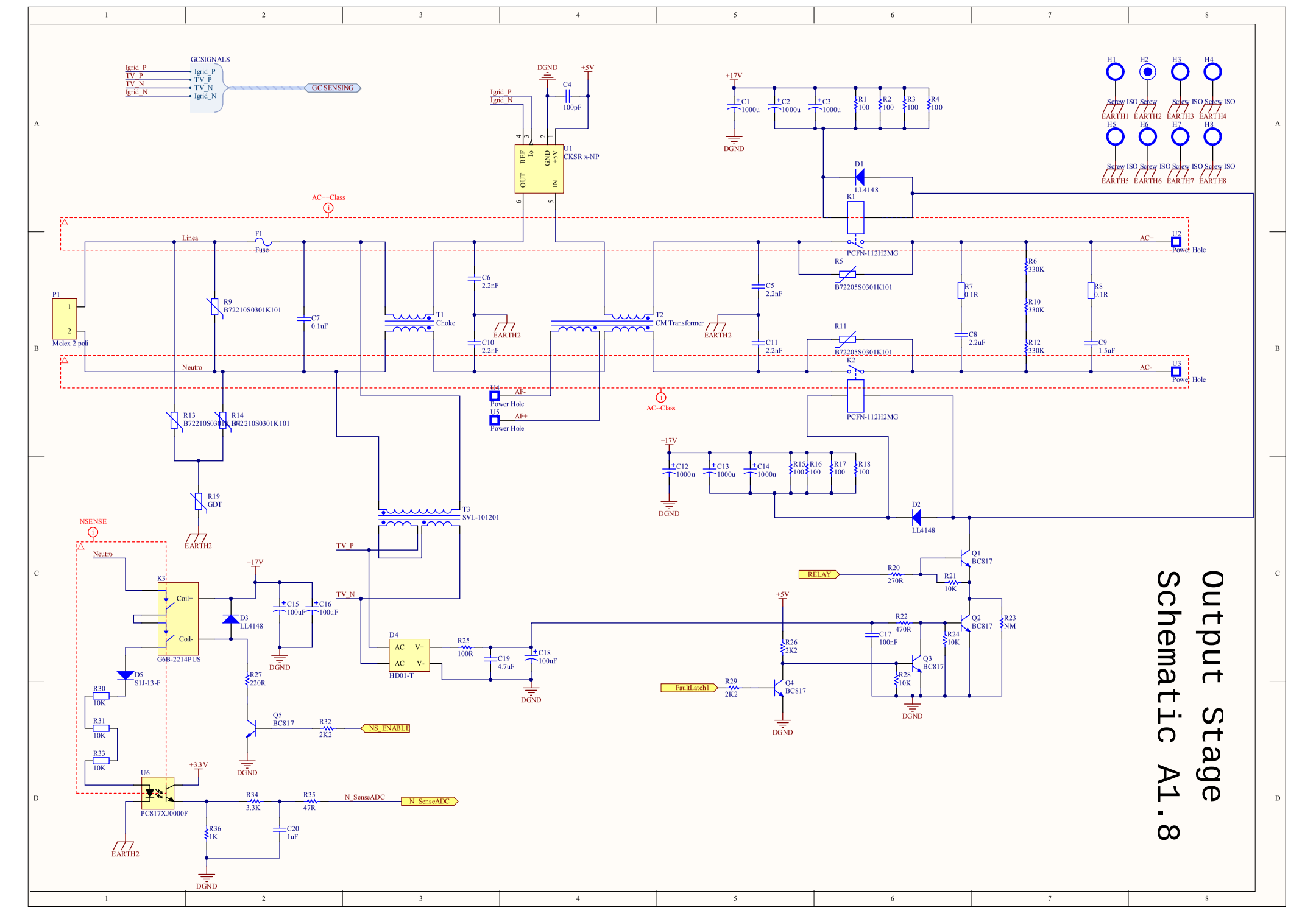

Power Circuit Schematic A1.5
Vdc
HX_Class
HY_Class
HZ_Class
HVFB_High_X
HVFB_High_Y
HVFB_High_Z
HVFB_Low_X
HVFB_Low_Y
HVFB_Low_Z
1000V, 10%
LL4148
IKW30N60H3
Vz 20V
GND_HVFB_HX
GND_HVFB_HY
GND_HVFB_HZ
HVFB_Out_X
HVFB_Out_Y
HVFB_Out_Z
HVFB_GND
HL_Class
BIS_Class
BISWITCH
BISWITCH_GD
FCB1
FESB16-JT
GND_BISWITCH
R47
R48
R49
R50
R51
R52
R53
R54
750
Vfc
LX_Class
LY_Class
LVFB_High_X
LVFB_High_Y
LVFB_Low_X
LVFB_Low_Y
GND_LVFB_HX
GND_LVFB_HY
LVFB_Out_X
LVFB_Out_Y
LVFB_GND
LL_Class
+17V
DGND
PRECARICA
BC817
2K2
K1
G6B-2214PUS
Coil-
Coil+
U16
U17
Power Hole
Res Varistor
R86
R90
HVFB_GND

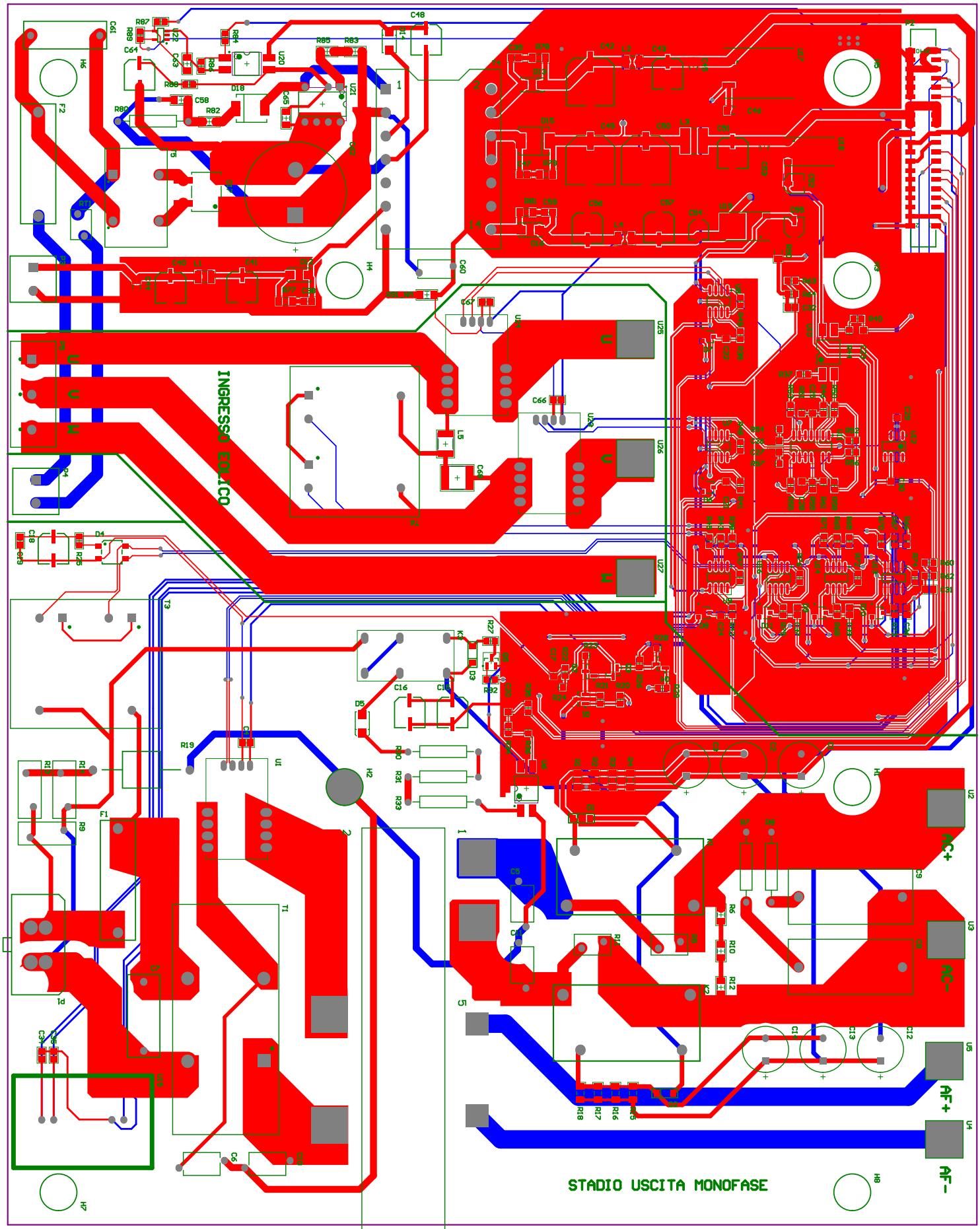
Power Card PCB A1.6



Flyback Schematic A1.7




GCSIGNALS
Igrid_P
TV_P
TV_N
Igrid_N
GC SENSING
DGND
+5V
C4
100pF
U1
CKSR x-NP
REF
Io
GND
+5V
OUT
IN
+17V
C1 1000u
C2 1000u
C3 1000u
R1 100
R2 100
R3 100
R4 100
DGND
H1 H2 H3 H4
Screw ISO
EARTH1 EARTH2 EARTH3 EARTH4
H5 H6 H7 H8
EARTH5 EARTH6 EARTH7 EARTH8
D1
LL4148
K1
PCFN-112H2MG
AC++Class
Linea
F1
Fuse
AC+
U2
Power Hole
R5
B72205S0301K101
R6 330K
R10 330K
R12 330K
R7 0.1R
R8 0.1R
C5 2.2nF
C8 2.2uF
C9 1.5uF
C11 2.2nF
P1
Molex 2 poli
R9
B72210S0301K101
C7 0.1uF
T1
Choke
C6 2.2nF
C10 2.2nF
EARTH2
T2
CM Transformer
R11
B72205S0301K101
Neutro
K2
PCFN-112H2MG
AC-
U3
Power Hole
U4
Power Hole
AF-
U5
Power Hole
AF+
AC--Class
R13
B72210S0301K101
R14
B72210S0301K101
R19
GDT
EARTH2
+17V
C12 1000u
C13 1000u
C14 1000u
R15 100
R16 100
R17 100
R18 100
DGND
D2
LL4148
T3
SVL-101201
NSENSE
Neutro
K3
Coil+
Coil-
G6B-2214PUS
+17V
C15 100uF
C16 100uF
D3
LL4148
DGND
TV_P
TV_N
D4
AC V+
AC V-
HD01-T
R25 100R
C19 4.7uF
C18 100uF
DGND
RELAY
R20 270R
R21 10K
Q1
BC817
+5V
R22 470R
Q2
BC817
R23 NM
C17 100nF
R24 10K
R26 2K2
Q3
BC817
R28 10K
DGND
FaultLatch1
R29 2K2
Q4
BC817
DGND
D5
S1J-13-F
R30 10K
R31 10K
R33 10K
R27 220R
Q5
BC817
R32 2K2
NS_ENABLE
DGND
U6
PC817XJ0000F
+3.3V
R34 3.3K
R35 47R
N_SenseADC
N_SenseADC
R36 1K
C20 1uF
EARTH2
DGND
Output Stage
Schematic A1.8



Output Stage PCB A1.9