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High-Speed Pipeline Analog-to-Digital Converter: Transistor-Level Design and Calibration Issues

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Preface

During the Ph.D. course many aspects related to the design of Analog Integrated Circuits have been considered with significant gain in terms of professional and academic experience. Central thread, the curiosity and the desire for discovering the answer of a problem. Following this motivation the research activity carried on during this three-years period has been based on three key points: the requirements analysis, the evaluation of architectural solutions and finally the effort to improve and optimize the solution itself.

The main activity was focused on the high-speed analog-to-digital conversion. On the basis of a time-interleaved converter idea, an high speed open-loop sampling circuit to be used as front-end stage was designed. The single conversion channel, based on a pipelined architecture, has been considered and the basic blocks have been designed: worthy of mention the flip-around track-and-hold, the flash sub-converter and the residue amplification circuit. The performance limits arising from the power consumption boundaries induce to turn the attention toward the calibration techniques. Digital algorithms to prevent gain, non-linearity and mismatch related errors have been deeply analyzed.

In addition to the main research field illustrated above, many collateral activities were carried out; the most important one is related to the modelling, design and testing of DC/DC Buck converters, briefly reported as side activity at the end of this dissertation.

Chapter 1

Introduction

The increasing demand for the implementation of more and more complex signal processing algorithms enforces the scientific research to improve the performance of the block linking the analog with the digital world, i.e. Analog-to-Digital Converters (ADCs). A considerable part of the research effort aimed at moving the border separating the analog and the digital domains toward the analog input. It is barely worth noticing that analog circuits does not always benefit from technology scaling: e.g. reducing the minimum achievable transistor size in a CMOS process allows to decrease the supply voltages leading to lower power consumption; despite to the oxide thickness scaling, the transistors threshold voltage does not scale down likewise, hence serious performance limits in analog circuits arise. On the countrary the digital circuits fully benefits from the latest deep-submicon technologies, therefore a design solution relaxing the constraints on the analog blocks of the converter with a more demanding digital processing seems the most promising choice. Moreover digital systems performing operations once entrusted to the analog circuitry allow the manufacturer to produce more flexible products in virtue of the high programmability level of digital solutions.

Advanced Digital Signal Processing (DSP) demands high performances to the analog counterpart in terms of speed and accuracy in

the front-end analog-to-digital conversion, hence the analog design issues still remain. In order to overcome the design limits imposed by the technology scaling constrains the analog front-end deficiency are tolerated and corrected by exploiting embedded software running on the digital process unit. From another point of view efficients calibration algorithms allow to voluntarily relax the performance required to the analog circuitry to save energy, silicon area and design effort.

All the aspects described above are tipically present in comunication system devices where high frequency bandpass signals must be transmitted and processed at high speed with a minimum loss of information and, especially for portable devices, with the lowest power consumption.

In this chaper a brief discussion on upcoming generation of Ethernet standard is reported and the designed circuits for this application are discussed.

1.1 10GBASE-T Ethernet Applications

All along, better performance at lower costs is the main task of electronic research engineering. This is the reason why Ethernet Alliance, a global non-profit industry consortium responsible for Ethernet standard definition and application, has driven the evolution of Ethernet over Unshielded Twisted Pair (UTP) from 10BASE-T to 10GBASE-T standard in the last decade.

Adopting a baseband 16 level pulse amplitude modulation (PAM) at 800 Mbaud/s of signaling rate, the signal processing for channel impairments mitigation, as in example line crosstalk cancellation, is feasible making 10GBASE-T comunication possible without the use of ad hoc cable typology. Since 3.125 bits per symbol are required, four UTP working at 2.5 GS/s each, are implemented in order to obtain an overal transmission rate of 10 Gb/s. Further improvements are obtained adopting Forward Error Correction techinques (FEC) as Low-Density Parity Check (LDPC) and high performances symbol mapping

as 128 points Double-Square (DSQ128) [1], [2].

Those standard specifications leads to suitable requirements for the analog-to-digital and digital-to-analog converters to be implemented in the 10GBASE-T tranceiver [3]. Focusing on the receiver hardware, the ADC must exhibits a resolution compatible with 10.5 effective bits around a target input frequency of 250 MHz at 800 MS/s; in terms of noise and linearity the ENOB specification leads to a minimum Signal to Noise and Distortion Ration (SNDR) of 65 dB. Since the target power budget for the whole tranceiver, depending on the cable lenght, varies between 1 W and 10 W, a reasonable ADC power consumption is about 300 mW.

1.2 High-Speed A/D Architecture

1.2.1 State-of-Art

State-of-Art in analog-to-digital converters design approaches the 10GBASE-T requirements however improvements in terms of effective resolution must be introduced.

At the moment only a few implentation of A/D converters suitable for 10GBASE-T application are reported in literature. In example, [4] reports a 1 GS/s, 11 bits ADC. The converter exhibits a peak SNDR of 55 dB, 58.6 dB of Signal to Noise Ratio (SNR) which results in an Effective Number of Bits (ENOB) of 9 bits; this solution, designed in a $0.13\,\mu$m digital CMOS process, shows a core power consumption of 250 mW. In [5] a 800 MS/s, 11 bits exploiting digital backgroud calibration with comparable performance, designed in 90 nm CMOS, is presented. Both ADCs consist of Time-Interleaved (TI) architecture which, at present days, seems the only solution suitable for the 10GBASE-T speed and resolution requirements.

In a time-interleaved architecture several conversion channels work in parallel at a reduced conversion rate $f_c = f_s/K$ where f_s represents the overall sampling frequency and K is the number of interleaved channels. In order to obtain the required overall conversion rate, a

Parameters	*10GBASE-T Requirement*	*Target*
Nominal Resolution	n.d.	12
Sampling Frequency	800 MS/s	$\frac{1}{4}$ GS/s= 250 MS/s
ENOB	10.5 bits @ 250 MHz of input signal	10.5 bits @ half Nyquist
SNDR	65 dB	65 dB
Power Consumption	n.d.	300 mW
Technology Process	n.d.	65 nm CMOS
Supply Voltage(s)	n.d.	$1.2/2.5V$ V
Temperature Range	n.d.	$0 - 100$ C CMOS

Table 1.1: Design Specifications (n.d. = Not declared in 10GBASE-T standard specifications).

single conversion channel working with a samping rate in the hundreds of MHz range is required. Considering a 65 nm standard CMOS process some solutions has been published in the last two years: [6] and [7] report two 10 bits pipeline ADC, at 100 MS/s and 125 MS/s respectively, both with an effective number of bits lower than 10 bits; a faster solution with lower resolution in reported in [8]. It is woth noticing that the higher the interleaving factor K, the lower the single channel sampling rate, however, more stringent is the timing accuracy.

1.2.2 Purpose of the Work

Time-Interleaving

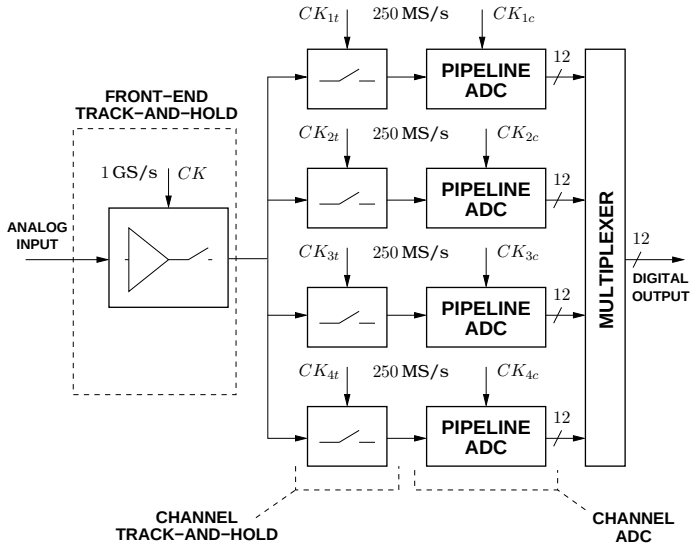
Purpose of the present work is the design of a 250 MS/s, 12 bits pipeline analog-to-digital converter in a 65 nm CMOS process, to be used in 1 GS/s Time-Interleaved architecture. In Tab.1.1 the target performaces are collected and compared to the 10GBASE-T standard requirements. The TI architecture is composed of four channel working at 250 MS/s each, driven by a Front-End Track-and-Hold (FETH) sam-

pling the input signal at the converter full rate of $1\,$GS/s; the four conversion channels are driven by four $250\,$MHz clock shifted of a quarter of clock period and the output data is obtained by multiplexing the channels results. Since each channel track-and-hold is driven by a $25\,\%$ Duty Cycle clock, only one channel loads the Front-End Track-and-Hold (FETH) when it is working in tracking phase; this solution allows to reduce the loading capacitance driven by the front-end stage, thus relaxing the current capability demanded to the $1\,$GS/s FETH. In Fig.1.1(a) a schematic representation of the TI-ADC is shown whereas in Fig.1.1(b) the channels timing is reported, assuming CK_{it} to be the i-th channel track-and-hold clock signal and assuming CK_{ic} to be the i-th channel converter clock.

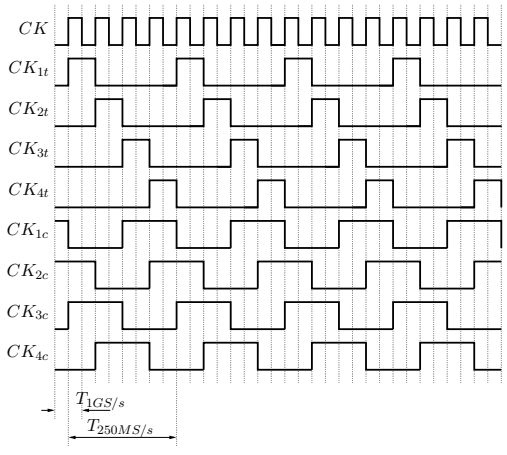
A/D Pipeline Conversion Channel

From the single channel specifications described above, the conversion channel is designed adopting a Pipeline architecture. Among the wide range of topologies, pipelined ADC represent the most reasonable choice for medium resolutions at medium-to-high conversion rates; since the effective converter resolution mainly depends on the performance of the first stages, the front-end stages represent the true bottleneck of the whole chain.

In this work a switched-capacitors pipelined ADC is presented with reference to the architecture reported in Fig.1.2. It is composed of $L+1$ stages where the first stage is the channel track-and hold. All the subsequent stages are composed of a switched-capacitors Multiplying Digital-to-Analog-Converter (MDAC) that performs at the same time input sampling (SH), residue calculation and amplification. Each stage embeds a flash Analog-to-Digital Sub-Converter (ADSC) implementing a rough quantization of the (amplified) residue provided by the provious stage. The digital output of the pipeline converter is obtained by composing the outputs of all sub-converters (ADSC) D_1, D_2 with a digital-correction algorithm. Different configurations, in terms of resolution of the ADSC embeded in each conversion stage, lead to



(a)



(b)

Figure 1.1: Time-Interleaved 1 GS/s ADC: (a) ADC arcitechture (b) channels timing.

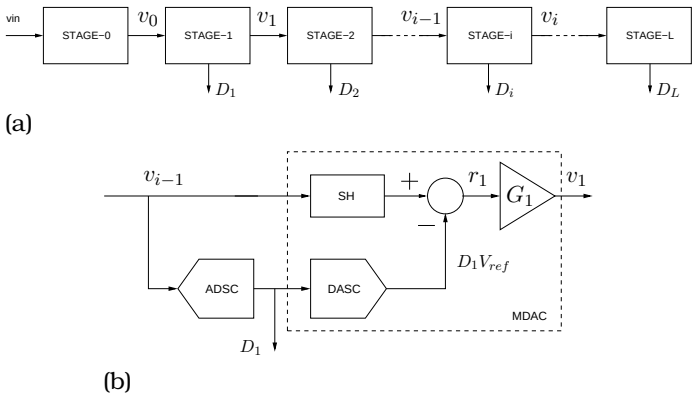


Figure 1.2: Pipeline ADC Architecture: (a) L-stages pipeline chain; (b) i-th stage detailed representation.

different capacitors size and different performances demanded to the operational amplifier (OPA) of each MDAC.

In order to prevent the residue over-range the Redundant Signed Digit correction technique (RSD correction) has been adopted. In example, a full-3 bits pipeline stage, is composed of a 7 decision levels coarse ADSC[1]; an ADSC thresholds shift with respect to the nominal position as well as a comparator offset component may produce amplified residue over-range (the amplified residue exceed the full-scale range), involving a conversion error; removing an ADSC decision level the flash converter resolution decrease to 2.5 bits however an $LSB/2$ decision level shift is tolerated[2]

[1]Being N the number of bit, a full-3 bits the stage flash converter requires

$$no.\,of\,Decision\,Levels = 2^N - 1 \tag{1.1}$$

[2]Being LSB the 3 bit converter Least Significant Digit. Being N the number of bit, a 2.5 bits the stage flash converter requires

$$no.\,of\,Decision\,Levels = 2^N - 2 \tag{1.2}$$

1.3 65 nm Low-Leakage CMOS Process

The proposed design has been implemented by exploiting a standard 65 nm low-leakage CMOS process with 10 Metal Levels (two Top Metallization), provided by SMIC™ (Semiconductor Manufacturing International Corporation). The standard process includes both core transistors (thin oxide MOSFETs) and I/O transistors (thick oxide MOSFETs) suitable for 1.2 V and 2.5 V operations respectively. The design kit includes linear MIM capacitors (Metal-Insulator-Metal) mandatory for high-linearity switched-capacitors circuits.

1.4 Contents

The Dissertation is organized as follows:

- Chapter 2 describes the Front-End Track-and-Hold design and the simulations results.
- Chapter 3 after a brief introduction on the conversion channel specifications, the pipeline stage blocks design and the obtained performance are discussed.
- Chapter 4 shows the Gain and Non-linearity Calibration algorithm and the MDAC Capacitors Mismatch estimation approach with Matlab® models description and simulations results.
- Chapter 5 ends the dissertation about the main research activity.
- Chapter 6 briefly reports the side activity on DC/DC Buck Converter Modelling, Design and Testing.

Chapter 2

Front-End 1 GS/s Open-Loop Track-and-Hold

As discussed in Chapter 1 high-speed, medium-to-high resolution analog-to-digital conversion requires special circuit solutions such as Time-Interleaving (TI) approach which in turn calls for Front-End Track-and-Hold (FETH). Generally speaking the task performed by a track-and-hold amplifier is the "signal freezing" in order to mitigate the settling and timing requirements of subsequent stages: for converters without any sampling circuit, the front-end stage elaborates fast-varying signal therefore it must exhibit a suitable bandwidth. In TI architecture the time-skew affecting the interleaved channels could seriously degrade the overall resolution; since each channel is fed with sampled signal (ideally constant in the hold phase) by means of a track-and-hold circuit the inter-channel timing mismatch is tolerated.

The foremost concern in the present design is the required sampling rate. Since the FETH must work at the TI analog-to-digital converter frequency, a wide bandwidth circuit is mandatory for preserving the linearity performance of the converter. Closed-loop solutions presented in [9] and [10] can benefit of the reduced distortion due to the feedback loop, however the feedback lopp itself limits the signal

bandwidth.
Open-loop samplers ensure high speed nevertheless require special circuit solutions for meeting the linearity requirements.

In this chapter an open-loop track-and-hold composed of an input buffer and a sampling network is presented and the design issues related to such circuits are illustrated.

2.1 Architecture

The FETH is designed for 1 GS/s operations with a nominal resolution of 12 bit. For the reasons descripted above an open-loop configuration has been chosen; it is based on a pseudo-differential input buffer realized by means of a pair of source followers (SF) and a pair of bootsrapped switches (BS). If the inter-channel (in TI structure) mismatch is negligible, the FETH can drive dirctly the hold capacitor of each channel sampling stage; moreover providing to each sampling network of each stage a clock with a duty cycle of $25\,\%$ allows the FETH to drive only one channel during each tracking phase. Some considerations about this basic blocks are discused in the next sections.

2.1.1 Source Follower Stage

The PMOS SF stage schematic is shown in Fig. 2.1(a) whereas the small-signal model is reported in Fig.2.1(b) [11]. All the non-linear contributions in the model of the MOS transistor are the reasons of the distortion being, together with the noise performances, the main issue of the present design. An exhaustive analysis of the source follower non-linearities is reported in [12].

The first problem arises from the body effect: since the bulk of M_1 is tied to a fixed voltage, the modulation of the threshold by the source-bulk voltage leads to a signal-dependent changing in the difference $v_o - v_i$ generating distortion. The effect is canceled if the source-bulk voltage is kept constant. However, a simple source-bulk con-

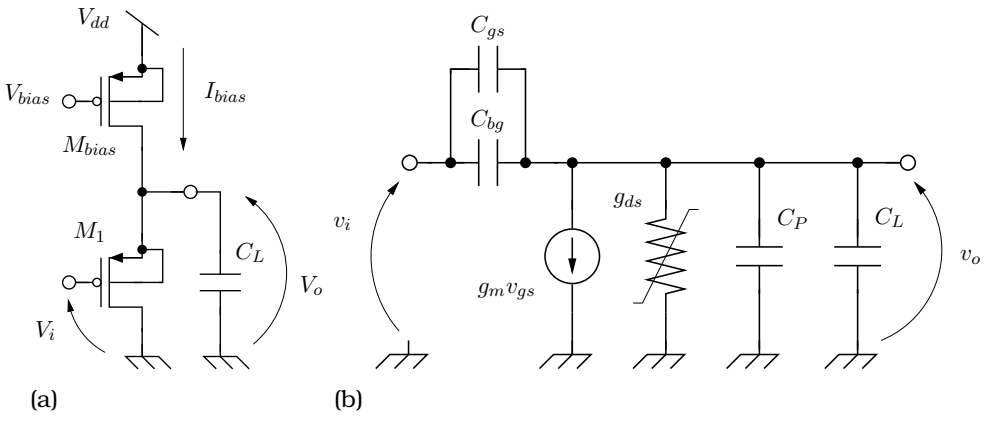


Figure 2.1: PMOS Source Follower: (a) schematic and (b) small-signal model

nection adds the well-substrate capacitance to the output load. It is worth noticing that in the case of a NMOS SF, a triple-well process is mandatory.

If the body effect is avoided, the v_{ds}-dependent output conductance of M_1 is the second cause of distortion. It is worth noticng that g_{ds} modulation effect arises in M_{bias} too; however, since the bias current generators can be implemented by means of advanced architectures, i.e. high-swing cascode mirrors, the output conductance modulation of the upper part of the circuit results negligible and the bias current can be considered almost constant. The v_{ds}-dependence of g_{ds1} can be mitigated by chosing the proper channel length and the bias point of M_1 [13]. In [14] the benefits of the cascode architecture and the headroom limitations are shown.

The third non-linear effect is related to the output current. The output voltage tracks the input and a frequency-dependent current flows through the load capacitance at the output node; the overall output node capacitance is due to the parasitic capacitance at the buffer output C_P and to the hold capacitor C_H. Since the output impedance of the bias structure is high, the output current affects

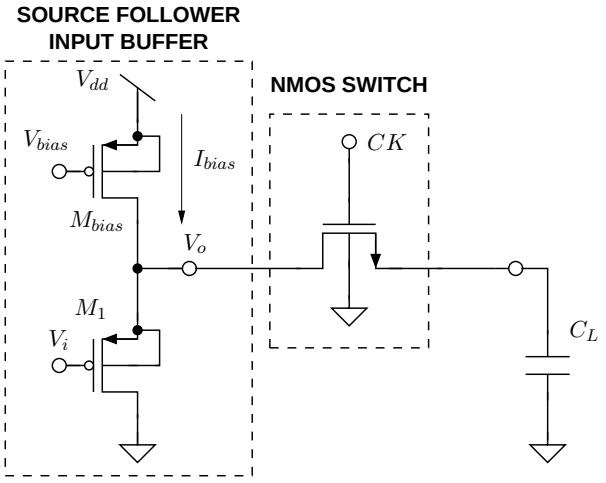


Figure 2.2: PMOS Source Follower and sampling network.

the drain current of M_1, causing a frequency and amplitude dependent modulation of the gate-source voltage. This effect leads to harmonic distortion affecting the output signal [13].

Using the SF buffer to drive a sampling network, the distortion caused by the settling error may become the dominant non-linear effect. In [15] the settling behaviour model of a SF based on sampling circuit is presented and the optimized sizing is discussed.

The resolution of the FETH is affected by the noise performance as well. The buffer broadband noise is filtered by the driven sampling network; tipically the follower contribution is lower than the quantization noise and the overall noise performances are limited by the sampling network (see Section 2.3).

2.1.2 Sampling Network

The basic elements of a sampling network are the switch based on a MOS transistor and the hold capacitor, as shown in Fig. 2.2. The hold capacitor C_H must be sized according to the noise requirements and

using the well-known relationship $v_n^2 = kT/C_H$, v_n^2 being the rms output noise contributed by the switch on-resistance. The main cause of harmonic distortion is the signal-dependent on-resistance of the switch, since its overdrive voltage depends linearly on the output voltage. The usage of a complementary transmission gate lowers the on-resistance value and thus attenuates only the harmonic distortion due to this effect.

Another relevant effect is the charge injection of the MOS switch at the sampling instant. Considering a level-1 MOS model and an equal partitioning of the channel charge at the drain and source terminals, the signal-dependent injected charge leads to offset and gain error. However a more accurate analysis, mandatory for deep-submicron devices, reveals that the channel charge injected to the output node at the switch turn-off, exhibits a non-linear dependence on the terminals voltage. Since the gate-source voltage and the charge forming the channel depend on the input signal, the error voltage arising during the turn-off is non-linear and it becomes a source of harmonic distortion.

2.2 Design Considerations

2.2.1 Requirements Overview

In order to match the 10GBASE-T requirements the proposed FETH must exhibit a nominal resolution of 12 bits with an ENOB greater than 10.5 at 250 MHz of input signal [1], therefore the required SNDR must be greater or equal to 74 dB. Neglecting harmoinc distortion with respect to noise (i.e. SNDR $\approx$ SNR), the SNDR spec can be used to size the hold capacitor C_H as described in the previous section: assuming the input amplitude to be 500 mV, 74 dB of SNDR leads to an hold capacitance as large as 1 pF. Such a large capacitance has detrimental effects on the distortion and a trade-off is mandatory. Two different design have been contemplated: at first a 400 fF capacitor have been selected whereas a 1.2 pF solutions has been evaluated (see Section

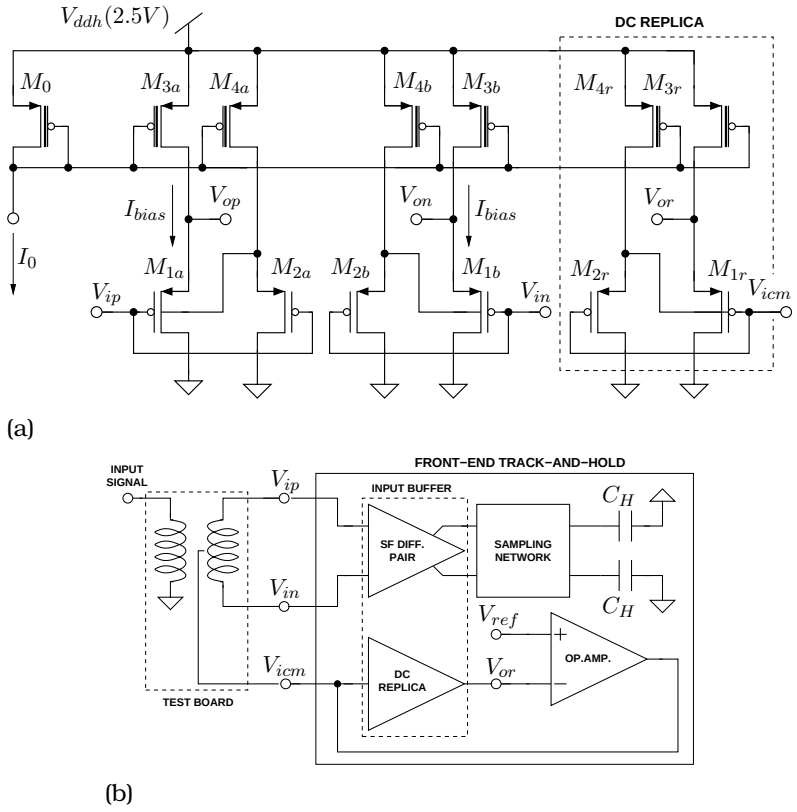


Figure 2.3: PMOS Source Follower schematic: (a) pseudo-differential schematic and (b) common-mode control loop

2.3) in order to obtain better noise performances.

2.2.2 Input Buffer

As afore-mentioned, the input buffer is composed of a pair of PMOS SF as shown in Fig.2.3(a). Initially, a low-voltage solution (1.2 V supply) has been evaluated; however, the limited output swing allowed to achieve a suitable distortion levels with a signal amplitude as low

as $300\,\text{mV}$, being incompatible with the SNR requirement; in order to preserve the SNR, a lower input amplitude calls for higher capacitors size leading to higher, and then inaceptable, power consumtions. A larger signal swing calls for a higher supply voltage. To this aim a $2.5\,\text{V}$ supply architecture combining I/O MOSFET (thick oxide) with CORE MOSFET (thin oxide) is adopted. Similar results can be obtained using thin oxide transistors only and using a cascode current generator. Since the FETH is designed to drive an ADC with $1.2\,\text{V}$ of supply voltage (low-power solution), the output of the buffer has to be kept lower than $1.2\,\text{V}$ controlling the buffer output common mode level. As a consequence M_{1a} and M_{1b}, that represent the pseudo-differential pair, can be realized by means of thin oxide transistors whereas the bias current generators M_{3a} and M_{3b} can be realized using thick oxide MOSFET; this solution allows to benefit of the larger g_m and transition frequency for the thin-oxide followers input devices and at the same time guarantees a large source-drain voltage for the current generators. The last condition is mandatory to achieve an almost signal-independent g_{ds} for M_{3a} and M_{3b}.

The body effect cancellation is obtained by driving the bulk of the input devices, M_{1a} and M_{1b}, by an auxiliary pair of source followers composed by M_{2a}, M_{4a} and M_{2b}, M_{4b}. This solution forces the bulk to track the source with a DC shift without loading the main follower output with the well-substrate capacitance.

The impact of the output common mode voltage (V_{ocm}) on the distortion performance calls for a closed-loop control. A scaled replica of the follower is added and a feedback loop controls the input common mode voltage to avoid the process-variation of the output DC level. As shown in Fig. 2.3(b), the loop is composed of the replica, a reference voltage V_{ref} and a single-ended operational amplifier which controls the replica input voltage and the common mode input voltage of the main source follower (V_{icm}). As mentioned before, the V_{ocm} is chosen so that the output voltage does not exceed $1.2\,\text{V}$ and the MOSFETs $M_{1a,b}$ are in saturation region; moreover V_{ocm} is optimized according to the performance of the sampling switch. Due to the control loop,

V_{ocm} exibiths only a $+1/-5\,\%$ of variation with respect to the typical value of $700\,\text{mV}$, over the full corner space.

The bias current of the Source Follower is selected according to the Slew-Rate requirements; assuming a $1\,\text{V}$ peak-to-peak sinusoidal input at $500\,\text{MHz}$ and a load capacitance of $400\,\text{fF}$, the minimum bias current is $670\,\mu\text{A}$ [13].

The transistors sizing was based on a methodology using the concept of *Inversion Factor* (IF) [16]. Considering $M_{1a,b}$ in saturation region and in weak inversion (WI) the intrinsic gain is high and the drain-source saturation voltage is low whereas in strong inversion (SI) the thermal noise is minimized. In WI the transistors aspect ratio compatible with the calculated bias current is high and the parasitic capacitances become relevant, hence the SI operation is chosen. Assuming the length to be $2.5\,\mu\text{m}$ to reduce the impact of the channel-length modulation effect and assuming IF to be 10, the source-drain saturation voltage results $230\,\text{mV}$; with a V_{ocm} of $700\,\text{mV}$ the SF MOSFETs are always in saturation region.

2.2.3 Sampling Switch

Conventional switches, i.e. complemetary transmission-gates, are not adequate for the linearity requirements; it can be shown that the on-state conducatne for the above switch topology resuts [17]:

$$g_{ON} \approx \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{dd} - V_i - V_{THn}) + \mu_p C_{ox} \left(\frac{W}{L}\right)_p (V_i - |V_{THp}|) \quad (2.1)$$

where $mu_{n,p}$ is the channel mobility, C_{ox} is the specific gate capacitance, $(W/L)_{n,p}$ is the MOSFETs aspect ratio and $V_{THn,p}$ is the transistor threshold voltage. Although for $\mu_n C_{ox} (W/L)_n = \mu_p C_{ox} (W/L)_p$ the on-conductance seems to be independent from the input level, the body effect introduces a signal dependance which can not be neglected. This effect is as pronounced as the dynamic range is reduced (low-voltage driving clock).

In order to mitigate the undesired effect above, a rail-to-rail scheme

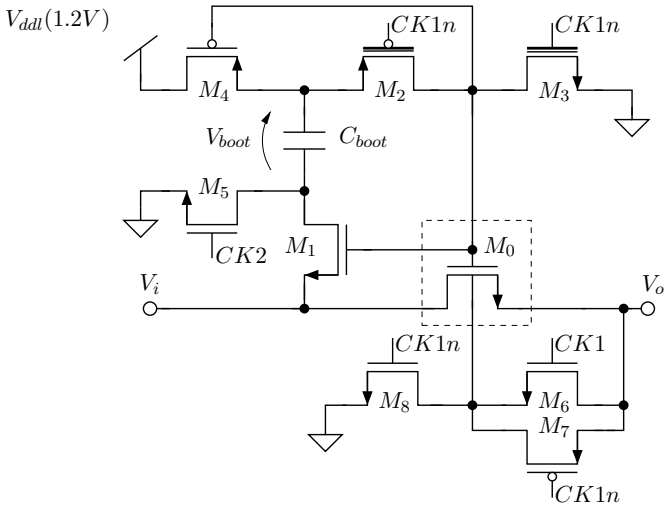


Figure 2.4: Rail-to-rail switch.

has been adopted. The used Bootsrapped Switch (BSW) schematic ($1.2V$ supply) is shown in Fig.2.4; based on [18] solution, several MOSFETs have been removed in order to ensure high-speed operation. Keeping the V_{gs} of the main switch M_0 (V_{gs0}) constant, the on-resistance and the channel charge become indipendent from the input signal and the related distortion is thus eliminated; in a single-ended version charge-injection generates pedestal error whereas in a differential structure, neglecting transistor mismatch, its effects are completely removed.

The main issue, in the proposed circuit, is the sizing of the bootstrap capacitor C_{boot}, which must be large enough to achieve a gate-to-source voltage of the MOS switch in track-mode close to the supply voltage. Due to the boosting, the voltage at the drain/source terminals of M_2 and at the drain terminal of M_3 exceed the supply voltage, thus raising oxide breakdown and reliability issues. For this reason thick oxide MOSFETs were used for M_2 and M_3. If thick oxide devices are not available, a cascode architecture must be used instead.

The bulk terminal of M_0 is tied to ground during the hold phase and it is connected to the source during the tracking phase, by means of M_6, M_7 and M_8. This solution remove the threshold modulation of M_0 (body effect) and lowers the THD of about 2dB. Furthemore the oxide stress is reduced for M_0.; the drawback is the need of a triple-well process.

As shown in [19], to ensure a proper amplitude accuracy, RC network represented by the switch and the hold capacitor during the tracking phase must exhibit a 3dB-bandwidth higher than $2^{\frac{N-1}{2}} f_{in}$; where N is the resolution and f_{in} is the input frequency. Assuming C_H to be $400\,$fF, a resolution of 12 bit at a $250\,$MHz input frequency, requires a minimum sampling network bandwidth of $11.3\,$GHz. The size of M_0 must be chosen according to the requirement described above. As shown in Section 2.3, the designed switch exhibits a 3dB-bandwidth higher than $10\,$GHz.

The switches composing the boosting network are sized to provide the minimum voltage drop: higher size MOSFETs lead to a higher power consumption of the clock buffer, hence a trade-off is mandatory.

2.3 Simulations

2.3.1 FETH Simulations

The proposed circuit has been simulated over the full Process-Voltage-Temperature corner space; i.e. a $\pm 10\,\%$ of tollerance on both the supply voltages ($1.2\,$V and $2.5\,$V) and a $0^\circ - 100^\circ\,$C temperature range are considered. At first the input buffer and the sampling network have been simulated separately in order to evaluate the performaces of such blocks; subsequently the whole FETH has been considered and the main resulting features are reported as follow comparing the $400\,$fF and the $1.2\,$pF design.

AC Performaces

The AC behaviour of the FETH has been verified: the 3dB-bandwitdh of the whole system is 16.1 GHz and 10.4 GHz in the typical-case and in the worst one respectively with a 400 fF of holding capacitor; the solution designed to drive 1.2 pF exhibits a typical 3dB-bandwitdh of 22.99 GHz and a worst-case one of 16.96 GHz. The SF, as described in [11], exhibits a wide bandwidth behaviour while the overall 3dB-frequency of the whole FETH is limited by the sampling network. It is worth noticing that the input buffer ehibits a gain quite lower than one (≈ 0.2 dB of attenuation).

Noise Performaces

Noise performance of a periodic steady-state circuit, i.e. sample-and-hold circuit in which track and mantaining phases alternate, can be evaluate by means of PSS/PNOISE (Periodic Steady-State/Periodic Noise) analysis [20]; since the main noise contributions descend from the circuit during the tracking phase similar results have been obtained using the simpler and faster continuous-time NOISE anlysis performed keeping the switch on.

Fig.2.5 shows the noise output voltage spectral density for both designed circuit (400 fF and 1.2 pF of holding capacitance). The equivalet root mean square output noise voltage, integrated over a conservative bandwidth 1 Hz $\div$ 100 GHz, results typically lower than $143\,\mu$V and lower than $79\,\mu$V with the 400 fF and 1.2 pF designs respectively whereas the worst-case voltages result lower than $161\,\mu$V and $97.1\,\mu$V. Assuming the input amplitude to be 500 mV, the worst-case SNR results 67 dB with 400 fF and 71.2 dB with 1.2 pF.

Linearity Performances

Fig.2.6 shows the FETHA transient behaviour. The linearity of the FETHA is a matter of primary importance: such performance is evaluated calculating the Discrete Fourier Transform (DFT) of the out-

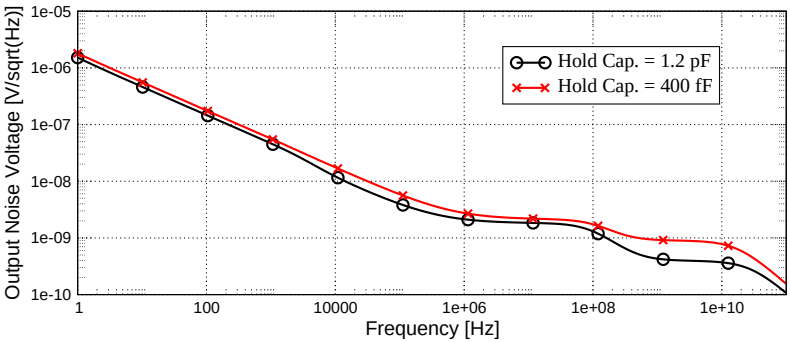


Figure 2.5: Output Noise Voltage spectral density: Typical case at 27° C.

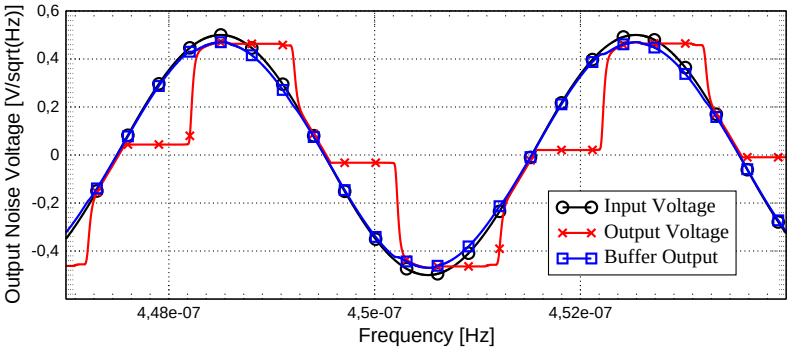


Figure 2.6: FETHA Transient behaviour: Typical case.

put samples obtained in response to several significat input stimulus; since the 10GBASE-T information bandwidth is centered around 250 MHz, single-tone and two-tones test at that frequency have been performed.

Transient simulations were performed at 1 GS/s sampling speed and a 1 V (differential peak-to-peak amplitude), 265 MHz input sine-wave as shown in Fig.2.6. At such frequency the 440 fF design exhibits a total harmonic distortion lower than $-92dB$ and $-82dB$ in the typical and in the worst cases; comparable results have been obtained for the 1.2 pF version. An example of DFT spectrum of the sampled

output signal is shown in Fig.2.7. The FETHA THD has been evaluated for different input amplitude: as shown in Fig.2.8 considering the 440 fF design and a 265 MHz input sine-wave, the THD increases monothonically with the input amplitude. Likewise the FETHA linearity performances have been analyzed sweeping the input signal frequency: as shown in Fig.2.9 considering the 440 fF design and a 1 V input sine-wave, the THD is optimized around the 250 MHz target frequency; it is worth to notice that at lower frequency the channel lenght modulation is the main linearity degradation effect whereas at higher frequency the output current through the hold capacitor become the dominant factor.

Two-tones tests were performed over the full corner space with $234.3MHz$ and $265.6MHz$ input stimuli: the simulated SFDR is $86dB$ and $79dB$ in the typical and worst-case respectively, for the 400 fF; beside, for the 1.2 pF design, the SFDR results 81.7 dB and 79.7 dB in the typical and worst-case respectively. Fig 2.10 shows a two-tones simulation results with input stimuli at $248.0MHz$ and $251.9MHz$ and considering a typical corner; the intermodulation products are visible at $244.1MHz$ and $255.8MHz$.

Power Consumption

Considering the 400 fF design the overall worst-case power consumption is 10.6 mW, including the buffer, the rail-to-rail switch and the clock buffer. The current consumption of the 2.5 V and 1.2 V analog supplies are 1.85 mA and 290μ A respectively, whereas the digital supply provides 3.93 mA. For the 1.2 pF version the total power consumption does not exceed 15.3 mW.

2.3.2 Final Consideration

In Tab.2.1 a summary of the simulated performances is reported. Assuming the input amplitude to be $500mV$, joining the SNR informations and the THD values the ENOB can be estimated: the 400 fF

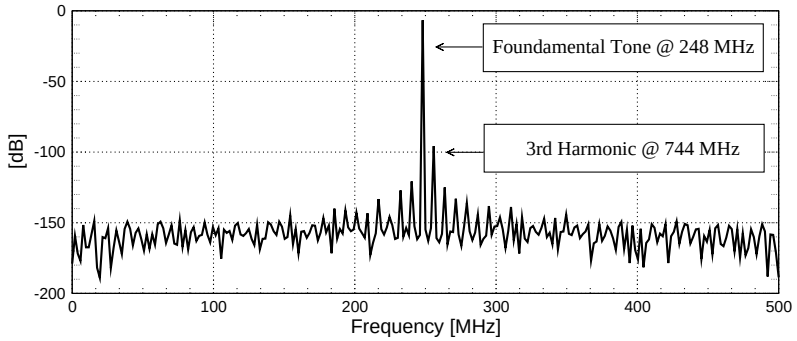


Figure 2.7: FETHA sampled output DFT (Single Tone Test): 512 pts. input @ $f_S(127/512)$, where $f_S = 1\,\text{GHz}$ is the sampling frequency.

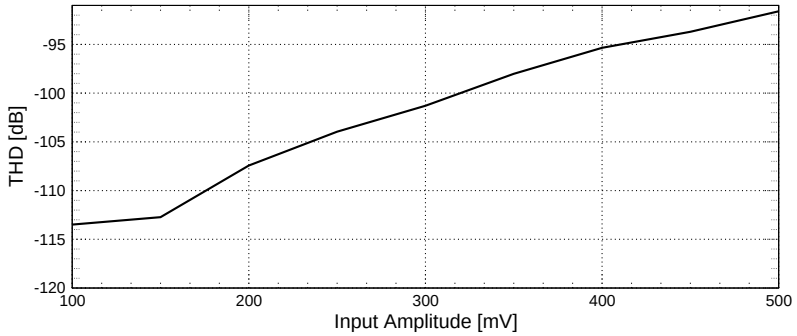


Figure 2.8: FETHA THD versus the input sine-wave amplitude @ $265\,\text{MHz}$.

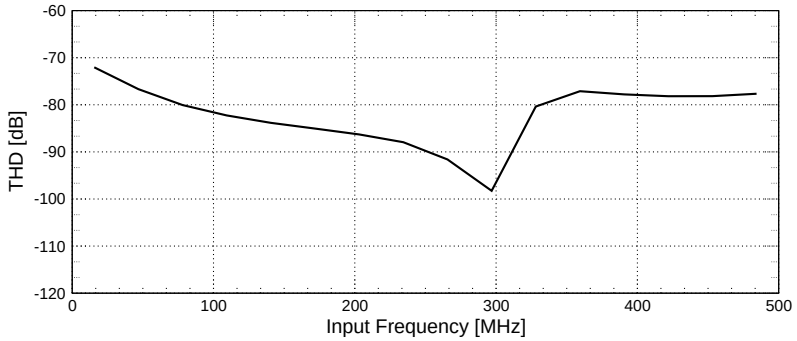


Figure 2.9: FETHA THD versus the input sine-wave frequency @ $1\,\text{V}$ of amplitude.

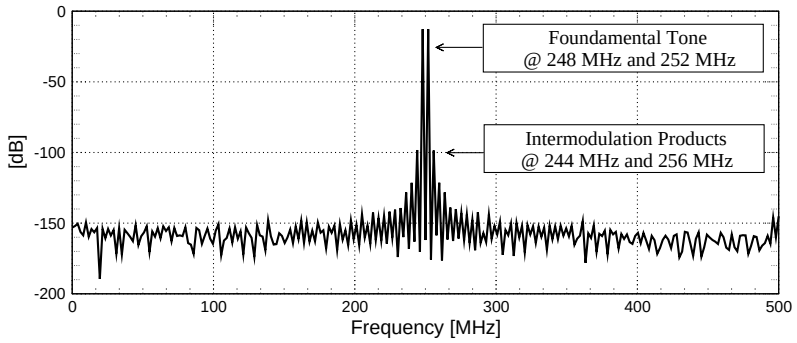


Figure 2.10: FETHA sampled output DFT (Two Tone Test): 512 pts. input @ $f_S(127/512)$ and $f_S(129/512)$, where $f_S = 1\,\text{GHz}$ is the sampling frequency.

	$C_H = 400\,fF$	$C_H = 1\,pF$
RMS Output Noise Voltage (V_{norms}) [μV]	161	97.1
THD [dB]	-82	-82
SFDR [dB]	79	79
SNR [dB]	67	71
SNDR [dB]	66	69
ENOB [bit]	10.6	11.2
Power Consumption [mW]	10.6	15.1

Table 2.1: FETHA worst-case overall performances summary.

FETHA exhibits a SNDR of $68dB$ (11 bit) and $66dB$ (10.6 bit) in typical and worst-case, respectively; increasing the holding capacitor up to $1.2\,\text{pF}$, despite of a higher power consumption in orger to provide comparable 3dB-bandwidth and slew-rate capability, a lower SNR results and then better overall performances have been achieved: in particular the worst-case SNDR rises to 69 dB (11.2 bit).

Chapter 3

250 MS/s Pipeline ADC Channel

3.1 Pipeline Blocks Specifications

By means of accurate stage model described in [21] the more suitable configuration for the overall application requirements has been individuated: the proposed chain is composed of five 3 bits stages and a 2 bit flash converter as last chain stage (333332). It is worth noticing that this configuration allows to design only one stages architecure, replicated along the pipeline chain.

The accurate model described in [21], fixed the chain configuration (333332), allows to define the operational amplifiers specifications for each stage; with reference to the first stage, the critical one in the whole ADC, the required performances in terms of resolution lead to stringent gain and bandwidth specification: the first stage amplifier must exhibiths a DC gain (A) higher than 78 dB and a minimum Unity Gain Bandwidth (UGB) equals to 2.4 GHz.

Starting from the required ENOB the Signal to Noise and Distortion Ratio (SNDR), assuming a full-scale input sine wave, is calculated

Pipeline Stage	*Capacitors*	*OPA DC Gain*	*OPA UGB*
1st	200 fF	78 GHz	2.4 GHz
2nd	190 fF	66 GHz	1.9 GHz
3rd	70 fF	58 GHz	1.5 GHz

Table 3.1: MDACs Operational Amplifiers Specifications for the first three stage.

as follows:

$$\text{SNDR} = 6.02 \cdot \text{ENOB} + 1.76 \tag{3.1}$$

therefore, 10.5 bits of ENOB correspond to 65 dB of SNDR. The SNDR in turn, including both the Total Harmonic Distortion (THD) and the SNR, is

$$\text{SNDR} = \frac{1}{\text{THD}^{-1} + \text{SNR}^{-1}} \tag{3.2}$$

Assuming, to a first order analysis, the SNDR to be equally distributed between linearity and noise, the minimum THD and the minimum SNR equal to 71 dB. Better linearity allows to relax the SNR constrain. The total noise budget must be shared among the pipeline stages and for each stage it must be shared between sampled thermal noise due to the switches (KT/C) and the operational amplifier. Following these considerations the accurate model in [21] provides the minimum capacitors size that for the first stage results 200 fF. Similar considerations lead to the FATHA capacitors size of 2 pF for a $100°$C maximum operating temperature; however, such sampling capacitor involves unacceptable power consumption and a trade-off is mandatory; the FATHA capacitor size is chosen to be 1 pF. The operational amplifiers specifications for the first three stages, calculated according to the model in [21], are collected in Tab.3.1.

It is worth noticing that such noise levels represent a stringent target in the operational amplifier design; in order to grant the required SNR relaxing the noise budget, the input signal amplitude must be maximized; otherwise the higher signal swing, the higher the impact

of non-linearities due to operational amplifier and switches. In this work the differential peak-to-peak signal amplitude is $1\,\mathrm{V}$.

3.2 Flip-Around Track-and-Hold Amplifier

In this paragraph the channel track-and-hold amplifier is presented. Alhough the switched-capacitors pipeline stage has sampling capability, the addition of a channel dedicated front-end sampling circuit is almost mandatory to relax the subsequent stage requirements; if the first stage is fed directly with the fast-varying input signal (up to Nyquist rate), it should exhibit dynamic performances much more stringent than a conversion stage fed with a sampled signal, and then constant during the acquisition phase.

3.2.1 Track-and-Hold Architecture

Track-and-hold circuits can be obtained by means of open-loop or closed-loop solutions [22]. The former, suitable for high speed operation, is hardly compatible for 12 bits resolutions; the latter, on the contrary, provides high linearity level taking advantage from the feedback loop however it suffers from poor analog bandwith. Among closed-loop architectures two possible solutions are available: Charge-Sharing circuit with gain of 2 and the unity gain Flip-Around solution. Since the charge-sharing approach exhibits a closed-loop bandwidth halved with respect to the flip-around one the latter is chosen in order to exploit the better power efficiency.

In Fig.3.1(a) the simplified schematic of the fully differential Flip-Around Amplifier (FATHA) here implemeted is shown. According to the timing diagram reported in Fig.3.1(b), the circuit operation can be described as follows: during the acquisition phase (ϕ_1) the holding capacitor C_H has the top plate connected to the input signal through the switches $BSW_{1,2}$ and the bottom plate is connected to the operational amplifier common mode input voltage V_{CMIN} through $TXG_{1,2}$;

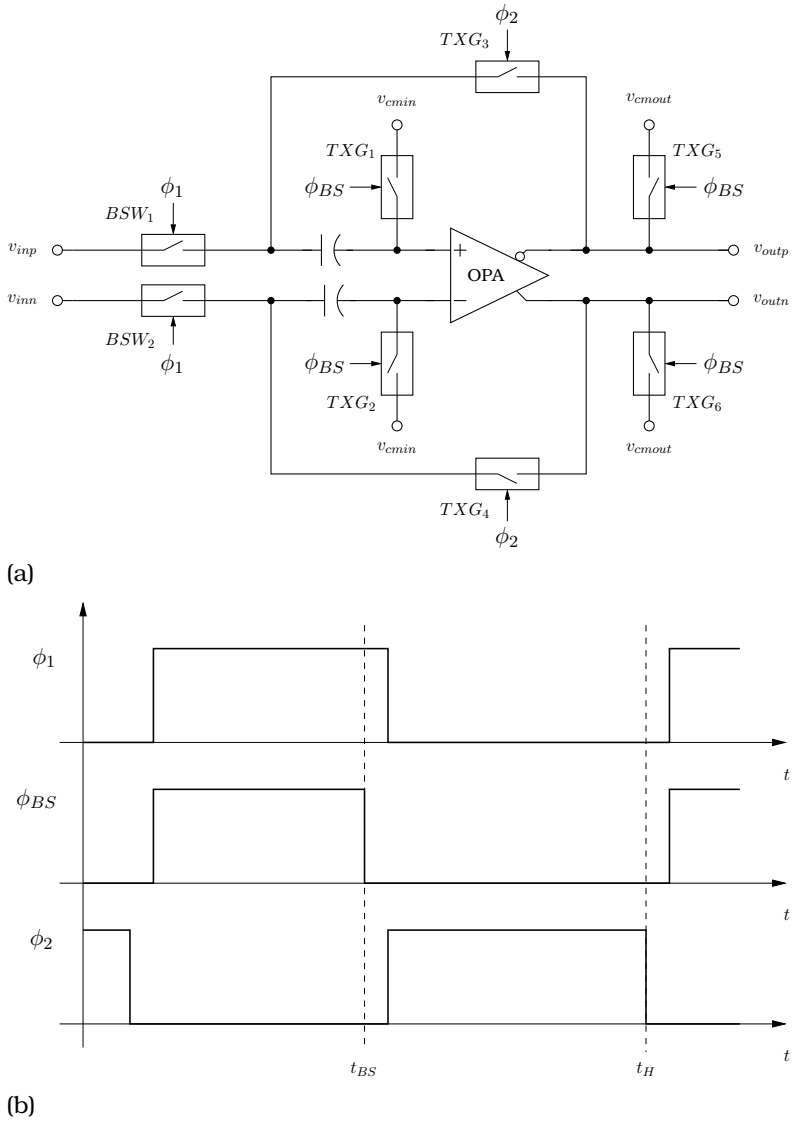


Figure 3.1: Flip-Around Track-and-Hold Amplifier: (a) schematic (b) clock phases.

at the end of the sampling phase the capacitors bottom plate are isolated from V_{CMIN} by turning $TXG_{1,2}$ off (ϕ_{BS}) and after a short deadtime the input source is disconnected by switching $BSW_{1,2}$ off. This opening sequence, known as bottom-plate sampling, avoids charge injection problems at the tracking to holding phase transition. During the tracking phase the operational outputs are shorted togheter and fixed to the output common mode voltage V_{CMOUT} in order to prevent the output saturation that may slow down the signal recovering during the subsequent amplification phase ($TXG_{5,6}$). Shortly after the $BSW_{1,2}$ have been tunrned off, C_H is connected between the operational amplifier input and output terminals closing the feedback loop through $TXG_{3,4}$ (ϕ_2). The holding phase begins and the operational amplifier (OPA) must perform the regenerative transient to settle the cirtuit output voltage. If the feedback loop is fast enough, a the end of ϕ_2 (t_H) the output voltage equals the input voltage at the bottom-sampling instant (t_{BS}):

$$v_{out}(t_H) = v_{in}\,(t_{BS}) \tag{3.3}$$

As shown in section 1.2.2, the FATHA is driven by a $250\,$MHz, $25\,\%$ Duty Cycle clock in order to allow the FETH to drive only one channel during each tracking phase. With respect to the situation shown in Fig.3.1(b), the actual timing differs only in terms of length of each phase; the clock period is therefore assigned for the $25\,\%$ to the acquisition phase ϕ_1 and for the remaining $75\,\%$ to the holding phase. This solution does not affect the front-end circuit, working at $1\,$GS/s, and relax the settling capability demanded to the OPA.

The operational amplifier common mode input voltage V_{CMIN}, chosen in order to bias properly the PMOS differential pair of the OPA, equals to $300\,$mV (OPA supply voltage equals to $1.2\,$V); the output common mode voltage, controlled by means of a feedback loop is set to $600\,$mV (see. paragraph 3.2).

The FATHA capacitors' size have been determined according to the noise performances compatible with the overall resolution of $12\,$bits; it is worth noticing that a power, noise and matching trade off could be

needed. In this case four unit of $260\,\text{fF}$ each are connected in parallel to obtain a $1.04\,\text{pF}$ holding capacitor.

3.2.2 CMOS Switches

One of the most important block in a switched-capacitors circuit are the switches used to change the signals path at phases transitions. Depending on the position and the role of the switch in the circuit different performances are demanded to the same switch. In example, as shown in Fig.3.1(a), the switches $TXG_{1,2}$ used to connect the C_H bottom plate to V_{CMIN} as well as the switches $TXG_{5,6}$ used to hold the operational amplifier to V_{CMOUT} during the acquisition phase, work on constant voltage therefore none particular linearity performance is demanded. The switches above should exhibit a resistance as low as in order to grant low drop voltage and fast settling at the turning on, avoiding significant parasitics loading to the rest of the circuit. For this reasons complementary transmission gate, with equal NMOS and PMOS sizes, are used; this conclusion has been drawn after simulations aimed to evaluate the best trade off between on-resistance and capacitive parasitics. Some benefits have been proved using complementary transmission gates with dummy switches to implement $TXG_{1,2}$.

More complicated is the design of the main switches $BSW_{1,2}$; since the input signal is fed to the holding capacitors through $BSW_{1,2}$, and the quality of the acquired sample depends on the linearity of these switches, proper solutions must be adopted. At low supply voltage ($1.2\,\text{V}$ in this work), being the MOSFETs threshold voltages fixed approximately to $600\,\text{mV}$, the linear region provided by the use of complementary transmission gates is not compatible with the signal amplitude. Boosting techniques, similar to the approach shown in chapter 2, have been adopted for the implementation of $BSW_{1,2}$. Initially rail-to-rail switches have been used in the feedback path too. The impact of the parasitics elements, due to the boosting capacitance and due to the large number of switches, vanish the benefits intro-

duced by the rail-to-rail operations; therefore the feedback switches $TXG_{3,4}$, are implemented by means of complementary transmission gates properly sized.

3.2.3 Operational Amplifier

The main task demanded to the track-and-hold operational amplifier is the transient recover in order to reproduce at the output nodes, the sampled voltage stored on the holding capacitor C_H. Since during the acquisition phase the OPA output nodes are shorted to the common mode voltage and the differential voltage is zero, the step response demanded to the amplifier must be compatible with the linearity requirements and the clock period. Typically, the transient behavior in presence of high swing steps includes a non-linear phase, during which the OPA works in slew-rate mode, and a linear one during which the operational amplifier works in linear region. The slew-rate phase duration depends on the operational amplifier bias current whereas the linear settling performance depends directly on the OPA bandwidth. Although the gain error of the sampling stage is not a relevant issue for analog-to-digital converters, an operational amplifier achieving high DC gain allows to improve the linearity of the closed-loop track-and-hold [22]. Based on the cosiderations above, the operational amplifier gain and bandwidth specifications have been evaluated and a trade off has been individuated: considering the distortion simulations results an Unity Gain Bandwidth higher than $1\,$GHz and a minimum DC gain of $70\,$dB appear to be adequate in terms of output signal resulting THD.

The OPA architecture choice is not a trivial matter hence different configurations have been investigated. As a first a two-stages, Miller-compensated OTA has been considered and discarded since the required settling speed involve difficult compensation and unacceptable power consumption. For the same reasons multistage amplifiers have been discarded. Telescopic amplifier employ five stacked devices between the supply rails leading to excessive distortion for full-scale

operations.

For the present design a fully-differential, folded-cascode amplifier exploiting gain boosting techniques has been chosen. A simplified schematic is shown in Fig.3.2(a). The differential input pair is composed of a couple of PMOS transistors in order to allows low input common mode voltage operations; in order to prevent output swing limitations, huge devices on the output node has been designed, paying attention to the arising parasitic capacitances effects. The output common mode voltage is controlled by means of a switched-capacitors sensing circuit, shown in Fig.3.2(b); since during the acquisition phase the operational amplifier is in idle mode, the sensing capacitance C_{CM} can be refreshed to be used, during the subsequent amplification phase, to control the bias current generators M_3 and M_4.

As afore mentioned, in order to improve the amplifier DC gain, output resistance boosting technique has been exploited [22], [23], [24]. Boosting amplifiers A_{TOP} and A_{BOT} are designed as single-stage, fully-differential, folded-cascode amplifiers with continuous-time common mode control; a NMOS input pair amplifier has been implemented to drive the PMOS cascode devices whereas a PMOS input pair with similar performances has been designed to drive the NMOS cascode devices.

The compensation of a folded-cascode architecture is determined by the loading capacitance; the main operational amplifier is compensated by means of the holding capacitance whereas the gain boosting amplifiers are compensated thanks to the loading effects of the gate capacitance of the driven cascode devices.

The bias current are generated starting from a bandgap voltage reference; in example, the main amplifier tail current is nominally equal to $1.2\,\text{mA}$ whereas the bias current generators M_3 and M_4 sink a nominal bias current equal to $3.4\,\text{mA}$.

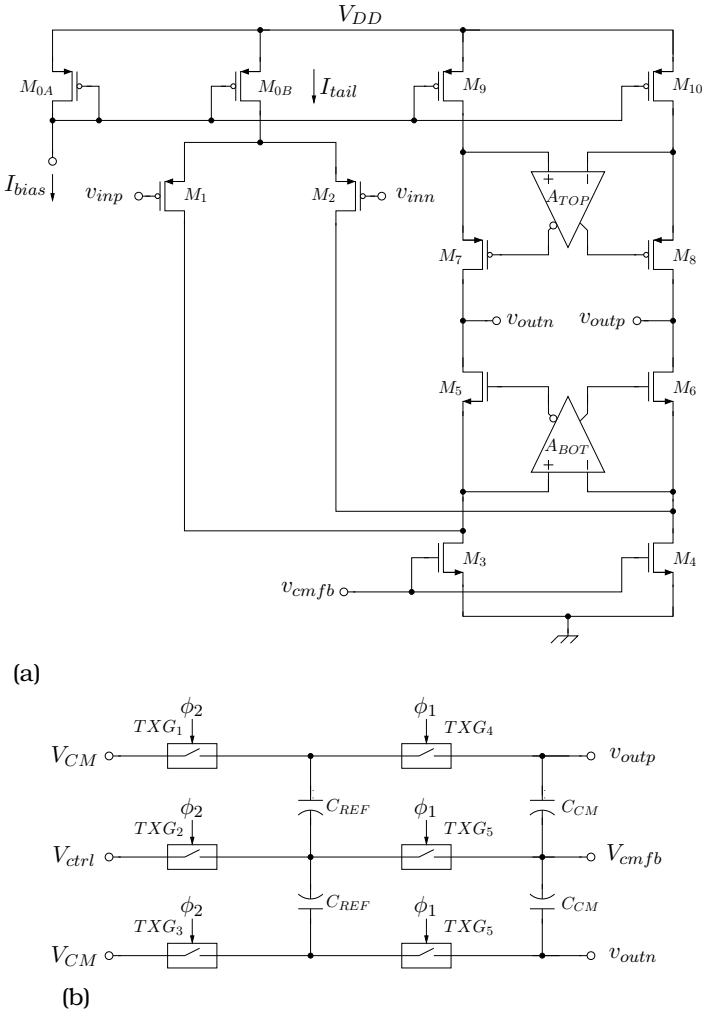


Figure 3.2: Flip-Around Track-and-Hold fully-differential folded-cascode Operational Amplifier with gain boosting: (a) main amplifier schematic (b) switched-capacitors common mode feedback control circuit.

Parameter	*Typical Case*	*Worst Case*
DC Gain [dB]	83	73
UGB [GHz]	1.73	0.96
Phase Margin [deg]	60	57
RMS Output Noise Voltage [μV] 1 Hz - 10 GHz/1 Hz - 3 GHz	193/86.1	322/128
Power Consumption [mW]	24	44

Table 3.2: Single-stage folded cascode operational amplifier with gain boosting performances.

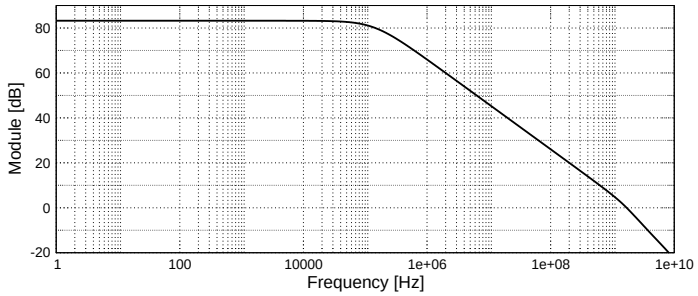
3.2.4 Simulations

An exhaustive set of transistor-level simulations was performed and some distinguishing results are here summarized; whereas not specified, the results shown are referred to the nominal conditions: 1.2 V of supply voltage at room temperature of 27°C assuming the process to be typical. The circuit was also simulated over the whole corner space considering a 10 % of tolerance over the supply voltage, a temperature range between 0 and 100°C and all the available process models (transistors, resistors and capacitors),

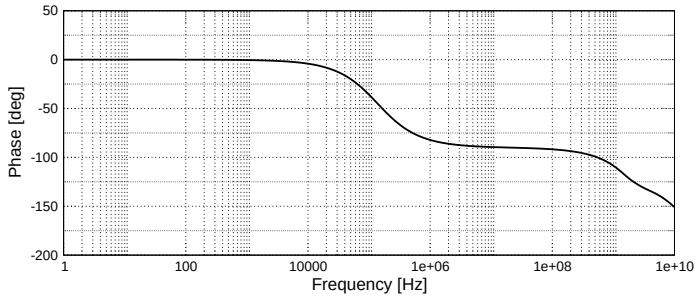
Operational Amplifier simulation results

As a first the frequency response of the operational amplifier described in section 3.2 has been evaluated. In Fig.3.3 the Bode diagrams (module and phase) of the OPA open-loop transfert function are depicted. A typical DC gain of 83 dB is proved whereas the unity gain bandwidth (UGB) results 1.73 GHz with a phase margin equal to 60°. The OPA performances have also been evaluated umbalancing the differential pair in order to evaluate the output swing: forcing the output differential voltage to be at the peak positive or negative voltage, the DC gain decrease up to 66 dB and 57 dB in the typical case and in the worst case one resplectively.

The OPA noise performance have been simulated. In Fig.3.4 the



(a)



(b)

Figure 3.3: Operational amplifier Bode plots (open-loop gain): (a) module (b) phase.

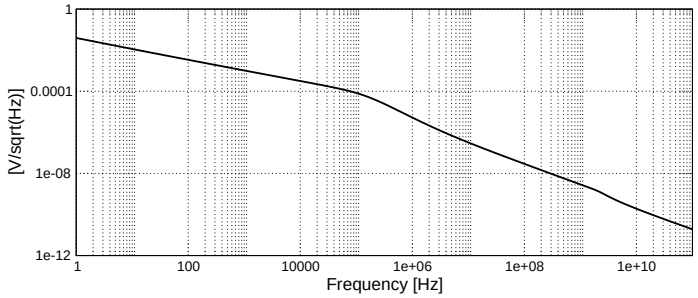


Figure 3.4: Operational amplifier output noise voltage (spectral density)

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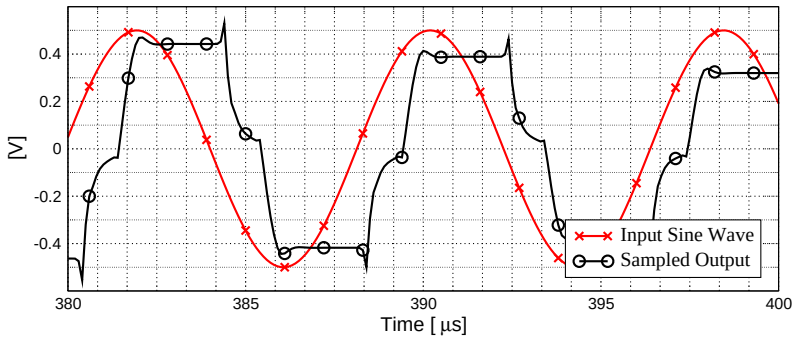


Figure 3.5: Flip-Around Track-and-Hold transient behaviour.

noise output voltage spectral density in typical conditions at $27°C$ is shown. The equivalent RMS output noise voltage, obtained integrating the spectral density over a conservative bandwidth between $1\,Hz$ and $10\,GHz$, results $193\,\mu V$; if the integration upper bound is reduced to $3\,GHz$ the RMS output noise voltage results $86.1\,\mu V$.

The operational power consumption is $24\,mW$ at $1.2\,V$ of supply voltage. In Tab.3.2 the operational amplifier typical and worst case performances are summarized.

Track-and-Hold simulation results

The transient behaviour of the sampling circuit was simulated with an full-scale, full-Nyquist input sine wave; In Fig.3.5 the input signal and the resulting sampled output are shown.

The linearity of the FATHA was evaluated by mean of transient simulations. As a first the switches performances was investigated in a dedicated test bench after which the whole track-and-hold was considered. Such performance, expressed in terms of (THD), was evaluated by means of Discrete Fourier Transform (DFT) of the held samples, when the circuit is driven by a full-scale, full-Nyquist sine wave ($125\,MHz$, 1 peak-to-peak volt). In Fig.3.6 the spectrum of sampled signal, delivered to the conversion chain, is shown with reference to

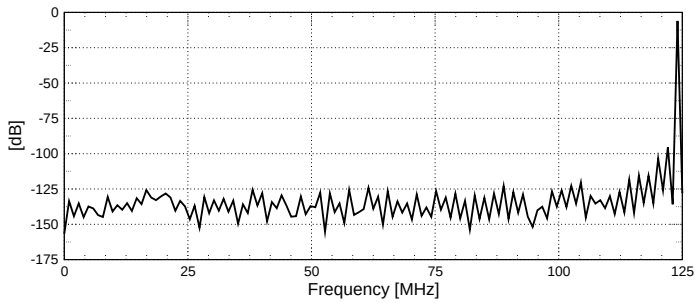
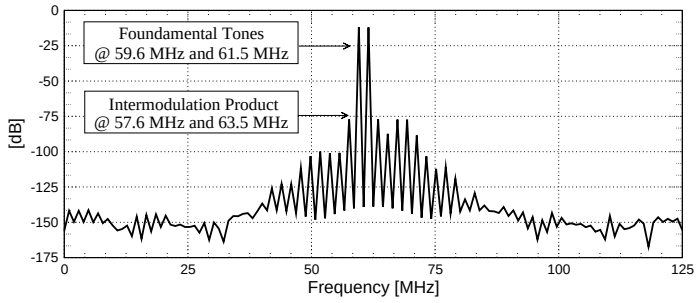


Figure 3.6: Flip-Around Track-and-Hold sampled output DFT result at full-Nyquist.

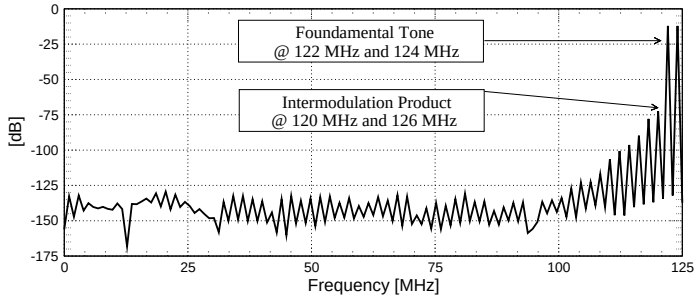
the typical case. The typical THD is lower than -92 dB corresponding, neglecting the SNR, to an ENOB higher than 15 bits whereas in the worst case the TDH increases up to -70 dB (ENOB$= 11.5$ bits). Further linearity verifications were performed evaluating the sampled signal spectra resulting from the two-tones test. In this case two half-scale sine waves (0.5 peak-to-peak volt) were considered and the Spurious Free Dynamic Range (SFDR) was evaluated. At full-Nyquist, considering two input tones at 122 MHz and 124 MHz, two intermodulation products appear at 120 MHz and 126 MHz and the typical SFDR results 93 dB; At half-Nyquist, considering two input tones at 59.6 MHz and 61.5 MHz, the intermodulation products results at 57.6 MHz and 63.5 MHz and the typical SFDR is 92 dB. In Fig.3.7 the spectra resulting from the two-tones test in typical conditions, at half and full-Nyquist, are shown.

The noise performance was also investigated. The equivalent RMS output noise voltage, obtained integrating the spectral density over a conservative bandwidth between 1 KHz and 10 GHz, results $156\,\mu$V

The overall power consumption results 24 mW and 44 mW in typical case and in worst case respectively; it is worth noticing that the only one significant contribution is the operational amplifier one. In Tab.3.3 the FATHA typical and worst case performances are collected.



(a)



(b)

Figure 3.7: Flip-Around Track-and-Hold sampled output DFT resulting from Two-Tones test: (a) at half-Nyquist (b) at full-Ntquist.

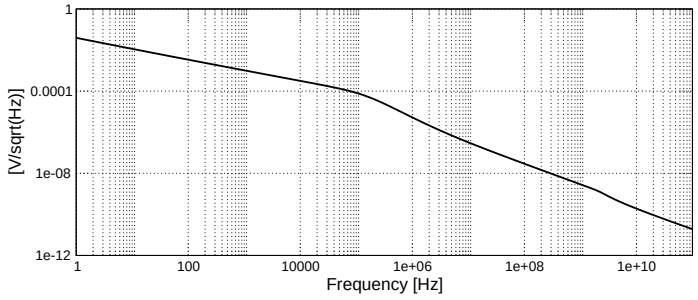


Figure 3.8: Flip-Around Track-and-Hold output noise voltage (spectral density)

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Parameter	*Typical Case*	*Worst Case*
THD [dB]	-92	-70
SFDR [dB] full-Nyquist/half-Nyquist	$93/92$	$78/73$
RMS Output Noise Voltage [μV] $1\,$KHz - $10\,$GHz	156	172
Power Consumption [mW]	24	44

Table 3.3: Flip-Around Track-and-Hold Amplifier performances.

3.3 Multiplying DAC

As briefly mentioned in the dissertation introduction the key element in a pipeline stage is the block performing the residue calculation, known as Multiplying Digital-to-Analog Converter (MDAC). In a pipeline chain each stage performs a low-resolution conversion (ADSC) and calculates the unconverted fraction of the analog signal; this fraction, the analog residue, properly amplifyed to exploit the converter full-scale range, is then fed to the subsequent stage. Since the residue calculation consist of an analog signals subtraction, switched-capacitors approach exploiting charge-sharing princyples allows to include all these features in a single block, the MDAC.

In this section the $2.5\,$bits MDAC chosen architecture is analyzed and the most important simulation results are reported.

3.3.1 MDAC Architecture

Regardless of the architectural implementation the input-output transcharacteristic of a $2.5\,$bits pipeline stage results from the $3\,$bit one by removing one decision level; being V_{REF} the positive full-scale voltage of the converter, the analog residue is obtained by subtracting from the analog input a signed fraction of V_{REF} according to ADSC results; the $2.5\,$bits stage gain is $2^{N-1} = 4$ where N represents the

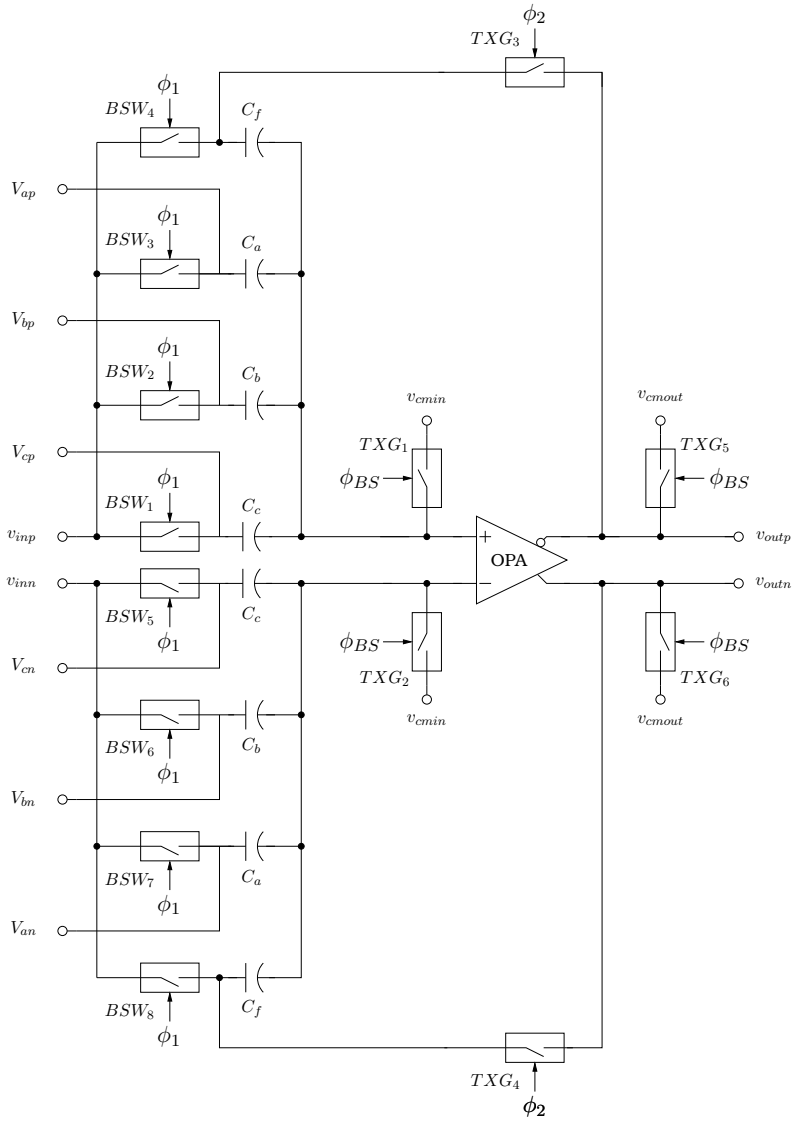


Figure 3.9: Charge-sharing MDAC schematic.

Decision Level	*Position*
TH_1	$-\frac{5}{8}V_{REF}$
TH_2	$-\frac{3}{8}V_{REF}$
TH_3	$-\frac{1}{8}V_{REF}$
TH_4	$+\frac{1}{8}V_{REF}$
TH_5	$+\frac{3}{8}V_{REF}$
TH_6	$+\frac{5}{8}V_{REF}$

Table 3.4: Trans-characteristic decision levels positions.

Stage Analog Input	*ADSC output*	
	Binary	*Signed Representation (D_1)*
$v_{i-1} < TH_1$	000	-3
$TH_1 < v_{i-1} < TH_2$	001	-2
$TH_2 < v_{i-1} < TH_3$	010	-1
$TH_3 < v_{i-1} < TH_4$	011	0
$TH_4 < v_{i-1} < TH_5$	100	$+1$
$TH_5 < v_{i-1} < TH_6$	101	$+2$
$v_{i-1} > TH_6$	110	$+3$

Table 3.5: ADSC output representations.

nominal resolution of the analog-to-digital sub-converter (i.e. 3). In Tab.3.4 the decision levels positions are collected whereas in Tab.3.5 the ADSC output coding is reported for purpose of clarity. Assuming D_1 to be the signed representation of the ADSC output, the amplified residue can be described as follows:

$$v_i = G_i v_{i-1} - D_1 V_{REF} \tag{3.4}$$

The 2.5 bits stage MDAC schematic is depicted in Fig.3.9. The operations consist of a sampling phase and an amplification one as well as for the track-and-hold; the flip-around circuit is driven by a 25 %

Stage Analog Input	V_{ap}	V_{an}	V_{bp}	V_{bn}	V_{cp}	V_{cn}
$v_{i-1} < TH_1$	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$
$TH_1 < v_{i-1} < TH_2$	0	0	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$
$TH_2 < v_{i-1} < TH_3$	0	0	0	0	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$
$TH_3 < v_{i-1} < TH_4$	0	0	0	0	0	0
$TH_4 < v_{i-1} < TH_5$	0	0	0	0	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$
$TH_5 < v_{i-1} < TH_6$	0	0	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$
$v_{i-1} > TH_6$	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$	$+\frac{V_{REF}}{2}$	$-\frac{V_{REF}}{2}$

Table 3.6: ADSC output representations.

duty cycle whereas the MDAC requires a $50\,\%$ clock. During the acquisition phase ϕ_1 all the capacitors are connected to the input signal by means of $BSW_{1p,2p,3p,4p}$ and $BSW_{1n,2n,3n,4n}$ while the capacitors bottom plate is connected to the input common mode voltage V_{CMIN}; in the meanwhile $TXG_{5,6}$ short the operational amplifier outputs terminals to the output common mode voltage V_{CMOUT} and the OPA is turned in idle mode; the tracking phase ends with the $TXG_{1,2}$ turning off performing the bottom plate sampling as in the flip-around circuit (ϕ_{BS}). After a short dead-time, the amplifying phase ϕ_2 starts and the feedback capacitors C_F top plate are connected to the operational amplifier output through the switches $TXG_{3,4}$; in order to perform the analog subtraction, the capacitors C_{ap}, C_{bp}, C_{cp}, as well as, C_{an}, C_{bn}, C_{cn}, are connected, according to the ADSC output, to $-V_{REF}$, 0 or $+V_{REF}$ (Tab.3.6). The charge-redistribution process occurs and at the end of ϕ_2, neglecting the possible incomplete settling, the output voltage described by (3.4) results.

3.3.2 Capacitors size, CMOS Switches and Operational Amplifier

The linearity demanded to the MDAC circuit calls for linear capacitor as Metal-Insulator-Metal topology (MIM). The minimum capacitors size, obtained by means of the accurated model in [21], is $200\,\text{fF}$ for the first stage, $190\,\text{fF}$ for the second and $70\,\text{fF}$ for the remaining stages; in order to avoid matching issues all the stages are designed considering $260\,\text{fF}$ elements.

The switches concerns are substantially the same presented for the flip-around track-and-hold (see section 2). The imput switches have been implemented using the rail-to-rail architecture with some modifications in order to lower the kick-back noise and the loading effect due to the boosting capacitor. Complementary transmission gates have been adopted for the remaining switches.

The MDAC OPA drives a comparable loading capacitance ($\approx 4 \times 260\,\text{fF}$) with similar constrains therefore the operational amplifier designed for the flip-around track-and-hold has been exploited. The operational amplifier has been equipped to provide a low-performance, low-power mode by reducing the bias currents; since the required MDAC performances scale down among the chain, the operational amplifier can be used for all the chain stages without waste of power.

3.3.3 Simulations

MDAC simulation results

The MDAC performances have been evaluated by means of transient analysis feeding the circuits with different input signals: as well as in the sample-and-hold circuits the quality of the amplificated residue provided to the following stage depends on the settling transient during the amplification phase. In the pipeline chain the MDAC input is driven by a sampled and then constant signal therefore time varying input signal are not reported here. The most severe condition occurs when two subsequent samples exhibit the maximum excur-

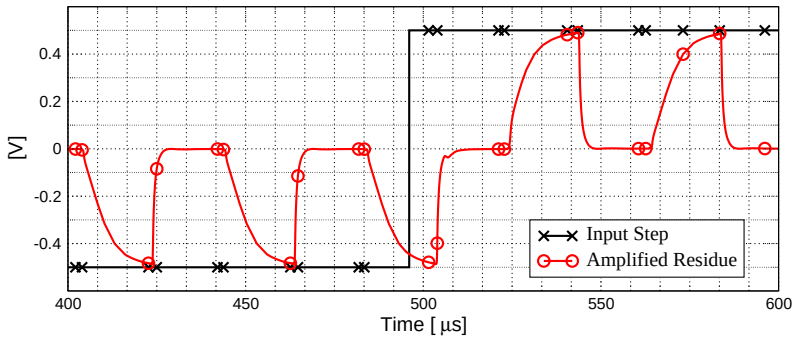


Figure 3.10: MDAC transient behaviour.

sion as possible; Fig.3.10 shows the input and the output voltages when the circuit is fed with a DC signal abruptly swinging from negative full-scale, i.e. $-500\,\text{mV}$ to the positive full-scale, i.e. $+500\,\text{mV}$. In Fig.3.11 the MDAC trans-caracteristic is depicted; since the curve results from a transient behaviour with a slow input ramp from the negative full-scale to the positive one, it is suitable to evaluate the linearity performances of the operational amplifier. This result is also useful to calculate, by interpolation, the MDAC model parameters, in example the actual stage gain and the third-order coefficient, used in the calibration methods investigation reported in chapter 4.

3.4 Coarse ADC

Each pipeline stage performs a coarse analog-to-digital conversion by means of an analog-to-digital sub-converter, typically implemented with a flash architecture. Since the $2.5\,\text{bits}$ stage exploits the RSD correction technique, a $3\,\text{bits}$ flash converter with six decision levels and as many latching comparators has been investigated.

The sub-converter here presented is also suitable to implemente the back-end stage; the additional bit (recalling the pipeline configuration chosen 333332) can be simply removed from the output data

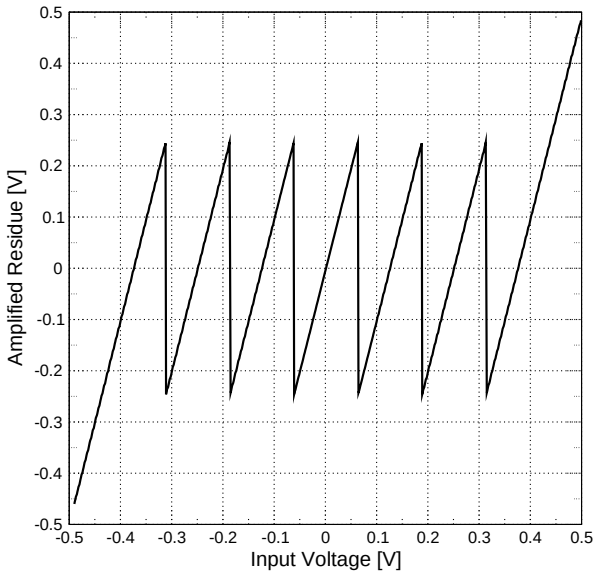


Figure 3.11: Actual MDAC trans-characteristic.

by truncating or used to improve the backgroud calibration technique described in chapter 4.

The encoding logic, the references generator and the multiplexing network driving the MDAC are, at the moment, in a preliminary versions and none significant results are available therefore, this section is focused on the latching comparator.

3.4.1 Comparator

The key features demanded to the latching comparator to be employed in the flash sub-converter is a very short conversion time and low kick-back noise: the former is mandatory to provide as fast as possible the voltage references to the MDAC circuit at the amplifying phase start; the latter is important in order to avoid the disturbances bouncing back toward the analog input to be stored by the MDAC sampling

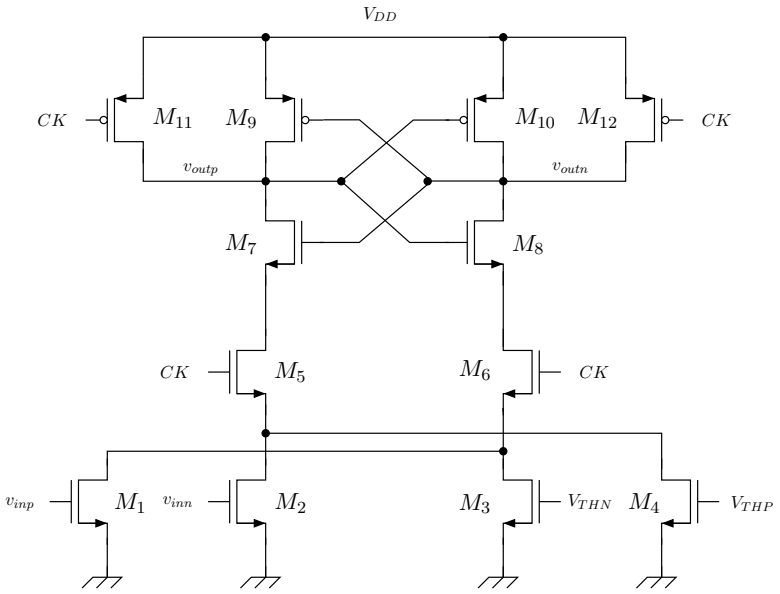


Figure 3.12: Analog-to-digital sub-converter latching comparator.

capacitors, degrading the residue generation. Typically, input referred offset and non-linearity are negligible thanks to the RSD correction.

The requirements above can be obtained by means of the latching comparator circuit depicted in Fig.3.12. Fast response results from the positive feedback occuring at the latching instant. The circuit operation can be described as follows. During the MDAC sampling phase ϕ_1 the control signal CK is low and the comparator is turned off; M_{11} and M_{12} pull up to the supply voltage the output nodes and M_5 and M_6 isolate the input transistors M_1, M_2, M_3 and M_4. At the end of the sampling phase the input differential voltage $v_{inp} - v_{inn}$ must be compared to the threshold $v_{THP} - v_{THM}$; at the CK rising edge (phi_2) the input devices are connected to the positive feedback loop composed of M_7, M_8, M_{10} and M_11 and the output nodes switch according to the

following consideration:

$$(v_{inp} - v_{inn}) > (v_{THP} - v_{THN}) \Rightarrow v_{outp} = V_{dd} \; and \; v_{outn} = 0 \qquad (3.5)$$

The output decisions levels, during the sampling phase ϕ_1 are frozen by means of two digital latches not shown in figure.

In order to limit the kick-back noise, the capacitive coupling of the kick-back pulse at the CK rising edge must be attenuated by means of thick-oxide transistors as input devices (M_1, M_2, M_3 and M_4). If the resulting attenuation is not enough or thick-oxide mosfets are not available, significant improvements result from a proper timing choice: the latching instant must be anticipate with respect to the MDAC bottom sampling in order to let the kick-back disturbance fade away.

3.4.2 Simulations

Comparator simulation results

Transient simulations were performed to evaluate the speed performances of the single latching comparator. The propagation delay is calculated as difference between the output transition instant (at $50\,\%$ of supply voltage) and the latching clock CK transition instant, when the differential input exhibits a small umbalancement δ_{in}, with respect to the threshold voltage $v_{THP} - v_{THM}$. Since each comparator in the flash ladder works on a different input common mode voltage, the simulation abobe have been performed in correspondence to all the possible threshold. The propagation delay, resulting from a δ_{in} of $100\,$pV is lower than $300\,$ps. Transient simulations have been used also to prove the kick-back noise tolerance.

The Bit Error Rate (BER) of a comparator to be used in an analog-to-digital converter is a matter of great importance: BER was evaluated by means of the method illustrated in [10] and [25]: the BER results lower than 10^{-10} over the whole corner space.

Since the proposed comparator does not sink current from the supply rail in static condition, the only one dissipation occurs at latching transient. Low power consumption results from simulation: the worst case power consumption does not exceed $127\,\mu$W leading to an estimated flash overall budget lower than 1 mW.

3.5 Final Considerations

The schematic-level simulation results allow to draw some design considerations. With regard to the FATHA as conversion channel front-end, performances suitable for 12 bits operation are proved. None significant issue appear, however, lower noise levels could be usefull especially to provide margin for the following stages.

The MDAC performances must be improved: as shown in Fig.**??** the steps response exhibits long slew-rate phase penalizing the residue settling. Evaluating the trans-characteristic in Fig.3.11 strong non-linearity is visible especially at fill-scale input amplitude.

Based on the highlighted deficiencies, two possible approaches can be considered: improve the weakness above at cost of higher power consumption or calibrate the stages errors. It is worth noticing that proving the calibration algorithm efficiency, the stages performance could be futhermore degraded, in order to lower the power consumption, exploiting the calibration contribution.

Chapter 4

A/D Converters Calibration Techniques: Gain Error, Non-Linearity and Capacitors Mismatch

The A/D converters' performance limitations arising from technology scaling, especially in the front-end converters, call for innovative calibration techniques. Unlike analog circuitry, digital computation capability takes benefit from the usage of deep-submicron CMOS processes, hence in the last few years the research effort has been focused on the study of digital correction algorithm.

With reference to the pipeline architecture shown in chapter 3, as extensively discussed, the key building block is the residue amplifier. The ADC overall resolution requirements and then the performances in terms of speed, noise and linearity demanded to each conversion stage lead to a lower bound of power consumption that represent the true bottleneck in most common applications [27], [28]. In the nineties the design effort has been oriented to the optimization of the analog system elements: for example stage scaling was considered in [29],

[30], [31], [32], optimum stage resolution in [33], [34], operational amplifier sharing in [35], [36], etc.

The limited voltage headroom resulting from the use of deep-submicron technologies closed the door to further improvements at analog design level, hence the most reasonable choice, is taking note of the analog block limits and develop digital techniques to estimate and correct all the non-idealities in the residue amplifier.

In this chapter two different calibration techniques are considered: the first one [37] allows background calibration of gain and non-linearity; an exhaustive set of behavioural simulations were performed in order to discover the limits and the pertinence with the designed pipeline stage, illustrated in chapter 3. Since the major limitation in the proposed method results from the assumption of negligible capacitors' mismatch, a second background technique, aiming at capacitors' mismatch estimation [38], was considered . Finally the possibility of integration of the two techniques is discussed.

4.1 Gain and Non-Linearity Background Calibration

4.1.1 Algorithm Description

Actual Gain Estimation

Recalling the notation adopted in chapter 3, an L-stages pipeline ADC can be represented as in Fig.4.1(a) whereas Fig.4.1(b) describes in detail the first stage. The latter is composed of the following blocks: an input sample-and-hold circuit with gain G_0, typically equal to one; an analog-to-digital sub-converter (ADSC) producing a N_1 bits digital word D_1, where N_1 represents the resolution of the stage; a digital-to-analog sub-converter (DASC); a subtractor node and a residue amplifier which produce the residue r_1 and the amplified residue v_1, respectively. All the following (L-1)stages form the Back-End analog-to-digital converter (BEADC) providing the digital word D_{BE}. The in-

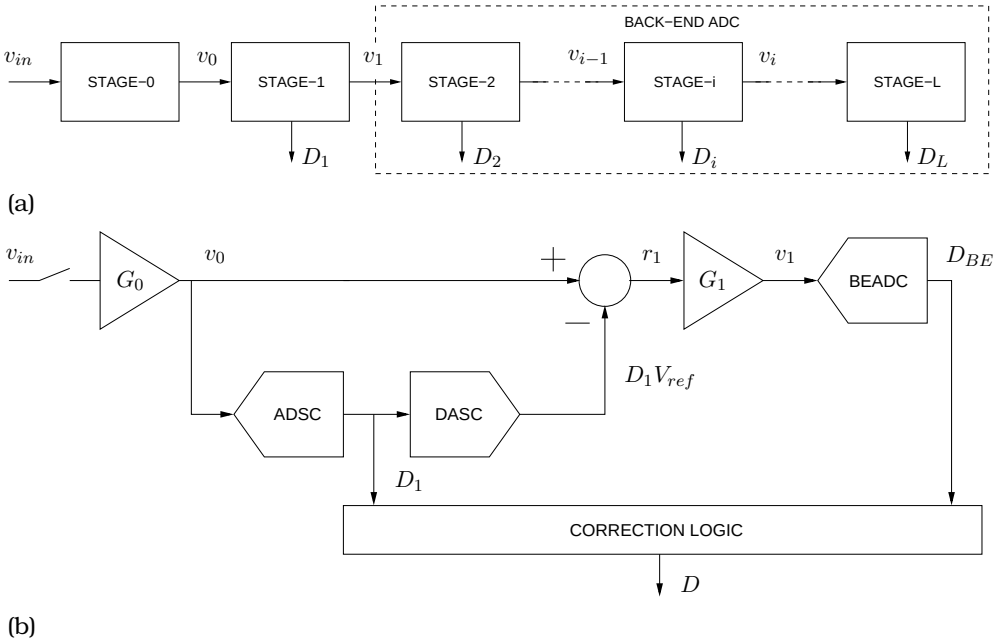


Figure 4.1: Pipeline ADC Architecture: (a) L-stage pipeline chain;(b) first two stages details

formation D_1 provided by the first stage must be combined with the back-end conversion result D_{BE} in order to obtain the correct output word:

$$D = D_1 + \frac{1}{G_1} D_{BE} \tag{4.1}$$

Assuming the ADSC non-idealities to be corrected by means of Code Redundancy Techniques [29],[39], in order to prevent over-range, the main remaining sources of error are found in inter-stage amplification and in digital-to-analog sub-conversion. In the present design the digital-to-analog sub-conversion is based on switched-capacitors techniques, hence the main source of DASC linearity error is capacitors' mismatch. For this reason the required overall resolution can be

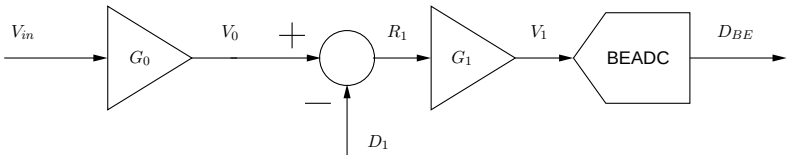


Figure 4.2: Pipeline ADC stage: normalized representation

obtained adopting mismatch correction algorithm as shown in paragraph 4.2. If equation (4.1) were applied in a real world case, assuming for G_1 the nominal value, a wrong output code would be obtained, even if DASC non-linearities can be neglected. On the contrary, by estimating the actual gain and replacing G_1 with the obtained estimate $\hat{G_1}$, (4.1) returns the correct output code:

$$D = D_1 + \frac{1}{\hat{G_1}} D_{BE} \tag{4.2}$$

V_{ref} being the positive full-scale voltage of the overall ADC, a normalized notation can be introduced as follows and the first pipeline stage can be represented as in Fig.4.2:

$$V_{in} = \frac{v_{in}}{V_{ref}} \tag{4.3}$$

$$V_0 = \frac{v_0}{V_{ref}} \tag{4.4}$$

$$R_1 = \frac{r_1}{V_{ref}} \tag{4.5}$$

$$V_1 = \frac{v_1}{V_{ref}} \tag{4.6}$$

Assuming the back-end conversion to be ideal and neglecting the quantization error V_1 can be approximated as

$$V_1 \approx D_{BE} \tag{4.7}$$

and substituting in equation (4.1) it results

$$G_0 V_{in} = V_0 = D_1 + \frac{1}{G_1} V_1 \tag{4.8}$$

and then

$$D_{BE} \approx V_1 = G_1 (V_0 - D_1) \tag{4.9}$$

Sobstituting (4.9) in (4.2)

$$D = D_1 + \frac{G_1}{\hat{G_1}} (V_0 - D_1) \tag{4.10}$$

Defining

$$m_1 = \frac{1}{G_1} \tag{4.11}$$

$$\hat{m_1} = \frac{1}{\hat{G_1}} \tag{4.12}$$

$$\varepsilon_m = \frac{\hat{m_1} - m_1}{m_1} \tag{4.13}$$

equation (4.10) becomes

$$\begin{aligned} D &= D_1 + \hat{m_1} G_1 (V_0 - D_1) = \\ &= D_1 + (1 + \varepsilon_m)(V_0 - D_1) = \\ &= V_0 (1 + \varepsilon_m) - D_1 \varepsilon_m \end{aligned} \tag{4.14}$$

where ε_m represents the relative error in the gain estimation ($\hat{m_1} = 1/\hat{G_1}$). If for a fixed input sample V_0 a well-known alteration in D_1 is introduced, a variation in the output code D results and this variation is proportional to the relative estimation error ε_m. The above alteration can be obtained by shifting the ADSC thresholds in order to produce two possible D_1 results, according to a random variable $S \in \{-1, +1\}$. D_1^+ and D_1^- being the two possible DASC outputs, by defining

$$\overline{D_1} = \frac{1}{2} \left(D_1^+ + D_1^- \right) \tag{4.15}$$

$$\Delta D_1 = \frac{1}{2} |D_1^+ - D_1^-| \tag{4.16}$$

the DASC output can be written as

$$D_1 = \overline{D}_1 + S\Delta D_1 \tag{4.17}$$

Therefore

$$D = V_0\left(1+\varepsilon_m\right) - \overline{D}_1\varepsilon_m - S\Delta D_1\varepsilon_m \tag{4.18}$$

It is worth to notice that by adopting the Code Redundancy Correction, if LSB is the stage Least-Significant-Bit, a $LSB/2$ shift of the decision levels of the flash ADSC, due for example to comparators' offsets, can be tolerated. Therefore, the on purpose shift of the decision levels described above does not affect the converter operation. In order to preserve the Code Redundancy benefit, ΔD_1 must be kept small. Assuming the Redundancy margin to be equally shared among positive and negative offset, $\pm LSB/4$ of ADSC levels deviation is acceptable; considering $\overline{D}_1$ equal to the nominal DASC output (without on purpose shifting) and assuming ΔD_1 to be $LSB/8$ a Code Redundancy margin equal to $\pm LSB/8$ still remains. Fig.4.3 shows the residue curve resulting for a 2.5 bit stage, assuming the conditions described above.

Since S is a zero-mean random sequence uncorrelated with the input signal, $S\Delta D_1$ can be considered as a calibration signal. Therefore, by correlating the conversion result D with the sequence S itself, an estimation of the gain error ε_m is obtained. Consider the signal x defined as

$$x = D - \overline{D}_1 \tag{4.19}$$

Replacing D with the result (4.18)

$$\begin{aligned} x &= D - \overline{D}_1 = \\ &= V_0\left(1+\varepsilon_m\right) - \overline{D}_1\varepsilon_m - S\Delta D_1\varepsilon_m - \overline{D}_1 = \\ &= \left(1+\varepsilon_m\right)\left(V_0 - \overline{D}_1\right) - S\Delta D_1\varepsilon_m \end{aligned} \tag{4.20}$$

The signal x is composed of an input dependent term,

$$I\left(V_0\right) = \left(1+\varepsilon_m\right)\left(V_0 - \overline{D}_1\right) \tag{4.21}$$

(4.22)

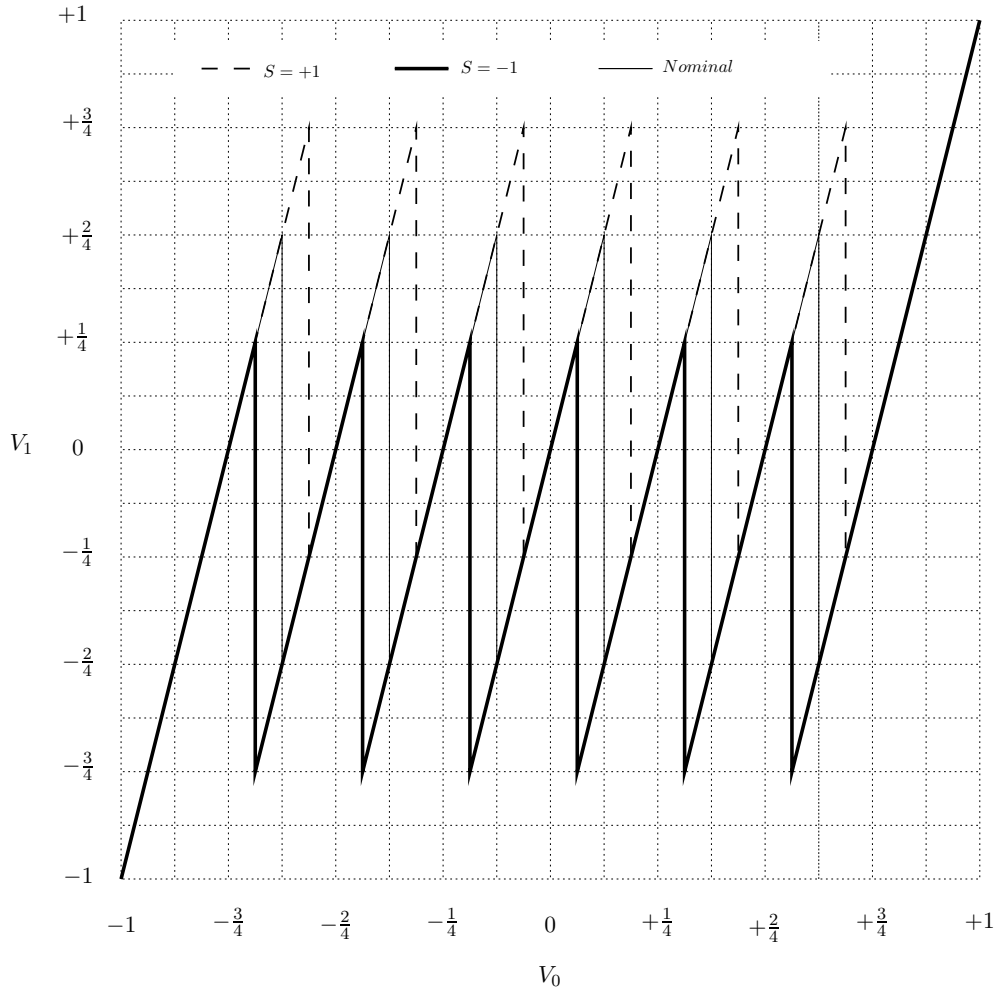


Figure 4.3: 2.5 bit, gain of 4 Pipeline ADC stage residue plot, with calibration signal added.

and a quantity related to the calibration signal and to the relative gain error, both uncorrelated with the random sequence S:

$$\varepsilon = -\Delta D_1 \varepsilon_m \tag{4.23}$$

hence

$$x = I(V_0) + S\varepsilon \tag{4.24}$$

Multiplying (4.24) by the random sequence S, reminding that $S = \pm 1$ and therefore $S^2 = 1$,

$$Sx = SI(V_0) + \varepsilon \tag{4.25}$$

Since S is a pseudo-random sequence with zero mean and uncorrelated with the input signal V_{in} and therefore with V_0, the mean value of Sx is proportional to the gain estimation error:

$$\begin{aligned} E\{Sx\} &= E\{SI(V_0)\} + E\{\varepsilon\} = \\ &= E\{S\}E\{I(V_0)\} + E\{\varepsilon\} = E\{\varepsilon\} \end{aligned} \tag{4.26}$$

and then

$$E\{Sx\} = E\{\varepsilon\} = \varepsilon = -\Delta D_1 \varepsilon_m = -\frac{\Delta D_1}{m_1}(\hat{m_1} - m_1) \tag{4.27}$$

In other terms, each sample of Sx represent a noisy estimate of the gain error and can be used to calculate $\hat{m_1}$ by means of a weighted average:

$$\hat{m_1}[k] = \hat{m_1}[k-1] + \mu_m S[k-1]x[k-1] \tag{4.28}$$

In (4.28) μ_m stands for the weighting coefficient in the updating sequence: on one hand a high value of μ_m leads to faster initial convergence and higher tracking speed; on the other hand a high value results in a higher steady-state error.

Non-Linearity Correction

The analysis presented in the previous section results in an estimation of the actual interstage gain to be used in equation (4.1) to compose the output word. Especially in low-voltage designs, where a full-scale signal, not far from the supply rails, must be converted, all the non-linear effects in the interstage amplification become relevant. Since the residue amplifier gain becomes dependent on the input signal level, the algorithm discussed in the previous section must be modified in order to account for the introduced distortion. Moreover, low-power constraints lead to significant limitations in terms of operational amplifier's bandwidth and current driving capability, hence non-linearities related to slew-rate combined to incomplete settling appear.

Fully differential operation removes all the even-order non-linear terms, provided that mismatch effects can be neglected. Considering the stage architecture described in chapter 3, a third-order non-linearity model should therefore ensure adequate accuracy. Fig.4.4 shows a qualitative and exaggerated representation of the impact of a third-order non-linearity on the stage I/O characteristic. As it is reasonable to expect, distortion increases with the signal amplitude and this results in a bending at the upper and lower ends of the residue curve segments.

The non-linearities described above can be represented adopting the model in Fig.4.5; as a consequence equations (4.7) and (4.8) must be modified as follows

$$G_0 V_{in} = V_0 = D_1 + \frac{1}{G_1}\left(V_1 + b_1 V_1^3\right) \tag{4.29}$$

where b_1 represents the cubic term coefficient. Being $\hat{b_1}$ an estimate of b_1, the conversion result can be written as

$$D = D_1 + \hat{m_1}\left(D_{BE} + \hat{b_1} D_{BE}^3\right) \tag{4.30}$$

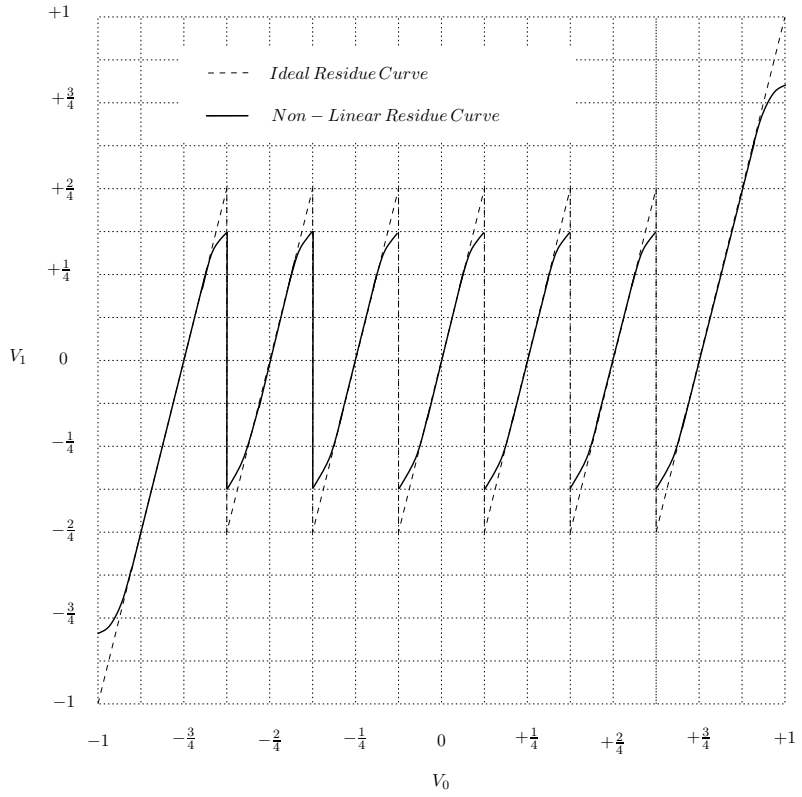


Figure 4.4: Example of third-order non-linearity in the residue curve.

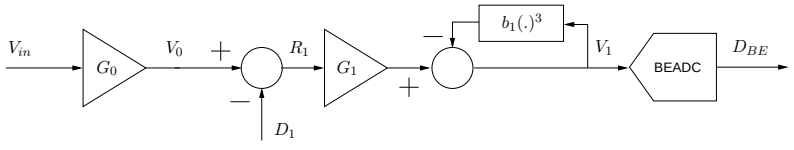


Figure 4.5: Pipeline ADC stage with third-order non-linearity model: normalized representation

Assuming one more time the back-end to be ideal ($D_{BE} \approx V_1$) equation (4.9) becomes

$$D_{BE} \approx V_1 = G_1 (V_0 - D_1) - b_1 D_{BE}^3 \tag{4.31}$$

and then

$$D = V_0 (1 + \varepsilon_m) - D_1 \varepsilon_m + \hat{m_1} \left(\hat{b_1} - b_1 \right) D_{BE}^3 \tag{4.32}$$

Since the third-order coefficient b_1 is small (hypothesis proved by simulating the designed pipeline stage presented in chapter 3 the third power of D_{BE} in 4.32 can be calculated by means of (4.33):

$$D_{BE}^3 = \left[G_1 (V_0 - D_1) - b_1 D_{BE}^3 \right]^3 \approx G_1^3 (V_0 - D_1)^3 \tag{4.33}$$

By substituting (4.33) in (4.32)

$$D = V_0 (1 + \varepsilon_m) - D_1 \varepsilon_m + \hat{m_1} G_1^3 \left(\hat{b_1} - b_1 \right) (V_0 - D_1)^3 \tag{4.34}$$

Adding the calibration signal as shown in (4.17) and defining

$$P = \left(V_0 - \overline{D}_1 \right) \tag{4.35}$$

it turns out that

$$(V_0 - D_1)^3 = P^3 + 3 (\Delta D_1)^2 P - S \Delta D_1 \left[3P^3 + (\Delta D_1)^2 \right] \tag{4.36}$$

obtained reminding that $S \in \{-1, +1\}$ and $S^2 = 1$ and $S^3 = S$. in Leaving, as in the previous section,

$$x = D - \overline{D}_1 \tag{4.37}$$

results in

$$x = I (V_0) + S \varepsilon (V_0) \tag{4.38}$$

where

$$I (V_0) = P (1 + \varepsilon_m) + P^3 \varepsilon_b + 3P (\Delta D_1)^2 \varepsilon_b \tag{4.39}$$

and

$$\varepsilon(V_0) = -\Delta D_1 \varepsilon_m - (\Delta D_1)^3 \varepsilon_b - 3\Delta D_1 P^2 \varepsilon_b \tag{4.40}$$

are both uncorrelated with S, and where

$$\varepsilon_m = \frac{\hat{m_1} - m_1}{m_1} \tag{4.41}$$

and

$$\varepsilon_b = G_1^3 \hat{m_1} \left(\hat{b_1} - b_1 \right) \tag{4.42}$$

It is important to note that both the terms I and ε now depend on the input signal through V_0; ε_b, similarly to ε_m for the gain, is proportional to the estimation error $(\hat{b_1} - b_1)$ of the non-linearity coefficient. Since the term containing ε_b in (4.40) is correlated to P^2, ε_b itself can be estimated by calculating the covariance of Sx and P^2 as follows [1]:

$$\begin{aligned} K_{(Sx)P^2} &= E\{(Sx)\,P^2\} - E\{Sx\}E\{P^2\} = \\ &= E\{\varepsilon(V_0)\,P^2\} - E\{\varepsilon(V_0)\}E\{P^2\} \end{aligned} \tag{4.43}$$

Since the above expression of K depends on $E\{P^2\}$ and therefore on the unknown input signal V_0, it cannot be directly used in order to estimate ε_b. However, by approximating the input signal V_0 with the conversion result D, $x = D - \overline{D}_1$ can be used instead of $P = V_0 - \overline{D}_1$. Thus ε_b can then be estimated by calculating the covariance of Sx and x^2, $K_{(Sx)x^2}$ as follows:

$$K_{(Sx)x^2} = E\{(Sx)\,x^2\} - E\{Sx\}E\{x^2\} \tag{4.44}$$

Since S has zero mean, neglecting all the high order terms in ε_b and ε_m,

$$E\{(Sx)\,x^2\} = E\{\varepsilon^3(V_0)\} + 3E\{\varepsilon(V_0)\,I^2(V_0)\} \approx 3E\{\varepsilon(V_0)\,P^2\} \tag{4.45}$$

[1] The covariance of A and B is defined as $K_{AB} = E\{AB\} - E\{A\}E\{B\}$

and

$$E\{Sx\}E\{x^2\} = E\{\varepsilon(V_0)\}E\{\varepsilon^2(V_0) + I^2(V_0)\} \approx E\{\varepsilon(V_0)\}E\{P^2\} \quad (4.46)$$

hence

$$K_{(Sx)x^2} \approx 3E\{\varepsilon(V_0) - E\{\varepsilon(V_0)\}E\{P^2\} \quad (4.47)$$

Comparing the equation (4.43) and the result (4.47) a factor 3 appears in the latter; therefore a modified version B of $K_{(Sx)P^2}$

$$B = E\{(Sx)x^2\} - 3E\{Sx\}E\{x^2\} \quad (4.48)$$

must be used to obtain an estimate of ε_b, since it may be verified by substitution of (4.45) and (4.46) into (4.48) that

$$B \approx 3E\{\varepsilon(V_0)P^2\} - 2E\{\varepsilon(V_0)\}E\{P^2\} = -9\varepsilon_b \Delta D_1 K_{P^2P^2} \quad (4.49)$$

B, therefore, is proportional to ε_b and thus, through (4.42), to the error $(\hat{b_1} - b_1)$ affecting the estimate of coefficient b_1. Note that the computation of B requires the knowledge of S and x only, from which noisy estimates of the average values of Sx^3, Sx and x^2 can be obtained as arithmetical means over a large number N_{avg} of samples as follows

$$\hat{E}[w] = \frac{1}{N_{avg}} \sum_{k=1}^{N_{avg}} w[k]. \quad (4.50)$$

Therefore an estimate $\hat{B}$ of B is provided by

$$\hat{B} = \hat{E}\{(Sx)x^2\} - 3\hat{E}\{Sx\}\hat{E}\{x^2\} \quad (4.51)$$

By adopting the same update algorithm described for $\hat{m_1}$, the non-linearity coefficient estimate $\hat{b_1}$ can be updated every N_{avg} samples according to

$$\hat{b_1}[k] = \hat{b_1}[k-1] + \mu_b \hat{B}[k-1]. \quad (4.52)$$

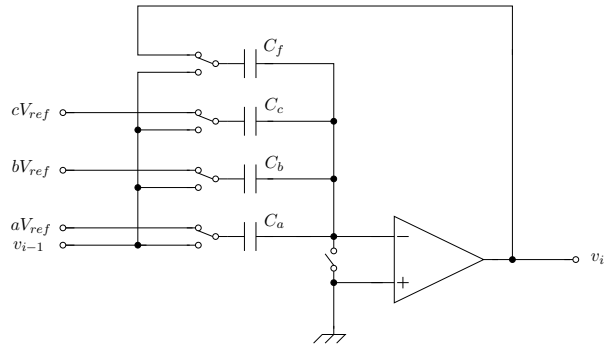


Figure 4.6: Single-ended switched capacitor 2.5, gain of 4 MDAC

Similarly to μ_m, the μ_b value determines the trade-off (tracking speed) versus (steady-state error). Moreover, convergence and tracking speed depend on the activity of the input signal: the higher the amplitude difference between subsequent samples, the higher the variation in P and therefore in x, bringing a wealth of information about amplifier non-linearity; in the limiting case of DC input, no information about non linearity is brought by the new arriving samples, hence no convergence is observed.

4.1.2 Matlab® Gain and Non-Linearity Calibration Model

A Matlab® model of the described calibration algorithm was implemented and simulated in order to assess the operation limits.

According to the design proposed in chapter 3 and the single-ended representation in Fig.4.6 [26] and [21], the pipeline stage model implements the following transfer function:

$$v_{out} = \left(1 - e^{-2\pi T_S \frac{f_T}{G_i}}\right) \left[v_{in} \frac{C_{MDAC}}{C_f + \frac{C_p + C_{MDAC}}{A}} - V_{ref} \frac{C_{SEL}}{C_f + \frac{C_p + C_{MDAC}}{A}} \right] \tag{4.53}$$

where, assuming a 2.5 bit, gain of 4 stage,

ADSC digital output	*a*	*b*	*c*	C_{SEL}
110	+1	+1	+1	$C_a + C_b + C_c$
101	+1	+1	0	$C_a + C_b$
100	+1	0	0	C_a
011	0	0	0	0
010	-1	0	0	$-C_a$
001	-1	-1	0	$-C_a - C_b$
000	-1	-1	-1	$-C_a - C_b - C_c$

Table 4.1: ADSC output coding.

T_S : is the sampling period of the pipeline chain.

f_T : is the UGB of the operational amplifier.

G_i : is the ideal stage gain.

C_{MDAC} : is the total MDAC capacitance; since C_a, C_b and C_c are the input reference capacitances and C_f is the feedback capacitance of the charge sharing architecture,

$$C_{MDAC} = C_a + C_b + C_c + C_f \tag{4.54}$$

A : is the operational amplifier DC gain.

C_p : is the operational amplifier parasitic input capacitance.

C_{SEL} : is the MDAC capacitance connected to $\pm V_{ref}$ according to the ADSC output defined as follows:

$$C_{SEL} = aC_a + bC_b + cC_c \tag{4.55}$$

For the sake of simplicity the ADSC result D_1 is also represented according to Tab.4.1, by means of three integer a, b and c.

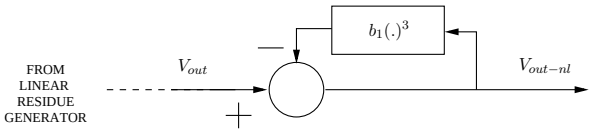


Figure 4.7: Schematic representation of the third-order non-linearity model

The equation (4.53), normalized to V_{ref} can be written as

$$\begin{aligned} V_{out} &= \left(1 - e^{-2\pi T_S \frac{f_T}{G_i}}\right) \frac{1}{1 + \frac{C_p + C_{MDAC}}{AC_f}} \frac{C_{MDAC}}{C_f} \left(V_{in} - \frac{C_{SEL}}{C_{MDAC}}\right) = \\ &= (1 - \varepsilon_S) \left(\frac{1}{1 + \varepsilon_A}\right) \frac{C_{MDAC}}{C_f} \left(V_{in} - \frac{C_{SEL}}{C_{MDAC}}\right) \end{aligned} \tag{4.56}$$

The above expression of the amplified residue V_{out} was derived considering linear operation of the operational amplifier; in order to include in the model the third-order non-linearity arising from the output swing and slew-rate limitations described in the previous section, the residue V_{out} must be elaborated according to Fig.4.7:

$$V_{out-nl} = V_{out} - b_1 V_{out-nl}^3 \tag{4.57}$$

The non-linear residue is calculated as radix of the cubic equation

$$b_1 V_{out-nl}^3 + V_{out-nl} - V_{out} = 0 \tag{4.58}$$

A realistic value of b_1 has been obtained by interpolating the residue curve of the designed MDAC illustrated in chapter 3 (see. simulation results in chapter 4.1.3). The worst-case stage parameters, derived from the above mentioned design, are summarized in Tab.4.2.

In Fig.4.8 a block diagram describing the stage calibration model is shown. The pipeline stage provides the output code D_1 and the amplified non-linear residue V_{out-nl} and both are used to perform the gain and non-linearity coefficient estimation as illustrated in the algorithm description. V_{out-nl} is then fed to an ideal back-end converter

Parameter	*Worst-Case Value*
Operational Amplifier DC Gain (A)	70 dB
Operational Amplifier UGB (f_T)	1.2 GHz
Operational Amplifier Parasitic Input Capacitance (C_p)	20 fF
Gain Coefficient (m_1)	0.2562
Third-Order Non-Linearity Coefficient (b_1)	0.07
Actual Stage Gain (see eq.(4.56))	3.9028

Table 4.2: Model parameters derived from the stage design in chapter 3 (assuming a clock frequency of 250 MHz).

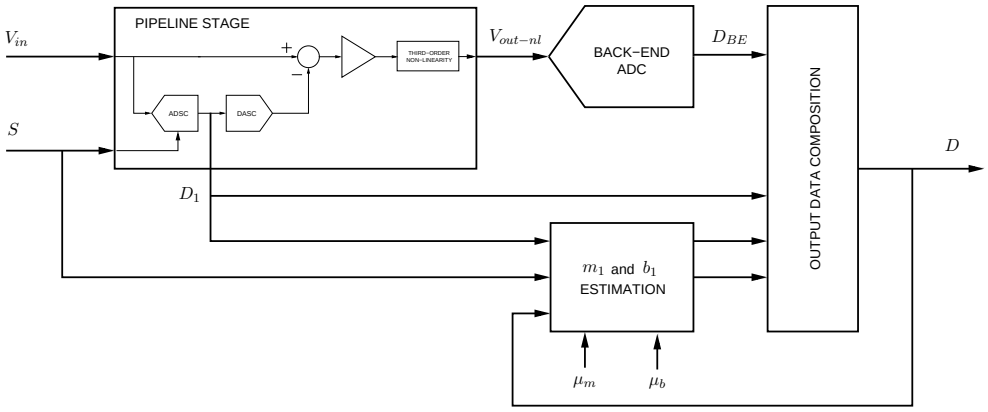


Figure 4.8: Pipeline stage and Calibration section block diagram.

that returns D_{BE}. Once the gain estimate $\hat{m_1}$ and the non-linearity coefficient estimate $\hat{b_1}$ are calculated, D_{BE} and D_1 are composed according equation (4.30) in order to provide the calibrated output code D. This latter is also fed back to the calibration logic.

The number representation must be taken into account. All the analogue operations were represented using *double* precision; the estimation of coefficients ($\hat{m_1}$ and $\hat{b_1}$) was performed assuming a 32 bit *fixed point* representation; however, correct operation was demonstrated also with lower word lengths. Different back-end configurations were evaluated: slight benefits can be obtained by increasing the number of bits in the back-end conversion; in any case, in order to evaluate the overall performance, the output data is truncated assuming the nominal resolution to be 12 bit.

As mentioned in the previous sections, the tracking speed depends on the constants μ_m and μ_b. The conflict between convergence time and steady-state error was mitigated by switching the μ values: in order to speed up the initial approach to the correct value, an higher μ is used during the conversion of the first million of samples; during the following conversions μ is switched to a lower value, allowing a better precision in the estimates.

4.1.3 Simulations

The operation of the pipeline stage was first simulated without applying any calibration technique. Assuming the non-calibrated stage to be characterized by the parameters in Tab.4.2 and assuming a full swing input sine wave at 62.25 MHz , a SNDR[2] of 41.86 dB is obtained from the simulation, to be compared the the ideal converter SNR of 73.47 dB. The ADC performance in the absence of calibration is significantly far from the target resolution hence, as expected, calibration is mandatory for proper 12 bit operation.

At first the gain only calibration technique was investigated. Assuming the stage to be affected from gain error only (gain of 3.9028 and

[2]The SNDR includes both THD and SNR; THD was calculated considering the overall power of the harmonics, whereas SNR results from the integration of the noise power in the resulting spectrum. Since no physical noise model was included, SNR takes into account numerical noise and quantization noise only. Signals' spectra were derived by means of FFTs on 1024 samples.

$b = 0.000001$) the convergence of the gain estimate $\hat{m}$ has been proved; the final value is achieved in about 10^6 samples[3]. Fig.4.9(a) shows the transient evolution of $\hat{m}$ whereas Fig.4.9(b) reports the transient evolution of the SNDR during the calibration cycles. In order to estimate the calibration benefits the output spectra were evaluated after a conservative number of samples: after 5000 slots of 1024 samples each, the calibrated SNDR becomes 72.50 dB, to be compared with 73.49 dB for the ideal stage and 50.27 dB for the non-calibrated one. Where not specified, the FFTs and then the THD, SNR and SNDR were calculated on the last 1024 points after $5 \cdot 10^6$ conversion cycles.

Neglecting the third-order non-linearity ($b = 0.000001$) a $\pm LSB/8$ ADSC thresholds shift is tolerated thank to the code redundancy, despite the calibration signal. With nominal ADSC thresholds the effect of capacitor mismatch was also investigated. Assuming the capacitors are described by

$$C_i = C_{nom} + \alpha \Delta C_i \; with \; i = a, b, c, f \tag{4.59}$$

and assuming the example configuration

$$\Delta C_a = 0.246 fF \;\; (0.1\% \; of \; C_{nom}) \tag{4.60}$$
$$\Delta C_b = 0.116 fF \;\; (0.05\% \; of \; C_{nom}) \tag{4.61}$$
$$\Delta C_c = -0.209 fF \;\; (-0.08\% \; of \; C_{nom}) \tag{4.62}$$
$$\Delta C_f = 0.124 fF \;\; (0.05\% \; of \; C_{nom}) \tag{4.63}$$
$$\tag{4.64}$$

the detrimental effects on the overall performances are summarized in Tab.4.3: a mismatch of a few percents is sufficient to nullify the benefit of the gain calibration technique. Assuming the MDAC capacitors to be matched and equal to the nominal value, gain-only calibration is not enough to provide the required resolution. Assuming the gain

[3]Since the first stage only is calibrated, in the adopted notation the subscripts were removed, therefore $\hat{m}$ indicates the estimate of the gain coefficient m and $\hat{b}$ indicates the estimate of the third-order non-linearity coefficient.

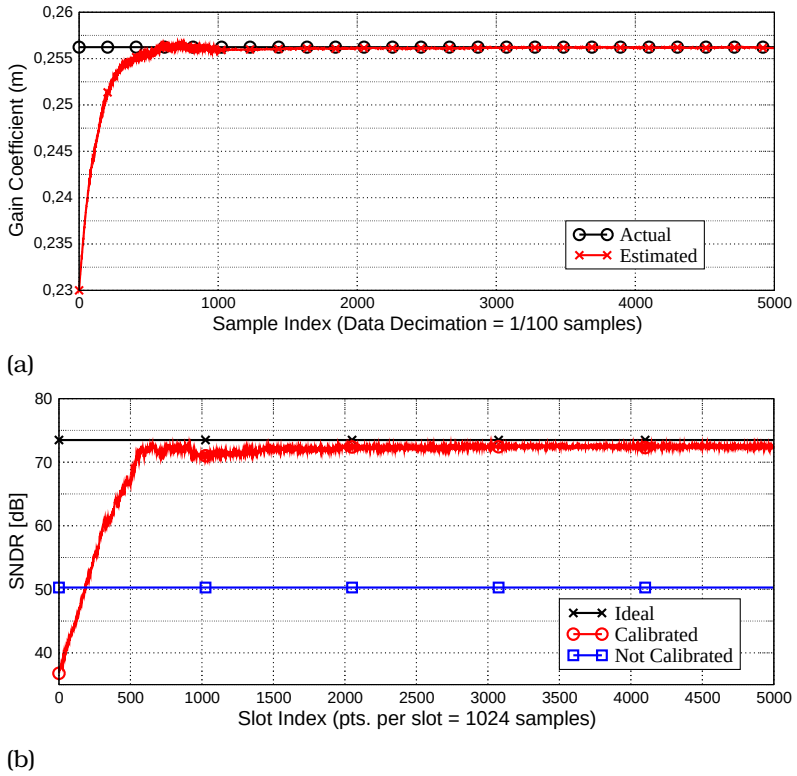


Figure 4.9: Calibration transient behaviour: (a) estimated gain coefficient $\hat{m}$ (b) calibrated SNDR.

value reported in Tab.4.2, simulations for different values of b demonstrate that significant distortion limitations arise even for small values of third-order coefficient; as shown in Fig.4.10 the calibrated SNDR drops to $63\,\text{dB}$ for $b = 0.01$.

The combination of gain error and non-linearity calibration allows to recover to the required resolution. Assuming the stage gain to be once more 3.9028 with a third-order non-linearity coefficient of 0.1, after 5000 slots of 1024 points each the calibrated SNDR becomes $71.42\,\text{dB}$ with respect to $73.49\,\text{dB}$ for the ideal stage and $50.27\,\text{dB}$ for

α	*SNDR/ENOB* (dB/bit)
0	72.50/11.75
1	71.13/11.52
2	69.66/11.28
4	66.39/10.73
6	63.58/10.26

Table 4.3: Gain only calibration: capacitors mismatch effect on the overall SNDR.

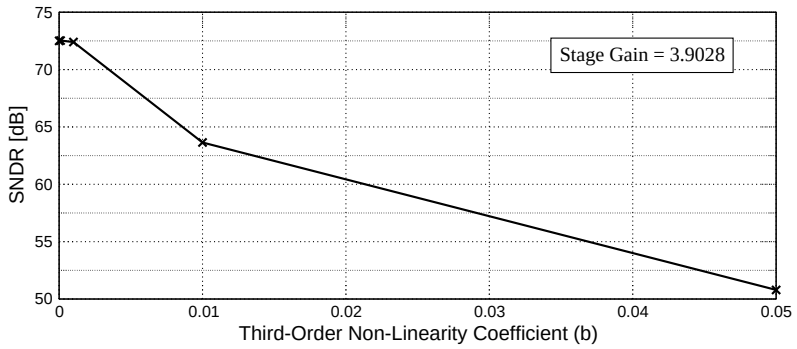
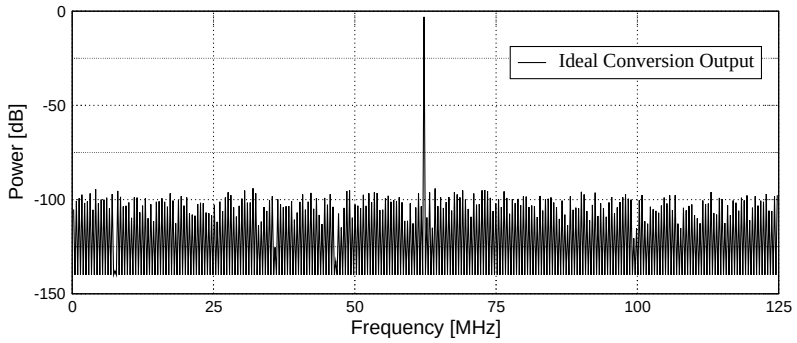
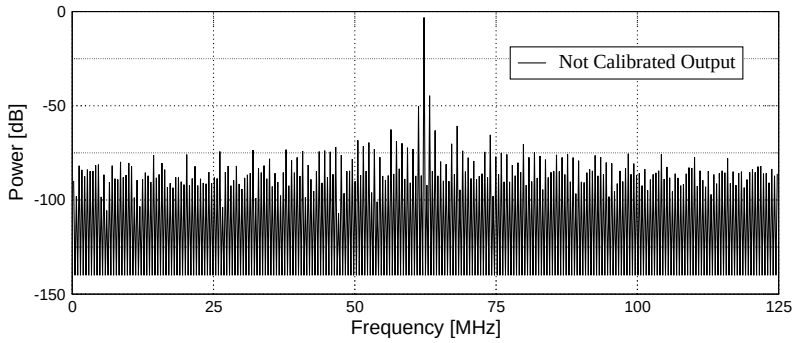


Figure 4.10: SNDR versus third-order non-linearity coefficient with stage gain of 3.9028 (SNDR measured after 5000 1024 points slots.

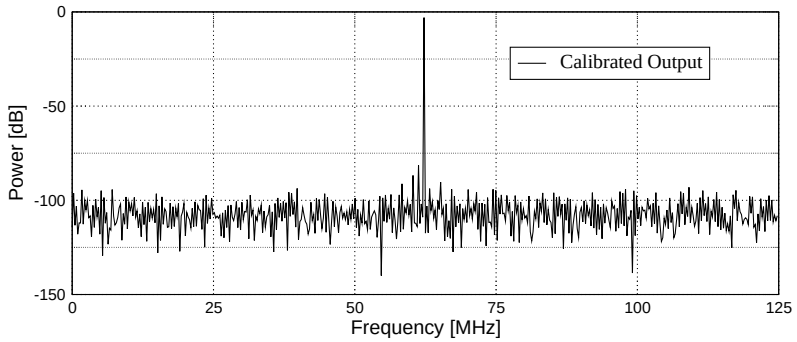
the not calibrated one. Fig.4.11(a), 4.11(b) and 4.11(c) represent the FFT results of the ideal converter output, the non-calibrated converter output and the calibrated one, respectively. Transient convergence of gain coefficient $\hat{m}$ and non-linearity term $\hat{b}$ are shown in Fig.4.12(a) and 4.12(b) respectively whereas Fig.4.12(c) depicts the SNDR increase, proving the validity of the algorithm. In this case the time-constants in the coefficients estimations are switched as illustrated in section 4.1: for the gain coefficient estimation the mobile averaging weight μ_m is fixed to 2^{-14} during the first $2^{21} \approx 2 \cdot 10^6$ conversion cycles and it is switched to 2^{-18} during the remaining time and then during normal operation of the background calibration. Similarly for



(a)

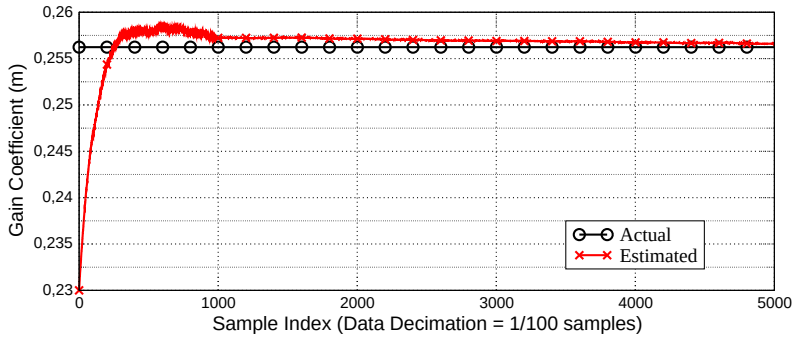


(b)

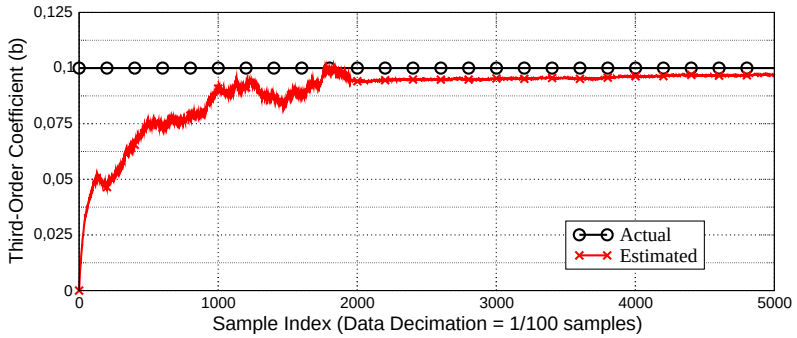


(c)

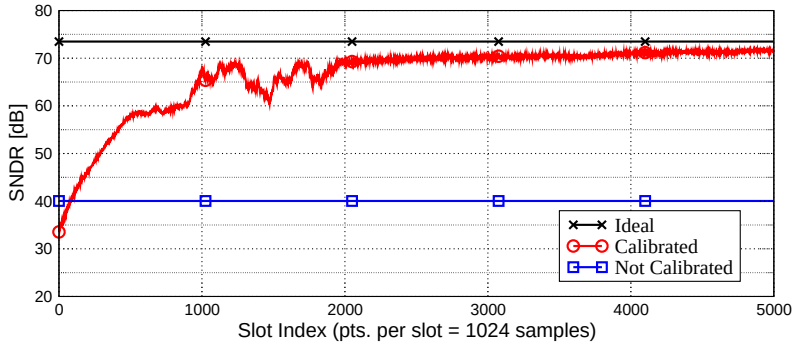
Figure 4.11: FFT results: (a) ideal conversion output; (b) not calibrated output and (c) calibrated output.



(a)



(b)



(c)

Figure 4.12: Calibration transient behaviour: (a) estimated gain coefficient $\hat{m}$; (b) estimated third-order non-linearity coefficient $\hat{b}$ and (c) calibrated SNDR.

the non-linearity estimation μ_b is switched from 2^5 to 2 after the same initial transient. The effect of the time-constant switching is clearly visible in the transient curves in Fig.4.12: the higher value of μ corresponds to the initial portion of the curve, noisy and with higher slope, whereas the lower μ corresponds to the less variable and almost horizontal part.

The code redundancy correction capability has been tested by shifting the ADSC thresholds as mentioned before. With no gain error and without third-order non-linearity, despite the background calibration signal, the code redundancy allows to tolerate a $\pm LSB/8$ shift; in the presence of gain error and third-order distortion a slight reduction in the tolerable thresholds shifts appears.

The effectiveness of the calibration algorithm has been proved for different value of gain and different non-linearity coefficient. Assuming the third-order non-linearity to be negligible ($b = 0.000001$) the SNDR results for a stage gain between 3.8 and 4.2 are shown in Fig.4.13(a); since over-range occurs, the calibration benefits vanish if the stage gain exceeds 4.02. Assuming the stage gain to be 3.9028, the SNDR versus the third-order coefficient b (between 0.000001 and 0.1) is shown in Fig.4.13(b) and in this case no limitation is observed.

In order to evaluate the required operational amplifier specifications the calibrated SNDR has been calculated for different values of DC gain and for different values of UGB. Assuming b to be 0.1, the calibration algorithm works properly, ensuring the required SNDR, for DC gain as low as $30\,$dB; concerning unity gain bandwidth, the SNDR begins to decrease once the UGB drops below $600\,$MHz.

As shown for the gain calibration only, the MDAC capacitors mismatch has detrimental effect on the correction results; assuming the pipeline stage to be as in Tab.4.2 the capacitors mismatch indicated in (4.60) with $\alpha = 6$, leads to a SNDR drop of about $10\,$dB; the SNDR comparison is depicted in Fig.4.14. The overall performances further degrade relaxing the operational amplifier specifications: for example an operation amplifier DC gain of $40\,$dB corresponds to a SNDR lower than $60\,$dB. Montecarlo simulations confirm the capacitors mismatch

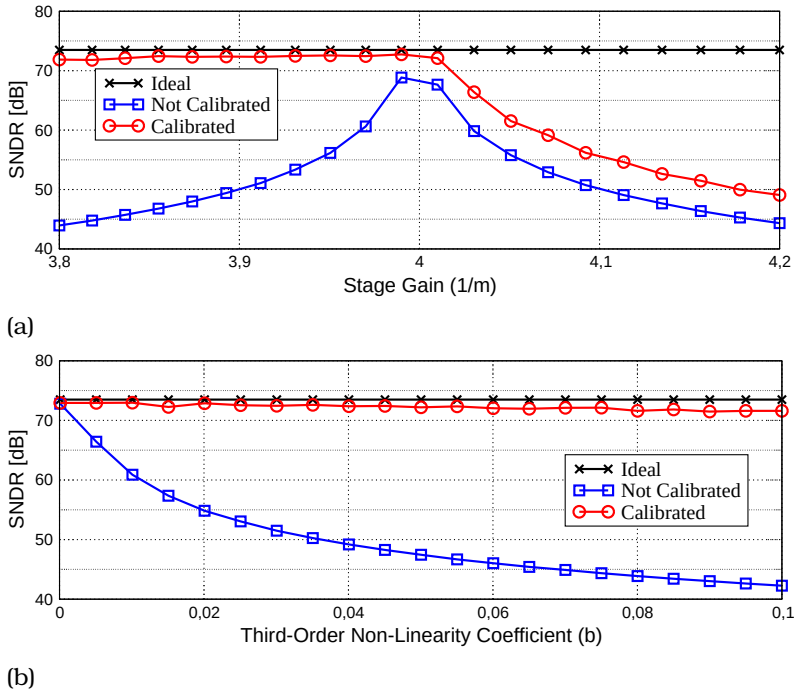


Figure 4.13: Calibration limits: (a) SNDR versus stage gain; (b) SNDR versus b.

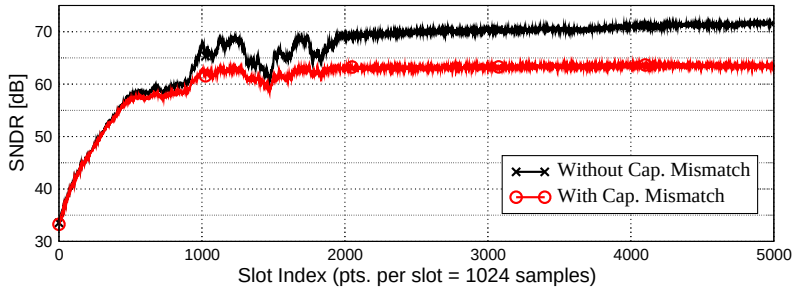


Figure 4.14: MDAC capacitors mismatch effect: SNDR comparison with and without mismatch.

Parameter	*Mean Value*	*Standard Deviation*
Third-Order Coefficient (*b*)	0.0501	0.0167
ADSC Thresholds Offset	0	$0.25LSB/3$
MDAC Capacitors Mismatch	0	$1\% \, of \, C_{nom} = 260\,\text{fF}$

Table 4.4: Statistical extraction parameters for SNDR Montecarlo analysis.

issues: assuming the operational amplifier characteristics to be constants, 100 run with statistical extraction of non-linearity coefficient, ADSC thresholds offset have been performed with and without capacitors mismatch; in Tab.4.4 the parameters extraction statistics are summarized assuming a normal distribution. The histograms resulting with and without capacitors mismatch are shown in Fig.4.15(a) and 4.15(b) respectively.

4.2 Capacitor Mismatch Foreground Calibration

4.2.1 Algorithm Description

The results illustrated in the previous paragraph prove the benefits of gain error and non-linearity calibration, however, serious limitations in terms of MDAC capacitors mismatch were observed. Therefore capacitor mismatch must be taken into account and an additional correction technique is mandatory.

With reference to the MDAC stage model illustrated in Fig.4.6, recalling the equation (4.56), the amplified residue normalized to V_{ref} is

$$V_{out} = (1-\varepsilon_S)\left(\frac{1}{1+\varepsilon_A}\right)\frac{C_{MDAC}}{C_f}\left(V_{in}-\frac{C_{SEL}}{C_{MDAC}}\right) \tag{4.65}$$

where the input-independent term

$$Actual\,Gain = G^{actual} = (1-\varepsilon_S)\left(\frac{1}{1+\varepsilon_A}\right)\frac{C_{MDAC}}{C_f} \tag{4.66}$$

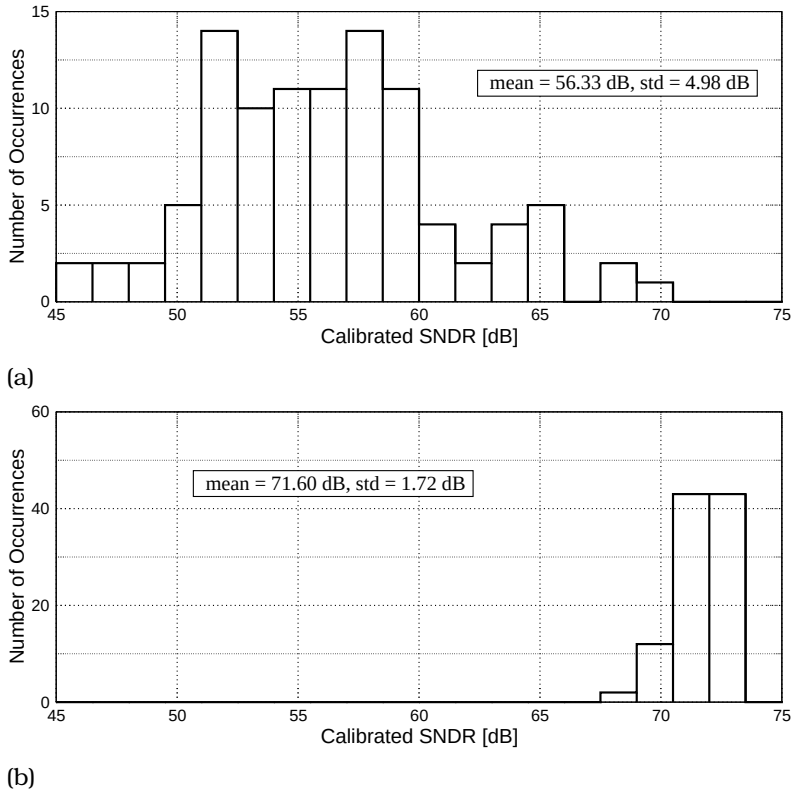


Figure 4.15: MDAC capacitors mismatch effect, Montecarlo analysis results: (a) with mismatch and (b) without mismatch.

represents the actual gain of the stage. Assuming $C = C_{MDAC}/G_i$ to be the average value of the MDAC capacitors; ε_a, ε_b, ε_c and ε_f being the relative weighting error, each capacitive element can be indicated

as follows:

$$C_a = \frac{C_{MDAC}}{G_i}(1+\varepsilon_a) = C(1+\varepsilon_a) \tag{4.67}$$

$$C_b = \frac{C_{MDAC}}{G_i}(1+\varepsilon_b) = C(1+\varepsilon_b) \tag{4.68}$$

$$C_c = \frac{C_{MDAC}}{G_i}(1+\varepsilon_c) = C(1+\varepsilon_c) \tag{4.69}$$

$$C_f = \frac{C_{MDAC}}{G_i}(1+\varepsilon_f) = C(1+\varepsilon_f) \tag{4.70}$$

Adopting this representation it turns out that

$$\varepsilon_a + \varepsilon_b + \varepsilon_c + \varepsilon_f = 0 \tag{4.71}$$

The capacitors mismatch affects both the stage gain and the linearity; using equations (4.67)

$$\begin{aligned} \frac{C_{SEL}}{C_{MDAC}} &= \frac{aC_a + bC_b + cC_c}{C_a + C_b + C_c + C_f} = \\ &= \frac{(a+b+c)}{G_i} + \frac{(a\varepsilon_a + b\varepsilon_b + c\varepsilon_c)}{G_i} \end{aligned} \tag{4.72}$$

The first term represents the ideal input-dependent quantity to be subtracted from the input signal in order to calculate the stage residue; the second one is the undesired additive term involving non-linearity. Theoretically, since the ε coefficients are known, the unwanted addendum can be removed by subtracting an equivalent quantity from the output conversion result; hence, the primary issue is the estimation of capacitors mismatch. A proved technique to determine the actual MDAC capacitors value is presented in [38]; this method, conceived to be used in background mode, can be adopted to perform a foreground estimation at the converter start up. As mentioned before, since the weighting errors are known each output word can be corrected eliminating the quantity highlighted in (4.72).

The pipeline stage representation of Fig.4.1(b) combined to the

residue description in (4.65) is useful to illustrate this approach. The i-th stage ADSC quantization error R_i, normalized to V_{ref}, can be written as

$$R_i = V_{i-1} - \frac{a+b+c}{G_i} \tag{4.73}$$

where a, b and c are defined in Tab.4.1. Neglecting the finite operational amplifier DC gain and bandwidth ($A \approx \infty$ and $f - t \approx \infty$) equation (4.53) becomes

$$\begin{aligned} V_i &= \frac{C_{MDAC}}{C_f} V_{i-1} - \frac{aC_a + bC_b + cC_c}{C_f} = \\ &= \frac{C_{MDAC}}{C_f} \left(R_i + \frac{a+b+c}{G_i} \right) - \frac{aC_a + bC_b + cC_c}{C_f} \end{aligned} \tag{4.74}$$

By substituting the capacitors expression (4.67)

$$V_i = \frac{G_i R_i}{1+\varepsilon_f} - \frac{a\varepsilon_a + b\varepsilon_b + c\varepsilon_c}{1+\varepsilon_f} \tag{4.75}$$

Assuming the mismatch terms to be small

$$\varepsilon_{j,l} << 1 \text{ with } j,\, l = 1,\, 2,\, 3,\, 4 \tag{4.76}$$

$$\frac{1}{1+\varepsilon_j} \approx 1 - \varepsilon_j \tag{4.77}$$

$$\varepsilon_j \varepsilon_l \approx 0 \tag{4.78}$$

and the residue in (4.74) can be linearized as follows:

$$V_i \approx (1-\varepsilon_f) \left[G_i R_i - (a\varepsilon_a + b\varepsilon_b + c\varepsilon_c) \right] \tag{4.79}$$

Since $\delta = V_i - G_i R_i$ represents the error in the residue calculation due to capacitor mismatch, by rotating the MDAC capacitors according a pseudo-random sequence, and correlating the measured residue with the sequence itself, it is possible to quantify the weighting error for each capacitor.

P_1	P_0	C_a	C_b	C_c	C_f
-1	-1	C_1	C_2	C_3	C_4
-1	$+1$	C_2	C_3	C_4	C_1
$+1$	-1	C_3	C_4	C_1	C_2
$+1$	$+1$	C_4	C_1	C_2	C_3

Table 4.5: MDAC capacitors shuffling scheme.

Considering a set of four capacitance $\{C_1, C_2, C_3, C_4\}$ the algorithm rotates this four elements in order to obtain, for each sampling instant, a different configuration of C_a, C_b, C_c and C_f. The assignment is controlled by two zero-mean, pseudo-random binary sequences P_0 and P_1 with values ± 1 according to the table Tab.4.5. According to this table C_a, C_b, C_c and C_f can be written as

$$\begin{aligned} C_a &= \frac{1}{2}\{\frac{C_4+C_3}{2} + P_0\frac{C_4-C_3}{2} + \frac{C_2+C_1}{2} + P_0\frac{C_2-C_1}{2} + \\ &+ P_1\left[\frac{C_4+C_3}{2} + P_0\frac{C_4-C_3}{2} - \frac{C_2+C_1}{2} - P_0\frac{C_2-C_1}{2}\right] \end{aligned} \quad (4.80)$$

therefore

$$\begin{aligned} \varepsilon_a &= \frac{1}{G_i}\{(\varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4) - P_0(\varepsilon_1-\varepsilon_2+\varepsilon_3-\varepsilon_4) + \\ &+ P_1(\varepsilon_1+\varepsilon_2-\varepsilon_3-\varepsilon_4) + P_1P_0(\varepsilon_1-\varepsilon_2-\varepsilon_3+\varepsilon_4)\} \end{aligned} \quad (4.81)$$

By defining

$$\Delta_1 = \varepsilon_1+\varepsilon_2-\varepsilon_3-\varepsilon_4 \quad (4.82)$$

$$\Delta_2+\Delta_3 = \varepsilon_1-\varepsilon_2+\varepsilon_3-\varepsilon_4 \quad (4.83)$$

$$\Delta_2-\Delta_3 = \varepsilon_1-\varepsilon_2-\varepsilon_3+\varepsilon_4 \quad (4.84)$$

it results

$$\varepsilon_a = \frac{1}{G_i}\left[-P_0(\Delta_2+\Delta_3) - P_1\Delta_1 + P_1P_0(\Delta_2-\Delta_3)\right] \quad (4.85)$$

Similarly for the other capacitors

$$\varepsilon_b = \frac{1}{G_i}\left[P_0\left(\Delta_2+\Delta_3\right) - P_1\left(\Delta_2-\Delta_3\right) + P_1P_0\Delta_1\right] \tag{4.86}$$

$$\varepsilon_c = \frac{1}{G_i}\left[-P_0\left(\Delta_2+\Delta_3\right) - P_1\Delta_1 - P_1P_0\left(\Delta_2-\Delta_3\right)+\right] \tag{4.87}$$

$$\varepsilon_f = \frac{1}{G_i}\left[P_0\left(\Delta_2+\Delta_3\right) - P_1\left(\Delta_2-\Delta_3\right) - P_1P_0\Delta_1+\right] \tag{4.88}$$

Substituting (4.85 and (4.86) in (4.79)

$$\begin{aligned} V_i &\approx \left(1+\varepsilon_f\right)\left[G_iR_i - \left(a\varepsilon_a + b\varepsilon_b + c\varepsilon_c\right)\right] = \\ &= G_iR_i - \frac{1}{G_i}\{P_0\left(\Delta_2+\Delta_3\right)\left(-a+b-c+G_iR_i\right) + \\ &+ P_1\left[\left(-a+c\right)\Delta_1 + \left(b-G_iR_i\right)\left(\Delta_2-\Delta_3\right)\right] + \\ &+ P_1P_0\left[\left(a-c\right)\left(\Delta_2-\Delta_3\right) + \left(b-G_iR_i\right)\Delta_1\right]\} \end{aligned} \tag{4.89}$$

Assuming the back-end converter to be ideal (or already calibrated), V_i can be approximated by the quantized version resulting from the BEADC conversion $\hat{V}_i$ therefore the sequence $\hat{V}_iP_0\left(-a+b-c\right)$ is known in real-time. Assuming the zero-mean, pseudo-random sequences P_0 and P_1 to be uncorrelated,

$$E\{P_0\} = E\{P_1\} = 0 \tag{4.90}$$

$$E\{P_0P_1\} = 0 \tag{4.91}$$

$$P_0^2 = P_1^2 = 1 \tag{4.92}$$

By correlating the residue sequence $\hat{V}_i$ with the sequence $P_0\left(-a+b-c\right)$

$$\begin{aligned} T &= E\{\hat{V}_iP_0\left(-a+b-c\right)\} = \\ &= -\frac{\Delta_2+\Delta_3}{G_i}\left[E\{\left(-a+b-c\right)^2\} + E\{G_iR_i\}E\{-a+b-c\}\right] \end{aligned} \tag{4.93}$$

Besides, correlating $\hat{V}_i$ with $P_1(-a+c)$,

$$\begin{aligned} U &= E\{\hat{V}_i P_1(-a+c)\} = \\ &= -\frac{\Delta_1}{G_i} E\{(-a+c)^2\} + \\ &- \frac{\Delta_2 - \Delta_3}{G_i}\left[E\{b(-a+c)\} - E\{G_i R_i\} E\{-a+c\}\right] \end{aligned} \tag{4.94}$$

and finally, correlating $\hat{V}_i$ with $P_1 P_0(a-c)$,

$$\begin{aligned} Z &= E\{\hat{V}_i P_1 P_0(a-c)\} = \\ &= -\frac{\Delta_2 - \Delta_3}{G_i} E\{(a-c)^2\} - \frac{\Delta_1}{G_i}\left[E\{b(a-c)\} - E\{G_i R_i\} E\{a-c\}\right] \end{aligned} \tag{4.95}$$

Unfortunately $G_i R_i$ is not available; however it can be approximated with the actual residue $\hat{V}_i$ and then with the back-end output, hence

$$E\{G_i R_i\} \approx E\{\hat{V}_i\} \tag{4.96}$$

By defining

$$\alpha = E\{(-a+c)^2\} \tag{4.97}$$
$$\beta = E\{b(-a+c)\} = -E\{b(a-c)\} \tag{4.98}$$
$$\gamma = E\{\hat{V}_i\} E\{-a+c\} = -E\{\hat{V}_i\} E\{a-c\} \tag{4.99}$$
$$\rho = E\{(-a+b-c)^2\} \tag{4.100}$$
$$\lambda = E\{\hat{V}_i\} E\{-a+b-c\} \tag{4.101}$$

equations (4.93), (4.94) and (4.95) become

$$T \approx -\frac{\Delta_2 + \Delta_3}{G_i}(\rho + \lambda) \tag{4.102}$$
$$U \approx -\frac{\Delta_1}{G_i}\alpha - \frac{\Delta_2 - \Delta_3}{G_i}(\beta - \gamma) \tag{4.103}$$
$$Z \approx -\frac{\Delta_2 - \Delta_3}{G_i}\alpha + \frac{\Delta_1}{G_i}(\beta - \gamma) \tag{4.104}$$

Since T, U, Z and the terms in (4.97) are real-time computed, an estimation $\widehat{\Delta_2+\Delta_3}$, $\widehat{\Delta_2-\Delta_3}$ and $\widehat{\Delta_1}$ of $\Delta_2+\Delta_3$, $\Delta_2-\Delta_3$ and Δ_1 can be obtained solving the equation (4.102)-(4.104) as follows:

$$\widehat{\Delta_2+\Delta_3} = -\frac{G_i T}{\rho+\lambda} \tag{4.105}$$

$$\widehat{\Delta_2-\Delta_3} = -\frac{\alpha Z+(\beta-\gamma)U}{\alpha^2+(\beta-\gamma)^2} \tag{4.106}$$

$$\widehat{\Delta_1} = -\frac{\alpha U-(\beta-\gamma)Z}{\alpha^2+(\beta-\gamma)^2} \tag{4.107}$$

Once these estimations are known, the mismatch terms ε_1, ε_2, ε_3 and ε_4 are determined.

The approach above can be modified in order to take into account the MDAC operational amplifier finite DC gain A; the linearized residue equation of (4.79) becomes

$$V_i \approx \left(1-\varepsilon_f-\frac{G_i}{A}\right)\left[G_iR_i-(a\varepsilon_a+b\varepsilon_b+c\varepsilon_c)\right] \tag{4.108}$$

Recalling the expression (4.85) and (4.86), (4.108) becomes

$$\begin{aligned} V_i \approx\ & G_iR_i\left(1-\frac{G_i}{A}\right)-\frac{1}{G_i}\{P_0(\Delta_2+\Delta_3)(-a+b-c+G_iR_i)+ \\ +\ & P_1\left[(-a+c)\Delta_1+(b-G_iR_i)(\Delta_2-\Delta_3)\right]+ \\ +\ & P_1P_0\left[(a-c)(\Delta_2-\Delta_3)+(b-G_iR_i)\Delta_1\right]\} \end{aligned} \tag{4.109}$$

that differs from the previous results in the first term only. The finite gain involves a stage gain error and makes the approximation (4.96) worse; in this case

$$E\{\hat{V}_i\} = E\{G_iR_i\}\left(1-\frac{G_i}{A}\right) \tag{4.110}$$

therefore the ADSC output word is not sufficient:

$$E\{G_iR_i\} \approx E\{\hat{V}_i\}\frac{1}{1-\frac{G_i}{A}} \tag{4.111}$$

The actual operational amplifier gain A in unknown and it has to be approximated with the nominal gain A_{nom}. As shown in paragraph 4.2.3, where simulations results are collected, the lower the gain A is, the coarser are the estimates of the capacitors weighting coefficients.

4.2.2 Matlab® Capacitors Mismatch Estimation Model

As done for the gain and non-linearity algorithm the technique described above was evaluated by means a Matlab® model. In Fig.4.16 a block diagram of the capacitors mismatch estimation model is shown. The pipeline stage is represented as in chapter 4.1.2, according to the equation (4.53), except for the addition of the capacitors rotation structure driven by the pseudo-random sequences P_0 and P_1. The back-end output $\hat{V}_i$, the ADSC conversion results a, b and c, the pseudo-random sequences are fed to the estimation block that computes the required expectations in order to provide the capacitors weighting coefficients. The model implemented here allows to verify the convergence of the coefficients, and thus to investigate the algorithm limits, however, it does not allow to directly evaluate the effective benefits of the calibration in terms of converter resolution. For this purpose the resulting mismatch terms must be introduced in the gain and non-linearity Matlab® model to prove the effective cancellation of the undesired input-dependent quantity in (4.72).

4.2.3 Simulations

The key point of the mismatch estimation algorithm is the convergence of the capacitors weighting coefficients ε_1, ε_2, ε_3 and ε_4 to the actuals values. The convergence can be proved by means of transient simulations when the converter is driven with a generic input signal.

Assuming the pipeline stage to be ideal (gain of 4 and $b = 0.00001$) and assuming the nominal MDAC capacitor unit to be $C_{nom} = 260\,\text{fF}$; considering the test set of capacitors in Tab.4.6 the estimated coefficients transient evolution results as in Fig.4.17; after $1{\cdot}10^6$ conversion

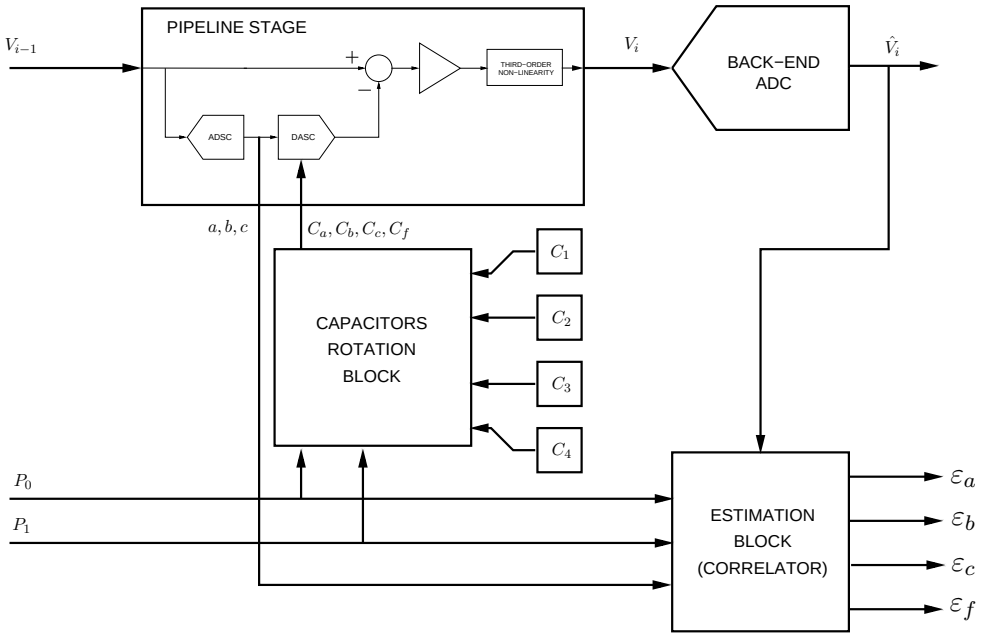


Figure 4.16: Pipeline stage and capacitors weighting coefficients estimation blocks diagram.

cycles the estimations $\widehat{\Delta_1}$, $\widehat{\Delta_2}$ and $\widehat{\Delta_3}$ are stabilized and the resulting relative error[4] , calculated after a conservative number of samples of $5 \cdot 10^6$, are collected in Tab.4.7; in Tab.4.8 Considering the actual MDAC parameters (see Tab.4.2) the convergence time is similar to that observed in the ideal case; the relative errors, reported in Tab.4.9 and Tab.4.10, appear slightly greater.

The above results were obtained using the 10 bit back-end output word as residue approximation according to (4.96). Compara-

[4]Since $\hat{x}$ is the estimated value and x the actual one, the relative error is

$$Error_{relative} \quad = \quad 100\frac{\hat{x} - x}{x}$$

expressed as percentage of the actual value.

Element	*Actual Value* [fF]	*Actual* ε	*Percentage of* C_{nom} [%]
C_1	229.32	-0.0996	-11.8
C_2	242.81	-0.0467	-6.6
C_3	260.34	0.0222	$+0.13$
C_4	286.31	0.1241	-10.1

Table 4.6: MDAC capacitors test.

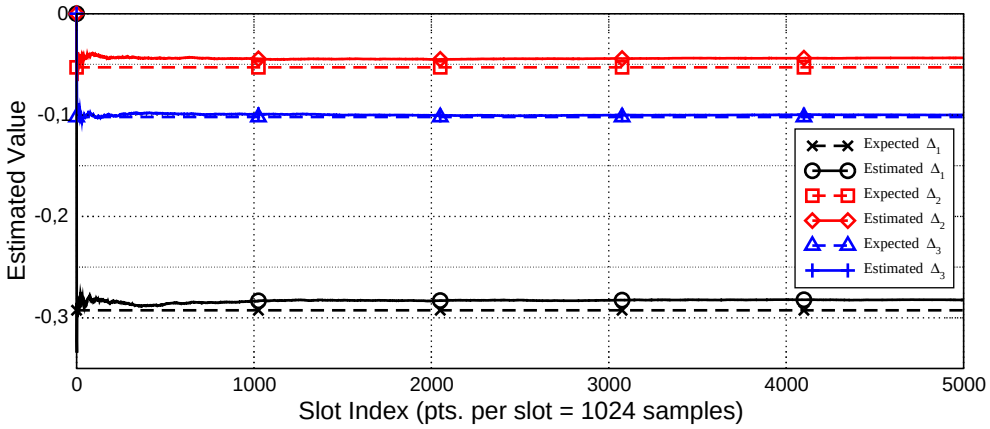


Figure 4.17: Estimated coefficient $\widehat{\Delta_1}$, $\widehat{\Delta_2}$ and $\widehat{\Delta_3}$: transient behaviour.

ble performances in terms of estimated coefficient accuracy, were demonstrated using, instead of the whole back-end result, a 3 bit requantized version added to a zero-mean dither; this solution, at the expense of the convergence time, allows a significant simplification in the calibration hardware.

The effect of the MDAC operational amplifier DC gain has been investigated. Since the calibration algorithm has been modified in order to take into account the stage gain error according to (4.108)-(4.111) the actual gain A is required; approximating A with the nominal operational amplifier DC gain A_{nom} the estimation error changes with

	Actual Value	*Estimated Value*	*Relative Error* [%]
Δ_1	-0.2926	-0.2824	-3.49
Δ_2	-0.0530	-0.0436	-17.7
Δ_3	-0.1020	0.0998	-2.15

Table 4.7: Estimation results (ideal MDAC): $\widehat{\Delta_1}$, $\widehat{\Delta_2}$ and $\widehat{\Delta_3}$ after $5 \cdot 10^6$ samples.

	Actual Value	*Estimated Value*	*Relative Error* [%]
ε_1	-0.0996	-0.0924	-7.26
ε_2	-0.0467	-0.0488	$+4.58$
ε_3	-0.0222	0.0207	-6.57
ε_4	-0.1241	0.1205	-2.94

Table 4.8: Estimation results (ideal MDAC): $\widehat{\varepsilon_1}$, $\widehat{\varepsilon_2}$, $\widehat{\varepsilon_3}$ and $\widehat{\varepsilon_4}$ after $5 \cdot 10^6$ samples.

	Actual Value	*Estimated Value*	*Relative Error* [%]
Δ_1	-0.2926	-0.2710	-7.38
Δ_2	-0.0530	-0.0424	-20.0
Δ_3	-0.1020	0.0962	-5.64

Table 4.9: Estimation results (actual MDAC): $\widehat{\Delta_1}$, $\widehat{\Delta_2}$ and $\widehat{\Delta_3}$ after $5 \cdot 10^6$ samples.

	Actual Value	*Estimated Value*	*Relative Error* [%]
ε_1	-0.0996	-0.0889	-10.7
ε_2	-0.0467	-0.0466	-0.21
ε_3	-0.0222	0.0196	-11.4
ε_4	-0.1241	0.1159	-6.67

Table 4.10: Estimation results (actual MDAC): $\widehat{\varepsilon_1}$, $\widehat{\varepsilon_2}$, $\widehat{\varepsilon_3}$ and $\widehat{\varepsilon_4}$ after $5 \cdot 10^6$ samples.

the difference between nominal and actual gain. The higher the actual gain A, the lower the discrepancy results: typically, if $A > 50\,\text{dB}$, the discrepancy resulting from the approximation $A \approx A_{nom}$ is negligible. For example, setting the nominal gain to $60\,\text{dB}$, the Δ_1 estimation error results $-7.3\,\%$, $-7.4\,\%$ and $-7.8\,\%$ with $54\,\text{dB}$, $60\,\text{dB}$ and $66\,\text{dB}$ of actual gain respectively; setting the nominal gain to $40\,\text{dB}$, the Δ_1 estimation error results $-13.9\,\%$, $-10.5\,\%$ and $-8.8\,\%$ with $34\,\text{dB}$, $40\,\text{dB}$ and $46\,\text{dB}$ of actual gain respectively. In other terms the estimation error increases with the operational amplifier gain decrease, moreover, the estimation error is degraded by the difference between actual and nominal gain; in this case, if the calibration algorithm uses an under estimation of the actual gain ($A_{nom} < A$), the estimation error improves.

4.3 Mismatch Foreground Calibration and Gain/Non-Linearity Background Calibration

4.3.1 Matlab® Calibration Model

It is reasonable to suppose that the capacitors mismatch dependence on the temperature variations is negligible; on the contrary the stage gain and the non-linearities, related to active devices proprieties, can be expected to strongly depend on temperature and they can significantly change during the converter life-time. For this reasons the capacitors mismatch can be considered as time-independent phenomenon and the weighting coefficients can be estimated in foreground mode at the converter start-up and then stored in a lookup table. In order to track any variation affecting the stage gain and the non-linearity, the calibration described in paragraph 4.1 must be performed in background mode; since the tracking speed versus steady-state accuracy trade off exist and it depends on the μ_m and μ_b values, the required overall resolution limits the maximum variation speed that can be tracked. Fig.4.18 depicts a block diagram of the calibra-

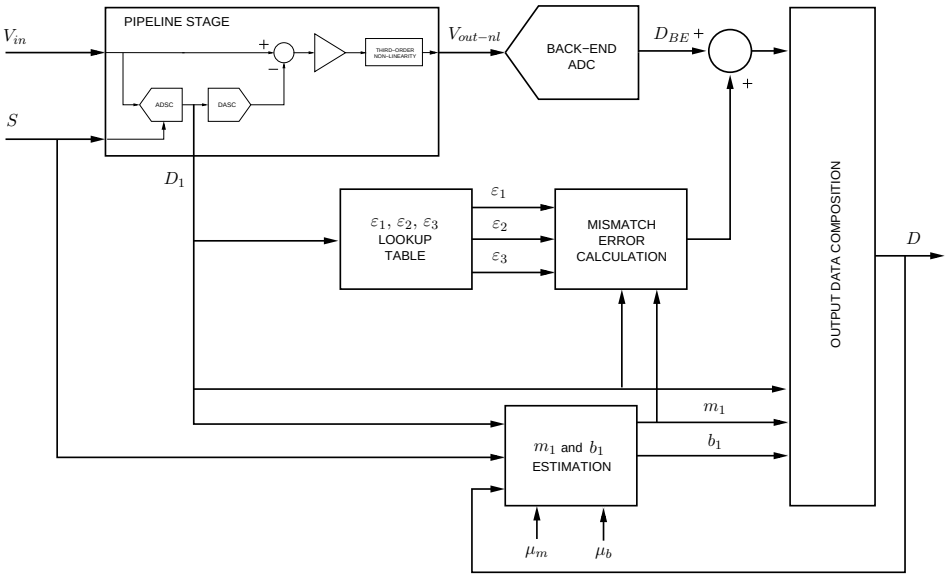


Figure 4.18: Pipeline stage and calibration architecture blocks diagram.

tion architecture exploiting both the capacitors mismatch correction technique and the gain/non-linearity algorithm. As afore mentioned, the mismatch estimation routine is performed at the converter start up; the MDAC capacitors rotation is performed according to the table Tab.4.5 for a fixed foreground calibration time compatible with the required estimation accuracy. When the estimation is completed, the MDAC capacitors are frozen in fixed configuration, i.e. $C_a = C_1$, $C_b = C_2$, $C_c = C_3$ and $C_f = C_4$ and the background calibration algorithm starts. Since the weighting coefficients have been determined, the error terms indicated in (4.72) are known and can be subtracted from the back-end output word while the gain and non-linearity routine is running. Once the gain and third-order coefficients reach the steady-state values the start up phase ends and the output data can be considered as calibrated.

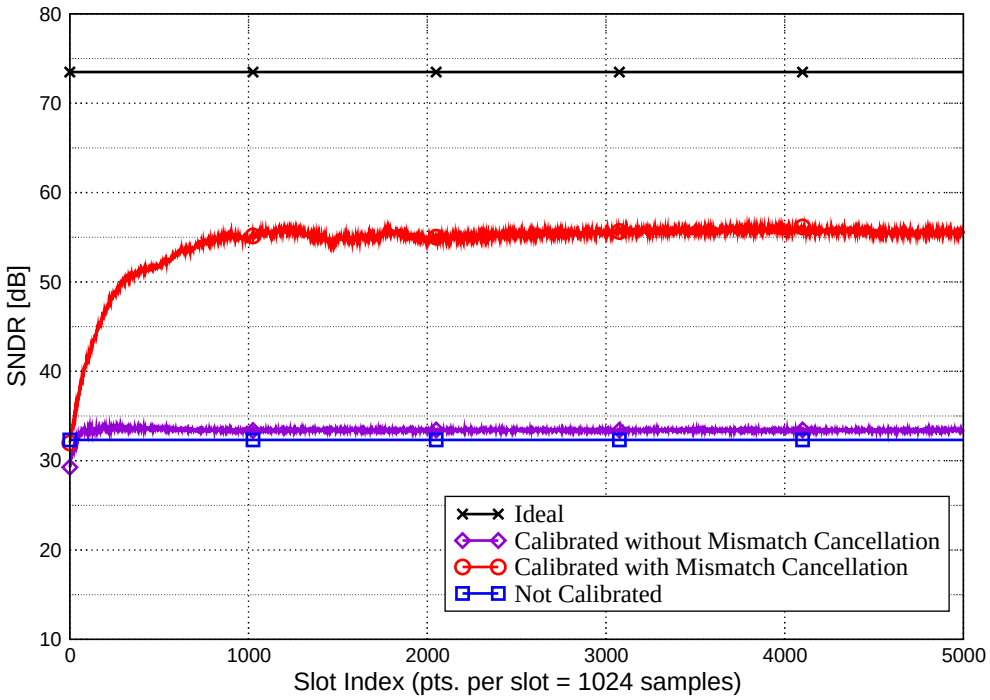


Figure 4.19: Calibration transient behaviour: mismatch cancellation effect.

4.3.2 Simulations

Assuming the MDAC to be ideal (gain of 4 and $b = 0.000001$) and considering the capacitors test set of Tab.4.6, the transient evolution of the calibrated SNDR results as in Fig.4.19; without any mismatch term cancellation, despite the gain and non-linearity calibration, the SNDR does not exceed $35\,\text{dB}$; subtracting from the back-end output word the estimated mismatch error term, the SNDR reaches $56\,\text{dB}$ after 5000 slots of 1024 samples each. Comparable results have been obtained simulating the actual stage (see Tab.4.2). Since the mismatch term cancellation involves a $21\,\text{dB}$ improvement, the benefits result-

ing from the calibration technique are proved. However, it is clearly visible that, in spite of the increase, the SNDR does not satisfy the resolution requirements.

The first limiting factor are the errors affecting the weighting coefficients. Assuming the MDAC to be ideal (gain of 4 and $b = 0.000001$), the lower the estimation error is, the higher the calibrated SNDR results. Starting from the estimated coefficients in Tab.4.8, Fig.4.20 depicts the calibrated SNDR improvement derived from a better coefficients estimation according to Tab.4.11.

The second cause of performance degradation is the non-linearity affecting the residue amplification. Fig.4.21 shows the calibrated SNDR for different third-order coefficient b, assuming perfect mismatch coefficients estimation. Tab.4.12 summarizes the calibrated SNDR evaluated after 5000 slots of 1024 samples each.

4.4 Open Issues

The calibration method to correct stage gain errors and non-linearity allows to achieve SNDR levels suitable for 12 bit operation; the technique efficiency is limited only by the MDAC capacitors mismatch, and therefore an additional calibration routine, eventually executed in foreground mode, is mandatory. The capacitor shuffling method described above allows to recover a part of the resolution loss due to capacitor mismatch, however, several open issues still remain. First, the performance dependence from the actual op-amp gain must be investigated in order to establish the operational amplifier specs; moreover it is important to establish whether or not the discrepancies between the actual operational amplifier gain and the nominal one, specified in the calibration algorithm, lead to a systematic bias in the weighting coefficients estimation. Second, the weighting coefficients estimates must be improved for better accuracy. Other aspects to be investigated are the effects of an input DC offset, the impact of the averaging time and weighting in the coefficients estimation routine and

Curve no.	*Estimation Error*		*Calibrated SNDR* [dB]
	Coefficient	*Error* [%]	
1	ε_1	-10.7	55.71
	ε_2	-0.21	
	ε_3	-11.4	
	ε_4	-6.67	
2	ε_1	-6.42	59.73
	ε_2	-0.13	
	ε_3	-6.84	
	ε_4	-4.00	
3	ε_1	-2.14	66.52
	ε_2	-0.4	
	ε_3	-2.28	
	ε_4	-1.33	
4	ε_1	0	70.56
	ε_2	0	
	ε_3	0	
	ε_4	0	

Table 4.11: Calibrated SNDR for different weighting coefficients estimation errors: SNDR evaluated after 5000 slots of 1024 samples each.

Curve no.	*Third-Order Coefficient* b	*Calibrated SNDR* [dB]
1	0.000001	70.56
2	0.00001	70.62
3	0.0001	70.52
4	0.001	69.99
5	0.01	66.36
6	0.1	50.03

Table 4.12: Calibrated SNDR for different third-order coefficient b and ideal weighting coefficients estimation: SNDR evaluated after 5000 slots of 1024 samples each.

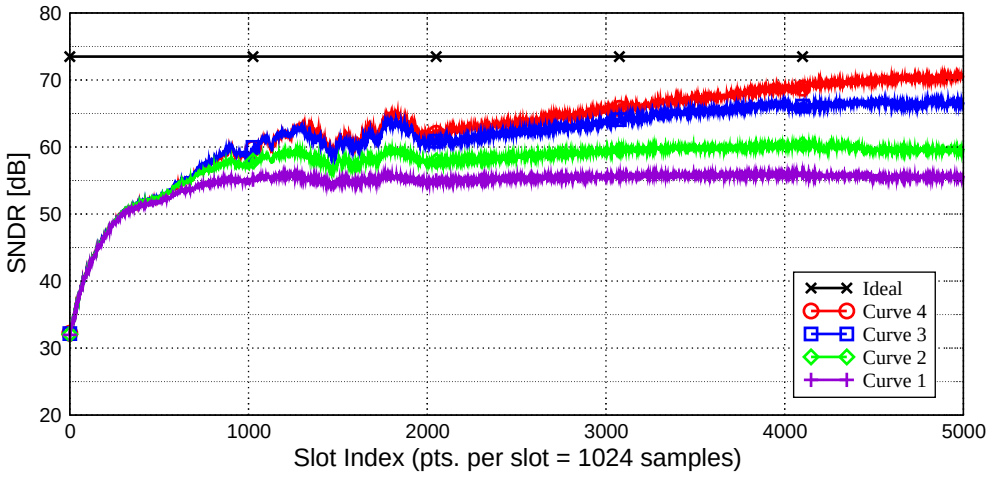


Figure 4.20: Calibrated SNDR with Mismatch Cancellation for different weighting coefficients estimation errors (see Tab4.11).

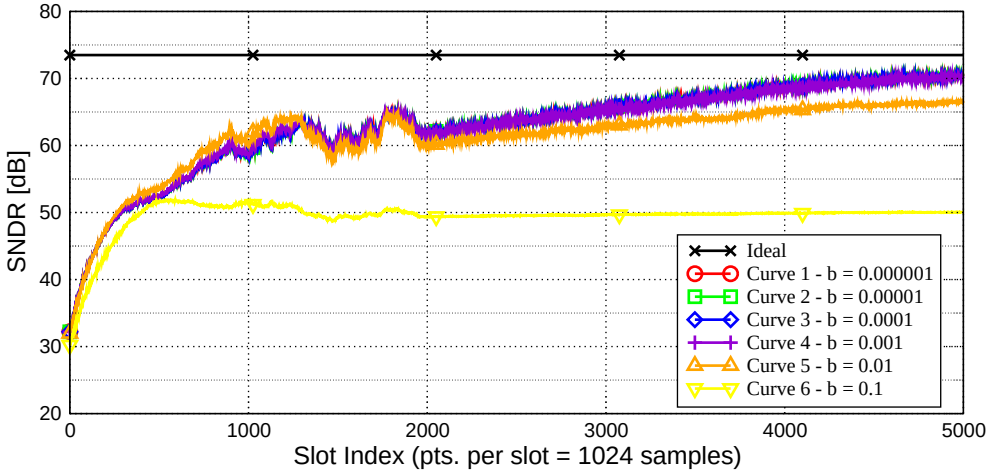


Figure 4.21: Calibrated SNDR with Mismatch Cancellation for different third-order coefficient b (see Tab4.12).

finally the effects of the pseudo-random sequences characteristics.

It was shown that the mismatch error term cancellation is affected by the residue amplifier non-linearity. In fact, since the unwanted additional term in (4.72) is processed through the MDAC operational amplifier, it is affected by the stage non-linearity as well as the input signal. In order to provide a cancellation as accurate as possible, the error term in the lookup table must be non-linearly processed in order to allow effective cancellation.

Further investigations on the possibility to perform in background mode simultaneous calibration of gain, non-linearity and mismatch could be useful to reduce the startup time.

Chapter 5

Conclusions

The purpose of this work was the design of the key blocks of a 1 GS/s Time-Interleaved, Fully Differential analog-to-digital converter suitable for 10GBASE-T Ethernet transceivers. The design has been developed in a 65 nm low-leakage digital CMOS technology.

Starting from the idea of four conversion channels working at 250 MS/s each, a Front-End Track-and-Hold has been designed in order to prevent the effect of inter-channel time-skew. The proposed architecture, illustrated in chapter 2, is composed of a source follower input buffer and a rail-to-rail switch featuring an effective resolution higher than 11 bits at 1 GS/s. Several solutions aiming at high-linearity and high-speed operation have been implemented, such as dynamic bulk biasing to avoid body effect and common mode control to attenuate the effect of Process-Voltage-Temperature variations on the achieved linearity.

The design of the single conversion channel was discussed in chapter 3. The first stage is a Flip-Around Track-and-Hold Amplifier driven by a 25 % Duty Cycle clock; this solution allows to lower the front-end loading capacitance during the acquisition phase; the circuit is based on a folded cascode operational amplifier with gain boosting technique and switched-capacitors CMFB.

A 12 bits pipelined ADC has been designed; 2.5 bits MDAC stages

were used with a 2 bits flash converter as back-end. Each conversion stage embeds a flash A/D converter with 6 decision levels; a high-speed latching comparator has been designed with suitable settling time, kick-back noise and BER ($< 10^{-10}$). The amplified quantization residue is processed by a switched-capacitor, charge sharing MDAC with gain of 4, using the same operational amplifier designed for the Flip-Around circuit. Considering the constraints posed on the maximum power consumption, the performances in terms of slew rate and settling time are not enough for an effective resolution of 12 bits; for these reasons calibration techniques are mandatory for achieving the target resolution.

Two different approaches are reported in chapter 4. The first one is a background algorithm to estimate and correct for gain error and third-order non-linearity in the MDAC; Matlab® simulations prove the effectiveness of this technique. The gain and non-linearity coefficient estimations converge in about 10^6 samples and after $5X10^6$ conversion cycle a converter resolution close to the nomimnal one os is achieved. The SNDR improvement is reduced if capacitors mismatch in the MDAC stages is considered. For this reason the second approach aims at the estimation of the capacitor mismatch at first. The proposed technique is based on the pseudo-random capacitor rotation. With a combininations of both calibration methods, a 25 dB SNDR improvement is acchieved.

It should be noticed that the effectiveness of the mismatch cancellation depends significantly on the accuracy in the estimation of the capacitor mismatch; for this reason the estimation algorithm must be optimized in order to achieve better performance. Furthemore, the reported research activity has proven that the linearity improvement provided by the cancellation of the capacitor mismatch exhibits a significant dependence on the non-linearity affecting the residue amplifier. Finally the convergence time must be further reduced in order to make those calibration algorithms compatible with on-line test at wafer sort.

Chapter 6

Side Activity: DC/DC Converter Modelling, Design and Test

In the last few decades a substantial part of the research effort has been oriented to the development of portable electronic devices like mobile phones, laptop, PDAs etc. The integrated circuits evolution allowed the realization of complex system reducing the required silicon area and the power consumption; exploiting low-power solutions battery-powered operations are feasible however the use of low-voltage architectures calls for suitable circuits implementing voltage regulation and power management. Since the system includes both analogue and digital parts, different voltage domains are required; indeed, while digital circuits benefits from supply voltage scaling, non-volatile memories and analog circuits usually need a higher supply voltage.

In order to extend the battery life the voltage regulation must be as efficient as possible. Moreover, maximizing the efficiency by reducing the energy losses in the power conversion process results in a lower overall heating: at first the use of fan or heat sink leads to addi-

tional power consumption, higher costs, higher size and weight often incompatible with integrated solutions; secondary a thermal causes an increase of series resistance of CMOS switch thus, higher energy loss.

For the reasons above, the power management has taken a key role in the design of quality and reliable products and so many solutions have been studied and developed. The power electronic solutions, designed for high-voltages and high-currents, are suitable for lower voltage domains; since the CMOS process provides good quality switches, high-speed switching techniques are compatible with the integrated circuits.

One of the most important category, specially in battery-powered devices, is the direct-current to direct-current conversion (DC/DC). In this chapter, after a brief introduction focused on the converters control strategies, a design-oriented mathematical model for DC/DC step-down converter, also known as Buck Converter, with Pulse Frequency Modulation (PFM) is presented; the transistor-level simulation results are shown in order to validate the proposed model and next a comparison with the experimental result allows to highlight the most relevant causes of efficiency degradation.

6.1 DC/DC Converters Overview

As shown in Fig. 6.1 a DC/DC switching converter is composed of a pull-up network to provide energy to a LC tank charging the output node and a reverse path, i.e. a diode, to sustain the inductor residual current when the pull-up is turned off. Since the loading current discharge the capacitor C, the main switch S has to be turned on periodically. The most important losses contributions are [40]:

1. *Conduction Losses*: due to the switches on-resistance, forward biased diode drop, inductor and capacitor serie resistance.

2. *Switching Losses*: resulting from charging and discharging of

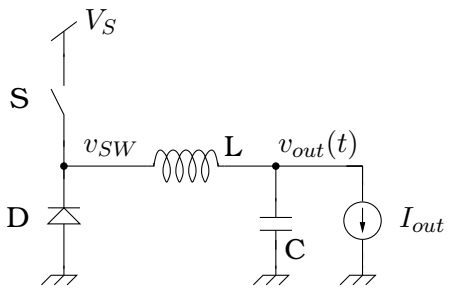


Figure 6.1: Simplified DC/DC Converter

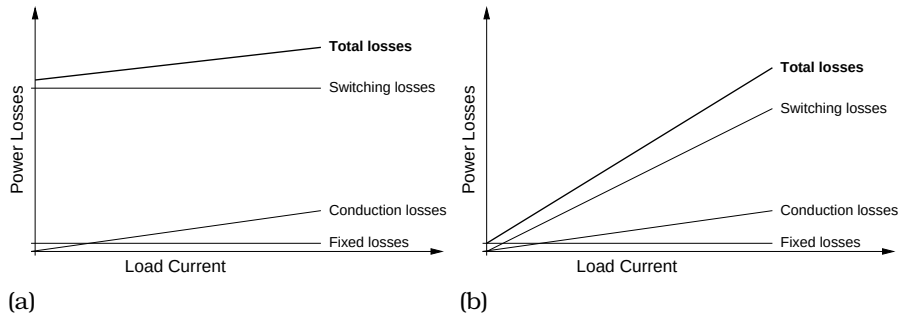


Figure 6.2: Power losses versus the loading current for: (a) Constant-Frequency Control; (b) Variable-Frequency Control

parasitic capacitances of the switches, switches voltage-current overlap, inductor core losses, digital control circuitry switching.

3. *Constant Losses*: bias, stand-by and leakage currents.

Conduction losses increase with the loading current whereas the switching losses are approximately independent from the load and increase with the switching frequency. Fig. 6.2 shows the Power losses trend versus the loading current for a fixed-frequency, 6.2(a), and for variable-frequency control, 6.2(b): in a fixed-frequency control the efficiency at low loading level is limited by the switching losses; in a variable-frequency control both the conduction losses and the switch-

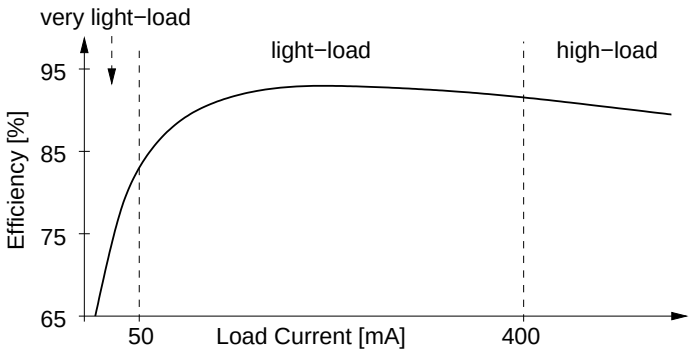


Figure 6.3: Efficiency Curve for a Constant-Frequency Control

ing losses scale down with the loading current resulting in the optimum control strategies for light load condition. On the contrary at high loading currents a variable-frequency control results in higher power losses with respect to the fixed-frequency approach.

The typical efficiency curve for a constant-frequency control is shown in Fig. 6.3; three regions have been individuated: in region A, high loads, the conduction losses are dominant; in region B, medium-to-light loads, the switching losses mostly due to the switches voltage-current overlap, are the main efficiency limiting factor; in region C, light loads, the losses resulting from charging and discharging process of parasitics capacitors are the most important effect.

A typical constant-frequency control strategy is obtained by modulating the width of the charging pulse (Pulse Width Modulation, PWM) whereas the comnmon variable-frequency technique is known as Pulse Frequency Modulation (PFM). Depending on the loading current, the output voltage ripple and the external inductance and capacitor values, two working modes are possible: if the inductor current is permanently higher than zero, the converter works in Continuous Conduction Mode (CCM); if the inductor current decrease to zero and remain zero for a portion of the switching period, the converter works

in Discontinuous Conduction Mode (DCM). For light loading current buck converters usually operate in DCM.

The main issue in the efficiency-oriented design of switching DC/DC converters is the variation of the load current. Indeed a system including several blocks such as transmitters, microprocessors, flash memories, etc. may experience a large variation of the current consumption. A mobile phone, for instance, requires low supply current in stand-by mode and sinks an high current during a call. For this reasons the current-dependent mode-hopping control strategy, combining constant and variable-frequency control depending on the current demand, is the best choice over a wide range of loading condition [41], [42].

In addition to the selection of the suitable control, many efficiency improvements have been developed and presente in literature. One of them is the soft-switching technique [42], [43], which eliminates the voltage-current overlap occuring in the power switch by turning on or off the switch itself when either its voltage drop or its current is zero (Zero Voltage Switching, ZVS and Zero Current Switching ZCS respectively); since capacitors and inductances leads to smoother voltage or current transition, soft-switching is obtained adding resonant or quasi-resonant circuit. A different technique aiming at increasing the efficiency, specially at light load, is known as width-switching [44]: since the optimum switches size depends on the loading current, the efficiency can be improved adjusting the switch width.

Focusing on the variable-frequency control many solutions have been reported in literature: [40] describes a buck converter with current sensing, performing the inductor peak control; [42] presents a similar converter based on the output voltage sensing performing the inductor current ripple control; [45] shows a PFM control with adaptive on-time control. None of these papers presents the design procedure starting from the efficiency constraints; on the contrary [46] proposes a simplified model for PWM converters.

The mathematical model presented in the following sections is a design-oriented description of a PFM Buck Converter working in Dis-

continuous Conduction Mode; the proposed design procedure, starting from the efficiency and output ripple specifications, returns the aspect ration of the power switches and it allows to correct the efficiency estimation considering the power consumption of the drivers.

6.2 DC/DC Converter Mathematical Model

6.2.1 Output Stage Model

In Fig. 6.4 the schematic of the output stage of a DC/DC Buck Converter is shown: the high side of the stage is composted of a PMOS power switch (M_1) providing energy to the LC tank and thus charging the output node; the bottom side must provide a freewheeling path for the residual inductor current when M_1 is turned off. In the asynchronous version, Fig. 6.4(a), the inductor current forces diode D_1 to be turned on; in the synchronous one, Fig. 6.4(b), the NMOS power switch (M_2) must be properly turned on at the PMOS switching off. In the former version the drop across the freewheeling path equals the forward diode voltage drpo whereas in the latter the drop is determined by the NMOS channel on-resistance; since the power transistor is properly sized and driven, synchronous architecture allows to achieve lower losses and then higher efficiency. In order to avoid cross-conduction because of a short-circuit occuring between the power source and ground, a dead-time (delay between the turning off of M_1 and the turning on of bottom switch) must be considered; however, when the dead-time is overestimated the residual inductor current forces the bulk-drain diode to be turned on causing an efficiency degradation.

Assuming the required regulated output voltage to be $\overline{V}_{out}$ and ΔV_{out1} to be the maximum voltage ripple, the average output voltage must equal $\overline{V}_{out}$; since V_{out}^{MIN} and V_{out}^{MAX} represent the lower and the upper output limits imposed by the specs, M_1 must be periodically switched on/off according to the output level. Moreover the output voltage limits can be expressed as function of $\overline{V}_{out}$ and ΔV_{out1} as fol-

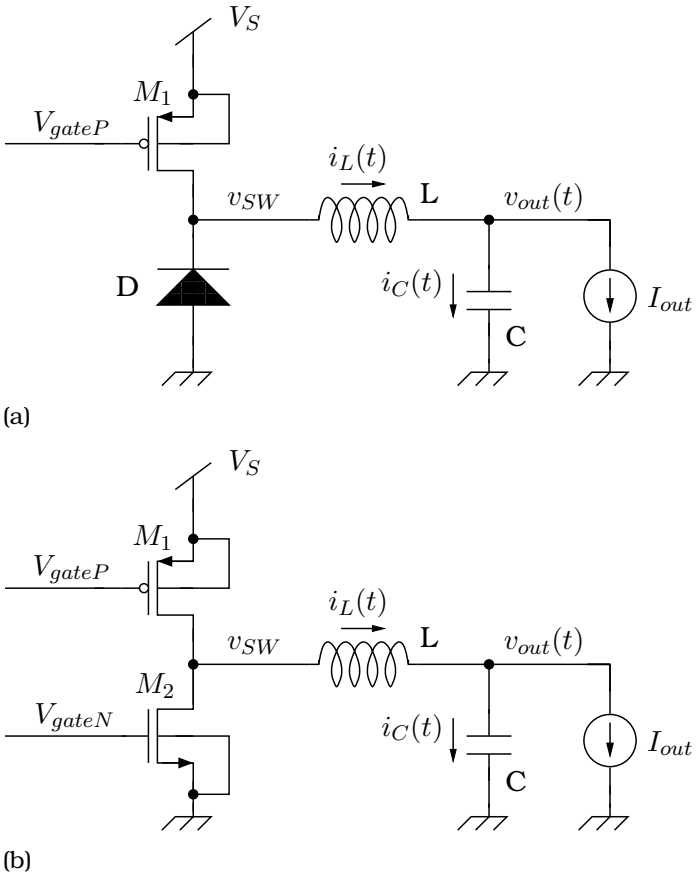


Figure 6.4: DC/DC Buck Converter Output stage schematic: (a) Asynchronous version, (b) Synchronous version

low:

$$V_{out}^{MIN} = \overline{V}_{out} - \frac{\Delta V_{out1}}{2} \tag{6.1}$$

$$V_{out}^{MAX} = \overline{V}_{out} + \frac{\Delta V_{out1}}{2} \tag{6.2}$$

Let us consider at first the asynchronous DCM DC/DC Buck Converter with PFM control, postponing several consideration about the

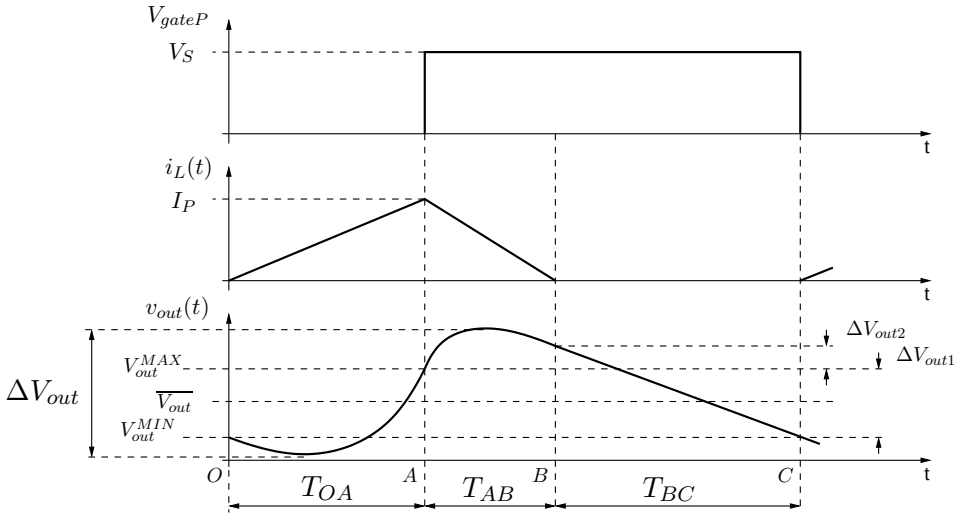


Figure 6.5: Key waveforms of a DC/DC Buck converter.

synchronous version. Since $v_{out}(t)$ is below V_{out}^{MAX}, the PMOS switch is on and charges the output capacitor C while D_1 is off; when $v_{out}(t)$ reaches the maximum value V_{out}^{MAX}, M_1 is turned off; the residual inductor current, discharging the SW node capacitance, forces $v_{SW}(t)$ below the ground level and the diode is switched on. The inductor current, flowing through D_1, gradually decreases to zero, then the diode is turned off leaving the output stage in high impedance condition. The loading current discharges the output capacitance until $v_{out}(t)$ reaches V_{out}^{MIN} and M_1 is turned on again. The key waveforms are shown in Fig. 6.5. Assuming ideal comparators for the sensing of the output voltage and neglecting the time delay affecting the circuit driving M_1, the switching period can be splitted in three parts: T_{OA}, T_{AB} and T_{BC}. During T_{OA}, M_1 is on and D_1 is off; negelcting the variation of the output voltage $v_{out}(t)$ with respect to its average value $\overline{V}_{out}$, the inductor current can be described by the following differential

equation

$$L\frac{di_L(t)}{dt} = V_S' - \overline{V_{out}} \tag{6.3}$$

where V_S' is the battery (i.e.input) voltage V_S minus the voltage drop across the on-state channel resistance of M_1. V_S' is a linear function of the current flowing through the PMOS; however, for the sake of simplicity, in the following calculation a constant value has been considered. The lower the channel on-resistance of M_1, the lower the variation of the voltage drop accross M_1, thus resulting in a more acceptable approximation. Under this assumption $i_L(t)$ increases linearly with time. Setting the time origin at the beginning of the charging phase, under the assumption of Discontinuous Conduction Mode,

$$t_O = 0, i_L(0) = 0 \tag{6.4}$$

and solving the equation (6.3), the inductor current is found:

$$i_L(t) = \frac{V_S' - \overline{V_{out}}}{L}t \tag{6.5}$$

Assuming I_P to be the inductor peak current, $i_L(t)$ can be expressed also as

$$i_L(t) = \frac{I_P}{T_{OA}}t \tag{6.6}$$

Combining the equations (6.5) and (6.6),

$$I_P = \frac{V_S' - \overline{V_{out}}}{L}T_{OA} \tag{6.7}$$

Since the loading current is constant (I_{out}), the charging current flowing through the capacitor C is

$$i_C(t) = i_L(t) - I_{out} \tag{6.8}$$

Inserting the equations (6.6) in (6.8) and integrating from t_O to the generic time instant t, $v_C(t)$ is obtained:

$$\begin{aligned} v_C(t) &= \frac{1}{C}\int_{t_O}^{t} i_C(x)dx = \frac{1}{C}\int_{t_O}^{t} [i_L(x) - I_{out}]\, dx = \\ &= \frac{1}{2C}\frac{I_P}{T_{OA}}t^2 - \frac{I_{out}}{C}t + v_C(t_O) \end{aligned} \tag{6.9}$$

The charging phase starts when the output voltage equals the minimum value V_{out}^{MIN}, and it is over when the output voltage reaches V_{out}^{MAX}; therefore:

$$v_C(t_O) = V_{out}^{MIN} \tag{6.10}$$

$$v_C(t_A) = V_{out}^{MAX} \tag{6.11}$$

and than

$$v_C(t) = \frac{1}{2C}\frac{I_P}{T_{OA}}t^2 - \frac{I_{out}}{C}t + V_{out}^{M}IN \tag{6.12}$$

Calculating $v_C(t_A)$, the expected ripple $\Delta V_{out1} = v_C(t_A) - v_C(t_B)$ (imposed by the specs), results

$$\Delta V_{out1} = v_C(t_A) - v_C(t_O) = \frac{T_{OA}}{C}\left(\frac{I_P}{2} - I_{out}\right) \tag{6.13}$$

Combining the equations (6.7) and (6.13), T_{OA} and I_P are known

$$T_{OA} = \frac{LI_P}{V_S' - \overline{V_{out}}} = L\left[\frac{I_{out} + \sqrt{I_{out}^2 + 2\frac{C}{L}\Delta V_{out1}(V_S' - \overline{V_{out}})}}{(V_S' - \overline{V_{out}})}\right] \tag{6.14}$$

$$I_P = I_{out} + \sqrt{I_{out}^2 + 2\frac{C}{L}\Delta V_{out1}(V_S' - \overline{V_{out}})} \tag{6.15}$$

Neglecting the parasitic capacitance at the SW node, the inductor current instantly discharges the SW node and forces diode D_1 to be turned on; the SW node voltage falls down to $-V_T$ (V_T being the forward biased diode voltage); assuming $v_{SW}(t) = -V_T$ for all the T_{AB} interval,

$$L\frac{di_L(t)}{dt} = -V_T - v_{out}(t) \tag{6.16}$$

Assuming, as before mentioned, $v_{out}(t)$ to be constant and equal to $\overline{V_{out}}$, the inductor current starts to decrease linearly from I_P to zero

$$i_L(t_A) = I_P \tag{6.17}$$

$$i_L(t_B) = 0 \tag{6.18}$$

thus, solving the equation (6.16),

$$-\frac{LI_P}{T_{AB}} = -V_T - \overline{V_{out}} \tag{6.19}$$

As in the previous interval T_{OA},

$$i_L(t) = -\frac{I_P}{T_{AB}}t + \frac{I_P}{T_{AB}}t_B \tag{6.20}$$

Using the equations (6.19) and inserting (6.7)

$$T_{AB} = \frac{LI_P}{V_T + \overline{V_{out}}} = T_{OA}\frac{V_S' - \overline{V_{out}}}{V_T + \overline{V_{out}}} \tag{6.21}$$

Joining the equations (6.8) and (6.20) and integrating on T_{AB} (or rather between t_A and t_B),

$$\begin{aligned} v_C(t) &= -\frac{I_P}{2CT_{AB}}\left(t^2 - t_A^2\right) + \\ &+ \frac{1}{C}\left(\frac{I_P t_B}{T_{AB}} - I_{out}\right)(t - t_A) + v_C(t_A) \end{aligned} \tag{6.22}$$

At t_B, the value of $v_{out}(t)$ has further increased of

$$\Delta V_{out2} = \frac{T_{AB}}{C}\left(\frac{I_P}{2} - I_{out}\right) \tag{6.23}$$

During T_{BC}, both transistors are off and the loading current discharges the output capacitance. Assuming $i_L(t)$ to be constantly zero,

$$i_C(t) = -I_{out} \tag{6.24}$$

hence

$$v_C(t) = -\frac{I_{out}}{C}(t - t_B) + v_C(t_B) \tag{6.25}$$

The output voltage decreases linearly until it reaches again V_{out}^{MIN} and

$$\begin{aligned} v_C(t_B) - v_C(t_C) &= \Delta V_{out1} + \Delta V_{out2} = \\ &= \frac{1}{C} T_{OA} \left(\frac{I_P}{2} - I_{out} \right) \left(\frac{V_S' - \overline{V_{out}}}{V_T + \overline{V_{out}}} \right) \end{aligned} \tag{6.26}$$

using equation (6.25), T_{BC} can be calculated as

$$T_{BC} = C \frac{(\Delta V_{out1} + \Delta V_{out2})}{I_{out}} = T_{OA} \left(\frac{I_P}{2I_{out}} - 1 \right) \left(\frac{V_S' + V_T}{V_T + \overline{V_{out}}} \right) \tag{6.27}$$

The switching period can be evaluated joining equations (6.14), (6.21) and (6.27):

$$T_{OC} = T_{OA} + T_{AB} + T_{BC} = T_{OA} \frac{I_P}{2I_{out}} \left(\frac{V_S' + V_T}{V_T + \overline{V_{out}}} \right) \tag{6.28}$$

Using the linear approximation for $i_L(t)$ during T_{OA} and T_{AB}, the output voltage shows a quadratic trend. It is clearly visible that, even with no delays in the switches driving, the effective output ripple ΔV_{out} is greater than the expected value ΔV_{out1}, imposed by specifications.

The output voltage equals the voltage across output capacitor C. As mentioned above using equations (6.9), (6.22) and (6.25), $v_{out}(t)$ can be expressed as follow. During T_{OA},

$$v_C(t) = \frac{1}{2C} \frac{I_P}{T_{OA}} t^2 - \frac{I_{out}}{C} t + V_{out}^{MIN} \tag{6.29}$$

During T_{AB},

$$v_C(t) = \frac{1}{C} \left(\frac{I_P t_B}{T_{AB}} - I_{out} \right) (t - t_A) + V_{out}^{MAX} \tag{6.30}$$

and during T_{BC},

$$v_C(t) = -\frac{I_{out}}{C}(t - t_B) + v_C(t_A) + \Delta V_{out2} \tag{6.31}$$

In order to evaluate the actual output voltage ripple, the minimum and the maximum value of $v_C(t)$ must be calculated from (6.29) and (6.30) respectively: the minimum occur at

$$t_{MIN} = \frac{I_{out}}{I_P} T_{OA} \tag{6.32}$$

and the minimum voltage is

$$V_{out}^{MIN-ACTUAL} = V_{out}^{MIN} - \frac{I_{out}^2 T_{OA}}{2CI_P} \tag{6.33}$$

The maximum occur at

$$t_{MAX} = t_B - \frac{I_{out}}{I_P} T_{AB} \tag{6.34}$$

and the maximum voltage is

$$V_{out}^{MAX-ACTUAL} = V_{out}^{MAX} + \frac{T_{AB}}{2C} \frac{(I_P - I_{out})^2}{I_P} \tag{6.35}$$

Therefore,

$$\Delta V_{out}^{ACTUAL} = \Delta V_{out1} + \frac{1}{2CI_P} \left[T_{AB} (I_P - I_{out})^2 + T_{OA} Iout^2 \right] \tag{6.36}$$

where

$$\Delta V_{out}^{EXTRA} = \frac{1}{2CI_P} \left[T_{AB} (I_P - I_{out})^2 + T_{OA} Iout^2 \right] \tag{6.37}$$

represents the out-of-specs output voltage ripple (i.e. the extra voltage ripple with respect to ΔV_{out1})

6.2.2 Efficiency Calculation and PMOS Switch Design

In a voltage regulator the Efficiency is defined as

$$\eta = \frac{\overline{P}_{out}}{\overline{P}_{in}} \tag{6.38}$$

where $\overline{P}_{out}$ and $\overline{P}_{in}$ are the average values over the switching period T_{OC} of the power delivered to the load and the power provided by the battery, respectively.

Since switch M_1 is on during the charging phase only, the DC/DC output stage described in the previous section sinks current from the input source during the interval T_{OA} whereas during T_{AB} and T_{BC} the input current is null; during T_{OA} the input current equals the current flowing through the inductor $i_L(t)$. Assuming V_S to be the input voltage, the average input power results

$$\overline{P}_{in} = \frac{1}{T_{OA}} \int_{t_O}^{t_A} V_S i_L(t) dt \tag{6.39}$$

therefore, using equation (6.6),

$$\overline{P}_{in} = V_S I_{out} \frac{\overline{V}_{out} + V_T}{V'_S + V_T} \tag{6.40}$$

The average output power results

$$\overline{P}_{out} = \frac{1}{T_{OC}} \int_{t_O}^{t_C} v_C(t) I_{out} dt \tag{6.41}$$

Since I_{out} is constant,

$$\overline{P}_{out} = \overline{V}_{out} I_{out} \tag{6.42}$$

From equation (6.38)

$$\eta = \frac{\overline{P}_{out}}{\overline{P}_{in}} = \frac{\overline{V}_{out}}{V_S} \left(\frac{V'_S + V_T}{\overline{V}_{out} + V_T} \right) \tag{6.43}$$

Solving the previous equation with respect to V'_S, the maximum voltage drop across the main switch M_1 and compatible with the required efficiency η, is determined:

$$V'_S = \eta V_S \left(1 + \frac{V_T}{\overline{V}_{out}} \right) - V_T \tag{6.44}$$

Approximating the current flowing through M_1 with the average inductor current over T_{OA}, i.e. $I_P/2$, the maximum channel on-resistance of the switch is found

$$R_{ONM_1} = \frac{V_S - V_S'}{I_P/2} \tag{6.45}$$

and considering equation (6.7),

$$R_{ONM1} = \frac{2\left(V_S - V_S'\right)}{I_{out} + \sqrt{I_{out}^2 + 2\frac{C}{L}\Delta V_{out1}\left(V_S' - \overline{V_{out}}\right)}} \tag{6.46}$$

Assuming switch M_1 working in linear region, the channel on-resistance is a linear function of $(V_{gs} - V_{THMOS})^{-1}$ where $(V_{gs} - V_{THMOS})$ represents the overdrive voltage used to turn on the switch M_1 and V_{THMOS} is the PMOS switch threshold voltage. Typically the process specifications includes the measured channel on-resistance for a some voltage overdrive $(V_{gs0} - V_{THMOS})$ and for a some channel length L_0, i.e. the usually minimum channel lenght), hence

$$R_{ON@V_{gs}} = R_{ON@V_{gs0}} \frac{v_{gs0} - V_{THMOS}}{v_{gs} - V_{THMOS}} \tag{6.47}$$

Using L_0 and assuming the on-resistance to be inversely proportional to the channel width, the following relationship for R_{ONM1} is found:

$$R_{ONM1} = \frac{R_{ON@V_{gs}}}{W_{M1}} \tag{6.48}$$

where W_{M1} represents the channel width of M_1. Therefore the design constraints, based on the efficiency specifications, leads to a minimum value for W_{M1}.

$$W_{M1} = \frac{R_{ON@V_{gs}}}{R_{ONM1}} \tag{6.49}$$

The model is still valid if the synchronous version of the DC/DC is considered instead of the asynchronous one. Turning on the NMOS just after the switch-off of M_1, $v_{SW}(t)$ falls below the ground level as in

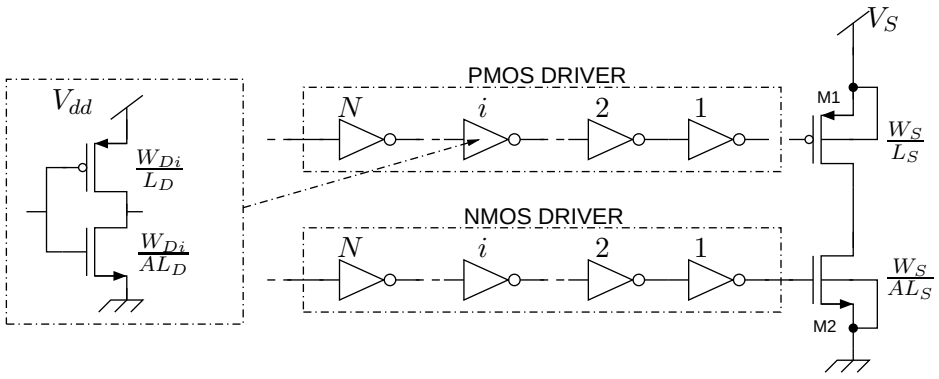


Figure 6.6: Schematic representation of a synchronous DC/DC Buck converter output stage with driver.

the asynchronous case. Nevertheless, the voltage drop across M_2 in this phase is usually smaller than V_T (diode forward threshold); this solution, as indicated in equation (6.43), allows to achieve a higher efficiency. The width of the NMOS switch is set in order to obtain a drop lower than the forward biased diode voltage; a reasonable choice is the PMOS/NMOS ratio typically used in a CMOS architecture, i.e. $W_{M2} = W_{M1}/2$.

6.2.3 Drivers Design

The output stage driving M_1 and M_2 (synchronous implementation) is based on two CMOS inverters chains. The last stages driving the MOS switches has to be sized according to the switch size whereas the preceeding stages have to be designed with a proper scaling factor; the chain length has to be chosen according to the driving capability of the control circuitry.

Fig. 6.6 shows a schematic representation of the system highlighting the adopted symbology. Assuming W_{Di} to be the PMOS width of the i-th stage of the driver chain and A to be the ratio between the

PMOS and NMOS widths of the generic CMOS inverter, the NMOS width results

$$W_{PMOS-DRIVER} = W_{Di} \tag{6.50}$$

$$W_{NMOS-DRIVER} = \frac{W_{Di}}{A} \tag{6.51}$$

The channel length, for both PMOS and NMOS, is set to L_D. The i-th stage loads the $(i+1)$-th inverter with a capacitance C_i,

$$C_i = W_{Di} L_D C_{OXPD} + \frac{W_{Di}}{A} L_D C_{OXND} = \alpha_D W_{Di} \tag{6.52}$$

where C_{OXPD} and C_{OXND} are the specific capacitances of the PMOS and NMOS used in the inverter chain respectively and α_D can be assumed as a technology dependent constant defined as

$$\alpha_D = \left(C_{OXPD} + \frac{C_{OXND}}{A} \right) L_D \tag{6.53}$$

Assuming K to be the scaling factor between the stages of the chain,

$$K = \frac{W_{Di}}{W_{D(i+1)}} \tag{6.54}$$

since the input capacitance of a CMOS inverter is proportional to the width of both MOS transistors, it results that

$$C_{i+1} = \frac{C_i}{K} \tag{6.55}$$

It is important to note that the first stage of the chain drives directly one of the two DC/DC switches; the first CMOS inverter of the PMOS driver is loaded by a capacitance C_{PS} defined as follows

$$C_{PS} = C_{OXPS} W_S L_S \tag{6.56}$$

where C_{OXPS} is the specific capacitance and W_{PS} and L_S are the width and lenght of M_1 (i.e. W_{PS} is equal to $WM1$ calculated in the previous section). Assuming the static dissipation negligible and recalling

the well-known expression of a CMOS inverter dynamic consumption, the single stage power consumption ofthe inverter driving the PMOS switch is found:

$$P_{D1} = V_{dd}^2 f C_{PS} \tag{6.57}$$

and for the $i-th$ generic foregoing stage

$$P_{Di+1} = V_{dd}^2 f C_i \tag{6.58}$$

where V_{dd} is the drivers supply voltage and f the switching frequency. The total power consumption of the PMOS switch driver is therefore

$$P_D^P = P_{D1} + \sum_{i=2}^{N} P_{Di} = P_{D1} + \sum_{i=1}^{N-1} V_{dd}^2 f C_i =$$
$$= P_{D1} + V_{dd}^2 f \alpha_D \sum_{i=1}^{N-1} W_{Di} \tag{6.59}$$

Using the equation (6.54),

$$W_{Di} = K W_{D(i+1)} \tag{6.60}$$

hence

$$W_{Di} = \frac{W_{D1}}{K^{i-1}} \tag{6.61}$$

Inserting in the equation (6.59)

$$P_D^P = P_{D1} + V_{dd}^2 f \alpha_D \sum_{i=1}^{N-1} W_{Di} =$$
$$= P_{D1} + V_{dd}^2 f \alpha_D \sum_{i=0}^{N-2} \frac{W_{D1}}{K^i} \tag{6.62}$$

If B is defined as the ratio between the width of the DC/DC PMOS switch and the width of the first inverter stage PMOS transistor,

$$B = W_{PS}/W_{D1} \tag{6.63}$$

using (6.56) the following relationship can be written

$$P_D^P = V_{dd}^2 f C_{OXPS} W_{PS} L_S + V_{dd}^2 f \alpha_D W_{D1} \sum_{i=0}^{N-2} \frac{1}{K^i} =$$
$$= V_{dd}^2 f \left(C_{OXPS} W_{PS} L_S + \alpha_D W_{D1} \sum_{i=0}^{N-2} \frac{1}{K^i} \right) =$$
$$= V_{dd}^2 f W_{PS} \left[C_{OXPS} L_S + \frac{L_D}{B} \left(C_{OXPD} + \frac{C_{OXND}}{A} \right) \sum_{i=0}^{N-2} \frac{1}{K^i} \right] \tag{6.64}$$

For the DC/DC synchronous version, a scaled inverter chain is mandatory in order to drive the NMOS power switch. Assuming R to be the PMOS/NMOS power switches width ratio (W_{PS} and W_{NS} respectively),

$$R = W_{PS}/W_{NS} \tag{6.65}$$

the NMOS driver power consumption can be calculated:

$$P_D^N = V_{dd}^2 f \frac{W_{PS}}{R} \left[C_{OXNS} L_S + \frac{L_D}{B} \left(C_{OXPD} + \frac{C_{OXND}}{R} \right) \sum_{i=0}^{N-2} \frac{1}{K^i} \right] \tag{6.66}$$

The overall power consumption, considering the worst-case synchronous

version, results

$$
\begin{aligned}
&P_D = P_D^P + P_D^N = \\
&= V_{dd}^2 f W_{PS} \left[C_{OXPS} L_S + \frac{L_D}{B} \left(C_{OXPD} + \frac{C_{OXND}}{R} \right) \sum_{i=0}^{N-2} \frac{1}{K^i} \right] + \\
&+ V_{dd}^2 f \frac{W_{PS}}{R} \left[C_{OXNS} L_S + \frac{L_D}{B} \left(C_{OXPD} + \frac{C_{OXND}}{A} \right) \sum_{i=0}^{N-2} \frac{1}{K^i} \right] = \\
&= V_{dd}^2 f W_{PS} \left[L_S \left(C_{OXPS} + \frac{C_{OXNS}}{R} \right) \right] + \\
&+ \left[\frac{L_D}{B} \frac{R+1}{R} \left(C_{OXPD} + \frac{C_{OXND}}{A} \right) \sum_{i=0}^{N-2} \frac{1}{K^i} \right] = \\
&= K_{DRIVERS} W_P S
\end{aligned}
\tag{6.67}
$$

where

$$
\begin{aligned}
K_{DRIVERS} = L_S &\left(C_{OXPS} + \frac{C_{OXNS}}{R} \right) + \\
&+ \frac{L_D}{B} \frac{R+1}{R} \left(C_{OXPD} + \frac{C_{OXND}}{A} \right) \sum_{i=0}^{N-2} \frac{1}{K^i}
\end{aligned}
\tag{6.68}
$$

Depending on the specifications and the technology process options several solutions are possible: if high input voltage are required, the use of thick oxide transistors for the output stage implementation is mandatory; in order to reduce the driver power consumption, low-voltage CMOS inverter (thin oxide MOSFETs) can be used; this approach requires voltage regulation in order to generate the V_{dd} itself and the efficiency in this voltage regulations introduces additional constrains. Drivers based on thick oxide transistors allow to supply the inverters chain using the DC/DC input voltage; this solution allows to maximize the switches overdrive leading to a lower channel on-resistance. Assuming the drivers supply voltage V_{dd} to be equal to

the DC/DC input V_S, the drivers power consumption in (6.68) must be added to the average input power in order to calculate a more accurate efficiency estimation. Recalling the equation (6.40)

$$\overline{P}_{in} = V_S I_{out} \frac{\overline{V}_{out} + V_T}{V'_S + V_T} + P_D \tag{6.69}$$

Introducing (6.46) and (6.68)

$$\overline{P}_{in} = V_S I_{out} \frac{\overline{V}_{out} + V_T}{V_S - \frac{R_{ON@V_{gs}}}{W_{PS}} \frac{I_P}{2} + V_T} + K_{DRIVERS} W_{PS} \tag{6.70}$$

Since

$$\eta = \frac{\overline{P}_{in}}{\overline{P}_{out}} \tag{6.71}$$

and

$$\overline{P}_{out} = \overline{V}_{out} I_{out} \tag{6.72}$$

it results

$$V_S I_{out} \frac{\overline{V}_{out} + V_T}{V_S - \frac{R_{ON@V_{gs}}}{W_P S} \frac{I_P}{2} + V_T} + K_{DRIVERS} W_P S = \frac{\overline{V}_{out} I_{out}}{\eta} \tag{6.73}$$

Solving with respect to W_{PS}, the PMOS switch size is determined.

6.3 Model Validation: Transistor-level Simulations

6.3.1 DC/DC Control Strategy

In order to validate the proposed description of the DC/DC converter by means of transistor-level simulations, a behavioural model of the control circuitry has been implemented. The Control Unit performing the Pulse Frequency Modulation (PFM) consist of an ideal Finite State Machine where comparators and logic gates are realized by means

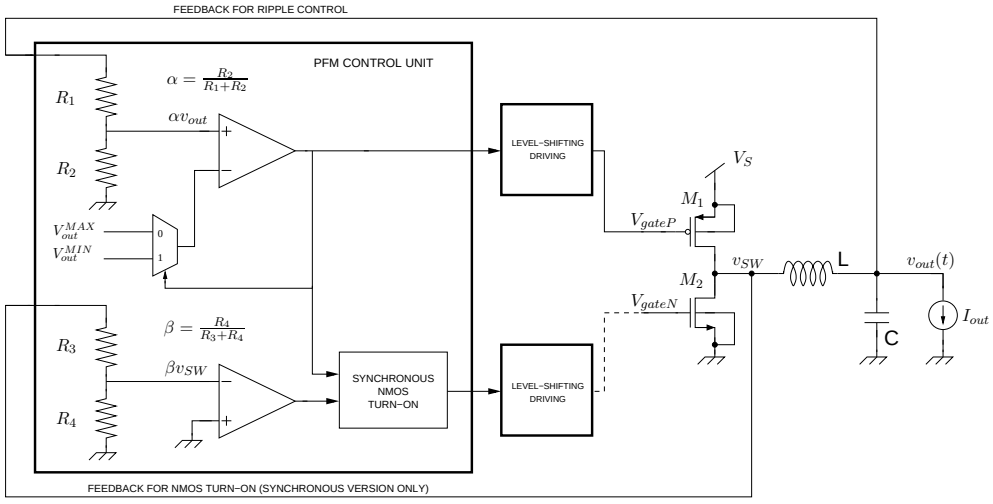


Figure 6.7: Block diagram of the PFM control unit.

of an Hardware Description Language as Verilog-A®. In Fig.6.7 the control unit block diagram is shown. The key point of the proposed PFM control is the driving of the output charging network (PMOS switch) according to the output voltage level; it must be noted that in the asynchronous converter this is the only function demanded to the control unit whereas in the synchronous version the control unit must control, in addition, the NMOS switch, replacing the freewheeling diode. The output voltage control is performed using a sensing network, a voltage comparator and a reference generator. According to the specified output ripple (neglecting the extra-ripple highlighted in the mathematical model) the PMOS switch must be turned off when the output voltage reaches V_{out}^{MAX} whereas it must be turned on when the output voltage, during the discharging phase, equals V_{out}^{MIN}; as shown in Fig. 6.3.1, the in/out comparison characteristic must provide an hysteretic window as wide as the maximum voltage ripple with central point in $\overline{V}_{out}$ (the required average output voltage). The

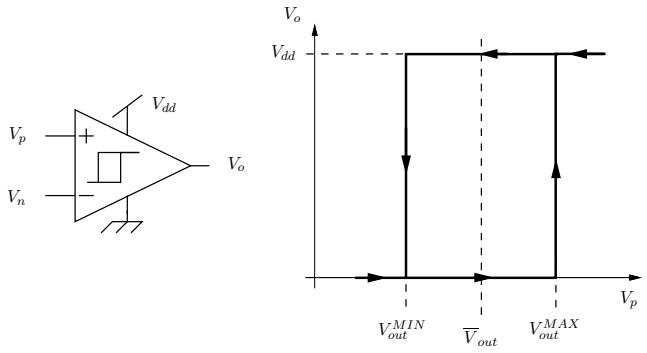


Figure 6.8: DC/DC output voltage sensing: voltage comparator hysteretic window

hysteresis above can be implemented in the voltage comparator or obtained, as in this design case, by dynamically changing the reference voltage which the output voltage is compared to. In order to adapt the DC/DC output voltage to the control unit voltage domain, a resistive voltage divider with scaling factor α has been introduced; according to the scaling ratio both the voltage references, i.e. the switching thresholds, must be scaled down.

The voltage comparator output indicates the DC/DC output level compared to the reference voltages and at the same time reveals if the converter is in the charging or in the discharging phase. This information is used to drive the PMOS by the inverter chain and for selecting the suitable threshold voltage for the comparator.

In the synchronous version the NMOS switch must be turned on at the end of the charging phase; in order to avoid the bulk-drain diode activation, the switch-on of the NMOS device is determined by the signal controlling the switch-off of the PMOS device, M_1; actually a dead-time must be introdiced in order to prevent an input to ground shorting. In order to operate in Discontinuous Conduction Mode, the NMOS switching off must occur when the inductor current is approximately zero or, similarly, when the switching node voltage

v_{SW} reaches zero hence, an additional comparator is needed to perform the SW-node sensing; since the SW-node can reach the input voltage a voltage divider is mandatory for the second comparator too with scaling ratio β.

6.3.2 Simulations Results

A DC/DC Buck converter has been designed using a 0.35μm CMOS process, following the criteria described above. Assuming the external components L and C to be design constraints, i.e. $L = 100\mu$H and $C = 2.2\mu$F. Since the input voltage V_S equals 6V the DC/DC and the driving stages are both based on high voltage MOS transistors; a low-voltage (thin oxide MOSFETs) control unit has been implemented with a supply voltage of 3.3V. The converter is designed to provide an average output voltage of 3.4V; in order to make the output voltage suitable to the control unit voltage domain the sensing network must perform a division by 2 by means of a voltage divider ($\alpha = 2$). In Tab. 6.1 the technology parameters being useful for the gate capacitances calculations are reported (worst-case values).

Parameter	*Unit*	*Value*	*Description*
t_{OXPHV}	nm	37	*High-voltage PMOS oxide thickness*
t_{OXNHV}	nm	36	*High-voltage PMOS oxide thickness*
ϵ_0	pF/m	8.85	*Vacuum dielectric constant*
ϵ_{OX}	$-$	3.9	*Oxide dielectric constant*
C_{OXPHV}	$F/\mu m^2$	$9.328X10^{-16}$	*Specific High-voltage PMOS gate capacitance*
C_{OXNHV}	$F/\mu m^2$	$9.588X10^{-16}$	*Specific High-voltage NMOS gate capacitance*

Table 6.1: Technology parameters

Asynchronous Version

Considering the asynchronous version of the DC/DC where the freewheeling diode is realized by means of the drain-bulk junction (body-diode) of an NMOS with the gate terminal connected to ground. Assuming the PMOS width W_S to be 15 mm and consequently the NMOS width W_S/A to be 7.5 mm; the ratio between the DC/DC PMOS width W_S and the first driver stage PMOS width W_D, defined in the previous section as B, is fixed to 23; the scaling factor in the driver chain K is set to 3 considering 4 inverter stages and the PMOS-NMOS width ratio R is 2; the on-state diode voltage drop V_T, estimated with preliminary simulations, is 1.15 V.

Simulating with a loading current of 5 mA and an input voltage of 6 V, the characteristic waveforms are shown in Fig.6.9, according to the model predicted behaviour. The model versus simulated results comparison are reported in Tab.6.2: the overall efficiency error is lower than 0.2 %; if the inductor peak current is about 38 mA, the mathematical model error results 175μ A, equal to 3 %; in terms of output voltage ripple the estimated value is 16.22 mV with respect to 15.73 mV derived by simulation; the estimated switching frequency of 109 KHz differs from the simulated one no more than 2.7 %. The maximum error occurs in the estimation of the power consumption of the driver; in this case the model under estimates this power consumption of about 15 %; the simulated driver consumption is 211μ W.

All the parameters have been evaluated and compared to the simulations results for different output stage size; keeping the size ratio and the driver scaling factors above, the PMOS switch has been swept from 10 mm to 40 mm for a loading current of 5 mA. The overall efficiency, the inductor peak current and the output voltage ripple comparison curves are reported in Fig.6.10(a), 6.10(b) and 6.10(c). The overall efficiency error is lower than 0.8 % whereas the I_P and the ΔV_{out}^{ACTUAL} error are both lower than 3.8 % over the whole width range. Similarly the model versus simulations results comparison has been performed for a fixed switches width varying the loading current from

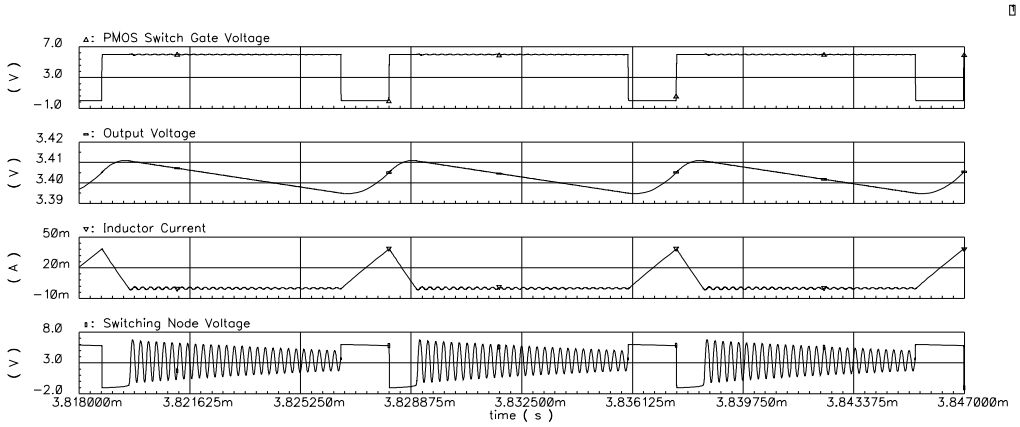
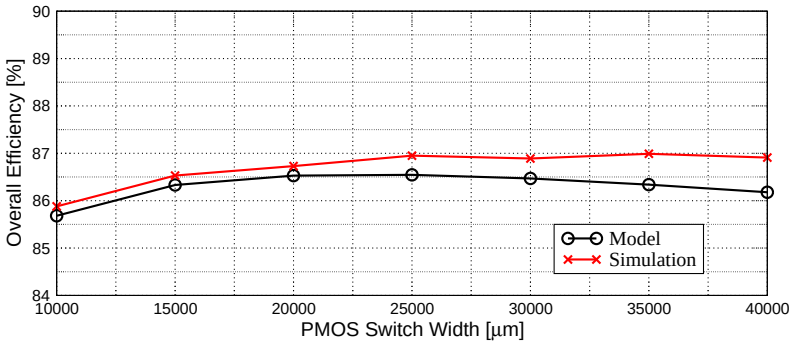
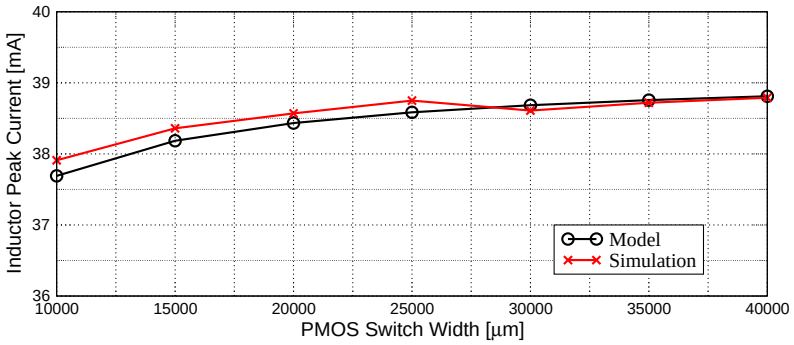


Figure 6.9: Asynchronous DC/DC waveforms: $V_S = 6\,\text{V}$, $I_{out} = 5\,\text{mA}$ and $W_{SP} = 15\,\text{mm}$.

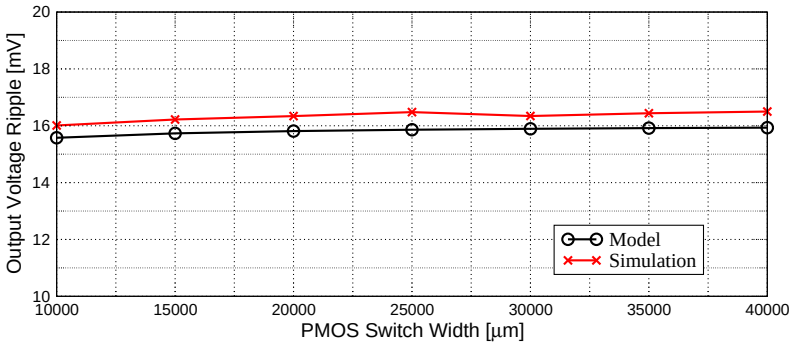
$5\,\text{mA}$ to $40\,\text{mA}$. Assuming the PMOS switch width to be $15\,\text{mm}$ (NMOS switch width equal to $7.5\,\text{mm}$) the comparison curves are shown in Fig.6.11(a), 6.11(b) and 6.11(c). In this case the maximum efficiency error is $0.3\,\%$ whereas the inductor peak current and the ripple output voltage errors do not exceed $6.7\,\%$.



(a)

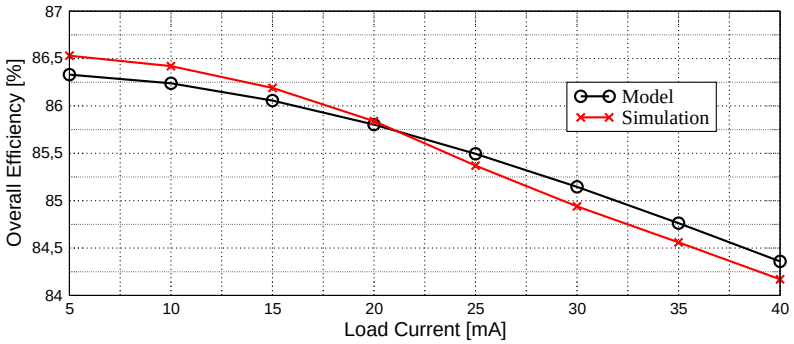


(b)

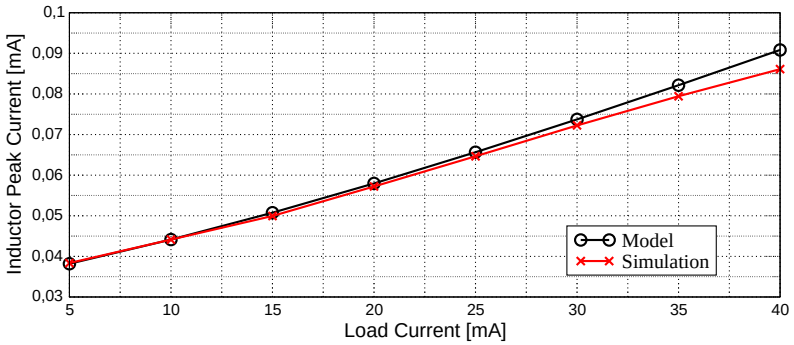


(c)

Figure 6.10: Simulated versus model expected value comparison for different DC/DC PMOS widths, with $I_{out} = 5\,\text{mA}$ (Asynchronous Version): (a) Overall efficiency, (b) Inductor peak current and (c) Output voltage ripple.



(a)



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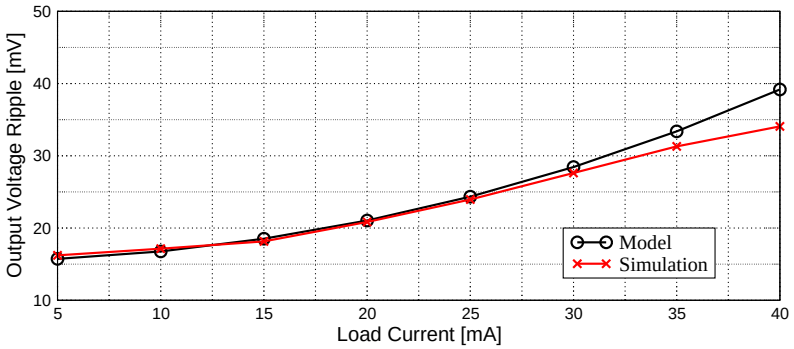


(c)

Figure 6.11: Simulated versus model expected value comparison for different loading current with DC/DC PMOS width $W_S = 15\,\text{mm}$ (Asynchronous Version): (a) Overall efficiency, (b) Inductor peak current and (c) Output voltage ripple.

	Model	*Simulation*
Overall Efficiency (η) [%]	86.33	86.53
Driver Power (P_D) [μW]	180	211
Inductor Peak Current (I_P) [mA]	38.2	38.4
Output Voltage Ripple (ΔV_{out}^{ACTUAL}) [mV]	15.73	16.22
Switching Frequency (f_{SW}) [KHz]	109.1	106.3

Table 6.2: Asynchronous DC/DC model versus simulated results comparison: $V_S = 6$ V, $I_{out} = 5$ mA and $W_S = 15$ mm.

Synchronous Version

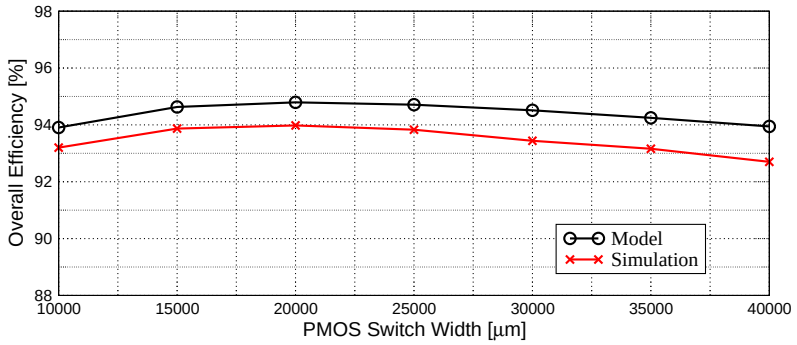
Using the same criteria, the synchronous version has been analyzed. Assuming the same MOSFET size ($W_S = 15$ mm and $W_S/A = 7.5$ mm), the ratio between the DC/DC MOSFET width and the first driver stage width is set to 23 for the PMOS driver chain and it is set to 19 for the NMOS one; the scaling factor in the driver chain K is assumed to be 3 considering 4 inverter stages and the PMOS-NMOS width ratio R is 2; the NMOS on-channel voltage drop V_T, estimated with preliminary simulations, is $125mV$. Since V_{SW} reaches the input voltage V_S ($6V$), the SW-node sensing path must provide a voltage division by 3.

Simulating with a loading current of 5 mA and an input voltage of 6 V, the model versus simulated results comparison are reported in Tab.6.3: the overall efficiency error is lower than 1.25 %; if the inductor peak current is about 38 mA, the mathematical model error results 32μA, lower than 1.2 %; in terms of output voltage ripple the estimated value is 17.33 mV with respect to 17.53 mV derived by simulation; the estimated switching frequency of 99.1 KHz differs from the simulated one no more than 0.8 %. Also in this case the maximum error occurs in the estimation of the driver power consumption: an under-estimation of 15 % is found; the simulated power consumption is 293μW. The overall efficiency, the inductor peak current and the output voltage ripple versus the output stage size (PMOS switch width swept from 10 mm to 40 mm) for a loading current of 5 mA are shown in

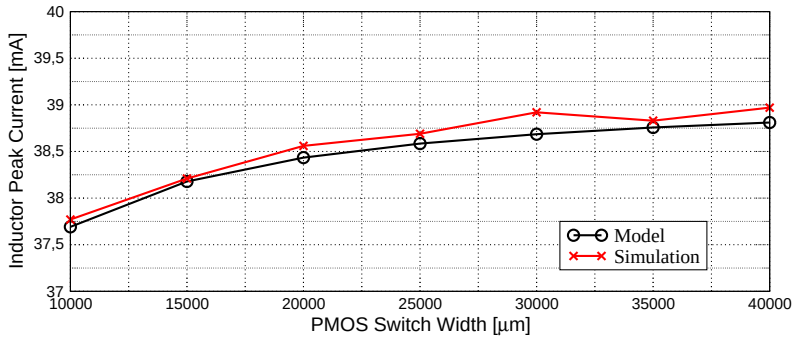
	Model	*Simulation*
Overall Efficiency (η) [%]	95.96	95.41
Driver Power (P_D) [μW]	249	293
Inductor Peak Current (I_P) [mA]	38.18	38.21
Output Voltage Ripple (ΔV_{out}^{ACTUAL}) [mV]	17.33	17.53
Switching Frequency (f_{SW}) [KHz]	99.1	98.3

Table 6.3: Synchronous DC/DC model versus simulated results comparison: $V_S = 6\,\text{V}$, $I_{out} = 5\,\text{mA}$ and $W_S = 15\,\text{mm}$.

Fig.6.12(a), 6.12(b) and 6.12(c). In this case the overall efficiency error is lower than $1.3\,\%$ whereas the I_P and the ΔV_{out}^{ACTUAL} error are both lower than $2.7\,\%$ over the whole width range.
Fixing the output stage size and varying the loading current from $5\,\text{mA}$ to $40\,\text{mA}$ the performances comparison curves result as in Fig.6.13(a), 6.13(b) and 6.13(c). In this case the maximum efficiency error is $1.4\,\%$ whereas the inductor peak current and the ripple output voltage errors do not exceed $11.2\,\%$. The Mathematical Model errors resulting from the synchronous version simulations are quite higher with respect to the asynchronous ones; it is fair to assert that this inaccuracy arise from the dead-time in the NMOS switch synchronous turn-on not included in the model description.



(a)



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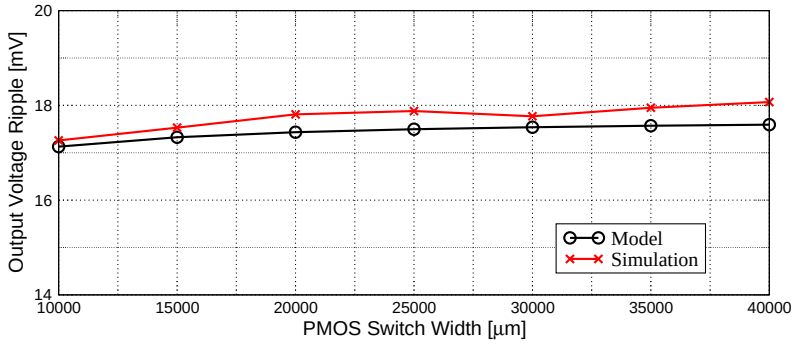
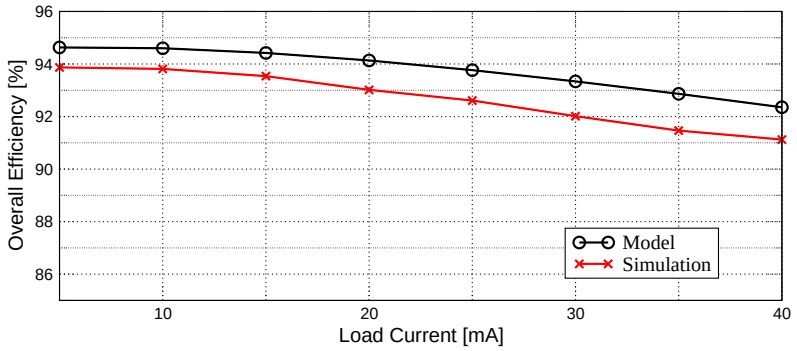
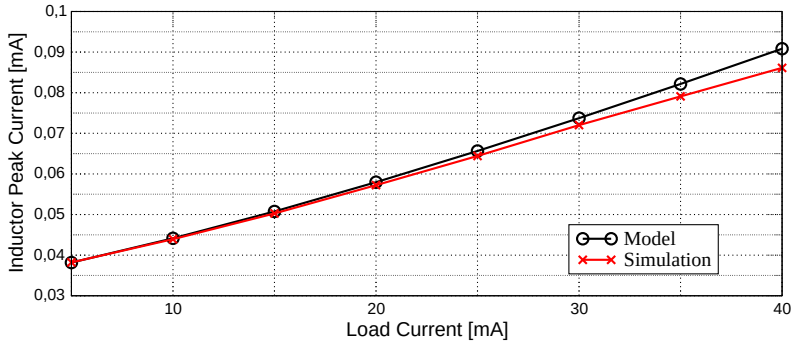


(c)

Figure 6.12: Simulated versus model expected value comparison for different DC/DC PMOS widths, with $I_{out} = 5\,\text{mA}$ (Synchronous Version): (a) Overall efficiency, (b) Inductor peak current and (c) Output voltage ripple.



(a)



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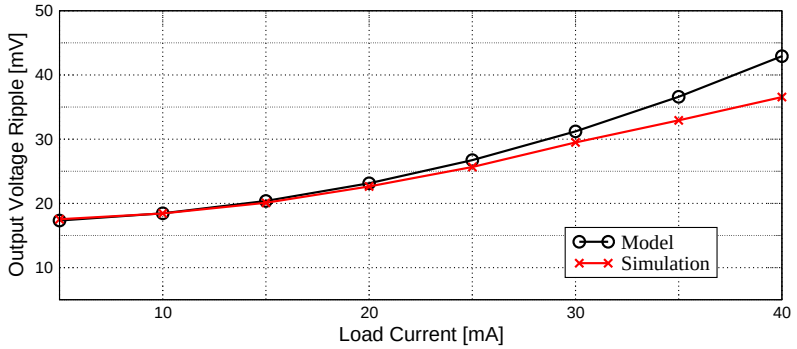


(c)

Figure 6.13: Simulated versus model expected value comparison for different loading current with DC/DC PMOS width $W_S = 15\,\text{mm}$ (Synchronous Version): (a) Overall efficiency, (b) Inductor peak current and (c) Output voltage ripple.

6.4 Model Validation: Prototype and Measurements

6.4.1 Design and Test Considerations

A 0.35μm CMOS proces prototype has been developed following the design procedure described above. The output stage and the driving chains have been implemented using thick oxide mosfets according to the previous description; the transistor size has been chosen to be 10 mm and 5 mm for the PMOS and NMOS power switches respectively. The control unit, based on the Fig.6.7 architecture, has been realized combining digital standard cells provided by the design kit and well-known hysteretic comparator described in [11]. The LC tank has been placed on board using a 100μH inductor with 2.5 ohm serie DC resistance and a 2.2μF Tantalum capacitor with 50 ohm ESR.

A simplifyed DC/DC test bench schematic is shown in Fig.6.4.1 [47], [48]. The input filter composed of R_{in} and C_{in} allows to the input source V_S to deliver a dc current only equals to the average input current; if the value of R_{in} has been previously measured, the average DC/DC input current $\overline{I}_{in}$ is obtained by the measured voltage drop accross R_{in} itself. Measuring the average input voltage $\overline{V}_{in}$ (by an Agilent 34401A) the average input power $\overline{P}_{in}$ is obtained, with an acceptable accuracy, by multiplying $\overline{V}_{in}$ and $\overline{I}_{in}$. The input resis-

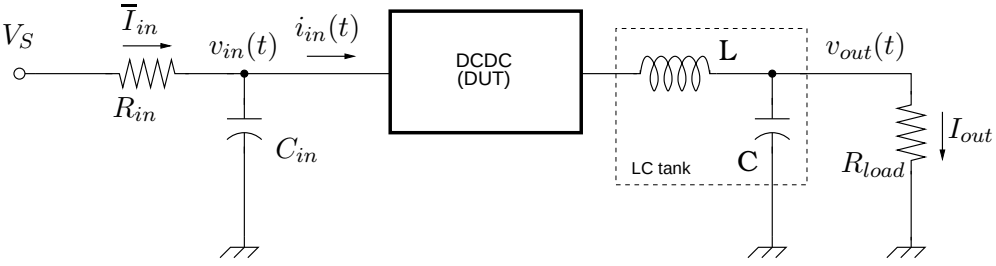


Figure 6.14: DC/DC Test Bench Schematic.

Element	*Value*	*Description*
R_{in} [ohm]	4.762	*Measured input resistance (nominal 4.75 ohm*
$_{Cin}$ [μF]	10	*Filtering input capacitance*
C [μF]	2.2	*Loading capacitance*
L [μH]	100	*LC tank inductor*
R_{load} [ohm]	-	*load resistance; variable in order to sink different loading current*

Table 6.4: DC/DC test bench passive elements

tance R_{in} has been estimated by means of a four terminal measurement set-up (using an Agilent 34401A). The average output power has been estimated measuring the root mean square of the output voltage V_{out}^{rms} (FLUKE45) and the load resistance R_{load} (Agilent 34401A): $\overline{P}_{out} = (V_{out}^{rms})^2/R_{load}$. Tab.6.4 summarize the passive elements on the DC/DC test board.

6.4.2 Test Results

Several tests have been performed in order to evaluate the prototype functionality; for simplicity reasons only the DC/DC input, the output voltage (external capacitor) and the switching node are available test points, thus allowing an accurate evaluations of the performance of the power converter. In Fig.6.4.2 the DC/DC output voltage and the SW-node voltage resulting from the tests at $6V$ of input voltage with 5 mA of loading current are shown. The afore descripted parametric simulations have been replicated during the prototype tests. Since the output stage size is fixed (PMOS width equals to $10mm$), the main performances sweeping the loading current have been evaluated; the measurements results curves, compared with the model and simulations ones are shown in Fig.6.16(a) and 6.16(b).

The tests results differ from the model and simulations expected values and the model validation appears as difficult. The overall efficiency error, calculated with respect to the model results, reaches

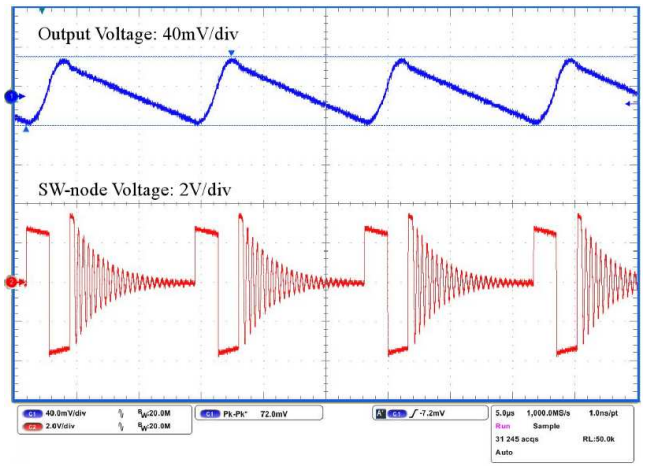
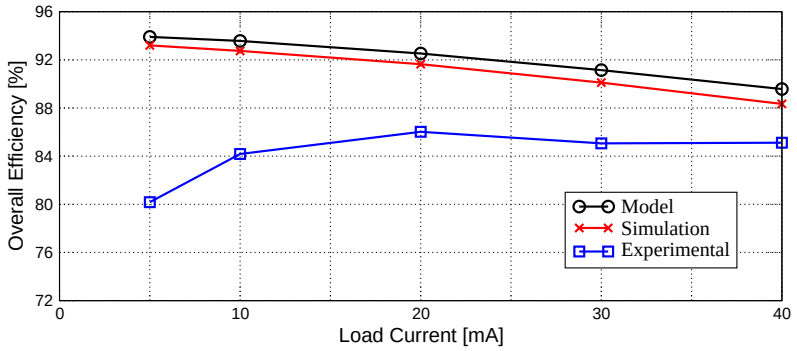
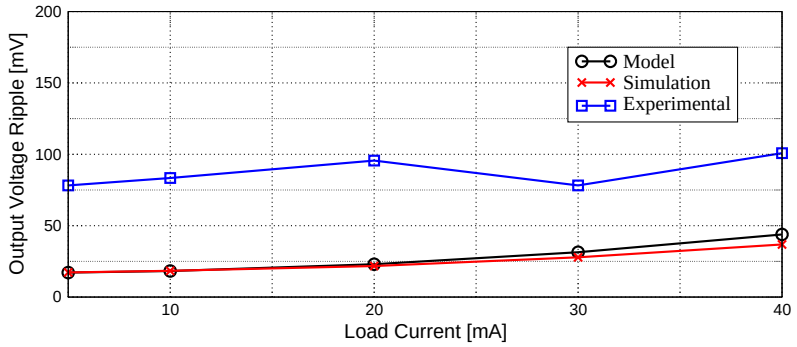


Figure 6.15: Measured DC/DC output voltage (top curve), and SW-node voltage (bottom curve).

$14\,\%$ at $5\,$mA and it is reduced to $4.5\,\%$ at $40\,$mA; the prototype shown a larger output voltage ripple with respect to the model one over the whole loading current interval. In order to explain the reasons of these poor performances, a set of transistor-level simulations has been performed introducing different possible source of degradations. The most important contribution has been individuated in the absence of dead-time in the synchronous NMOS turning-on. Similarly, reducing the driving signal edge slopes a cross-conduction current results in the DC/DC output stage leading to a $7/8\,\%$ efficiency reduction; moreover a lower driving capability increase the driving stages power consumption causing an additional efficiency drop. Adding parassitics elements as the inductor serie resistance and the capacitor equivalent serie resistance further degradation results. In terms of output voltage ripple the main responsible in the model vs measured error is the delay occuring in the control unit sensing circuits. All of these effects lead to an overall efficiency and to a ripple compatible with the values measured for the prototype samples.



(a)



(b)

Figure 6.16: Simulated and measured versus model expected value comparison for different loading current with DC/DC PMOS width $W_S = 10\,\text{mm}$ (Synchronous Version): (a) Overall efficiency, (b) Output voltage ripple.

6.5 Conclusions

The proposed mathematical model for DC/DC Buck converters with PFM control in DCM is presented and validated by means of a CMOS 0.35μ m design case. A comparison between transistor-level simulation results and calculated values from the analytical model shows the good accuracy of the proposed model. The prototype tests results exhibit a non-negligible error with respect to the expected ones revealing some chip faults. Investigating for the performances degradation causes several key-points in the DC/DC design have been highlighted.

Despite the designed integrated circuit imperfections the proposed mathematical model, validated by means of transistor-level simulations, is useful as a preliminary design tool: the model allows to evaluate the performances limits for a proper set of design constrains; since the output stage and the driving stages are generally the main contribution in terms of silicon area, the mathematical model allows to estimate the required area for this power converter.

Bibliography

[1] H. Barrass et Al., *10GBASE-T: 10 Gigabit Ethernet over Twisted-Pair Copper*, Version 1.0, Ethernet Alliance 2007, www.ethernetalliance.org.

[2] S. K. Gupta, et Al., *10GBASE-T for 10Gb/s Full Duplex Ethernet LAN Transmission over Structured Copper Cabling*, Radio Freq. Integrated Circuits Symp., RFIC 2008 IEEE. Jun. 2008. Page(s): 203 - 206.

[3] S. Bates et Al., *10 GBPS over copper lines State of the art in VLSI*, System-on-Chip for Real-Time Applications, Fifth International Workshop on, 2005. July 2005. Page(s): 491.

[4] S. K. Gupta, et Al., *A 1-GS/s 11-bit ADC With 55-dB SNDR, 250-mW Power Realized by a High Bandwidth Scalable Time-Interleaved Architecture*, IEEE J. Solid-State Circuits, Dec. 2006. Page(s): 2650, Vol. 41 Issue: 12.

[5] Cheng-Chung Hsu, et Al., *An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration*, Solid-State Circuits Conference 2007. Digest of Technical papers. ISSCC 2007, IEEE International. Feb. 2007. Page(s): 464.

[6] P. Delizia, et Al., *A 10-b 100-MS/s pipelined ADC with an optimized bit-stage resolution in 65nm CMOS technology*, Circuits

and Systems, Proceedings of 2010 IEEE International Symposium on, ISCAS. May-June 2010. Page(s): 4033.

[7] P. N. Singh, et Al., *A 1.2V 11b 100Msps 15mW ADC realized using 2.5b pipelined stage followed by time interleaved SAR in 65nm digital CMOS process*, Custom Integrated Circuits Conference, 2000. CICC '08. IEEE. Sept. 2008. Page(s): 305.

[8] Y Kim, et Al., *A 9.43-ENOB 160-MS/s 1.2V 65nm CMOS ADC base on multi-stage amplifiers*, Custom Integrated Circuits Conference, 2009. CICC '09. IEEE. Sept. 2009. Page(s): 271-274.

[9] B. Razavi, *Principles of Data Conversion System Design*, *IEEE Press* 1994, ISBN 0780310934 / 0-7803-1093-4.

[10] R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, *Kluwer Academic Publishers* 1994, ISBN 0-7923-9436-4.

[11] P. E. Allen, D. R. Holdberg, *CMOS Analog Circuit Design, Second Edition*, *Oxford University Press* 2002, ISBN 0-19-511644-5.

[12] P. Wambacq, W. Sansen, *Distortion Analysis of Analog Integrated Circuits*, Norwell, MA: Kluwer Academic Publishers, 1998.

[13] H. Rapakko, et Al., *On the Performance and Use of an Improved Source-Follower Buffer*, Circuits and Systems, 2007 IEEE Trans. on, Mar. 2007.

[14] K. Hadidi, et Al., *A novel highly linear CMOS buffer*, Electronics, Circuits and Systems, 1998 IEEE Intern. Conf. on, Sep. 1998.

[15] H. Rapakko, et Al., *The optimization of the settling process of the source follower based sampling circuit using continuous g_m-model*, Circuits and Systems, The 2004 47th Midwest Symp. on, Jul. 2004.

[16] D. M. Binkley, et Al., *A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design*, Computer-Aided Design of Integrated Circuits and Systems, IEEE 2003 Trans. on, Feb. 2003.

[17] C. J. B. Fayomi, et Al., *Design and Characterization of Low-Voltage analog switch without the need of Clock Boosting*, Circuits and Systems, The 2004 47th Symp. on (MWSCAS Ó4), Jul. 2004. Page(s): iii, 315 - 318, Vol. 3.

[18] M. Dessouky, et Al., *Rail-to-rail operation of very low voltage CMOS switched-capacitor circuits*, Circuits and Systems, The 1999 IEEE Intern. Symp. on, May-Jun. 1999.

[19] L. Wang, et Al., *A High-Speed High-Resolution Low-Distortion CMOS bootsrapped Switch*, Circuits and Systems, 2007 IEEE Intern. Symp. on, May 2007.

[20] Cadence Design System, Inc., *Spectre® Circuit Simulator Reference*, Product Version 7-0.1.076, 2003.

[21] C. Azzolini, et Al., *High-Level Accurate Model of High-resolution Pipelined ADC's*, Instrumentation and Measurement Technology, 2006 IEEE Conference on.

[22] B. Razavi, *Design of Analog CMOS Integrated Circuits*, *McGraw-Hill* 2001, ISBN 0-07-238032-2.

[23] K. Bult, et Al., *A fast-settling CMOS op amp with 90 dB DC-gain and 116 MHz unity-gain frequency*, Solid-State Circuits Conference 1990. Digest of Technical papers. 37th ISSCC 1990, IEEE International. Feb. 1990. Page(s): 108, Vol. 1.

[24] D. Vecchi, et Al., *100-MS/s 14-b track-and-hold amplifier in 0.18-m CMOS*, Solid-State Circuits Conference 2005. Proceedings of the 31st European. 31st ESSCIRC 2005. Sept. 2005. Page(s): 259.

[25] W. Evans, *Comparator Metastability Analysis*, www.designers-guide.org.

[26] A. Boni, et Al., *Systematic design and modelling of high-resolution, high-speed pipeline ADCs*, *Elsevier Measurements* 2005. Vol. 37 Issue: 4.

[27] Y. Chiu, et Al., *Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS*, Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005. Sept 2005 Page(s): 375 - 382.

[28] B. Murmann, et Al., *Power Dissipation Bounds for High-Speed Nyquist Analog-to-Digital Converters*, Circuits and Systems I. IEEE Transaction on, 2009. Page(s): 509 - 518, Vol. 56 Issue: 3.

[29] S. H. Lewis, et Al., *A Pipelined 5-Msample/s 9-bit analog-to-digital converter*, Solid-State Circuits, IEEE Journal of, 1987. Page(s): 954 - 961, Vol. 22 Issue: 6.

[30] S. M. Yoo, et Al., *A 10 b 150 MS/s 123 mW 0.18μm CMOS pipelined ADC*, Solid-State Circuits Conference 2003. Digest of Technical papers. ISSCC 2003, IEEE International. Page(s): 326 - 497, Vol. 1.

[31] T. Cho, et Al., *A 10 b, 20 MS/s, 35 mW pipelined A/D converter*, Solid-State Circuits, IEEE Journal of, 1995. Page(s): 166 - 172, Vol. 30 Issue: 3.

[32] D. W. Cline, et Al., *Power optimized 13-b 5Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS*, Solid-State Circuits, IEEE Journal of, 1996. Page(s): 294 - 303, Vol. 31 Issue: 3.

[33] S. H. Lewis, et Al., *Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications*, Circuits and Systems II: analog and Digital Signal Processing, IEEE Transactions on, 1992. Page(s): 516 - 523, Vol. 39 Issue: 8.

[34] J. Goes, et Al., *Systematic design for optimization of high-speed self-calibrated pipelined A/D converters*, Circuits and Systems II: analog and Digital Signal Processing, IEEE Transactions on, 1998. Page(s): 1513 - 1526, Vol. 45 Issue: 12.

[35] P. C. Yu, et Al., *A 2.5-V, 12-b, 5-Msample/s pipeline CMOS ADC*, Solid-State Circuits, IEEE Journal of, 1996. Page(s): 1854 - 1861, Vol. 31 Issue: 12.

[36] J. Ming, et Al., *An 8b 80 Msample/s pipelined ADC with background calibration*, Solid-State Circuits Conference 2000. Digest of Technical papers. ISSCC 2003, IEEE International. Page(s): 42 - 43,446.

[37] J. P. Keane et Al., *Background interstage gain calibration technique for pipelined ADCs*, Circuits and Systems I: Regular Papers, IEEE Transaction on. Jan. 2005. Page(s): 32, Vol. 52, Issue: 1.

[38] G. Chiorboli, et Al., *DAC calibration by weighting capacitor rotation in a pipelined ADC*, Third IASTED International Conference on Circuits, Signals, and Systems, Proceedings of, 2005. Page(s): 31 - 35.

[39] P. G. A. Jespers, *Integrated Converters: D to A and A to D Architecture, Analysis and Simulation*, *Oxford University Press* 2001, ISBN 0-19-856446-5.

[40] B. Arbetter, et Al., *DC-DC Converter Design for Battery-Operated System*, Power Electronics Specialists Conference, 1995. PESC '95 Record, 26th Annual IEEE. 18 - 22 June 1995 Page(s): 103 - 109, Vol. 1.

[41] M. Gildersleeve, et Al., *A Comprehensive Power Analisys and a Higly Efficient, Mode-Hopping DCDC- Converter*, ASIC 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on. 6 - 8 Aug. 2002 Page(s): 153 - 156.

[42] S. Zhou, et Al., *A High Efficiency, Soft Switching DC-DC Converter With Adaptative Current-Ripple Control for Portable Applications*, Circuits and Systems II: Express Briefs IEEE Transactions on. April 2006, Page(s): 319 - 323, Vol. 53, Issue 4.

[43] K.M. Smith Jr., et Al., *A Comparison of Voltage-Mode Soft-Switching Methods for PFM Converters*, Power Electronics IEEE Transactions on. March 1997, Page(s): 376 - 386, Vol. 12.

[44] S. Musunuri, et Al., *Improved of Light-Load Efficiency Using Width-Switching Scheme for CMOS Transistors*, IEEE Power Electronics Letters. September 2005, Page(s): 105 - 110, Vol. 3, Issue 3.

[45] B. Sahu, et Al., *An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptative On-Time Pulse-Frequency Modulation (PFM) Control*, Circuits and Systems I: Regular Papers, IEEE Transactions on. Febbruary 2007, Page(s): 312 - 321 Vol. 54, Issue 2.

[46] V. Kursun, et Al., *Monolithic DC-DC Converter Analysis and Mosfet Gate Voltage Optimization*, Quality Electronic Design, 2003. Proceedings. Fourth International Symposium on. 24 - 26 March 2003, Page(s): 279 - 284.

[47] J. Naik, *Performing Accurate PFM Mode Efficiency Measurements*, *Texas Instruments, Application Report* 2006, SLVA236.

[48] J. Naik, *Taking Accurate Efficiency Measurements*, *EETimes-India* September 2006.