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DESIGN OF A LOW-COST PASSIVE UHF RFID TAG IN 0.18μm CMOS TECHNOLOGY

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This one's for me.

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Well — I guess I'll write these ones in Italian. . .

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Chapter 1

Introduction

The process of goods stockage, management and control during the production flow is a critical issue for most of the world industries. In fact, the efficiency in mantaining an up-to-date inventory of parts and pieces, keeping track of the position of the unfinished products along the fabrication chain and identifying single items or classes of objects is a crucial parameter for the minimization of production delays and costs.

Every company is looking for more and more simple and efficient ways to carry out such operations. Manual inventory performed by several people has been long abandoned, given its expensiveness in terms of physical resources, cost and especially time; furthermore, the error ratio in such a process can be quite elevated. The introduction of novel technologies and methodologies in the last decades led to more reliable and economical forms of product identification, like optical bar reading.

Indeed, printed labels attached to the objects are extremely cheap and quick to track by means of a code reader interfaced with a common personal computer. However, there is still the need of one or more human operators handling products and reader, since the optical visibility between the latter and the labels is mandatory, and their mutual distance can not exceed few dozens centimeters.

Although the cost reduction introduced by bar reading architectures is quite important, industries are still calling for cheaper technologies, allowing to decrease the identification time and the human operator presence, in order to further shrink the goods management cost while achieving the highest reliability. Moreover, the late emerging battle against counterfeiting calls for more secure technologies, able to make life hard to falsifiers and smugglers. The most recent years have seen a new application enter this panorama, raising high expectations and research efforts: Radio-Frequency IDentification, or shortly RFID.

1.1 Radio-Frequency Identification

A Radio-Frequency Identification system is composed of a *reader*, or *interrogator*, and several *transponders* or *tags* [1], establishing a wireless communication. The tags generally exhibit a unique identifying code, allowing to track the objects they are associated to; however, they can also possess sensors and devices able to carry multiple pieces of information regarding the product or the environment conditions (for example, temperature or humidity).

There are many possible implementations of an RFID system; they are usually classified according to the transponder tipology. A first distinction can be made according to the physical means used by reader and tags to communicate between each other: the transponders can be divided — although improperly — in *magnetically coupled* and *electromagnetically coupled*. Tags of the former tipology operate typically with low carrier frequencies, no more than few MHz, and the main EM field component is the magnetic one. Usually, the coupling happens by means of inductors, able to detect the magnetic field and translate it into electric signals to be processed, and vice-versa. Since the power of such a field dramatically drops by increasing the distance between interrogator and transponder ("reading distance"), the operative field of such tags is limited to few inches: they are used,

for example, in the memory sticks employed in automatic coffee machines, but they have no applications in goods management.

In order to obtain higher reading distances, data must be transmitted exploiting the RF electromagnetic field. Tags electromagnetically coupled communicate with the reader by means of an antenna: in order to reduce the size of such a device (dependent on the field wavelength), the involved carrier frequencies are far higher than the mentioned ones, typically ranging in the UHF bands (from several hundreds MHz to many GHz). Antennas operating in such a frequency span are relatively small, featuring a size of some square centimeter, and the recent research efforts regarding low-cost, flexible materials for their realization make the UHF tags gain momentum in the market. In fact, while the UHF transponders are usually bigger than the magnetic-coupled ones, they exhibit an extremely higher reading distance, and are hence a good candidate for supply chain applications.

Another classification can be made between *active* and *passive* tags. The former category includes the transponders carrying on-board an independent power source, typically a small battery, providing the supply for the circuits. These devices exhibit the highest reading range (i.e. the maximum distance allowing a correct communication between tag and reader), reaching even some kilometers: they are mostly employed to control position and movements of small animals, and the high power budget allows the presence of many sensors. Their use in the supply chain management is however scarcely considered, since the cost of battery and manufacturing is unbearable for high volumes, and there is no use in having such an elevate reading range for this kind of purpose.

On the other hand, passive tags do not carry on-board any power source, but they obtain their power supply from the incident electromagnetic field generated by the reader, by means of an antenna or inductors. Obviously, the available power is far lower than the one of the active transponders: there are strong limitations for the EM field strength set by local governments, due to health concerns. Since the collectable power rapidly decreases with the distance from the inter-

Figure 1.1: Photograph of a UHF RFID interrogator

rogator, passive tags usually carry a very small number of sensors and a limited amount of data, and their reading range rarely exceeds some meters. Nonetheless, they can be extremely tiny and compact, and their production costs are considerably lower than the ones of active tags. Moreover, they do not need direct visibility with the reader, as long as they are reached by the EM field. They are therefore suitable to fit the industries needs for the manufacturing chain: the communication is established automatically with the reader, and the human work can be minimized. Furthermore, it is extremely difficult to falsify such devices, and the system security can be further increased by using encrypted communications.

Radio-Frequency Identification is now a mature technology, ready to take the place of optical bar reading in the supply chain management. UHF passive tags have quickly gained the spotlight, offering the best promises for both devices and personnel cost reductions. While the first commercial RFID systems are now available on the shelves (as the reader in Fig. 1.1), there are still considerable opportunities in such a market: the research efforts are moving towards cost-reduction techniques, in order to produce cheaper and cheaper tags to be sold in huge amounts. The present work addresses the design of a passive UHF RFID transponder, featuring a strong cost mini-

mization policy: if the proposed tag could manage to achieve the same performances of the state-of-the-art devices with a reduced production cost, it would become a fierce competitor in the rapidly expanding RFID market.

1.2 Chapters overview

After the previous brief introduction addressing the market requests calling for Radio-Frequency Identification, more technical issues are analyzed in the following chapters. An overview of the main electromagnetic propagation laws is reported in Chapter 2, as well as the description of the standards regulating the communication requirements and contents of the desired RFID system. Furthermore, an analysis of the tag architecture and its design goals are reported in the same chapter.

After such a top-level description, Chapter 3 and 4 are dedicated to the analysis of the proper tag analog frontend design, depicting in detail architectural choices, circuits and methodologies, respectively of the power harvesting and management section and of the interface between the EM field and the digital core of the tag. Simulation results are reported validating the circuit theories and analyses.

Before the conclusions drawn in Chapter 6, the results of the measurements performed on a testchip are described in Chapter 5. Since the chip exhibits many differences from the actual product, the same chapter depicts also such variations, as well as the board appositely designed for testing purposes and the measurements methodologies.

1.3 Collateral activities

In addition to the development of the RFID passive tag, many secondary projects have been accomplished during the Ph.D. studies period. The main ones are reported in the following sections.

1.3.1 LVDS serializers/deserializers

The transmission of great amounts of parallel digital data throughout PCBs and wired systems suffers from several drawbacks, mainly in terms of space and mutual interference. On the other hand, achieving high data-rates with a serial transmission is a challenging task, since the time-division multiplexing of several bits on a single channel causes a dramatic shortening of the equivalent bit period.

Single-ended data transmission on CMOS levels becomes less and less suitable for such a purpose. Therefore, the Low-Voltage Differential Signaling (LVDS) is often used for point-to-point data transmission across boards, as its differential logic may provide high achievable data-rates and tolerance to noise and disturbances with a moderate power consumption.

Several LVDS serializers and deserializers have been designed, with data-rates ranging from 20 to 125Mb/s and bit frequencies from 800 to 1000MHz. Both the proper LVDS transceivers and the SerDes structures have been analyzed and designed according to the mentioned specifications, using both CMOS and BiCMOS 0.35μm technologies: the former relatively obsolete process has been taken to its limits in order to achieve the considerable involved data-rates.

1.3.2 Analog/Digital converters

While the outstanding trend of devices minimization and numeric data analysis techniques push the utmost of the signal processing into the digital domain, the vast majority of the physical signals is analog. The market of analog/digital converters able to interface sensors and actuators with the binary world is unceasingly growing, calling for more and more accurate and fast ADC's.

Particularly, UWB applications raise a request on high-speed and moderate or low resolution converters. The topology allowing the highest conversion rates is definitely the flash one: $2^N - 1$ parallel comparators with different threshold levels decide the digital output code

of the ADC. Given the exponential growth of devices with the resolution, soon leading to unacceptable area and power consumption, such a kind of converter is suitable to be used only for a small number of bits.

A 2GS/s 8-bits flash ADC has been developed in 0.18μm standard CMOS technology [2]. The converter consists of two interleaved 1GS/s ADC's driven by a common track and hold stage. Many techniques have been employed in order to reduce power and area occupation, like a subranging first decisional stage with mobile thresholds and chained preamplifiers. Furthermore, a foreground calibration technique has also been introduced [3], able to overcome the problems raising from the components mismatch. The overall power consumption is 1.2W, which is a good result in comparison to the works reported in literature featuring comparable technologies.

1.3.3 DC/DC converters

Recent years have seen the development of many novel power sources, able to exploit more durable and environment-aware energies than the ones coming from oil and other traditional materials: photovoltaic panels and fuel cells are now mature technologies ready for the global market. The latter are more suitable for portable applications; however, during their life-cycle the DC voltage they can provide ranges approximately from 0.4 to 0.6V, a value too low to empower most of the current electronic devices. Therefore, some sort of step-up DC/DC converter has to be used in order to provide a suitable power supply to the different applications: the conversion process should exhibit the maximum efficiency.

A DC/DC converter has been designed in order to achieve a 5V output DC voltage from a fuel cell. It has been realized with a digital CMOS 0.18μm technology with 5V-capable I/O transistors, and exhibits a power efficiency of more than 89% [4]. Such a low power loss is obtained by combining a Dickson-like charge pump and a boost converter.

1.3.4 RF circuits for reference signals generation and distribution

Almost every electronic circuit needs a known-frequency signal to be used as clock (in A/D and D/A converters, for example) or as local reference (in RF frontends involving mixers). Recently, the frequencies involved in such applications drifted more and more towards the 1-10GHz interval, and the request for their precision and low-noise increased as well; however, quartz oscillators, granting the latter properties, rarely reach the 100MHz band. In order to obtain the much higher required frequencies, a Phase-Lock Loop must be employed, having constant or programmable division factor according to the target application.

Several PLL's have been designed with different purposes: a synthesizer to be used in WLAN transceivers operating in the 4-5GHz band [5] with programmable output frequency and low noise specifications (realized in 0.35μm BiCMOS technology), a fixed-factor (x12) PLL able to run from 200 to 900MHz for SerDes clocking (0.35μm CMOS technology), another fixed-factor (x260) PLL running nominally at 13GHz for radar applications (90nm CMOS technology). Each one of them has been top-level designed, and many internal blocks have been developed more in detail, especially dividers and oscillators.

Finally, the issues of clock transmission across the different blocks of a chip have been analyzed, especially for ADC's and serializers, which happen to exhibit a high sensitivity to clock skew, slow edges and supply noise on the clock lines.

Chapter 2

System Architecture

In order to design the tag, a preliminary analysis must be performed on the operating conditions that the transponder will face during its primary activity.

The main concerns regard the strength of the received electromagnetic field, that can be estimated, according also to the standards and the local government rules regulating the matter, by resorting to the basic electromagnetic propagation laws. Once known the order of magnitude of the received power and the signals format, it is possible to lay out a basic schematic of the transponder, as well as describing its main desired properties.

Before starting the proper design, several considerations about the tag components can be done regarding power optimization, and the most important architectural choices can be made. The latter are primarily driven by the cost reduction policy adopted for the project, then successively by low power consumption and area occupation constraints.

In this chapter, after a quick overview of the most useful electromagnetic propagation laws and the standard regulations adopted for the project, a global description of the tag is exposed. Moreover, the antenna and chip properties are evinced according to the available operating conditions and design goals.

2.1 Fundamentals of EM field propagation

The propagation of an electromagnetic wave into open space from its source point is spherical. An antenna radiating a power P_T uniformly in all directions is called "isotropic" or "spherical" (Fig. 2.1).

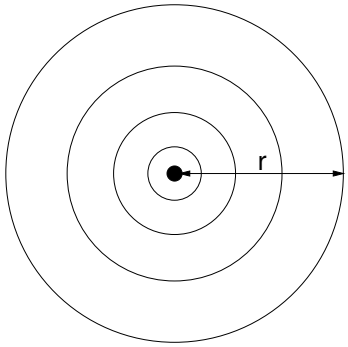

Figure 2.1: Isotropic antenna propagation

The radiation density measured in any point at a distance r from such an emitter is

$$S = \frac{P_T}{4\pi r^2} \tag{2.1}$$

This condition holds in the so-called *far field*, i.e. r is higher than twice the wavelength of the EM field λ. On the contrary, in the *near field* it is very difficult to determine the relationships between the electrical and magnetical components of the EM wave, as well as the radiation density: such an analysis is not intended to be reported in this work, and the far field condition will be assumed to hold in every calculation.

Actually, no physical isotropic antenna exists: every emitter has its *radiation pattern*, featuring a certain gain $G_T(\theta, \phi)$ for any direction described by the angles θ and ϕ. The directionality of an antenna is determined by its physical characteristics: it is possible to concentrate

the emitted power in a small solid angle, as well as prevent any energy to be transmitted in some directions, according to the application of the antenna.

The maximum gain of the emitter G_T that can be found along the main radiation direction is in any case equal or higher than 1, since

$$P_T = \int_{As} S \, dA \tag{2.2}$$

where As is the area of any spherical surface centered on the antenna. This equation holds for every emitter, and can be fulfilled only if S is higher in at least one direction than the one of the spherical antenna (having gain 1 for every θ and ϕ).

Along the main radiation direction, therefore, the radiation density is G_T times the one of an isotropic emitter:

$$S = \frac{P_T G_T}{4\pi r^2} \tag{2.3}$$

The *Effective Isotropic Radiated Power*, or shortly EIRP, can be defined as the power that should be provided by a spherical antenna in order to experience the same radiation density at a distance r coming from the given emitter:

$$P_{T,EIRP} = P_T G_T \tag{2.4}$$

For example, a dipole antenna exhibits a maximum gain G_T=1.64: hence, its $P_{T,EIRP}$ is equal to $1.64 P_T$. Actually, the power emitted by a dipole antenna is also known as ERP (*Effective Radiated Power*), so $P_{T,EIRP} = 1.64 \, P_{T,ERP}$.

On the other hand, a receiving antenna (in matching conditions) sensing a radiation density S delivers the following available power to its load [6]:

$$P_{AV} = \frac{\lambda^2}{4\pi} G_{ANT} \tag{2.5}$$

where λ is the wavelength of the received electromagnetic wave and G_{ANT} is the receiving antenna gain (assuming the antenna to be oriented in the maximum gain direction).

From (2.3), (2.4) and (2.5) it follows that

$$P_{AV} = P_{T,EIRP} \left(\frac{\lambda}{4\pi r} \right)^2 G_{ANT} \tag{2.6}$$

The last equation, known as *Friis transmission equation* [7], describes the amount of received power of an antenna with gain G_{ANT} at a distance r from a source emitting an EM wave with wavelength λ and power $P_{T,EIRP}$.

It can be noticed that the available power experiences an inverse dependency on the square of the distance between the emitter and the receiver, that is, in the RFID case, the reading distance: therefore, if r doubles, the available power will become 1/4. This poses strong limitations on the maximum possible reading range.

2.2 Adopted standards

There are several standards regulating the Radio-Frequency Identification communications for passive tags. The choice of the one to be adopted proves important, since many design constraints and possible solutions depend on the different requirements to fulfill. In fact, parameters like the operating frequency (that can be in the 800-900MHz or in the 2.4-2.5GHz bands) or the reader maximum emission power (generally from 500mW to 4W or more) heavily impact the reading range of the tag; moreover, the hand-shaking protocol and the different forms of preambles may suggest different solutions for issues like synchronization and power management, and the possible requirement for an embedded memory in the tag may influence the technology options and the architectural choices of the design.

Although it is generally possible to reuse a considerable part of a chip designed for a certain standard in the eventual migration to

another one, several changes have anyway to be made, especially in the digitally synthesized logic parts of the circuit. Furthermore, it is not a good practice to design a tag able to fulfill the requirements of different standards, while usually readers are multi-standard compliant. In fact, the extremely low power available to passive tags is a tight bottleneck, and the introduction of a great amount of analog and especially digital circuits necessary to achieve the compliance with different standards would cause a noticeable extra power consumption, impacting the tag performances and the reading range. Therefore, passive tags are generally specialized devices able to fulfill the requirements of the specific standard they have been designed for.

Among the various possibilities, the standard adopted for this design is the ISO/IEC 18000-6, section B, first released by the International Organization for Standardization in August 2004 [8].

Such a standard dictates the parameters for air interface communications in a band ranging from 860 to 960MHz. It sets the rules for a half-duplex reader-tag communication (i.e. while the reader transmits the tag listens and vice-versa), based on the amplitude variations of the RF field power transmitted by either reader or tag. While it addresses also several issues related to the reader capabilities, like collision arbitration policies or emission masks, the important part of the standard for the present project is the one regulating the communication protocols and electromagnetic features (like data-rate, power, modulation depth and their respective tolerance) that affect the design of a compliant tag. A peculiar feature of the standard is that no non-volatile memory is required to be on the transceiver, so there is no need for EEPROM-capable technologies.

The restrictions dictated by the ISO18000-6B standard are further tightened by the local governments specifications. As a matter of fact, according to the country where the RFID system will be used in, the rules regulating allowed bandwidths and power levels may increase the constraints and reduce the alternatives in architectural and structural choices. Since the designed tag is specifically thought for the Italian market, where the laws on wireless and electrical emis-

sions are particularly strict with respect to the rest of the western world, several rules and requirements have to be fulfilled besides the ISO compliance ones. Such a regulation can be found in the ETSI rule sets [9] for European countries.

The main communication rules and specifications, coming both from the ISO18000-6B and ETSI guidelines, are reported in the next two paragraphs, considering respectively the reader-to-tag and tag-to-reader transmission.

2.2.1 Reader-to-tag communication

The communication is based on the reader-talks-first principle: the interrogator sends a request to the transponders, that will answer (each one independently, or singularly if the reader asks to "talk" only with a single, specified tag) only after the end of its request. No tag transmits unless it has received and properly decoded any instruction.

The transmitted electromagnetic field is composed by a carrier waveform, whose frequency is established by the ETSI regulations to be in the 865-870MHz span (the operating frequency for the project has been assumed to be f=869.5MHz, corresponding to a wavelength λ=34.5cm in open space), amplitude-modulated (ASK) by a binary pattern having a 40kb/s data-rate. The maximum allowed transmission power is set to 500mW ERP, corresponding to 820mW EIRP, although at the present moment the italian regulations are switching to the less restrictive EU ones which allow a transmitted power of 4W EIRP in the same frequency range.

Assuming the transponder to have a unity-gain antenna, its available power (in impedance matching conditions) coming from (2.6) versus the reading distance is reported in Fig. 2.2: it is worth noticing that such a power rapidly drops into the microwatts range when the distance becomes higher than few meters. The power awareness and efficiency of the tag is therefore a must in order to ensure a decent reading range for the product.

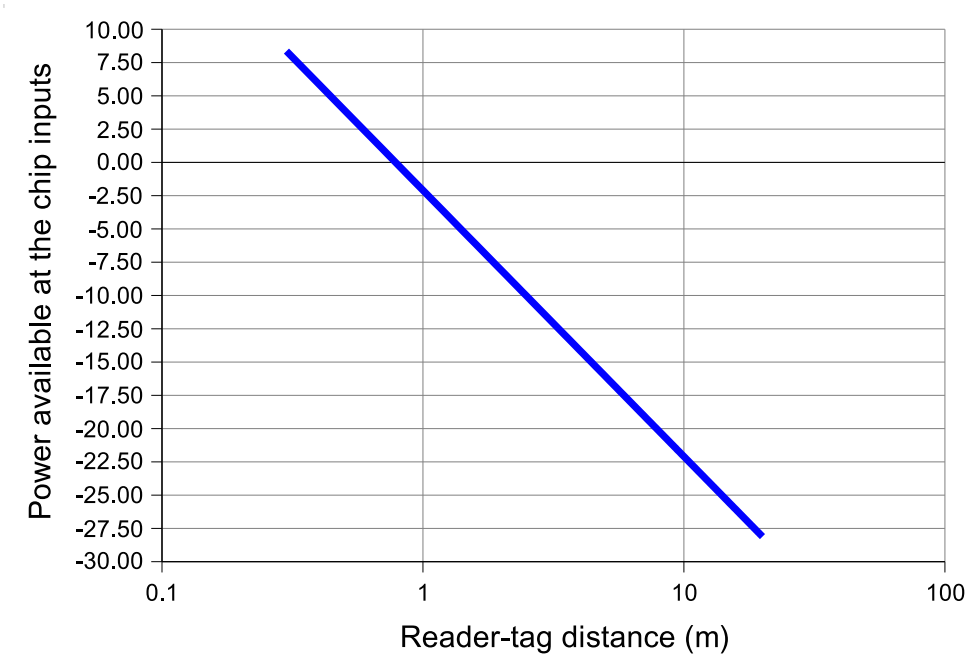

Figure 2.2: Available power for a 0dB matched antenna tag with a 500mW ERP standard compliant reader vs. reading distance

The transmitted bits are Manchester coded, i.e. halfway any bit time there is always a level transition (0→1 for a logic 0, 1→0 for a logic 1): this proves particularly useful for synchronization purposes, as explained in Section 4.3. There is also another parameter, defined as the amplitude modulation depth:

$$M = \frac{A - B}{A + B} \tag{2.7}$$

where A and B are, respectively, the maximum and the minimum level of the carrier amplitude (as shown in Fig. 2.3). Although the ISO/IEC

standard lets M to be nominally 18% or 100%, only the former modulation depth is allowed according to the ETSI specifications: from (2.7), the ratio between B and A in such a case is 0.695, and the demodulation circuit of the tag (described in Section 4.2) must be able to resolve the difference between the two levels, that could be as low as a few dozens mV.

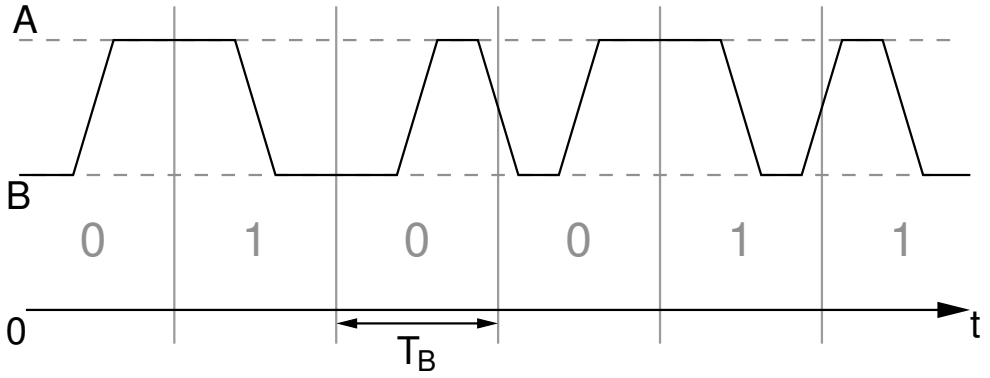

Figure 2.3: Example of bits transmitted from the reader (envelope)

The reader-to-tag communication protocol set by the standard establishes a transmission packet divided in 7 main phases:

1. *Preamble Detect*: an unmodulated steady RF carrier, transmitted for a 400μs minimum time interval, during which the tag powers up and stores the field energy.
2. *Preamble*: 9 Manchester NRZ zeroes.
3. *Delimiter*: a known start-of-transmission 10-bits data path.
4. *Command*: the proper command.
5. *Parameter*: according to the command, a small amount of parametric data can be transmitted.

6. *Data*: Application data fields, according to the command.

7. *CRC-16*: Control sequence.

Commands, operands and control sequences are described in detail in the cited standard. Since only the first two phases affect the analog frontend behavior, they will be taken into account in the apposite sections, while the others can be easily found in [8].

2.2.2 Tag-to-reader communication

The return link is established by using the backscatter technique. During the answering phase, the reader continues to produce an unmodulated RF carrier, providing the necessary energy to the tag. The latter transmits the information back to the interrogator by modulating its reflected energy: its state is toggled between "high reflectivity" and "low reflectivity" — according to the logic value to be sent to the reader — by changing the equivalent impedance seen by the antenna. The reader is able to detect the backscattered energy modulation and thus to decode the transceiver answer.

The usual state of the tag is "low reflectivity" (or "space"), i.e. there is impedance matching at the antenna terminals and the power delivered to the tag chipset is maximum: the amount of electromagnetic reflected energy is minimum. In the opposite "high reflectivity" state (or "mark"), usually by means of a switch, the antenna terminals are shorted each other, and, as explained by the antennas theory, a stationary waveform is formed where no power is delivered to the load and the energy reflected into the open space is maximum. According to the standard, the difference between the two states must satisfy a specific requirement, expressed as a function of the radar cross sectional area variation (i.e. the difference of the equivalent area shown to a radar source). This parameter is influenced by the strength of the switch and by the antenna physical and electrical parameters.

A simple graphic explanation of the two reflectivity states is reported in Fig. 2.4. It should be noticed that, in the "mark" case, no

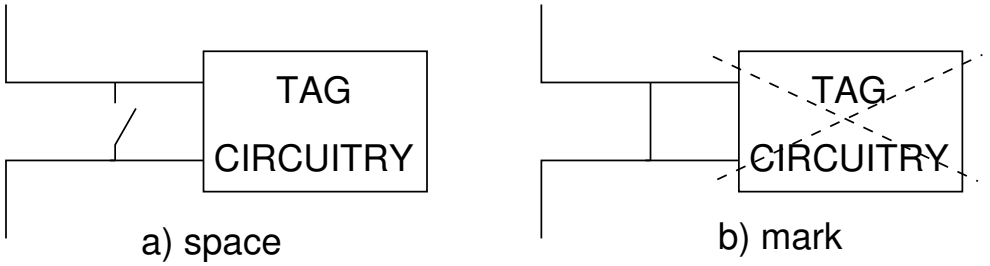

Figure 2.4: a) low and b) high reflectivity state of the tag

source empowers the transceiver circuits, since the EM field is reflected back to the reader: it is mandatory therefore to introduce a sort of energy storage device able to provide a suitable power supply for the blocks during the "high reflectivity" intervals.

The return link data-rate is set to 40kb/s, equivalent to a symbol period T_{rlb}=25µs, with a tolerance of $\pm$15%. Data is coded according to the FM0 (or Bi-Phase Space) technique: a transition occurs at the beginning of each transmitted bit, and at half the bit time of every logic 0. An example is reported in Fig. 2.5.

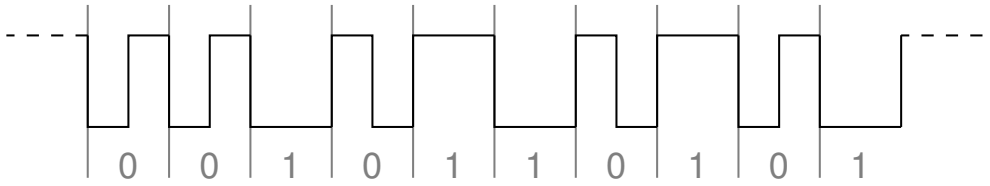

Figure 2.5: Example of FM0 transmission

The tag-to-reader communication protocol set by the standard establishes a transmission packet divided in 4 main phases, explained in detail in [8] and not directly affecting the design of the analog frontend:

1. *Quiet*: a quiet time interval where no backscatter occurs.

2. *Preamble*: A known start-of-transmission bits packet.

3. *Data*: Data fields, according to the previous reader request. Typically contains the tag unique identification code.

4. *CRC-16*: Control sequence.

2.3 Design goals and strategies

The proposed tag should be ready to enter the supply chain management RFID market. Since, as described in Chapter 1, the best transponder tipology to be employed in such a field is the passive electromagnetic one, it should exhibit performances comparable to the ones of the tags of the same category already present on the market, at a lower cost.

In order to perform a comparison with the already available — or announced — products, the main parameter taken into account is the reading range. Obviously, such a comparative test must be done in the same operating conditions for every device. Many results found in literature have therefore to be reported to the adopted standard regulations: although this procedure may experience a certain approximation, the comparison is still fair enough.

Besides the free-space propagation hypotesis and the ISO18000-6B and ETSI regulations described in the previous sections, the only operating condition to be set is the working temperature range. The supply chain applications that the tags are designed for do not require extreme values, especially for the food industry where rarely temperatures exceed some dozens degrees. A quite expanded range has been considered, spanning from 0 to 85 $^{\circ}$.

In order to reduce the production costs, in the tag design the following guidelines have been considered:

- *Reducing the number of components*. Manufacturing costs experience a noticeable dependency on the number of discrete objects to be included on-board: although the price of common devices like SMD capacitors or inductors is extremely low, the PCB mounting and testing procedures exhibit a non-negligible impact on the product cost. Therefore, specific techniques must be employed in order to reduce the tag components to the smallest possible amount, that is 2: the antenna and the chip.

- *Cutting the chip production costs*.

  The price-per-tag can be highly reduced by adopting a low-cost, general purpose and relatively old technology for the chip fabrication, although the design of the analog blocks may suffer from the devices non-optimal performances and the absence of specific process options: such limitations must be overcomed with a smart design.

  It is preferrable to employ the chip-on-board strategy: the die is directly attached to the antenna. Besides the advantages coming from reduced parasitics effect and small size and thickness, the expenses due to the package are utterly removed. Bonding is still present, although in this case the pads are immediately connected to the PCB surface.

  The chip area must be minimized.

  Special care in the circuit design must be taken in order to avoid any unnecessary post-fabrication operation, like wafer sort trimming to compensate the process variations.

The reading range can be maximized by designing an efficient power rectification network and cutting the current consumption of the main circuits, i.e. the design is driven by low-power constraints, with the limitations due to the abovementioned low-cost policies. The following chapters will describe in detail the adopted design techniques.

2.4 Tag structure and components

According to the guidelines exposed in Section 2.3, the designed tag is made up of a planar antenna and the chip (object of this work). Since there are no other components, the only connections to be made are between the antenna terminals and two I/O pads on the die.

2.4.1 Antenna properties

Although the physical design of the printed antenna (and thus its size, type and material) is a part of the project not covered by this work, the design provides its electrical characterization.

In fact, in order to transfer the maximum power that can be harvested from the RF field to the tag, the condition of impedance matching must be met between antenna and chip. Such a constraint means that the antenna has to be realized in a way that its impedance value is equal to the complex conjugate of the chip one [10]. The latter is basically determined by the devices present between the two chip inputs, as better explained in Section 3.4, and is typically composed of a real (resistive) and a negative imaginary (capacitive) part, allowing hence to model the chip with a $R_{IN} - C_{IN}$ equivalent series circuit.

Therefore, the power matching can be achieved by setting the antenna equivalent resistance R_{ANT} to be equal to R_{IN}, while C_{IN} has to be balanced with an equivalent inductor L, as shown in Fig. 2.6. Since an accurate design allows to keep the inductance value as low as few dozens nH, there is no need to place an inductor as external component, that would basically add an undesired extra cost. As a matter of fact, an inductive antenna can be designed by setting its resonance frequency f_{ANT} slightly above the one of the RF carrier used in the communication (i.e. f=869.5MHz): a careful antenna design can thus grant the power matching condition without adding extra components.

If the matching condition is met ($R_{ANT} = R_{IN}$ and $\omega L = (\omega C_{IN})^{-1}$), the Friis equation in (2.6) can be used without introducing any de-

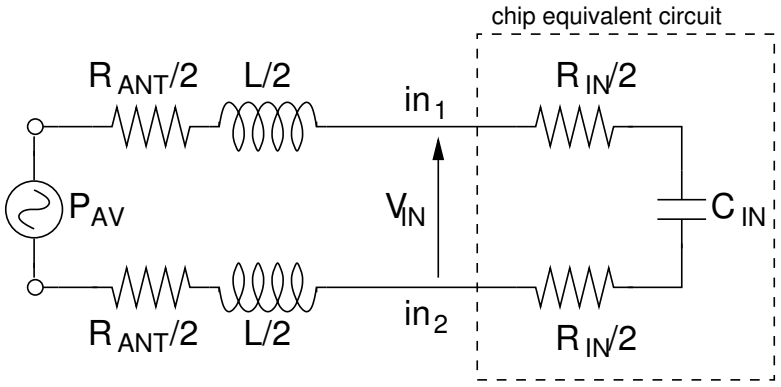

Figure 2.6: Passive tag equivalent schematic

grading factor due to the impedance mismatch, and the available power at the chip inputs is the highest for the given reading distance. It is possible from here to calculate the input peak voltage: referring to Fig. 2.6, it can be shown that

$$V_{IN} \approx \sqrt{2\frac{P_{AV}}{R_{IN}}}\frac{1}{\omega C_{IN}} \tag{2.8}$$

From the last equation, it can be seen that the input peak voltage can be increased by designing a tag with low resistive and capacitive parts. Since, given the non-linear behavior of the RF/DC power retriever explained in Chapter 3, a higher rectification efficiency can be achieved with an elevate input peak level, the tag should be in some manner designed to minimize R_{IN} and C_{IN}. However, it should be noticed that the physical realization of a good antenna with a very low real impedance is a tough task, since the antenna gain would considerably decrease. Moreover, the parasitic effect of the ohmic losses in the antenna tracks would introduce a noticeable efficiency drop. Finally, design constraints better explained in Section 3.4 limit the possibility of decreasing both R_{IN} and C_{IN} at the same time.

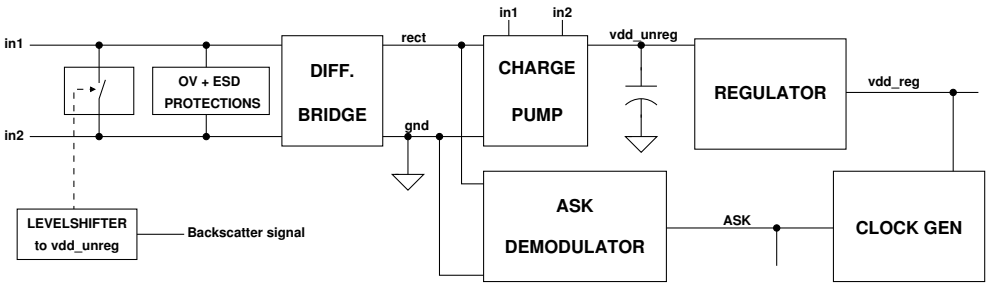

Figure 2.7: Block diagram of the designed chip

2.4.2 Chip properties

The chip is made up of two main sections, the analog frontend and the digital core. The scope of this work is the design of the former one: its block diagram is shown in Fig. 2.7. Its main function is the generation of a stable rectified DC voltage (by means of the bridge and the charge pump) starting from the incident RF field caught by the antenna. Such a power supply is then regulated by a suitable regulator before being used to empower the digital section. All of these circuits, along with the device safety protections, are described in detail in Chapter 3.

There are also many blocks interfacing the RF field and the digital core: a demodulator, a clock generation system, a Power-On-Reset block and the backscatter transistor, as well as level-shifters able to convert the digital data into different power domains. Such circuits are described in Chapter 4.

Although for testing purposes it is useful to access many points of the circuit (as explained in Section 5.1), the actual RFID chip has only 2 I/O pads, $in1$ and $in2$. No external components are required by the circuitry, and there is no need for a package, since the two pins can be easily bonded directly on-board: the production costs are considerably relaxed.

Furthermore, the cost reduction policy driving the project led to the choice of a cheap digital 0.18μm technology, not featuring any particular analog process option, except for MIM capacitors. Actually, these devices have been used (for the capacitors of the charge pump in Section 3.2), but they could be easily replaced with interdigited fringe capacitors to avoid the use of an extra fabrication mask. However, since the silicon foundry did not provide any model for such a kind of device, the MIM option has been employed.

The chosen technology is relatively out of date, since at the present moment many 65nm and 45nm microchips are facing the market. Its expensiveness is therefore quite limited; furthermore, it is a good compromise between still older and newer, short-channel digital CMOS processes. The former are slightly cheaper, but the long-channel MOS thresholds can be high enough to limit the circuit functionality (the threshold is a crucial parameter, as explained in detail in Section 3.1). The latter exhibit transistors with lower threshold, but also with a non-negligible leakage and gate currents, that would heavily impact the functionality of an ultra-low-power product such as an RFID tag; moreover, their silicon area costs are definitely higher.

The design process features 1 poly, 5 thin metal layers, and a sixth thick metal top layer with high current capabilities and low resistance.

Available devices in the chosen process are standard and low-threshold (LVT) CMOS transistors, as well as native zero-threshold (ZVT) NMOS's: each one of these components is present both in a thin-oxide and a thick-oxide form, although no 3.3V-capable thick-oxide transistor has been actually employed in the design. Along with the typical model, the silicon foundry provides worst-case descriptions for every kind of transistor, namely WS (worst-speed case) and WP (worst-power case). Furthermore, according to the fab statistical information, MonteCarlo models of the devices have been implemented in order to take into account the effects of random wafer and mismatch variations.

A summary of the technology properties is reported in Table 2.1.

Name	**Value**
Minimum standard device channel length [μm]	0.18
Typical standard NMOS threshold [V]	0.51
Typical standard PMOS threshold [V]	-0.5
Typical LVT NMOS threshold [V]	0.31
Typical LVT PMOS threshold [V]	-0.42
Typical ZVT NMOS threshold [V]	-0.02
Typical MOS capacitance [$\mu F/m^2$]	8500
Typical MIM capacitance [$\mu F/m^2$]	1000

Table 2.1: Adopted technology main properties

Finally, it should be noticed that at least one post-fabrication operation must be done on the chip: the assignment of the identifying code. This is done at the wafer sort by acting on 64 fuses in the digital section.

Chapter 3

Power management

The absence of any form of on-board power source in the RFID tag calls for the design of an RF/DC converter able to harvest the energy of the UHF electromagnetic field and to transform it in a suitable supply for the circuits of the transponder.

As a matter of fact, the power level recoverable from the RF field, as reported in equation (2.6), decreases rapidly with the reading distance: the desired tag should work at several meters from the interrogator, where the available power can be as small as few microwatts. The power retriever should hence be able to provide a supply voltage to the analog and digital circuits of the tag sufficient to grant their correct functionality: it is mandatory to optimize the RF/DC converter in order to obtain the highest efficiency in such a low-power condition. The goal is quite difficult to achieve, since the chosen technology limitations prevent the usage of most of the architectures present in literature.

This chapter describes the solutions adopted to perform such a task, as well as the circuits for the regulation of the rectified level and for the chip safety. Furthermore, an equivalent model for the calculation of the chip input impedance has been developed: on the basis of such an analysis, the antenna electrical properties can be evinced.

3.1 Low voltage activation bridge

3.1.1 Full-wave rectifier

The unmodulated input voltage can be written as

$$v_{in}(t) = V_{IN}\sin(2\pi ft) = V_{IN}\sin\left(\frac{2\pi t}{T}\right) \tag{3.1}$$

where f is the UHF carrier frequency (869.5MHz) and T is the corresponding time period.

Most RFID tags presented in the last years employ structures based on the well-known full-wave diode bridge, reported in Fig. 3.1.

Assuming negligible, for the sake of simplicity, the discharge of the loading capacitor, the $rect$ terminal sets one diode threshold (V_T) below the peak of the highest potential reached either by $in1$ or $in2$. Similarly, the gnd terminal sets V_T above the lowest peak hit by one of the two input pins. Therefore, the resulting rectified voltage V_{rect}, as shown in Fig. 3.2, is

$$V_{rect} = V_{IN} - 2V_T \tag{3.2}$$

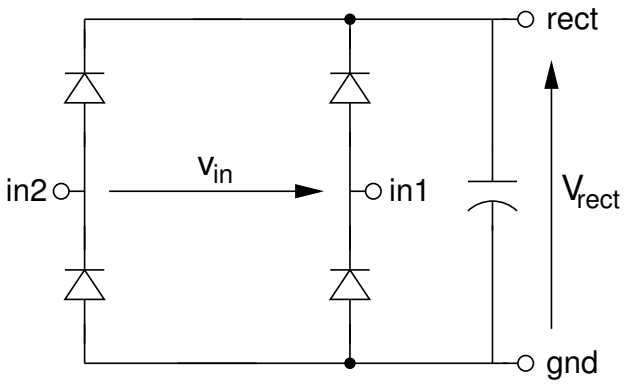

Figure 3.1: Schematic of the full-wave rectification stage

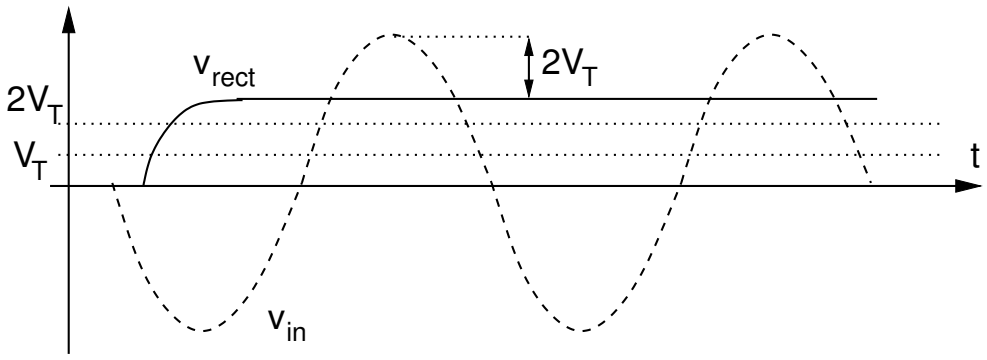

Figure 3.2: Output waveform of the full-wave bridge

It is immediate from (3.2) that the minimum input peak value useful to achieve a non-null rectified voltage is $V_{IN} = 2V_T$: if it was lower, the diodes would not conduct and the output voltage would be zero, since no current flow could charge the capacitor.

The loss of two diode thresholds in the rectification process for a single stage calls for the use of low-V_T devices, especially in this kind of application where V_T is not negligible with respect to V_{IN}. As a matter of fact, most reported works employing this technique, in order to limit the voltage drop, resort to specific technology options. Most used are Schottky devices [11] [12] [13] [14], which feature very low forward voltage, but also tags exploiting BiCMOS [15], Silicon-on-Insulator (SOI) [16] or ferroelectric [17] processes can be found in literature. Each one of these options brings considerable advantages in the design of power efficient rectifiers; however they also feature production costs noticeably higher than the ones of a standard CMOS process. Since the desired tag is aimed to the maximum cheapness, it is not possible to rely on these expensive technologies: the diodes have thus to be implemented with diode-connected MOS transistors, experiencing considerable parasitics and relatively high threshold. The latter could be reduced by resorting to low-threshold-voltage devices, but

the limitation of the $2V_T$ rectification loss still remains a heavy burden to carry. It becomes therefore mandatory to find a way to overcome such a high voltage drop in the supply generation.

3.1.2 Adopted rectifier

The proposed solution, first seen in [18] and then in successive applications [19], is shown in Fig. 3.3.

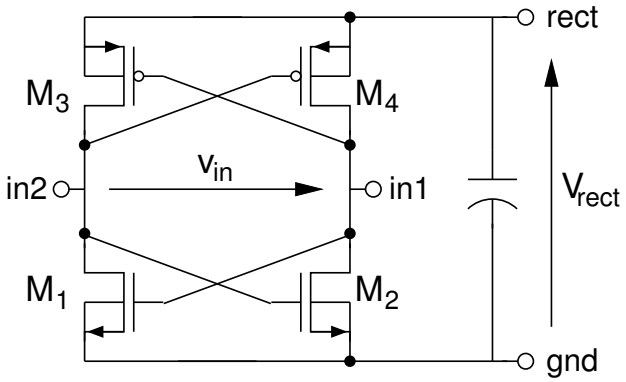

Figure 3.3: Schematic of the proposed rectification stage

In order to better understand the working principle of the circuit, initially the on-resistance of the four transistors is assumed to be negligible: hence, they behave like ideal switches. Moreover, the PMOS and NMOS thresholds are considered to be equal: $-V_{THp} = V_{THn} = V_T$. This approximation holds considering as V_T the maximum between $-V_{THp}$ and V_{THn}.

During the time intervals where $|v_{in}(t)|$ is higher than V_T, either one of the NMOS transistors M_1 or M_2 experiences a V_{GS} high enough to be turned on, while the other, having an equivalent negative V_{GS} given the simmetries of the circuit and the input signal, is in off-state. The closed switch shorts the gnd terminal to its source, i.e. the pin

with the lowest voltage: therefore, gnd follows the minimum potential present at the inputs. Likewise, the $rect$ terminal is connected to the input pin featuring the highest potential by either M_3 or M_4. During the positive phase of $vin(t)$ the closed switches are M_1 and M_4, while during the negative phase it is the dual couple M_2-M_3 that conducts. It happens thus that $v_{rect}(t) = |v_{in}(t)|$.

During the time intervals where $|v_{in}(t)|$ is lower than V_T, every transistor is in off-state since there is not enough V_{GS} or V_{SG} to turn any device on. Considering once more negligible the capacitor discharge, $v_{rect}(t)$ remains in a quiescent state until the transistors are turned again on, and its value is the last stored on the capacitor, V_T.

Waveforms showing the signals voltages in the circuit are reported in Fig. 3.4.

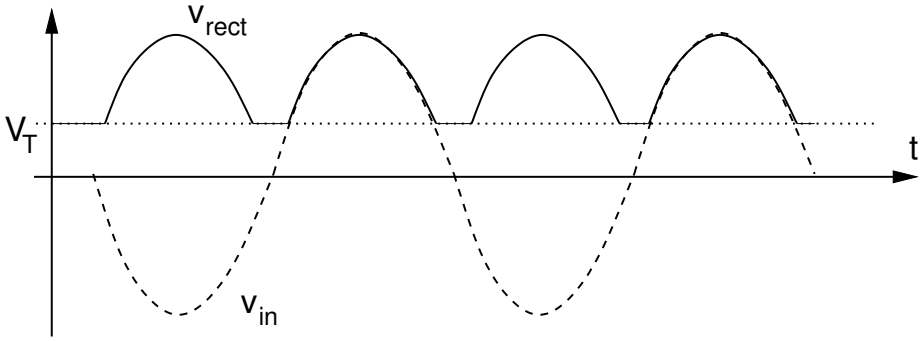

Figure 3.4: Output waveform of the proposed rectifier

It is worth highlighting that the output voltage of such a bridge is not suitable to be used directly as the power supply of a circuit, since it is far from being stable, ranging from V_T to V_{IN}. In order to reduce the ripple to acceptable levels for the application, $v_{rect}(t)$ has to be filtered: this operation can be done considering the MOS's on-resistance r_{sw}, that in the previous calculations has been neglected. In fact, the series of the r_{sw} of the two transistors and the loading

capacitor forms a low-pass RC filter, that can be sized to suppress the UHF ripple. In this case, $v_{rect}(t) \simeq V_{RECT}$, the latter being the average level of the waveform in Fig. 3.4, which can be calculated as follows on the basis of Fig. 3.5.

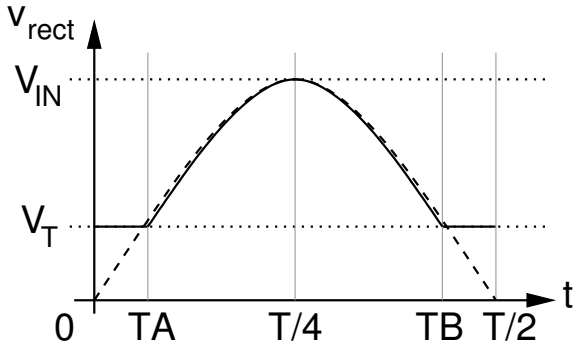

Figure 3.5: Rectifier output voltage during half input period

Analyzing half an input period (the one where $v_{in}(t) > 0$, for example), the rectifier output voltage can be written as

$$v_{rect}(t) = \begin{cases} V_{IN} \sin\left(\frac{2\pi t}{T}\right) & \text{if } T_A < t < T_B \\ V_T & \text{if } 0 < t < T_A \,,\, T_B < t < \frac{T}{2} \end{cases} \tag{3.3}$$

where

$$T_A = \frac{T}{2\pi} \arcsin\left(\frac{V_T}{V_{IN}}\right) \tag{3.4}$$

and

$$T_B = \frac{T}{2} - \frac{T}{2\pi} \arcsin\left(\frac{V_T}{V_{IN}}\right) \tag{3.5}$$

The average value of the waveform can be computed by integrating (3.3). However, given the simmetry of the function, it is simpler to calculate the integral only over half this interval (thus T/4) and then double the result:

$$
\begin{aligned}
V_{RECT} &= \frac{1}{\frac{T}{2}}\left[\int_0^{T_A} V_T\,dt + \int_{T_A}^{T_B} V_{IN}\sin\left(\frac{2\pi t}{T}\right)\,dt + \int_{T_B}^{\frac{T}{2}} V_T\,dt\right] \\
&= \frac{2}{T}\cdot 2\left[\int_0^{T_A} V_T\,dt + \int_{T_A}^{\frac{T}{4}} V_{IN}\sin\left(\frac{2\pi t}{T}\right)\,dt\right] \\
&= \frac{4}{T}\left[T_A V_T + \frac{TV_{IN}}{2\pi}\cos\left(\frac{2\pi T_A}{T}\right)\right] \\
&= 4\frac{T_A}{T}V_T + \frac{2}{\pi}V_{IN}\cos\left(2\pi\frac{T_A}{T}\right) \qquad (3.6)
\end{aligned}
$$

and, remembering the value of T_A given in (3.4),

$$
V_{RECT} = \frac{2}{\pi}\left[V_T + V_{IN}\cos\operatorname{arcsin}\left(\frac{V_T}{V_{IN}}\right)\right] \qquad (3.7)
$$

A plot of V_{RECT} versus the V_{IN}/V_T ratio is reported in Fig. 3.6; in the same figure, a comparison is made between the DC output levels of the full-wave and the proposed rectifier, assuming the same V_T for both the diodes of Fig. 3.1 and the MOS transistors of Fig. 3.3. It can be noticed that the adopted solution exhibits a lower activation threshold (V_T vs. $2V_T$) and a higher rectified output for low input voltages, i.e. in the case where $V_{IN} < 5.65V_T$: it is therefore preferrable in the worst operating conditions, enhancing the reading range of the tag. In fact, the efficiency loss (with respect to the full-wave bridge) experienced if $V_{IN} > 5.65V_T$ does not impact the correct behavior of the tag, since in those conditions there is plenty of power available to be transferred to the chip by the charge pump depicted in Section 3.2.

It is worth spending a few words on the sizing of the input RC filter, and thus on the bridge transistors. The filter must suppress the output ripple occurring at UHF frequencies, around 900MHz; since v_{rect} is used also for demodulation purposes, as explained in Section 4.2, it should be able to track the 40kHz AM envelope of the RF signal. The filter pole frequency should thus be positioned somewhere between 50kHz and 50MHz in order to exhibit a fast tracking of the

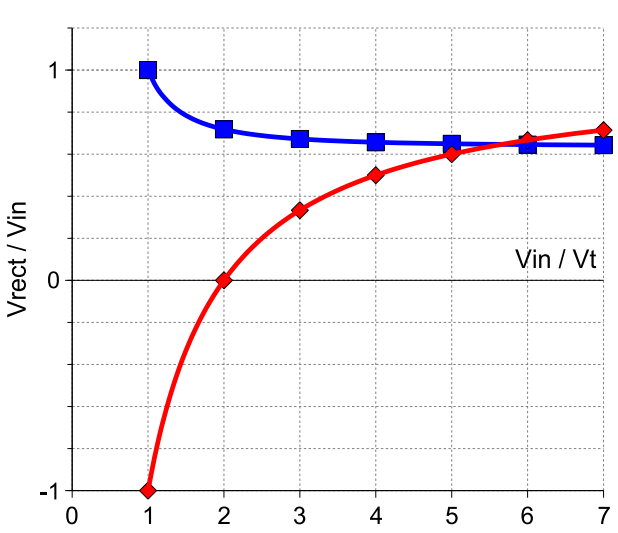

Figure 3.6: Comparison between full-wave (♦) and proposed (■) rectifier output

amplitude modulation and a good rejection of the UHF ripple. While this frequency span could seem wide at first sight, it proves crucial to carefully consider the choice of the components size, because of three main factors:

1. The on-resistance of the bridge switches is dependent on the input voltage. As a matter of fact, the higher is the input voltage, the lower is the transistors on-resistance: considering the low-threshold MOS devices used in the bridge (in order to further decrease the activation minimum level), for input peak voltages ranging from V_T (around 0.3V) to the maximum $|V_{GS}|$ allowable on the devices (1.8V), the value of a MOS r_{ds} may exhibit variations of more than two orders of magnitude.

2. As explained more in detail in Section 3.4, the equivalent series impedance of the chip is partly influenced by the input resistors value: from the analysis reported in Section 2.4.1, the input peak voltage V_{IN} is enhanced for high R_{IN}, and it happens that the higher r_{sw}, the higher R_{IN}, potentially increasing the efficiency. Moreover, the capacitor should be big enough to exhibit a very low impedance in the UHF frequencies.

3. In the previous calculations, since the current flow is estimated to be a few μA, the ohmic losses on the MOS's r_{ds} have been utterly neglected. However, excessively increasing the transistors on-resistance might cause a considerable voltage drop across the switches, able to overwhelm the advantages of the previous point.

According to such considerations, the optimum sizing of the components can be determined: the input transistors have been chosen to be 2/0.24μm (for the NMOS's) and 6/0.24μm (for the PMOS's), while the capacitor value is 2pF, implemented with an NMOS.

3.2 Voltage multiplier

3.2.1 Charge pump

The output level of the bridge described in the previous section is usually too low to establish a supply voltage sufficient to bias the core circuitry, especially when the reading distance rises above some meters.

Another rectification stage able to increase the DC supply voltage has to be introduced; among the different architectures available to perform such a task, a common Dickson charge pump [20] can be considered a good solution in terms of efficiency and area occupation. In order to keep the simmetry of the load on the two input pins, a pseudo-differential structure can be considered. A three-stages standard Dickson charge-pump is shown in Fig. 3.7.

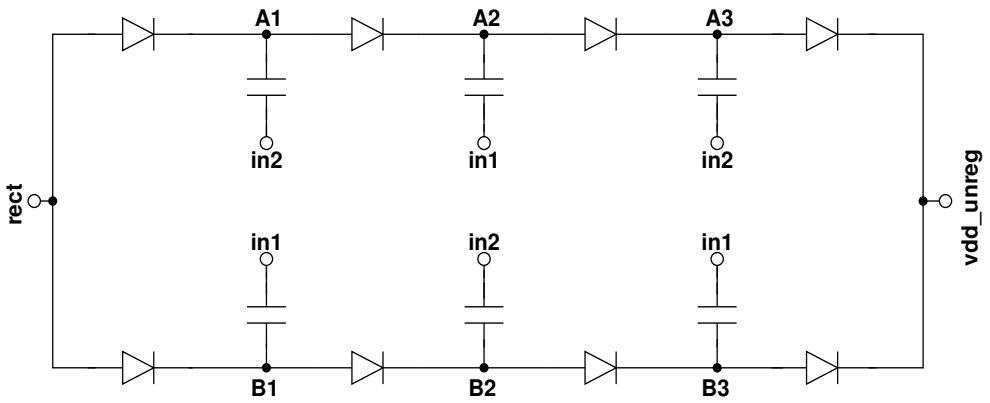

Figure 3.7: Schematic of a 3-stages pseudo-differential Dickson voltage multiplier

As mentioned before, Schottky diodes are not available in the chosen technology. In order to reduce the voltage drop across the diodes, they can be implemented with diode-connected low-threshold MOS transistors; the efficiency of this solution is limited mainly by the body effect on the devices and by their parasitic capacitance towards the substrate.

Moreover, other techniques can be employed to enhance the rectification efficiency.

Looking at the 3-stages Dickson charge pump of Fig. 3.7, in the half input period where in_2 is low the first diode is on and A_1 is set to $V_{RECT} - V_T$, while in the successive half period A_1 rises with in_2 and the diode is turned off. Therefore, the diode represents a device that stops the current flow when in_2 is high and conducts when in_2 is low; dually, it can be seen as a switch open if in_1 is low and closed (with a threshold loss) if in_1 is high. Given the fact that, according to (3.7), V_{RECT} is generally lower than the input peak voltage V_{IN}, it is also true that in_1 and in_2 exhibit a peak potential higher than $rect$. If the difference between these potentials was high enough to turn on

a transistor, the first diode could be substituted with a device, that, acting as a switch driven by the input potential, performs the same task without losing the threshold voltage V_T. Fortunately, the employed technology provides native zero-threshold NMOS transistors (ZVT), which exhibit a V_{TH} slightly positive or negative (according to the process corner) but quite close to zero. Such a device can successfully be employed for the task, allowing to gain a V_T in the rectification process: two ZVT NMOS's are put in place of the first couple of diodes, one driven by in_1 (between $rect$ and A_1) and another driven by in_2 (between $rect$ and B_1). The transistors size is determined balancing two constraints: they have to be large enough to neglect the voltage drop due to their on-resistance, without adding too much capacitance to the inputs.

A second technique to improve the efficiency is the substitution of the last diodes with a cross-coupled PMOS peak detector similar to the one used in the bridge of Section 3.1.2. Since the output capacitor connected to the bridge is huge ($\simeq$1nF), in this case there is no need to have a large switch on-resistance to filter the ripple, hence the transistors are far more performant than the ones of the input bridge.

The modified version of the charge pump is reported in Fig. 3.8.

3.2.2 Output capacitor

It is mandatory for the correct behavior of the chip to introduce an energy storage capacitor, able to keep the supply voltage high enough to empower all the circuits in the time intervals where the rectification network does not provide the necessary power to the load. This happens during the reading phase when a logic 0 is detected and the amplitude modulation depth approaches 100%, and during the backscatter answering phase where a "high reflectivity" state may lead to the absence of any noticeable input power.

Therefore, a big capacitor has to be placed at the output of the charge pump. It should guarantee a low drop-out during a low-input-power time slot, whose maximum length, according to the standard

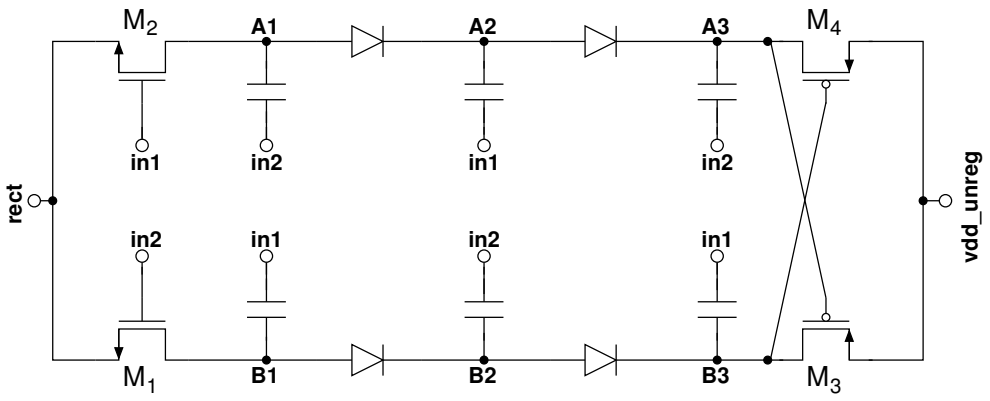

Figure 3.8: Schematic of the adopted voltage multiplier

and thanks to the Manchester coding of the transmitted bits, is 25μs; meanwhile, its value should not be too high, not only for area occupation reasons, but also because it should be completely charged within the 400μs time slot allocated for the chip powering up.

According to such considerations, the chosen size of the capacitor is 1nF. It is straightforward that such a value can be obtained on-chip only by using a MOS device: this does not pose any critical issue, since there is no need for linearity. The transistor size is 4000x32um, and, as reported in Section 5.2, it occupies more than 80% of the area of the analog section (although it is comparable to the size of the digital core).

3.3 Device safety protections

There are two kinds of electrical events that, despite having different origin, may lead to the physical damage of the chip: an electrostatic discharge and an excessive potential difference between two transistor terminals. It is mandatory to adopt the most effective countermea-

sures to prevent both of them from impairing the chip functionality. The thus introduced protection circuits, however, should impact as less as possible the behavior of the transponder during its normal working conditions.

3.3.1 Electrostatic Discharge (ESD)

This phenomenon is due to the electrostatic charge that may accumulate on the chip surface and on other insulators in proximity of the die, especially during handling and bonding in the tag manufacturing phase. A fast accumulation of such a charge could produce a strong voltage unbalance (even many thousands volts) between two terminals of the chip, inducing the breakdown of the devices connected to the pads. A safety low-resistive path should thus be included, enabling a current flow to reduce the potential difference to permitted levels during the rapid discharge.

The RFID chip has only two input/output pads, therefore the protection circuit scope is reduced with respect to the usual dies (where a whole padring has to be considered). In order to avoid a damage in the devices directly connected to them, especially the bridge ones, a circuit providing the low-resistive discharge path and a sensing net has to be placed between the terminals; however, this position is also the most critical, given its impact on the rectification efficiency and input impedance. Therefore, special attention must be paid in the design of this circuit.

The usual way to create the discharge path is placing one or more diodes in series between the terminals in both directions: an input voltage high enough to turn them on would be clamped while a great amount of current would be allowed to flow through them. This approach, given the application, has two main drawbacks:

1. The high parasitic capacitance introduced at the inputs. This is not desirable since, as explained in Section 3.4, a capacitance between the two input pads, while not directly affecting the input

peak voltage, causes a heavy reduction of the resistive part of the input impedance, generating thus difficulties in the design of the antenna. Since the current flow to bear during the ESD event is massive, the diodes — and their parasitic capacitance — must be quite large.

2. The suppression of the amplitude modulation. This is the most unwanted effect: during the standard functionality, if the input peak voltage was high enough to turn on the diodes, any amplitude modulation occurring above their collective threshold would be almost cancelled. This would mean the impossibility to decode the reader requests when the reading distance is low (so the available power is high).

In order to overcome these issues, another solution has been employed, depicted in Fig. 3.9: in its simplest version, the circuit is composed only of the part on the right of the dashed line, with the A terminal shorted to gnd.

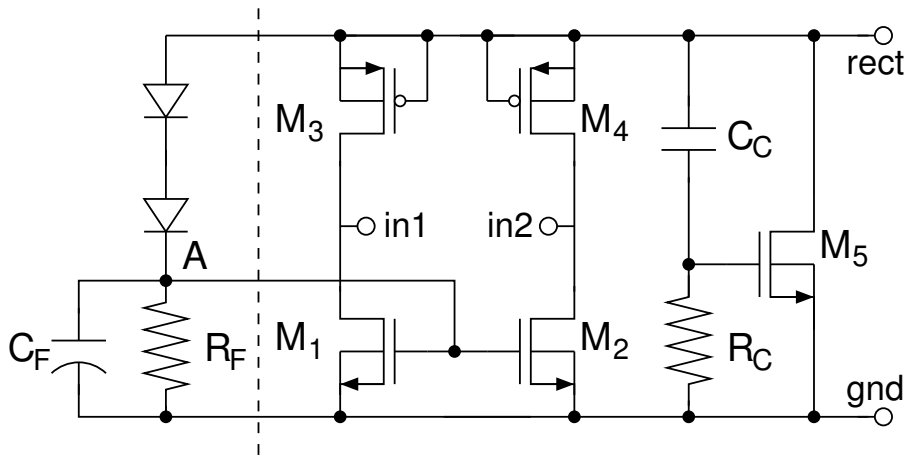

Figure 3.9: Schematic of the input protection circuit

When an ESD event occurs, the input voltage $|in_1 - in_2|$ tends to rise abruptly. The RC filter of the input bridge (Section 3.1) is generally not fast enough to notice this peak; however, the diode-connected transistors $M_1 ... M_4$ allow $rect$ and gnd to track promptly such a variation. The rising front is then reported by C_C to the gate of M_5, which in turns starts to conduct: the higher the peak, the higher the current shunted by M_5. A current flow is thus established through a low-resistive path, which, according to the polarity of the ESD peak voltage, is formed either by M_1-M_5-M_4 or M_2-M_5-M_3. Once exhausted the ESD event, M_5 is turned off by R_C.

The input capacitance of this circuit is the one of the four diode-connected MOS transistors drains, significantly lower than their gates one. Moreover, if the high-pass $R_C C_C$ filter is correctly sized, the AM modulation of $rect$ has a negligible effect on the gate of M_5, leaving the protection in off-state and preventing any information loss.

3.3.2 Input Overvoltage

The ESD event is a fast, single-shot phenomenon that generally does not happen during the normal operations of the chip. It is however not the only situation where, without adopting particular cares, some devices could experience a breakdown due to an excessive voltage difference. This can easily happen if the tag gets too close to the interrogator.

As a matter of fact, the adopted 0.18μm technology allows a maximum voltage difference of 1.8V between any terminal of a MOS transistor. From (2.6) and (2.8), the input peak voltage V_{IN} may reach this level with a reader-tag distance of 1.2m: getting closer to the interrogator could cause the breakdown of the rectifier transistors.

Hence, the circuit in the left part of Fig. 3.9 has been developed, introducing a slight modification of the ESD protection circuit. An estimation of the input peak voltage is made by sensing $rect$: if it is lower than the two diodes composite threshold, the protection is not activated and does not affect the main circuit behavior.

In the case that $rect$ is high enough to turn on the two diodes, the potential of the A node follows it and rises above gnd, bringing M_1 and M_2 into a more conductive state, and turning them on if the input peak voltage exceeds a safety level. The low-impedance path formed between the input pads by M_1 and M_2 degrades the power matching of the input network, forcing thus the input voltage to decrease and to set to a safe potential: this feedback mechanism allows to reduce the minimum reading distance to 30cm, although it should be noticed that such a short distance makes the far field approximation used in (2.6) no more effective. Also in this case, a $R_F C_F$ filter is needed in order to prevent the amplitude modulation suppression.

Finally, it is worth highlighting that the circuit does not increase the capacitive load at the inputs, since it reuses the devices already present in the ESD protection; the latter becomes in addition more effective, because an electrostatic discharge event would turn the overvoltage sensing circuit on and thus add an extra M_1-M_2 discharging path.

3.3.3 Charge Pump Overvoltage

Preventing the input peak voltage to get higher than the safety level is not sufficient to grant that the latter is not exceeded in other points of the rectification circuitry, especially in the voltage multiplier where the DC level reaches its maximum. Given the charge pump architecture, the control can be done at the end of the stage, remembering that the uttermost voltage that can be experienced in the circuit is two diode thresholds higher (on A_1 and B_1 in Fig. 3.8).

Differently from the input stage case, there is no information at this point of the circuit associated to the amplitude modulation to be recorded; furthermore, the parasitic capacitance introduced does not represent a problem, since it is in parallel with the loading 1nF capacitor. There are thus no disadvantages in the use of clamping diodes to limit the output voltage.

3.4 Tag equivalent model

Given the peculiar bridge-hybrid charge pump employed architecture, it is not possible to resort to already reported solutions for the estimation of the RC equivalent model [21] [22], and a new one must be extrapolated.

Since the final product will not be shipped in a package but directly soldered to the antenna with the chip-on-board methodology, no parasitics associated to the package have to be taken into account: only the resistance and inductance of the bonding wires can play a role in the estimation of the model. However, since they are in series with the RC equivalent of the die, they can be simply summed to the final result, and may be neglected in the calculation of the proper RC net.

A first step consists in separating the contribution given by the capacitance directly connected between the inputs, like the one of the bridge transistors or the ESD protection diodes, from the equivalent RC series of the rest of the circuit. Referring to Fig. 3.10, it is simple to estimate the input impedance of such a network:

$$Z_{IN} = \frac{\frac{1}{sC_i}\left(R_R + \frac{1}{sC_R}\right)}{\frac{1}{sC_i} + R_R + \frac{1}{sC_R}} = \frac{1}{s(C_i + C_R)} \frac{1 + sR_RC_R}{1 + sR_R(C_R \parallel C_i)} \tag{3.8}$$

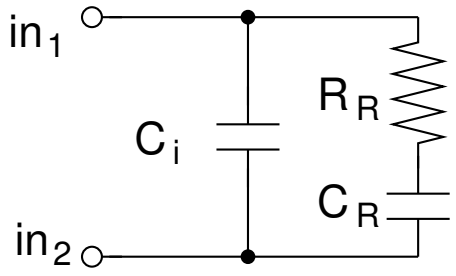

Figure 3.10: Capacitor between the inputs

Separating the real and the imaginary part in (3.8) leads to the following expressions:

$$R_{IN} = \frac{R_R C_R^2}{(C_i + C_R)^2} \frac{1}{1 + \omega^2 R_R^2 (C_R \parallel C_i)^2} \tag{3.9}$$

$$X_{IN} = -\frac{1}{\omega(C_i + C_R)} \frac{1 + \omega^2 R_R^2 (C_R \parallel C_i) C_R}{1 + \omega^2 R_R^2 (C_R \parallel C_i)^2} \tag{3.10}$$

These equations can be noticeably simplified assuming that

$$R_R^2 C_R^2 \omega^2 \ll 1 \tag{3.11}$$

This assumption holds supposing that the sizing of the components leads to a good minimization of the equivalent resistor and capacitor, as requested in Section 2.4.2.

The input impedance becomes thus

$$Z_{IN} = \frac{R_R C_R^2}{(C_i + C_R)^2} - j \frac{1}{\omega(C_i + C_R)} \tag{3.12}$$

or, for the matching purposes explained in Section 2.4.1,

$$R_{IN} \simeq \frac{R_R C_R^2}{(C_i + C_R)^2} \tag{3.13}$$

$$C_{IN} \simeq C_i + C_R \tag{3.14}$$

It is worth noticing that under matching conditions the input peak voltage does not depend on C_i. In fact, combining (2.8), (3.13) and (3.14),

$$V_{IN} = \sqrt{2 \frac{P_{AV}}{R_{IN}}} \frac{1}{\omega C_{IN}} = \sqrt{2 \frac{P_{AV}}{R_R}} \frac{1}{\omega C_R} \tag{3.15}$$

Although the last equation shows that C_i does not influence V_{IN}, it is anyway good practice to keep its value relatively low, since the equivalent resistance decreases rapidly with it, and the feasibility of high quality factor antennas with small resistance becomes very critical.

For the calculation of R_R and C_R, a model of the entire rectification network has been developed. Given the circuit and the input waveform simmetries, the estimation of the impedance seen at the input terminals may be equivalently done in the case that $v_{in}(t) < 0$ or $v_{in}(t) > 0$: the latter situation has been used in the following analysis, i.e. $in_1 > in_2$. Particularly, the input voltage is assumed to be high enough to turn the circuit devices on, so $v_{in}(t) > V_T$. In this case, the equivalent circuit of the power harvesting network becomes the one shown in Fig. 3.11.

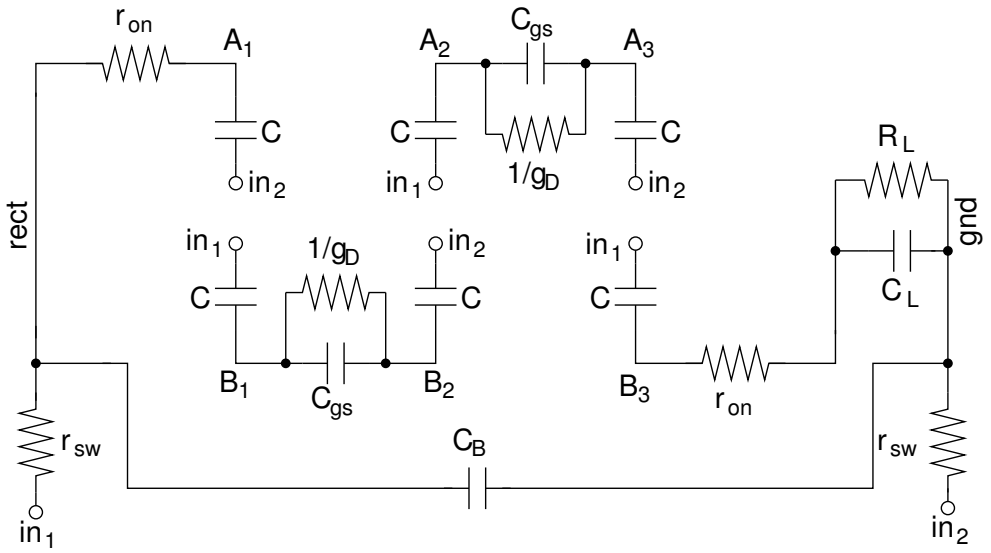

Figure 3.11: Equivalent model of the whole RF/DC converter when $in_1 > in_2$)

For the sake of simplicity, the capacitors related to the off-state devices have been neglected. Simulations show that this approximation leads to less than a 5% error in the estimation of the equivalent impedance. The diodes have been substituted with a RC parallel model, where c_{gs} is the gate-source capacitance of the associated transistor and g_D represents the diode conductance. While c_{gs} is quite independent of the V_{GS} once the MOS is turned on, g_D varies with the current flowing through the device, or, during the transient, with the input level. An average value can be considered, knowing approximatively the input peak voltage in matching conditions. The same considerations can be done on the bridge transistors, represented by their equivalent on-resistance r_{sw} (or conductance g_{sw}).

Many simplifications can be done on the circuit shown in Fig. 3.11. Given the operating frequencies, the 1nF capacitor C_L can be considered a short circuit, allowing therefore to ignore the equivalent resistor representing the load R_L. Moreover, also C_B (the capacitor at the bridge output) is assumed to be well represented by a short circuit in the UHF band: this assumption is less accurate than the previous one, but the error it originates can be estimated in a small percent. Finally, the on-resistance of the switches in the charge pump (both the ZVT NMOS at the beginning and the PMOS at the end) can be considered low enough to be neglected.

After these simplifications, the equivalent circuit can be redrawn as in Fig. 3.12.

The admittance of the whole circuit is

$$Y_R = \frac{g_{sw} + sC}{2} + 2\frac{SCg_D + s^2Cc_{gs}}{2g_D + s(C + 2c_{gs})} \tag{3.16}$$

leading to the impedance

$$Z_R = \frac{4g_D + 2s(C + 2c_{gs})}{2g_d g_{sw} + s[(C + 2c_{gs})g_{sw} + 6g_D C] + s^2 C(C + 6c_{gs})} \tag{3.17}$$

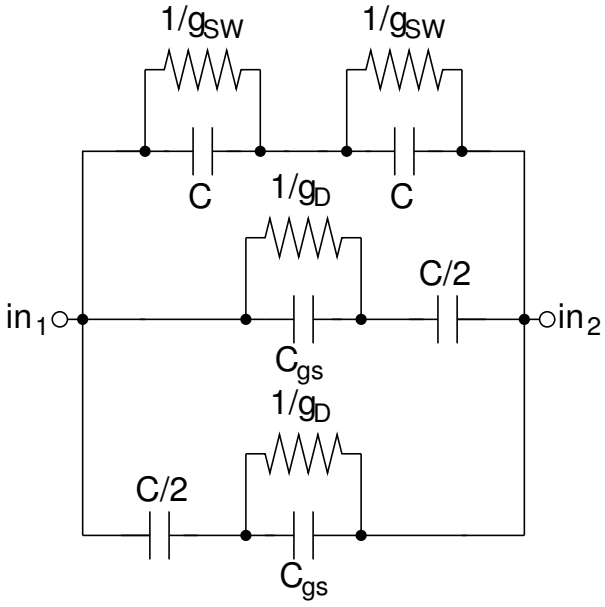

Figure 3.12: Simplified rectification model

The equivalent resistor and capacitor are therefore

$$R_R = \frac{8g_D^2 g_{sw} - 12\omega^2 g_D C c_{gs} + 8\omega^2 g_D C^2 + 2\omega^2 (C + c_{gs})^2 g_{sw}}{[2g_d g_{sw} - \omega^2 C(C + 6c_{gs})]^2 + \omega^2 [(C + 2c_{gs})g_{sw} + 6g_D C]^2} \quad (3.18)$$

$$C_R = \frac{[2g_d g_{sw} - \omega^2 C(C + 6c_{gs})]^2 + \omega^2 [(C + 2c_{gs})g_{sw} + 6g_D C]^2}{\omega^2 C[24g_D^2 + 2\omega^2 (C + 6c_{gs})(C + 2c_{gs})]} \quad (3.19)$$

A more general analysis can be done considering a generic N-stages pseudo-differential charge pump: a pedestrian modification to the circuits of Fig. 3.8 and Fig. 3.11 shows that the equivalent simplified network is made up of the double $r_{sw}C$ structure (the highest branch of Fig. 3.12) and $N - 1$ branches in parallel like the ones in the lower part of Fig. 3.12, where there are 2 branches for a 3-stages charge

pump. This more generic structure leads to an equivalent resistor and capacitor described as

$$R_R = \frac{8g_D^2 g_{sw} - 4N\omega^2 g_D C c_{gs} + 4(N-1)\omega^2 g_D C^2 + 2\omega^2 (C + c_{gs})^2 g_{sw}}{[2g_d g_{sw} - \omega^2 C(C + 2Nc_{gs})]^2 + \omega^2 [(C + 2c_{gs})g_{sw} + 2Ng_D C]^2} \quad (3.20)$$

$$C_R = \frac{[2g_d g_{sw} - \omega^2 C(C + 2Nc_{gs})]^2 + \omega^2 [(C + 2c_{gs})g_{sw} + 2Ng_D C]^2}{\omega^2 C[8Ng_D^2 + 2\omega^2 (C + 2Nc_{gs})(C + 2c_{gs})]} \quad (3.21)$$

From such a model, the expected input impedance of the chip, calculated at 869.5MHz with an input available power of -16dBm (the matching has to be done with the lowest input powers, affecting g_D and g_{sw}, in order to achieve the maximum reading range), is 32-j472Ω, corresponding to a resistance of 32Ω and a capacitor of 388fF. Simulations confirm a good accuracy of the model, since the value found both with SpectreRF™ and ADS™ is 35-j512Ω.

3.5 DC voltage and rectification efficiency

The reading range of the tag, once known the output current requested by the digital core and the analog circuits described in Section 3.6 and Chapter 4, is determined by the minimum power that allows the rectification circuit to provide such a current with the minimum supply voltage compatible with the proper tag functionality.

In the present application, the digital core has been developed in a successive phase. Hence, initially a first worst-case assumption on its average current consumption has been made, estimating the loading current to be I_{DIG}=5μA. Under this condition, and knowing that the regulation system of Section 3.6 exhibits a correct functionality if $vdd_unreg > 0.8$V (worst-case scenario), the minimum input power required to grant the DC output level to be high enough is $\simeq$-16dBm (assuming to have a good impedance matching). A simulation of the voltage multiplier output is shown in Fig. 3.13: it should be noticed that

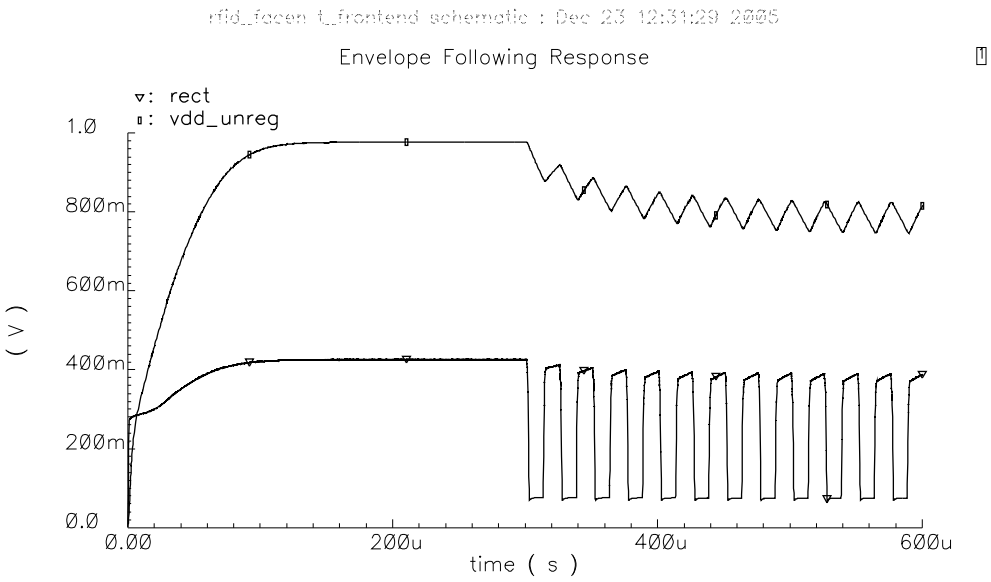

Figure 3.13: Simulation of the charge pump output @ r=5m, 0dB-gain antenna, with I_{DIG}=5μA

in this worst-case analysis, besides I_{DIG} and the analog circuits current (estimated in the most power-hungry process corner), the simulation takes into account also the effect of a 100% AM modulation of the input signal (better shown by the first bridge output voltage). The reading distance r associated to the abovementioned available power is approximately 5 meters (assuming to connect the chip to a unity-gain matched antenna).

The main parameter employed to estimate the goodness of the power harvesting circuit is the rectification efficiency η. The most common definition of such a figure of merit is the ratio between the power delivered to the load and the power present at the input of the circuit. In the present application, however, the latter is dependent also on the matching between antenna and chip, whose impedance

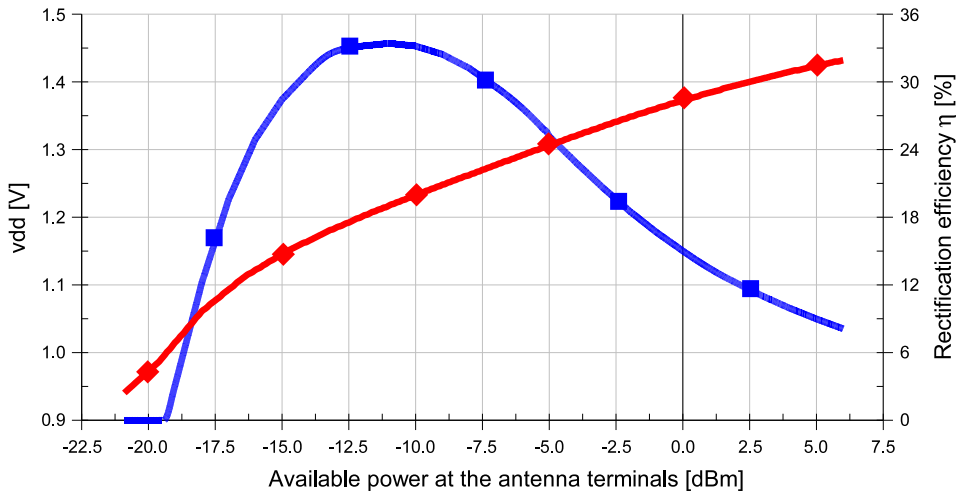

Figure 3.14: Rectification efficiency @ vdd_unreg=1V (■) and output voltage with no loading current (♦) vs. input power

varies according to the reading distance. It is therefore more useful to define the efficiency as the ratio between the average DC output power of the RF/DC converter and the *available* power at the input (i.e. the power that would be delivered to the chip in perfect matching conditions for a fixed antenna): the impedance mismatch impacts this parameter, better reflecting the variations with the reader-tag distance.

$$\eta = \frac{P_{out}}{P_{AV}} \tag{3.22}$$

Fig. 3.14 shows the efficiency of the circuit assuming a fixed output voltage of 1V, and the charge pump output level with no loading current vs. the available input power. It can be noticed that in proximity of P_{AV}=-12dBm η exhibits a peak and then starts to decrease, as well as the derivative of the output voltage: this is mainly due to the

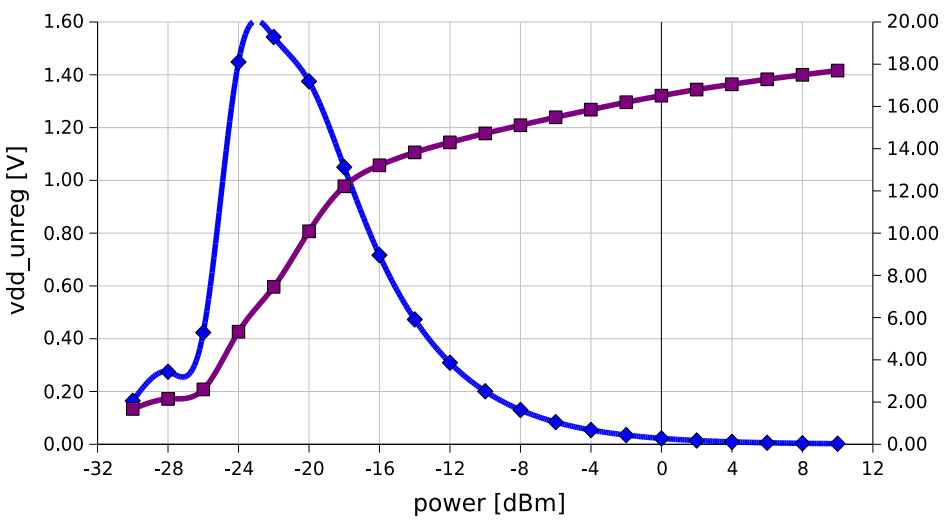

Figure 3.15: Rectification efficiency (♦) and output voltage (■) vs. input power @ I_{DIG}=1μA

overvoltage protections described in Sections 3.3.2 and 3.3.3, which deliberately force an impedance mismatch at the antenna terminals and thus the loss of part of the available input power (that in such conditions far exceeds the circuit requirements).

As a matter of fact, the average power consumption of the digital core has been deeply overestimated: once designed, it has been found that such a section draws an average current of about 1μA. Fig. 3.15 shows both the rectification efficiency and the output voltage of the RF/DC converter in the worst-case operating conditions (fast transistors model and high temperature), with the actual average current load requested by the digital section. The abovementioned considerations about the efficiency loss due to the safety protections can be made also in this case. Assuming 0.8V to be the minimum output voltage threshold necessary for the correct circuit functionality, the

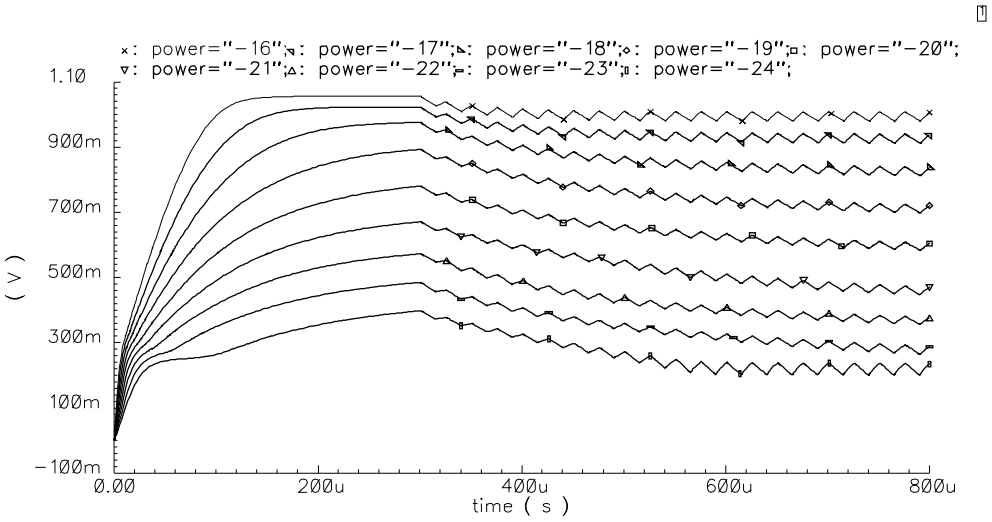

Figure 3.16: OOK modulation effect on vdd_unreg with $P_{AV} = -24 \div -16$dBm

minimum input power required by the tag is estimated to be -20dBm, meaning approximately a reading range of 8 meters under the usual conditions (500mW ERP reader, unity-gain antenna).

Actually, such a result does not take into account the input power reduction due to the modulation effect (coming either from the reader AM or the tag backscattering): Fig. 3.16 shows the unregulated voltage behavior with a 100% AM modulation (that is, On-Off Keying) in low-power conditions, and, assuming the same 0.8V voltage threshold for the circuit functionality, it can be noticed that the minimum required input power increases to something less than -18.5dBm, i.e. a reading range of $\simeq$6.7 meters. Such a distance is comparable to, or higher than, the ones reached by the cited works, and thus the designed tag, given the lower cost due to the cheap technology and architectural choices, can be a fierce competitor in the passive UHF RFID market.

3.6 Voltage Regulation

The supply voltage present on the 1nF capacitor has a strong dependency on the reading distance, as mentioned in the previous sections; moreover, it is affected also by the amplitude modulation of the input voltage. Feeding the digital core with this supply level is possible and does not impact the tag functionality, since the higher current request of the gates due to a higher supply would happen only in conditions of an available power greater than the minimum one. Nonetheless, it is useful to proceed with a custom design of the digital cells in order to achieve the maximum power savings [23], and this is better accomplished with a fixed power supply. Furthermore, the tag requires a clock reference: due to cost, area and power optimization reasons better explained in Section 4.3, such a task is performed in the proposed tag by a ring oscillator, whose frequency is strictly dependent on the supply level. Hence the need for a stable and distance-independent power supply voltage, obtained from vdd_unreg by means of a regulator based on a voltage reference.

3.6.1 Voltage reference

Many CMOS circuits have been proposed in the past years providing a temperature- and supply-independent voltage reference, based either on the well-known current-mode bandgap-like structures [24] [25] or on the MOS threshold properties [26]. They are, however, not suitable to be employed in ultra-low power and very-low voltage conditions like the ones experienced in a UHF RFID tag. Indeed, the former architecture exhibits great stability and precision, but can be employed only if the supply voltage is higher than 0.9V. Moreover, its current consumption is quite large, given the presence of one or more op-amps and startup circuits. The latter tipology is more suitable to be used in such an application; nonetheless, the reported solutions, while being quite accurate, still feature an unacceptable current consumption and the need for a supply voltage higher than 1V.

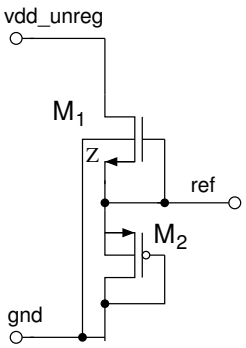

Figure 3.17: Schematic of the voltage reference

A new voltage reference is proposed, made up only of 2 MOS transistors: its schematic is shown in Fig. 3.17. By carefully sizing the devices, an ultra-low power reference can be obtained, featuring an acceptable rejection of temperature and supply variations.

M_1 is a native zero-voltage threshold (ZVT) NMOS. It exhibits a threshold voltage ranging from a negative (-100mV) to a slightly positive threshold V_{T-Z} over the process and temperature corners (neglecting the MOS body effect): in the nominal case, it is around 0V. Therefore, when it is biased with a zero gate-source voltage it typically works in the strong inversion region (or a moderately weak inversion if the threshold is positive). On the condition that the transistor length is high enough to neglect the channel modulation effect, the drain current of M_1 can be described with the well-known MOS square law:

$$I_{REF} = \mu_Z(T)\frac{C_{ox}}{2}\left(\frac{W}{L}\right)_1 V_{T-Z}^2(T) \tag{3.23}$$

where C_{ox} is the oxide specific capacitance of the device, and μ_Z is the carrier mobility, which, along with V_{T-Z}, exhibits a temperature dependency:

$$\mu_Z(T) = \mu_Z(T_0)\left(\frac{T}{T_0}\right)^{\eta_{\mu Z}} \quad (3.24)$$

$$V_{T-Z}(T) = V_{T-Z}(T_0) + \alpha_{V_{TZ}}(T - T_0) \quad (3.25)$$

T_0 is the ambient temperature, while, for the ZVT transistor in the 0.18μm technology adopted for this design, $\alpha_{V_T} = \alpha_{V_{TZ}}$ =-0.9μV/K and $\eta_\mu = \eta_{\mu Z}$ =-0.85. On the basis of these relationships, equation (3.23) can be rewritten as following:

$$\begin{aligned} I_{REF} &= \mu_Z(T_0)\frac{C_{ox}}{2}\left(\frac{W}{L}\right)_1 [V_{T-Z}(T_0) + \alpha_{V_{TZ}}(T - T_0)]^2 \left(\frac{T}{T_0}\right)^{\eta_{\mu Z}} \\ &= K_{M1}(0)\left(\beta_1 T^{\eta_{\mu Z}} + \beta_2 T^{\eta_{\mu Z}+1} + \beta_3 T^{\eta_{\mu Z}+2}\right) \end{aligned} \quad (3.26)$$

where

$$\beta_1 = \frac{[V_{T-Z}(T_0) + \alpha_{V_{TZ}} T_0]^2}{T_0^{\eta_{\mu Z}}} \quad (3.27)$$

$$\beta_2 = \frac{\left[2\,\alpha_{V_{TZ}} V_{T-Z}(T_0) - 2\,\alpha_{V_{TZ}}^2 T_0\right]}{T_0^{\eta_{\mu Z}}} \quad (3.28)$$

$$\beta_3 = \frac{\alpha_{V_{TZ}^2}}{T_0^{\eta_{\mu Z}}} \quad (3.29)$$

$$K_{M1}(0) = \frac{\mu_Z(T_0)\, C_{ox}}{2}\left(\frac{W}{L}\right)_1 \quad (3.30)$$

As a matter of fact, the term of the sum in (3.26) associated with β_1 for the chosen device type is negligible, while the ones referring to β_2 and β_3 exhibit, respectively, a quite small and a fairly positive temperature coefficient. Therefore, a long-channel gated ZVT device can be represented as a current source with a positive temperature coefficient.

The voltage reference is obtained by making the current provided by M_1 flow through a diode-connected PMOS M_2. Assuming also for

the latter the long-channel condition, its source-gate voltage can be expressed with the MOS square law:

$$V_{REF} = -V_{T-P}(T) + \sqrt{\frac{2\,I_{REF}(T)}{\mu_P(T)C_{ox}\left(\frac{W}{L}\right)_2}} \quad (3.31)$$

$$= -V_{T-P}\left(T_0\right) + \alpha_{V_{TP}}\left(T - T_0\right) + \sqrt{\frac{2\,I_{REF}(T)}{K_{M2}(0)\,\left(\frac{T}{T_0}\right)^{\eta_{\mu P}}}} \quad (3.32)$$

where V_{T-P}, $\alpha_{V_{TP}}$, $K_{M2}(0)$ and $\eta_{\mu P}$ correspond to V_{T-Z}, $\alpha_{V_{TZ}}$, $K_{M1}(0)$ and $\eta_{\mu Z}$ in (3.24), (3.25), (3.30) evaluated for the PMOS device M_2 in Fig. 3.17.

Using (3.26) in the previous equation and neglecting its β_1 contribution, the following relationship for the reference voltage is found:

$$V_{REF} \simeq -V_{T-P}\left(T_0\right) + \alpha_{V_{TP}}\left(T - T_0\right) + \\ + \sqrt{X\,T_0^{\eta_{\mu P}}}\left(\sqrt{\beta_2 T^{\Delta_\eta+1}} + \sqrt{\beta_3 T^{\Delta_\eta+2}}\right) \quad (3.33)$$

where

$$X = \frac{K_{M1}(0)}{K_{M2}(0)} \quad (3.34)$$

$$\Delta_\eta = \eta_{\mu Z} - \eta_{\mu P} \quad (3.35)$$

The NMOS to PMOS W/L ratio that grants the lowest temperature dependency of the reference voltage can be found by setting to zero the derivative of the V_{REF} expression in (3.33) with respect to the temperature at T_0. The resulting optimum ratio is

$$X_{opt} = \frac{1}{T_0^{\eta_{\mu P}}}\left[\frac{2\alpha_{V_{TP}}}{(\Delta_\eta+1)\sqrt{\beta_2 T_0^{\Delta_\eta-1}} + (\Delta_\eta+2)\sqrt{\beta_3 T_0^{\Delta_\eta}}}\right]^2 \quad (3.36)$$

Such a relationship sets a voltage reference with a good rejection of the temperature variations. In order to minimize also the dependency of V_{REF} on vdd_unreg, the simplest solution is to keep the transistors channel length very large, especially for M_1, in order to reduce the channel modulation effect. This technique, besides not introducing any extra current consumption, grants also the fulfillment of the long-channel device condition used before in the calculations.

The previous relationships leave a degree of freedom in the choice of the transistors size: this proves useful for power saving purposes. In fact, the current requested by the stage is I_{REF}, and from (3.23) it is evident that the lower is the W/L ratio of the ZVT NMOS, the lower is such a current. Chosen a target value, by adopting a very small channel width also the channel length L is determined, and from (3.36) the PMOS size is set consequently, possibly keeping the same channel length of M_1 in order to limit the mismatch effect.

Following these guidelines, the designed voltage reference has M_1 and M_2 sized, respectively, 0.5/18μm and 4/18μm. Fig. 3.18 shows a simulation of V_{REF} vs. the junction temperature: the curve maximum can be easily spotted, and the reference variation over the whole 0–85° temperature range is around 900μV (less than 0.16%). Moreover, as reported in the simulation in Fig. 3.19, the variation over the 0.8–1.8V supply span is 13.4mV, corresponding to a PSRR of ≃33dB. The typical DC current consumption of this stage is 160nA.

It should be noticed that, in comparison with the reported works and to the most common structures, the variability of the reference voltage is relatively high. Nonetheless, for the kind of application, the loss of precision is an affordable tradeoff with the power consumption.

Once designed the circuit according to the reported methodology, the reference voltage features a good rejection of temperature and supply variations: its spread through the PVT (Process, Voltage, Temperature) space is thus due mainly to the process tolerance. It is worth highlighting that there is a sort of intrinsic feedback mechanism in the reference schematic allowing to reduce the process variations on the ZVT NMOS parameters: in fact, the higher is the current set by

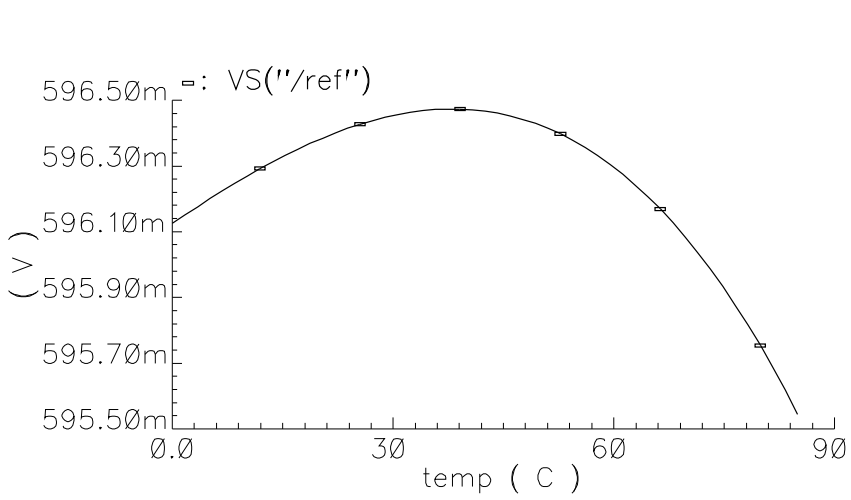

Figure 3.18: Reference voltage vs. temperature

M_1, the higher becomes also V_{REF}, increasing thus the body effect on the ZVT transistor threshold and reducing again I_{REF}.

Nonetheless, the variation of threshold, oxide capacitance and mobility of both transistors cause a quite wide span of V_{REF} throughout corners: Fig. 3.20 shows the results of 1000 MonteCarlo simulations, and it can be seen that the reference voltage ranges from 0.5 to 0.7V. Such a span may appear to be very large; however, it is worth pointing out that, given the wafer characteristics, the resulting reference voltage is minimally affected by the operating conditions (temperature and supply). Since the oscillator described in Section 4.3.2, that is the digital circuit with the highest sensitivity to the supply level, employs a self-calibration system which can overcome this variability, the spread of the voltage reference can be considered acceptable without significant functionality issues in the tag.

A summary of the reference electrical features is reported in Table 3.1.

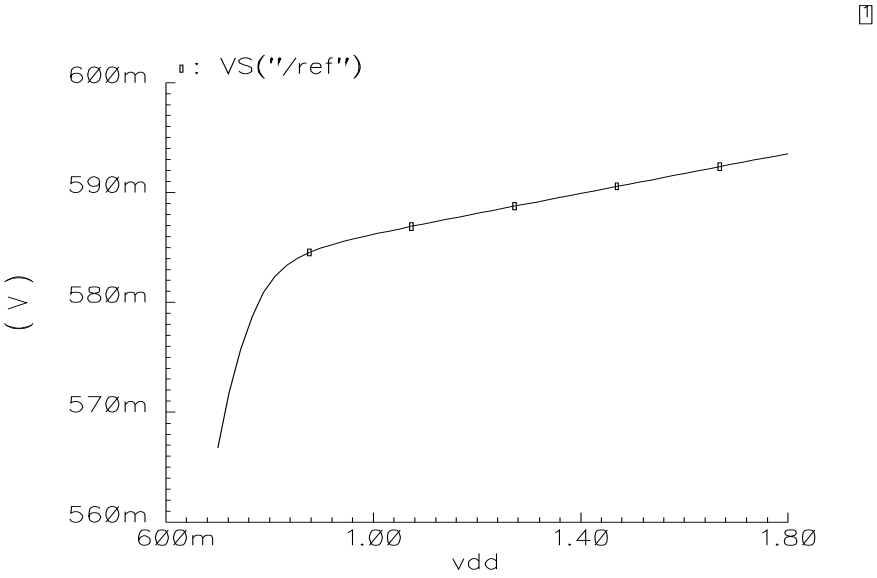

Figure 3.19: Reference voltage vs. unregulated supply

	Min	**Typ**	**Max**
V_{REF} [V]	0.493	0.590	0.682
ΔV_{REF}, T=0÷85° [mV]	0.02	0.97	12.1
DC PSRR, vdd_unreg=0.8÷2V [dB]	28	33	42
I_{REF} [nA]	40	157	397

Table 3.1: Voltage reference corners results summary

3.6.2 Low Drop-Out Regulator

A voltage regulator is needed to set the supply of the core devices to V_{REF}. It should feature a low drop-out in order to be used in low-power conditions and good power-line regulation, for a current load estimated to vary between few dozens nA and 10μA according to the

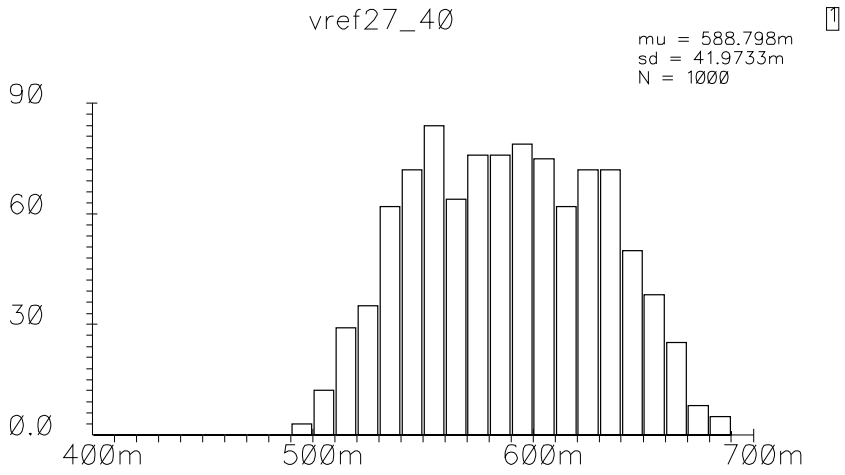

Figure 3.20: Voltage reference through Montecarlo process+mismatch simulations

digital core activity, and a small power consumption. The most suitable architecture for such a regulator is the series PMOS LDO, whose schematic is shown in Fig. 3.21.

The tail current is provided by a long-channel gated ZVT NMOS, as the one used in the circuit of Fig. 3.17. Indeed, this solution, while experiencing a certain lack of precision in the current value, proves less power-hungry than generating a current reference from V_{REF} by means of an op-amp, since a current source is needed in the tag only by the regulator and the demodulator of Section 4.2. The current consumption varies between 120 and 200nA according to the corner.

The circuit stability is achieved by adding the compensation capacitance C_C between the gate and the drain of M_S, and has been successfully simulated for loading currents ranging from 10nA to 10μA. The regulated voltage exhibits low dependency on such a load, as shown in Fig. 3.22: the variation of vdd_reg is around 1% in the mentioned 10nA-10μA (that is 3 orders of magnitude) current span.

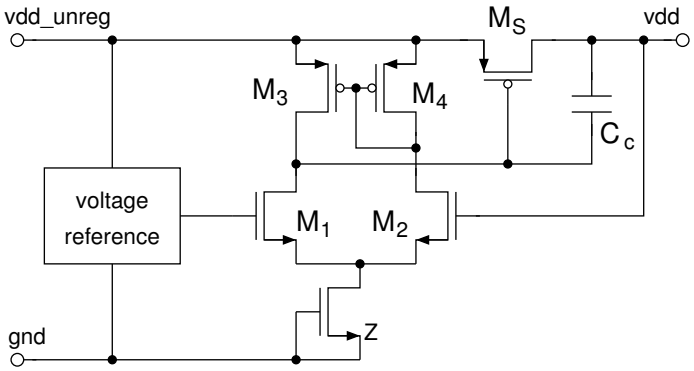

Figure 3.21: Schematic of the LDO

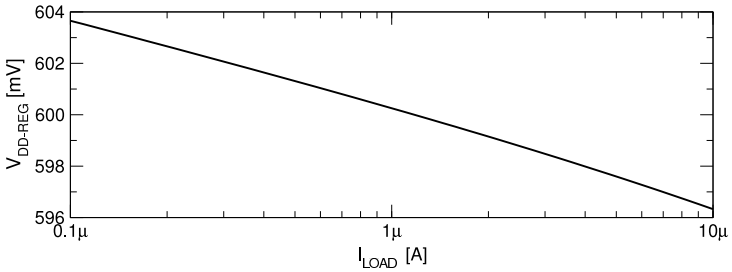

Figure 3.22: vdd_reg variation vs. loading current

Chapter 4

Analog/Digital Interface

The retrieval of the RF field energy is one of the most challenging issues in the design of an RFID passive tag, however it is not the only task that the analog frontend has to accomplish. In fact, it is mandatory to introduce an interface between the electromagnetic waves received by the antenna and the digital core of the circuit acting on CMOS levels. The modulated EM field transmitted from the reader has to be translated into logic states, and the tag answer coming from the digital section has to be used for the backscatter impedance modulation. Moreover, the core needs an initialization signal and a suitable clock reference to work correctly. The analog circuits depicted in this chapter provide the interface between the RF waveforms and the binary I/O data flow, as well as the control signals requested by the digital section of the tag.

4.1 Power-On Reset

The digital core of the transponder needs a signal to reset the registers at the beginning of the operations, in order to avoid the possibility of experiencing metastability in the flip-flops. The Power-On Reset signal (or shortly POR) is thus generated with the circuit shown in Fig. 4.1.

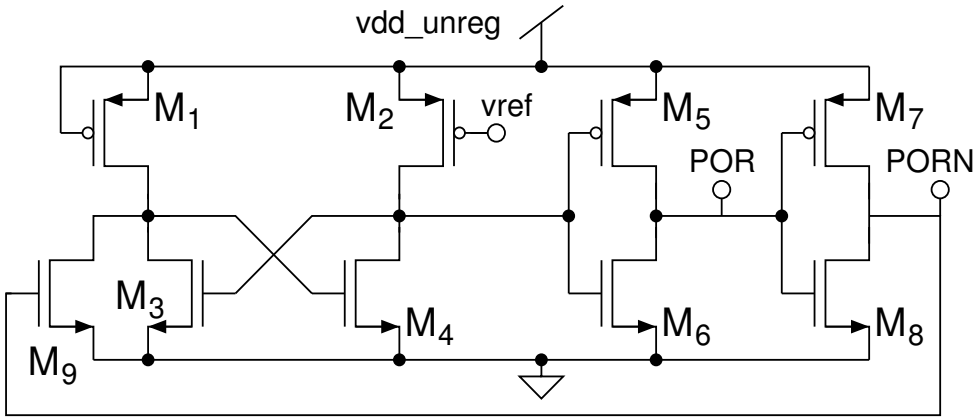

Figure 4.1: Power-On Reset circuit

The input pin $vref$ is connected to the voltage reference described in Section 3.6.

During the start-up phase, or more generally when the input available power is too low, the unregulated voltage supply is not sufficient to turn the reference diode-connected PMOS in Fig. 3.17 on. The ZVT transistor M1 in the same figure is in on-state because its threshold is always lower than zero, but, since there can be no current flow, it operates in triode region, shorting thus $vref$ to vdd_unreg. Only when the reference becomes higher than the PMOS threshold voltage $-V_{THp}$ a current flow is allowed in the circuit, and the value of $vdd\_unreg - vref$ becomes greater than zero (this explanation does not take into account subthreshold currents for the sake of simplicity; actually, the voltage difference starts to grow slightly before $vdd\_unreg = -V_{THp}$).

Transistors M_1 to M_4 in Fig. 4.1 are LVT. M_3 and M_4 are sized such in a way that their leakage current is higher than the PMOS couple one when all the four transistors are turned off: therefore, for a low value of $vdd\_unreg - vref$ the gates of the cross-coupled pair tend to be shorted to the ground potential, since M_1 is always off and

M_2 experiences a not sufficient V_{SG}. When the difference between the unregulated power supply and the voltage reference approaches the threshold voltage of M_2, the latter begins to draw current, and its drain terminal rises to vdd_unreg, indicating thus that there is enough energy to empower the chip. This value is then inverted to generate the POR signal. Transistor M_9 grants that V_{GS4} is definitely set to 0 not only because of the leakage current of M_3, so the current consumption of the circuit in a quiescent state is negligible.

Waveforms showing the behavior of the Power-On Reset circuit during the start-up phase are reported in Fig. 4.2. It should be noticed that the actual signal sent to the digital core is the inverted value $PORN$, which starts from "low" and turns "high" when the supply voltage reaches a sufficient value: this signal is a lot smoother than POR, and its level is well-defined during every phase of the transient.

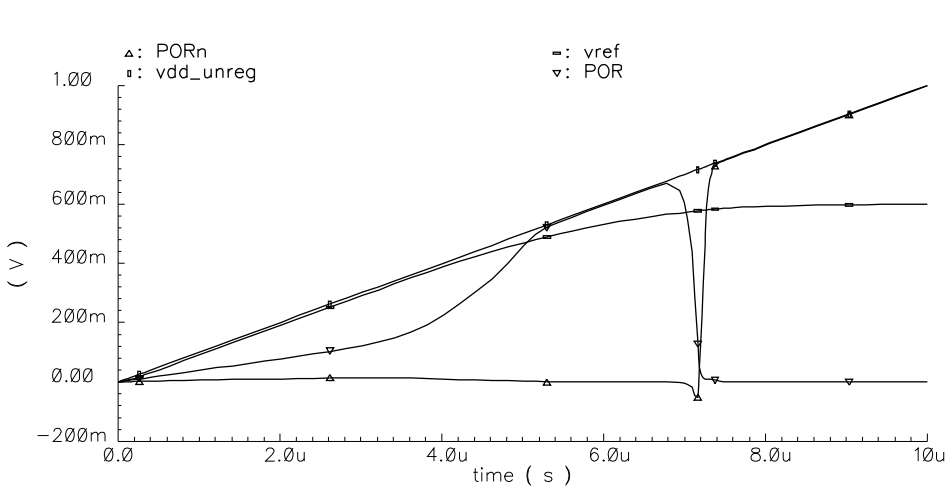

Figure 4.2: Power-On Reset waveforms

4.2 AM Demodulator

The actual AM demodulation of the signal is done by the first rectification stage, described in Section 3.1, loaded with the small filtering capacitor. In fact, the $r_{sw}C$ filter suppresses the UHF carrier, and its output $rect$ is the envelope of the AM signal, or, in other words, the data brought back into baseband. The decoding of the Manchester symbols is done by the digital core of the circuit, which operates on CMOS digital values (0 and vdd_reg). Therefore, it is mandatory to translate the AM signal envelope into CMOS levels: this operation is performed by the circuit shown in Fig. 4.3.

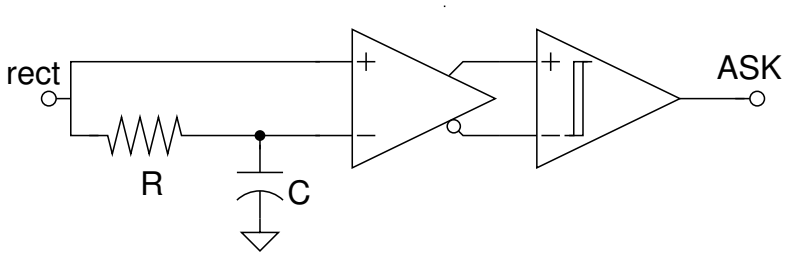

Figure 4.3: ASK demodulator to CMOS levels

4.2.1 Data preprocessing

The identification of the logic levels, especially in the case of low modulation depth where $rect$ presents an excursion of a few dozens mV, can be a tough task. A comparison between the $rect$ voltage and some known level should accomplish it, but, since the "high" or "low" potentials of the rectified signal depend on the distance between tag and reader, no fixed reference can be used. Furthermore, the 40kHz AM modulation with Manchester coding causes a maximum ASK signal frequency of 80kHz, and the AC-coupling of $rect$ to a known common-mode potential is not feasible (the capacitors would be huge).

Therefore, in order to provide a suitable input to the comparator to be evaluated against $rect$, the average level of the rectified voltage is retrieved by means of another RC low pass filter, which suppresses the modulation but is still able to track long-term variations that can occur in case of a change in the reader-tag distance.

There is no particular need for precision on the pole frequency of the filter, provided that it is lower than the ASK data-rate: the Manchester coding of the incoming data causes the average level of $rect$ to be constant, since every bit features an equal time interval of "low" and "high". For area constraints, it would be useful to keep the frequency not much lower than the 40kHz of the ASK modulation. Nonetheless, it is not possible to get too close to the data-rate: in fact, during the *preamble detect* time interval at the beginning of the operations used for the chip powering up, there is no AM modulation for few hundreds μs, and the output of the filter tends to collapse to $rect$. Then, during the *preamble* field, where 9 Manchester zeroes are transmitted, the filter output reaches its correct level. If the settling of the filter was too fast, the CMOS decoded bits of the preamble would exhibit an incorrect period due to the relatively slow rising/falling time of the ASK modulation (nominally 17% of the bit time): such an erroneous evaluation must be avoided, since the timing of the whole transmission is set on the basis of the preamble bit time estimation (as explained in Section 4.3).

The designed filter pole is located, in the typical case, at 15kHz: this allows a quick settling of the filter without experiencing high variations on the estimated period during normal operations, as shown in Fig. 4.4: in the worst case, only the first couple of CMOS bits lacks precision in the evaluated period and has to be skipped by the clock synchronization system, while the others are useful to provide a correct timing. The error on the first bit period is less than 5%, while starting from the second bit it becomes less than 1%.

The large capacitor and resistor needed to design a filter with such a low cutoff frequency are not feasible to be realized with standard devices, but, since the tolerance on the pole frequency is quite

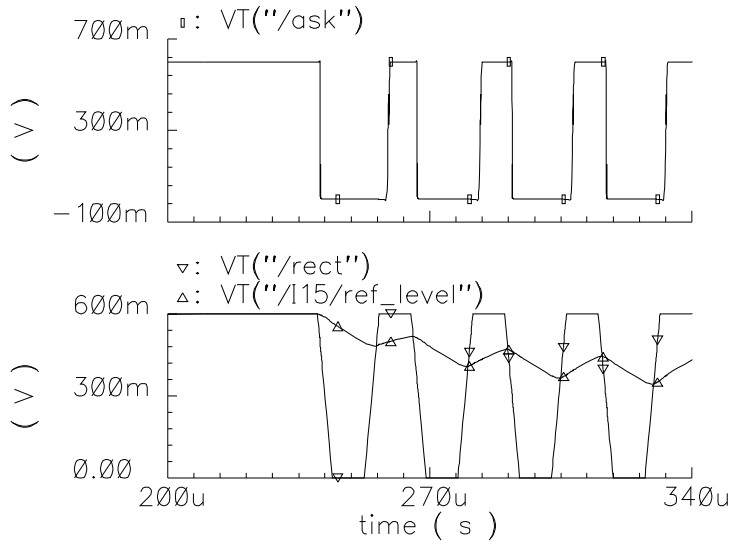

Figure 4.4: Preamble field: first demodulated bits

loose, they can be implemented with MOS transistors. The resistance is obtained by means of a series of 2 diode-connected native zero-threshold-voltage NMOS's with very low W/L (0.24/30μm), and exhibits a nominal value of 2MΩ, while the 5pF capacitor is made up of an NMOS sized 20/30μm.

4.2.2 Comparator

The common mode voltage at the inputs of the comparator is the average value of $rect$, that, according to the distance between tag and interrogator in the desired reading range, can vary from 0.3 to 1V (approximately). It is quite difficult to design a comparator working with this wide range of input common mode with a fixed supply; moreover, the regulated vdd_reg can be far lower than $rect$ in proximity of

the reader. On the other hand, the unregulated output of the charge pump vdd_unreg depends in the same manner of $rect$ on the available energy, and is always higher than the first bridge output. Therefore, the comparator is directly empowered with the unregulated supply: a down-conversion buffered level-shifter is used to feed its output to the digital core of the tag.

The schematic of the comparator is shown in Fig. 4.5. As explained in Section 3.6, the low number of analog stages and the variability of the voltage reference throughout the process corners discourages the creation of a current reference: in this case, as well as in the regulator of Fig. 3.21, the current sources of the circuit are implemented with ZVT NMOS's with $V_{GS} = 0$. Every ZVT transistor has the same size in order to grant the best matching.

The input pair $M_{1,2}$, given the low input common mode in the worst case, is made up with LVT transistors. According to the input differential value, the latch structure composed by $M_{3,4}$ allows one of the two branches to be switched off, driving all the current on the other one. Since $\left(\frac{W}{L}\right)_6 = 2\left(\frac{W}{L}\right)_8$ and $\left(\frac{W}{L}\right)_5 = 2\left(\frac{W}{L}\right)_7$, the output of the external branch whose PMOS is turned off is set to zero by the ZVT current source, while the other is driven to vdd_unreg (the pull-up current set by the PMOS is twice the pull-down current set by the ZVT NMOS).

An important issue comes from the fact that, as mentioned in the previous paragraph, during the *preamble detect* phase the output of the filter collapses to $rect$. Not considering the possible offset, both the positive and negative outputs in this case would assume the same value, and it could even not be a definite logic state: nominally in the quiet state the pull-up and pull-down currents on the external branches are balanced. The logical value expected by the digital core in this situation is "high", because the amplitude of the RF signal is maximum. In order to identify the correct state of the input signal, the differential pair $M_{1,2}$ has been slightly unbalanced: $\left(\frac{W}{L}\right)_1 = \left(\frac{20}{0.3}\right)$ µm and $\left(\frac{W}{L}\right)_2 = \left(\frac{30}{0.3}\right)$ µm. Such a difference in the pair allows the CMOS data to assume a "high" state if the input potentials are identical; the unbalance is however not high enough to cause an incorrect evalua-

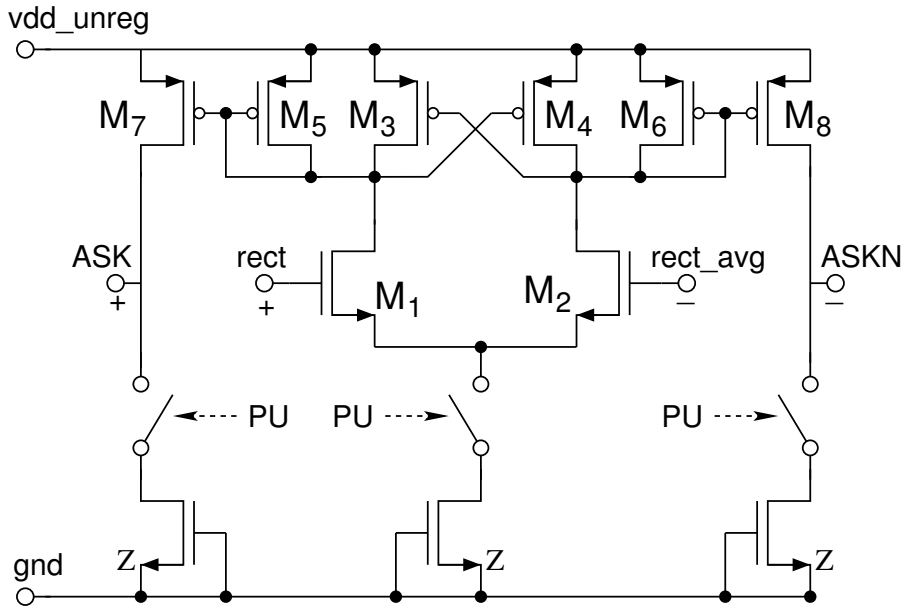

Figure 4.5: Schematic of the comparator

tion of a "low" state for differential input voltages lower than 20mV, condition that should be met even in the worst-case scenarios.

It is worth pointing out that this circuit is actually employed only when the tag is listening to the reader, while it becomes useless in the backscatter answering phase, where the available power is the lowest due to the antenna shorting. In order to save power, the ZVT current sources have been equipped with switches that block the current flow once the reading phase has ended: they are actually NMOS transistors with channel length higher than the minimum one to reduce the leakage. The signal controlling this operation, coming from the digital core, is level-shifted to the highest supply vdd_unreg (with the circuit shown in Fig. 4.12) in order to reduce the voltage drop through the switches without increasing too much their size.

Simulations results evidence the fact that the offset of the comparator, as typically found in this kind of circuit, is quite large: in the case of low modulation depth (18%), the excursion of $rect$ could be as low as few dozens mV, not enough to overcome such a large shift of characteristics. This could cause wrong data to be sent to the digital core. It is hence mandatory to insert a pre-amplifier before the comparator, improving the input swing; it is a simple active-load differential stage, with the same supply, ZVT current source and power-up switch described for the comparator. MonteCarlo simulations confirm the benefits of the pre-amplifier, exhibiting a correct output data flow throughout process and mismatch variations.

The average current consumption of the circuit, in a typical case assuming $rect$ to vary around 0.5V and vdd_unreg=1.4V, is around 600nA. It should be noticed though that the current request tends to decrease as the available power (and thus vdd_unreg and $rect$) decreases, since the voltages of the ZVT current sources drain terminals get lower and lower.

4.3 Clock generation

In order to achieve a reader-tag communication with the correct data-rate set by the standards, it is mandatory for the tag to have an accurate internal clock generation system. Moreover, since the timing of the logic core of the circuit relies on this clock, a higher precision on its frequency reflects in a better control of the overall power consumption: the digital gates can be customized aiming at the lowest power request given the highest working frequency of the circuit.

Due to the process variations in the chip manufacturing, the realization of oscillators with the desired precision is not feasible with the currently available technologies. Specifically, the chosen 0.18μm process features variations of ±15% on capacitors and ±20% or more on resistors and transistor characteristics (i.e. MOS threshold, mobility and oxide capacitance). Whichever architecture should be chosen, an

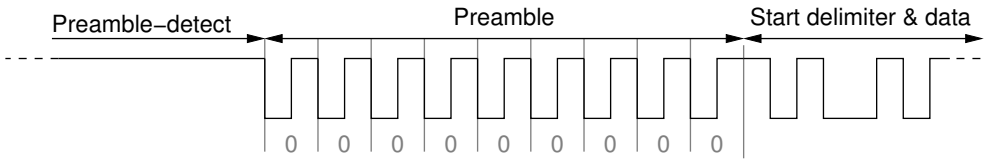

Figure 4.6: Reader-to-tag communication: preamble field

oscillator nominally tuned to the correct frequency would not guarantee an acceptable data-rate in many corners of the PVT space, even if the specs have a quite loose tolerance (15% on the retransmission data-rate for the ISO18000-6B standard).

Most commercially available RFID tags generate their clock using oscillators tuned to the desired frequency with a post-fabrication trimming procedure. Although this technique grants low power consumption, the trimming operation heavily affects the cost of the overall product. Thus, since the proposed tag has a cost-driven design, a new solution has been developed, allowing to obtain a quite accurate data-rate frequency without resorting to external trimming in exchange of a slightly higher current request.

4.3.1 Self-calibrating clock circuit

The idea at the basis of the circuit takes advantage of the preamble bits present in the reader-to-tag standard-regulated communication. The ISO/IEC 18000-6B standard requires the reader to send, after the *preamble detect* unmodulated RF signal used for the tag powering-up, a *preamble* field made up of 9 Manchester-coded NRZ logic zeroes, that is a 9-periods 40kHz square wave with 50% duty cycle (Fig. 4.6). Once demodulated, this signal is commonly employed to synchronize the tag internal clock with the data flow.

The proposed circuit [27] makes use of an oscillator whose frequency is several times higher than the desired one. The data-rate period is evaluated by averaging the number of these high-frequency

clock periods between two transitions during the preamble field; the result of such a measurement is then stored and used to define the division factor that will be applied to the HF-clock in the successive phases of interrogation and retransmission. As already pointed out in Section 4.2, the first bits in the preamble have to be skipped since their evaluated period could suffer a certain lack of precision. A block diagram of the clock generation circuit is shown in Fig. 4.7.

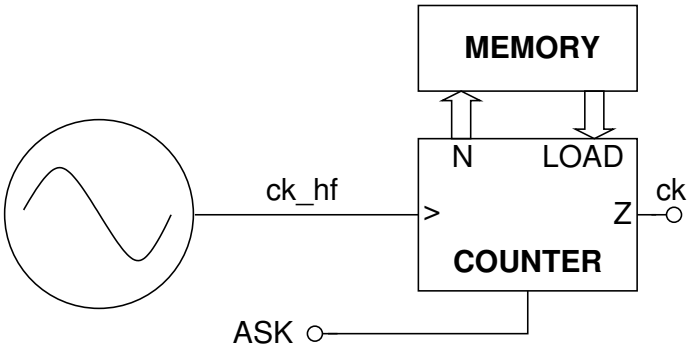

Figure 4.7: Clock generation circuit

A recently reported solution [28] employs a similar technique to generate the internal clock without resorting to trimming at the wafer sort. It should be noticed, though, that while that work resorts to a high-frequency-based evaluation of the received bits and a fixed dividing ratio (that does not fulfill the retransmission data-rate tolerance), the proposed architecture has been specifically designed to reduce the fast-switching (and thus more power-hungry) circuitry only to the oscillator and the counter in both up- and down-link communications, providing in either way a correct timing.

As a matter of fact, during the interrogation phase, the Manchester coding of the received bits allows the possibility of a continuous clock resynchronization, since, according to their logic value, they present a high-low or low-high transition occurring in the middle of the bit

period. The clock can be realigned with these transitions without resorting to extra HF-working circuits [29].

Thus, the tolerance on the generated signal is basically defined by the one that the standard specification dictates on the return link transmission bit time, that is $\pm 15\%$ of the period T_L (see Table 4.1).

	$T_L[\mu s]$	$f_{dr}[kbps]$
+ 15%	28.75	34.78
nominal	25.00	40.00
- 15%	21.25	47.06

Table 4.1: Standard specifications on return link bit time and data-rate

The number of high-frequency periods counted during T_L can be rewritten as $int(T_L f_{ckH})$, f_{ckH} being the HF-clock frequency. Therefore, the resulting internal clock period used for the data management T_{ckL} is

$$T_{ckL} = \frac{int(T_L f_{ckH})}{f_{ckH}} \tag{4.1}$$

The error on the nominal data period T_L is thus

$$\epsilon = 1 - \frac{int(T_{ckL})}{t_L} \tag{4.2}$$

In order to fulfill the requirements of Table 4.1, the minimum frequency f_{ckH} of the HF-clock can be obtained combining (4.1) and (4.2):

$$\frac{\Delta T_{L,max}}{T_L} = 1 - \frac{int(T_L f_{ckH,min})}{T_L f_{ckH,min}} \tag{4.3}$$

Figure 4.8 shows that the minimum acceptable value of the high-frequency clock is $f_{ckH,min}$ =240kHz, suggesting at least a three-bits counter to generate the 40kHz low-frequency clock with a minimum division factor of 6.

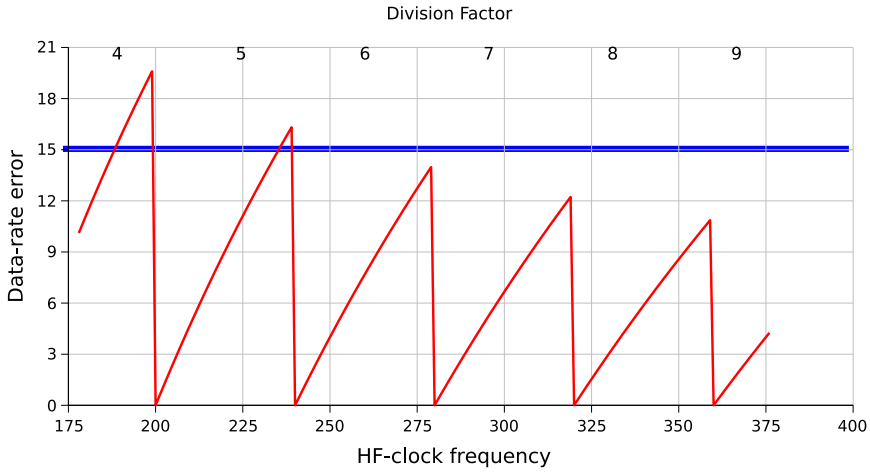

Figure 4.8: Data-rate relative error vs. HF-clock frequency

It should be pointed out that the proposed technique is suitable to be used not only for the chosen standard, but for every one providing a preamble field for the clock synchronization from reader to tag.

4.3.2 High frequency oscillator

The choice of the oscillator architecture, among the several possible ones, is driven in this application by power consumption and in a second time by area constraints.

Commercial tags usually employ relaxation or RC oscillators, because they are simple to calibrate with an external trimming. Since this technique has been discarded for the project, these kinds of oscillator lose their main advantage, and while their current request is not excessive, the size of their components may represent an issue given the involved low frequencies. Integrated LC-tank based circuits suffer of the same problems; moreover, the low voltage supply raises several difficulties in the design of such architectures.

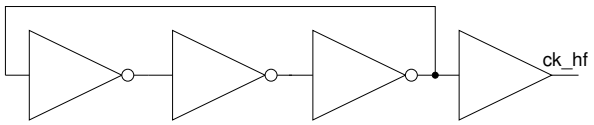

Figure 4.9: Buffered 3-stages ring oscillator

Ring oscillators are by far the smallest and least power-hungry circuits, but they exhibit a great frequency spread over supply voltage, process and temperature variations. Nonetheless, the presence of the supply regulator depicted in Section 3.6 and the auto-calibration technique described in the previous paragraph allow to overcome these issues, indicating therefore the ring oscillator architecture as the most suitable for the desired application.

In order to minimize the power consumption of the circuit, the number of inverting stages has been set to the minimum one, i.e. three. The schematic of the ring oscillator is reported in Fig. 4.9.

The inverters have been realized with regular PMOS's and NMOS's, without resorting to low-threshold devices that would increase both the switching and the leakage current. As a matter of fact, the regulated voltage supply ranges from 0.5 to 0.7V, and the threshold potentials of the transistors V_{THn} and V_{THp}, respectively for NMOS and PMOS devices, range (in absolute value) from 0.35 to 0.5V. Hence, $|V_{THp}|, V_{THn} > vdd\_reg/2$: this means that during the transitions there can be no interval where both the MOS's are in strong inversion region, saving therefore considerable amounts of dynamic power.

Since the number of stages N is equal to 3, the oscillation frequency of the circuit is

$$f_{ckH} = \frac{1}{2NT_d} = \frac{1}{6T_d} \tag{4.4}$$

where T_d is the delay of an inverter, calculated as the average of the propagation times in the high-low (t_{pHL}) and low-high (t_{pLH}) transitions:

$$T_d = \frac{t_{pHL} + t_{pLH}}{2} \tag{4.5}$$

The propagation time of a single inverter, loaded by an equal port, can be calculated on the basis of the analysis performed in [30], assuming that the current of the MOS working in the subthreshold region affects negligibly the charge of the loading capacitor. For example, t_{pHL} can be expressed as

$$t_{pHL} = \left(\frac{\frac{V_{THn}}{V_{DD}} + \alpha_n}{1 + \alpha_n} - \frac{1}{2} \right) t_T + \frac{C_L V_{DD}}{I_{D0n}} \tag{4.6}$$

$$t_T = \frac{C_L V_{DD}}{I_{D0n}} \left(\frac{0.9}{0.8} + \frac{V_{D0n}}{0.8 V_{DD}} \ln \frac{10 V_{D0n}}{e V_{DD}} \right) \tag{4.7}$$

where α_n is the velocity saturation parameter, V_{D0n} and I_{D0n} are, respectively, the drain-source saturation voltage and the maximum drain current of the NMOS when the inverter input voltage is V_{DD}, while C_L is the loading capacitance, including the layout parasitics, of the following stage. It should be pointed out that the capacitor value is strongly dependent on the output level, since the transition is roughly centered around the MOS threshold voltage: both the loading transistors switch between weak and strong inversion, where their gate capacitance can vary by a factor of 3 according to the typical MOS capacitor characteristic. An average value has been used in calculations.

The same analysis can be applied for the calculation of t_{pLH}:

$$t_{pLH} = \left(\frac{\frac{-V_{THp}}{V_{DD}} + \alpha_p}{1 + \alpha_p} - \frac{1}{2} \right) t_T + \frac{C_L V_{DD}}{I_{D0p}} \tag{4.8}$$

$$t_T = \frac{C_L V_{DD}}{I_{D0p}} \left(\frac{0.9}{0.8} + \frac{V_{D0p}}{0.8 V_{DD}} \ln \frac{10 V_{D0p}}{e V_{DD}} \right) \tag{4.9}$$

While $\alpha_{n,p}$, $V_{THn,p}$ and $V_{D0n,p}$ are parameters set by the technology and show little dependency on the transistors length and width, C_L

and I_{D0} are strong functions of the MOS's size, since the first is proportional to the product and the second to the ratio between channel width and length. Therefore, given the desired output frequency, the devices dimensions can be easily obtained combining (4.6), (4.8) and (4.4): estimated parameters and results are summarized in Table 4.2, and it can be noticed that the relatively low target frequency of 800kHz causes the transistor channels to be quite longer than the minimum that the technology allows (0.18μm).

	Nmos	**PMOS**
Target f_{ckH} [kHz]	800	
V_{DD} [mV]	600	
α	2.1	1.9
$\|V_{TH}\|$ [mV]	350	460
W [μm]	1	2
L [μm]	8.3	8.3
V_{D0} [mV]	226	150
I_{D0} [nA]	1100	167
C_L [fF]	110	
Calculated f_{ckH} [kHz]	805	
Simulated f_{ckH} [kHz]	790	

Table 4.2: Typical-case parameters of the ring oscillator

The introduction of a buffer stage in order to retrieve the clock and retransmit it to the digital core can cause the output frequency to decrease, but if the capacitive load is small compared to the already present one the performance loss will not be critical. Since in the designed circuit the buffer input capacitance is less than 0.8% of the inverter one, the clock period remains almost unaltered.

It is worth pointing out that the inverter delay suffers far more of temperature and process variations with respect to the typical design situation in which the MOS threshold is far lower than the supply voltage: a wide spread of the output frequency over PVT space can

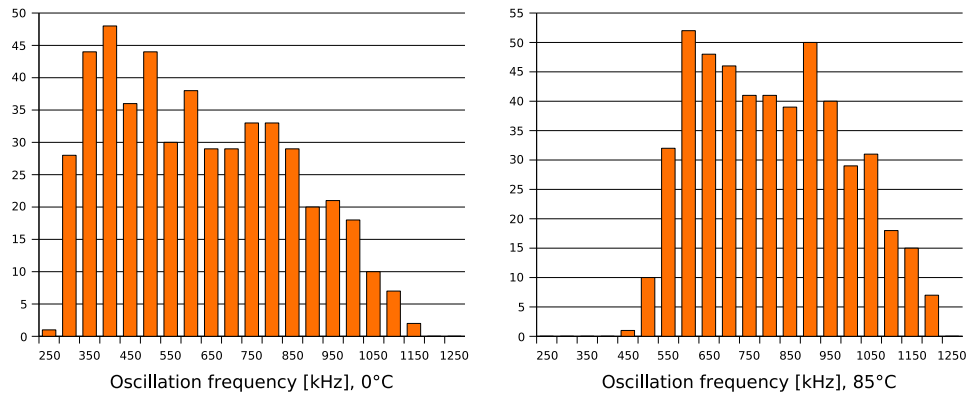

Figure 4.10: Oscillator output frequency through 500 MonteCarlos

thus be expected. In fact, setting the transistors size to obtain a minimum frequency of 240kHz in the slowest corners reflects into the maximum frequency being pushed towards 1.1MHz: this causes the extension of the counter to 5 bits in order not to experience an overflow, as the highest division factor becomes now 25. Furthermore, since a 5-bits counter can manage an input frequency of 1.24MHz for an output frequency of 40kHz, the span of the desired oscillator has been traslated to 284÷1220kHz, thus reducing the maximum error on the low-frequency clock period to 12.5% (for a frequency of ≃320kHz divided by 7). This explains why the data reported in Table 4.2 refer to a typical frequency of 800kHz. Fig. 4.10 shows the distribution of the clock frequency through 500 MonteCarlo simulations considering process and mismatch variations, affecting both the oscillator and the regulator to ensure the most realistic scenario. The simulations have been repeated at 0 and 85 degrees.

The average current requested by the oscillator in the typical case is 170nA, mostly due to the buffers that have to drive a relatively long line to reach the digital core of the chip; the maximum value collected through the same MonteCarlos is 380nA, as reported in Fig. 4.11.

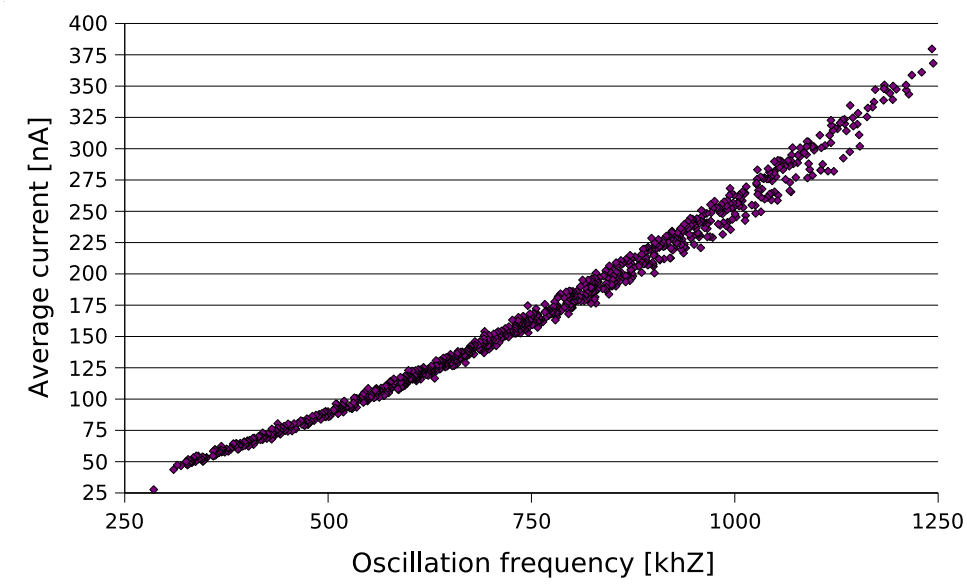

Figure 4.11: Oscillator current consumption vs. frequency through MonteCarlos

4.4 Backscatter transmitter

The digital section, once elaborated the instructions received in the interrogation phase, outputs a MOD binary signal representing the answer to be sent to the reader. Such a data flow has to be translated, applying the backscatter technique described in Section 2.2.2, into "high reflectivity" or "low reflectivity" states of the tag, that means shorting the antenna terminals or leaving them untouched according to the bit logical value.

The standard sets the discrimination between high and low reflectivity state by referring to the variation of radar cross sectional area. Since this parameter heavily depends on the antenna physical features [31], it is somewhat difficult to define specs on the strength

of the switch, which has been implemented with a standard NMOS device. Furthermore, the lower is the on-resistance of the MOS (and hence the poorer the impedance matching), the more the current and voltage distribution through antenna and load behaves like standing wavefronts: the evaluation of the electrical quantities and parameters involved in this situation becomes a task particularly hard to accomplish.

The size of the backscatter transistor has therefore been estimated to be 20/0.18μm: it should be enough to guarantee a good radar cross sectional area variation without introducing a noticeable capacitance between the two inputs; also it should support the maximum current flow without suffering an excessive stress. In order to improve the switch strength, the signal driving the transistor, coming from the digital core under the regulated power supply, has been level-shifted to the highest potential of the chip (*vdd_unreg*) with the circuit shown in Fig. 4.12.

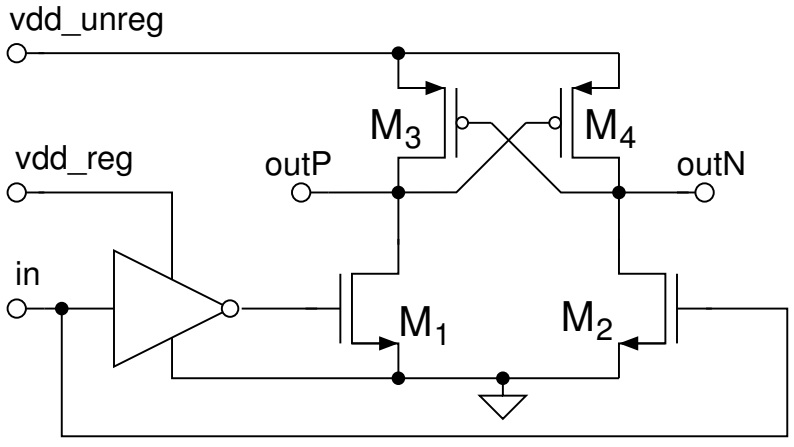

Figure 4.12: Level-shifter from regulated to unregulated supply

Chapter 5

Testing and measurements

The designed circuits functionality and performances have been verified on a suitable testboard, employing an appositely modified version of the chip allowing to measure the electrical features of the previously depicted blocks. In this chapter, both this chip and the PCB are described, along with the measurements methodologies and results.

5.1 Design for testability

The transponder chip has only the $in1$ and $in2$ I/O pins, connected to the two antenna terminals. For testing purposes, it could be used only for the measurement of the input impedance and the functionality of the whole tag: no information can be retrieved about the DC levels and rectification efficiency, the internal clock frequency, the references and the digital data. Moreover, a malfunction occurring in any of these circuits could cause the whole tag to fail, without any mean of understanding where the failure originates from. Therefore, in order to validate the results obtained in simulations, it is necessary to access several other points of the chip.

Many are the measurements that have to be taken on the chip to confirm functionality and electrical features of the circuits. In fact,

Test	**Measure type**
Tag input impedance	RF/AC
First bridge output voltage	RF/DC
Power retriever output voltage and efficiency	RF/DC
Voltage and current reference	DC
Regulator performances	DC
Clock frequency	transient
POR functionality	DC
Demodulator functionality	transient
Power retriever output voltage with antenna	RF/DC
Tag functionality	transient

Table 5.1: Measurements to be performed on the testchip

there is a certain lack of precision in the modelization of the transistors parameters, especially given the very low involved power and currents and the use of ZVT and LVT transistors (usually poorly characterized by the fab models). Therefore, for almost every block described in the previous chapters a functionality test should be performed, measuring also the circuit performances where needed.

The tests to be taken are summarized in Table 5.1.

5.1.1 Probe points and modularity

In order to perform the tests of Table 5.1, the signals to be probed in the circuit are the following ones:

- gnd: reference level for almost every test
- vdd_unreg: for the power retriever output level and efficiency
- vdd_reg: for the regulator performances
- V_{REF}: for the voltage reference characterization

- $PORN$: for the Power-On-Reset functionality
- ASK: for the demodulator functionality
- CK: for the HF clock measurements
- $rect$: for the first bridge analysis

Actually, a perfect replica of the voltage reference circuit has been employed for the V_{REF} characterization. Such a choice is due to the noise introduced by the switching signals on the padring, that, coupling with the original reference voltage, would affect also the measurements of the regulator performances. Moreover, this solution simplifies the layout routing.

Another pin has been added to perform measurements on the gated ZVT NMOS current reference. As a matter of fact, given the usually poor quality in the modelization of such a kind of device (especially for long gate channels), its use as current source is an architectural choice quite risky: hence the need to provide an independent probe point to characterize it. The expected current values for a 0.5/30μm transistor are in the hundreds nA range, and it is difficult to measure such low currents with a common ammeter. Thus, a 1MΩ resistor has been placed on the testboard, allowing to achieve the I_{REF} value by measuring the voltage drop caused by the current flow: the schematic of such a solution is shown in Fig. 5.1.

The digital section of the chip features a multiplexer bank allowing to connect the A/D interface I/O signals either to external data or to the ones generated by the digital core. It is therefore possible to test independently the two sections, as well as perform measurements on the global architecture: there are two digital input pads in the analog section allowing to feed RX and MOD from the testboard.

Similarly, it would be extremely useful to have the possibility to test separately and independently the main blocks of the circuit. For example, the performances of the RF/DC converter affect the behavior of the voltage regulator, and the digital section or the oscillator would

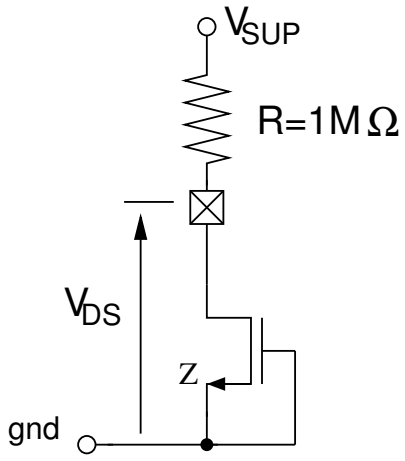

Figure 5.1: Schematic of the current reference testing circuit

be more easily characterized with an external supply. Moreover, a possible failure in any section on the power line (bridge, charge pump, reference and regulator) would make the testing of the other blocks impossible. Therefore, a modular decomposition of the power supply domains has been introduced, allowing to use the DC voltages coming either from the power management circuits or from the testboard.

Such a modularity has been achieved by inserting two switches on the power line, one on the unregulated and the other on the regulated voltage supply.

The former, located immediately after the 1nF MOS capacitor, separates the output of the charge pump vdd_unreg_out from the effective supply of the other analog blocks vdd_unreg_in: both these potentials can be accessed from the testboard. When the switch is open, they can be employed respectively for the RF/DC converter characterization and for an independent analog supply; when the switch is closed, they are shorted and the whole circuit can be tested. Actually, the switch could have been placed outside the chip on the PCB; however,

in order to limit the ripple effect due to the bonding wires and other parasitics, the internal solution has been preferred, and it has been implemented with a big-sized transmission gate (400/0.24μm for the LVT-PMOS, 200/0.24μm for the LVT-NMOS) with an external driving signal vdd_unreg_sw.

Likewise, the second switch separates the output of the voltage regulator vdd_reg_out and the effective regulated supply vdd_reg_in. The latter can feed the oscillator and the other low-voltage circuits, and, separately with another apposite switch, the digital section of the chip. An identical transmission gate has been employed, driven by the vdd_reg_sw signal.

Figure 5.2 depicts the frontend schematic with these newly introduced probe points and control signals.

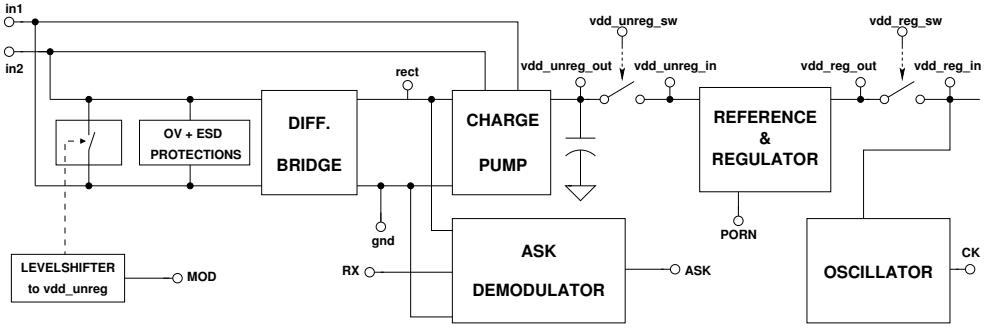

Figure 5.2: Schematic of the analog frontend with I/O pins

5.1.2 Padring

The introduction of several pins to be used as probes or inputs may impact the chip behavior. In fact, it is necessary to create a padring structure in order to simplify the bonding process and to protect the pads from ESD events among each other.

The standard pads with protection diodes introduced for such a purpose need both a ground and a supply ring. While the gnd potential is suitable to be used for the former one, it is somewhat difficult to determine what signal to use for the padring supply. The highest potential in the circuit is vdd_unreg; however, it is not a good idea to use it to provide the supply voltage for the other pads. As a matter of fact, such a choice would dramatically increase the power drawn from $in1$ and $in2$ during the RF measurements: the leakage current of the protection diodes (that are quite large) and especially the dynamic power associated with the switching signals present in the padring (such as CK or ASK) would overwhelm the actual consumption of the tag circuits, which can be as low as few hundreds nA.

It is hence mandatory to introduce a padring supply pin $VDD18$, whose potential can be set from an external voltage source: as long as its value is higher than the unregulated voltage, it causes little interference with the main circuit, and allows vdd_unreg to experience only its proper loading current. If $VDD18$ is left unconnected, the padring supply will settle to $vdd\_unreg - V_{TD}$, where V_{TD} is the threshold of the protection diode present between the unregulated supply pad and the power ring, and the extra current will again load the rectification stage.

In order to drive the line capacitance of the PCB and the instrumentation wires, the digital switching signals, especially the high-frequency clock, have to be buffered. Since their power supply is the regulated one, such buffers, if connected to vdd_reg, would cause the same unwanted extra power consumption loading the rectification circuit. The presence of the padring supply allows to overcome this issue, since the buffers dynamic current is provided by an external source independent of the power harvesting circuit. It is necessary however to change the supply domain of the signals from vdd_reg to $VDD18$: a level-shifter like the one depicted in Fig. 4.12 has been used for such a purpose for ASK, $PORN$ and CK.

A summary of all the I/O pads of the testchip is reported in Table 5.2. Every one of them is connected to a pin of the packaged chip.

Pin name	Direction	Description
in1	Input	Analog RF input
in2	Input	Analog RF input
gnd	Ground	Ground
VDD18	Supply	1.8V padring supply
rect	I/O	Bridge output, demodulator input
vdd_unreg_out	Output	RF/DC converter analog output
vdd_unreg_sw	Input	Unregulated supply digital switch
vdd_unreg_in	Input	Unregulated supply analog input
vdd_reg_out	Output	Regulator analog output
vdd_reg_sw	Input	Regulated supply digital switch
vdd_reg_in	Input	Regulated supply analog input
ASK	Output	ASK demodulator digital output
PORN	Output	Power-On-Reset digital output
CK	Output	High-frequency clock digital output
MOD	Input	Backscatter switch digital input
RX	Input	Demodulator-enabling digital input
Vref	Output	Voltage reference analog output
Iref	Output	Current reference analog output

Table 5.2: Summary of I/O pads of the testchip

5.1.3 Package

While the final product will be directly mounted on the antenna, a packaged version of the testchip proves useful, since it is simpler to solder the prototype on the PCB rather than bonding it.

Apart from $in1$ and $in2$, every other I/O signal exhibits a low working frequency (from DC to 1.2MHz) and it is scarcely influenced by the package parasitics. On the contrary, measurements involving the RF section, like the ones on rectification efficiency and input impedance, suffer of the package presence: for such tests, it is preferrable to use a chip-on-board solution with a limited number of bonded pads.

5.2 Layout

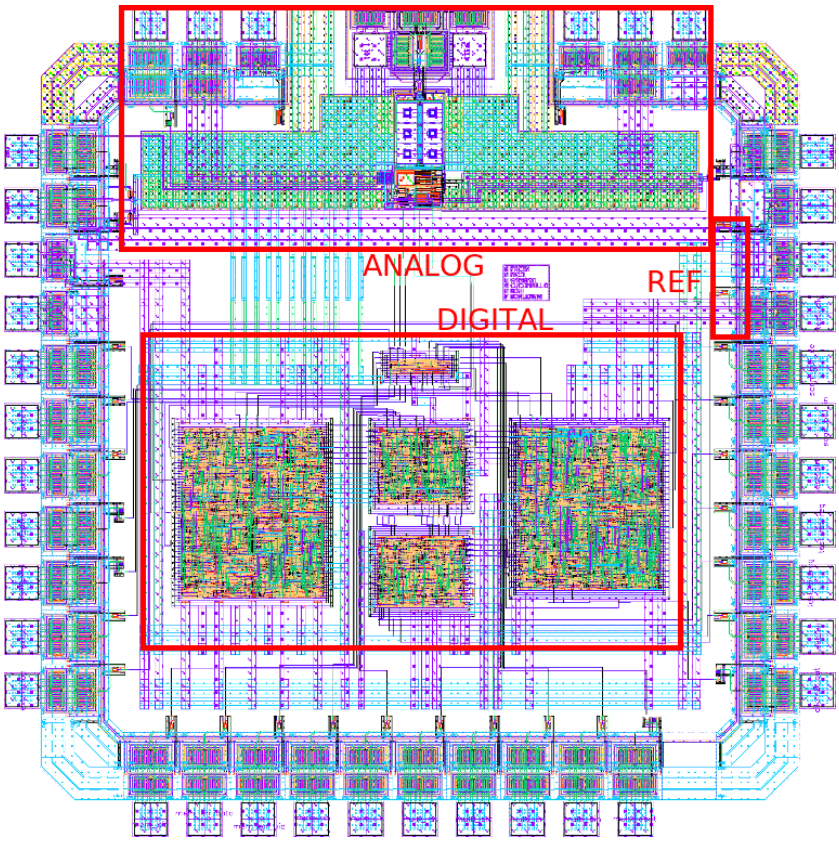

Figure 5.3: Testchip layout

The layout of the testchip is shown in Fig. 5.3: the size of the die is 1.5x1.5mm^2. It can be noticed though that a great amount of area is occupied by the padring; moreover, two different implementations of the digital core have been included, as well as the independent current and voltage references.

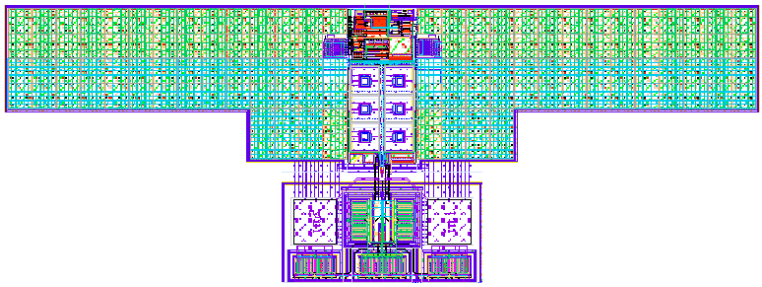

Figure 5.4: Analog section layout

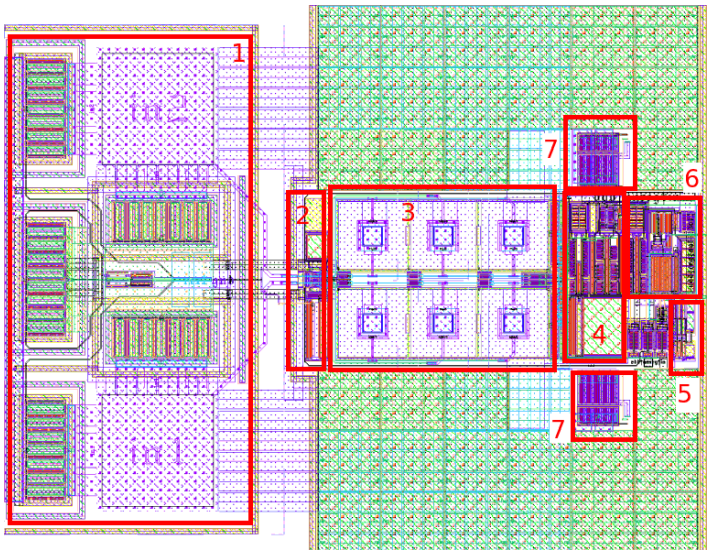

Figure 5.5: Zoom of the analog frontend layout: input pads and ESD/OV protections (1), first bridge and backscatter transistor (2), charge pump (3), demodulator (4), voltage reference and regulator (5), oscillator (6) and supply switches (7)

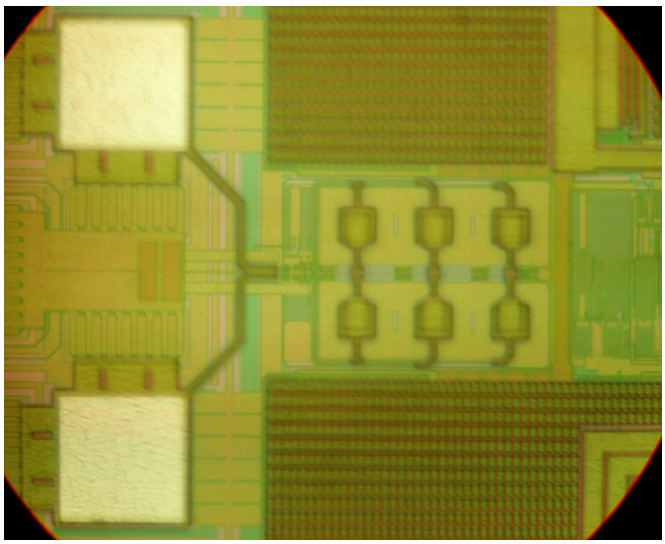

Figure 5.6: Photograph of the analog input section of the die

The analog section size is about 1x0.35mm^2, and can be greatly reduced, since the 1nF capacitor (the two lateral wings in Fig. 5.4) has been shaped to fit the space left by the padring.

The layout of the core of the analog section is reported in Fig. 5.5: the main circuits have been highlighted. The area occupation is dominated by the capacitor, while other less significant contributions are mainly due to the pads and protections and the voltage multiplier. The simmetry of the input section circuitry can easily be spotted; the most critical paths (the RF ones) have been realized with the highest metal levels (5 and 6) in order to reduce the parasitics. A zoom of a die micrograph showing the input section is also shown in Fig. 5.6.

Finally, the layout of the final version of the product is reported in Fig. 5.7: the capacitor has been reshaped and the digital section has been put on the side of the analog one. The size of the circuit is about 1x0.37mm^2.

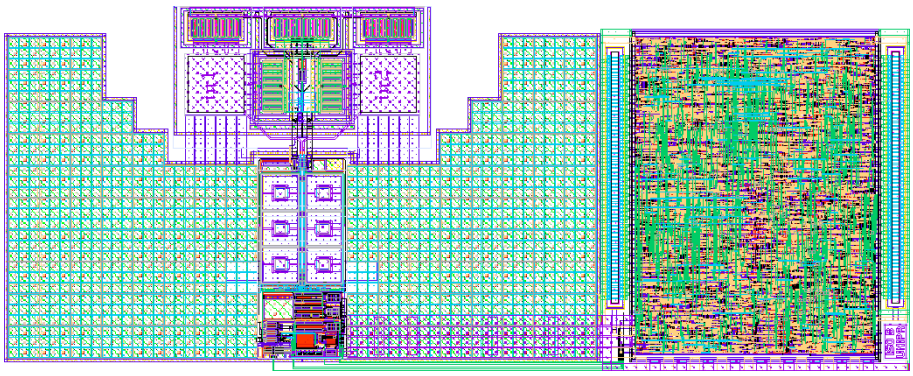

Figure 5.7: Final product layout

5.3 Testboards

5.3.1 PCB design

Although the testchip is made up of both analog and digital sections, different boards have been realized to test them separately. While the digital PCB may employ the analog RF inputs and the 1.8V padring supply to test the whole chip functionality, the board dedicated to the analog measurements does not take care of the digital I/O pins.

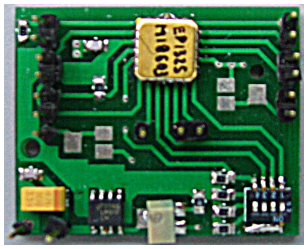

Figure 5.8: Testboard photograph in its actual size (4x3.2cm^2)

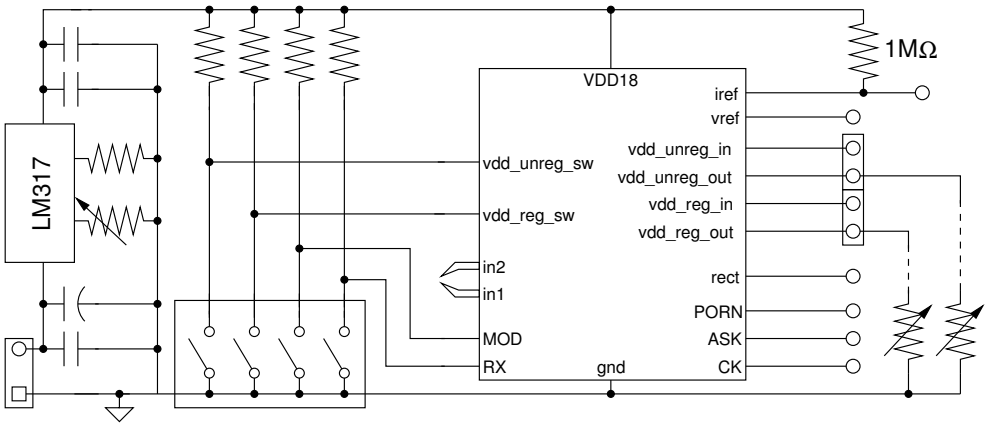

Figure 5.9: Analog testboard schematic

A schematic of the testboard is shown in Fig. 5.9.

In order to suppress noise and ripple, the 1.8V supply for the padring is provided by a trimmable LM317 voltage regulator. Its input comes from a voltage source, and is filtered by both a ceramic and an electrolitic SMD capacitor; its output is filtered by ceramic capacitors, one placed nearby and another in proximity of the RFID chip.

The digital inputs (MOD, RX and the supplies control gates) are connected either to the ground or the 1.8V supply by means of suitable switches: if a switch is closed, the signal is tied to gnd, while in the dual case a 10kΩ resistor brings it to $VDD18$. The vdd_reg_in – vdd_reg_out and vdd_unreg_in – vdd_unreg_out supply couples can be connected internally on the chip by means of their respective switch, but they are also placed contiguously on the testboard so that they can be shorted each other by means of a jumper.

There is the possibility to place a SMD trimmer both at vdd_reg_out and vdd_unreg_out, implementing a variable load emulating the digital core current request. Given the value of the expected currents and voltages, the trimmers maximum level is set to 2MΩ: such a resis-

tance allows to obtain an equivalent I_{LOAD} of few hundreds nA. On the contrary, the 1MΩ SMD resistor for the current reference characterization is not variable.

Each one of the RF input signals $in1$ and $in2$ is connected with a very short and small path to a metallic pad on the board, allowing to employ a network analyzer with a 150μm pitch, 50Ω coplanar probe in the measurements in order to maximally reduce the parasitics effect. The length of the paths is approximately 1mm, far shorter than the wavelength of the UHF carrier on the board (more than 15cm for a two-layers FR4 PCB with 1.6mm depth and 35μm metal thickness): the impedance mismatch introduced is marginal, as well as the space occupation on the PCB. In fact, in the board photography of Fig. 5.8 they are barely noticeable above the packaged chip on the top; the zoom reported in Fig. 5.10 on the chip-on-board PCB better shows such an RF structure.

5.3.2 Testboard with antenna

Once performed the measurements on the RF input impedance, as described in Section 5.4.1, different antenna prototypes have been realized matching the chip impedance according to the criteria explained in Section 2.4.1, allowing to test the functionality of the tag with the actual reader.

A single antenna has been made for the packaged version of the chip (shown in Fig. 5.11), while two different kinds of antenna prototypes (loop and dipole-like) have been developed where the chip is bonded directly on board. Although none of them represents the actual antenna of the final product, which will be implemented on a flexible material able to better adjust to the products to identify, they are useful to perform many tests on the reading distance.

At the present moment, the chip-on-board antennas are not available for measurements, since the bonding process takes a considerable amount of time.

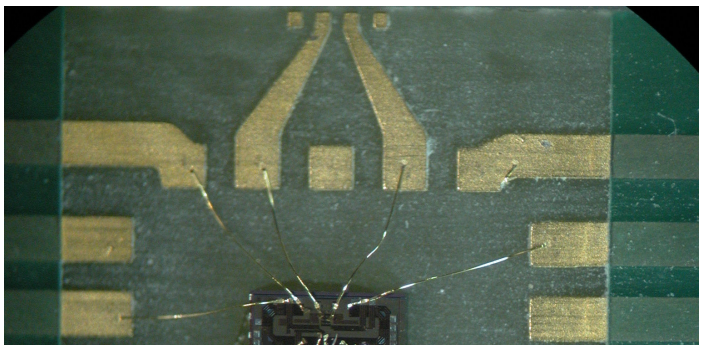

Figure 5.10: Zoom of the chip-on-board PCB

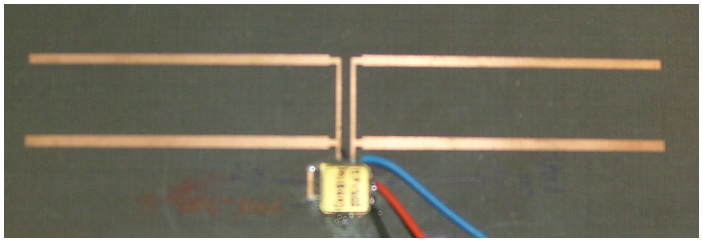

Figure 5.11: Photograph of the antenna and packaged chip

5.4 Experimental data: RF section

5.4.1 Impedance measurements

It is quite difficult to perform correct impedance measurements on the chip. In fact, the input peak voltage (and thus the impedance value) depends on the matching between source and tag, and there are many non-linear contributions in the relationship between input power and impedance. Most instruments have an output impedance of 50Ω. On the other hand, it is impossible to design a matching network without knowing the impedance to match.

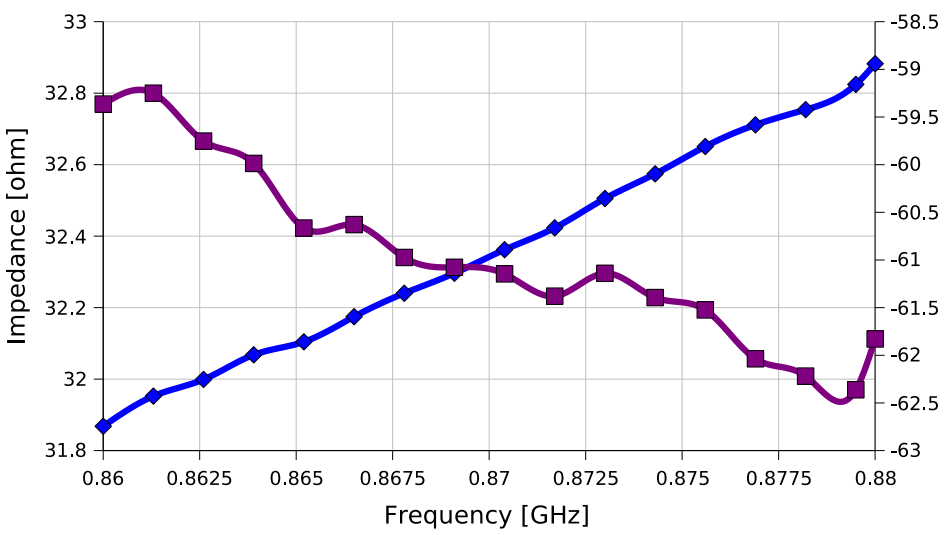

Figure 5.12: Packaged die input real (■) and imaginary (⧫) impedance

The approach adopted to characterize the tag input impedance consists in connecting the chip directly to a network analyzer, by means of a 50Ω coplanar probe: such a method is quite common and can be found in literature [32].

The input power considered for the measurements can not be the one used in simulations (-16dBm), since, as reported in Section 5.4.2, the impedance mismatch prevents the chip to work correctly (vdd_unreg is too low) with such a low power. Therefore, the power level employed for this test has been defined as the one allowing to achieve an unregulated voltage equal to 0.8V: from the measurements reported in Fig. 5.14, such a power is -2dBm. Although this method is not rigorous, it should provide a fair estimation of the actual impedance.

Fig. 5.12 shows the results obtained on the packaged testchip with externally powered padring. The impedance seen at 869.5MHz

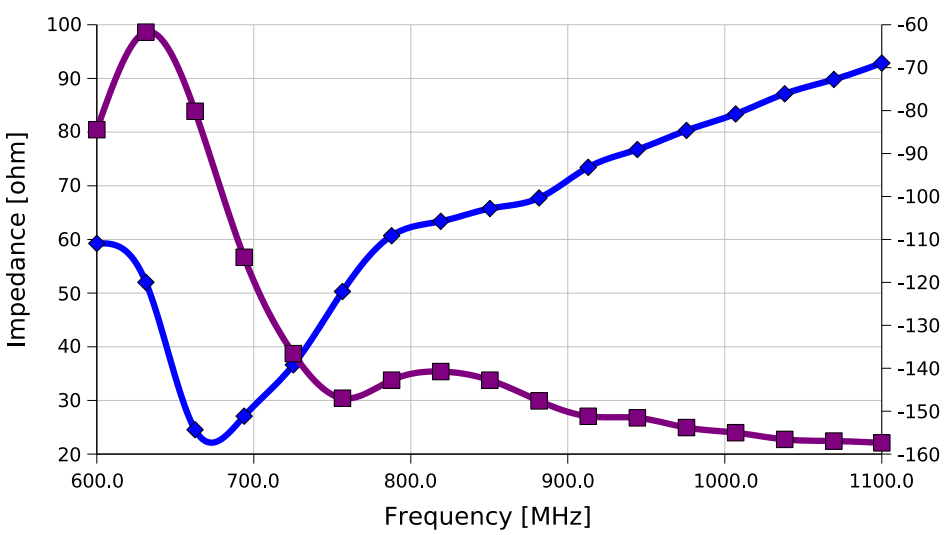

Figure 5.13: Bonded on board chip input real (■) and imaginary (♦) impedance

is 32.3-j61Ω: while the real part well fits the simulated data (as seen in Section 3.4), the negative imaginary impedance is several times lower than the expected one of 512Ω, meaning an equivalent series capacitor of almost 3pF. Such a considerable difference can be partly ascribed to the package parasitic effects: in fact, the same measurements taken on the chip bonded on board, reported in Fig. 5.13, exhibit a negative imaginary part of 101Ω, thus a 1.8pF equivalent capacitor, with more or less the same resistive part.

Nonetheless, there is still a remarkable discrepancy between the data obtained from modeling and simulations and the measured ones. The test methodology above described could have a hidden flaw in the estimation of the impedance, especially for its reactive part; other effects may also have not been considered in simulations. Further investigations on such a phenomenon are still in progress.

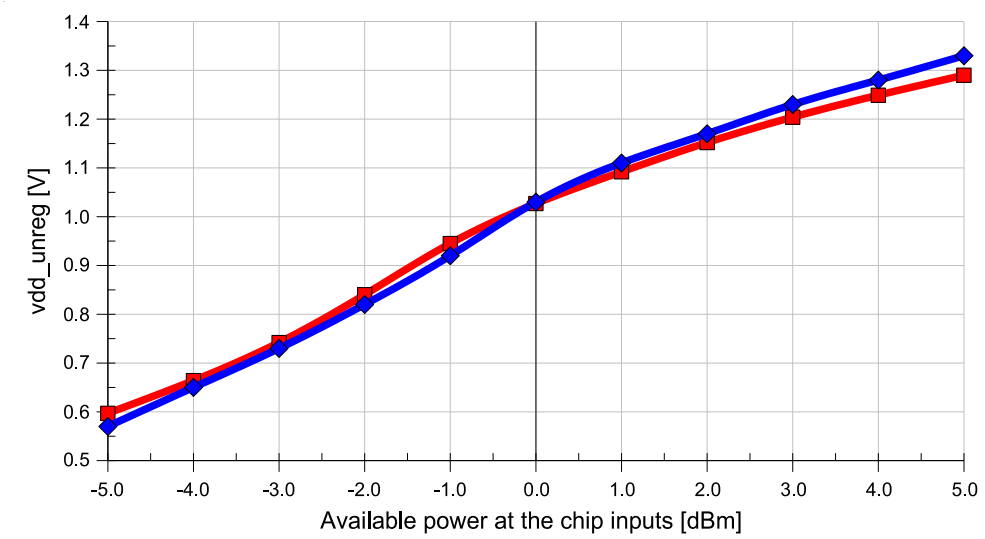

Figure 5.14: Simulated (♦) and measured (■) vdd_unreg vs. input available power

5.4.2 Power retrieval

The same instrumentation used for the impedance measurements has been employed to characterize the RF/DC converter, sweeping the available power coming from the network analyzer and retrieving vdd_unreg with a voltmeter.

The impedance mismatch occurring between the 50Ω network analyzer coplanar probe and the designed chip impacts the overall performances, and it is hence not possible to make a direct comparison between the obtained results and the simulations carried out in Section 3.5.

The load seen by the power retriever is the one of the analog blocks, with no extra current requested to the regulated supply (that is, the vdd_reg_sw pin has been grounded). A new set of simulations has been

carried out assuming such a set of conditions (impedance mismatch, package parasitics, same loading current), leading to the results reported in Fig. 5.14: the comparison between simulated and measured vdd_unreg exhibits a very good fitting, validating thus the theory described in Chapter 3 [33].

A measurement in the same conditions has been performed also on the unpackaged self-powered ($VDD18$ tied to vdd_unreg instead of a voltage source) chip: the results are shown in Fig. 5.15. The rectified voltage quickly drops below 0.8V around 0dBm, because of the current waste on the padring. When the input power is high, however, the results become similar to the previous ones: this is due to the fact that the power on the pads starts to be comparable with the one deliberately shunted by the overvoltage protections in the externally padring-powered chip.

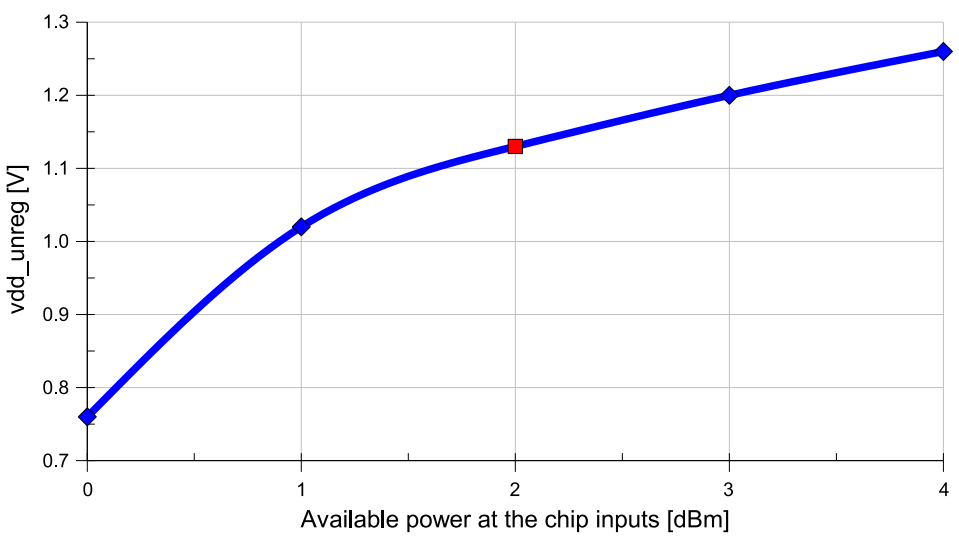

Figure 5.15: Measured vdd_unreg vs. input power, self-powered chip-on-board

5.4.3 Results with antenna

The only available results at the present time are the ones of the antenna of Fig. 5.11. The RF unmodulated field is generated by the reader of Fig. 1.1 with 1.5W EIRP, and the whole chip+antenna package has been placed on a mobile support: the RF/DC converter output voltage vdd_unreg has been measured varying the reading distance.

Such data have been achieved with the packaged chip and no external $VDD18$, i.e. the tag is self-powered and there is a lot of power waste on the padring: since the regulated supply empowers also the oscillators, the switching current on the padring is quite considerable. In fact, according to the results reported in Fig. 5.16, the output voltage of the RF/DC converter barely reaches 0.9V in proximity of the reader.

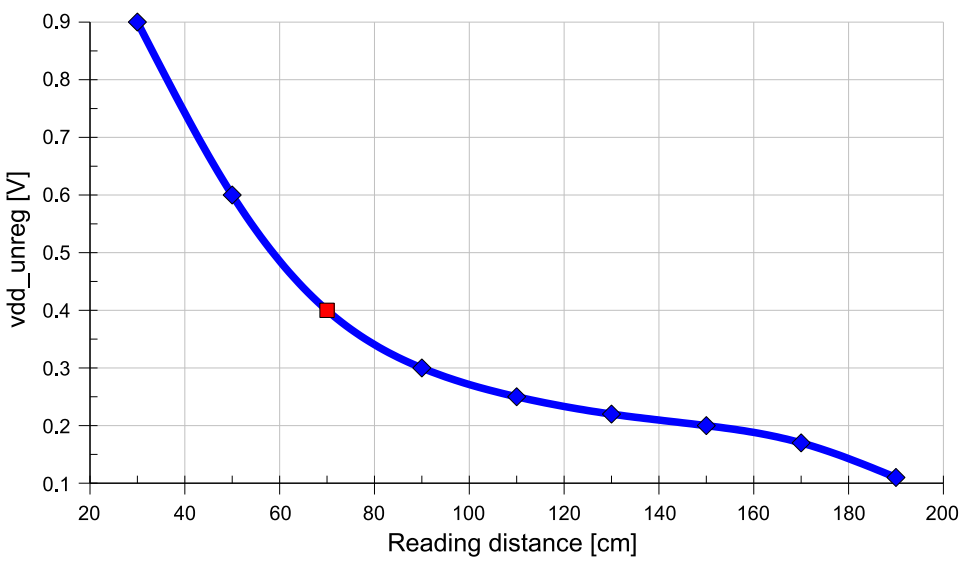

Figure 5.16: Measured vdd_unreg vs. reading distance

Further tests will be performed on the other chip and antenna bundles, trying also to provide the padring supply, in order to obtain more significant results.

5.5 Experimental data: baseband section

5.5.1 Voltage and current references

As mentioned in Section 5.1.1, two dedicated probe points are present in the testchip for a current and a voltage reference which are an exact replica of the ones used in the main tag, in order to characterize both of them independently of the rest of the circuit.

The gated ZVT NMOS used as current reference represents the most hazardous architectural choice in the design, since such a component is usually not accurately modeled by the silicon foundry. The first test is the determination of the current nominal value and its dependency on the drain-source voltage V_{DS}: referring to the circuit in Fig. 5.1, the I_{REF}/V_{DS} curve has been characterized by changing V_{SUP}.

The results, reported in Fig. 5.17, evidence a nominal value (for a transistor with W/L = 0.5/30μm) higher than the expected one, and a noticeable dependency on V_{DS} that did not emerge from simulations. The latter issue is the most critical, since it affects also the voltage reference.

In fact, the variation of V_{REF} with respect to the supply voltage is higher than expected from the simulation in Fig. 3.19. The measurements, performed at ambient temperature, show a variation of more than 40mV in the 0.8–1.8V supply span, that is almost three times the expected 14mV. Fig. 5.18 shows the voltage reference characteristic, as well as the output voltage of the regulator loaded with a 400kΩ resistor: there is a small discrepancy between the two values, mostly due to the regulator offset and the mismatch between its reference and the one actually measured. The PSRR of the whole LDO+reference stage is about 22dB: although being lower than the

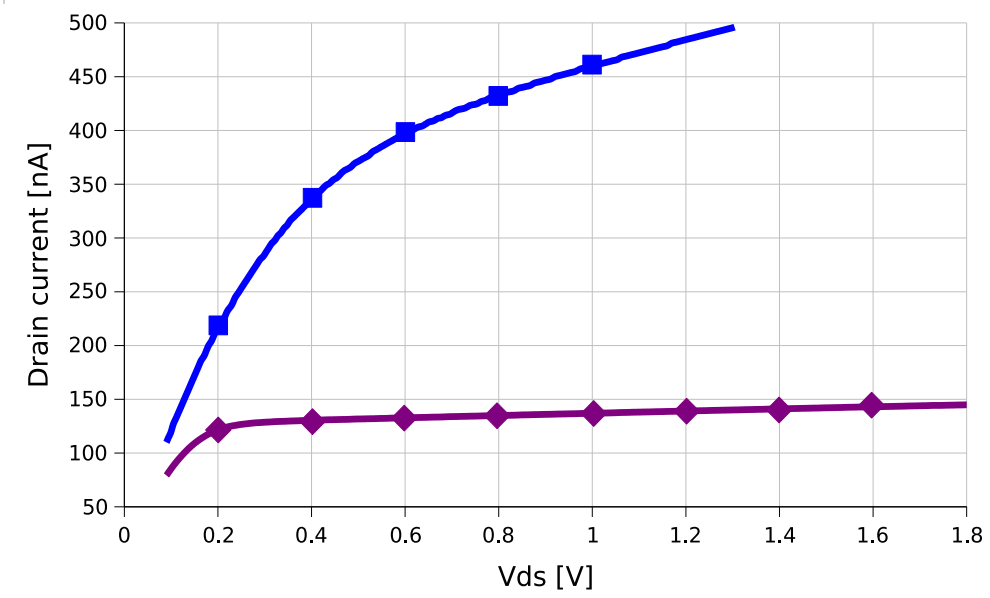

Figure 5.17: Simulated (♦) and measured (■) value of the current reference vs. V_{DS}

value found in simulations, it is still sufficient to reduce the distance dependency of the regulated supply, such in a way that the high-frequency oscillator period remains in the desired range, as reported more in detail in the next section.

The reference voltage has been characterized also in the 0–85 ° temperature range. The testboard has been put in a suitable oven, where the internal temperature could be controlled. Actually, the simulations performed in the previous chapters refer to the junction temperature and not to the air one; however, since the power consumption of the chip is few microwatts, the heating of the chip due to its own activity is negligible, allowing therefore to consider junction and air temperature to be approximately equal.

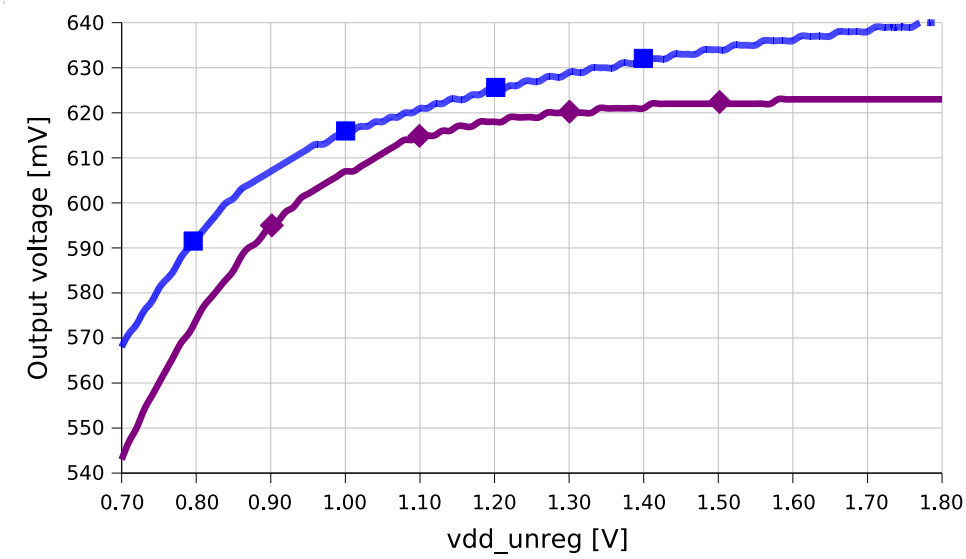

Figure 5.18: Voltage reference (♦) and regulator output (■) vs. supply

The results of the measurement are shown in Fig. 5.19. The sizing of the components done on the basis of the analysis performed in Section 3.6.1 proves effective: the derivative of the voltage reference indeed becomes zero in the desired range, thus minimizing the temperature effect. It can be noticed though that the measured sensitivity is not as good as the one expected from simulations; nonetheless, the variation of V_{REF} can be considered very small for the target application.

5.5.2 Oscillator

The clock generation system (Section 4.3) is made up of a dual analog/digital section. In fact, the oscillator of Section 4.3.2 has been designed with analog methodologies, while the auto-calibration circuit

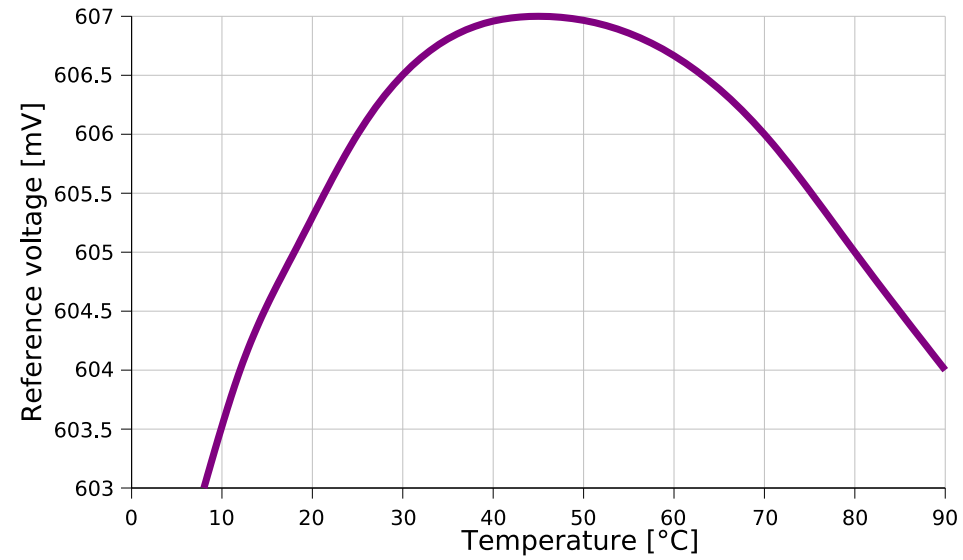

Figure 5.19: Measured reference voltage vs. temperature

has been digitally developed. The characterization focus has therefore been on the ring oscillator; the CK output has been probed with an oscilloscope.

Since the voltage reference and regulator has been proven functional, vdd_reg has been used as supply voltage of the oscillator, better reflecting the actual performances of the chip. The unregulated supply has been provided with a voltage source: the first measurement performed is the determination of the sensitivity of the clock frequency with respect to vdd_unreg, i.e. with the reading distance. Such a parameter is reduced by the voltage regulator, although its PSRR has proven to be not particularly fair.

In fact, results reported in Fig. 5.20 show a variation of 250kHz in the whole 0.8–1.8V range. This means that a very fast movement

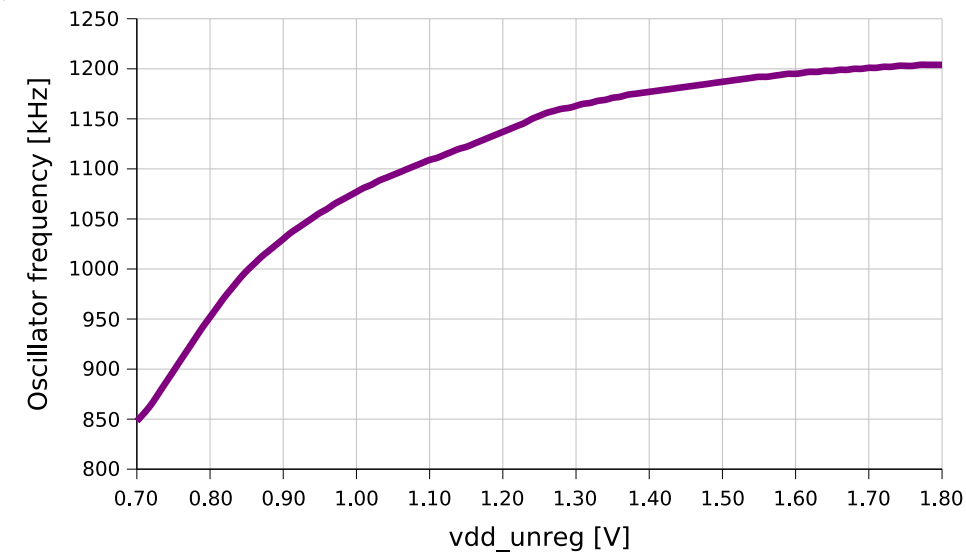

Figure 5.20: Oscillator frequency vs. vdd_unreg

of the tag with respect to the interrogator could cause a timing error; however, in the actual applications the RFID transceiver should not experience a speed higher than few meters per second, that is not enough to exhibit significant variations of vdd_unreg during a packet transmission interval.

The measured clock frequencies are 20% higher than the expected ones. The data provided by the silicon foundry confirmed that the chip belongs to a slightly fast-corner wafer; still, the discrepancy between simulations and measurements exceeds the expectations, and such a difference can be ascribed to the lack of precision in the transistor models. In the final product, a small modification in the transistors size should be made in order to increase the average clock period. Nonetheless, the highest measured frequency is 1.2MHz, not exceeding the overflow limit of the 5-bits counter in Fig. 4.7.

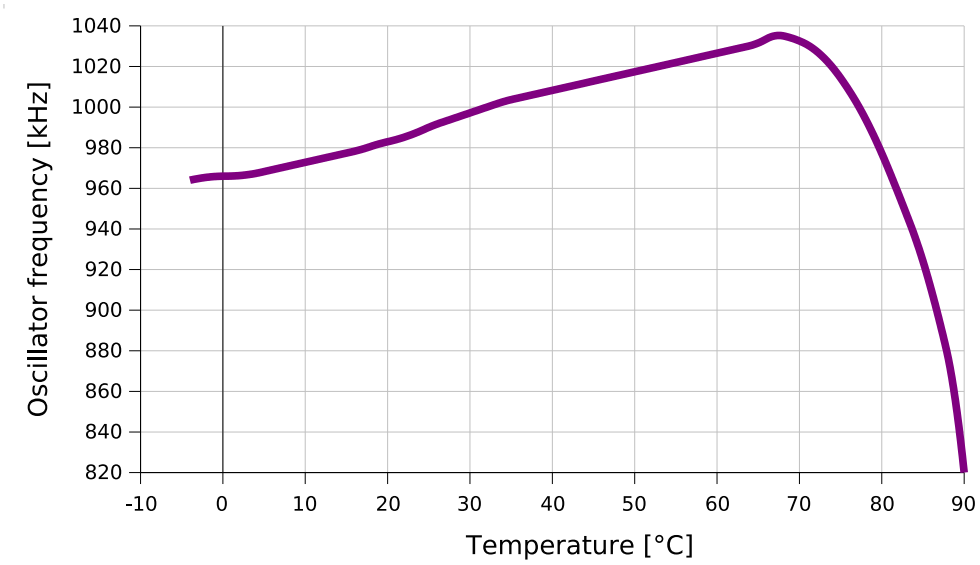

Figure 5.21: Oscillator frequency vs. temperature

The curve of the oscillator frequency vs. temperature is shown in Fig. 5.21. It should be noticed that the characteristic follows the one of the regulated supply in Fig. 5.19, exhibiting a maximum around 70 degrees and then starting to decrease. The drop at high temperatures is quite dramatic, but still f_{ckH} remains in the desired range.

5.5.3 Demodulator and Power-On-Reset

The functionality of the demodulator/CMOS converter (Section 4.2) has been succesfully verified in two tests. The first consisted in feeding a data pattern directly on the $rect$ terminal (without RF signal) and then looking at the CMOS output signal ASK. The unregulated supply voltage and the $rect$ level are set according to the expected values.

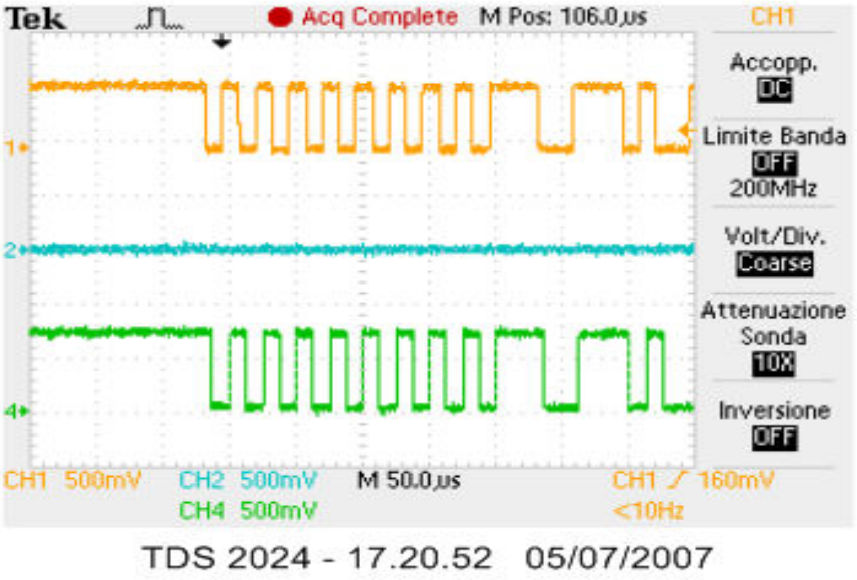

Figure 5.22: Oscilloscope output: input pattern (top) and demodulator output (bottom)

The second test has been done by modulating the RF signal at the chip inputs according to the standard specs and retrieving the CMOS demodulated output ASK. The results obtained for an available power of 0dBm (without matching network) are shown in Fig. 5.22, confirming the correct functionality of the circuit, also for different levels of input power.

As for the Power-On-Reset circuit (Section 4.1), a functionality test has been taken by slowly sweeping up and down vdd_unreg (provided by a voltage source) and looking at the $PORN$ output. Fig. 5.23 reports the results of such a measurement, performed at the ambient temperature: it can be noticed that the vdd_unreg trigger level is around 0.52V as expected.

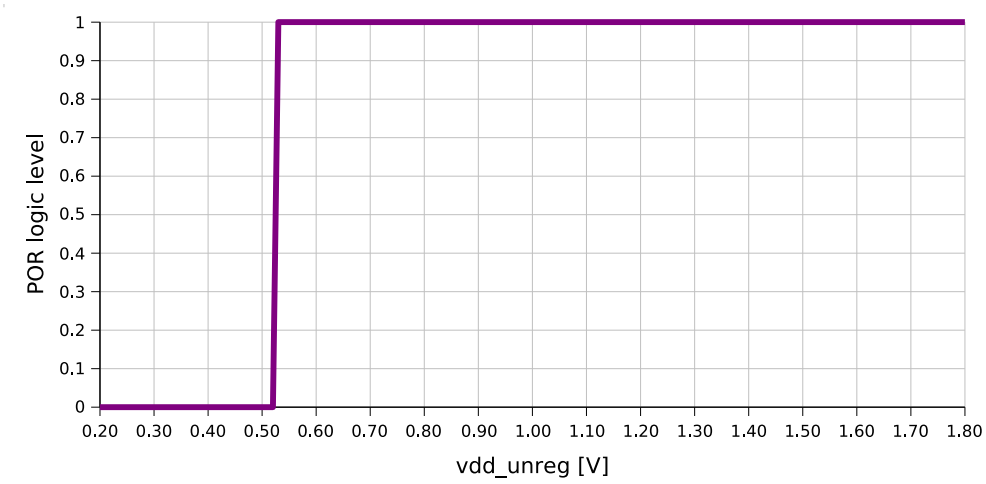

Figure 5.23: Power-On-Reset output vs. vdd_unreg

5.6 Experimental data: whole chip functionality

The last test performed concerns the tag functionality. The analog and digital sections have been connected together, with the core supply tied to the regulator output and all the A/D interface signals (but one) internally generated.

Given the high number of signals to be set and read in such a configuration, the feasibility of such a measurement on the tag with the antenna presents some physical issues. Therefore, the test has been carried out on the packaged testchip with the digital testboard: the input RF pads $in1$ and $in2$ have been connected to a signal generator (without any impedance matching net), with a 869.5MHz carrier and a 40kHz modulating pattern coming from an FPGA. The latter provided also the configuration bits for the digital section, and the padring has been externally powered. The only signal not reported from the digital core to the analog frontend is the answer modula-

tion one, which would cause the antenna shorting for backscattering purposes: in order not to cause a strong impedance mismatch that could damage the RF signal generator, the backscatter switch (Section 4.4) has been kept off, and its driving signal MOD, set to zero on the testboard, has been read on the apposite pad.

The waveforms of the chip signals during a reader/tag facsimile communication are shown in Fig. 5.24. The top waveform shows the would-be backscatter modulation signal MOD, while the middle one depicts the demodulator output ASK: it is worth highlighting the fact that such a signal becomes zero during the answer thanks to the RX bit that turns such a circuit off when no demodulation is needed. In the bottom part, both the unregulated and regulated voltages can be seen: it can be noticed the drop of the former during the answer due to the core activity, while the latter is quite constant during the whole transmission cycle.

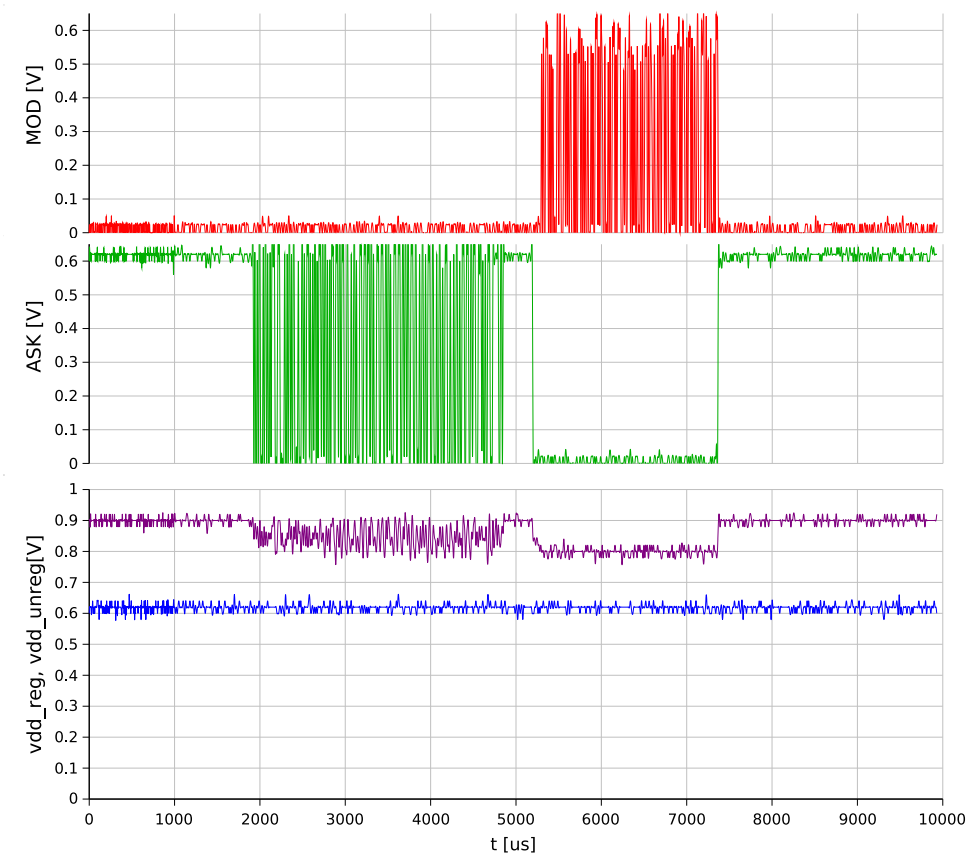

Figure 5.24: Waveforms during a reader/tag communication

Chapter 6

Conclusions

Industries are calling for cheap and secure technologies to reduce the cost of goods stockage, management and control, able to replace mechanisms like bar reading or manual inventory that require considerable amounts of time and personnel resources in checks and objects handling.

Radio-Frequency Identification (RFID) is now a mature technology able to fulfill such a request. An RFID system, composed by an interrogator and several transponders associated to the products to be controlled communicating by means of a wireless network, allows an almost effortless object tracking and management, suppressing at the same time the need for direct optical visibility between reader and tags. Particularly, passive RFID tags which do not carry any on-board battery or power source exhibit a considerable cost shrinking with respect to standard devices: the ability to obtain their supply from the electromagnetic field dramatically reduces the number of expensive on-board components. In their cheapest implementations, they are made up only of a single chip and a receiving antenna.

Further cost reduction techniques have been investigated in this work, analyzing the design of a passive tag family realized with a standard digital technology without any special process option (on the contrary of most reported works) and featuring peculiar solutions able

to avoid the need for trimming at the wafer sort and external components, while showing the same performances of the devices already present in the market.

The power available to the chip exhibits a strong dependency on the inverse of the distance between reader and tag, and can be as low as few microwatts when the latter becomes higher than some meters. Therefore, in order to maximize the reading range achievable with the current electromagnetic emissions regulations and standards, the whole tag has to be carefully designed, starting from the antenna-chip interface, and focusing on the design of an efficient RF/DC power converter. The latter makes use of advanced techniques in order to overcome the limitations due to the absence of expensive technology options; moreover, a supply regulation system based on a novel ultra-low-power voltage reference allows to considerably reduce the dependency on temperature and reading distance.

The presence of such a regulated supply is extremely useful to limit the digital circuits current consumption. Moreover, it suggests the generation of a reference clock able to perform a self-calibration and synchronization with the data received from the reader. This solution, at the price of a very small extra power consumption, allows to avoid the trimming procedure at the wafer sort (that would be otherwise necessary in order to achieve a precision in the transmission data-rate sufficient to fulfill the standard requirements), further cutting the production costs.

Several other circuits have been designed to interface the RF inputs and the digital core of the circuit, aiming at the lowest power consumption in order not to reduce the reading range. Furthermore, in order to test the functionality of the designed blocks, a suitable testchip has been developed, where modularity and apposite solutions allow to characterize either each circuit singularly or the global chip behavior. Measurements have been taken on the tag by means of apposite testboards able to test the chip with or without a package, and some tests have been performed with the chip connected to a matched antenna in order to verify the reading range.

The circuit theory described in this work finds quite satisfactory confirmations in such tests. The goals set at the beginning of the project have therefore been met: a passive UHF RFID tag has been implemented, able to obtain results similar to — or better than — the ones reported in literature, resorting however to a low-cost digital technology and several cost-reduction techniques. The designed transponder exhibits hence considerable advantages in terms of cheapness and realization, and is therefore suitable to be considered a fierce competitor in the emerging Radio-frequency Identification market for goods stockage and control.

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