AUTOMATIC LOOM TEST EQUIPMENT FOR LABORATORY AND PRODUCTION ENVIRONMENTS

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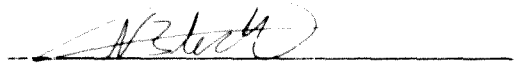
A project report submitted to the Faculty of Engineering, University of the Witwatersrand, Johannesburg, in partial fulfilment of the requirements for the degree of Master of Science in Engineering.

Johannesburg, 1986.

DECLARATION

I declare that this project report is my own, unaided work. It is being submitted for the Degree of Master of Science in the University of the Witwatersrand, Johannesburg. It has not been submitted before for any degree or examination in any other University.



10TH day of DECEMBER 1986.

ABSTRACT

Cables (two or more wires within a single covering) and looms (an assembly of discrete wires) require testing after fabrication to ensure continuity between desired points, the absence of short circuits, adequate insulation resistance, and undamaged insulation. Today's users require systems which have higher test speeds, expandability, easier programming and lower cost.

A market investigation of the automatic loom testers available today, shows that there is no inexpensive solution. With the rapidly growing demand for loom testing facilities, the need for a new, fully functional, low-cost automatic loom tester has arisen. Due to the many forms that such testers take (i.e. varied packaging, node capacity etc.) the design presented here concentrates on an open-ended approach, the aim of which is to develop and prove technologies which satisfy the various loom testing philosophies of interest.

Three expandable modules have been developed, namely the GO/NO-GO, QUALITY, and CENTRAL PROCESSING UNIT cards. On this basis, a customer can configure an automatic loom tester to satisfy the needs of his particular environment.

To my wife

Shelee

ACKNOWLEDGEMENTS

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NOMENCLATURE

ADC	-	Analogue to Digital Converter
ATE	-	Automatic Test Equipment
BCD	-	Binary Coded Decimal
BJT	-	Bi-polar Junction Transistor
CAD	-	Computer Aided Design
CMOS	-	Complimentary Metal Oxide Silicon
CPU	-	Central Processing Unit
DC	-	Direct Current
DDR	-	Data Direction Register
DIP	-	Dual In-line Package
EPROM	-	Erasable Programmable Read Only Memory
FET	-	Field Effect Transistor
GND	-	Ground
HP	-	Hewlett Packard
I/O	-	Input/Output
IC	-	Integrated Circuit
LC	-	Liquid Crystal
LED	-	Light Emitting Diode
MPU	-	Micro-Processing Unit
MTBF	-	Mean Time Between Failures
OA	-	Operational Amplifier
PCB	-	Printed Circuit Board
PIA	-	Peripheral Interface Adapter
PPI	-	Programmable Peripheral Interface
RF	-	Radio Frequency
ROM	-	Read-Only Memory

SIP	-	Single In-line Package
TTL	-	Transistor Transistor Logic
UUT	-	Unit Under Test
ZIF	-	Zero Insertion Force

1 INTRODUCTION

Cables (two or more wires within a single covering) and looms (an assembly of discrete wires) require testing after fabrication to ensure continuity between desired points, the absence of short circuits, adequate insulation resistance and undamaged insulation.

Today's equipment supplies reveal that users are seeking systems with higher test speeds, expandability, easier programming and lower cost. A typical listing of user requirements includes:

- programming for a known good unit under test;
- download capability;
- simple operation;
- reliable tests for high impedance shorts;
- simplicity of interface with the unit under test.

Users are also becoming more aware of problems created by leakage between conductors, leading to damage of voltage-sensitive solid-state, devices such as CMOS. In addition, any excessive resistance caused by the cable or loom can reduce the small voltages used in today's systems to non-usable levels.

The recent electronic revolution has seen an abundance of new devices and systems. In order for the many modules which comprise a system to communicate, a transport mechanism must exist. These interconnection networks are made available by groups of wires called looms. Determining the state of these looms is possibly the most important check in an electrical system.

1.1 Loom Testing Environments

The majority of loom testing is aimed at verifying continuity between termination points and detecting short circuits. Short circuits can either be caused by a dir[illegible]wire, a bare wire contact, or a high impedance sh[illegible]t through low resistance insulation.

The broader spectrum of testing philosophies can be broken down into three distinct categories:

- go/no-go testing;
- power-line testing; and
- hi-pot testing.

1.1.1 Go/no-go testing

When testing a loom or a loom/motherboard combination, it is important to know whether all the wires or PCB tracks are in their correct position, with no variations (additional short and/or open circuits). This requires a cross-checking technique where each wire is tested with respect to every other wire. This domain of testing concentrates on continuity and insulation resistance tests.

Continuity tests will show if there are circuit breaks or high resistances present. The tester is programmed to verify each connection according to the desired continuity pattern and maximum allowable resistance.

Insulation resistance tests can detect short circuits between adjacent wire runs. A voltage is impressed in sequence on each wire run and all other runs are monitored for possible short circuits by measuring and verifying an acceptable resistance level. High impedance short circuits can be detected using this technique.

1.1.2 Power-line testing

Due to specialized or military requirements, it may be necessary to determine the resistance, at some rated current, in a particular wire. If the resistance exceeds a certain upper limit, say 500 milli-ohms for example, the functionality of a system may be affected.

This increase in resistance, could cause undesirable current limiting or create an unwanted voltage divider. This test philosophy plays a vital role in the investigation of areas such as the quality of pin joints and the condition and type, of wire used. Defects of this type, namely a few severed wire strands or a poorly crimped pin joint, involve resistance variations in the milli-ohm region.

1.1.3 Hi-pot testing

When working in higher voltage environments it might be necessary to check the isolation properties of cables and looms. Hi-pot tests are performed to detect cracked or pinched insulation. The impressed high voltage will arc whenever an air gap or insulation discontinuity exists.

1.2 Practical Loom Testing Considerations

Although the smaller percentage of cables and looms are tested using the Hi-Pot and Power-Line testing techniques, these techniques are extremely costly. They require precision analogue and high voltage modules, involving high quality relays, expensive ADCs, and transformers.Depending on the thickness and length of a particular wire, continuity implies an extremely low resistance; usually below a few ohms.

Discontinuity on the other hand, implies a high resistance, somewhere in the mega-ohm region. Rarely would the case arise in which a wire represented a resistance somewhere between these boundaries, of continuity and discontinuity.

Over a period of two years in production using a few designs involving loom and motherboard test equipment for entire systems, the following 'real' faults were found:

- wires placed incorrectly;
- wires omitted or too many wires inserted;
- broken wires or tracks;
- short circuits due to solder splashes;
- short circuits due to damaged insulation;
- poorly crimped pin joints causing intermittent faults;
- oxidized solder, resulting in discontinuity.

Apart from the occasional need for a precision resistance test, it appears that the go/no-go test approach more than satisfies the general cable and loom testing requirement; the basic idea being the verification of a particular short circuits/open circuits pattern. Setting a specific resistance threshold, say 10 milli-ohms or 100 mega-ohms, where any value below 10 milli-ohms would indicate a short circuit and any value above 100 mega-ohms would indicate an open circuit, would have no meaningful advantage over a technique which does not define a rigid threshold. Test implementation using digital measuring techniques would be the logical path to follow, as it would enhance test equipment measurement speed, cost, size of the equipment and reliability.

1.3 Market Investigation of Loom Test Equipment Currently Available

Cable and loom test equipment ranges from large console systems to bench-top testers. The larger systems are primarily designed for testing backplane wiring and bare PCBs, although all bare board and backplane testers are also adaptable for testing cables and looms. One of these larger systems is not suitable for cable and loom testing applications because .... Smaller systems, often referred to as bench-top testers, with emphasis on or specially designed for, cable and loom testing are available.

The larger systems are nevertheless being widely used for cable and loom testing in conjunction with their primary function of testing complex interconnected assemblies such as multi-layer PCBs and wire-wrapping backplanes. The use of these sophisticated testers for loom testing has meant a considerable increase in the quality of looms.

In general, the type of loom to be tested will determine the size of the test equipment required. For small cables, such as those for consumer and commercial markets, interconnection accuracy is the main concern. Test requirements for these applications can be satisfied by a small solid-state switching test system. However, for an application such as satellites or missiles, test equipment can be required to test as many as 100 000 terminations and more intensive testing can be required. Larger test systems having greater test-point capability and high voltage switching will therefore be required.

One of the most difficult problems in loom testing is building the interface. If the user does not ensure the integrity of the interface between the tester and the loom, more time will be spent testing the interface than testing the assemblies. The interface consists of a mating connector and a harness assembly for connection to the tester.

A broad range of loom test equipment that can fulfil testing requirements ranging from simple flat cable jumpers to complex aircraft looms exists. The application will determine the capabilities of the test equipment needed. The testers to be discussed include large systems for testing bare boards, backplanes and those systems designed specifically for loom testing.

1.3.1 Hewlett Packard 3060A

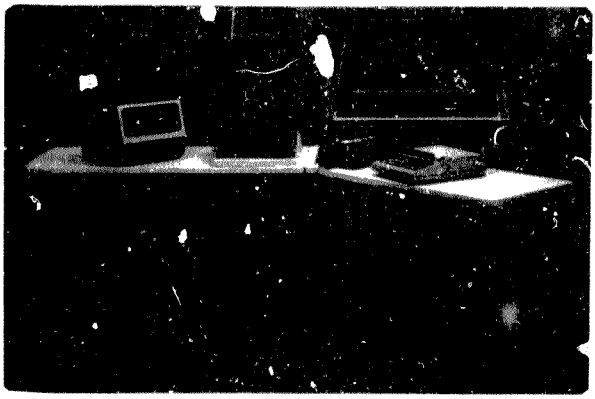


Figure 1.1 Hewlett Packard 3060A loom tester

The 3060A Board Test System has been designed for automatic PCB testing. The system is capable of performing advanced in-circuit component tests, and board-level functional stimulus/response tests. The in circuit component testing technique uses short circuit/continuity testing for the direct isolation of short circuits caused by solder and other process problems.

The user may select a threshold level for defining a short circuit or an open circuit which can be selected between, 5 ohms and 125 kilo-ohms. For example, if the system were used to test blank boards, one might encounter plating growths of several hundred ohms to several kilo-ohms. To detect these, the threshold level can be set at some value that would show a shorted node (with the ohm value below the threshold value) for those nodes that fit into the plating growth resistance range.

Basic hardware description

The 3060A short circuit/continuity test employs a basic resistance measurement technique, illustrated in Figure 1.2.

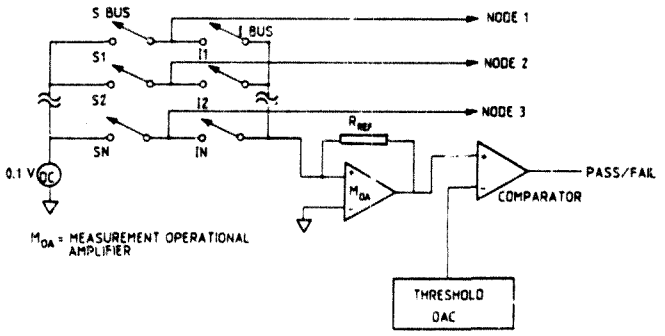


Figure 1.2 Short circuit/continuity functional diagram

The short circuit/continuity test uses a reference array with a specified threshold to determine the result of each node-to-node check. The reference array is generated by a test on a board which is known to be good. The result of the test (i.e. shorted pairs) is stored in a data array. If a shorted pair detected by the short circuit test is not found in the data array, an error message is printed out. After all the pairs have been tested, the shorts test uses the data array to perform an opens test. The opens test is conducted only on the known shorted pairs in the data array. If any pair is detected as an open, an error message will be printed out.

Both the reference array and shorts test perform the same basic relay closures during their execution. The test first closes a relay on the I-bus (assume I_1) and then closes S_2 through S_N (N is the total number of nodes) relays on the S bus. A measured impedance (parallel combination) less than the threshold level signifies a short. If a short is found, the next step is to make a node-to-node search for the short. This is done by closing the I_1 relay and only one of the S-bus relays at a time beginning at S_2 in this example. A simple measurement sequence without any shorts will take ten milliseconds per node, or for a full system (512 nodes), it would take 512 x (0,01 s) which is equal to 5,12 seconds. This feature of the Shorts/Continuity Test contributes to its reading rate. Unless a shorted node is initially indicated, only one measurement is made per node (i.e. one I-bus relay closed to all S-bus relays). Only when a short is indicated does the system compare a specific I-bus relay to each S-bus relay individually.

Cost implications

The 3060A, or its upgraded model, costs approximately R300 000. Apart from its size, it is not very effective from a continuity and insulation resistance test point of view. Another drawback is the expensive interface needed to communicate with the 3060A.

The I/O part consists of a 700-paddle-pin matrix bed. When interfacing a particular UUT or a set of UUTs, the following items would be required:

a. a patch-panel base matrix to house the patch pins needed to make contact with the controller bus terminations;

b. a box enclosure, housing mating connectors and harness assemblies for connection to various units under tests;

c. patch pins.

Figure 1.1 illustrates the machine and interface.

The cost of a complete patch-panel box including labour and materials, could range anywhere between R5 000 and R10 000. At R4 per patch pin and R2 000 per patch-panel base it can be appreciated that this price is unrealistic.

1.3.2 Wayne Kerr A8000

The Wayne Kerr A8000 is a fully functional printed circuit board tester, modelled very closely on the HP 3060A. The in-circuit testing techniques allow for continuity testing on both bare and assembled printed circuit boards and wiring looms. The demarcation value of resistance between a short-circuit and an open-circuit can be established anywhere between 5 and 50 ohms.

The test equipment is priced at about R100 000. Again, from a continuity and insulation resistance test point of view the price of the loom tester cannot be justified. This equipment also has a high-cost interface mechanism.

1.3.3 Olivetti WPV58

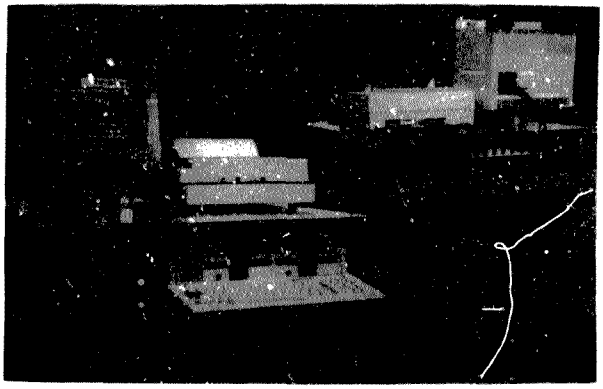


Figure 1.3 Olivetti WPV58 loom tester

The WPV 58 is a wiring pattern verifier which provides testing of wiring looms, back panels and interconnection cables. The test is based on continuity and insulation tests, executed on the device under test. The results of these tests are then compared with test data from a known good assembly acquired during the auto-learning procedure. A reading of less than 200 ohms indicates a short circuit, and a reading of more than 1 megaohm indicates an open circuit.

The system consists of the following units:

Master unit. The master unit includes:

- a processor;
- a keyboard;
- a crt (video);
- a printer;
- an I/O interface;
- a measuring unit;
- a scanner unit (up to 8192 channels);
- a connector panel (8192 ways).

First slave unit. The first slave unit includes:

- a scanner unit (from 8193 to 16384 channels);
- a connector panel (8192 ways).

Second slave unit. The second slave unit includes:

- a scanner unit (from 16385 to 24576 channels);
- a connector panel (8192 ways).

The system hardware architecture is illustrated in Figure 1.4.

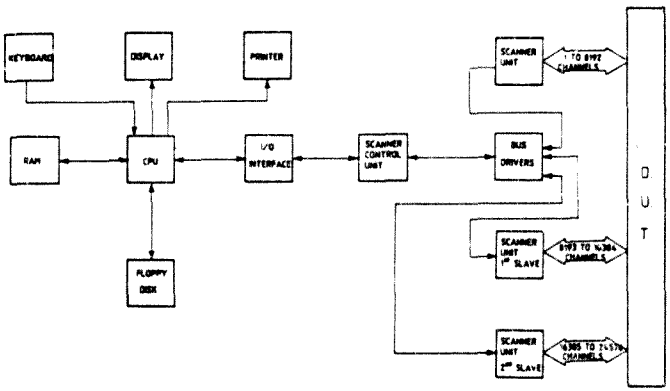


Figure 1.4 Block diagram of MPV58 system hardware

Test techniques

The integrity of the interconnection network of the unit under test is tested by means of continuity tests and insulation tests. Refer to Figure 1.5 for the general test method.

Continuity testing. The continuity test of a network is carried out by connecting one point to a measurement voltage and another to the ground.

The presence or absence of current at a defined comparison level will detect the existence of the continuity between the selected points.

The test is extended to all the points of the network.

Multipoint insulation testing. The insulation test among two or more points (or networks) is carried out by connecting a point to a reference voltage and the others to ground.

The presence or absence of current at a defined comparison level will detect the existence of an insulation error between the point concerned and one of the other points.

If an error occurs, the tester proceeds to verify, by the point to point insulation test, the whole group of points to detect the short circuited ones.

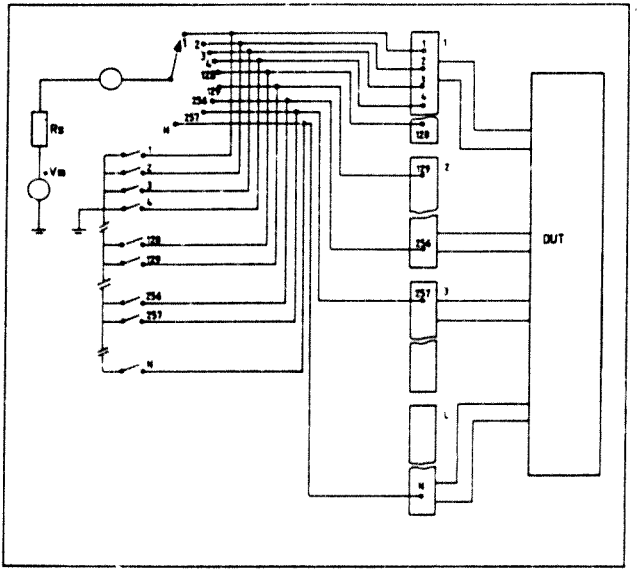


Figure 1.5 General test method

Units under test communicate with the test equipment via banks of 128-pin Zero Insertion Force (ZIF) connectors, creating a fairly economical and reliable interface.

The operator/system interface is extremely user-friendly, featuring:

- editing capabilities that make it possible to modify the test programs generated, using the computer keyboard. This also applies to hand-programming as opposed to self-programming using a known good assembly;

- input capabilities, where a list of the assembly wiring is entered into the computer and the tester is allowed to generate a test program based on this wire list;

- printout capabilities, where diagnostic messages are printed during test time, without stopping the test;

- memory capacity, where several test programs can be stored on a single floppy disk.

The use of a computer as a system controller provides exceptional software features that meet varied and demanding requirements. With a test capacity of up to 24 576 channels, the WPV 58 can grow, simply and quickly as needs expand, with the minimum of downtime.

Although the Olivetti loom testing system has many capabilities, it costs about R100 000.

1.3.4 Cablescan AHT-200

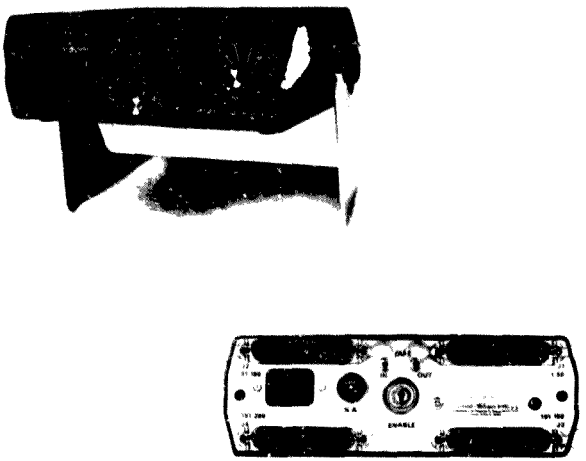


Figure 1.6 Cablescan AHT-200 loom tester

The AHT-200 memorizes point-to-point and multip'e circuit connections of an existing cable or harness. This memory is then retained in the unit when any number of additional assemblies are monitored and tested. To input memory, a properly wired assembly is connected, the mode switch is set to LEARN, and the START button is pressed. After a few seconds the PASS light will come on, indicating that the AHT is programmed and ready to monitor or test. The AHT-200 can be used either as a continuity monitor or an automatic tester.

A continuity monitor

Once a good cable is memorized, the AHT can assist in the wiring of assemblies when the mode switch is placed in the MONITOR position. Any attempt to miswire while assembling the loom will be signalled by both an audio and visual display. A short circuit condition will also cause an audio and visual indication, and the two point numbers which are short circuited or miswired will be displayed.

An automatic tester

A complete loom is interconnected to the AHT and the mode switch is set to TEST. The unit checks point-by-point and multiple connections against its memory and signals with the PASS light if the wiring is correct. If the wiring is not correct, a missing or poorly connected wire will be indicated by the OPEN light and the flashing of two point numbers which are connected. If additional errors exist, they will be detected as soon as the first has been corrected, or the START button has been pressed to advance the test. The AHT can feed its memory to the cassettes of ordinary tape recorders. Learning tables can then be stored while the AHT is used to monitor or test differently wired looms.

General specifications

Capacity	: 299 points maximum;
Operating speed	: less than 40 seconds;
Sensitivity	: short circuit: less than 1 kilo-ohm indicates a short circuit; open circuit: more than 10 kilo-ohms indicates an open circuit;
Display	: 11 mm LED numeric display: LED indicators for PASS, OPEN, SHORT;
Size	: 27 x 21 x 9 cm excluding handle;
Interface	: four 25-way D-type connectors.

When using small solid-state switching measurement techniques, the above sensitivity has no meaningful significance, as previously discussed. The price of this automatic tester is approximately R6 000.

1.3.5 Cablescan EHT-4000A

Figure 1.7 Cablescan EHT-4000A

The EHT-4000 A performs basically the same functions as the AHT-200, with the following improvements:

- on-board storage cassette facility;
- a maximum capacity of 2 048 points;
- external CRT te.minal and printer connection facilities.

With a printer option, a hard-copy of test results can be obtained. This type of recorded proof is usually required in most test departments.

The CRT connection option is most valuable for creating and editing test programs. The system uses customer notation (up to eight characters per point) for point identification, with no need to cross-reference to a special tester point number list.

This bench-top tester includes a continuous scan feature for intermittent faults. Intermittent shorts or open connections caused by vibration, temperature extremes, etc., are readily detected while the assembly is subjected to the suspected position. The EHT will repeatedly test all connections until an error is detected, at which time it will display the type of problem and the point numbers involved.

The test point capacity can be expanded to 2 048 in the mainframe, by the insertion 128-point scanner boards. By adding another card frame, namely Extension Module, a total of 4 096 points can be achieved.

The EHT has an on-board 20-character alpha-numeric display, coupled to a dedicated, but limited membrane keypad. The cost of this piece of automatic test equipment is about R10 000:

- R2 000 for the Extension Module card frame;
- R700 for each 128-point scanner board.

Market Investigation; conclusion and recommendations

Although automatic test equipment such as the Hewlett Packard 3060A or the Wayne Kerr A8000, already exist in the organization, they were never designed for intensive loom testing applications. Even though they can be tailored to meet such conditions, their UUT to ATE interface mechanism involves high cost; no more than one or two of these expensive systems could therefore be purchased. This eventually lead to work loading problems which hampered the production flow rate.

On the other hand, the Olivetti WPV 58 wiring pattern verifier, although very powerful, is extremely expensive. Only in areas where backplane and loom assemblies comprising thousands of wires have to be tested, would such a machine really be required.

Only the 'low cost' bench-top automatic loom testers, costing between R6 000 and R15 000 remain. Equipment such as the Cablescan AHT-200 and the EHT-4000A, already described, fall into this category.

These testers offer attractive features such as:

- digital measuring techniques, which enhance measurement speed;

- small light-weight modules, making it possible to have portable units;

- printer and CRT terminal connection capabilities (only the EHT-4000A).

Due to poor exchange rates for the South African Rand, and the uncertainty of state exchange rate, and the possible imposition of sanctions, it would be expensive as well as risky to rely on any particular supplier to meet future loom testing equipment needs.

It was thus recommended that the Company develop and standardize on its own bench-top automatic loom tester. It was thought that, with cost in mind, such a tester could find its way into every relevant laboratory or production line. The idea was to produce a portable stand-alone unit, incorporating many of the above-mentioned features, at a manufacturing price of well below R1 000.

1.4 Proposed Design

1.4.1 Proposed design specification

The following specification typifies the standard loom tester to be developed. However, specialized user application requirements as well as future upgrading, will see an eventual growth in this baseline specification.

Function

The proposed tester tests for gross short circuits and open circuits in looms, and compares each node with every other. It tests wire and pin joints for quality and measures the resistance in any particular node-to-node link.

Functional specifications

The proposed tester has more than 300 nodes which can be tested in less than 30 seconds. It has approximately 20 quality measurement paths with a quality resistance threshold of less than 500 milli-ohms.

Functional characteristics

The proposed tester has the ability to learn from a good loom; it can present a simple pass/fail output or give a node list showing the actual error pattern found; the learnt test pattern can also be printed out; it has a continuous scan feature for detecting intermittent fault conditions.

Cost

The cost to produce the proposed tester is approximately R800 per unit.

Other considerations

Other considerations were that hard output should be from either an internal printer or an RS232-C or parallel interface to a separate printer; that test pattern storage should be in the form of some removable medium, for example, an EPROM cartridge similar to that used on video games; that the tester should work off mains or battery power; and that the MTBF should be greater than 3 000 hours, should not need to be proven, and that this would become evident during use.

1.4.2 Proposed design outline path

From a Kentron point of view, the continuity testing environment concerned, covers two major areas:

Short and open circuit testing of looms, comparing every node with every other (this technique basically checks a loom according to its latest interconnection diagram); and quality testing mode in which precision resistance measurements can be made on any chosen wire, providing information on the quality of pin joints, wires, etc.

Due to the many variations that an automatic loom tester can have, the idea would be to go for a more open-ended, bottom up type approach. This allows areas such as node capacity, packaging and user interfacing to be easily upgraded without changing the baseline test concepts of the machine.

The idea was to develop and prove a technology which satisfied the continuity testing environments concerned. As a start, a from user interface point of view, the standard model consisted of a panel of switches and LEDs, indicating modes and results. An RS232-C serial port initially provided a facility for hard copy printouts of the diagnostic results required. This communication link may further be upgraded allowing terminal connection, hence offering full editing and documentation facilities.

The initial packaging was a Euro-card rack, confining the design approach to independent card modules. Basic cards would be developed:

- a go/no-go card, satisfying short and open circuit testing, comparing every node with every other; and

- quality card testing which would implement precision resistance testing down to milli-ohm regions;

- a CPU card which would provide the processing and communications link between user interfaces and the measurement cards; and a

- power unit module which would comprise a 5 Volt, 3 ampere micro-computer power supply as well as an intelligent Nicad battery charger. Nicad batteries would be used to provide the option of tester portability.

The system node point capacity can easily be expanded by simply connecting any number of measurement cards in a chain. User input/output device upgrading such as NEAR-ASCII membrane keypads, LC displays, RS232-C terminal connection, etc., can be achieved with minimal CPU card hardware and firmware expansion. A particular customer might require a smaller stand-alone portable automatic loom tester. By changing the packaging, a hand-held housing with a combination of the standard card modules or a subset thereof, could easily be achieved.

2 TECHNICAL DEVELOPMENT AND IMPLEMENTATION OF THE GO/NO-GO TEST PHILOSOPHY

The functionality of the proposed automatic loom tester includes two distinct measurement philosophies:

- The go/no-go testing environment, which checks looms according to data obtained from known good assemblies. The short and open circuit point testing is carried out by comparing every node with every other.

- The power line or quality testing environment, where precision resistance measurements can be made on any chosen wire, providing information on the quality of pin joints, wires, etc.

Go/no-go testing, will be performed by a rack card known as the go/no-go measurement card. Another rack card known as the quality measurement card will facilitate all power-line testing requirements.

2.1 Development of the Go/No-go Measurement Card

Test requirements for this type of application can effectively be satisfied by a small solid-state switching test system. Focussing on speed, size and space, the answer would be to opt for a digital design, for example, using the following simple measuring technique.

Consider a measurement board having 'n' input/output port bits, (1, 2, 3, 4, (n-1), n). Place a logic 'low' test bit on port bit 1. All the other port bits are kept at a logic 'high'.

At the time, with respect to the microprocessor, that port bit 1 is configured as an output containing a low potential, whereas the other port bits are all configured as inputs containing high potentials. Once connecting the UUT, i.e. the loom, to the measurement system, the MPU will then proceed to read the logic levels on each of the port bits configured as inputs. Any low potential will then imply a short between port bit 1 and the input port bit currently being read.

These so called port bits will commonly be known as nodes. Any termination on a loom or cable will represent a node, thus each wire is considered to contribute two nodes to the nodal count. This type of technique will enable individual nodes to be cross-referenced with all other nodes in the test set. After all the nodes have been cross-checked with every other, a comprehensive short circuit/open circuit table describing the wiring layout of a particular loom is generated.

Figure 2.1 demonstrates the basic building block needed to implement this go/no-go nodal test scan.

Due to the initial complexity portrayed by this concept, the I/O port configuration is best explained by means of a practical example.

Connect the loom shown in Figure 2.2 to the I/O port bus PDO-PD7. All loom termination points are divided into node numbers. Since the short/open circuit test building block shown in Figure 2.1 is byte-wide only, we chose our loom to have eight termination points.

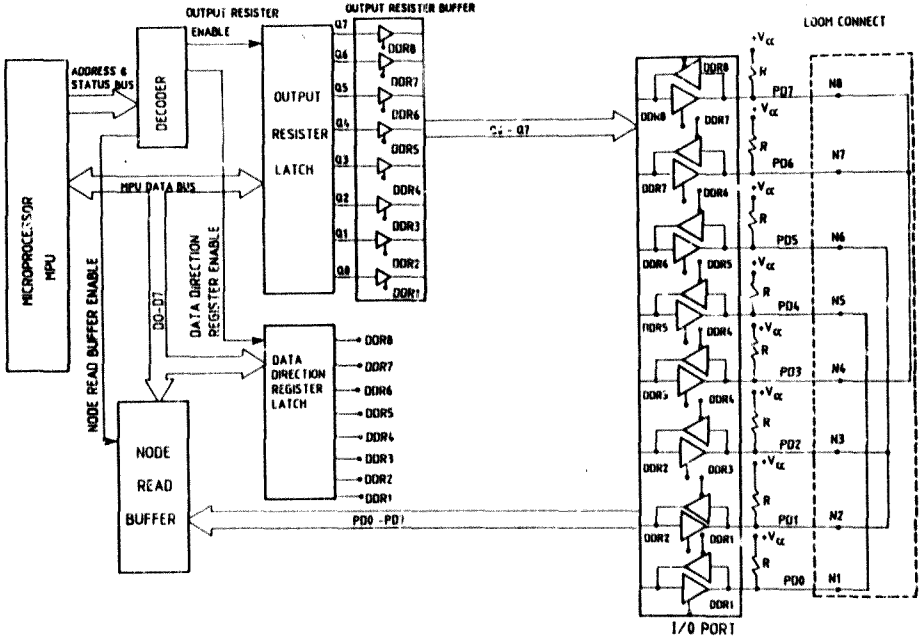


Figure 2.1 An eight-bit short circuit/open circuit go/no-go test block

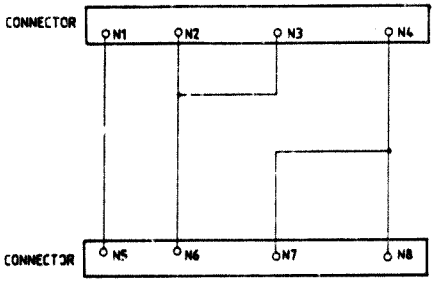


Figure 2.2 Loom interconnection diagram

Refer to both Figures 2.1 and 2.2 for the following explanation. The I/O port buffer lines must be configured as inputs or outputs. This is done by latching the required byte into the data direction register, via the MPU. The MPU address and status buses activate the decoder, enabling the Data Direction Register (DDR) latch. The byte currently stored in the MPU's accumulator is transferred via the data bus to the DDR latch. In this case, since node N1 will generate the first test bit, the byte stored in the accumulator will be 00000001. The lowest significant bit D0 corresponds to latch bit DDR1. Thus I/O port lines PD1 to PD7 are configured as inputs, whereas only line PD0 is configured as an output. By examining Figure 2.1, this logic can be verified.

Due to the pull-up resistors R, all input port lines represent a logic 'high'. In order to define the logic level of port bit PD0, the current test port bit, the output register latch must be initialized. The MPU enables the output register latch via the decoder and transmits the required byte. All the output register buffers except that corresponding to latch bit Q0 are tri-stated. This implies that all latch bits except Q0 are 'don't cares.' Byte XXXXXXX0 therefore generates the required test port bit, causing N1 to sit at a logic 'low'. Any other node connected to N1, due to the insertion of the loom, will now measure logic 'low'. Those nodes, (loom terminations), not shorted to N1 will remain in their normal pulled-up state.

In order to obtain this information the logic levels present at the nodes (N1 to N8) must be read and deciphered by the MPU. This is accomplished via the Node Read Buffer. The MPU enables this buffer by means of the decoder, then latches the byte into its accumulator after which the information is processed internally.

In the example provided, node N5 is shorted to N1, thus the port bit PD4 becomes a logic 'low'. All the other port bits remain in their pulled up 'high' state. After the Read Node Buffer cycle is executed, the following byte

D7D6D5D4D3D2D1D0 = 11101110

will be found in the accumulator. Data bit D4 corresponds to I/O port bit PD4 which in turn corresponds to loom termination node N5. Since node N1 generated the test point bit, it can be safely said that the loom terminations represented by N1 and N5 are shorted together. At a higher level, nodal information can be directly converted into connector pin notation.

Repeating the same procedure for N2, port bits corresponding to node N1, N3, N4, N5, N6, N7, or N8 are configured as inputs. Whereas the port bit representing node N2 is configured as an output, generating the logic 'zero' test point bit. After the Read Node Buffer byte has been read, the byte 11011001, can be found in the accumulator.' Following the same pattern just described, it can clearly be seen that nodes N2, N3 and N6 are all shorted together. All the other nodes are considered to be open with respect to N2.

Thus, after allowing each node to individually generate a logic 'low' test point bit, relative to all the other nodes, a complete short circuit/open circuit pattern duplicating the looms' interconnection configuration will be generated. In order to increase measurement speed the inherent redundancy found in this type of measurement technique would have to be removed. Going back to the loom under test in this example, cases of this redundancy can be seen. For example, once it is determined that node N2 is shorted to both N3 and N6, these nodes can be removed from the test bit generation list. This would otherwise produce identical but converse information, resulting in a waste of time. The solution to this problem is best handled by the firmware, to be discussed at a later stage.

2.1.1 Available technology

In order to compare various technology options from a space, and cost-effectiveness point of view, some broad specification must be set. As a start, it is assumed that the measurement system can test up to 240 nodes, implying a maximum capability of one loom with 240 termination points at a time. In some looms, or loom motherboard combinations, many points may be tied together. Radio frequency-type work, where every signal might have its own ground return path, is a typical example. These ground return paths are eventually all brought together causing a large number of nodes to be tied together. Some caution should be taken to ensure against these loading problems, which ultimately cause logic level corruption. If a measurement system has such effects, the entire measurement system can be rendered useless when testing certain types of loom.

This first approach is to design the eight-node short circuit/open circuit test building block from discrete small-scale integration CMOS or TTL chips. From Figure 2.1 it can be seen that a minimum of ten individual IC chips are required to configure this basic measurement block.

It is important that the individual buffers constituting the I/O Port and Output Register Buffer, each contain separate I/O and tri-state control lines respectively. Basically, seven tri-state buffers, two 8-bit latches and one decoder are required. If this form of technology were to be used to produce the 240-node test board, a total of 300 chips would be needed. Although a worthwhile starting point, the solution is far from practical, especially from a cost and space standpoint.

The next step is to find a chip that incorporates the entire eight-bit short circuit/open circuit test building block. A logical direction to follow, would be to source some type of programmable, peripheral interface chip. The Intel 8255 Programmable Peripheral Interface (PPI) is one such option that might satisfy the requirement. The 8255 is a general-purpose programmable I/O device. It has 24 I/O pins which may be individually programmed in two groups of twelve, and used in three major modes of operation. In mode 0, being the only mode of relevance, each group of twelve I/O pins may be programmed in sets of four to be inputs or outputs.

Operating in mode 0, a designer has a 24-bit, I/O port at his disposal. This effectively incorporates three 8-bit short circuit/open circuit building blocks in a single forty-pin package. Using this set-up, only 10 of these 8255 PPI would be required to implement the 240-node measurement system. This technique is basically the ideal choice, however it does not meet all the requirements necessary to simulate the principles of the short circuit/open circuit measurement block shown in Figure 2.1.

In order to test individual nodes with respect to all other nodes, obtaining a complete short circuit/open circuit pattern, it is essential for all the I/O port lines to be individually programmed as an input or an output. The PPI 8255 does not allow for this vital ingredient, at best allowing ports to be programmed as inputs or outputs in sets of four only.

Another similar type of chip is the Signetics 6521 Peripheral Interface Adapter (PIA). This device has two 8-bit bi-directional peripheral data buses and four control lines. The functional configuration of the PIA is programmed by the MPU during initialization. To meet the 240-node measurement requirement, 15 of these 6521 PIAs are needed. Although the chip count is 30% larger than in the PPI 8255, each of the I/O lines can individually be programmed to act as an input or output. The only area left for investigation is node loading, i.e. the number of nodes that can be shorted together at one time without causing logic level corruption during the measurement cycle. The two 8-bit bi-directional ports provided by the PIA 6521 are referred to as the 'A' side and the 'B' side. The peripheral 'B' I/O port buffers are push-pull devices as shown in Figure 2.3.

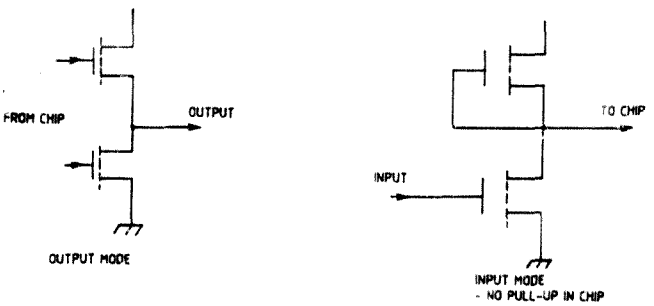


Figure 2.3 Peripheral I/O port 'B' buffer

When the I/O lines are programmed to act as inputs, the output buffer enters the high impedance state. These inputs will have an impedance of greater than one mega-ohm.

The DC characteristics of this port are listed below:

- input leakage current (I_{1H} and I_{1L}) = 10,0 µA;
- input 'high' voltage V_{1H} = 2,4 V;
- input 'low' voltage V_{1L} = 0,4 V;
- output 'low' current I_{OL} = 1,6 mA;
- output 'high' current I_{OH} = 100,0 µA;
- output 'high' voltage $V_{OH(min)}$ = 2,4 V;
- output 'low' voltage $V_{OL(max)}$ = 0,4 V.

Assuming all the I/O ports have the same DC characteristics as port B. Taking the passive pull-up resistors needed in the output stage of the measurement block, the maximum allowable number of nodes that can be tied together can be calculated. Since the minimum output level of a logic 'high' state is 2,4 V, and taking a maximum input leakage current of 10 µA into account, a pull-up resistor value of 220 kilo-ohms is chosen. This basically ensures the integrity of the high-level state under all conditions.

W[illegible] bit in the output mode (the test node) and 'n' the input mode (the referenced nodes), the maximum al[illegible]ber of shorted nodes can be determined (refer Figu[illegible]

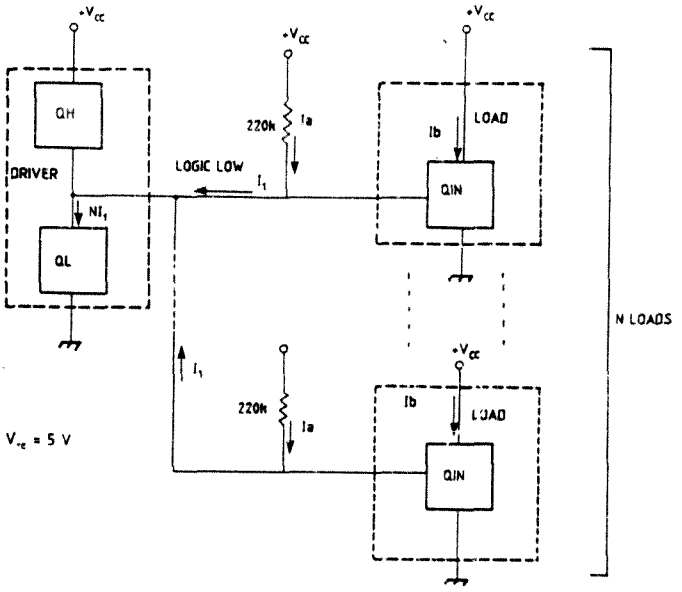


Figure 2.4 Port bit loading

I_1 = load and resistor leakage currents;
assume V_{OL} = 0,4 V;
$\therefore I_a$ = (5 - 0,4)/220 k = 20 µA;
thus I_1 = 10 µA + 20 µA = 30 µA.

From the DC characteristics list, it can be seen that the maximum driver sink current before logic level corruption occurs, is 1,6 mA.

The maximum node number n therefore = $\frac{1,6\ mA}{30\ mA}$ = 80 nodes.

Although this limit might prove to be acceptable for many of the looms under test, it can impose serious restrictions on the flexibility of the system as a whole. This will most certainly become evident when the loom tester is to be upgraded to handle fairly large looms.

The buffers which drive the peripheral 'A' I/O port contain passive pull-ups as shown in Figure 2.5.

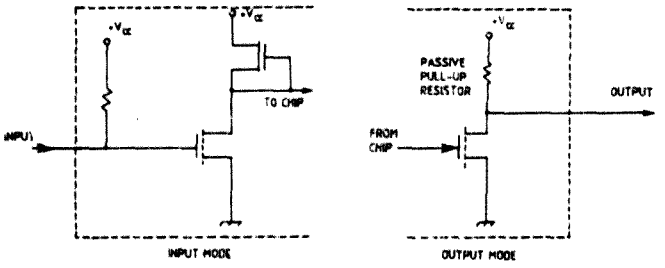


Figure 2.5 Peripheral I/O port 'A' buffer

The switches can sink a full 1,6 mA, making these buffers capable of driving one standard TTL load. In the input mode, the pull-up devices shown in Figure 2.5 are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode. Thus, when using this type of I/O port only one node pair (driver and load) may be tied together, after which logic level corruption will occur. If a driver sinks more than 1,6 mA, its output logic 'low' level moves into the grey region, anywhere between 0,4 V and 2,4 V. In this region of uncertainty the output can assume either of the two logic states, a 'high' or a 'low'. This will ultimately corrupt the measurement information collected.

It appears, at this stage, that programmable peripheral interface-type chips are basically unsuitable for the simulation of the original 8-bit short circuits/open circuits test building block. A unique short circuit/open circuit measurement integrated circuit chip could be designed, using semi-customised development techniques. However, due to the cost, approximately R50 000, this should be a last resort if no existing technology can be found suitable.

Programmable logic arrays were considered, but the I/O lines could not be programmed individually. The basic idea then, was to find a technology that supported the DC characteristics necessary to handle mass multi-node loading, as well as allowing I/O port bits to be independently controllable, or totally isolated from one another.

Another way around this I/O rt line isolation problem, is to use a method whereby all the I/O lines can be fixed together without causing bus contention. This is easily implemented with logic circuits using collector pull-up resistors. The outputs of the gates from which the digital data comes, are simply connected in parallel as illustrated in Figure 2.6.

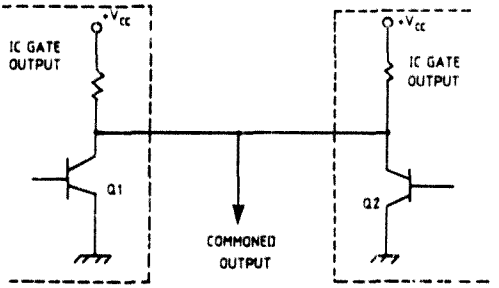


Figure 2.6 Gate outputs connected in parallel to share a common output line

By connecting their outputs directly, the collector resistors are effectively paralleled, thereby reducing the total resistance to one half the value of an individual resistor. The two output transistors then share a common collector resistance. With this arrangement either transistor Q1 or Q2 can bring the output to the logic 'low' condition. If Q1 conducts and Q2 is cut off, or if Q2 conducts and Q1 is cut off, the output will be a binary 0. The only time that the output will rise to +Vcc, is when both Q1 and Q2 are cut off. The way to ensure that digital data is transmitted by one gate then, is to disable the gates not transmitting data. This is done by applying the appropriate input to the gate so that its output transistor is cut off. This permits the other transistor to control the state of the output.

Parallel gate outputs form what is known as the 'wired-or connection.' It is given this name simply because either transistor Q1 or Q2 can bring the output to a binary 0 level. The implementation of this idea is carried out by 'open collector' integrated circuits. In these circuits, the active pull-up stage is eliminated and the collector of the shunt output transistor is made available at an output pin. An external collector pull-up resistor is connected to this.

Instead of using tri-state logic necessary for I/O line isolation, a new 8-node short circuit/open circuit measurement block was designed using open-collector technology. Refer to Figure 2.7.

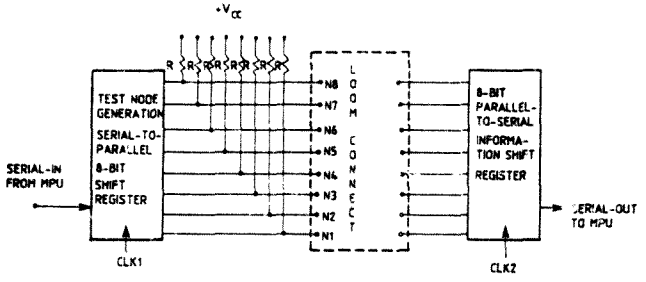


Figure 2.7 Eight-node serial input/output short circuit/open circuit measurement block

Initialization procedure:

1. choose an 8-bit serial-to-parallel shift register;
2. set the serial input bit 'high';
3. clock the shift register 8 times;
4. set the serial-in bit 'low', clocking the shift register one only;
5. pull the serial-in line 'high'.

At this point, the test node generation shift register is basically initialized, with node N1 generating the first logic 'low' test bit. In other words, N1 is being cross-referenced with all the other nodes. Assuming that any of the other nodes are shorted to node N1 due to the insertion of a loom, the concept of 'wire or-ing' removes any danger of bus contention between the shorted outputs. By placing nodes N1 to N8 in the 'high' state, these outputs are effectively disabled from the output bus, permitting node N1, at a logic 'low', to control the state of the output.

Once a test bit has been configured, the data must be read and interpreted by the MPU, determining which nodes are shorted together. An accumulation of this type of information defines the interconnection configuration of the particular loom or motherboard under test. An 8-bit parallel-to-serial shift register is chosen to perform this function.

The loom shown in Figure 2.8 is chosen to demonstrate a complete measurement cycle using the serial measurement block just described.

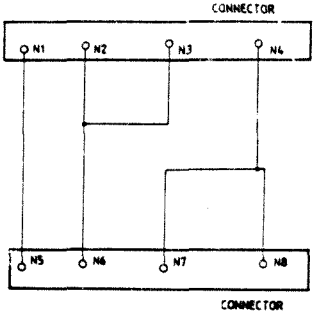


Figure 2.8 Interconnection configuration of unit under test

It is assumed that the test node generation shift register has been initialized. This initialization procedure is identical to that just described. Thus, all node outputs are at a logic 'high', except for node N1, at a logic 'low'. At this stage the first short/open data byte can be read, since initialization effectively configures the N1 test node bit. The information shift register's serial-out bit is clocked 8 times, transmitting the desired byte into a specified MPU register. According to the example provided,

N8N7N6N5N4N3N2N1 = 11101110

is the first received byte, and the lowest significant bit representing N1. This indicates that N1 and N5 are tied together, while all the other nodes are open-circuit with respect to node N1.

CLK1 is clocked once, shifting the 'low' level test node bit to node N2. Since the serial-in line is in the 'high' state, the clocking action reverts N1 back to a 'high'. Thus all the outputs except N2 represent a logic 'high'; in effect in the disabled mode. After executing the read cycle just described, the byte = 11011001 is transferred to the MPU for software decoding. This information indicates that nodes N3 and N6 are shorted to N2. As N3, N5 and N6 are already known to be shorted to other nodes, they are removed from the test bit generation list. This removes the inherent redundancy found in this measurement technique, ultimately improving measurement speed.

The next test bit generating node will then be node N4. CLK1 must now be pulsed twice in order to align the logic 'low' test bit to N4. Note that after initialization, the serial-in line is permanently held 'high'. This enables the 'low' test bit to ripple through the shift register every time CLK1 is pulsed. After reading the short circuits/open circuits byte corresponding to test bit node N4, the byte N8N7N6N5N4N3N2N1 = 00110111 is stored in the MPU, indicating that nodes N7 and N8, are shorted to N4.

Once the test node generation list has been completed, the accumulated data shows the following continuity set-up:

1 N1 shorted to N5;
2 N2 shorted to N3 and N6;
3 N4 shorted to N7 and N8.

This information correlates with the interconnection configuration of the UUT, shown in Figure 2.8.

In order to meet the 240 node requirement, chosen to compare the merits of different technologies, 30 of these serial short circuits/open circuits measurement blocks are needed. This involves 60 low-cost, 16-pin IC packages. Compared to other viable solutions, this measurement technique seems to be a logical choice, as it has advantages in all areas of concern, namely cost, speed and space.

The next step is to specify a standard for the go/no-go card module. The initial packaging will consist of a standard 3U Euro-card rack, enhancing the open-endedness and modularity of the design approach. Once the fundamental measurement and control modules have been established, the tester will then be able to accomodate a wide variety of node capacity and packaging requirements. For example if a single go/no-go measurement card can test 'n' nodes or loom termination points, and the particular Unit Under Test (UUT) requires three times that capacity, the solution would be to simply chain three of these measurement modules together.

All PCB cards used in the system are standard 100 x 160 mm Euro-cards. The main reason for choosing these dimensions is to ensure the future availability of packaging used, for example, new racks may be required to house an expanded or damaged system. Non-standard sized racks may not always be available, thus opting for a non-standard PCB size could prove to be a problem later on. Keeping the board surface area, as well as Computer Aided Design (CAD) limitations in mind, a capacity of 50 nodes per measurement card is an acceptable limit.

2.1.2 Detailed go/no-go measurement card design

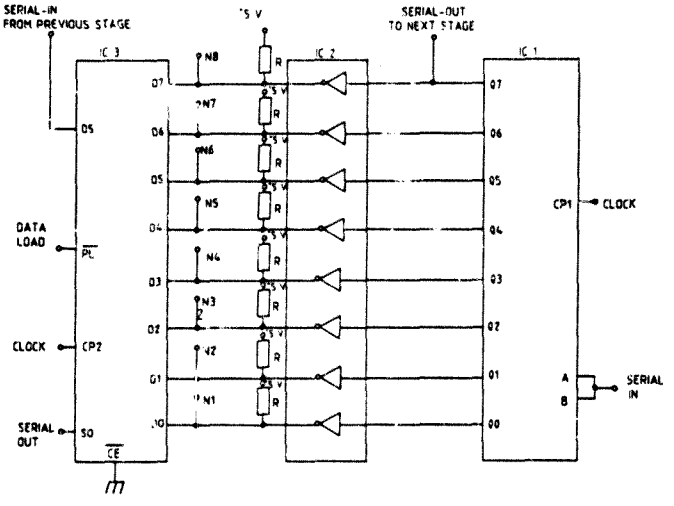
Outline specification

Function. The function of the go/no-go measurement card is to test for gross short and open circuits in looms. The tester compares each node with every other.

Functional specifications. The go/no-go tester has a capacity of 50 nodes. The time taken to test 50 nodes is less than one second.

Serial short circuit/open circuit measurement building block

The core of the go/no-go card design hinges on the serial short circuit/open circuit building block test technique. Refer to Figure 2.9.



IC1 = 164 serial-to-parallel shift register;

IC2 = 05 open collector hex inverting buffer;

IC3 = 165 parallel-to-serial shift register.

Figure 2.9 Eight-node short circuit/open circuit building block hardware architecture

In ord r to keep the overall card power consumption as low as possible, all ICs are of the high speed CMOS type. The subject of power consumption for purposes of portability will be considered when designing the secondary cell backup power unit.

Pull-up resistors. The passive pull-up resistors (R) will consist of Single In-line Packages (SIP). Each package incorporates eight thick-film resistors of equal value, each connected between a common bus and a discrete PC board pin. The SIP resistor network features low profile compatibility with Dual In-line Packages (DIPs), reduces PCB space, reduces total assembly costs and has a proven automatic insertion capability.

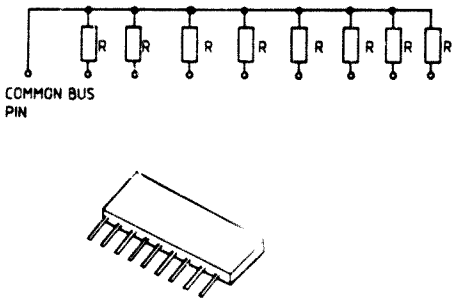


Figure 2.10 Internal and external SIP configuration

Since each standard go/no-go measurement module facilitates 50 loom termination points (nodes), seven of these SIP resistor networks are required per card module.

Due to the digital nature of the measurement implementation, some resistance threshold indicating a short circuit or an open circuit must be chosen.

Many of the automatic loom testers on the market today specify this resistance threshold in the region of 20 to 40 kilo-ohms. The question to ask is: What relevance do these specifications have to the go/no-go test philosophy? In 'real-world' situations, a wire can be represented by one of two resistance domains:

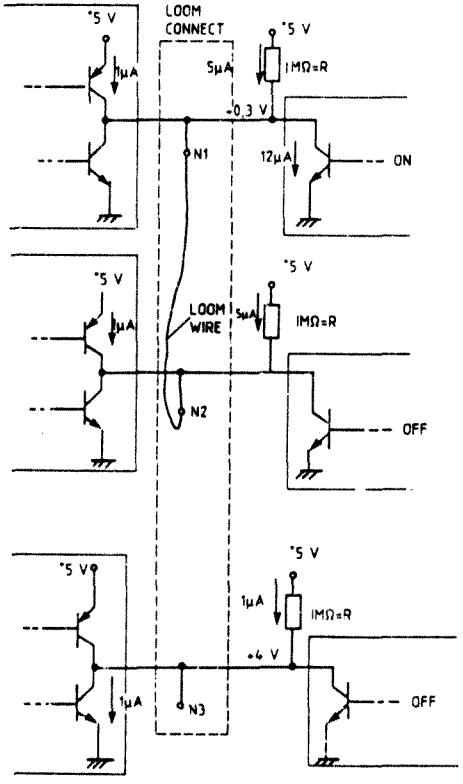
- a continuous path or a short circuit ranging anywhere from tens of milli-ohms to tens of ohms;

- a discontinuous path or an open circuit usually in the mega-ohm region.

One could then argue that choosing a resistance threshold of either 100 ohms or 1 mega-ohm could have the same success in detecting continuous paths and discontinuous paths. To ensure utmost reliability of measurement results, it will be assumed that a rare case such as that of a wire displaying a resistance between the regions of continuity and discontinuity, can exist. Keeping the hardware constraints of the design in mind, the resistance threshold indicating a short circuit from an open circuit must be as high as possible.

This implies that, information stating a path of discontinuity, represents a true open-circuit in the particular wire under test. Continuous path test data will almost always represent a true short-circuit in the wire, except during the rare instance where the actual resistance is greater than a couple of ohms, but less than the threshold limit. Even if this situation were to occur, all loom wires falling in the go/no-go test category, consist of status or control signal paths. Since all these termination points feed into high impedance inputs, thus carrying minute currents, wire resistance is not all that critical. Only in situations where wires carry current of any significance, would the resistance in a wire be highly critical. This type of wire would then fall under the POWER LINE testing philosophy. Wires of this nature are catered for by a completely different measurement module, known as the Quality Card. Refer to Chapter 3.

Refer to Figure 2.11 for the determination of the resistance threshold limit.



Input line of '165' Parallel-to-serial shift register

Output line of '05' inverting Open-collector buffer

Figure 2.11 Detailed input/output hardware breakdown of the node port lines

Applying a logic 'low' test bit to N1 and choosing a value of R = 1 mega-ohm, the DC characteristics of the three-node setup are examined. It should be noted that nodes N2 and N3 are disconnected from the test bit generation bus line. Connection between N1 and N2 is due to the loom wire only. Node N1, generating the 'low' level test bit, can read anywhere from 0,15 V depending on the sink current, which is determined according to the particular node loading at the time. The specifications used to calculate the threshold resistance are for high speed CMOS hex inverters with open drain outputs.

The maximum output, low voltage for the inverting hex '05' buffer for output sink currents less than or equal to 4,5 mA is 0,33 Volts. The maximum input, low voltage allowed by a high speed CMOS 165 shift register input is 0,8 Volts. Any potential above this point and below 2 Volts, (the minimum input high voltage level) causes uncertainty. In this region an input can interpret the voltage level as a logic 'high' or logic 'low'. The resistance threshold limit indicating the short circuit/open circuit barrier, can now be approximated.

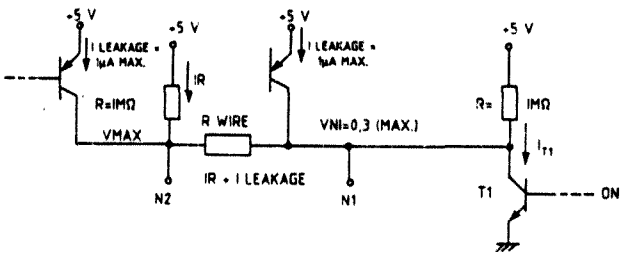


Figure 2.12 Shorted node pair N1 and N2 resistance model

Since the maximum voltage at N2 cannot exceed 0,8 Volts, or cause logic level corruption:

$$I_R = \frac{V}{R} = \frac{4,2}{10^6} = 4,2 \text{ mA}$$

$$\therefore R_{WIRE} = \frac{V_{MAX} - V_{N1}}{I_R + I_{LEAKAGE_{MAX}}} = \frac{0,8 - 0,33}{5,2 \times 10^{-6}} = 100 \text{ kilo-ohms}$$

This is applicable for a temperature range between -40 °C and +85 °C.

This 100 kilo-ohm threshold limit is based on a maximum of 4,5 mA being sunk through test bit generation transistor T1. In situations where one or two loom termination points are shorted together, the sink current is tens of micro-amps only. V_{N1} will then be approximately 0,15 V pushing the shorts/opens threshold resistance to approximately 120 kilo-ohms.

On the other hand, V_{N1} will still be below 0,8 Volts, typically 0,7 Volts, while sinking up to 9 mA through transistor T1. It can be seen that as the test node load is allowed to increase, the shorts/opens resistance threshold greatly decreases. In this particular case of loading, the resistance threshold decreases down to 17 kilo-ohms.

Test node loading versus short circuit/open circuit threshold resistance specifications. Refer to Figure 2.12.

Case one

$$I_{T1} = 4,5 \text{ mA}; \; V_{N1} \text{ (max)} = 0,33 \text{ V}.$$

The current sourced by each node via a 10cm wire short to the logic 'low' test node, consists of the following current components:

$$I_N = I_R + I_{LEAKAGE};$$

Where: I_R is the maximum current sourced through the passive pull-up resistor R; and

I_N is the maximum leakage current sourced via a parallel to the serial shift register input.

$$\therefore I_{T1} = N \, I_N$$

$$= N \, (I_R + I_{LEAKAGE})$$

$$N = I_{T1}/(I_R + I_{LEAKAGE})$$

where N is the number of nodes.

The number of nodes or loom terminations that can be shorted to any one point, exhibiting a shorts/opens resistance threshold of approximately 100 kilo-ohms is:

$$N \approx (4{,}5 \text{ mA})/(4{,}2\ \mu A + 1\ \mu A);$$

$$\approx 850 \text{ nodes}.$$

Case two

$$I_{T1} = 9 \text{ mA},\ V_{N1} = 0{,}7 \text{ V}.$$

At a shorts/opens resistance threshold of about 17 kilo-ohms the test node load can accommodate as many as 1 700 nodes, without corrupting measurement data. By changing the collector pull-up resistors (R), one could vary the threshold point from below 100 kilo-ohms. However, reducing the value of collector resistor (R) greatly degrades the node loading capacity of the system.

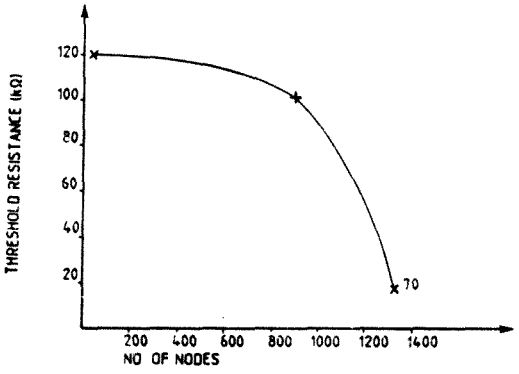


Figure 2.13 Shorts/opens threshold resistance versus node loading

Basic operation of the eight-node building block. Refer to Figure 2.9, which illustrates the hardware architecture of the measurement building block. The measurement technique for an eight-node serial short circuit/open circuit block has already been described in some detail. It is therefore necessary only to concentrate on final detail due to specific hardware choices. The object is to place a logic 'low' test bit on each of the eight nodes, cross-referencing them individually with every other node. All signals entering/exiting the building block are controlled by a microprocessor.

The following algorithm determines short and open circuit information:

a. A logic 'low' is placed on the serial-in input.

b. Clock CP1 is toggled eight times. Data is serially shifted in and out of the eight-bit register during the positive-going transition of the clock pulse.

c. Outputs Q0 to Q7 are now 'low', causing the outputs of the open-collector inverting buffers to be deactivated. Due to the passive pull-up resistors all outputs are in the pull-up or 'high' state.

d. The serial-in input is toggled to the 'high' state.

e. Clock CP1 is toggled once.

f. Output Q0 now represents a logic 'high', causing output N1 of the inverting buffer to be activated. This 'low' level output line controls the entire output buffer bus. Any of the other output lines tied to N1 through a loom wire, will then also display the 'low' state.

g. The serial-in input is again toggled low. The single high level output bit of the serial to parallel register, ultimately generating the test bit can now be positioned via the inverting buffer at any of the node outputs simply by toggling clock CP1.

h. At this point, the 'low' level test bit is at the N1 output. The short circuit/open circuit information byte N1 to N8, is loaded into the parallel-to-serial register, via control of the $\overline{PL}$ input. When the parallel load ($\overline{PL}$) input is low, parallel data from the D0 to D7 inputs are loaded into the register asynchronously.

i. The serial-out output bit is read into the MPU, then clock CP2 is pulsed once. This read cycle is repeated eight times after which the entire information byte has been stored by the microprocessor. Data transfer occurs on the positive edge of the clock.

j. A 'low' level test bit will then be placed on each of the node output lines, N1 to N8, following the above procedure.

k. To ensure maximum measurement speed, the inherent redundancy found in this technique must be eliminated. This is accomplished by excluding all nodes, known to be shorted to previous test node bits, from the test bit generation list.

The serial-in input (DS) from, and serial-out output (Q7) to other measurement blocks will be discussed in Cascaded Building Blocks.

The entire I/O status/control bus of the measurement block is controlled by appropriately toggling specified MPU port bits. In the case of the positive-going edge clocks CP1 and CP2, the specified MPU port bits needed to be toggled low-high-low. The clock signal supplied by the MPU displayed gross rounding in the signal rising edge.

Figure 2.14 Clock train supplied by MPU port bits

This rounding effect caused a delay in the effective triggering time of the shift register clock logic, which lead to serious false triggering. Often a serial input bit would be shifted two or even three positions, by a single clock pulse.

IC logic families normally require fast transitions between voltage levels to operate satisfactorily. If a signal level is changing slowly and a fast transition or edge is required, the Schmitt trigger is a useful interfacing device. This is because the output of a Schmitt triggered gate makes a rapid transition whenever the input voltage passes through a certain threshold voltage, irrespective of how slowly the input signal level may be changing with time. To ensure quality signal transmission a 7414 hex Schmitt trigger inverter will interface between the MPU and measurement block control/status bus.

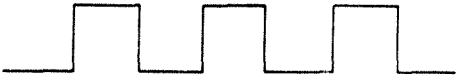


Figure 2.15 Clock train fed via the Schmitt buffer

The input/output voltage transfer characteristic of the 7414 Schmitt trigger input IC is illustrated in Figure 2.16.

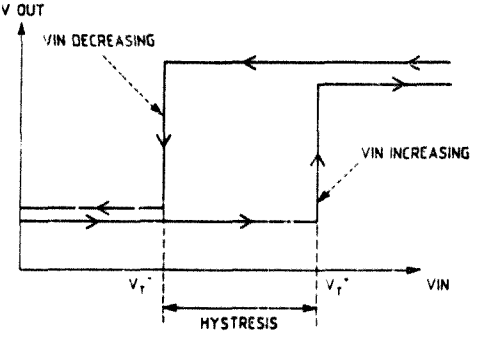


Figure 2.16 Voltage transfer characteristics

The transfer characteristic shows that a positive-going threshold voltage V_T^+ exists, corresponding to V_{IH}, as the input signal increases from below V_T^-. Since the Schmitt trigger input is connected to an inverting gate, the output makes a rapid high/low transition as V_{IN} passes through V_T^+. Similarly, a negative threshold voltage V_T^- exists, corresponding to V_{IL}, as the input signal level decreases from above V_T^+. The region between V_T^+ and V_T^- is referred to as the hysteresis of the trigger. $V_T^+ = 2$ V and $V_T^- = 0,6$ V giving a hysteresis of $V = V_T^+ - V_T^- = 1,4$ V, exhibiting excellent noise immunity.

The two-node short circuit/open circuit measurement block

Each standard go/no-go card measurement module is specified to have a fifty node capacity. After cascading six serial eight-node measurement blocks, there are still two node positions not accounted for.

It is thus necessary to design a discrete two-node shorts/opens measurement block. The idea is to simulate the exact function provided by the eight-node block, making all measurement blocks compatible with one another. The fifty go/no-go measurement module is then possible by simply cascading the building blocks together.

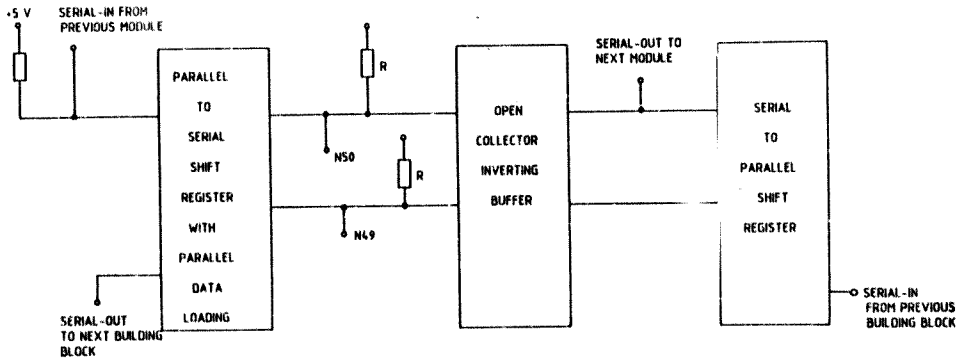
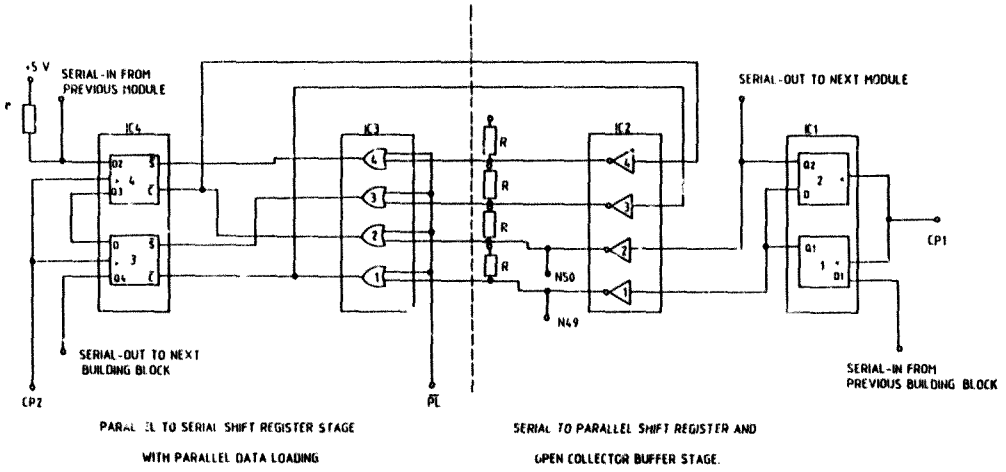


Figure 2.17 Functional block diagram of the two-node short circuit/open circuit measurement block

The serial-to-parallel shift register function must be able to generate a 'low' level test bit on outputs N49 and N50 individually. The isolation requirement of the output node bus lines is facilitated using the open collector buffer technique. Data present on node points N49 and N50, carrying the information necessary to determine a loom interconnection configuration, must be loaded into the output shift register stage. Thus besides being able to serially transmit information to the MPU for interpretation, the parallel to serial shift register must include a parallel data load facility.



IC1 and IC4 : 7474 dual D edge-triggered flip-flops with preset and preclear;

IC2 : 7405 open collector hex inverter;

IC3 : 7432 quad 2-input OR-gate.

Figure 2.18 Detailed hardware structure of two-node measurement block

With reference to Figure 2.18:

Assume that D1 is a logic 'high', being the serial-out line from the previous eight-node block. This implies that node output N48 is, via its open collector inverting buffer port line, currently generating the 'low' level test bit. Since N49 and N50 are in the pulled-up state, outputs Q1 and Q2 represent a 'low' state. Pulsing clock CP1 then places the 'low' level test bit on node line N49, enabling the loom termination point corresponding to this node to be cross-referenced with every other node. The application of another pulse to CP1, ripples the test bit to node output N50. Only at the instant of the positive clock edge is the information on the D input entered into the flip-flop. This basically covers the serial to parallel shift register and open collector buffer stage.

Once a test bit pattern has been set up the measurement data must be loaded into the output shift register in parallel and serially shifted into the micro-processor. The analysis of the parallel to serial shift register stage with parallel data loading, assumes the test bit to be positioned at node output N49. The parallel load line ($\overline{PL}$) is 'high', causing the outputs of the OR gates to be logic 'high'. Due to the 'low' level active nature of the asynchronous preset and preclear inputs, the outputs of flip-flops 3 and 4 are unaffected. When the parallel load line is pulled active 'low' the logic 'low' test bit is gated through to OR gate 1's output. This activates the preclear input of flip-flop 3, causing output Q4 to be pulled low thus representing the output at N49. Care must be taken to ensure that the preset input is kept in the inactive state.

This is accomplished by feeding the OR gate 1 output through inverting buffer 3, forcing the output of OR gate 3 'high'.

In the same manner the 'high' level output at N50 must be fed through to flip-flop 4 output, Q3. With $\overline{PL}$ low and N50 high the output of OR gate 2 is a high, thus keeping the preclear input in the inactive mode. In order to enter a high state into output Q3 the preset input of flip-flop 3 must be activated, i.e. driven to the low state. This is done by feeding the high level output of OR gate 2, through inverting buffer 4 resulting in the OR gate 4 output being 'low'. It can thus be seen that the output logic levels of node N49 and N50, are effectively loaded into flip-flop outputs Q4 and Q3 respectively.

Cascaded measurement building blocks

Cascading one two-node and six eight-node building blocks together, comprises the full 50-node go/no-go measurement card module. The ease involved in this linking process is mainly due to the inherent expansion facility found in shift registers in general. The objective basically is to extend the test bit generation/reception algorithm to the 50-node measurement system required. Figure 2.19 illustrates this cascading effect basically comprising the go/no-go card measurement module. Refer to Figures 2.9 and 2.18 for detailed measurement block hardware configurations.

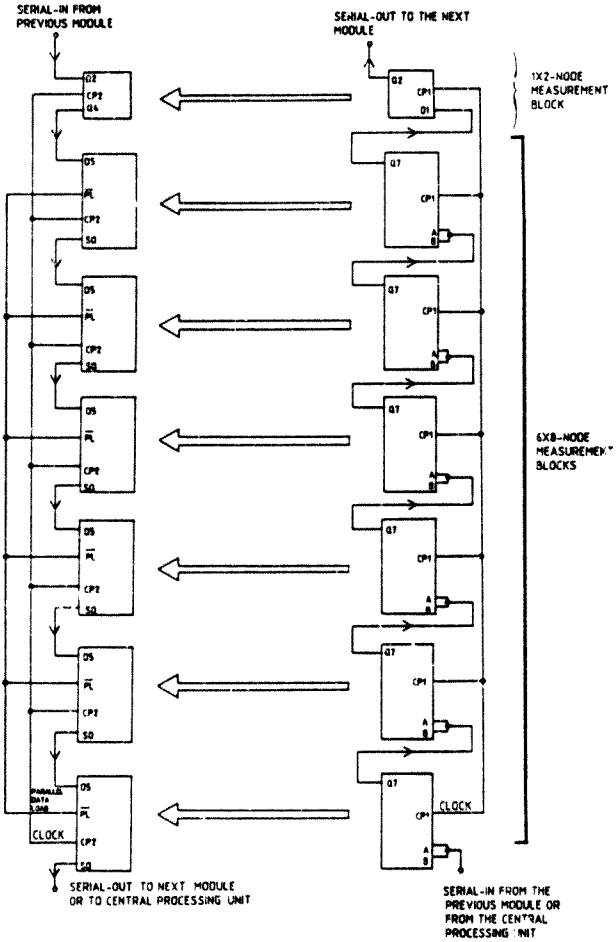
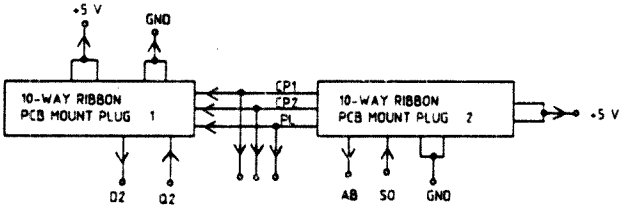


Figure 2.19 Fifty-node cascaded measurement block configuration

Two ten-way ribbon PCB mounting plugs are mounted on the rear edge of every fifty-node go/no-go measurement card module, providing an easy low-cost expansion facility. Refer to Figure 2.20. When the node capacity of the test system is to be upgraded, new measurement modules are simply 'chained' in. This enables each go/no-go card to communicate with neighbouring modules, as well as receive/transmit control signals to/from a central processing unit.

Refer to Appendix A for the detailed go/no-go measurement card circuit diagram.



Plug 1 handles all the signals needed for the next measurement module to be chained in. Plug 2 facilitates the signal requirements of the present module. In order to ensure optimum power flow the +5 V and GND paths occupy double connector pins each.

Figure 2.20 Chaining expansion facility on board each measurement module

Tester/UUT interface

The interface consists of a mating connector and a harness assembly for connection to the tester. If the user does not ensure the integrity of the interface between the tester and the loom under test, more time will be spent in troubleshooting the interface than in testing the assemblies. Each go/no-go/GO card module consists of two 26-way ribbon PCB mounting plugs, providing node lines N1 to N50 with a link to front panel connectors. Thus, on ordering the tester, the customer has a wide choice of front panel connectors, depending on the test environment. This might prove to be cost-effective, if for example, a particular type of connector seems to predominate among the various loom assemblies, its mating counterpart can be chosen as a front panel connector on the tester. In this type of situation the building of UUT/tester interfaces would become less of a problem. Many users would prefer to have this option available when ordering this equipment.

Transmission line effects

During a test operation many of the node lines will, via the loom, be tied together. A signal requires a finite time to travel along a loom wire, and making allowance for this is important in bus timing. The delay is caused by distributed inductance and capacitance on the wire which, as a result, is described as a transmission line and is modelled as illustrated in Figure 2.21. In addition to the signal delay down the loom wire, the second and usually more serious affect is the generation of unwanted reflections from both the load and source ends of the line leading to a ringing effect.

This effect is often observed on the leading and trailing edges of the signals and is illustrated in Figure 2.21. This, and the less common rounding of signal edges can lead to the loading of false measurement data into the parallel-to-serial shift registers.

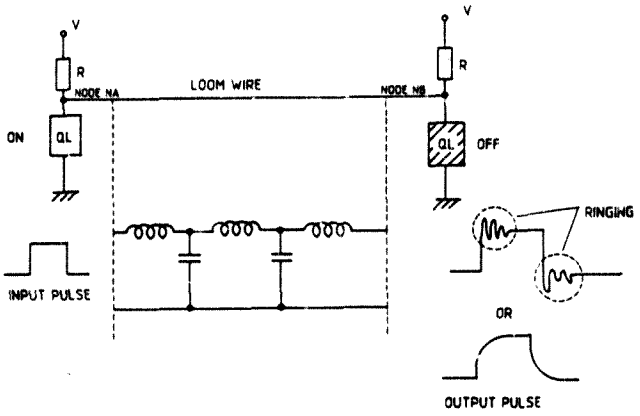


Figure 2.21 Transmission line model and effects

This effect is often observed on the leading and trailing edges of the signals and is illustrated in Figure 2.21. This, and the less common rounding of signal edges can lead to the loading of false measurement data into the parallel-to-serial shift registers.

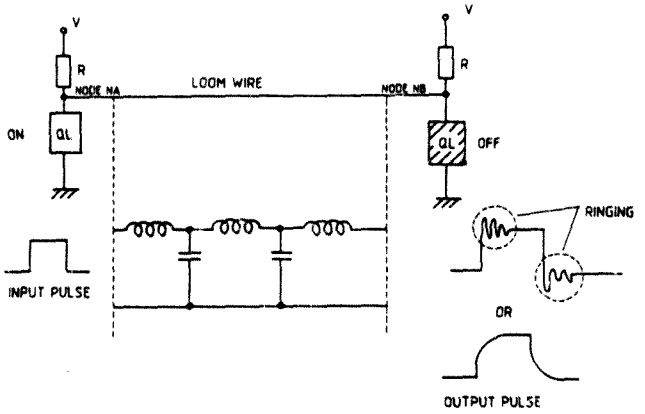


Figure 2.21 Transmission line model and effects

To ensure integrity of all measurement data loaded into the parallel-to-serial shift registers, which will eventually be interpreted by the MPU, the following steps are taken:

a. all inputs to the shift register ICs chosen are diode-clamped, minimizing transmission line effects and simplifying the system design. The technique used in this diode termination approach is to connect Schottky diodes from the signal line to Vcc and from the signal line to ground as illustrated in Figure 2.22. The effect of the diodes is to eliminate the voltage excursions above +5 V and below 0 V.

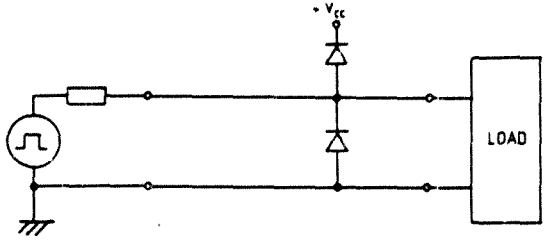


Figure 2.22 Diode termination

b The signal travels at approximately 0,6 times the velocity of light (C = 3 x 10^8 m/s) and for a line of length (L) the transit time t_D is:

$$t_D = \frac{L}{0,6C}$$

Signal reflections in the wire stabilize after approximately $10t_D$. For a loom length of approximately 1,8 m, the stabilization time is equal to:

$$10[1,8/(1,8 \times 10^8)]$$
$$= 100 \text{ ns.}$$

Allowing for extremely long looms and the noisiest of environments, a software delay of 100 micro-seconds was chosen.

2.1.3 Measurement software

Storage of measurement data

Due to the specific hardware architecture of the go/no-go measurement system, the serial measurement data fed into the MPU for interpretation, is stored in a predetermined pattern. In order to maximize the efficiency of the algorithms necessary to determine short and open-circuit information, the data storage characteristics must be fully understood.

A 16-node measurement system was used to demonstrate the data storage pattern, serially transmitted to the MPU. Figure 2.23 illustrates the example measurement setup. The loom under test interfaces to this system via the node output points N1 to N16. Figure 2.24 shows the interconnection configuration of the chosen loom to be tested. Although seemingly small, the 16-node system comprehensively defines the principles behind the serial data storage mechanism.

Describing a 50-node system, i.e. the standard go/no-go measurement card, or even a 150-node test setup involving the cascading of three go/no-go modules, would merely duplicate the principles defined for the chosen 16-node example.

Ignoring unnecessary detail, initialization assumes that outputs N2 to N16 all pulled-up, with N1 only being in the logic 'low' state generating the test bit. In other words connector pin 1 is being cross-checked with every other connector pin in the loom interconnection configuration. It should be noted that the loom configuration shown in Figure 2.24 is being referred to. Thus according to the measurement theory of the serial shorts/open building block previously discussed, any connector pin shorted to pin 1, should exhibit a 'low' level at its corresponding node line N?. Node outputs N1, N5 and N9 represent logic 'low' states, while the rest remain in the inactive pulled-up state.

Once the parallel data load control signal has been activated, the status of the node bus N1 to N16 is loaded into the relevant parallel-to-serial measurement transmitter blocks. Bit D7 corresponds to serial-output Q7, implying that information is clocked into the MPU in the following order:

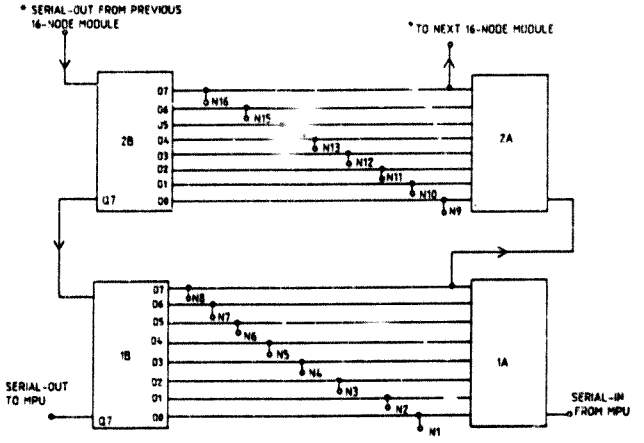
N8:N7:N6:N5:N4:N3:N2:N1:N16:N15:N14:N13:N12:N11:N10:N9.

Conserving data storage space as well as software manipulation overhead, and greatly enhancing the measurement speed and fault diagnostics, it was decided to store short-circuit information only, i.e. all data bits representing a logic 'low'. The remaining data, although not recorded, is assumed to be open-circuit.

The first measurement cycle, which

- places a 'low' level test bit on node N1;
- parallel-loads the node bus into parallel-to-serial transmitter blocks; and
- serial-shifts measurement data into the MPU,

finds N5:N1:N9 stored in the MPU, in this specific order.



* If 32 nodes were required, node lines N17 to N32 would be supplied by a second cascaded 16-node module.

A = serial-to-parallel shift register, open collector buffer, test bit generation block.

B = parallel-to-serial, parallel data load, measurement information transmitter block.

Figure 2.23 A 16-node measurement system module demonstrating the serial data storage pattern