Mains Power Quality Improvement using Active Filters

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Certificate of Research

This is to certify that, except where specific reference is made, the work described in this thesis is the result of the candidate's research. Neither this thesis, nor any part of it, has been presented, or is currently submitted, in candidature for any degree at any other University.

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Preface

The work contained in this thesis was carried out on a part time basis while employed as a Senior Lecturer at the School of Electronics of the University of Glamorgan and from 2006 onwards within the CCI Faculty of the University of Glamorgan. Supervision was carried out by Dr Marcel Jayne (Director of Studies) and Dr David Rees.

Acknowledgments

I would like to thank Dr Jayne for his advice and help throughout the time spent on this work and additionally Dr Rees for his advice in the preparation of this thesis. I would also like to thank Prof Jon Clare for his feedback following the viva.
I would like to thank my wife Jackie, for her continued support.
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Synopsis

Improvements in the control of mains connected apparatus brought about by energy switching converters has resulted in disturbances to the supply current due to their non-linear characteristics. These disturbances result in a supply current that no longer retains the same shape and phase of the source Voltage which is the ideal requirement for a purely resistive load. The resulting current waveforms of these non-linear loads contain unwanted harmonics and non-unity power factors. EMC problems also arise as a consequence of the fast switching devices in the electronic control of power apparatus.

This thesis reports the results of an investigation into methods of actively filtering the unwanted harmonics from the supply current for single phase domestic applications. Designs were considered for loads up to a maximum of 15kW and simulations of such systems were carried out. Practical work was carried out at reduced Voltages and power levels to prove the viability of the developed theory. The focus of the work was initially to investigate the suitability of "Sliding Mode Control" for the control of the Active Power Filter (APF). Recent research investigations (see references [5.2], [5.3], [5.4], [5.5], [5.6], [5.7], [6.1]) indicated that this method achieved some success, however, after detailed investigation it was found that the sliding mode control methods of referenced papers did not provide the required steady state or dynamic response. A specific version of Sliding Mode based on a switching algorithm accounting for the practical limitations of physical devices called Discrete Sliding Mode (DSM) was developed. The conventional H-bridge was further developed by adding an additional inductor, two diodes and two switching devices allowing the system itself to change dynamically in response to load characteristics. Simulation models were derived based on the DSM technique and applied to the problem of harmonic reduction for a number of complex non-linear loads. Simulation results showed that the Sliding Mode technique was unnecessarily complex and unsuitable for the application of Active Filtering. Using averaging principles based on the flow of real power, detailed analysis of the dynamic response of several APF configurations was made possible. This work led to the development of a new control method called "Energy Compensation". Energy compensation in conjunction with the development of a new technique referred to as "Proportional Hysterisis Control"

allowed optimum placement of system poles in the Z-plane. A test system was built to demonstrate the proportional hysterisis control method using energy compensation. This test system provided a comprehensive user interface allowing all relevant control parameters to be varied and monitored. Good correlation was obtained between theoretical and practical results for steady state and transient responses (i.e. for loads that are assumed periodic but change after a few mains cycles) for a range of non-linear loads.

Several new ideas and techniques emerge in this thesis, a summary of which is as follows:

An algorithm is presented for applying Sliding Mode Control to a physical APF system taking physical switching devices into account including methods of deriving the reference signals. The theoretical developments are applied to the design of an enhanced APF bridge. A new discrete method is presented for analysing the APF system which is used to demonstrate the unsuitability of the sliding mode technique for APF control. The analysis method is further used to show how a control method can be obtained using “Energy Compensation” and “Proportional Hysterisis Control” that optimises the transient response and is shown to work well in a practical system.

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Glossary of Terms

APF: Active Power Filter

PWM: Pulse Width Modulation

SLMC: Sliding Mode Control

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

IGBT: Insulated Gate Bipolar Transistor

VSCS: Variable Structure Control System

C: Capacitor reference

L: Inductor reference

I_s: Source current

I_{sref}: Source current reference

$I_{srefRMS}$: RMS value of I_s

I_{s1ref}: Fundamental in-phase source current component

$I_{s1refRMS}$: RMS value of I_{s1ref}

I_f: Filter current

I_{f1}: Fundamental component of APF current with +/- 1 power factor with respect to V_s

I_{f1RMS}: RMS value of I_{f1}

I_{fref}: Filter current reference

$I_{frefRMS}$ RMS value of filter current reference

I_{f1ref}: Fundamental component of I_{fref} with +/- 1 power factor with respect to

$I_{f1refRMS}$: RMS value of I_{f1ref}

$\dot{I}_{f\min}$: Minimum design value for $\dot{I}_f$

$\dot{I}_{f\max}$: Maximum design value for $\dot{I}_f$

$I_{fRMSmax}$: Maximum fundamental RMS current that can be supplied by the APF

I_{fn}: RMS value of the nth harmonic current supplied by the APF

I_{fave}: Average value of the maximum fundamental current that the APF can supply

I_{fmax}: Maximum design value of APF current

V_s: Source Voltage

V_{sRMS}: RMS of source Voltage

V: Peak of source Voltage

I_L: Load current

I_{L1}: Fundamental component of I_L with +/- 1 power factor with respect to V_s

I_{L1RMS} RMS value of I_{L1}

I_{Ln} Amplitude of the nth harmonic of the load current

V_{cap}: Capacitor Voltage

V_{capref}: Time dependent Capacitor reference Voltage

$V_{capconst}$: Capacitor dc Voltage associated with V_{capref}

V_{capave}: Average capacitor Voltage in steady state

V_{capdev}: Maximum deviation of capacitor Voltage from $V_{capconst}$

s: Laplacian variable

S: sliding surface (function of time)

K: Input ideal conductance

x: State variable (function of time)

$\tilde{x}$: Error in state variable (function of time)

x_d: State variable reference (function of time)

T: Switch sample time

τ: Period of the mains cycle

z: Z transform discrete variable

z_{2T}: Z transform variable for a system sampled with period 2T

z_τ: Z transform variable for a system sampled with period τ

Chapter 1 An Introduction to the Thesis

This chapter introduces the work contained in this thesis.

The following aspects are dealt with:

- "The Power Quality Problem" An overview of the problems associated with non-linear loads
- "A survey of Active Power Filters": A review of the area generically referred to as Active Power Filters and other related devices
- "An outline of the reported research work and contribution to existing knowledge"
- "Aims and Objectives" of this research thesis
- "A Guide to the Thesis"

1.1 The Power Quality Problem

There is a progressive increase in the number of complex electronic apparatus requiring connection to the public mains supply, many of which incorporate ac to dc conversion and switched mode power supply techniques. The efficiency and cost advantage that such techniques offer will ensure that this trend will increase. For example, the ever increasing number of personal computers in the home and the office is now a cause for concern and with processors becoming faster, the power per unit continues to increase. There is now justification for the need for harmonic removal at the single phase supply point for domestic installation and the small to medium office. Whereas the switched mode power supply is efficient in terms of energy transfer, the conversion from ac to dc in such apparatus can cause major disturbances to the harmonic content of the associated supply current.
The use of SCR devices for power control of lighting and electrical machinery also results in unacceptable harmonic disturbances.

It is these concerns that have prompted the work reported in this thesis to research methods of harmonic correction. The system to be studied known generically as the "Active Power Filter" (APF) is essentially a switched non-linear power converter. The purpose of such a system is to track the current consumption of a locally connected device (or devices) which themselves are non-linear in their energy consumption cycle, and attempt to eliminate the disturbances so caused by removing all watt-less components of current from the source.

1.2 A survey of Active Power Filters

The term Active Power Filter (APF) in the context of this thesis refers to a device based on the principles of the switching inverter that actively suppresses the flow of the reactive and higher order harmonic components of load current caused by connecting a non-linear load to the power source. The remaining current taken from the source should only be that which supplies real power (unity power factor) to the load. To achieve this it is necessary to have access to transistor components that can handle both the high currents of the load at Voltages above the peak of the source and

be able to switch under these conditions at frequencies significantly higher than the highest harmonic current component of the load that requires suppression.
By removing these components, the resulting supply current should have a significantly improved Total Harmonic Distortion (THD) level and a much improved power factor (see section 2.2 for discussion of THD).
The principle of compensating for reactive and harmonic power components using high frequency switching devices can be traced back to the early 1980's but significant interest in the area started to appear in the early 1990's (as can be seen from the range of references given in the References and Bibliography sections of this thesis) when fast switching power MOSFETS and IGBTs (Insulated Gate Bi-Polar Transistors) from semiconductor companies (e.g. International Rectifier, ST Microelectronics, Fairchild, Semikron etc) became available. All APF techniques involve the use of an energy reservoir which absorbs or delivers energy as required by the reactive and harmonic load components, where the energy reservoir is usually a capacitor (Voltage fed) or sometimes an inductor (current fed).

APF's appear in both single and three phase forms for low power (up to 100kVA). Medium power (100kVA to 10 MVA) levels are considered unviable for APF's owing to the high Voltages concerned. Even if transformers are used to step down the Voltage prior to using an APF then the currents are still too high for the available switching devices. Instead, more traditional techniques are used to remove reactive and harmonic components:

- Inductive and capacitive static compensators
- Relay controlled LC circuits
- Tuneable harmonic filters
- Line commuted thyristor converters
- Synchronous condensers
- Cascaded multi-level inverter VAR compensators/STATCOM

Within the low power category there are two APF topologies: the shunt active filter and the series active filter.
The shunt active filter is placed in parallel with the non-linear load and under steady-state i.e. steady-load conditions, generally only handles the reactive and harmonic

load components (see section 2.4.3 for a discussion of power flow paths). The heat dissipation due to switching losses is therefore reduced. However (depending on the load) the devices may still have to handle currents almost up to the peak of the full load current.
The series active filter has to continually handle the full load including the reactive and harmonic components and therefore switching losses will generally be higher. The shunt device is therefore more suitable for the higher-end of the lower power applications.
For the higher power applications where switching devices are unavailable to handle the currents concerned, it is possible to use several shunt APFs in parallel. If the non-linear load is distributed, then a separate APF can be assigned to each section.
It should be noted that within the wider context, the term "Active Power Filter" is also used to describe devices that suppress some of the reactive and harmonic load components of current using techniques not necessarily based on the high frequency inverter. Classifications are given in broad terms in figs 1.1 – 1.4.
Shunt APF arrangements are of the inverter type as shown in figs 1.1 and 1.2 or of the switched capacitor and lattice type as shown in figs 1.3 and 1.4. With the inverter types, a control circuit is used to determine the required source current and a switching system (usually PWM or occasionally hysterisis) forces the bridge to handle the difference current between the load and the source reference. With the switched capacitor and lattice types, inductors or capacitors or tuned circuits are switched into circuit to absorb the reactive and harmonic components of the load current.

There are also proposed hybrid techniques that combine switching devices with tuned filters (e.g. ref [3.2]) where transformer coupled shunt connected series LC tuned networks remove the low order odd harmonics.

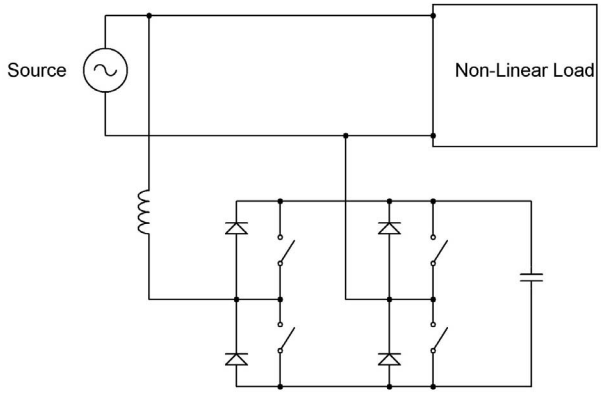


Fig 1.1: Voltage fed Inverter Bridge APF

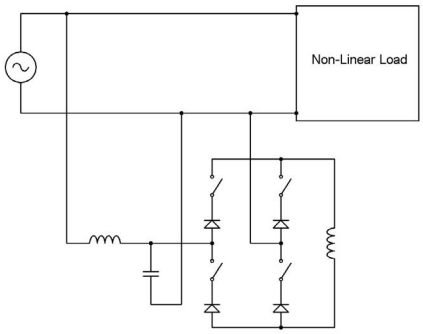


Fig 1.2: *Current fed Inverter Bridge APF*

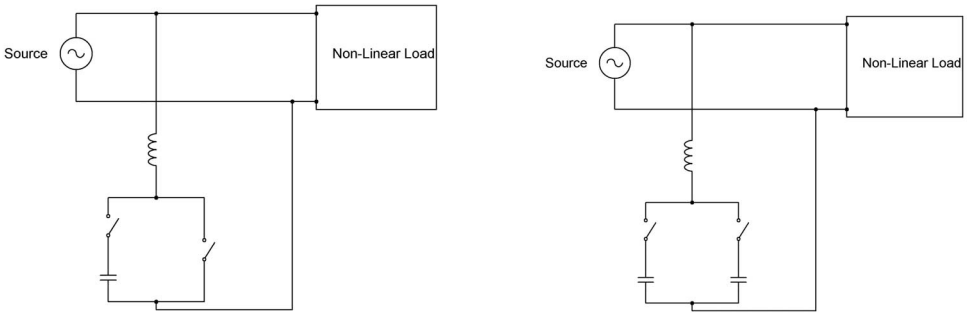


Fig 1.3*: Switched Capacitor APF*

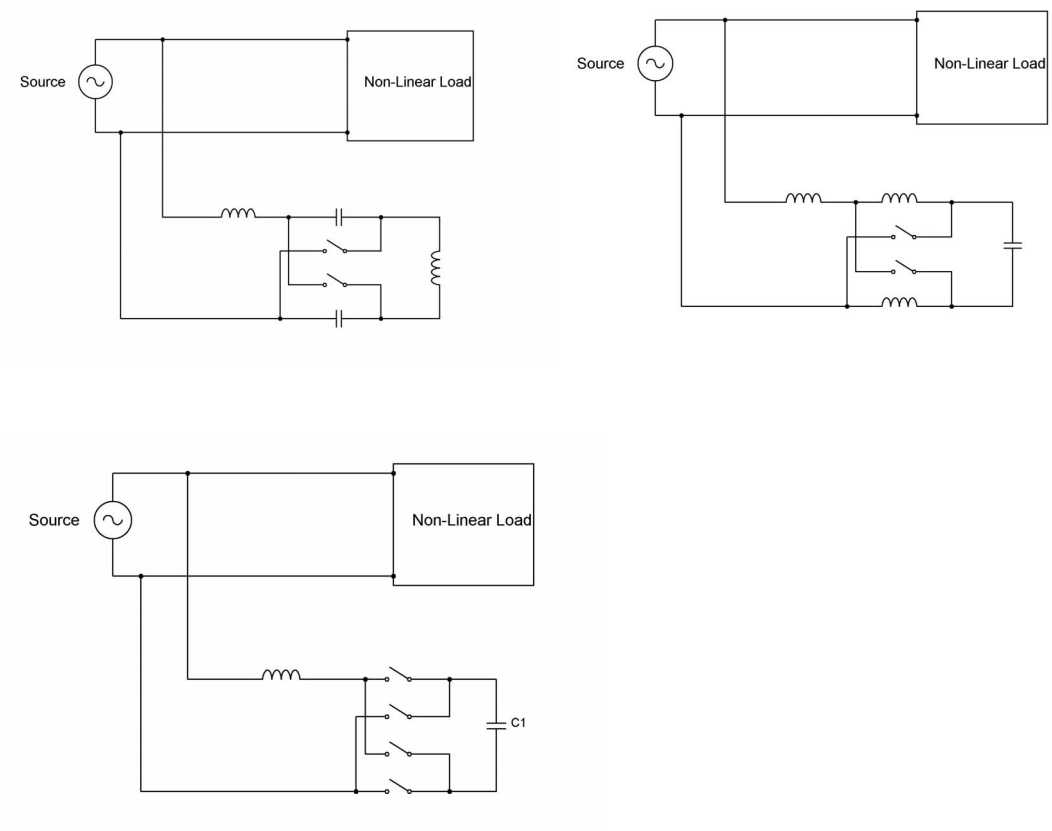


Fig 1.4: *Lattice Structures*

Another interesting hybrid technique has been developed (see Ref [3.1]) which overcomes some of the limitations of the available switching devices for low power inverter bridge applications. Two inverter bridges are placed in parallel with one using IGBTs and the other using MOSFETS (see section 3.11.1). The IGBT's are intended to handle the higher current low frequency reactive components and the MOSFETS will handle the lower current higher frequency harmonic components. Energy storage is provided by a common split capacitor bank.

For high power systems, Static VAR Compensators (SVC's) have been available for many years. The basic SVC is essentially a bank of capacitors which are switched into service as required to adjust the power factor of the system. In more recent years more sophisticated devices have become available employing thyristor controlled capacitor switches (TSC) and additionally thyristor switched reactors (TSR) (e.g. see ref [7.1]) enabling greater and more rapid VAr compensation. A new range of devices for use in high power systems started to appear during the 1990's extending the concept of the SVC with the use of GTO's (Gate Turn-Off devices). This new concept is generally referred to as STATCOM (STATic COMpensator) and is a VSC (Voltage Source

Converter) (see discussion ref [7.4]). The STATCOM device has some similarities with the inverter based APF circuit topology except that the STATCOM is not intended to remove the high order harmonic components of the load current from the source owing to switching speed limitations of high power handling devices.
There are a number of designs within the area of STATCOM devices which aim to overcome the problem of high power high frequency switching. One interesting technique involves phased switching of multiple capacitor banks and is referred to as a chain-circuit topology (see ref [7.4]). The capacitors are switched progressively in series to produce a stepped Voltage wave that follows the source Voltage wave.

Another technique for high power VAr and harmonic component removal involves the parallel use of GTO's for low frequency reactive current removal with IGBT's for higher frequency harmonic component removal (see ref [7.2]).

Yet another technique, known as a Unified Power Flow Controller (UPFC), consists of a parallel connected GTO based STATCOM together with a series connected GTO inverter. The dc Voltage of the parallel connected STATCOM energy storage capacitor is used via another GTO inverter to inject a series phase controlled Voltage via a series connected transformer (see fig 1.5).

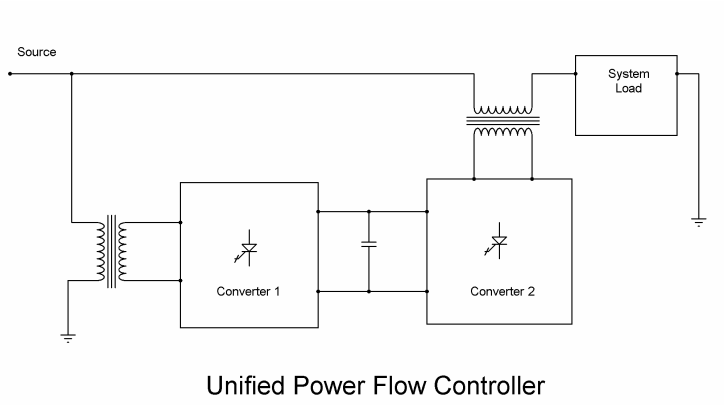


Fig 1.5: *Block Diagram of a Unified Power Flow Controller (UPFC)*

A power network can use some or all of the above devices:

- SVC
- TSC
- TSR
- STATCOM
- UPFC

Such a network actively controlling the VAr and harmonic components of current is referred to as FACTS (Flexible Alternative Current Transmission System) (see Ref [7.3]).

In the author's opinion, it seems inevitable that with the progressive improvement of device switching speeds and high Voltage power handling capability that the two areas of STATCOM and APF will merge.

1.3 Outline of the reported research work and contribution to existing knowledge

Existing literature concentrates on either the single-phase system or the three-phase system. The Reference section and Bibliography sections gives an indication of the breadth of work already carried out in the area of APFs. All available work uses an H-Bridge to shape the source current and focuses on some aspect of the control system which is usually given in terms of a continuous time approximation so that linear frequency transform techniques can be employed. Either hysterisis or PWM is used to translate the control output signal to drive the H-bridge. A different approach is taken in the work presented here since it is considered that the method of driving the H-bridge (i.e. deriving the switching signals) should not (in general) be treated in isolation from the control method. The control systems presented in this thesis are all sampled systems so there is a distinct move towards expressing the systems in a digital framework. The initial focus of the work of this thesis integrates sliding mode with a sampled switching system to form a version of discrete sliding mode. In later work, the combined methods proposed in chapter 5 using Energy Compensation with Proportional Hysterisis Control also require that H-bridge switching becomes an integral part of the control method. The thesis presents some existing ideas and

follows through a logical development supported by simulation and analysis while adding some new methods to achieve an improved design.
Chapter 3 introduces the sliding mode method and is investigated thoroughly both theoretically and in simulation. A different approach to Sliding mode presented from other researchers is similarly investigated. No sliding mode approach was found to give the desired system response. Linear control techniques were reviewed for comparison and were shown to provide reasonable responses but with poorer transient recovery times. The work leads to a new development based on energy calculations using the energy storage capacitor Voltage as a sense parameter. Using the capacitor as a sensor is a fairly common technique but a significant contribution of this thesis lies in the way the information is used to maintain the Capacitor Voltage at a desired reference level, obtain an input current reference which controls the input system conductance and control the switching hysterisis boundary to optimise the transient recovery time following a load change.

1.3.1 The Sliding Mode Method and the "Energy Compensation" method

A rigorous theoretical study of the APF using an implementation of the Sliding Technique with associated simulation models is presented. Some of the major criticisms of existing work in this area are the lack of operational details of the switching system and how to implement switching in the context of Sliding Mode. Furthermore, the rationale behind the method of deriving the source current reference is often overlooked. This thesis aims to unite existing knowledge in these areas and fill the gaps in this knowledge.
The principle of Sliding Mode requires convergence to a surface constructed in state space by switching the system structure between two discrete states as the state trajectory passes across the surface. Direction of the trajectory is always to reduce the error in the state variables. True sliding mode assumes that the system (in steady state) continually resides on the switching surface and as such would require a (theoretically) infinite bandwidth. The work presented in this thesis accepts that the system will never reside on the surface but near to it and builds this into a switching strategy that is referred to as Discrete Sliding Mode (DSM). An algorithm for the specific implementation of DSM in the context of the APF was developed.

Following on from the development of the APF model based on DSM and the associated simulation output, it was found that the DSM technique was not entirely suitable for APF control. Furthermore, analysis of existing Sliding Mode techniques gave questionable results. It will be shown that, in the author's opinion, the Sliding Mode technique for a state space order greater than zero is flawed. However a new technique emerged from the work based on "energy compensation" that provided an optimum control of critical APF parameters. Much of the analysis and techniques developed as part of the attempt to apply Sliding Mode were carried through to the work on "energy compensation", requiring only small changes to the simulation model. The zero-order switching trajectory was enhanced using a proportional hysterisis error boundary. Throughout the work a discrete approach was adopted for the control algorithms which was a natural consequence of starting with DSM. Energy Compensation in conjunction with Proportional Hysterisis current error control allowed optimum placement of the system poles in the Z-plane.

1.3.2 The APF Model

It was decided to base the work on the shunt Voltage-fed H-Bridge structure (see fig 1.1) owing to the benefits this has in low power applications where, in general, only the reactive and harmonic current components of the load have to be handled by the switching devices (see section 2.4.3 for specific cases). The popular H-Bridge configuration (used almost exclusively in all references to APF's) (see fig 1.6) has been updated in a manner similar to that shown in ref [8.3] to include another "arm" allowing more control flexibility and a better response (see fig 1.7). This new bridge will be referred to as the 3/2 H-Bridge.

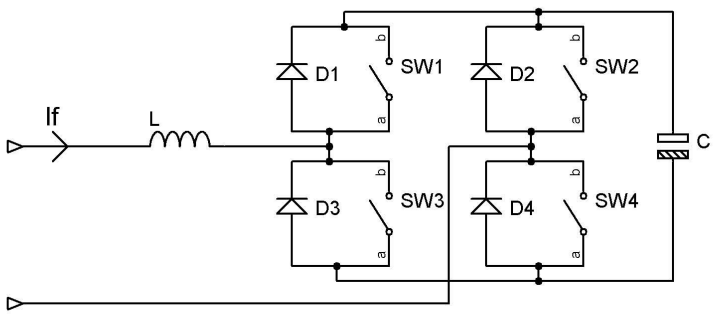


Fig 1.6: *Single Phase H-Bridge*

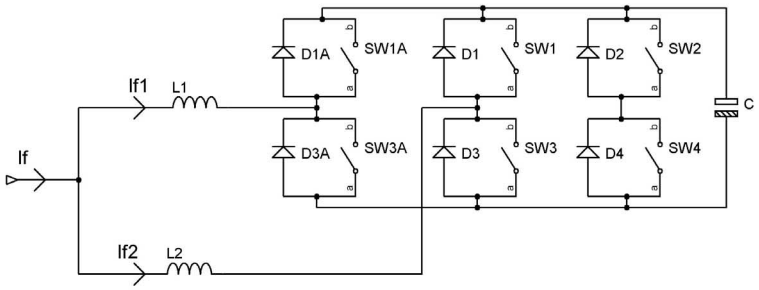


Fig 1.7: *Single phase 3/2 H-Bridge*

The range of harmonic loads that can be compensated is improved by use of the 3/2 H-Bridge. By dynamically switching the arms of the bridge the best compromise can be achieved using the "reachability condition" (see section 3.7) which reduces overshoot and helps the system follow a reference signal. The concept of switching bandwidth will also be introduced. The bandwidth resource determines the limit of harmonics that can be removed from the load and is dependent primarily on which arms of the 3/2 H-Bridge are in use and on the Voltage of the APF energy storage capacitor.

1.3.3 Practical Demonstration System

In order to demonstrate the effectiveness of the optimum solution using Energy Compensation and Proportional Hysterisis current error control, a system was built. For practical purposes a reduced Voltage was used (approx 53V RMS). An IGBT H-bridge was used together with a custom built 20mH 5A input inductor. The system was designed to allow the user total control over all relevant parameters and access to all necessary measurement points. The system successfully demonstrated the new techniques giving results as predicted by theory and simulation.

1.3.4 Summary of the Contribution to Knowledge

Several new ideas have resulted from the work contained in this thesis:

- An algorithm for applying Sliding Mode Control to a physical APF system including methods of deriving the reference signals
- The specification and design of an APF model

- A method for analysing the dynamic response of the APF
- Demonstrating the unsuitability of the sliding mode technique for APF control
- Application of the Energy Compensating principle together with Proportional Hysterisis current error control allowing optimum response of the APF supported by theory, simulation and a practical working system.

An important feature of this thesis is that the necessary mathematics and its application to the APF are developed in parallel and complement each other. Above all, it is intended that the reader of this thesis will be presented with a clear and unambiguous procedure to design an efficient and optimally controlled APF.

1.4 Aims and Objectives

The aims of this thesis are to investigate methods of reducing the impact of harmonic distortion on the mains current waveform introduced by non-linear loads (for example those produced by switching converters). The objectives are to review and investigate the most appropriate circuit topologies for an Active Power Filter (APF) and to develop a suitable control system that will effectively provide the switching signals necessary for the switching elements of the APF.

1.5 A Guide to the Thesis

The main work presented in this thesis falls into four parts covered by the chapters 2, 3, 4 and 5 with concussion contained in chapter 6.

Chapter 2 examines existing work on APFs and passive filtering techniques. Specifications for limits of distortion are discussed and some basic preparatory theory is dealt with.

Chapter 3 is a development of existing ideas specifically related to sliding mode control and its application to the shunt APF with several new additions and enhancements. In particular there is a deliberate move away from analogue techniques which places the system firmly into the sampled (discrete) domain. The results of simulation demonstrated some success; however the results were not entirely

conclusive and satisfactory. Analysis and comparison with results from other researchers (in particular ref [5.4]) showed some similarities but did not provide an acceptable system response. It was felt that existing research work did not demonstrate adequately the suitability of the sliding mode control method. It was considered that a new approach was necessary to re-investigate the APF control system.

Chapter 4 of the thesis introduces a variation of an existing technique based on "averaging". This approach to analysing the APF is based on a signal flow method using "Real Power Flow". Only those components of current responsible for carrying real power (not harmonic or reactive power) are considered. This analysis technique provided insight into the methods used in Chapter 3 and further demonstrated the unsuitability of the chosen Sliding Mode implementation. Both zero order and first order sliding models were analysed and the theoretical results compared to outputs from the APF simulation model developed in Chapter 3. The principle of APF control became much clearer enabling a new control method to be developed. The principle of this new control method, which is an enhancement of previous work mainly contained in Chapter 3 but also, in part, by other researchers (notably ref [8.1], [8.2], [8.3]) was implemented in the APF model developed in chapter 3. Real Power signal flow analysis gave accurate predictions of performance of the new APF model. It will be shown that this method provided an optimal control of critical parameters of the APF.

Chapter 5 of the thesis details the practical demonstration test system. Key constructional details are provided and discussed. Details relating to the schematics and controlling software are also provided. The results obtained from practical work are critically compared to those obtained from the APF model developed in chapter 4.

Chapter 6 of this thesis contains the conclusion of the work presented and recommendations for further work.

Chapter 2 Initial Investigations and Preparatory Theory

This Chapter contains the following preparatory work:

- Literature Review
- Limits of Harmonic Disturbance
- Active and Reactive Power Calculations
- Mains Harmonic Current removal: Passive and Active Filtering Methods
- Control Strategies for Shunt Active Power Filters

2.1 Literature Review

A review of existing research into APF's revealed a large body of knowledge indicated in the References & Bibliography sections of this thesis which has been categorised to enable an overview of the extent of work to be appreciated. A survey of the uses of APF's and their control methods is provided in Reference section 9 and Bibliography section 9 and in particular ref [9.2] was found to be a good introduction to the subject.

Classification of APFs is problematic since it depends on an individual's point of view however they all have the common purpose of providing compensation for load generated reactive and harmonic power. Compensation techniques normally aim to reduce the reactive and harmonic content of the offending load *current* whereas *Voltage* harmonics are not normally dealt with owing to the low impedance of the supply. All of the APF references given in the Reference section and Bibliography section of this thesis aim to reduce reactive and harmonic power by re-shaping the current, each with its own variant of control technique. By reducing the harmonic and reactive current components it is assumed that distortion of the supply Voltage can be reduced.

It was decided to subdivide existing work into two main areas of either three phase APFs or single-phase APFs. It was then decided to subdivide each of these areas in terms of the switching technique and then further sub-divide in terms of the control method. It is also possible to subdivide APFs into "shunt" and "series", however series APF work is not referenced here. The focus of this thesis is only on the shunt APF owing to the fact that the series APF must handle higher currents (i.e. include the real power component) – see section 1.2.

This thesis is concerned with single phase systems but three phase methods were included for completeness. Single phase methods mainly use the conventional Voltage-fed H-Bridge (where the energy store is a capacitor). There are two aspects of the APF design to consider:

- The method of driving the H-bridge switching elements
- The method of control

Virtually all researchers use the PWM technique to drive the switching elements of the H-bridge (see Bibliography section 5). The hysterisis drive technique is used to a lesser extent.

Control methods must deal with the issues of generating the source current reference, control of the energy storage capacitor Voltage and obtaining a suitable transient response to changes in non-linear load.

A distinction is usually made between reactive-compensation and harmonic-compensation. However, since the prime concern is with non-linear loads in the presence of a possibly distorted Voltage, then the distinction between reactive power and harmonic power is blurred. It is therefore important to define these terms and this is dealt with in section 2.3.3. There are a number of solutions to the control problem most of which are analysed in the continuous time domain but implementation can be either using analogue hardware or DSP.

The following lists the control methods that researchers have employed in the single phase methods:

- Proportional plus Integral (PI) control
- Predictive/Dead Beat control
- Adaptive/Neural techniques
- Sliding Mode (Variable Structure Control)
- Fuzzy Logic control
- Magnetic flux compensation
- Capacitor energy control

Sliding mode (being one of the newer methods for investigation; refs [5.2], [5.3], [5.4], [5.5], [5.6], [5.7] and [6.1]) appeared to offer some promising results. Being worthy of further study, Sliding Mode was the initial focus for the work contained in this thesis. Much of the existing research work uses PWM as the means of translating the H-Bridge control signal into a switching waveform suitable for driving the bridge switching transistors. The Sliding technique generates a switching output directly which is used to drive the H-bridge switching transistors. In some respects therefore the Sliding mode technique is a development of the Hysterisis technique used by other researchers (Ref [5.1], [8.1], [8.2], [8.3]). The DSM technique developed in this thesis is a combination of the Hysterisis approach and Sliding Technique linked to a sampling clock.

2.2 Limits of Harmonic Disturbance

This section presents a study of the relevant specifications applicable to harmonic disturbance. It is necessary to have a measure of performance so that the effectiveness of the simulation models and practical results can be assessed. Use of the Total Harmonic Distortion (THD) measure will be made.

A good background to the causes of concern for the quality of mains power can be found in ref [7.4].

Two aspects need to be addressed

- The absolute limits in terms of allowable harmonic current levels and the evaluation of a current THD
- The effect of harmonic currents on the Voltage supply and the evaluation of a Voltage THD

The specification most applicable for harmonic components in loads is given in refs [2.3] and [2.4]. The focus in this thesis is on single phase domestic loads (i.e. $\leq$ 16A) therefore current limits will be taken specifically from ref [2.3].

The intention of the work presented in this thesis is to remove reactive and harmonic distortion from the mains supply, which is caused by non-resistive load components. Using a controlled switching system the supply current must be forced to be proportional to the mains Voltage. It is important to note that this does not mean that (as in many of the existing methods) the intention is to force the supply current to be sinusoidal, since the Voltage itself may contain distortion for other reasons (for example supply transformer saturation). Forcing the current to follow the mains Voltage will make the combined load/APF look resistive which is discussed in section 2.4.2.3.

The following is an extract from ref [2.1] section 4.3 that is highly relevant to the situation under consideration:

> *"In specifying compatibility levels for harmonics, two facts must be considered. One is the increase of the number of harmonic sources. The other is the decrease of the proportion of purely resistive loads (heating loads), which function as damping elements, in relation to the overall*

load. Therefore increasing harmonic levels are to be expected in power supply systems until the sources of harmonic emissions are brought under effective limits"

The APF strategy of forcing the source current to follow the source Voltage is implicit in the above paragraph since the non-linear load then behaves as a pure resistive heating load which aids damping of the overall system.

There are practical limitations to the removal of distorting harmonics from the domestic mains supply; it is therefore necessary to specify an acceptable limit to the allowable distortion.

Ref [2.3] specifies the harmonic currents for class A, B, C and D equipment. Class A equipment includes household appliances, portable tools, lamp dimmers and audio equipment. Therefore class A is considered most appropriate for this work whose focus is on single phase domestic appliances.

Class A harmonic limits are given in table 2.1:

Limits for Class A equipment

Harmonic order n	**Maximum permissible harmonic current** A
Odd harmonics	
3	**2.30**
5	**1.14**
7	**0.77**
9	**0.40**
11	**0.33**
13	**0.21**
15 ≤ n ≤ 39	**0.15 . 15/n**
2	**1.08**
4	**0.43**
6	**0.30**
8 ≤ n ≤ 40	**0.23 . 8/n**

Table 2.1*: Class A harmonic current limits as given in ref [2.3]*

Ref [2.3] defines total harmonic current as follows:

$$\text{Total harmonic current} = \sqrt{\sum_{n=2}^{40} I_n^2} \qquad \text{-----\{eqn 2.1\}}$$

Note that the sum extends to the 40th harmonic (i.e. 2kHz for the standard 50Hz mains source).

Evaluating from the 2nd up to the 40th harmonic at the allowable levels given in table 2.1, the Total harmonic current is calculated as 3.0419 A RMS.

Voltage harmonic disturbance as a result of the worst case limits given in table 2.1 can be evaluated by knowing the supply impedance. Ref [2.5] gives the supply

impedance as 0.15 + j 0.15 Ohms for a phase conductor and 0.1 + j 0.1 Ohms for a neutral conductor. The total impedance is 0.25 + j 0.25 Ohms.
At 50Hz this is equivalent to a resistance of 0.25 Ohms in series with an inductor of 796 μH.
To evaluate the effect of harmonic currents on the Voltage source a measure of the total harmonic Voltage is required which can be found as follows:

$$\text{Total harmonic Voltage} = \sqrt{\sum_{n=2}^{40} V_n^2} \qquad \text{-----\{eqn 2.2\}}$$

Based on the harmonic currents and source impedance the Total harmonic Voltage can be evaluated as follows:

$$\text{Total harmonic Voltage} = \sqrt{\sum_{n=2}^{40} \left(R^2 + (2\pi f_0 Ln)^2\right) I_n^2} \qquad \text{-----\{eqn 2.3\}}$$

Where f_0 is the fundamental mains frequency; R and L are the specified source resistance and inductance respectively.
Using eqn 2.3, the calculated Total harmonic Voltage using the absolute maximum current of Table 2.1 with a source impedance as given above is 4.2307V RMS.

EN 61000-2-2:2002 ref [2.1]: "Compatibility levels for low-frequency conducted disturbances and signalling in public low-Voltage power supply systems" is the "European Normalised standard for specifying the allowable conducted harmonic Voltage levels up 9 kHz".
It defines Total Harmonic Distortion (THD) as follows:

$$THD = \sqrt{\sum_{h=2}^{h=H} \left(\frac{Q_h}{Q_1}\right)^2} \qquad \text{-----\{eqn 2.4\}}$$

where h is the harmonic number (h=1 refers to the fundamental) and
H is the maximum harmonic to be considered (H is normally 50 but 25 if the risk of higher harmonics is low).
Q_h is the RMS value of the h^{th} harmonic and Q_1 is the RMS value of the fundamental.
Current THD is similarly defined in ref [2.4] for summation of harmonic numbers 2 to 40.

Ref [2.3] assumes a maximum phase load current of 16A. Using Q1 = 16 A RMS and the worst case harmonic current levels of table 2.1, eqn 2.4 gives the maximum allowable current THD as 3.0419/16 = 0.19 (19%). Similarly, using Q1 = 240V RMS, the maximum Voltage THD allowable with the current levels as given in Table 2.1 with the given source impedance is 4.2307V/240 = 0.0176 (1.76 %).

2.2.1 Long and Short Term Harmonic Specification

The concept of a long and short term Harmonic specification is derived form ref [2.1] which is concerned with mains disturbances up to 9kHz with an extension to 148.5kHz for mains signalling. The subject of APF's is not relevant above the 40th harmonic owing to the limited bandwidth of the switching converter. Frequencies above 2kHz are generally removed using passive filtering.
Section 4.3 of ref [2.1] specifies harmonic distortion for long term effects and short-term effects.

"*The long term effects relate mainly to thermal effects on cables, transformers, motors, capacitors etc. They arise from harmonic levels that are sustained for 10 min or more*."
"*Very short –term effects relate mainly to disturbing effects on electronic devices that may be susceptible to harmonic levels sustained for 3 sec or less. Transients are not included*."

The standard ref [2.1] defines "long term" as in excess of 10 minutes and over this period the THD should not exceed 8%.
A table is included in ref [2.1] for the allowable levels of each Voltage harmonic as a percentage of the fundamental and is reproduced here:

Odd Harmonics Non-Multiples of 3		Odd Harmonics Multiples of 3		Even Harmonics	
Harmonic Order h	Harmonic Voltage %	Harmonic Order H	Harmonic Voltage %	Harmonic Order h	Harmonic Voltage %
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.4	6	0.5
13	3	21	0.3	8	0.5
$17 \leq h \leq 49$	2.27x(17/h)-0.27	$21 < h \leq 45$	0.2	$10 \leq h \leq 50$	0.25x(10/h)+0.25

Table 2.2*: Allowable levels of each harmonic as a percentage of the fundamental*

The levels defined in ref [2.1] for short term, are those in the above table, scaled by a factor k where:

$$k = 1.3 + \frac{0.7}{45}(h-5)$$

Short term harmonic distortion is that which is sustained for 3 seconds or less, but does not include transients. The allowable THD = 11%.

2.2.2 Interpreting a Voltage THD specification

It would appear from the discussion in section 2.2 that provided the absolute levels of current in Table 2.1 are not exceeded then the Voltage THD at the point of coupling will not exceed 1.76% which is well below both the short and long term EMC requirements. It should be noted however that the quality of the supply Voltage before any load is applied cannot be controlled, consequently the aim is to minimise *additional distortion* caused by the load. If the supply current is actively forced to follow the Voltage, then it will make the load look resistive. This means that any harmonic distortion present in the Voltage waveform at the point of supply will remain but will not be made any worse.

2.2.3 Voltage and current THD specification for higher current levels

Two specifications (ref [2.2] and [2.4]) are given for the higher current levels. Reference 2.4 is for currents in excess of 16A and up to 75 A. Table 2.3 is an extract from ref [2.4]

Minimal R_{sce}	Admissible individual harmonic current I_n/I_1 [a] %				Admissible harmonic current distortion factors %	
	I_5	I_7	I_{11}	I_{13}	*THD*	*PWHD*
33	10,7	7,2	3,1	2	13	22
66	14	9	5	3	16	25
120	19	12	7	4	22	28
250	31	20	12	7	37	38
≥350	40	25	15	10	48	46
The relative values of even harmonics up to order 12 shall not exceed 16/*n* %. Even harmonics above order 12 are taken into account in *THD* and *PWHD* in the same way as odd order harmonics. NOTE Linear interpolation between successive R_{sce} values is permitted. See also Annex B.						
[a] I_1 = reference fundamental current; I_n = harmonic current component.						

Table 2.3: Current emission limits for balanced three phase equipment

It is evident from table 2.4 that the allowable limits for higher current levels are significantly relaxed in comparison with the maximum allowable limits inferred by ref [2.3] for class A equipment.

Reference [2.2] is the G5/4 specification for Harmonic Limits as required by the Electricity Association (EA) of manufacturers, and power consumers and covers harmonic distortion up to the 50th harmonic with three phase systems. This is a UK specification and is more stringent than the G5/3 specification that it replaces. Companies required to investigate their harmonics must, in accordance with G5/4, record measurements over at least a seven day period. The limits are as follows:

Harmonic	G5/4 Table 12 – 11kV	G5/4 Table 7 – 400V
Current	(A)	(A)
Fundamental	N/A	N/A
I_3	6.6	48.1
I_5	3.9	28.9
I_7	7.4	41.2
I_9	1.8	9.6
I_{11}	6.3	39.4
I_{13}	5.3	27.8
I_{17}	3.3	13.6
I_{19}	2.2	9.1
I_{23}	1.8	7.5
I_{25}	1.0	4.0
I_{29}	0.8	3.1
I_{31}	0.7	2.8
I_{35}	0.6	2.3
I_{37}	0.5	2.1
I_{41}	0.4	1.8
I_{47}	0.3	1.4
I_{49}	0.3	1.3

Table 2.4: *G5/4 Current Distortion Limits*

Total current distortion is limited on a harmonic by harmonic basis measured in absolute amps

Harmonic	G5/4 – 11kV	G5/4 – 400V
Order	Harmonic Voltage %	Harmonic Voltage %
5	3	4
7	3	4
11	2	3
13	2	2.5
17	1.6	1.6
19	1.2	1.2
23	1.2	1.2
25	0.7	0.7
29	0.63	0.63
31	0.60	0.60
35	0.56	0.56
37	0.54	0.54
41	0.5	0.5
47	0.47	0.47
49	0.46	0.46

Table 2.5: *G5/4 Voltage Distortion Limits*

The total Voltage distortion must not exceed 5% in 400V systems and 4% in 6.6kV, 11kV and 20 kV systems

More detailed information relating to Voltage distortion is taken from table 1 of the G5/4 specification (ref [2.2]):

Table 1: G5/4 Harmonic Limits (Voltage Distortion) at 415V

Odd Harmonics (Non Multiple of 3)		Odd Harmonics (Multiple of 3)		Even Harmonics	
Order 'h'	Voltage (%)	Order 'h'	Voltage (%)	Order 'h'	Voltage (%)
5	4.0	3	4.0	2	1.6
7	4.0	9	1.2	4	1.0
11	3.0	15	0.3	6	0.5
13	2.5	21	0.2	8	0.4
17	1.6	>21	0.2	10	0.4
19	1.2			12	0.2
23	1.2			>12	0.2
25	0.7				
>25	0.2 + 0.5(25/h)				

Limit for Total Harmonic Distortion = 5%

Table 2.6: *G5/4 Harmonic Limits (Voltage Distortion) at 415V*

2.2.4 THD as a performance indicator

From the preceding discussion it becomes apparent that there are two viewpoints with regard to a Voltage THD limit for lower power single-phase domestic equipment (current up to 16A). Either the limit is inferred from absolute worst case data as given in Table 2.1 with respect to some specified source impedance or is obtained from EMC specifications (ref [2.1]). Furthermore the current harmonic distortion is not

perceived as a problem unless the total harmonic current from all apparatus at the point of supply (i.e. at the supply meter of a domestic installation for example) encroaches onto limits of Table 2. Nevertheless, it is necessary to establish a performance indicator to assess the quality of the methods developed in this thesis. The loads used in this thesis for assessment are not designed to handle the power necessary to incur such current harmonic limits, however the THD concept will be retained as a relative measure of performance, since in principle, the system could be scaled to more demanding power levels. Therefore for simulated results and measured practical results four measures will be made:

- A load current total harmonic measure (based on harmonic numbers 2 to 40)
- A source current total harmonic measure (based on harmonic numbers 2 to 40)
- A load current THD measure
- A source current THD measure

A Voltage THD value based on the standard source impedance of 0.25 Ohm and 796 μH will be obtained from calculation.

Absolute performance indicators will be as follows:

- For all test loads, the source current total harmonic distortion must not exceed 19%
- The Source Voltage total harmonic distortion must not exceed 1.76%

Relative performance indicators will be the difference in current THD of load and source currents.

2.3 Active and Reactive Power Calculations

There are three main goals of an APF:

- That which reduces the harmonic content of the source current waveform
- That which reduces the reactive content of the source current waveform
- Improve the power factor

(see refs [7.1], [7.4], [7.5], [7.6])

Improvement of the power factor is a direct consequence of reducing the reactive current component.

In order to achieve the three goals of the APF, a current reference must be available that has the same waveshape as the source and must be in-phase with the source Voltage. The derivation of the current references will be dealt with in depth in a later chapter. The magnitude of the source reference current must be such that under steady state conditions (for an unchanging load) it represents the real power component of the load.

By reducing the harmonic content, much of the watt-less component of VA is reduced. By forcing the current to follow the Voltage, the power factor (dependent on phase between Voltage and current) is forced towards unity and as a result the reactive component is reduced. Normally, the load current will contain three parts referred to as the "Active Current", the "Reactive Current" and the "Harmonic Current". These terms are defined in section 2.3.3. Sections 2.3.1 and 2.3.2 present the necessary theory of real power components and watt-less components.

2.3.1 Active and reactive power calculations in a single phase sinusoidal system

For simplicity the Voltage source will be assumed to contain no harmonics and consist just of the fundamental. This will be the case when the APF simulation model is developed in Chapter 3.

Let the supply be given by:

$$v_s(t) = V\sin(\omega t) \qquad \text{-----\{eqn 2.5\}}$$

and the supply current be given by:

$$i_s(t) = I\sin(\omega t + \phi) \qquad \text{-----\{eqn 2.6\}}$$

then instantaneous power is given by

$$p(t) = V\sin(\omega t).I\sin(\omega t + \phi) = V.I\left(\cos(\phi)\sin^2(\omega t) + \sin(\phi)\sin(\omega t)\cos(\omega t)\right)$$

$$\text{-----\{eqn 2.7\}}$$

The following example (Figs 2.1, 2.2, 2.3) applies a source Voltage of peak 340V to a load consisting of 150 Ohms in series with a capacitor of 10μF. It will be seen that the power waveform has a net positive value (the real average power) but also contains a component that averages to zero (the reactive power).

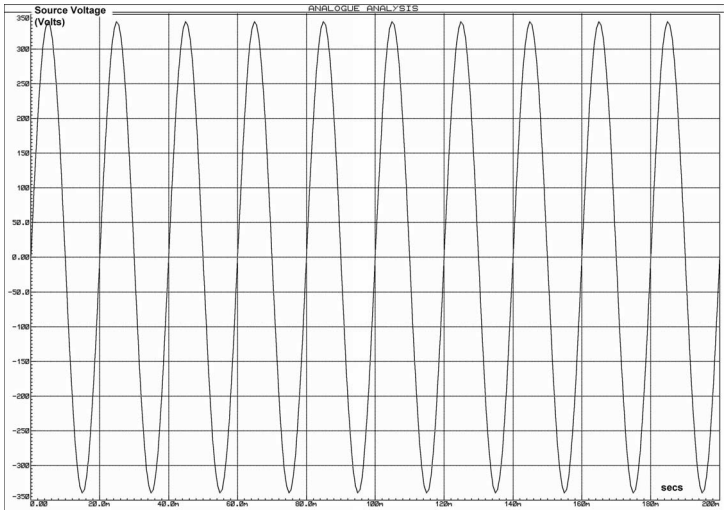


Fig 2.1: *Source Voltage(t)*

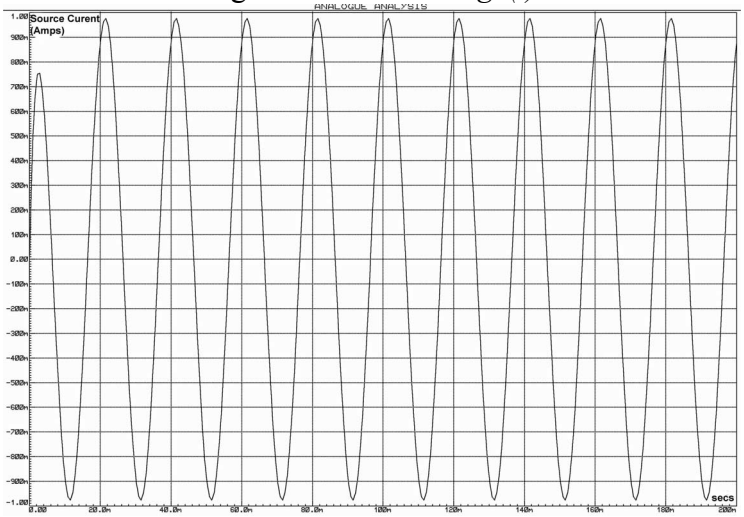


Fig 2.2: *Source Current(t)*

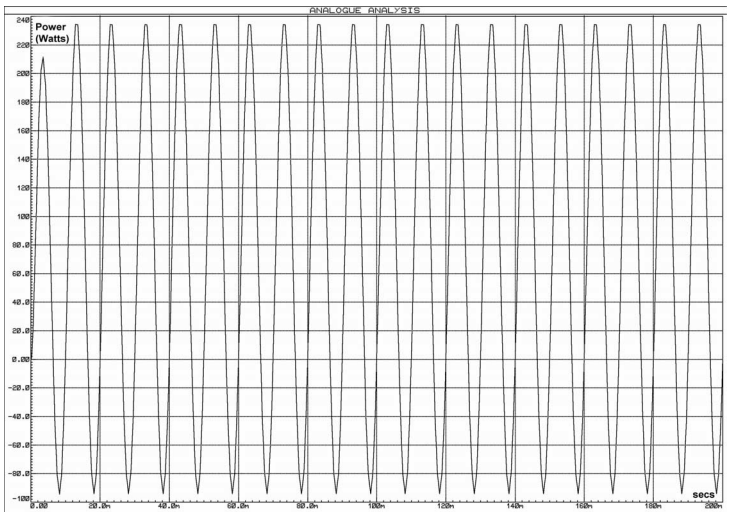


Fig 2.3: *Power to load(t)*

It can be seen that the power contains a dc and an ac component.

The average power is found from:

$$\frac{1}{T}\int_0^T I.V.\sin(\omega t).\sin(\omega t+\phi)dt = \frac{1}{2}I.V.\cos(\phi) \qquad \text{-----\{eqn 2.8\}}$$

Alternatively this can be viewed as:

Average value over one period of $(V.I.\sin(\omega t).(\sin(\omega t)\cos\phi+\cos(\omega t).\sin\phi))$

= average value $\left(V.I.\sin^2(\omega t)\cos\phi+V.I.\sin(\omega t)\cos(\omega t)\sin\phi\right)$

$= \frac{1}{2}V.I.\cos\phi+0$

The amplitude of the oscillatory power component that averages to zero is

$V.I.\sin\phi$ -----{eqn 2.9}

The active current component is $I\sin(\omega t)\cos\phi$ -----{eqn 2.10}

The reactive current component is $I\cos(\omega t)\sin\phi$ -----{eqn 2.11}

The RMS value of the load current = $I_{RMS} = \frac{I}{\sqrt{2}}$ -----{eqn 2.12}

The RMS value of the source Voltage = $V_{RMS} = \frac{V}{\sqrt{2}}$ -----{eqn 2.13}

The RMS value of the active current component is $\frac{I\cos\phi}{\sqrt{2}}$ -----{eqn 2.14}

The RMS value of the reactive current component is $\frac{I\sin\phi}{\sqrt{2}}$ -----{eqn 2.15}

The real average power delivered to the load = $I_{RMS}.V_{RMS}.\cos\phi$ -----{eqn 2.16}

The reactive power that oscillates between load and source is

$2.I_{RMS}.V_{RMS}.\sin(\omega t).\cos(\omega t).\sin\phi = I_{RMS}V_{RMS}\sin(2\omega t)\sin\phi$ -----{eqn 2.17}

The apparent power delivered to the load = $I_{RMS}.V_{RMS}$ -----{eqn 2.18}

The power factor is given by:

$$\frac{\text{Real Power}}{\text{Apparent Power}} = \frac{I_{RMS}V_{RMS}\cos\phi}{I_{RMS}V_{RMS}} = \cos\phi \qquad \text{-----\{eqn 2.19\}}$$

i.e. for the case of a sinusoidal load current with no harmonic distortion, the power factor is $\cos\phi$.

2.3.2 Active, Reactive and Harmonic Power in a Single phase system with periodic non-sinusoidal load current and APF control of the supply current

If it is assumed that the unloaded source Voltage is sinusoidal then it is reasonable to assume that the combination of a non-linear load and APF will result in a source Voltage that is also sinusoidal even although the load current is non-sinusoidal. This is true for two reasons which are:

a) That the source impedance is normally very low
b) That an APF will attempt to force the source current to follow the Voltage thereby making the load appear purely resistive and removing much of the local harmonic distortion from the source Voltage.

Therefore it is reasonable to continue to assume that the source Voltage is $V\sin(\omega t)$.

If in steady state the load current is periodic then it can be given by:

$$I_L(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t) \qquad \text{-----\{eqn 2.20\}}$$

where a_n and b_n are the amplitudes of the nth odd and even harmonics and

$a_0/2$ is the average (dc) current

Let $b_n = I_{Ln}\cos\phi_n$ -----{eqn 2.21}

and $a_n = I_{Ln}\sin\phi_n$ -----{eqn 2.22}

(ϕ_n is the phase relative to the n^{th} harmonic Voltage)

Then the phase of the nth current harmonic is:

$$\phi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right) \qquad \text{-----\{eqn 2.23\}}$$

The amplitude of the nth current harmonic is:

$$I_{Ln} = \sqrt{a_n^2 + b_n^2} \qquad \text{-----\{eqn 2.24\}}$$

$I_L(t)$ eqn {2.20} can be re-written as:

$$I_L(t) = \frac{I_{L0}}{2} + \sum_{n=1}^{\infty} I_{Ln}\sin(n\omega t + \phi_n) \qquad \text{-----\{eqn 2.25\}}$$

($I_{L0}/2$ is the average dc current i.e. I_{L0} = 2* average current).

The instantaneous power in the load is then given by:

$$p(t) = V\sin\omega t\left(\frac{I_{L0}}{2} + \sum_{n=1}^{\infty} I_{Ln}\sin(n\omega t + \phi_n)\right) \qquad \text{-----\{eqn 2.26\}}$$

The average value (over one period) of this power function is given by:

Average value of (p(t))

$$= \text{ave value}\left(V.\frac{I_{L0}}{2}\sin(\omega t) + V.I_{L1}.\sin(\omega t)\sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} V.I_{Ln}\sin(\omega t)\sin(n\omega t + \phi_n) \right)$$

= average value of

$$\left(V.\frac{I_{L0}}{2}\sin(\omega t) + V.I_{L1}.\sin(\omega t)\cos(\omega t).\sin\phi_1 + V.I_{L1}.\sin(\omega t).\sin(\omega t)\cos\phi_1 + \sum_{n=2}^{\infty} V.I_{Ln}\sin(\omega t)\sin(n\omega t + \phi_n) \right)$$

$$= \frac{V.I_{L1}}{2}\cos\phi_1 \qquad \text{-----\{eqn 2.27\}}$$

The result for the average (real) power delivered to the load in the case of a distorted periodic current (eqn {2.27}) is similar to that for the non-distorted sine wave case (eqn {2.8}). Note that all the additional harmonics do not contribute to the (average) real power.

The component of power oscillating between source and load that averages to zero is:

$$\left(V.\frac{I_{L0}}{2}\sin(\omega t) + V.I_{L1}.\sin(\omega t)\cos(\omega t).\sin\phi_1 + \sum_{n=2}^{\infty} V.I_{Ln}\sin(\omega t)\sin(n\omega t + \phi_n) \right)$$

In this expression the component of power: $V.I_{L1}.\sin(\omega t)\cos(\omega t).\sin\phi$ is the reactive part since it only contains frequencies found in the Voltage waveform.

The remaining terms $\left(V.\frac{I_{L0}}{2}\sin(\omega t) + \sum_{n=2}^{\infty} V.I_{Ln}\sin(\omega t)\sin(n\omega t + \phi_n) \right)$ constitute the harmonic part since the current harmonics are not contained in the Voltage waveform.

The various current components of the distorted periodic load current are as follows:

The active current component is: $I_{L1}\sin(\omega t)\cos\phi_1$ -----{eqn 2.28}

The harmonic current component is: $\left(\frac{I_{L0}}{2}_{1} + \sum_{n=2}^{\infty} I_{Ln}.\sin(n\omega t + \phi_n) \right)$ -----{eqn 2.29}

The reactive component of current is: $(I_{L1}\cos(\omega t).\sin\phi_1)$ -----{eqn 2.30}

Other current and Voltage relationships relating to the distorted periodic load current:

The RMS value of the load current = $I_{RMS} = \sqrt{\frac{I_{Lo}^2}{4} + \sum_{n=1}^{\infty} \frac{I_{Ln}^2}{2}}$ -----{eqn 2.31}

The RMS value of the source Voltage = $V_{RMS} = \frac{V}{\sqrt{2}}$ -----{eqn 2.32}

The RMS value of the active current component is $\frac{I_{L1} \cos \phi_1}{\sqrt{2}}$ -----{eqn 2.33}

The RMS value of the reactive and harmonic current component is

$$\sqrt{\frac{I_{Lo}^2}{4} + \frac{I_{L1}^2}{2} \sin^2 \phi_1 + \sum_{n=2}^{\infty} \frac{I_{Ln}^2}{2}}$$ -----{eqn 2.34}

The apparent power delivered to the load = $I_{RMS}.V_{RMS}$ -----{eqn 2.35}

The power factor can be defined as: $\frac{1}{2} \frac{V I_{L1} \cos \phi_1}{V_{RMS}.I_{RMS}}$ -----{eqn 2.36}

2.3.3 Defining Harmonic and Reactive Currents in the presence of a distorted Source Voltage

This thesis will use three terms to define specific components of the current waveform.

The *Active Current* is that part that delivers the real power. It consists of the current fundamental component in phase with the fundamental Voltage component plus the higher current harmonics that are in phase with any Voltage harmonics (for a distorted source Voltage)

The *Reactive Current* is that part of the current that contains the fundamental and higher harmonics at 90 degrees to the corresponding Voltage fundamental and higher harmonics. These components deliver no useful power. For example, if the source Voltage has a significant third harmonic, then the third harmonic of the current with zero power-factor with respect to the third harmonic of the Voltage will be referred to as a reactive component.

The *Harmonic Current* comprises those harmonics above the fundamental at frequencies that are not contained in the source Voltage, (i.e. at frequencies above the significant spectral components of the source Voltage). These components deliver no useful power.

2.4 Mains Harmonic Current removal: Passive and Active Filtering Methods

There are basically two methods of removal of unwanted current harmonics. These two methods fall into the categories of serial and parallel (shunt). The techniques employed can either be passive (see ref [1.3]) or active. Although much has been written about active power filters, a good overview is presented in ref [9.1] from which the following diagram is taken:

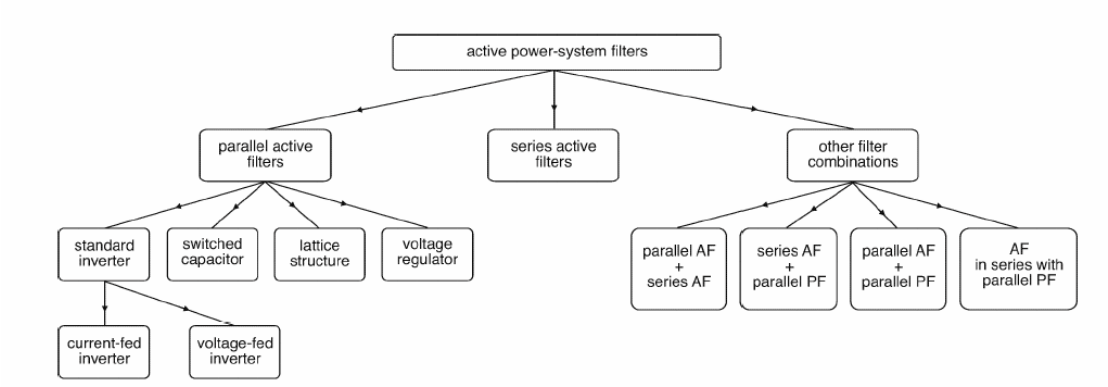


Fig 2.4: *Subdivision of power system filters according to power circuit configurations and connections*
AF: Active filter
PF: Passive filter

Whatever method is used for filtering, the purpose of the filter is to attenuate the unwanted harmonics to a level that meets the given specification (as discussed in section 2.2).

2.4.1 Passive filtering

The main applications for passive filtering systems are in low power apparatus where they are used for the removal of both low frequency harmonics of the supply frequency (i.e. conducted EMC emissions) and for the removal of high frequency components above 30MHz (i.e. radiated EMC emissions) (see ref [1.3]).
Active filters are only suitable for low frequency harmonic removal (typically up to 1kHz).
A passive circuit is connected in series or parallel (or both) with the non-linear load (fig 2.5).

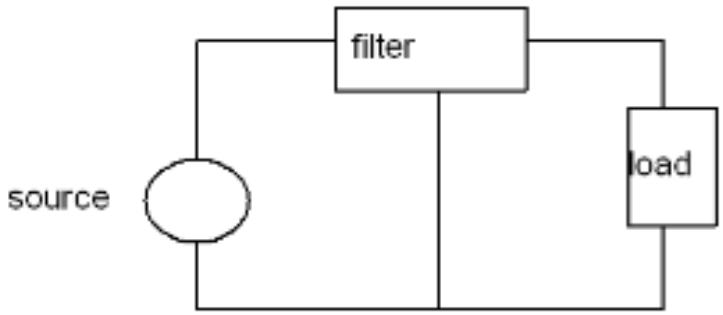


Fig 2.5: *passive series connected filter*

If such a filter contains lossy elements such as a resistor or ferrite component, then the harmonic energy is dissipated within the filter. If the filter contains reactive elements then the energy is reflected back to the load.

The passive filter often consists of a series inductor and parallel-connected capacitors (fig 2.6).

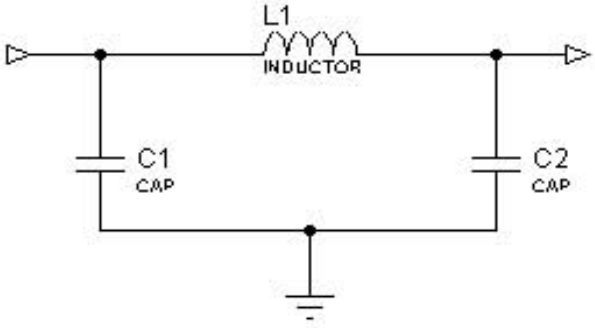


Fig 2.6: *A typical series passive filter*

Such a network may be inserted on both the live and neutral lines of the source. The capacitors would need to be Y rated (connection line to earth). Additionally X rated (connection line to line) capacitors may be connected between live and neutral. The filter inductance must be designed so that the core does not saturate at maximum load currents and reduce the inductive value. For higher frequency component elimination, consideration must be given to the self-capacitance of the inductor. Higher numbers of turns in the inductor coil increases the self-capacitance and higher permeability cores also tend to have higher dielectric constants. Careful layout of the core winding such as wide separation and a multi section bobbin will help reduce self-capacitance.

Parallel-connected capacitors are normally intended for high frequency removal and lossy ceramic capacitors are advantageous (such as dielectrics X7R, Y5V, Z5U).

The network (fig 2.6) will be effective at eliminating differential mode harmonic currents. However to eliminate common mode harmonics (normally when addressing problem related to EMC conducted emissions) a common mode choke is employed, which together with differential mode capacitors results in the circuit of fig 2.7.

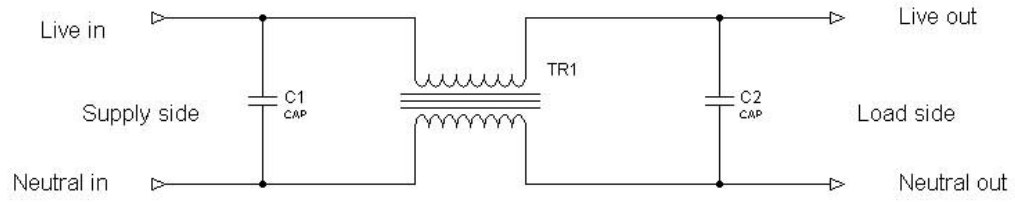


Fig 2.7*: Common mode input filter*

Additionally capacitors may be connected to earth at the load side as shown in fig 2.8.

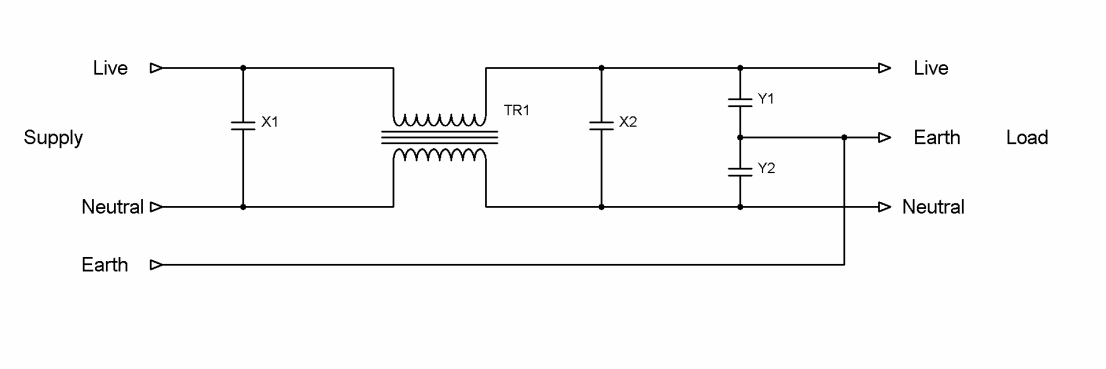


Fig 2.8*: Common mode input filter with additional differential mode suppression capacitors*

Note the use in fig 2.8 of X1 and X2 rated capacitors between live and neutral and Y1 and Y2 rated capacitors to earth. Such capacitors are designed for the failure modes that can occur in these situations.

The passive filters described here are effective for low power applications but they suffer from many problems.

Differential-mode passive filter problems:

- Inductor core must not saturate. Saturation leads to reduced inductance and ineffective filtering.
- The inductor wire must offer low series resistance.
- The inductor will inevitably be bulky and expensive
- Capacitors must have high ripple current capability and be rated for use between live and earth.

Common-mode passive filter problems:

- Capacitors must have high ripple current capability and be rated for use between live and neutral.
- The common mode choke must offer minimal series resistance.
- Any imbalance between live and neutral currents will cause saturation of the core.

The biggest drawback of these passive filters is that they are connected to the input of the load and as such must handle the full load current.

2.4.2 Active Filtering

This section examines the two basic types of Active filters which are the Series-Connected and the Parallel-Connected.

2.4.2.1 Active Series Connected Filters

Active series connected filters will use switching techniques to attempt to force the input current waveform to either follow a sinewave (in phase with the source Voltage fundamental) or directly follow the mains Voltage supply. An energy store is required as a buffer between the input and output switching converters:

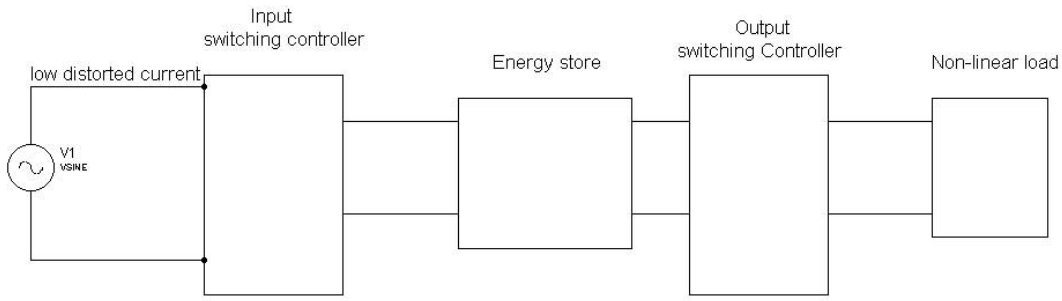


Fig 2.9*: Block diagram showing a series connected Active Filter between source and load*

The energy store can either be capacitive or inductive depending on the design. If the energy store is inductive then the APF is referred to as a current source and if capacitive then a Voltage source APF.

As with the passive series input filter, the main drawback is that the filter switching components have to be rated to carry the main load current.

2.4.2.2 Active shunt connected filters

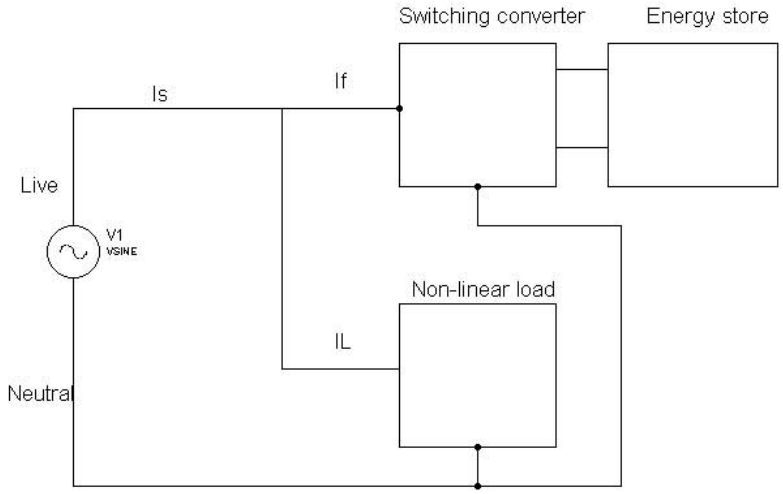


Fig 2.10*: Block diagram showing the connection for a shunt Active Filter*

The filter consists of a switching converter and an energy store that can be inductive or capacitive (but capacitive types are more common and practical). The current drawn by the filter plus the current drawn by the non-linear load is forced to follow either a sinewave (in phase with the source Voltage fundamental) or the mains Voltage directly with the purpose of eliminating the harmonics introduced by the load.

Of the entire range of filter types presented this is the most effective for larger power loads since the filter is not expected to carry the full load current, it is only generally expected to compensate for the unwanted harmonics (see ref [9.1]). Effectively the filter circuit resonates with the load at the unwanted harmonic frequencies. The filter supplies the unwanted harmonics (which have been shown in section 2.3.2 to carry no real power) while the real power is drawn from the mains supply. Under certain

conditions the filter also acts as a buffer for real power by acting as a frequency changer moving real power from one harmonic to another (see section 2.4.3).

2.4.2.3 Active shunt filters synthesising a resistive load

Attention is drawn to the fact that the ideal supply current waveform (I_s) is that which follows the mains supply Voltage waveform, not (as sometimes assumed) a pure sine wave. By forcing the source current to be proportional and in phase with the source Voltage at the point of common coupling, the composite load current ($I_f + I_L$) will present only a resistance to the supply, i.e. the APF synthesises a resistive load. The ideal current is therefore $K.V_s$ where the proportionality constant K is the *input conductance* of the composite load and V_s is the time dependent source Voltage. Much work in this area assumes that the ideal current to be drawn from the source should be sinusoidal, ignoring the fact that the source Voltage is often not sinusoidal but itself contains harmonic distortion. When the source Voltage is distorted, resistive synthesis will have the effect of drawing active power from the source harmonics. As stated in ref [3.3], if an APF draws sinusoidal current from a distorted source, the source's Voltage harmonics do not contribute to the active power but increase the apparent power which reduces the power factor when compared to a system using resistive synthesis. Also transmission system resonant circuits in the presence of a distorted Voltage can cause resonances which can be damped if resistive synthesis is used. As suggested in ref [1.13] (chapter 4), harmonic currents should be drawn from the supply so that the corresponding Voltage drop across the supply impedance can offset the distortion at the point of common coupling which in turn will help to reduce the Total harmonic Voltage at this point.

Because of the advantages offered by the active parallel filtering method synthesising a resistive load, it is the technique chosen for the investigation in this thesis. It was considered the most appropriate method for removal of harmonics at the point of supply to a domestic installation.

2.4.3 Power Flow paths in a Shunt APF synthesising a resistive load

The shunt APF is the focus of the work in this thesis since it is suited to the goal of developing a single phase domestic APF. Therefore it is necessary appreciate the flow paths of current carrying real power and those carrying no useful power.

There are two conditions to consider:

- When the source Voltage is undistorted (i.e. a sinewave at the fundamental frequency)
- When the source Voltage is distorted

2.4.3.1 When the Source Voltage is not distorted

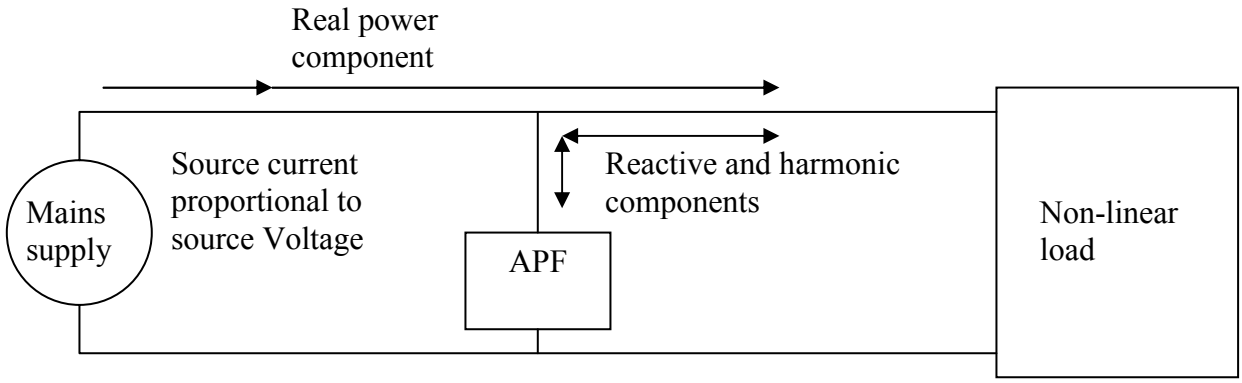


Fig 2.11: Power flow for a non-distorted source Voltage

The theoretical purpose of the APF is to supply the reactive and harmonic component of the load while the supply provides only the real power component. A practical APF will not remove the entire watt-less component form the source owing to bandwidth and switching limitations.

2.4.3.2 When the source Voltage is distorted

For the majority of cases the flow of currents is the same as Fig 2.11. However a situation may arise where the load may not absorb a power carrying source harmonic. Consider the example situation of fig 2.12:

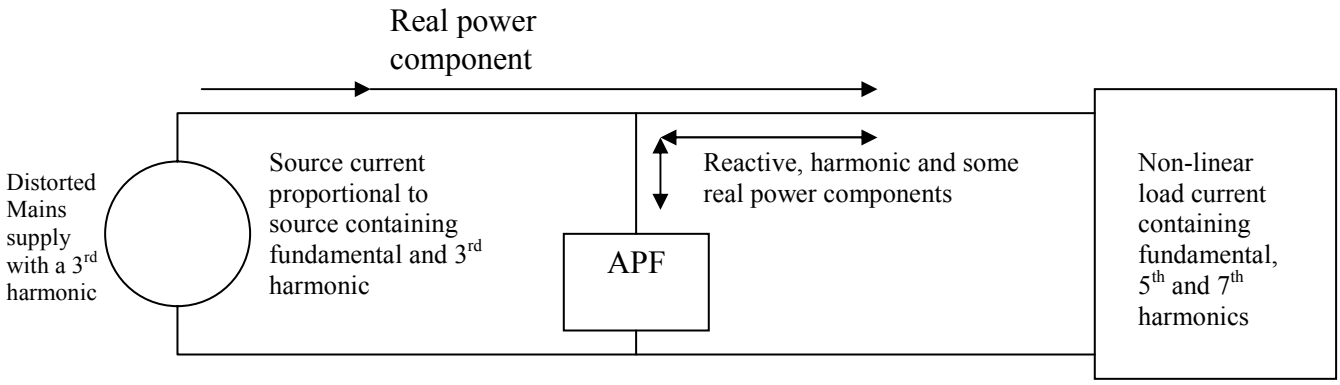


Fig 2.12: Power flow for a distorted source Voltage

Fig 2.12 shows a situation where the source current is forced to follow the source Voltage so that the overall system appears resistive. In the example shown, this causes the source current to contain a 3rd harmonic that carries real power since it will be in phase with the 3rd harmonic of the source Voltage. However the given load does not absorb power in the third harmonic. The example shown indicates that the load will only absorb power in the fundamental since the third harmonic is missing form the load current. Harmonic power in the 5th and 7th harmonics resonates between the load and the APF. The real power taken from the source in the 3rd harmonic is converted by the APF to a real power component in the fundamental, i.e. the APF acts as a power frequency changer.

A numerical example follows:

Let Mains supply be $V_s = 340\cos(\omega t) + 20\cos(3\omega t)$

Let Load current be $I_L = 10\cos(\omega t) + 2\sin(5\omega t) + 0.5\cos(7\omega t)$

Then Load power = $\frac{1}{2}(340 * 10) = 1700\ \text{W}$

For the input to appear as a pure conductance K:

Source current $I_s = K.V_s = K(340\cos(\omega t) + 20\cos(3\omega t))$

From a power calculation:

$1700 = \frac{K}{2}(340^2 + 20^2) = 58000K$ giving K = 0.02931

Therefore $I_s = 9.9655\cos(\omega t) + 0.5862\cos(3\omega t)$

APF current $I_f = I_s - I_L = -0.03448\cos(\omega t) + 0.5862\cos(3\omega t) - 2\sin(5\omega t) + 0.5\cos(7\omega 7)$

In the 3rd harmonics the APF imports $\frac{1}{2}(0.5862 \times 20) = 5.862\ \text{W}$

In the fundamental the APF exports $\frac{1}{2}(0.03448 \times 340) = 5.862\ \text{W}$

This example shows that 5.862 W has been converted from the 3rd harmonic to the 1st harmonic.

2.5 Control Strategies for Shunt Active Power Filters

For more than a decade much work has been carried out investigating suitable methods for dealing with the non-linear control problem. The circuit arrangement for the APF itself is normally an H-Bridge and this will form the central part of the

design. The capacitive (Voltage fed) “H-Bridge” is shown in fig 1.6 and is used extensively by many researchers. The H-Bridge may employ an inductor to store energy instead of the capacitor when the switch arrangements are as shown in fig 1.2. The majority of researchers use the capacitor-Voltage source technique which tends to indicates that this is the most practical solution.

It is important to make the distinction between the switching method and the control method.

The most common technique for driving the H-Bridge is Pulse Width Modulation (PWM). PWM is used to translate the control signal from whatever control strategy is used into binary outputs for the H-Bridge. In practice the switches will be either power IGBT’s or MOSFET’s. Gate drives will be provided via isolation (for example transformer or opto-isolator). The PWM interface together with the switching devices can be thought of as a power amplifier. The average Voltage at the output of the bridge will follow the input drive signal. The PWM interface converts the drive signal into a high fixed frequency carrier wave with a variable mark/space ratio. Other techniques used to drive the switching devices are Hysterisis and Sliding control where the emphasis is on H-bridge output current control rather that average Voltage. These alternative techniques derive the switching signals directly rather than relying on an interface such as the PWM carrier generator. The frequency at which the devices are switched using these alternative drive techniques can be either fixed or variable.

Popular control techniques using PWM employ mainly Proportional-Integral (PI) or Predictive (also known as deadbeat) strategies and these require the PWM method for translation to bridge-driving binary signals.

Other control strategies using PWM that are less common are “fuzzy logic”, “least compensation current”, “selective harmonic compensation” and adaptive (neural network) techniques (see References and Bibliography sections 5).

2.5.1 Variable Structured Control

Within the last ten years there has been interest in employing “Variable Structured Control” (VCS) (a particular class of which is known as “Sliding Mode”). This class of control provides a binary output directly as a result of the control method so the

need for PWM translation into a carrier wave is not necessary. Sliding Control effectively combines the control method, the error amplifier of the control loop, and the high gain switching amplifier as a single entity. The application of sliding mode to the solution of APF control has not been studied as extensively as other control methods, but appears to offer a viable alternative (in particular see ref [6.1]).
The switching regime of true (pure) sliding mode is a variable frequency method; however a new approach is taken in this thesis (Chapter 3) that transforms the concept of sliding mode into a fixed frequency discrete method. Texts on sliding mode control (e.g. ref [1.1], [1.2] chap 7) tend to overlook the detailed application issues and concentrate very much on the underlying theory, whereas papers relating to sliding mode in APF design ([5.3] [5.4] [5.6] [5.7]) tend to omit some of the issues of how the sliding surface is derived from the practical system. Chapter 3 of this thesis focuses on the theory and application of sliding mode to the control of the single phase shunt APF.

Chapter 3 The Application of Sliding Mode Control to the Shunt APF: Design Methods and Simulation

This chapter details the development of the Sliding Mode method as it applies to the shunt APF.

In common with existing single phase APF methods using sliding control (refs [5.2], [5.3], [5.4], [5.5], [5.6], [5.7]) a sliding function will be derived and used to control an H-bridge (fig 3.11). In an attempt to simplify the control system in a manner that could be run on inexpensive hardware, the control system developed in this chapter differs from existing work as follows:

- The bridge is driven directly from the error derived form the sliding function and not from a PWM system
- The sliding function will be of first order and the states derived directly from circuit parameters and not synthesised using additional integrating circuits
- The system will not employ low pass filters to smooth the capacitor reference
- The system will not employ a PI integrator in the control feedback path

Some initial Sliding Mode theory is presented. This is followed by a detailed analysis of Power flow to and from the H-bridge and how this relates to transistor switch settings.

The concept of Discrete Sliding Mode (DSM) is introduced as a means of implementing the Sliding Technique for H-Bridge Control.

The control state variables are selected and the details are presented relating to obtaining references for the chosen states based on energy calculations.

A set of rules are presented for developing an APF based on the foregoing theory which are then used to specify a MATLAB (Simulink) model for simulation and the details of the simulation model are dealt with.

A set of results are produced for 3 different non-linear loads to assess the effectiveness of the APF development using zero and first order DSM.

Finally a detailed comparison is made between the system developed and results presented in Chapter 3 with those of other researchers working in the same area.

3.1 *Sliding Mode Control*

The purpose of this section is to examine some of the relevant standard theory of pure sliding control methods as a preamble to presenting the concept of "Discrete Sliding Mode Control" which has been developed for controlling the shunt APF.

3.1.1 Introduction to Sliding Mode Control

Sliding Control was initially conceived by Utkin [1.12] and is a discontinuous control action with the primary function to switch between two different system structures such that a new type of motion exists. Sliding mode control in the continuous time domain is conceived as a method of imposing a specific response characteristic to a system whose open-loop behaviour can be modelled with ordinary differential equations. The restriction of the sliding method is that the resulting sliding motion is of reduced order. (see Ref [1.1] proposition 3.1). When constructing the sliding equation, the controlled states can be obtained by synthesis or obtained directly from existing physical system parameters. If the sliding space is to be constructed from physical states then it is necessary to be able to identify those states within the system that are related by linear differential equations.
In the following work some use is made throughout of references [1.2] and [1.12].
It is instructive to consider pure sliding mode in the following manner:

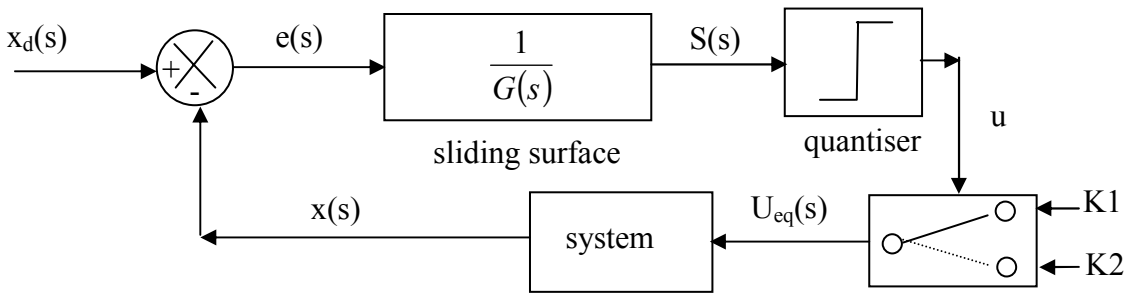


Fig 3.1*: A control loop representation of Sliding Mode*

Although the system is essentially non-linear by virtue of the nature of a quantising device, parts of the system are linear so that the use of the complex frequency domain

can still be of some use. The linear part of the system (G(s)) is shown as a separate block; it is separated out here to simplify the concept under discussion.

$x_d(s)$ is the input function: this is the function that ideally the system output x(s) should follow.

Let e(s) be the error function = $x_d(s) - x(s)$
(Note: texts on sliding mode normally choose error to be $x(s) - x_d(s)$, but it is more convenient not to use this convention - it makes no difference to the results).

The sliding transfer function has been represented by 1/G(s).
For illustration, the sliding space used in reference texts shall be adopted i.e. a first order low pass filter:

$$G(s) = \frac{\lambda}{s + \lambda}$$

or:

$$\frac{1}{G(s)} = \frac{s + \lambda}{\lambda}$$

The output from 1/G(s) is a variable S(s) where $S(t) = L^{-1} S(s)$ is the state-space to which convergence should take place i.e. the sliding space.

The use of S in this context could be somewhat confusing, therefore upper case will be used for the sliding function and a lower case s used as the Laplacian operator.

S(t) now enters a quantiser (fig. 3.1) (it is more convenient to consider time domain at this point). The effect of quantising in this context is to hard limit the output to a binary variable. It is conventional to use the sign function (sgn) here:

$u = -sgn(S(t))$

i.e. $u = 1$ if $S(t) < 0$
and $u = -1$ if $S(t) > 0$

If the binary input u is 1 then it should force the system into a state where S(t) > 0 and if u = -1 then it should force the system to a state where S(t) < 0.

The state of u selects one of two system inputs, i.e. it switches the system to act in one of two different ways. From a simplified point of view the system has been represented as having either input K1 or K2 depending on the switch position. In practice u may be controlling the position of one or many switches buried within the system itself. It must be emphasised that there are only two states and that the system will reside in one of these states depending on sgn(S(t)).

The state of u must always act to reduce the magnitude of S(t).

As a result of switching the system, it is essential that the error e(t) should be controlled so as to reduce the magnitude of S(t) and for this to happen knowledge of the system performance either mathematically or intuitively is essential. A completely unknown or erratic system could not be dealt with using sliding control.

Provided that the overall system behaviour is known, then it can be determined which switch condition is appropriate for reducing S(t). It may be necessary that a partial redesign of the system is necessary to ensure that two appropriate switching conditions exist.

Each time the sign of S(t) changes, pure sliding control assumes that there is an instantaneous switch action. This implies fast switching and consequently very high system bandwidth. If this is true then S(t) can be kept relatively small.

Pure Sliding Control relies on the sliding function S(t) being kept as small as possible. It is assumed that for very high system bandwidth S(t) = 0.

The sliding surface is defined by:

$$\frac{e(s)}{G(s)} = S(s)$$

Using the example given earlier for G(s):

$$e(s) = \frac{\lambda . S(s)}{\lambda + s}$$

It is necessary for S(t) to go to zero for t > 0, therefore for pure sliding mode:

$S(t) = \delta(t)$ (the Dirac function)

and $S(s) = 1$

to achieve this, the error function must be given by:

$$e(s) = \frac{\lambda}{\lambda + s}$$

and $e(t) = \lambda e^{-\lambda t}$

i.e. pure sliding mode forces the error function to follow the impulse response of G(s).

Therefore:

$$x_d(t) - x(t) = \lambda e^{-\lambda t}$$

Provided S(t) can be kept at zero (assuming a high enough system bandwidth) then x(t) will converge to the demand input $x_d(t)$ with a time constant of $1/\lambda$.

3.1.2 An alternative viewpoint for the sliding control loop

The effect of the quantiser is to magnify the value of s(t). For any small deviation of sign of s(t) the value of u changes sign, therefore the effect of the quantiser and switch in fig 3.1 can be replaced by a large gain (M) giving fig 3.2.

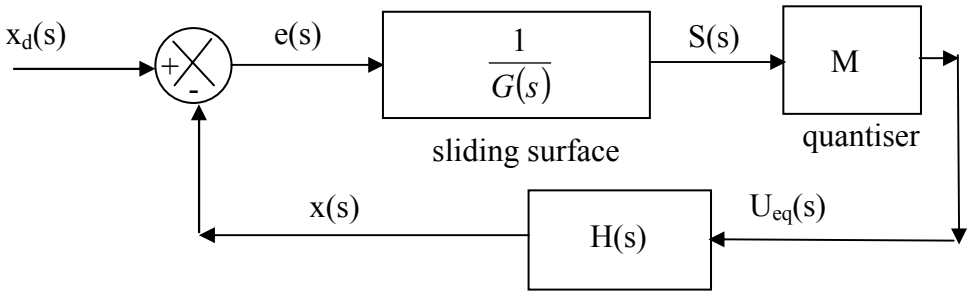


Fig 3.2*: Linearised equivalent control loop representation of Sliding Mode*

As before, $G(s) = \frac{s+\lambda}{\lambda}$

$U_{eq}(t)$ is the linear interpretation of the hard limited switched output u.

For this loop:

$$\frac{S(s)}{x_d(s)} = \frac{\frac{(s+\lambda)}{\lambda}}{1 + M.H(s).\frac{(s+\lambda)}{\lambda}} = \frac{(s+\lambda)}{\lambda + M.H(s)(s+\lambda)}$$

$$x(s) = H(s).M.S(s)$$

therefore:

$$\frac{x(s)}{x_d(s)} = \frac{M.H(s).(s+\lambda)}{\lambda + M.H(s)(s+\lambda)}$$

$$H(s).(s+\lambda)(x_d(s) - x(s)) = \frac{\lambda.x(s)}{M}$$

or

$$H(s).(s+\lambda).e(s) = \frac{\lambda.x(s)}{M}$$

For t > 0, provided abs($u_{eq}(t)$) > 0, then as M becomes very large it follows that

$S(t) = \delta(t)$

Therefore $S(s) = 1$

which gives: $x(s) = H(s).M$

Since in general H(s) ≠ 0

$\therefore (s+\lambda).e(s) = \lambda$

$\therefore e(s) = \frac{\lambda}{(s+\lambda)}$

hence the same result as before i.e. $e(t) = x_d(t) - x(t) = \lambda e^{-\lambda t}$

3.1.3 Interpreting Pure Sliding Mode on a State Space diagram

It is conventional to view a plot of the state space variables as they cross the sliding surface. The example already provided describes a first order equation which can be plotted in two dimensions of $e(t)$ and $\dot{e}(t)$

The first order sliding surface is:

$$\dot{e}(t) + \lambda e(t) = 0$$

Where the solution (as already stated) is $e(t) = \lambda e^{-\lambda t}$

This describes a straight line on a state diagram of $\dot{e}(t)$ against $e(t)$:

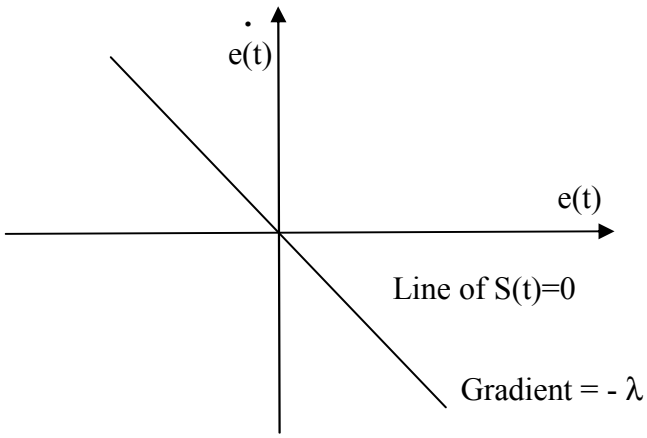


Fig 3.3*: First-order state space showing the line about which switching takes place during sliding*

Re-writing the line equation:

$$\dot{x}_d(t) - \dot{x}(t) + \lambda(x_d(t) - x(t)) = 0 = \dot{x}(t) - \dot{x}_d(t) + \lambda(x(t) - x_d(t))$$

Using $x(t)$ and $\dot{x}(t)$ as the state variables, a first-order sliding surface is as follows:

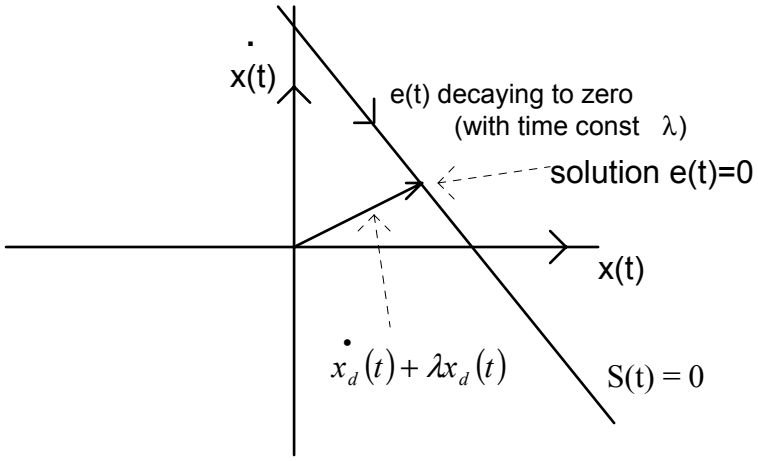


Fig 3.4*: Sliding line shown with respect to system variables*

Fig 3.4 shows the sliding surface displaced to a point $\dot{x}_d(t) + \lambda x_d(t)$

The effect of switching to maintain S(t) to zero forces the state variable x(t) to converge onto the sliding surface. Provided S(t) remains at zero then the error converges to zero with a time constant of 1/λ (i.e. the impulse response of the first order system). If the input x_d was a step function then the solution point e(t)=0 would reside on the axis of x(t) at the intersection with the line S(t)=0.

In terms of the application of this technique two error states are selected:

$\tilde{x}_1 = \tilde{x}$ (Note the use of error notation, where $e = x_d - x = \tilde{x}$)

$\tilde{x}_2 = \dot{\tilde{x}}$

The solution for each state is $\tilde{x}_1 = const.e^{-\lambda t}$ and $\tilde{x}_2 = -const.\lambda e^{-\lambda t}$

The fact that $\tilde{x}_2$ has been magnified by λ will be referenced in the next section.

As x approaches zero, the two states x_1 and x_2 converge to x_{1d} and x_{2d} respectively. It is evident that two error states are controlled with just one binary-switched input. The technique can be applied to higher orders. For example three state variables can be controlled by setting s(t) to a second order differential surface function.

For three state variables:

$\tilde{x}_1 = \tilde{x}$, $\tilde{x}_2 = \dot{\tilde{x}}$, $\tilde{x}_3 = \ddot{\tilde{x}}$

$$S(t) = \ddot{\tilde{x}} + \lambda_1 . \dot{\tilde{x}} + \lambda_2 \tilde{x}$$

The Eigen values must be distinct, real and negative.

The Eigen values determine the speed of convergence and must be chosen from knowledge of the system and the input reference that x must follow.

3.1.4 The effect of extreme λ values and a zero order surface

Suppose the 1st order derivative term from 1/G(s) is removed so that G(s) = 1, (i.e. effectively put $\lambda \to \infty$) then this gives $S(t) = \tilde{x}(t)$. The effect of switching is to force S(t) and hence $\tilde{x}(t)$ to zero i.e. the sliding surface is now the $\dot{\tilde{x}}$ axis and the solution is the single point where $\tilde{x} = 0$. In this case the maximum system bandwidth is used to force just one error state to zero.

A similar effect can be obtained if λ is reduced to a relatively small value. In this case the sliding surface is the $\tilde{x}$ axis and most of the available bandwidth is used to force $\dot{\tilde{x}}(t)$ to zero. The effect of "sharing the bandwidth" between two states is shown on the following state diagram:

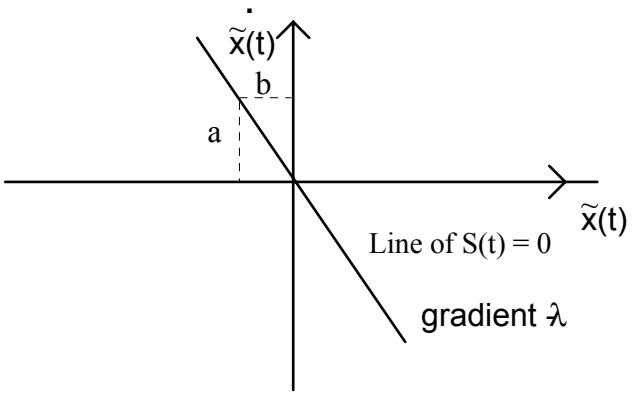


Fig 3.5*: Transient errors in system variables depend on λ*

If λ was zero then 'a' on the state diagram would be zero and the switching effect would solve the simple equation $\dot{\tilde{x}}(t) = 0$ and distance b would not be controllable.

As λ increases above zero then both 'a' and 'b' are controllable but a large error in 'a' also means a large error in 'b'. If λ is relatively large, then a small error in 'b' results in a large error in 'a'. From 3.1.3 $\tilde{x}_1 = const.e^{-\lambda t}$ and $\tilde{x}_2 = -\lambda.const.e^{-\lambda t} = -\lambda.\tilde{const}.x_1$ i.e. the error x_2 is the error in x_1 magnified by λ. A large λ will increase the convergence speed but at the expense of a large error in $\tilde{x}_2$ for a small error in $\tilde{x}_1$

When λ = 0 the system will only control one state error-variable i.e. $\begin{pmatrix} \dot{\tilde{x}} \end{pmatrix}$.

When λ > 0 the system will control both state error-variables.

3.1.5 Ensuring convergence to the switching surface

It is essential that switching S(t) to zero (i.e. about the sliding surface) will cause the system to converge onto the surface. To ensure convergence to a solution on the sliding surface $S^2(t)$ must be a Lyapunov function (see refs [1.1] [1.2]) and therefore:

$\frac{1}{2}\frac{d}{dt}S^2(t) = S(t).\dot{S}(t) \le -\eta$ where η is a positive constant -----{eqn 3.1}

This states that the square of the distance to the surface at any point (i.e. $S^2(t)$), decreases along all system trajectories. All trajectories in the state space are constrained to point towards the surface. Once on the surface they remain on the surface and slide along it. This requirement is therefore called the "sliding condition".

3.1.6 The Equivalent Dynamics while on the sliding surface

The switching input is a binary value; however the input can be viewed as an analogue value when in sliding mode. This "equivalent" input can be derived from the system equations by imposing Filippov's construction ([1.1] 1.2]):

$\dot{S}(t) = 0$

The equivalent input calculated by the construction must not exceed the limits of the switching binary input.

For example (details to be given later) if the binary input is β where $\beta \in \{0,1\}$ then the equivalent input must satisfy $0 \le \beta \le 1$ where the switching variable β is defined in section 3.4.

3.1.7 The effect of "Chattering" in the design of a Sliding Mode Controlled System

It has been shown that the effect of switching is to force S(t) to zero. To achieve this (theoretically) would require an infinite system bandwidth. Practically, the system may "chatter" about the switching surface. Chattering leads to high frequency switching activity which in turn leads to practical problems. Specifically the APF's switching transistors are limited in their ability to switch between low and high impedance at high frequencies and if driven above this frequency would over dissipate and fail. The concept of DSM (Discrete Sliding Mode) to be discussed later will overcome this problem. Conventional Sliding Mode designs usually incorporate a "boundary layer" about the switching surface. This boundary layer imposes a hysterisis about the sliding surface. The following figure illustrates the boundary layer for the example of the first order surface:

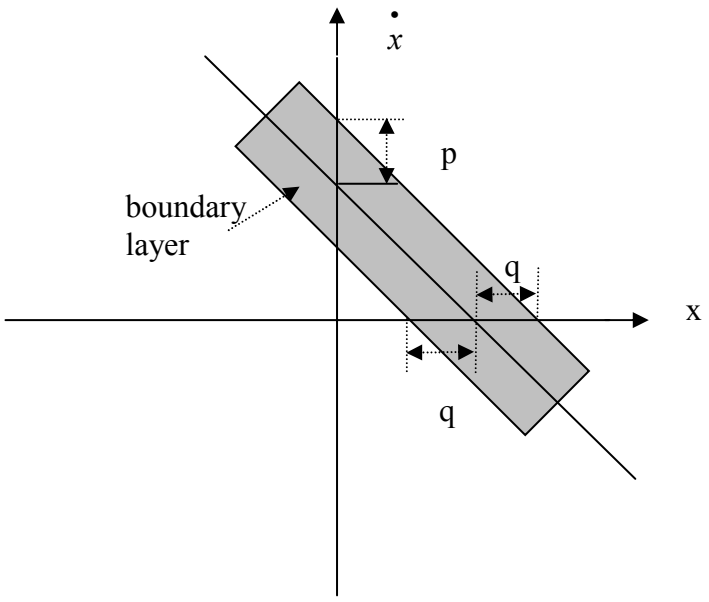


Fig 3.6*: Showing the sliding "chattering" boundary*

The boundary layer is defined by:

$|S(t)| \leq p$ for p > 0

From $S(t) = \dot{\tilde{x}} + \lambda \tilde{x}$ when $\tilde{x} = 0$ it follows that $\left|\dot{\tilde{x}}(t)\right| \leq p$

$\frac{p}{q} = \lambda$ where q is as shown on Fig 3.6

Tracking of the state variable x(t) is now guaranteed to lie within q. It can be seen from the diagram that the error in $\dot{\tilde{x}}(t)$ is now given by: $\left|\dot{\tilde{x}}(t)\right| \leq \lambda q$ and the range of $\dot{\tilde{x}}(t)$ is $\leq 2\lambda q$

3.2 Introducing the concept of Discrete Sliding Mode (DSM)

Pure sliding mode assumes that as the system state crosses the switching surface immediate action is taken to "push" the system back towards the surface. This requires continuous monitoring of the system variables and very large bandwidth. The imperfections of the system lead to chattering, and the method of reducing chattering is to impose a hysterisis boundary as already described in section 3.1.7. Such a system can be thought of as a combination of sliding mode and hysterisis control. Discrete sliding mode adopts a concept of regular sampling of all relevant system variables with period T. The measurement and control signal application are performed only at regular intervals of time, and the control signal is held constant in between these instants. Discrete Sliding Mode is a fairly new concept (ref [1.4]) and has only appeared during the last ten years. There are specific requirements in this thesis for DSM and as such the algorithm and supporting theory are presented.

Immediately following the sample instant, the value of S(t) is calculated and the switches of the APF set appropriately. The system moves to a new state and may (or may not) cross the switching surface when after a further sample duration T the next set of sampled data is collected. The choice of T is dependent on the system and therefore a good knowledge of the system is required. In the case of the APF the bridge switching transistor components and design specification determine T. In

particular T is chosen in conjunction with the inductor value and the speed at which the transistors can switch. $\frac{dI_f}{dt}$ (where I_f is the input filter current) is an important factor that is related directly to T. These and other considerations have been taken into account during the design for simulation (sections 3.11.2, 3.11.3).

Immediately following a sample instant, S(t) is evaluated and if it happens that the surface has yet to be crossed then no change is made to the switches. It is important therefore to track the switch status and feed this information forward to the next sample interval. A switch state memory is therefore needed (which is built into the simulation model to be dealt with in section 3.12.5).

If the surface has been crossed, then the switches must be updated to allow the system to move back towards the surface.
During the period when the system crosses the surface, overshoot will occur (as it does when a boundary layer is imposed); however in the case of the boundary layer it is possible to guarantee the limit of overshoot. Overshoot in discrete sliding mode is dependent on the system state and the value T and will vary between each sample interval; however it must be possible to estimate the worst-case overshoot.
During the time the system has crossed the sliding surface and before the occurrence of the next sample instant, the system will be moving away from the surface, consequently the condition for convergence of S(t) to zero previously quoted as

$$\frac{1}{2}\frac{d}{dt}S^2(t) = S(t).\dot{S}(t) \leq -\eta$$

is only applicable at the instant S(t) has been updated.

3.2.1 Examining the spectrum of a System controlled using DSM

The DSM concept has some similarities to signal sampling and it is instructive to analyse DSM from this point of view. The following theory develops the DSM concept (as defined by the application in this thesis) in terms of its sampled spectrum. Conventional sampling of signals and the Nyquist limit are well understood and documented in many texts on communication theory (for example see ref. [1.5]).

DSM is dynamic and system dependent and therefore a worst case condition will be imposed for illustrative analysis.

Let the system switch between two states, one with a step response of $h_1(t)$ and the other with a step response of $h_2(t)$. As an example, a DSM system may have the following characteristics:

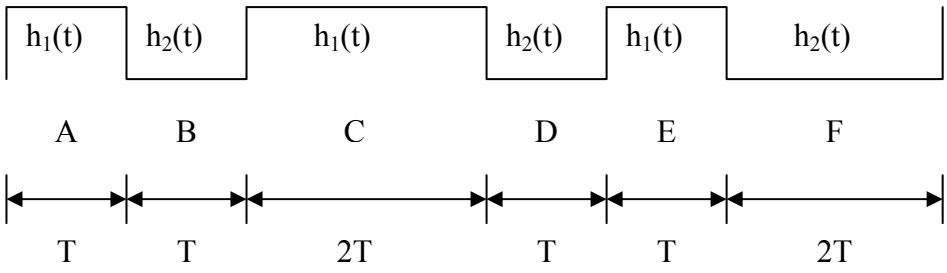


Fig 3.7*: A typical DSM switching sequence for two system responses $h_1(t)$ and $h_2(t)$*

In this example, periods A, B, D and E correspond to the controlled state crossing the sliding surface, however during periods C and F the system has not crossed the surface and so remains in the current state for an additional clock sample.

For the purpose of analysis a simplified and worst case DSM system will be considered where the *system changes state every clock period*.

To build this system there must be two logical clocks as follows:

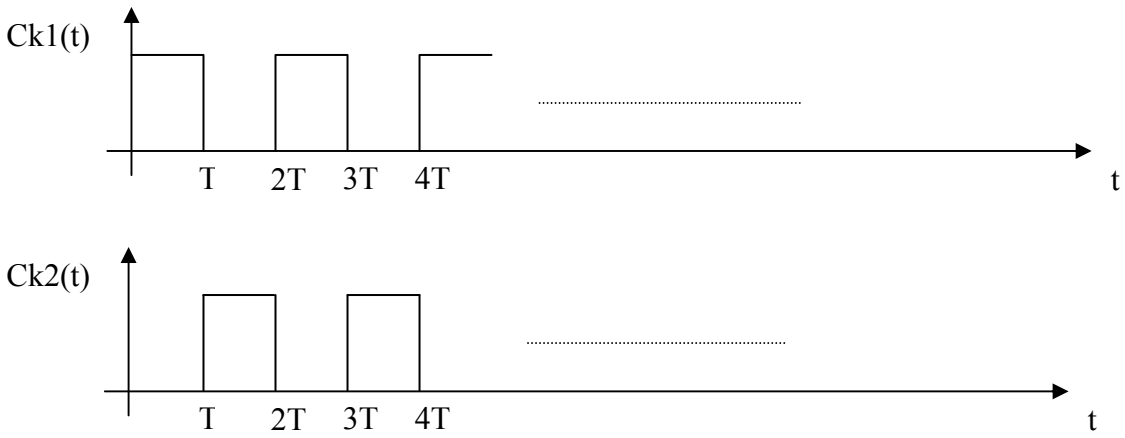


Fig 3.8*: A pair of anti-phase clocks on which to build a simplified DSM system*

As a harmonic series:

$$Ck1(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{\infty}\frac{1}{(2n+1)}\sin(2n+1)\omega_0 t \qquad \text{where } \omega_0 = 2\pi/2T = \pi/T$$

and

$$Ck2(t) = \frac{1}{2} - \frac{2}{\pi}\sum_{n=0}^{\infty}\frac{1}{(2n+1)}\sin(2n+1)\omega_0 t$$

Let the combined function be f(t) = Ck1(t).h_1(t) + Ck2(t).h_2(t)

$$= \frac{(h_1(t)+h_2(t))}{2} + \frac{2}{\pi}(h_1(t)-h_2(t))\left[\sum_{n=0}^{\infty}\frac{1}{(2n+1)}\sin(2n+1)\omega_0 t\right]$$

$$= \frac{(h_1(t)+h_2(t))}{2} + \frac{2}{\pi}(h_1(t)-h_2(t))\left[\sum_{n=0}^{\infty}\frac{e^{j(2n+1)\omega_0 t} - e^{-j(2n+1)\omega_0 t}}{2(2n+1)}\right]$$

Taking the Fourier Transform of this function (recognising that the function is periodic and therefore setting the integration limits to one period of the combined function):

$$F(\omega) = \int_0^{2T}\frac{h_1(t)+h_2(t)}{2}e^{-j\omega t}dt + \int_0^{2T}\left[\frac{1}{\pi}(h_1(t)-h_2(t))\sum_{n=0}^{\infty}\frac{e^{-j(\omega-(2n+1)\omega_0)t} - e^{-j(\omega+(2n+1)\omega_0)t}}{2n+1}\right]dt$$

Using the frequency-shift theorem and letting $G(\omega) = H_1(\omega) + H_2(\omega)$:

$$F(\omega) = \frac{G(\omega)}{2} + \frac{1}{\pi}\sum_{n=0}^{\infty}\left[\frac{1}{(2n+1)}(G(\omega-(2n+1)\omega_0) - G(\omega+(2n+1)\omega_0))\right]$$

It is necessary to define a bandwidth limit for $H_1(\omega)$ and $H_2(\omega)$. Bandwidth in this context is defined at the point where "slope overload" just occurs. The bandwidth limit is the frequency of a sine wave which has the same maximum rate of change as that possible by the system function response when driven by a step function (which must be interpreted in the context of the system in hand).

Assuming that a bandwidth can be defined for both $H_1(\omega)$ and $H_2(\omega)$ then $F(\omega)$ can be viewed as:

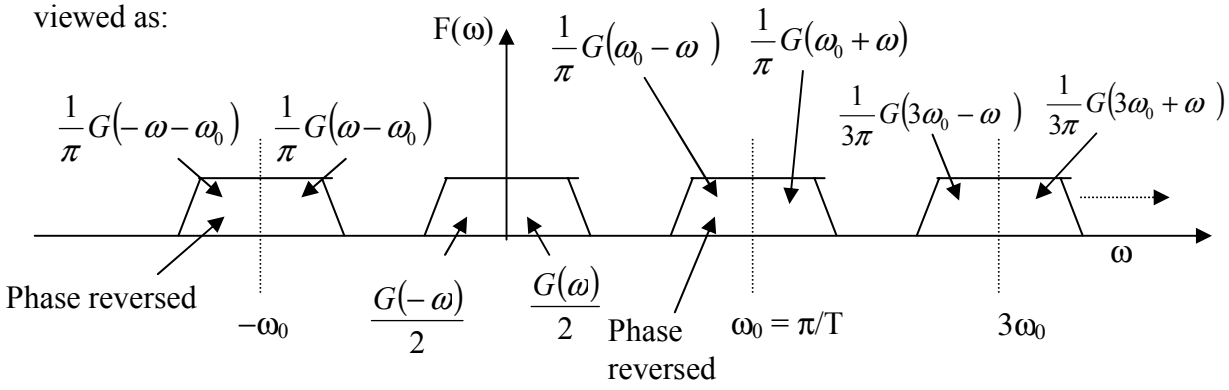


Fig 3.9: *A discontinuously occupied DSM spectrum*

Unless the spectrum is continuously occupied then there is no guarantee that the switching surface s(t) will be crossed and the DSM concept of repeating the last function will be necessary.

If the DSM spectrum is discontinuous then there is no guarantee that the switching surface will be crossed in period T. The controller will detect this situation and must maintain the same switching condition until the next switching interval. This effectively halves the sampling DSM frequency (i.e. halves ω_0) to cater for the lower system bandwidth and ensures a continuous DSM spectrum. The effect of dynamically repeating the previous switching state if the switching surface has not been crossed to ensure spectral continuity is formalised as the DSM algorithm in fig 3.14.

For a continually occupied spectrum:

Bandwidth $G(\omega) > 1/2T$

Or

2 * Bandwidth $G(\omega)$ > sampling frequency

(Note that the term "sampling" is used interchangeably with the term "switching" and that the sampling frequency = 1/T).

Note that $G(\omega) = H_1(\omega) + H_2(\omega)$ and therefore the **sum** of the bandwidths of $H_1(\omega)$ and $H_2(\omega)$ must be greater than 1/2T.

To maintain symmetry about S(t) the bandwidths of $H_1(\omega)$ and $H_2(\omega)$ must be approximately the same. If they are not then drift will occur about S(t) and the DSM algorithm containing the repeated function principle will correct the drift.

For efficient operation the bandwidths of $H_1(\omega)$ and $H_2(\omega)$ should be as high as possible, however, this will result in excessive overshoot.
Overshoot is undesirable in an APF and to avoid this, the 3/2 H-bridge concept has been developed in this thesis. Using this technique the effective bandwidth of $H_1(\omega)$ and $H_2(\omega)$ are dynamically switched as required by the load by using the reachability conditions (see sections 3.7.2 and 3.12.4.1 (ref "fast_inductor")).

3.3 A detailed discussion of the H Bridge and the Switching "Modes"

Section 3.3 and subsequent sub-sections formalises the various switching states by establishing the concept of "Active" and "Passive" modes of the H-bridge by examining the rate of power flow and builds this into a DSM framework.

The H-Bridge is the main switching system and in its basic form is shown in fig 3.10.

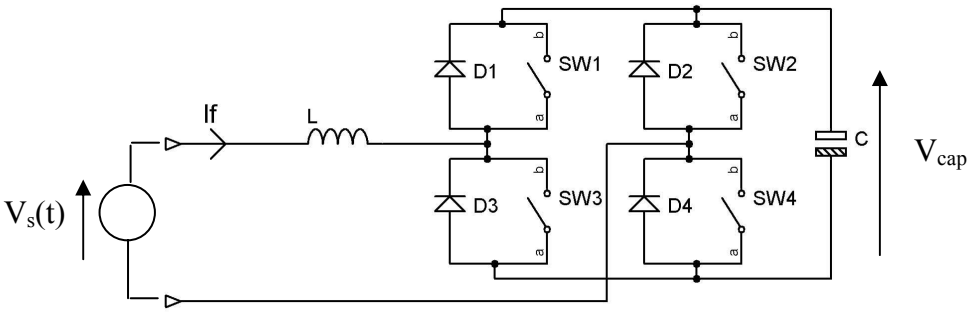


Fig 3.10: *Ideal Single Phase H-Bridge*

The H-bridge is a familiar diode bridge with the addition of switches that can cause timed pulses of current to flow out-of and into the capacitor. The switches are assumed to be ideal for the purpose of theoretical analysis and each is in parallel with a diode. The practical implementation of the H-Bridge will use IGBTs as shown in Fig 3.11.

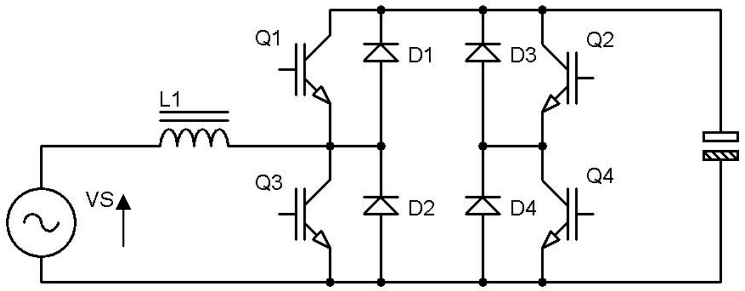


Fig 3.11: Practical Single phase H-Bridge using IGBTs

The diodes will conduct during both the "active" and "passive" modes (to be defined later). In some respects the system is similar to that of the boost converter where the series inductor controls the rate of current flow. The capacitor Voltage will rise to some defined level above the mains peak and is used as an energy store.
The control system will force the input current to be proportional to the mains (forcing the mains to supply only real power). The reference current that the input current must follow will be referred to as I_{sref}.
If the absolute value of the real power load current is less than the absolute value of I_{sref}, the filter must absorb the additional energy. The corresponding energy is stored in the capacitor. If the real power load current is greater than the absolute value of I_{sref}, then the capacitor must source energy to the load.
There are two parameters that must be controlled; the source current (forced to be proportional to the mains Voltage) and the average value of the capacitor Voltage that must be kept to a value sufficiently high to enable the filter to work within its designated specifications.

3.3.1 Power, Energy and Current flow

Note the designated direction of I_f (the H-Bridge Filter Current) in fig 3.10.

It is essential throughout the analysis of the bridge to be able to refer to either energy or power or some other parameter that is moving towards or away from the bridge. There are two important parameters to consider which are Power and the rate of change of Power. Power depends on V_s and I_f and the rate of change of Power depends on V_s and $\frac{dI_f}{dt}$.

The supply will be taken as the reference with Voltage $V_s(t) = V \sin \omega t$.

Noting the designated direction of I_f, the power taken by the filter is:

$$P(t) = V_s(t) I_f(t)$$

therefore:

$$\partial P(t) = V_s(t) \cdot \partial I_f(t) + I_f(t) \cdot \partial V_s(t)$$

However, since the sample time T is normally much smaller than the period of the source (τ) then it will be assumed that for the period T, $V_s(t)$ is constant giving:

$\left.\frac{dP(t_1)}{dt}\right|_T = V_s(t_1)\frac{dI_f(t_1)}{dt}$ where $\left.\frac{dP(t)}{dt}\right|_T$ is restricted to a single period T

and $t_1 \in [t, t+T]$

It follows that $\text{sgn}\left(\frac{dP(t)}{dt}\right) = \text{sgn}(V_s).\text{sgn}\left(\frac{dI_f(t)}{dt}\right)$ -----{eqn 3.2}

When entering into the physical design and numerical analysis of the filter (see section 3.11.5 step 7), it will be seen that a typical value for $\frac{dI_f(t)}{dt}$ is between 10^4 As^{-1} and 10^5 As^{-1}.

Therefore it will be assumed the following statements are correct:

If V_s is positive and $\frac{dI_f(t)}{dt}$ is positive then power (source to filter) is *increasing* and *absorbed* by the filter.

If V_s is negative and $\frac{dI_f(t)}{dt}$ is negative then power (source to filter) is *increasing* and *absorbed* by the filter.

If V_s is positive and $\frac{dI_f(t)}{dt}$ is negative then power (filter to source) is *increasing* and *delivered* by the filter.

If V_s is negative and $\frac{dI_f(t)}{dt}$ is positive then power (filter to source) is *increasing* and *delivered* by the filter.

The bridge alternates between consuming power and delivering power in a way that evens out the load on the mains source in order to force the mains supply current to follow the mains supply Voltage thereby making the load look resistive.
Energy is stored in the magnetic field of the inductor and as the bridge switches operate the energy is either delivered to the source or sent back to the storage capacitor. The capacitor Voltage grows to a level above the peak of the mains Voltage. The simulated design used in this thesis will be specified to charge the capacitor to around 550 Volts when it will be capable of forcing current back into the mains source as required.

Control of the switches must ensure that there is never an instance when two switches are on causing a short across the bridge. Also, the phasing of the switches must take the mains Voltage into account so that the capacitor polarity is correct as seen from the bridge terminals.

3.3.2 Active and passive modes of the H-Bridge and Current flow paths

In general the transistor switches forming the bridge circuit of Fig 3.11 can be driven in three ways.

- Method 1: Bi-Polar which uses a purely "Active" approach in that two transistors are enabled at any time (whether or not both are actually conducting)
- Method 2: Uni-polar which, as with method 1 is "Active" and enables two transistors at any time whether or not both are actually conducting)
- Method 3: which interleaves "active" and "passive" modes where transistors are only switched on when conduction is required

See ref [5.8] for Unipolar and Bipolar operation.

The Bi-Polar method requires that Q1 and Q4 are enabled followed by Q2, Q3. Transistors in each leg (Q1, Q3 and Q2, Q4) are triggered in complement. This method is *not* suitable for correct APF operation.

The Unipolar method requires that Q4 remains on and Q2 remains off when V_s (direction as shown in figs 3.10 and 3.11) is positive and Q4 remains off and Q2 remains on when V_s is negative. Q1 and Q2 are switched so as to reduce the error in I_f and are always the complement of each other.

Note that switching depends on the condition of the sliding variable S(t). It will be shown that the chosen sliding surface depends on the error in the filter current and the error in the capacitor Voltage at the m^{th} sample interval where the sampling period is T. The filter current error is the difference between the filter reference current and the actual filter current at the m^{th} sample interval:

$$I_{ferror}(mT) = I_{fref}(mT) - I_f(mT) \qquad \text{-----\{eqn 3.3\}}$$

The capacitor Voltage error is the difference between the measured capacitor Voltage and the capacitor reference Voltage at the m^{th} sample interval:

$$V_{caperror}(mT) = V_{capref}((mT) - V_{cap}(mT) \quad \text{-----\{eqn 3.4\}}$$

Then the sliding variable at the m^{th} sample interval is given as:

$$S(mT) = \frac{1}{C} I_{ferror}(mT) + \alpha\lambda V_{caperror}(mT) \quad \text{-----\{eqn 3.5\}}$$

(see section 3.6.5 for further details).

3.3.2.1 H-Bridge switching method 2: Unipolar

Refer to fig 3.11 for transistor references

The Unipolar "Active" method of driving the bridge is defined in the following table:

Mode reference	Category	Error condition to enter mode	Polarity of V_s	Sign of I_{fref}	Sign of $dI_f(t)/dt$	Transistors enabled	Conducting devices
1	Active	S(mT) < 0	+	-	-	Q1, Q4	Q1, Q4
2	Active	S(mT) > 0	+	-	+	Q3, Q4	D3, Q4
3	Active	S(mT) > 0	+	+	+	Q3, Q4	Q3, D4
4	Active	S(mT) < 0	+	+	-	Q1, Q4	D1, D4
5	Active	S(mT) > 0	-	+	+	Q3, Q2	Q3, Q2
6	Active	S(mT) < 0	-	+	-	Q1, Q2	D1, Q2
7	Active	S(mT) < 0	-	-	-	Q1, Q2	Q1, D2
8	Active	S(mT) > 0	-	-	+	Q3, Q2	D3, D2

Table 3.1: *Eight modes of the H-Bridge using Unipolar Active switching*

The following set of Figures show the current paths for each Mode given in table 3.1. IGBTs that are On or Off are indicated with a logic 1 or 0 on their gates respectively.

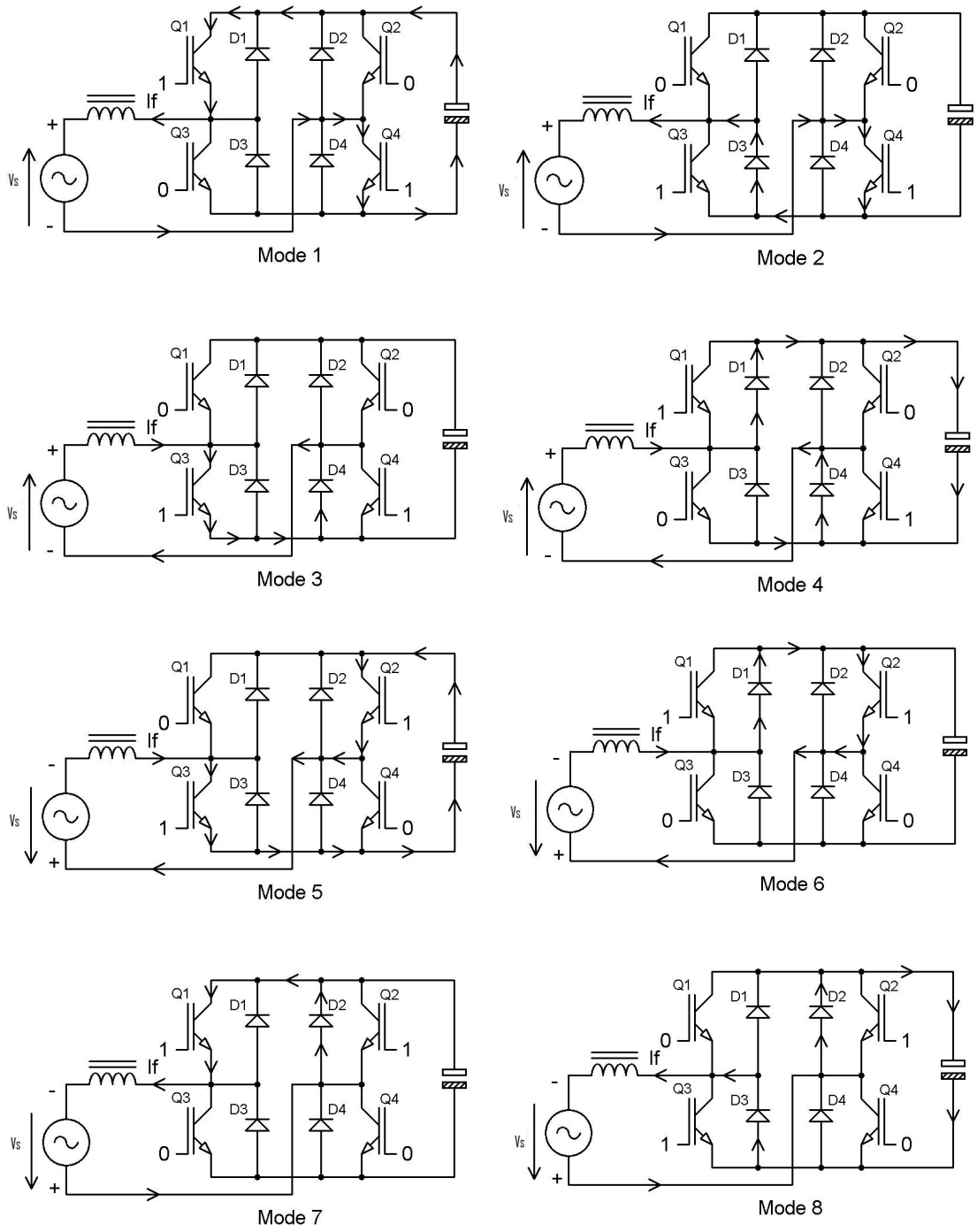


Fig 3.12: *Current paths for eight Unipolar "Active" H-Bridge modes where enabled transistors have "1" on their gates and disabled transistors have "0" on their gates*

Table 3.1 illustrates that filter current error determines which mode of a mode-pair is in operation. The particular switching pair is determined by the signs of V_s and I_{fref}. The pairs are Modes 1 & 2, 3 & 4, 5 & 6, 7 & 8.

The system will oscillate about a mode pair until the V_s and I_f sign conditions change.

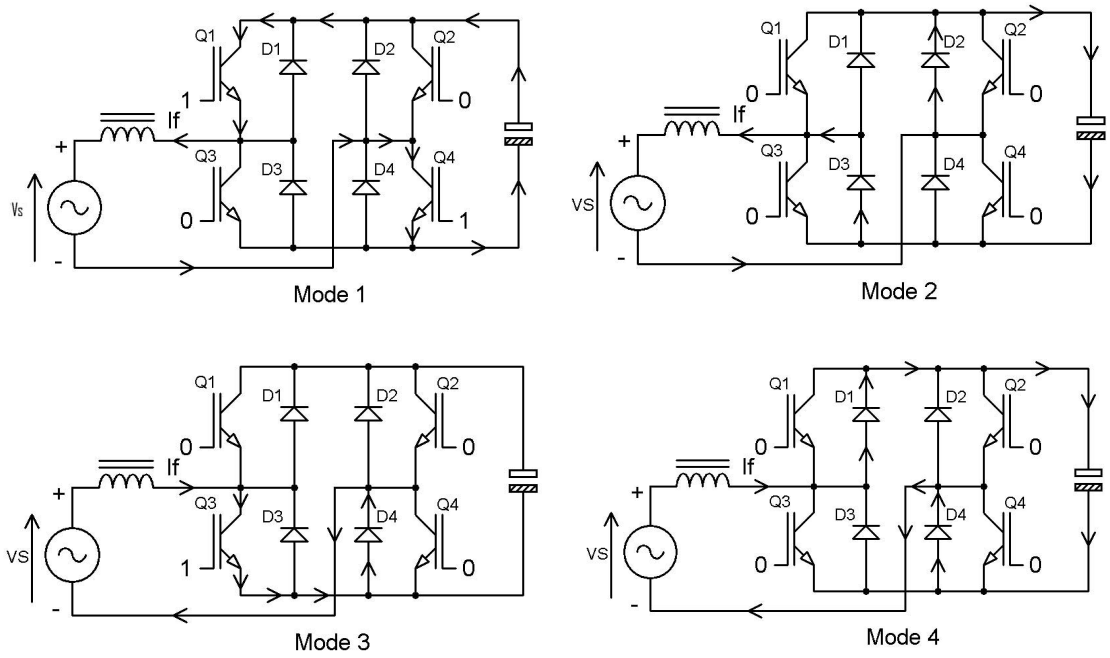
3.3.2.2 H-Bridge switching method 3: "Active" and "Passive"

The "Active" and "Passive" switching method is given in the following table:

Mode reference	Category	Error condition to enter mode	Polarity of V_s	Sign of I_{fref}	Sign of $dI_f(t)/dt$	Transistors enabled	Conducting devices
1	Active	S(mT) < 0	+	-	-	Q1, Q4	Q1, Q4
2	Passive	S(mT) > 0	+	-	+	none	D2, D3
3	Active	S(mT) > 0	+	+	+	Q3	Q3, D4
4	Passive	S(mT) < 0	+	+	-	none	D1, D4
5	Active	S(mT) > 0	-	+	+	Q3, Q2	Q3, Q2
6	Passive	S(mT) < 0	-	+	-	None	D1, D4
7	Active	S(mT) < 0	-	-	-	Q1	Q1, D2
8	Passive	S(mT) > 0	-	-	+	none	D3, D2

Table 3.2: *Eight modes of the H-Bridge using Active and Passive switching*

The following Figure set shows the current path for each Mode given in table 3.2. IGBTs that are On or Off are indicated with a logic 1 or 0 on their gates respectively.



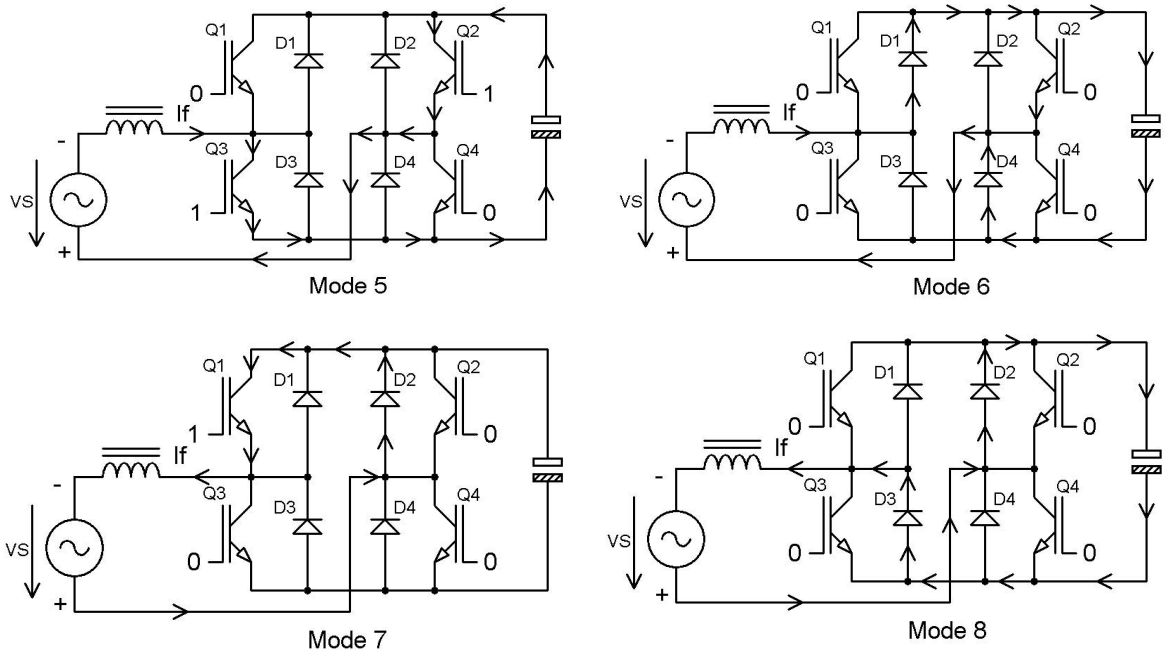


Fig 3.13: *Current paths for four "Active" H-Bridge modes (1, 3, 5, 7) and four "Passive" modes (2, 4, 6, 8) where enabled transistors have "1" on their gates and disabled transistors have "0" on their gates*

Table 3.2 illustrates that filter current error determines which mode of a mode-pair is in operation. The particular switching pair is determined by the signs of V_s and I_{fref}. The system resides in an Active/Passive mode pair where the pairs are Modes 1 & 2, 3 & 4, 5 & 6, 7 & 8 and will continue to oscillate about a mode pair until the V_s and I_f sign conditions changes.

3.3.2.3 Unipolar and Active/Passive modes

Comparison of the two modes "Unipolar" and "Active"/"Passive" reveals that the two modes 2 and 6 are different.

Unipolar:

In modes 2 and 6 the inductive current circulates around the bridge.

Active/Passive:

In modes 2 and 6 the current is diverted back to the capacitor.

The Active/Passive scheme therefore gives better control of the current since dI_f/dt is not so dependent on source Voltage in these modes.

The Unipolar scheme requires an interlock delay between switching Q1 to Q3 and Q2 to Q4 to prevent "shoot through". The Active/Passive scheme does not require the interlock delay since there is a sample interval following the turn off of any transistors when the system resides in a Passive mode.

There are no advantages of the Unipolar scheme over the Active/Passive scheme. Owing to the reduced complexity brought about by eliminating the interlock delay and the improved control in modes 2 and 6 it was decided to base the remainder of the work in this thesis on the Active/Passive scheme. However there is no loss in generality to the results obtained by choosing this method. Furthermore, the practical work presented in Chapter 5 will be based on the Active/Passive approach.

3.3.3 The application of DSM to the Switching Mode considerations of the H-bridge

An Active switching mode drives the system towards S(t)=0. When the switching line is crossed, the switches are returned to the Passive mode (i.e. all off).

By using the established convention of considering changes in power (section 3.3.1), if power is moving from the source to the APF it will be referred to as power absorption and if power is moving from the APF to the source it will be referred to as power delivery. The Active mode will result in power delivery and the Passive mode will result in Power absorption.

The following flow diagram (fig 3.14) describes how the H-bridge switches should be controlled. The flow chart is executed once every sample period T.

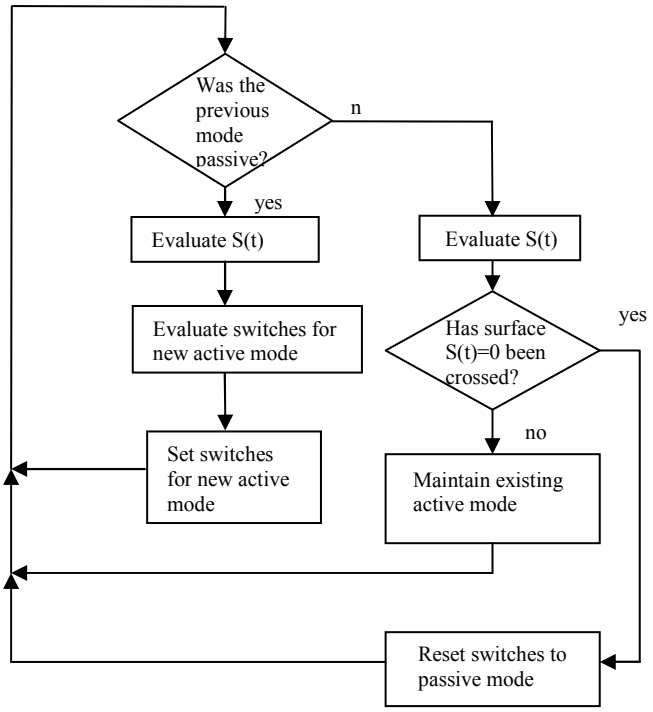


Fig 3.14*: A block diagram of the DSM algorithm*

(Reference is made throughout to the basic H-bridge of fig 3.11 and Appendix A).

Table 3.3 describes the switching phases of the H-Bridge and refers to the *Power Change (with time)* that is absorbed or delivered.

	Power Delivered to source from APF		Power Absorbed from source into APF	
Vs	Increasing (Active phase)	Decreasing (Passive phase)	Increasing (Active phase)	Decreasing (Passive phase)
+	Mode 1 Q1, Q4 on I_f -ve dI_f/dt –ve Q1, Q4 conducts	Mode 2 no transistors on I_f -ve dI_f/dt +ve D2, D3 conducts	Mode 3 Q3, on I_f +ve dI_f/dt +ve Q3, D4 conducts	Mode 4 no transistors on I_f +ve dI_f/dt -ve D1, D4 conducts
-	Mode 5 Q3, Q2 on I_f +ve dI_f/dt +ve Q3, Q2 conducts	Mode 6 no transistors on I_f +ve dI_f/dt -ve D1, D4 conducts	Mode 7 Q1, on I_f -ve dI_f/dt -ve Q1, D2 conducts	Mode 8 no switches I_f -ve dI_f/dt +ve D2, D3 conducts

Table 3.3: *showing rate of power transfer Modes of the H-Bridge*

Table 3.2 allows Modes to be defined as switching pairs where the operational pair is determined by the signs of V_s and I_f. Table 3.3 allows each mode within a pair to be defined in terms dI_f/dt which in turn allows the specific mode to be categorised as the rate of Power delivered or absorbed.

For example, if V_s is +ve and $\frac{dI_f}{dt}$ is -ve the system is in an increasing power delivery mode (1) or a decreasing power absorbed mode (4). The direction of power transfer depends on I_f and V_s but the rate of power transfer depends only on $\frac{dI_f}{dt}$. For example, in mode 4 V_s is +ve, I_f is +ve and dI_f/dt is –ve so power is being transferred from the source to the filter capacitor but the rate of change of power in the direction form source to filter is reducing towards zero.

Note that all power increasing modes whether delivered or absorbed are active and that all decreasing power modes whether delivered or absorbed are passive.

Also, note that power delivered-increasing is distinct from power absorbed-decreasing and similarly power delivered-decreasing is distinct from power absorbed-increasing even though in both cases $\frac{dI_f(t)}{dt}$ is the same sign.

3.3.4 State Space interpretation of the active switching phases of the H-Bridge

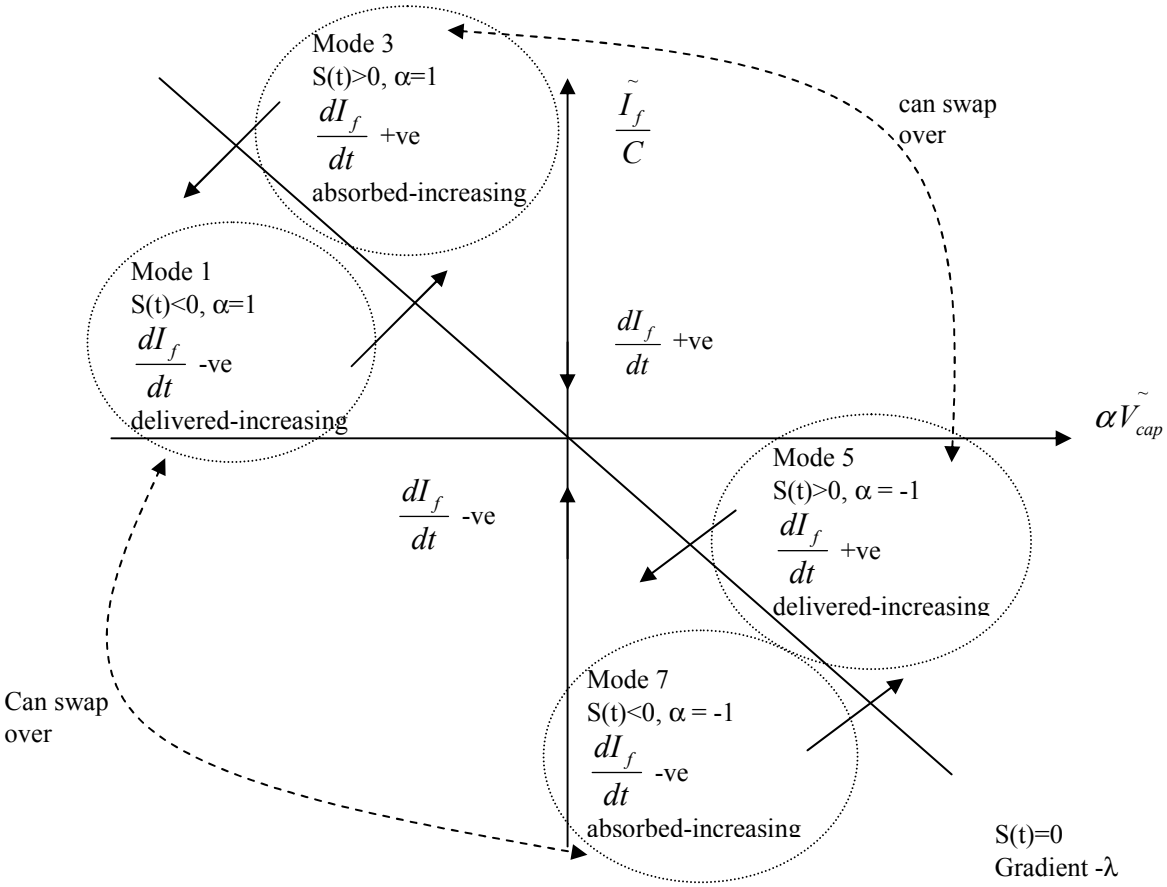


Fig 3.15*: Diagrammatic representation of the active modes of Tables 3.2 and 3.3*

Fig 3.15 represents the active switching phases in diagrammatic form as the system attempts to force S(t) to zero and solve the 1st order differential equations for V_{cap} and I_f. The passive modes are not shown, but exist between the active modes as described in Tables 3.2 and 3.3. For example, an active absorbed-increasing mode will attempt to reverse the sign of S(t). If after time T this has been successful then a passive mode follows. If the passive mode successfully reverses the sign of S(t) then another active absorbed mode will start, but if the passive mode leaves the sign of S(t) unchanged then an active delivered-increasing mode must start. The diagram therefore shows the active modes as an absorbed-delivered pair. The dotted arrows indicate that the pairs

can swap places depending on the sign of the error states at the sample time. Note that active modes 1 and 3 are the complement of each other and active modes 5 and 7 are complements of each other. If modes 3 and 5 swap position on the state diagram then so must modes 1 and 7.

The choice of state variables i.e.:

$$x(t) = \alpha V_{cap} \quad \text{and} \quad \dot{x}(t) = \frac{I_f(t)}{C}$$

is consistent with the system equations given in section 3.4 and will be presented in section 3.6.2.

3.4 System Equation and the choice of Switching Variables

Section 3.4 and subsequent sub-sections investigates suitable switching variables and system equations and how these are used to define the H-Bridge modes.

In addition to the input switching variable u defined in section 3.1.1 as

u = 1 if S(t) < 0 (Active mode)

and u = -1 if S(t) > 0 (Active mode)

the following are also needed:

u = 0 for a Passive mode (all H-Bridge switches off)

$\alpha = \text{sgn}(V_s)$

i.e.

$\alpha = 1$ if V_s +ve

$\alpha = -1$ if V_s -ve

and

$\beta = 0$ when $u.\alpha = 1$ (Active absorbed mode)

$\beta = 1$ when $u.\alpha = -1$ (Active delivered mode)

β is undefined during a passive mode

3.4.1 System Equations

The system link equation can be written as follows:

$$\frac{dI_f(t)}{dt} = \frac{\alpha}{L}\left[abs(V_S(t)) - \beta.V_{cap}(t)\right] \qquad \text{-----\{eqn 3.6\}}$$

Note: during the active delivered modes, proper switch operation in accordance with table 3.3 ensures that the magnitude of the Voltage across the inductor is abs(V_s(t))– V_{cap}.

Since $\alpha.abs(V_s(t)) = V_s(t)$ then:

$$\frac{dI_f(t)}{dt} = \frac{V_s(t)}{L} - \alpha.\beta.\frac{V_{cap}(t)}{L} \qquad \text{------\{eqn 3.7\}}$$

Also due to proper switch operation in the active modes:

$$\frac{dV_{cap}(t)}{dt} = \alpha.\beta.\frac{I_f(t)}{C} \qquad \text{------\{eqn 3.8\}}$$

L is the APF input inductor and V_{cap} is the Voltage across the APF storage capacitor.

Note: only the active effects that the filter is having on the source are considered, i.e. how power is actively delivered or absorbed. The passive modes are internal to the APF when the absorbed energy is transferred from the magnetic field of the inductor to the electric field of the storage capacitor.

During the active modes, when power increases towards the source, (delivered-increasing active modes, $\beta = 1$) {eqn 3.8} indicates that the *sign* of the change in capacitor Voltage depends on α.sgn(I_f). During the active phase when power increases towards the APF (absorbed-increasing active phase $\beta = 0$) {eqn 3.8} indicates that the capacitor Voltage remains unchanged.

Placing {eqn 3.8} into tabular form:

		Active Increasing Power Delivered to source from APF ($\beta = 1$)	Active Absorbed Power Absorbed from source to APF ($\beta = 0$)
Vs	α		
+	1	$\frac{dV_{cap}(t)}{dt} = \frac{I_f}{C}$	$\frac{dV_{cap}(t)}{dt} = 0$
-	-1	$\frac{dV_{cap}(t)}{dt} = -\frac{I_f}{C}$	$\frac{dV_{cap}(t)}{dt} = 0$

Table 3.4: *Active Phase system equations*

Written in state space form the two APF defining equations (3.7 and 3.8) can be written as:

$$\begin{bmatrix} \dot{I}_f \\ \dot{V}_{cap} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{\alpha.\beta}{L} \\ \frac{\alpha.\beta}{C} & 0 \end{bmatrix} \begin{bmatrix} I_f \\ V_{cap} \end{bmatrix} + \begin{bmatrix} \frac{abs(V_s)}{L} \\ 0 \end{bmatrix}$$

The output state is $\begin{bmatrix} I_f \\ V_{cap} \end{bmatrix}$.

3.5 Solving the System Equations in the Active Phases

This section is concerned with the solution of equations 3.7 and 3.8 (which refer to the active phases) for an undistorted sinusoidal source.

3.5.1 When β=0

This is the less interesting case since eqn {3.8} gives no information other than the capacitor Voltage remains unchanged.

When β = 0 (Power actively absorbed increasing) from eqn {3.7}:

$$\frac{dI_f(t)}{dt} = \frac{V_s(t)}{L} \qquad \text{-----\{eqn 3.9\}}$$

Assuming that there is no Voltage distortion of the mains then $V_s(t) = V.\sin(\omega t)$

(where V is the peak of the mains cycle)

$$\therefore I_f(t) = \frac{V}{L.\omega}[1 - \cos(\omega t)] + I_f(0)$$

3.5.2 When β = 1

When β = 1 (Power delivered increasing) from {eqn 3.7}

$$\frac{dI_f(t)}{dt} = \frac{V_s(t)}{L} - \alpha.\frac{V_{cap}(t)}{L} \qquad \text{-----\{eqn 3.10\}}$$

and from {eqn 3.8}

$$\frac{dV_{cap}(t)}{dt} = \frac{I_f(t)}{C}.\alpha$$

$$\therefore \frac{d^2 I_f(t)}{dt^2} = \frac{\dot{V}_s(t)}{L} - \alpha^2.\frac{I_f(t)}{C.L}$$

$$\alpha^2 = 1$$

$$\therefore \frac{d^2 I_f(t)}{dt^2} + \frac{I_f(t)}{C.L} = \frac{\dot{V}_s(t)}{L} = \frac{\omega.V}{L}\cos(\omega.t)$$

The transient part of the solution is:

$$I_{ft}(t) = Q.\cos\left(\frac{t}{\sqrt{C.L}} + \theta\right) \qquad \text{-----\{eqn 3.11\}}$$

(for time independent values Q and θ)

The steady state part of the solution is:

$$I_{fss}(t) = \left(\frac{\omega.V.C}{1 - \omega^2 L.C}\right)\cos(\omega.t) \qquad \text{-----\{eqn 3.12\}}$$

The full solution is:

$$I_f(t) = Q.\cos\left(\frac{t}{\sqrt{C.L}} + \theta\right) + \left(\frac{\omega.V.C}{1 - \omega^2 L.C}\right)\cos(\omega.t) \qquad \text{------\{eqn 3.13\}}$$

Hence:

$$\dot{I}_f(t) = -\frac{Q}{\sqrt{C.L}}\sin\left(\frac{t}{\sqrt{C.L}} + \theta\right) - \frac{\omega^2 V.C.\sin(\omega.t)}{1 - \omega^2 L.C} \qquad \text{-----\{eqn 3.14\}}$$

Solution example over first half period of mains cycle assuming $I_f(0) = 0$:

$$\dot{I}_f(0) = -\frac{Q}{\sqrt{C.L}}\sin(\theta) \qquad \text{-----\{eqn 3.15\}}$$

given $I_f(0) = 0$ into eqn {3.13}:

$$\therefore Q.\cos(\theta) = -\frac{\omega.V.C}{1-\omega^2.L.C} \qquad \text{-----\{eqn 3.16\}}$$

At the instant t just > 0 (or in the general case when t is just greater than a half period of the mains supply) eqn {3.10} gives:

$$\dot{I}_f(0) = \frac{V_s(0)}{L} - \alpha\frac{V_{cap}(0)}{L} = -\alpha\frac{V_{cap}(0)}{L} \qquad \text{-----\{eqn 3.17\}}$$

eqns {3.15, 3.17} give:

$$\therefore -\frac{Q}{\sqrt{C.L}}\sin(\theta) = -\alpha\frac{V_{cap}(0)}{L}$$

$$\therefore Q.\sin(\theta) = \alpha\sqrt{\frac{C}{L}}.V_{cap}(0) \qquad \text{-----\{eqn 3.18\}}$$

eqns {3.16, 3.18} give:

$$Q^2 = \frac{\omega^2 V^2 C^2}{\left(1-\omega^2 L.C\right)^2} + \frac{C}{L}V_{cap}^2(0) \qquad \text{-----\{eqn 3.19\}}$$

and

$$\tan(\theta) = \alpha\sqrt{\frac{C}{L}}.V_{cap}(0).\left(\frac{1-\omega^2 L.C}{-\omega.V.C}\right) = \frac{\alpha V_{cap}(0)\left(\omega^2 L.C-1\right)}{\omega.V.\sqrt{L.C}} \qquad \text{-----\{eqn 3.20\}}$$

Using eqns {3.13, 3.19, 3.20} the full solution for $I_f(t)$ given $I_f(0) = 0$ is:

$$I_f(t) = \left(\frac{\omega.V.C}{1-\omega^2 L.C}\right)\cos(\omega.t) + \left[\sqrt{\frac{\omega^2 V^2 C^2}{\left(1-\omega^2 L.C\right)^2} + \frac{C}{L}V_{cap}^2(0)}\right]\cos\left(\frac{t}{\sqrt{C.L}} + \tan^{-1}\left(\frac{\alpha V_{cap}(0)\left(\omega^2 L.C-1\right)}{\omega.V.\sqrt{L.C}}\right)\right)$$

-----{eqn 3.21}

3.5.3 Plotting the equations for $I_f(t)$ and $dI_f(t)/dt$

The equations developed in section 3.5.2 were for the condition when $\beta = 1$ (i.e. power actively delivered). This section investigates the nature of the results with $I_f(0) = 0$ and $V_{cap}(0) = V_c$ (given parameter). The equations are only valid for a half mains cycle (for a fixed α). At the start of a new cycle, the initial conditions for constants Q and θ must be re-evaluated. Depending on initial conditions, part of the solution may not be applicable to active delivered power. It is only that part of the solution for which the rate of change of power is negative is used for active delivered power.
In order to plot equations {3.13, 3.14} over several cycles it is necessary to re-evaluate the initial conditions at the start of each cycle. Two new variables c1 and c2 are introduced.

In terms of Q and θ: $$c1 = Q\cos\left(\frac{t}{\sqrt{CL}} + \theta\right)\Bigg|_{t=t_0} \quad \text{----\{eqn 3.22\}}$$

where t_0 is the time at the instant α changes sign and Q and θ are the values taken at time t_0

Re-arrange eqn {3.13}:

$$c1 = I_f(t) - \left(\frac{\omega VC}{1-\omega^2 LC}\right)\cos(\omega t)\Bigg|_{t=t_0} \quad \text{----\{eqn 3.23\}}$$

In terms of Q and θ: $$c2 = Q\sin\left(\frac{t}{\sqrt{CL}} + \theta\right)\Bigg|_{t=t_0} \quad \text{----\{eqn 3.24\}}$$

Re-arrange eqn {3.14} and use eqn {3.17} and noting that $\sin(\omega t_0) = 0$ at time t_0:

$$c2 = \alpha V_{cap}(t)\sqrt{\frac{C}{L}}\Bigg|_{t=t_0} \quad \text{----\{eqn 3.25\}}$$

where *t_0 is the time at the instant α changes sign and Q and θ are the values taken at time t_0*

At each value of t_0 (i.e. where α changes sign) Q and θ are evaluated from:

$$Q = \sqrt{c1^2 + c2^2} \quad \text{----\{eqn 3.26\}}$$

$$\theta = tan^{-1}\left(\frac{c2}{c1}\right) - \frac{t}{\sqrt{CL}}\Bigg|_{t=t_0} \quad \text{----\{eqn 3.27\}}$$

The following m-file was used to produce a plot of $I_f(t)$ and $dI_f(t)/dt$:

```
% This function evaluates the response of the system as given in section
% 3.5.2
% Equations 3.13 and 3.14 are evaluated from t=0 to t=100m. Alpha is updated
% after each 10ms section of the plot.

%use filter_current3(Vpeak,C,L,Vcap(0))

function filter_current3(V,C,L,Vc)
w=2*pi*50;
t=0:20e-6:100e-3;
If(1)=0;        %initial condition
Vcap(1)=Vc;     %initial condition
alpha=1;        %default value
alphaold=0;
%dIf is the derivative of If wrt t
dIf(1)=-Vc/L;    %initial condition
m=2;
for n=2:5001
   alpha=sign(sin(w*t(n)));
   if (alphaold ~= alpha) & (alpha ~= 0)

      alphaold=alpha;
      m=n;

      %c1 = value of Qcos(t/sqrt(CL)+theta) at previous zero crossing
      c1(m)=If(m-1)-(w*V*C/(1-w*w*L*C))*cos(w*t(m-1)); %If must be a smooth function

      %c2 = new value of Qsin((t/sqrt(CL))+theta)

      %dIf can have discontinuities

      c2(m)=alpha*Vcap(m-1)*(C/L)^0.5;

      %find new value of Q
      Q(m)=(c1(m)^2 + c2(m)^2)^0.5;

      %find new value of theta
      theta(m)=atan(c2(m)/c1(m))-t(m-1)/(C*L)^0.5;
      if (c1(m) < 0) & (c2(m) > 0)
         %2nd quadrant not fourth
         theta(m) = theta(m) + pi;
      end
      if (c1(m) < 0) & (c2(m) < 0)
         %3rd quadrant not 1st
         theta(m) = theta(m) + pi;
      end
   end

   %find current value of If
   If(n)=Q(m)*cos(t(n)/(C*L)^0.5 + theta(m)) + w*V*C*cos(w*t(n))/(1-w*w*L*C);

   %find current value of dIf
   dIf(n)=(-Q(m)*sin(t(n)/(C*L)^0.5 + theta(m))/(C*L)^0.5-w*w*V*C*sin(w*t(n))/(1-w*w*L*C));
   Vcap(n)=(V*sin(w*t(n))-L*dIf(n))*alpha;
end
subplot(3,1,1)
plot(t,If)
```

```
title ('Filter Current');
ylabel ('Amps');
grid on;
subplot(3,1,2)
plot(t,dIf)
title ('Rate of change of filter current');
ylabel ('Amps/s');
grid on;
subplot(3,1,3)
plot(t,Vcap)
title('Capacitor Voltage');
ylabel('Volts');
xlabel ('secs');
grid on;
```

The above plot uses a step time of 20μs (which will also be the step time used in later simulations). The array starts at index 1 which corresponds to t=0.

When alpha changes sign the new values of Q and θ are updated. A new value of the constant c1 is evaluated where c1 is given by eqn{3.22}

$$c1(m) = Q.\cos\left(\frac{t(m-1)}{\sqrt{C.L}} + \theta\right)$$

A new value of c2 is evaluated where c2 is given by eqn {3.24}

$$c2(m) = Q.\sin\left(\frac{t(m-1)}{\sqrt{C.L}} + \theta\right)$$

Q and θ are obtained from c1(m) and c2(m) and remain fixed until α changes sign.

The program is run with the following parameters:

C=1000μF, L=21mH, Vpeak = 340V, Vcap(0)=550V (=Vc).

(These values are obtained from the system simulations that will be provided in later sections).

Running the m file
filter_current3(340,1000e-6,21e-3,550)

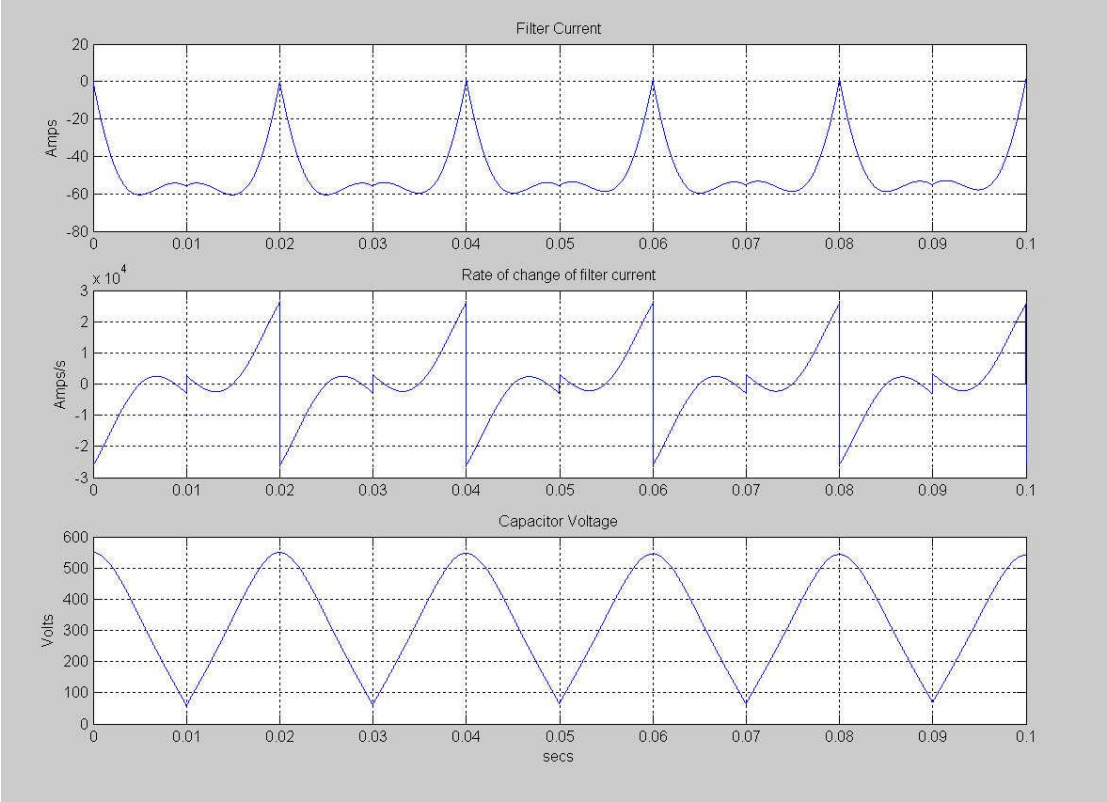


Fig 3.16*: A plot of I_f, dI_f/dt and V_{cap} for C=1000μF, L = 21mH Vpeak=340 and Vcap(0)=550 for the bridge of Appendix A with all switches open*

Note the following:

The capacitor Voltage always remains positive. There are no step changes in If(t). Step changes in dIf(t) occur at the α switching points.

If the Inductor value is reduced to 16mH, keeping all other parameters the same, then the capacitor Voltage just reaches zero:

Running the m file
filter_current3(340,1000e-6,16e-3,550)

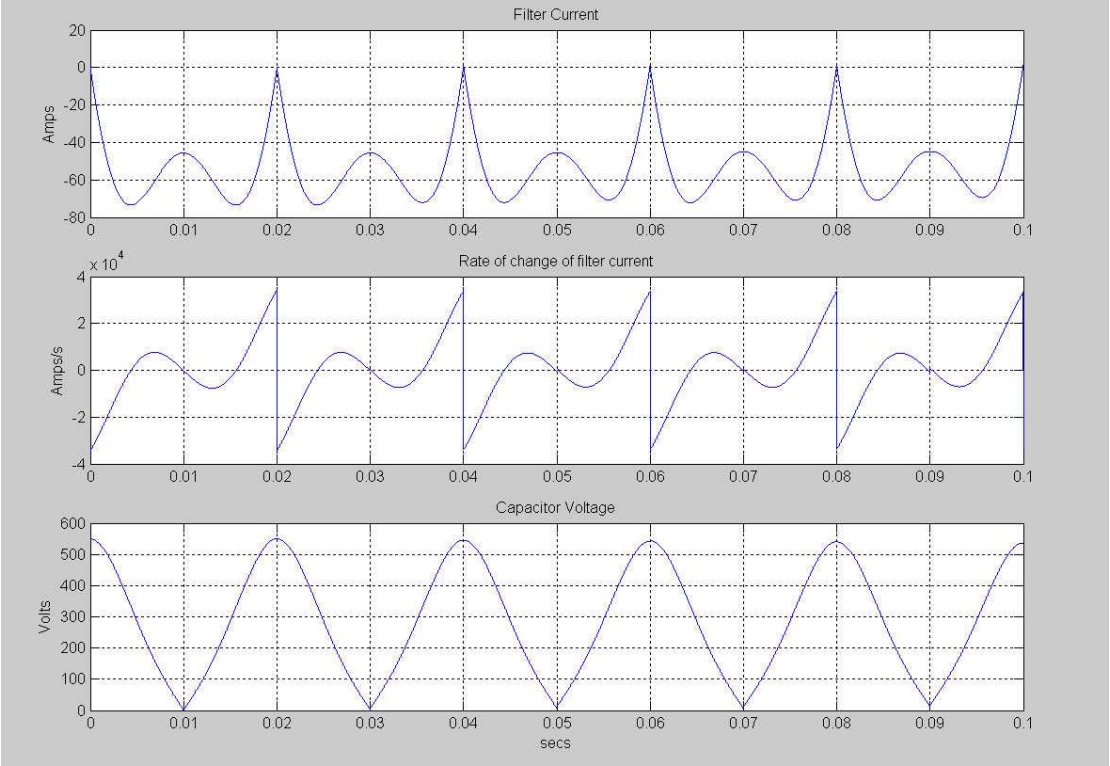


Fig 3.17*: as Fig 3.13 except L = 16mH which just forces V_{cap} to zero*

Note that Capacitor Voltage is always *just* positive.

For lower inductor values the capacitor discharges completely and evaluation of the new initial conditions becomes a numerical problem leading to unreliable results.

The region of *active delivered power* requires an additional plot of dP(t)/dt which is given for the case when L=21mH. The valid region is where dP/dt is –ve (i.e. active delivered power transferring from APF to load). Under normal switching conditions, the capacitor Voltage will never fall below mains Vpeak so the situation seen here where $\beta = 1$ and dP/dt goes +ve (shaded areas of plot) will never occur.

Diagram showing shaded areas which are invalid operating areas for a normal APF:

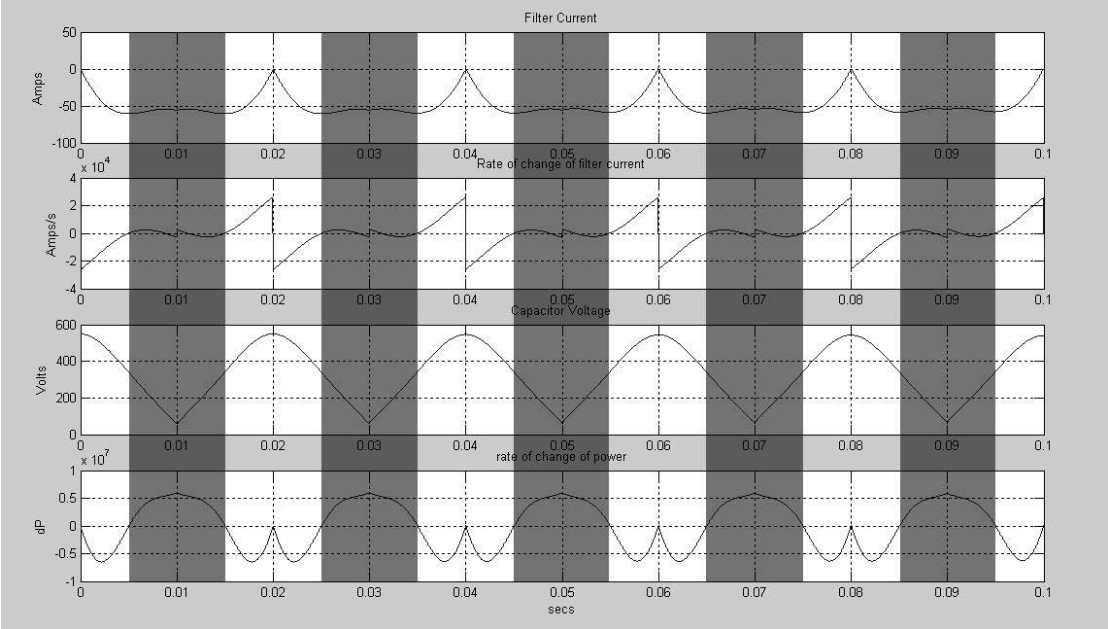


Fig 3.18*: As fig 3.13 with the rate of change of power (dP/dt) entering the H bridge also shown. The non-shaded area where dP/dt is negative and Vcap exceeds Vpeak is the valid operating region for an APF*

Non-shaded areas where $\frac{dP}{dt}$ is –ve are those where power is actively transferred from the APF to the supply. Within the shaded areas, the capacitor Voltage is less than or equal to the peak of the supply therefore no energy can be transferred from APF to supply.

3.6 Assigning State variables for DSM and deriving the associated references

This section and subsequent sub-sections investigates suitable sliding space state variables and the method of obtaining the references for these variables.

3.6.1 Maximum order of the Sliding Space

Reference [1.1] (ref text section 3.4) shows that the order of the sliding space is of reduced order

= number of states of the system – number of inputs.

The system equations given in section 3.5.2 indicate clearly that when $\beta = 1$ the system is second order, therefore with a single input control (u) the sliding space order is a maximum of 1. However, when $\beta = 0$ (section 3.5.1) the system is of single order, so the maximum order of the sliding space is zero.

Therefore the 1st order sliding space is only valid under the condition of active power delivered-increasing when $\beta = 1$. When $\beta = 0$, the system reverts to a zero order space.

3.6.2 Assigning the physical state variables to define the DSM sliding surface

Two state variables are needed to form a sliding space of order 1: x and $\dot{x}$ as explained in section 3.1.3. Eqn {3.8} clearly shows that if β = 1 then

$x = \alpha V_{cap}$ and $\dot{x} = \frac{I_f}{C}$.

Since it is necessary to control both I_f and V_{cap} then these variables will form the 1st order sliding surface. Note that this sliding implementation differs from some other methods by using physical measured variables rather than using variables synthesised with additional integrators.

When β = 0, eqn {3.8} gives $\frac{dV_{cap}(t)}{dt} = 0$, therefore $x = \alpha.V_{cap}$ **is uncontrollable**.

When β = 0, eqn {3.7} gives $\frac{dI_f(t)}{dt} = \frac{V_s(t)}{L}$ which is non-zero (for t ≠0, π, 2π, 3π,…),

therefore $\dot{x} = \frac{I_f}{C}$ **is controllable**.

3.6.3 Deriving the Reference for I_f

The primary control of the APF is to force the supply current to f*ollow the supply Voltage*. A secondary requirement is to maintain the capacitor Voltage at a value higher than the peak of mains and at some pre-determined value. Small fluctuations in V_{cap} can be tolerated. This section considers in some detail the reference current for input to the controller.

The APF is connected in parallel with the non-linear load (i.e. the load that is causing mains current distortion).

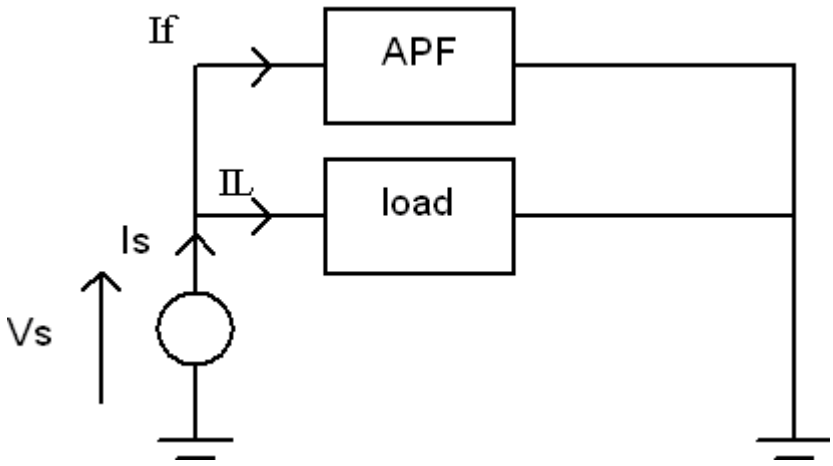


Fig 3.19*: Showing relationship between I_s, I_L and I_f*

Ideally it is required that the source current follows a reference $I_{sref} = K.Vs$

K can be thought of as the *ideal conductance* presented to the source (units mho).

From fig 3.19:

$$I_s - I_f = I_L \qquad \text{------\{eqn 3.28\}}$$

From the requirement for the source current to be proportional to the source Voltage (see section 2.4.2.3):

$$I_{sref} = K.V_s \qquad \text{------\{eqn 3.29\}}$$

I_{sref} represents the current component of the load (I_L) that carries the real power.

The error in supply current = $I_{sref} - I_s$

Let I_{fref} be the current that must flow in the APF in order to correct I_s

and the error in APF current = $I_{fref} - I_f$

i.e. referring to fig 3.19

$$I_{fref} + I_L = I_{sref} \qquad \text{-------\{eqn 3.30\}}$$

$$\therefore I_{fref} = I_{sref} - I_L$$

Eliminate I_L between eqn {3.28} and eqn {3.30}:

$$\tilde{I}_f = I_{fref} - I_f = I_{sref} - I_s$$

Therefore the error in filter current = error in supply current

Provided K is known (ideal input conductance) then I_{sref} can be derived from eqn {3.29} and hence I_{fref} obtained from eqn {3.30} provided I_L is measured.

The problem is to obtain K, which is load dependent.

3.6.4 Obtaining the ideal input conductance

Provided the reference current remains proportional to the source Voltage (as given in eqn {3.29}) then I_{sref} will represent the real load power.
In the case of a purely sinusoidal source Voltage (Fig 2.11) the reactive and harmonic components of the load will oscillate between the load and the APF when the load is steady (i.e. periodic) and the sum of the energy transfer from APF to load over one mains period will be zero.
In the case of the distorted source Voltage (Fig 2.12) the reactive and harmonic components will again oscillate between APF and load and the sum of the energy transfer over one mains period will be zero. The component of real power handling current that flows into the APF at one frequency and from the APF to the load at another frequency, also represents APF energy that sums to zero over one mains period.
The correct input conductance is therefore that value of K for which the sum of energy transfer to and from the APF is zero over one cycle. By using the capacitor as a sensor, the Voltage change on the capacitor over one mains period must be zero.
It follows therefore that once a steady working value of I_{sref} is reached the Voltage $V_{cap}(t) = V_{cap}(t + 0.02)$ (for 50Hz mains).
i.e. the capacitor Voltage should read the same value after τ = 20ms (one mains cycle) has passed.

The technique used to obtain K is by *iteration*. K is given an initial start value which is adjusted every period of the supply (symbol τ which is taken as 20ms) based on the change in capacitor Voltage (measured every τ). Once the capacitor Voltage remains the same after one period, further changes in K are no longer necessary.

The difference in capacitor Voltage after period τ is given by:

$$V_d = V_{capnew} - V_{capold}$$ -----{eqn 3.31}

If V_d is –ve then abs(I_{sref}) is too low therefore increase K

If V_d is +ve then abs(I_{sref}) is too high therefore reduce K

The change in capacitor energy after one period is

$$\frac{1}{2}C\left(V_{capnew}^2 - V_{capold}^2\right) = \frac{1}{2}C\left(V_{capnew} - V_{capold}\right)\left(V_{capnew} + V_{capold}\right) = \frac{1}{2}CV_d\left(V_{capnew} + V_{capold}\right)$$

Therefore the change in capacitor energy is:

$$\Delta E = \frac{1}{2}CV_d\left(V_{capnew} + V_{capold}\right)$$ -----{eqn 3.32}

from eqn {3.30}:

$$I_{fref} = I_{sref} - I_L$$

Assuming that the load is steady (i.e. periodic) then it can be assumed that the RMS value of I_L is constant giving:

$$\Delta I_{fref} = \Delta I_{sref}$$ -----{eqn 3.33}

(i.e. the change in I_{fref} = the change in I_{sref})

The energy supplied to the APF over one period is

$\tau.V_{sRMS}.I_{frefRMS}$ where V_{sRMS} and $I_{frefRMS}$ are RMS quantities.

The *change* in energy supplied to the APF over one period is:

$\tau.V_{sRMS}\Delta I_{frefRMS}$ and using eqn {3.33} this is also $\tau.V_{sRMS}\Delta I_{srefRMS}$

Since the sum of the energy changes must be zero then:

$$\tau.V_{sRMS}\Delta I_{srefRMS} + \Delta E = 0$$ -----{eqn 3.34}

giving $\Delta I_{srefRMS} = -\frac{\Delta E}{\tau.V_{sRMS}}$

Using two measures of I_{sref} separated in time by a supply period τ (and using RMS quantities):

$\Delta I_{srefRMS} = I_{srefnewRMS} - I_{srefoldRMS}$ and from eqn {3.29}:

$I_{srefoldRMS} = V_{sRMS}.K_{old}$ $\qquad$ $I_{srefnewRMS} = V_{sRMS}.K_{new}$

therefore:

$\Delta I_{srefRMS} = V_{sRMS}(K_{new} - K_{old})$ where K_{new} and K_{old} are the corresponding ideal conductances.

This gives:

$$V_{sRMS}(K_{new} - K_{old}) = \frac{-\Delta E}{\tau.V_{sRMS}}$$

giving:

$$K_{new} = K_{old} - \frac{\Delta E}{\tau.V_{sRMS}^2} \qquad \text{-----\{eqn 3.35\}}$$

Note that V_{sRMS} is the RMS value, and for the 240 Volt mains $V_s^2 = 240^2$

With τ = 20ms eqn 3.31 gives:

$$K_{new} = K_{old} - \frac{\Delta E}{1152}$$

Summary:

To obtain the value of K and hence I_{sref} proceed as follows:

1. Start with some value of K (initial condition)
2. Measure the capacitor Voltage at the start and the end of a period of τ (20ms). (This can be conveniently measured at the zero crossing point of the source Voltage).
3. Use eqns {3.31, 3.32} to obtain the energy change
4. Use eqn {3.35} to obtain the new value of K
5. Use eqn {3.29} to obtain I_{sref} in terms of the source Voltage
6. Carry out 2 to 5 indefinitely

Eventually K and hence I_{sref} will settle to a steady value until the load changes, when the algorithm will find new steady values.

Note

The above algorithm will attempt to produce an ideal energy balance without regard to the final capacitor Voltage V_{cap}.

When energy balance is required with respect to a specific Voltage level (as it will be for the first order DSM controlled system) then V_{capold} in eqn {3.31} and eqn {3.32} must be replaced with a given reference value V_{capref}. Methods of control of the capacitor Voltage will be dealt with in depth in later sections.

3.6.5 The Sliding Equation and derivation of the reference for the capacitor Voltage (V_{capref})

It was established in section 3.1.3 that the 1st-order sliding space is defined by:

$$S(t) = \dot{\tilde{x}}(t) + \lambda \tilde{x}(t) = \left(\dot{x}_d(t) - \dot{x}(t) \right) + \lambda \left(x_d(t) - x(t) \right)$$

With the choice of state variables (as given in section 3.6.2) then it has been shown that the 1st-order sliding space is only valid when $\beta = 1$.

Examining the system equations (Table 3.4) it can be seen that these two variables are related by:

$$\frac{dV_{cap}(t)}{dt} = \alpha.\beta.\frac{I_f(t)}{C} \qquad \text{-----\{eqn 3.36\}}$$

also:

$$\alpha \frac{dV_{cap}(t)}{dt} = \beta.\frac{I_f(t)}{C} \quad \text{since } \alpha^2 = 1$$

As given in section 3.6.2:

$$x(t) = \alpha V_{cap}(t) \qquad \text{----\{eqn 3.37\}}$$

$$\dot{x}(t) = \alpha \dot{V}_{cap}(t) = \frac{I_f(t)}{C} \qquad \text{----\{eqn 3.38\}}$$

Also $\dot{\tilde{x}}(t) = \frac{I_{fref}(t)}{C} - \frac{I_f(t)}{C}$ $\qquad \tilde{x}(t) = \alpha\left(V_{capref}(t) - V_{cap}(t)\right)$

(which is true only when $\beta = 1$).

Therefore when the system resides on the sliding surface:

$$S(t) = \frac{I_{fref}(t)}{C} - \frac{I_f(t)}{C} + \alpha\lambda\left(V_{capref}(t) - V_{cap}(t)\right) = 0 \qquad \text{-----\{eqn 3.39\}}$$

($S(t) = 0$ when sliding)

Using eqn {3.38} in eqn {3.39} gives:

$$\alpha.\dot{V}_{cap}(t) + \alpha.\lambda.V_{cap}(t) = \frac{I_{fref}(t)}{C} + \alpha.\lambda.V_{capref}(t)$$

or

$$\dot{V}_{cap}(t) + \lambda.V_{cap}(t) = \alpha\frac{I_{fref}(t)}{C} + \lambda.V_{capref}(t) \qquad \text{-----\{eqn 3.40\}}$$

In steady state it is required that $I_f = I_{fref}$ and $V_{cap} = V_{capref}$

In steady state ($\beta = 1$) eqn {3.38} must still hold therefore:

$$\frac{dV_{capref}(t)}{dt} = \alpha.\frac{I_{fref}(t)}{C} \qquad \text{-----\{eqn 3.41\}}$$

In steady state it is required that the average capacitor Voltage remains close to a known constant value ($V_{capconst}$).

Assigning $V_{capref} = V_{capconst}$ then from eqn {3.41}

$\frac{dV_{capref}(t)}{dt} = \frac{dV_{capconst}}{dt} = 0$ therefore $I_{fref}(t) = 0$ which is *not* an acceptable solution.

The solution that satisfies the above equations {3.39}, {3.40}, {3.41} is:

$$V_{capref}(t) = \beta.V_{capconst} + \frac{\beta}{C}\int \alpha(t).I_{fref}(t)dt \qquad \text{-----\{eqn 3.42\}}$$

Equation {3.42} is the key to enabling sliding mode to control both filter current and the average capacitor Voltage.

Using eqn {3.42} at steady state (for $\beta = 1$) , when $V_{cap}(t) = V_{capref}(t)$ equation {3.40} gives:

$$\alpha\frac{I_{fref}(t)}{C} + \lambda.V_{capref}(t) = \alpha\frac{I_{fref}(t)}{C} + \lambda.V_{capref}(t) \qquad \text{(i.e. balance is obtained)}$$

Using eqn {3.39} the sliding surface for $\beta = 1$ can now be formed as:

$$S(t) = \frac{I_{fref}(t)}{C} - \frac{I_f(t)}{C} + \alpha\lambda\left(V_{capconst} + \frac{1}{C}\int \alpha(t).I_{fref}(t)dt - V_{cap}(t) \right) = 0 \quad \text{-----\{eqn 3.43\}}$$

When $\beta = 0$ (absorbed-increasing mode) the capacitor Voltage remains steady and under these conditions:

$$S(t) = \frac{I_{fref}(t)}{C} - \frac{I_f(t)}{C} = 0 \text{ which reduces to } I_{fref}(t) = I_f(t)$$

Once V_{capref} has been obtained using eqn {3.42} it is important that this should be used in place of V_{capold} in equations {3.31} and {3.32}. ΔE in eqn {3.35} will then be the energy change of the APF storage capacitor relative to the capacitor reference.

The solution to the integral of eqn {3.42} poses some problems. It will be noticed that the switching variable α has been incorporated into the integral *as a function of time*; α must be applied to I_{fref} first *before* integrating. If α is treated as a constant and applied after the integral of I_{fref}, then the residual area under the function will cause a step discontinuity.
Furthermore, since equation {3.42} is strictly not applicable for the active absorbed-increasing modes then $\alpha.I_{fref}$ should be gated to zero at these times to prevent errors in the αI_{fref} area function. αI_{fref} should be integrated under all active delivered-increasing modes and all passive modes. For this purpose a signal must be generated which will be called *Ifref_gate* which defaults to 0. Ifref_gate is a tri-state variable that is evaluated each switching cycle by the DSM control algorithm to determine the next switching state.

The following table defines Ifref_gate:

APF mode	*State of Ifref_gate*
Active increasing *power* delivered to source	1
Active increasing *power* absorbed by APF	0
Passive phase with inductive *energy* entering capacitor (Vs +ve and If +ve or Vs –ve and If –ve)	1
Passive phase with inductive *energy* entering load (Vs +ve and If –ve or Vs –ve and If +ve)	-1

Table 3.5*: State definitions for the tri-state variable Ifref_gate*

Table 3.6 applies the same rectification to Ifref_gate as that applied to I_f in the subsequent period T by the H-bridge, i.e. it compensates for the direction of current flow around the H-bridge.

There is a further problem implementing eqn {3.42} since a pure integrator will sum the area under $I_{fref}(t)$ and any transient effects will indefinitely affect $V_{capref}(t)$. The solution to this problem is to replace the integrator with a 1st order low pass filter with a long impulse response transient time constant.

Let the integrator be:

$G_i(s) = \frac{1}{s+a}$ and let a = 10 so that the impulse response time constant is 100ms (i.e. 5 periods of the mains). Any residual area under the filter current will be insignificant after a few mains cycles.

Using Discrete Sliding Mode, it is appropriate that $G_i(s)$ is transformed into the Z domain to get:

$$G_i(z) = \frac{T.z}{z - e^{-a.T}} = \frac{T.z}{z - e^{-10.T}} \qquad \text{-----\{eqn 3.44\}}$$

(T is the regular sample period of the Discrete Sliding Mode).
I_{fref} gated by Ifref_gate and by α, represents the current flowing into and out-of the capacitor. Under steady state conditions (for a non-linear but periodic load) the energy balance principle discussed in section 3.6.4 will force the area under $\alpha.I_{fref}$ to zero, (zero net charge over one mains cycle) however until steady state is reached, $\alpha.I_{fref}$ will in general have a non-zero integral i.e. there will be a residual area under $\alpha.I_{fref}$. To overcome this problem the average of the integral must be obtained and then subtracted from the resulting area. A suitable function for performing the average of the integral is:

$$G_a(s) = \frac{50}{s+50}$$

or as a function of z:

$$G_a(z) = \frac{50.T.z}{z - e^{-50.T}} \qquad \text{-----\{eqn 3.45\}}$$

There is yet a further problem to evaluating equation {3.42} which arises because in steady state the non-absorbed component of I_{fref} will be an ac signal so $\alpha.I_{fref}$ (gated by Ifref_gate) will be a dc signal and the result of integration will create an indefinitely increasing area sum function. To remove this, $\alpha.I_{fref}$ is passed through a function that blocks d.c. A suitable function is:

$$G_{dc}(s) = \frac{s}{s + 50}$$

or as a function of z:

$$G_{dc}(z) = \left(\frac{z-1}{z.T}\right)\left(\frac{T.z}{z - e^{-50T}}\right) = \left(\frac{z-1}{z - e^{-50T}}\right) \qquad \text{-----\{eqn 3.46\}}$$

A block diagram for evaluating equation {3.42} is:

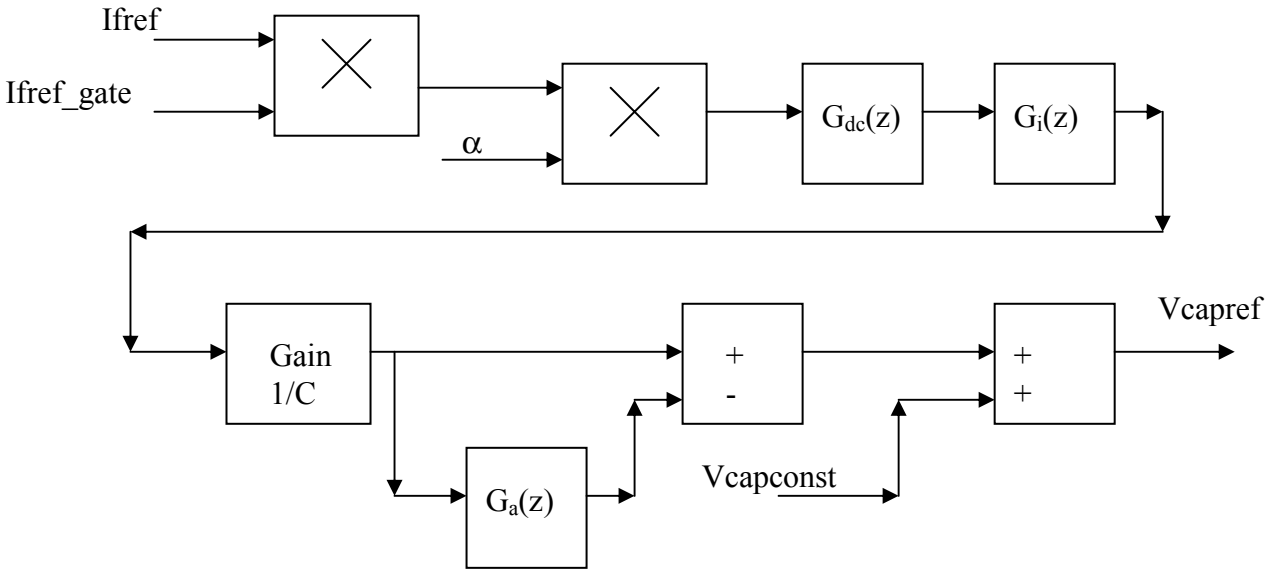


Fig 3.20*: Block diagram showing the derivation of Vcapref*

3.7 Using Lyapunov stability about the sliding surface to find the reaching condition

Using the reachability quoted earlier in section 3.1.5:

Eqn {3.1}:

$\frac{1}{2}\frac{d}{dt}S^2(t) = S(t).\dot{S}(t) \leq -\eta$ for η a positive constant

it follows that a sufficient condition for reachability is:

$\frac{1}{2}\frac{d}{dt}S^2(t) = S(t).\dot{S}(t) < 0$

It is necessary to find the reachability condition for the two states of β (β = 1 and 0).

From the time derivative of eqn {3.43} and noting that the derivative of $V_{capconst}$ (the time-invariant part of V_{capref}) is zero:

$$\dot{S}(t) = \frac{\dot{I}_{fref}(t) - \dot{I}_f(t)}{C} + \lambda\alpha\left(\frac{\alpha.I_{fref}(t)}{C} - \dot{V}_{cap}(t)\right) \quad \text{(for } \beta = 1\text{)}$$

and using eqn {3.8}

$$\dot{S}(t) = \frac{\dot{I}_{fref}(t) - \dot{I}_f(t)}{C} + \lambda\alpha\left(\frac{\alpha.I_{fref}(t)}{C} - \alpha.\beta.\frac{I_f(t)}{C}\right) = \frac{\dot{I}_{fref}(t) - \dot{I}_f(t)}{C} + \lambda\left(\frac{I_{fref}(t)}{C} - \frac{I_f(t)}{C}\right)$$

(for β =1)

When β = 0 the capacitor error component is removed giving:

$$\dot{S}(t) = \frac{\dot{I}_{fref}(t) - \dot{I}_f(t)}{C}$$

Therefore for β = 1 the requirement for sliding surface reachability is:

$$S(t).\left(\frac{\dot{I}_{fref}(t) - \dot{I}_f(t)}{C} + \lambda\left(\frac{I_{fref}(t)}{C} - \frac{I_f(t)}{C}\right)\right) \leq 0 \qquad \text{-----\{eqn 3.47\}}$$

For β = 0 the requirement for the sliding surface is:

$$S(t).\left(\frac{\dot{I}_{fref}(t)-\dot{I}_f(t)}{C}\right)\leq 0 \qquad \text{-----\{eqn 3.48\}}$$

The four active modes given in table 3.5 have to be applied to eqn {3.47} and eqn {3.48}

3.7.1 Reachability Conditions

3.7.1.1 Reachability Condition 1

$\beta = 0,\ \alpha = 1,\ \dot{I}_f(t)$ *+ve, S(t) > 0*

To guarantee reachability using eqn {3.48} $\dot{S}(t) < 0$

Therefore:

$$\dot{I}_{fref}(t) < \dot{I}_f(t)$$

3.7.1.2 Reachability Condition 2

$\beta = 0,\ \alpha = -1,\ \dot{I}_f(t)$ *-ve, S(t) < 0*

To guarantee reachability using eqn {3.48} $\dot{S}(t) > 0$

$$\dot{I}_{fref}(t) > \dot{I}_f(t)$$

3.7.1.3 Reachability Condition 3

$\beta = 1,\ \alpha = 1,\ \dot{I}_f(t)$ *-ve, S(t) < 0*

To guarantee reachability using eqn {3.47} $\dot{S}(t) > 0$

$$\dot{I}_{fref}(t)-\dot{I}_f(t) > -\lambda\left(I_{fref}-I_f\right)$$

3.7.1.4 Reachability Condition 4

$\beta = 1,\ \alpha = -1,\ \dot{I}_f(t)$ +ve, $S(t) > 0$

To guarantee reachability using eqn {3.47} $\dot{S}(t) < 0$

$$\dot{I}_{fref}(t) - \dot{I}_f(t) < -\lambda\left(I_{fref} - I_f\right)$$

3.7.2 Combined reachability conditions

Reachability Conditions 1 and 2 can be combined as:

$$abs\left(\dot{I}_{fref}(t)\right) < abs\left(\dot{I}_f(t)\right) \qquad \text{-----\{eqn 3.49\}}$$

Condition 3 and 4 can be combined as:

$$abs\left(\dot{I}_{fref}(t)\right) - abs\left(\dot{I}_f((t))\right) < -\lambda.abs\left(I_{fref} - I_f\right) \qquad \text{-----\{eqn 3.50\}}$$

from eqn {3.28} and eqn {3.30}:

$$I_{fref} - I_f = I_{sref} - I_s$$

This gives an alternative form for {3.50}:

$$abs\left(\dot{I}_{fref}(t)\right) - abs\left(\dot{I}_f((t))\right) < -\lambda.abs\left(I_{sref} - I_s\right) \qquad \text{-----\{eqn 3.51\}}$$

3.7.3 Practical Implications of DSM on the Reachability Condition

When applying the Reachability condition of eqn {3.51} the practical constraints of the DSM algorithm impose two factors that will violate the condition. In the event that either $\dot{I}_{fref}(t) > \dot{I}_f(t)$ or $\dot{V}_{Capref}(t) > \dot{V}_{Cap}(t)$ the condition cannot be met. These conditions indicate that the system is not fast enough to cater for the load conditions i.e. the physical system needs to be altered (either the inductor values or $V_{capconst}$). In fact the Reachability condition can be used as a measure of the APF's ability to harmonically correct a given load. If eqn {3.51} is always satisfied then the system

bandwidth is adequate for the load. The percentage of time that eqn {3.51} is violated can be used as a quality measure of the adequacy of the system's bandwidth.
To evaluate Reachability in the DSM system the following discrete block of fig 3.21 is used.

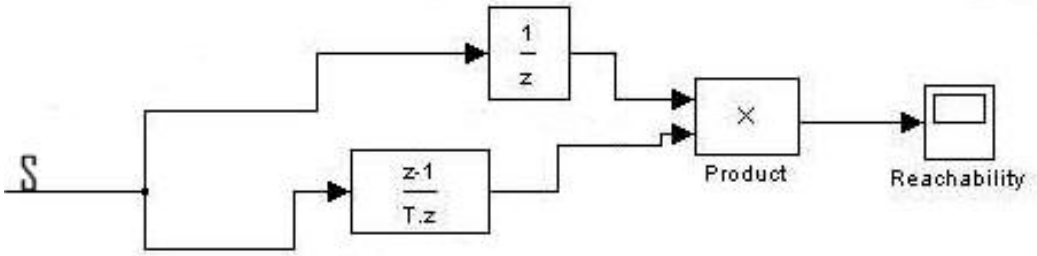


Fig 3.21*: Deriving the Reachability signal*

The sample period of the block is T.

Fig 3.21 will be included later in the full system simulation.

The rate of change of S is calculated as the slope over one sample period and is then multiplied by the value of S at the beginning of that sample period (hence the delay of T in the path of S).

3.8 The Single Phase 3/2 H-Bridge

This section deals with a new development of the H-Bridge that introduces an additional inductor to help achieve the reachability condition of eqn 3.51.

The value of $\dot{I}_f(t)$ is determined by the capacitor Voltage, $V_s(t)$ and L. Once $V_{capconst}$ and L have been selected for a specific design requirement, the maximum rate at which the filter current can flow is restricted. Setting L to a small value will enable a faster filter response but the overshoot in sample period T may be excessive.
The system presented here uses two inductors – a larger value when lower rates of APF current flow are required and a smaller value for the times when a larger rate of change of APF current is demanded by the load. The schematic of the 3/2 H-Bridge is given in fig 3.22 where the default "slow" inductor is L2 and the "fast" inductor is L1.

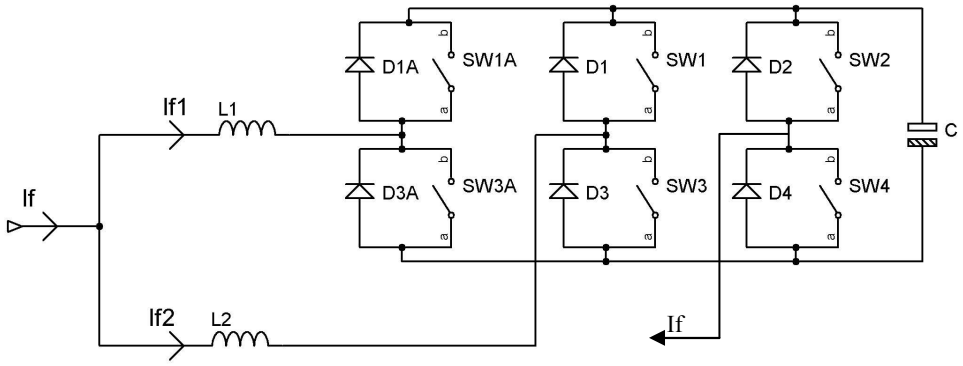


Fig 3.22: *3/2 H-Bridge showing two inductors ("slow" L2 and "fast" L1)*

A similar scheme has been suggested in ref [8.3] where L1 and L2 appear in series and the centre of the third "arm" is connected to the centre tap of the two inductors. When a high $\dot{I}_f(t)$ is required switches 1a and 1 operate together and switches 3a and 3 operate together. The effective inductance during fast $\dot{I}_f(t)$ is the parallel combination of L1 and L2.

An interesting consequence of the arrangement of L1 and L2 is that under some circumstances L1 and L2 act in series. Under some conditions when switch 3a and switch 1a are open it is still possible to measure current pulses in L1. The effect will occur during a passive cycle when L2, acting as a current source, will return magnetically stored energy back to the source which will cause one of the diodes in series with L1 to conduct. The current in L1 will always act against that in L2 which effectively reduces the current seen by the load. This reduced current would be similar to having a single inductor L2 of a slightly larger value (hence the series effect of L1 and L2). Since the effect is dependent on the source Voltage (magnitude and sign) then it is difficult to quantify. In practice the effect makes little difference to the results and has been ignored in the system control algorithm.

3.9 Application of Equivalent Dynamics to the H –Bridge

In this section, Filippov's construction is used to obtain the equivalent analogue range of β that will be used in the system design to evaluate λ. Also the implications of β both as an analogue and a digital variable are considered.

The time derivative of eqn 3.39 gives:

$$\dot{S}(t) = \frac{\dot{I}_{fref}(t) - \dot{I}_f(t)}{C} + \alpha\lambda\left(\dot{V}_{capref}(t) - \dot{V}_{cap}(t)\right) = 0$$

Using eqn {3.8} and eqn {3.42}

$$\dot{S}(t) = \frac{\dot{I}_{fref}(t) - \dot{I}_f(t)}{C} + \frac{\lambda.\beta.\alpha}{C}\left(I_{fref} - I_f\right) = 0$$

Using eqn {3.7}

$$\dot{S}(t) = \frac{\dot{I}_{fref}(t) - \frac{V_s(t)}{L} + \alpha.\beta\frac{V_{cap}(t)}{L}}{C} + \frac{\lambda.\beta.\alpha}{C}\left(I_{fref} - I_f\right) = 0$$

Table 3.4 clearly indicates that the equivalent switching input (that which switches between active increasing phases) is β. The equivalent dynamics can therefore be quoted in this context as $0 < \beta_{eq} < 1$. β_{eq} is the equivalent analogue input that would replace the switched input in the case of pure (infinite bandwidth) sliding mode. Applying these criteria results in:

$$\beta_{eq} = \alpha\left(\frac{V_s(t) - L.\dot{I}_{fref}(t)}{V_{cap}(t) + \lambda.L.\left(I_{fref}(t) - I_f(t)\right)}\right) \qquad \text{-----\{eqn 3.52\}}$$

Applying $0 \le \beta_{eq} \le 1$ gives:

$$0 \le \alpha\left(V_s(t) - L.\dot{I}_{fref}(t)\right) \le V_{cap} + \lambda.L.\left(I_{fref}(t) - I_f(t)\right)$$

Or $$0 \le \alpha\left(V_s(t) - L.\dot{I}_{fref}(t)\right) \le V_{cap} + \lambda.L.\tilde{I}_f(t)$$

$$0 \le \left(|V_s(t)| - \alpha L.\dot{I}_{fref}(t)\right) \le V_{cap} + \lambda.L.\tilde{I}_f(t) \qquad \text{-----\{eqn 3.53\}}$$

(where $\tilde{I}_f(t)$ is the APF error current)

3.9.1 Applying Active Conditions to β_{eq}

When β = 1 (Active power delivered phase)

Using Eqn {3.7}:

$$\alpha \dot{I}_{fref}(t) = \frac{|V_s(t)| - V_{capref}}{L}$$ (where L is either L2 or L1//L2)

Substituting for $\alpha \dot{I}_{fref}(t)$ into eqn {3.53} gives:

$$0 \le \frac{\tilde{V}_{cap}}{\lambda.L} \le \tilde{I}_f(t)$$ -----{eqn 3.54}

When β = 0 (Active power absorbed phase)

Using Eqn {3.7} gives $\alpha \dot{I}_f(t) = \frac{|V_s(t)|}{L}$

Substituting for $\alpha \dot{I}_{fref}(t)$ into eqn {3.53} gives:

$$0 \le V_{cap} + \lambda.L.\tilde{I}_f(t)$$

$$\therefore -\tilde{I}_f(t) \le \frac{V_{cap}}{\lambda L}$$ -----{eqn 3.55}

Eqn {3.55} gives a lower bound on I_f. There is no capacitor control when β = 0.
Eqn {3.54} gives:

β = 1 when the filter current error is greater than $\frac{\tilde{V}_{cap}}{\lambda.L}$

β = 0 when the filter current error is less than $\frac{\tilde{V}_{cap}}{\lambda.L}$

The use of the equivalent construction presents β_{eq} given by eqn {3.52} as an analogue variable between 0 and 1.

When there is no error ($\tilde{I}_f(t) = 0$ and $\dot{\tilde{I}}_f = 0$) eqn {3.54} gives $\tilde{V}_{cap} = 0$

and eqn {3.52} gives: $\beta_{eq} = \frac{|V_s(t)|}{V_{cap}(t)}$ -----{eqn 3.56}

Since $\beta_{eq} \leq 1$, then $|V_s(t)| \leq V_{cap}$ which forces V_{cap} to be at least equal to the peak of the source Voltage.

3.9.2 Switching control when β=0

It is evident that the first order sliding surface is not applicable when β = 0. There is a case for switching λ to zero during these modes, however this will cause large swings in $\tilde{I}_f$ (see discussion in section 3.1.4). To minimise the changes in $\tilde{I}_f$ it has been decided to maintain the 1st order switching surface for all passive and active modes. During the modes when β = 0, the system will continue to switch about s(t) =0 but there will be no movement in the direction of $\tilde{x}$ since the capacitor Voltage will not change.

3.10 Demonstrating the advantages of a class C^0 current reference function

A class C^0 function is one which is continuous but whose 1st derivative is discontinuous. For a smooth $V_s(t)$ and $V_{cap}(t)$, eqn {3.7} gives $\dot{I}_f(t)$ as a smooth function. For a steady load $\dot{I}_f(t) = \dot{I}_s(t)$ and so $\dot{I}_s(t)$ is also a smooth function. This implies that $I_s(t)$ must belong the class of C^1 functions. To prevent any higher order harmonics being imposed onto $I_s(t)$ it is important to make $I_{sref}(t)$ a smooth function i.e. $I_{sref}(t)$ should also belong to the class of C^0. When the load changes, K should be updated at the zero crossing point of $V_s(t)$ to give the new value of $I_{sref}(t)$ (where I_{sref} is given by eqn {3.29}). This will prevent discontinuities (and hence high order harmonics) being introduced into $I_{sref}(t)$. By sampling the capacitor Voltage at the zero crossing points of the mains and updating K after a short calculation time (i.e. a time significantly shorter than the mains period), the current reference $I_{sref}(t)$ becomes a continuous function but the derivative $\dot{I}_{sref}(t)$ is not continuous (there is a discontinuity when K is updated) so such a function belongs to the class C^0. When steady state is reached, $\dot{I}_{sref}(t)$ become continuous.

If the capacitor is periodically sampled at any other point along the mains cycle then K can still be derived from the energy difference calculation of eqn {3.32} but $I_{sref}(t)$ will contain discontinuities and will therefore not belong to class C^0.

The following example examines a load that on average remains steady but oscillates (periodically) forcing K to change periodically.

Let K be represented by:

$K(t) = k.(1 + a(t))$

Where a(t) = A for $(2n\tau < t < (2n+1)\tau)$ (τ = mains period)

a(t) = -A for $((2n+1)\tau < t < (2n+2)\tau)$

and $n \in N : n \geq 0$ (N is the set of natural numbers)

Assuming that the mains Voltage is sinusoidal then it follows:

$$I_{sref}(t) = V_s(t)K(t) = kV \sin \omega t(1 + a(t)) \text{ where } \omega = \frac{2\pi}{\tau}$$

a(t) is a square wave with period 2τ and amplitude A so:

$$a(t) = \frac{4A}{\pi}\left(\sum_{n=0}^{\infty} \frac{\sin\left[(2n+1)\frac{\pi t}{\tau}\right]}{(2n+1)}\right)$$

$$\therefore I_{sref}(t) = kV \sin \omega t\left(\frac{4A}{\pi}\left(\sum_{n=0}^{\infty} \frac{\sin\left[(2n+1)\frac{\pi t}{\tau}\right]}{(2n+1)}\right) + 1\right)$$

$$= kV\left(\frac{2A}{\pi}\sum_{n=0}^{\infty} \frac{\cos\left(\left(\frac{2\pi}{\tau} - (2n+1)\frac{\pi}{\tau}\right)t\right) - \cos\left(\left(\frac{2\pi}{\tau} + (2n+1)\frac{\pi}{\tau}\right)t\right)}{2n+1} + \sin \omega t\right)$$

$$= kV\left(\frac{2A}{\pi}\sum_{n=0}^{\infty} \frac{\cos\left((1-2n)\frac{\pi}{\tau}t\right) - \cos\left((3+2n)\frac{\pi}{\tau}t\right)}{2n+1} + \sin \omega t\right)$$

$$= kV\left(\frac{2A}{\pi}\left[\cos\left(\frac{\pi t}{\tau}_{n=0}\right) + \frac{1}{3}\cos\left(\frac{-\pi t}{\tau}_{n=1}\right) + \frac{1}{5}\cos\left(\frac{-3\pi t}{\tau}_{n=2}\right) + \frac{1}{7}\cos\left(\frac{-5\pi t}{\tau}_{n=3}\right) \ldots - \cos\left(\frac{3\pi t}{\tau}_{n=0}\right) - \frac{1}{3}\cos\left(\frac{5\pi t}{\tau}_{n=1}\right) - \frac{1}{5}\cos\left(\frac{7\pi t}{\tau}_{n=2}\right) - \frac{1}{7}\cos\left(\frac{9\pi t}{\tau}_{n=3}\right) \ldots\right] + \sin \omega t\right)$$

$$= kV\left(\frac{2A}{\pi}\left[\frac{4}{3}\cos\left(\frac{\pi t}{\tau}\right)-\frac{4}{5}\cos\left(\frac{3\pi t}{\tau}\right)+\left(\frac{1}{7}-\frac{1}{3}\right)\cos\left(\frac{5\pi t}{\tau}\right)+\left(\frac{1}{9}-\frac{1}{5}\right)\cos\left(\frac{7\pi t}{\tau}\right)+\left(\frac{1}{11}-\frac{1}{7}\right)\cos\left(\frac{9\pi t}{\tau}\right)...\right]+\sin\omega t\right)$$

----{eqn 3.57}

$$= kV\left(\frac{2A}{\pi}\left[\frac{4}{3}\cos\left(\frac{\pi t}{\tau}\right)-\frac{4}{5}\cos\left(\frac{3\pi t}{\tau}\right)+\sum_{\substack{m=5\\ m:odd}}^{\infty}\left(\frac{1}{m+2}-\frac{1}{m-2}\right)\cos\left(\frac{m\pi t}{\tau}\right)\right]+\sin\omega t\right)$$

-----{eqn 3.58}

For all m > 4: $\frac{1}{m-2}-\frac{1}{m+2}<\frac{1}{m}$

(m: odd)

$$\frac{4}{m^2-4}<\frac{1}{m}$$

It can be seen that the harmonics rapidly reduce. The only significant harmonics present in $I_{sref}(t)$ are at half the mains frequency (25Hz) and at 3/2 times mains frequency (75Hz).

Comparing the following two plots it can be seen how little contribution is made by the higher order harmonics emphasising the advantage of this method of deriving the current reference.

The first plot is that of equation 3.57 (i.e. including the harmonics up to the 9th of half mains frequency).

The following values were used:

V = 340, τ= 20ms, k=0.1 (10 ohms average load) A = 0.1 (i.e. k varying +/- 10%)

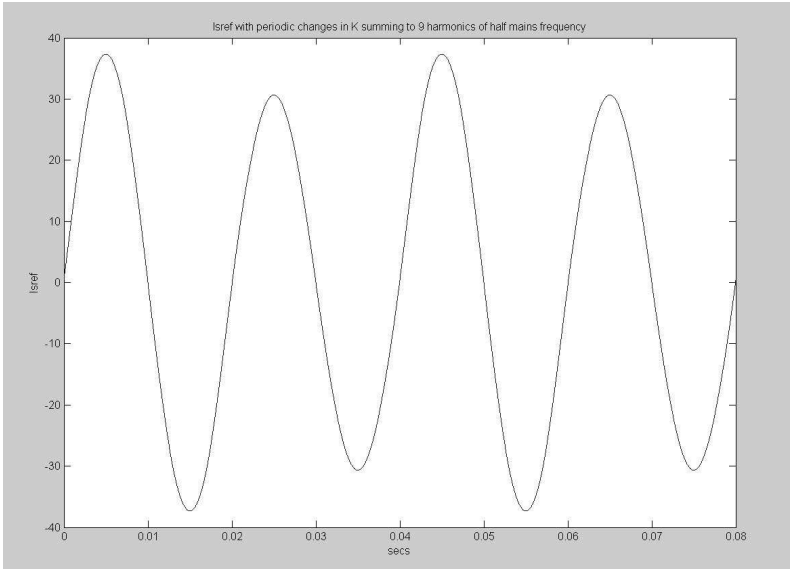


Fig 3.23*: A plot of I_{sref} v time for a periodically changing load. All harmonics up to the 9th are included.*

The second plot is with the higher harmonics removed:

$$I_{sref}(t) = kV\left(\frac{2A}{\pi}\left[\frac{4}{3}\cos\left(\frac{\pi t}{\tau}\right) - \frac{4}{5}\cos\left(\frac{3\pi t}{\tau}\right)\right] + \sin\omega t\right)$$

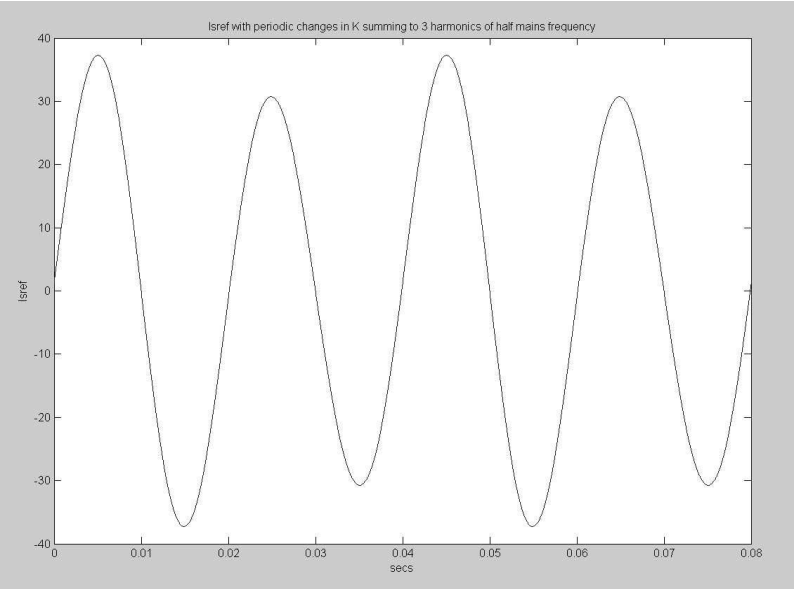


Fig 3.24*: As fig 3.23 but only including harmonics up to the 3rd*

The well defined harmonic structure and the suppression of higher harmonics is an advantage of the discrete K method where sampling takes place at the periodic zero crossing of the source Voltage.

3.11 Design of the H-Bridge and the Derivation of Associated Component Values

This section details the component design of the APF system using the 3/2 H-Bridge. The values to be presented here will be used later in the simulation of the system.

3.11.1 Considerations of Power Transistor specifications

See refs [10.1, 10.2, 10.3, 10.4 10.5]

It is necessary to consider the characteristics of power transistors for practical use so that a realistic sampling period (T) can be chosen.

There are three choices:

- BJT (Bi-Polar Junction Transistors
- IGBT (Insulated Gate Bi-Polar Transistors)
- MOSFET (Metal Oxide Semiconductor Field Effect Transistors)

BJTs have the advantage of lower turn-on Voltages when saturated, but to achieve this state requires a large base current (of the order of a fifth of the collector current). Also they require high reverse base drive currents to achieve fast turn off. The BJT and the IGBT both rely on minority carriers and since holes have a longer lifetime than electrons then hole conduction in the base region means that then they are much slower than MOSFETs. The IGBT comprises an input FET which provided the base current to an output BJT and therefore has the advantage of a simplified drive circuit. The advantages of using either MOSFETs or IGBTs for power applications outweigh those of the BJT and most modern designs therefore use either the MOSFET or the IGBT. It is the intention of this section to choose which technology would be most suitable for the H-Bridge application.

The MOSFET (see ref [10.5]) is a development of the Field Effect Transistor of the 1970's. The MOSFET is a majority carrier device and therefore is capable of higher switching frequencies. The forward Voltage drop of BJT's reduces with temperature and therefore is subject to thermal runaway. Parallel connection of multiple BJTs presents problems since as the forward Voltage drop reduces with temperature this causes one device to over-current. Conversely, the MOSFET forward Voltage drop increases with temperature, and this allows the parallel connection of multiple MOSFETs since they will tend to current-share. For higher specified Voltages, the forward Voltage drop of BJT's is lower than the equivalent MOSFET which increases the MOSFET package power dissipation compared to BJT's. Due to the construction of the MOSFET there will be a reverse body diode (which may or may not be convenient depending on the application). Since the H-Bridge requires the reverse bias diode for each device then this feature is an advantage. However the reverse breakdown Voltage of this body diode limits the upper Voltage specification of these devices. For sufficiently high Voltages, avalanche breakdown can occur in the off state (when the gate-drain is shorted).

The IGBT (see ref [10.2]) has superior conduction characteristics (they are less dependent on Temperature and Voltage) but generally have slower switching speeds than MOFETS. Unlike the MOSFET there is no reverse body diode so for the H-

Bridge application an external additional device needs to be included. This has some advantages in that the diode specification can be individually selected. Some manufactures produce a “Co_Pak” which includes a diode with the IGBT as one device.

Apart from a P+ substrate, the IGBT construction is the same as the MOSFET, however the characteristics are similar to the BJT. The IGBT is effectively a PNP output driven by an N-channel MOSFET. The base of the PNP is not brought out which affects the turn-off time since there is no active removal of base charge. The on-state Voltage of the IGBT never drops below a diode threshold since the arrangement cannot saturate the PNP (in this respect it is similar to a Darlington). Since the PNP is never saturated, it will turn off quicker than a fully saturated BJT under the same conditions. For larger currents the IGBT on-state Voltage can be affected by the gate Voltage of the input MOSFET unlike the power MOSFET whose on-state Voltage is fairly insensitive to input gate Voltage.

The design for the H-Bridge can use either MOSFETS or IGBTs.

The two key H-Bridge application limitations are the maximum off-state Voltage and the on-state current. The effect of the bridge is to act as a boost converter so the off-state Voltage must be at least twice the peak of the input source (680V) to cater for the worst case instantaneous Voltage. In addition, there will be mains-borne transients, therefore a device of typically greater than 800V should be chosen. Step 2 of section 3.11.5 gives a typical current requirement of at least 16.7A.

Some typical MOSFETS for consideration:

- STE45NK80ZD MOSFET from ST Microelectronics. 800V, 25A continuous current at 25°C
- STE40NK90ZD MOSFET from ST Microelectronics. 900V, 40A continuous current at 25°C
- FQA13N80_F109 MOSFET from Fairchild. 800V 12.6A continuous current at 25°C

Some typical IGBTs for consideration:

- FGA15N120AND IGBT Co-Pak from Fairchild. 1200V 24A continuous current at 25°C
- HGTG18N120BND IGBT with Anti-parallel “hyperfast” diode from Fairchild. 1200V 54A continuous current at 25°C
- FGA25N120ANTD IGBT from Fairchild. 1200V 25A continuous current at 25°C
- FGL40N120AN IGBT from Fairchild. 1200V 40A continuous current at 25°C
- HGTG11N120CND with Anti-parallel “hyperfast” diode from Fairchild. 1200V 43A continuous current at 25°C

- IRG4PF50W IGBT from International Rectifier. 900V 51A continuous current at 25°C
- IRG4PH50U IGBT from International Rectifier. 1200V 45A continuous current at 25°C
- IRG4PSH71K IGBT Co-Pak from International Rectifier. 1200V 78A continuous current at 25°C
- IRG4PSH71UD IGBT from International Rectifier. 1200V 99A continuous current at 25°C
- IRGPS40B120U IGBT from International Rectifier. 1200V 80A continuous current at 25°C
- IRGPS60B120KD IGBT from International Rectifier. 1200V 105A continuous current at 25°C
- STGW30N90D IGBT from ST Microelectronics. 900V 60A continuous current at 25°C
- STGW30NC120HD IGBT from ST Microelectronics. 1200V 60A continuous current at 25°C

The specified switch-on times for IGBTs are typically of the order of 30ns to 100ns and the off times are typically 150ns to 350ns. Package dissipation limits the switching capability. Switching losses of the device are affected by the dI/dt characteristics for the device and for a given V_{ce} and I_c the package dissipation is therefore dependent on the frequency of operation.
Over the last few years the popularity of the IGBT has grown. Modules are available comprising 4 IGBTs and 4 diodes arranged as an H-bridge in a package that can be conveniently bolted to a heatsink (see ref 10.6). Such a device (SK30GH123) will be used in the low Voltage demonstration test rig (chapter 5). This device is capable of withstanding a collector – emitter Voltage of 1200 V and a maximum collector current of 33A. The switch-on time is typically 40ns at a collector current of 20A and the turn-off time is typically 300ns at 20A but the turn off time can increase to 400ns at 5A.

3.11.2 Choosing T

The first step is to decide on a value for the DSM switching/sampling time T. T will determine the speed at which the transistor switches must operate. Although shown as ideal switches for the purpose of simulation, the limitation of speed of practical MOSFETs or IGBTs is a prime concern. Since the DSM scheme is basically an active phase followed by a passive phase then the maximum frequency of operation will be (0.5/T)Hz provided the sliding surface is crossed each period (see algorithm fig 3.14).

For the model, T has been set to 20 μs giving an operating frequency of 25kHz. This frequency will allow choice of devices from either MOSFET or IGBTs .

3.11.3 Selecting a minimum value for $\dot{I}_f(t)$

The maximum change rate in APF current depends on the maximum change rate of load current, which in general is unknown.
Initially it is necessary to specify a maximum RMS value for the APF current $I_{fRMSmax}$. A method of approach for this is dealt with in the next section.

For a fundamental sine wave at 50Hz with a peak current of $\sqrt{2}*I_{fRMSmax}$ the maximum current gradient is $2*\pi*50*\sqrt{2}*I_{fRMSmax}$. This value should be selected as a *minimum* for $\dot{I}_f(t)$ since any value lower than this will cause "fundamental slope overload".
Therefore:

$$\dot{I}_{f\min} > 444.3 * I_{fRMS\max} \qquad \text{-----\{eqn 3.59\}}$$

Note that under steady state conditions, (assuming that the system is able to follow I_{sref} exactly and that V_s is purely sinusoidal) then I_f will generally consist only of the reactive and harmonic component which will consist of a 50Hz component 90^0 phase shifted from $I_s(t)$ plus higher order harmonics.

Let the maximum design value be $\dot{I}_{f\max}$. Selection of this value depends on L1 and L2 of the 3/2 H-Bridge and is presented in the next section.
For the nth harmonic current component of RMS value I_{fn}, the maximum slope will be $2*\pi*50*n*\sqrt{2}*I_{fn}$.
The APF's ability to handle harmonic components in terms of the slope overload limit is given by: $2*\pi*50*n*\sqrt{2}*I_{fn} < \dot{I}_{f\max}$

therefore: $$n.I_{fn} < \frac{\dot{I}_{f\max}}{444.3} \qquad \text{-----\{eqn 3.60\}}$$

3.11.4 Criteria for Selecting $V_{capconst}$, C, L and λ

The method of selecting values for $V_{capconst}$, C, L and λ follows:

Step 1

The maximum current demand of the installation and hence the maximum VA rating should be specified.

Step 2

A value for the worst case RMS filter current has to be specified. However, since the load and its reactive component are undefined, then assume that the reactive component to be compensated by the APF is based on a phase shifted fundamental current sine wave (i.e. use eqn {2.9} and eqn {2.16}) with a specified power factor for the load. Hence calculate the worst-case RMS current ($I_{f\,RMSmax}$) that the APF will supply.

Step 3

In order to specify the rectifiers and transistors of the bridge, it is necessary to know the peak and average current flow. Knowing the worst case *RMS* current ($I_{f\,max}$), the peak current can be calculated as $\sqrt{2}*I_{f\,RMSmax}$ and the worst-case *average* current from the APF calculated as $\sqrt{2}*I_{f\,RMSmax}/\pi = I_{f\,ave}$.

Step 4

An average Voltage (introduced in eqn {3.42} as $V_{capconst}$) for the capacitor should be specified. For a 240V RMS source it is recommended that this should be typically at least 200V above the peak of the source to enable current to be driven back to the source. The level chosen will determine the bandwidth of the system (i.e. the max rate of change of APF current).

Step 5

A worst-case capacitor Voltage deviation about the average value has to be specified. It is recommended that for a 240V RMS source, V_{capdev} should be no more than 40V. C can then be evaluated using the VAR flow in the APF from step 2.

Notes:

V_{capdev} is defined as the Voltage deviation from $V_{capconst}$ so a specification of 40 V means a total capacitor Voltage change of 80V.

During steady state (when K has stabilised) only the VAr component specified in step 2 will flow in the capacitor since in steady state $V_{capold} = V_{capnew}$ giving $\Delta E = 0$ in eqn {3.35}.

The change in capacitor energy that occurs over half a mains cycle can be calculated by assuming that the movement in capacitor Voltage is symmetrical about $V_{capconst}$. At some point on the mains cycle $V_{cap} = V_{capconst} + V_{capdev}$ and at a point on the mains cycle $\tau/2$ later, $V_{cap} = V_{capconst} - V_{capdev}$.

It follows that the change in capacitor energy over half a mains cycle is:

$$\Delta E = \frac{1}{2} 2CV_{capdev} 2V_{capconst} = 2CV_{capdev} V_{capconst}$$

The reactive power flowing in the APF can be calculated by considering the change in capacitor energy over half a mains cycle using:

$$VAR = \frac{C.V_{capconst} 2V_{capdev}}{\tau/2}$$

Using $\tau/2 = 0.01$, calculate C:

$$C = \frac{VAR}{V_{capconst} 2V_{capdev} * 100} \qquad \text{-----\{eqn 3.61\}}$$

Step 6

It is necessary to specify a value for the sample time T. This is determined from knowledge of the switching capability of the transistors. The maximum switching frequency occurs in DSM when an active phase is followed by a passive phase. This gives the maximum switching frequency as 1/(2*T) Hz.

Step 7

It is necessary to specify a minimum value for $\dot{I}_{f\,\min}$ using eqn {3.59}. This is a fairly arbitrary choice since the harmonic structure of the load is not known. Choosing $\dot{I}_{f\,\min}$ in accordance with eqn {3.59} will prevent fundamental slop overload occurring.

Step 8

L2 (the "slow" inductor) has to be specified. It is known that the worst-case minimum driving Voltage occurs when the source is at the peak V and the system is in the power delivered state (minimising the differential Voltage between the source and V_{cap}).

L2 can be evaluated as:

$$L2 = \frac{V_{capconst} - V}{\dot{I}_{f\min}} \qquad \text{-----\{eqn 3.62\}}$$

Step 9

L1 (the "fast" inductor) has to be specified. The value of L1 depends on the maximum harmonic frequency that needs to be followed and compensated, which in turn depends on the load. Since the load is unknown then a more systematic method is required. After much investigation and simulation, the following method for selecting L1 is recommended.

The selected value for $\dot{I}_{f\max}$ should be that which occurs in the passive mode when the source is at the –ve peak and L2 is switched into circuit. V_{cap} and the source Voltage then point in the same direction around the loop comprising the bridge and the source giving:

$$\dot{I}_{f\max} = \frac{V_{capconst} + V}{L2} \qquad \text{----\{eqn 3.63\}}$$

To maintain symmetry, the max rate of change of I_f should have the same value at the extremes of the source Voltage. When V_s is at the positive peak (V), to achieve $\dot{I}_{f\max}$ the system must switch L1 into operation. The effective inductance is then L1//L2 = L1.L2/(L1+L2)

Therefore:

$$\dot{I}_{f\max} = \frac{V_{capconst} - V}{L1 // L2} = \frac{(L1 + L2)(V_{capconst} - V)}{L1.L2} \qquad \text{-----\{eqn 3.64\}}$$

Equating eqn {3.63} and eqn {3.64} and re-arranging:

$$\frac{L2}{L1} = \frac{V_{capconst} + V}{V_{capconst} - V} - 1 \qquad \text{-----\{eqn 3.65\}}$$

It is acknowledged that a higher value of $\dot{I}_f$ is achievable by switching L1 and L2 together (in parallel) when the source is at zero volts in the power delivered phase however this higher rate cannot deliver a symmetrical wave and is not included in this calculation.

Step 10

A value for λ has to be specified.

Eqn {3.55} can be used to obtain a limit for λ (the sliding mode time constant is 1/λ).

λ must be set to a value that satisfies eqn {3.55} for the maximum current error:

$$-\tilde{I}_f(t) \le \frac{V_{cap}}{\lambda L}$$

$$\therefore\ I_f(t) - I_{fref}(t) \le \frac{V_{cap}}{\lambda L}$$

$$\lambda \le \frac{V_{cap}}{L.I_{f\max}} \text{ when } I_{fref} = 0. \qquad \text{-----\{eqn 3.66\}}$$

In this equation, assume $V_{cap} = V_{capconst}$ and assume $I_{fmax} = \sqrt{2} * I_{fRMSmax}$ to obtain the minimum value of λ.

The choice of L can either be L2 or L1//L2 but choosing the larger inductor (L2) gives the minimum λ value.

L1 should only be used at extreme values of $\dot{I}_f(t)$

L2 is the normal switched inductor. If L1 is used in this calculation then λ will have a much larger value that will force the current error to be much larger (see section 3.1.4) and cause L1 to be used far more frequently as the overshoot of the error in I_f increases. The correct value of L to use here is therefore L2.

The designer should aim for a value of λ that causes the transient of the resulting 1st order system to die away within half the cycle of the source (i.e. τ/2 = 10ms).

Step 11

It is necessary to evaluate the worst case APF current overshoot as $\dot{I}_{f\max} T$ and assess its effect in the context of the system

Step 12

It is necessary to evaluate the APF's ability to deal with harmonic components by using eqn {3.60}.

3.11.5 Design Values for a Prototype APF

The following APF values are obtained form the criteria presented in the previous section and will be used later in the simulated model. Each step corresponds to the steps in section 3.11.4.

Step1

Since the APF is intended for domestic applications it will be assumed that a typical upper RMS value for I_s is 60A RMS. The maximum VA rating is then 14.4kVA for a 240 RMS supply.

Step 2

Using eqn {2.9} and eqn {2.16}, set cos(ϕ) at 0.96 (i.e. power factor of .96) giving sin(ϕ) = 0.28

For a 240 V RMS supply, the specified maximum load is 240*60 = 14.4kVA

The real load component is 13.824kW and the reactive component is 4.032VAr.

This gives the worst-case APF reactive current component as $I_{fRMSmax}$ = 16.8A RMS.

Step 3

For $I_{fRMSmax}$ = 16.8 A RMS the peak value of $I_f = I_{fmax}$=16.8*√2 = 23.76 A

The mean value of I_f over half a cycle is then I_{fave} = 23.76/π = 7.56A

Step 4

Since the peak of the mains supply is nominally 340, $V_{capconst}$ is set to 550 (just greater than 200 V above peak mains).

Step 5

Set V_{capdev} = 40 V. This means that the worst-case capacitor Voltage swing is from 590 to 510 V.

Using eqn {3.61} $C = \frac{VAr}{V_{capconst} 2V_{capdev} * 100}$ = 4032/(550*2*40*100) = 915 μF

The nearest preferred value is 1000 μF.

Step 6

For the prototype model, a value of T = 20μs has been chosen. This gives a maximum transistor switching frequency of 25kHz. (Two sample periods corresponds to a transistor switching cycle).

Step 7

Using eqn {3.59} $\dot{I}_{f\min} > 7464$ As^{-1}. Allowing for slightly higher current gradients and after much simulation it is suggested that the value of $\dot{I}_{f\min}$ should be set higher than the minimum value. However, much higher current gradients will cause excessive current overshoot. A value of $\dot{I}_{f\min} = 10^4$ As^{-1} is recommended.

Step 8

Using eqn {3.62} with $V_{capconst}$ = 550, V = 340

$L2 = 210/10^4 = 21$ mH

Step 9

Using eqn {3.63} $\dot{I}_{f\max} = \frac{V_{capconst} + V}{L2} = \frac{550 + 340}{0.021} = 42.4 kAs^{-1}$

Using eqn {3.65} $\frac{L2}{L1} = \frac{V_{capconst} + V}{V_{capconst} - V} - 1$ gives L2/L1 = 3.24

Giving L1 = 6.5mH

Step 10

Using eqn {3.66} $\lambda \leq \frac{V_{capconst}}{L2.I_{f\max}}$ gives $\lambda \leq 1102.3$.

Setting $\lambda = 1100$ satisfies the criteria even if the current error reduces.

Selecting $\lambda = 1100$ gives a sliding space time constant of 1/1100 = 0.91 ms.

Step 11

The worst-case APF current overshoot = $\dot{I}_{f\max} T$ =42.4 *10^3 * 20 e^{-6} = 0.848A. As a percentage of designed full load peak this is 3.57 % of the maximum peak APF current.

$\dot{I}_{f\max}$ will only occur under high load current changes.

For a low reactive load of 203 VAr (i.e. 240*0.848) containing high frequency harmonics causing the fast inductor to be switched into circuit, the overshoot would be as large as the harmonic components the APF was attempting to compensate. However since the designed power factor is 0.96 then the actual power component would be 696W. For this small load Is = 2.9 A RMS and the overshoot current is 29.2% of the supply current.

Therefore the effectiveness of the APF for fixed sample time T reduces as the load reduces with a fixed power factor. The only way to overcome this problem is to increase the sampling frequency as the load reduces which has an impact on the selection of bridge components. It is important therefore to note that an APF should be designed to match a specified load range and harmonic content.

Step 12

Using eqn {3.60} $n.I_{fn} < \dfrac{\dot{I}_{f\max}}{444.3}$

$n.I_{fn} < 95.43$

Noting that the maximum RMS current for the APF has been specified as 16.8A RMS then it can be seen that harmonics of the same maximum value up to n = 5 can easily be accommodated.

For example the APF can accommodate a 6^{th} harmonic of 15.9 A RMS.

3.12 Description of the Model used for Simulation

This section describes the APF simulation in detail using DSM with components specified in section 3.11.5.

Extensive use has been made of MATLAB, in particular “Simulink” for simulating the model (see refs [1.6], [1.7], [1.8], [1.9], [1.10]). The Electrical system (source and 3/2 H-Bridge) was simulated using the “Sim-Power-System” toolbox.

"Sim-Power-Systems" include interface blocks that allow current and Voltage parameters to feed into the signal flow diagrams of Simulink.

Refer to Appendix C for a complete graphical view of the MATLAB model.

All unit delays of T, zero-order hold blocks of T and digital filters based on sample time T are linked to the value T stored in the MATLAB workspace and set to 20μs (section 3.11.5 step 6).
The system is a mix of continuous and discrete blocks. A suitable solver for the system is the "ode23b" stiff solver (see [ref 1.7]). This solver is set to variable step with auto min and max step size. This arrangement has been shown to give good results and accurate system representation.

3.12.1 Simulation block "3/2 H Bridge"

The 3/2 H-Bridge discussed and presented in section 3.8 is shown in Sim-Power-Systems form in Appendix C: "3/2 H Bridge".
Each Arm of the bridge is constructed form an "ideal" diode and an ideal switch. The series resistance of the switch has been set to 0.01 Ohm. The switch properties include a parallel snubber circuit (series RC). The snubber resistor has been set to 100 Ohms and the capacitor to 10nF. Since the switch is modelled as a current source a snubber path is essential since then the switch cannot be left without a current path when switching into a series inductor (see MATLAB/Simulink help [ref 1.7]).
The diode property includes another parallel snubber circuit which has been set to 100 Ohm in series with 1nF and has an "on" forward Voltage set to 0.7V with an "on" resistance of 0.01 Ohm. Additionally the diode property includes an inductance which would be set to zero under normal circumstances, but has been set to 10uH in this simulation owing to problems that occur with the solver, the details of which follow in section 3.12.1.1.

Each switch has a control input such that logic 0 opens the switch and logic 1 closes the switch. The capacitor Voltage is interfaced with Simulink via the Voltage measurement block "Capacitor Voltage". Similarly, the capacitor current is measured using a current measurement block "Capacitor Current". Logical switch controls to all

switches are each fed through a delay unit of 1 microsec to overcome problems with the simulation (see section 3.12.1.2).

3.12.1.1 Overcoming Diode problems during Simulation

The model used by the MATLAB toolbox SimPowerSystems is as follows:

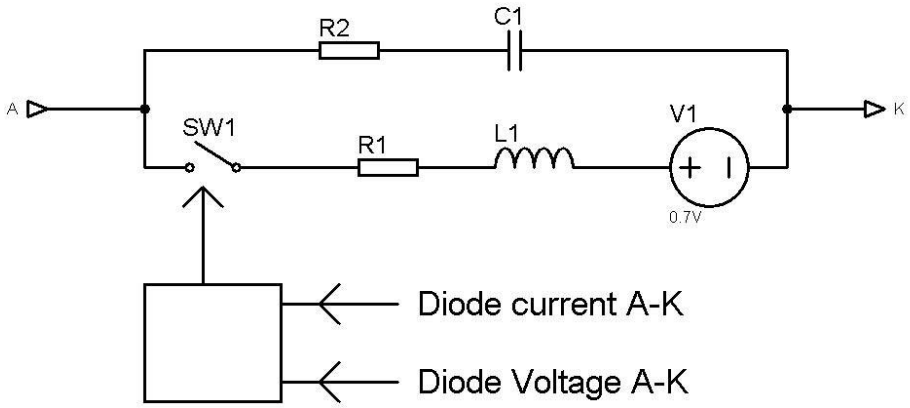


Fig 3.25: *SimPowerSystems Diode Model*

The following discussion requires reference to the 3/2 H-Bridge of Appendix B.

Currents are not established immediately in the diodes. There is a simulation step following the change of state of any of the switches before the diodes conduct. Furthermore currents already established in the diodes do not stop instantaneously. There is a simulation step following any switch change of state before a diode will stop conducting.
Unless these facts are appreciated, small changes in the APF storage capacitor Voltage will occur due to instantaneous spikes of current lasting for one simulation step. Although the spikes are very small, the energy change can lead to small errors in the harmonic correction of the supply source current (Is).

At the instant of switching any of the bridge arms, the APF input inductors (Lfast – L1 of Appendix B and Lslow – L2 of Appendix B) act as constant current sources and therefore there must be a path for the current to avoid problems with the simulation. Since the diodes do not conduct instantaneously, the inclusion of a snubber network is essential to avoid problems with the Simulink solver.

Also at the instant of switching there will be a conducting diode which instantaneously has the full Voltage of the APF storage capacitor applied to it in reverse bias. Although in the next simulation step the diode will be opened, there is one simulation step that will have a Voltage (typically 550 to 600V) across a diode resistance of 0.01 Ohm (on-resistance R1 in fig 3.25) leading to a current spike of tens of kA. To avoid this it is essential to include the series inductor (a small value such as 10uH is sufficient). In comparison with the values of L1 and L2 this is a very small inductor which will have no noticeable effect on the simulation results.

3.12.1.2 Overcoming ideal switch simulation problems

Careful examination of the currents and the reachability conditions of the simulation gave rise to some inexplicable results which were not immediately obvious. Eventually the problem was tracked to the ideal switches used in the H-bridge. Whereas the results were as expected for many samples of the simulation, it was noticed that occasionally (apparently at random) the switch would be set to close by the logical switch signal but the full bridge Voltage remained across the bridge for 1 sample period. It is possible to measure the switch's current and Voltage using the measuring port of the switch model when it was then discovered that the switches *internal* current for the occasional one sample period was in the region of 60kA (i.e. bridge Voltage divided by the ideal series resistance of 0.01 Ohm), whereas the current *external* to the switch was that expected from the model. This rather peculiar situation gave rise to the incorrect bridge Voltage being applied to the source which in turn led to the reachability condition breaking down for that sample period. The problem arose due to the order in which the solver updated the control loop. By putting a short delay in series with the logical control to all H-bridge switches, the problem was eliminated since it forces switch closure slightly later than the update time of the control parameters.

Since the sample time is 20μs then it was decided (arbitrarily) to set these delays to 1μs.

This strange situation would obviously not arise in practice; the 1μs delay is only included for simulation purposes.

3.12.2 Simulation block "Source"

Refer to Appendix C: "Source"
The source consists of an ideal sinusoidal Voltage of 340V amplitude at 50Hz.
The algorithm (switchcontoller3a.m – see section 3.12.5) produces Isref proportional to Vs so Isref will also be sinusoidal. If harmonics are introduced into Vs then they will appear in Isref so that the input appears purely resistive. Since the simulation is only intended for analysis and evaluation, then if the input is assumed purely sinusoidal it is easier to evaluate the DSM system and calculate THD from the results.

A Voltage measurement block passes signal V_s to the Simulink system.

Three current measurement interface blocks extract the signals I_s, I_f and I_L.

3.12.3 Simulation block "Non-Linear Load"

Refer to Appendix C: "Non-Linear Load"
The purpose of this section is to create a load that will disturb the current waveform away from a sine-wave. A set of simulations will be run and for each one the non-linear load will be changed to assess the effectiveness of the DSM system.
The initial settings for the load are as follows:
The load consists of a diode bridge (each diode has the same characteristics as in section 3.12.1.1 except that the series inductor is set to zero). The d.c. side of the bridge feeds a capacitor (80 μF or 40uF depending on selected load) and two resistors of 30 Ohm (Rload and Rload switched 1). The switched resistor is switched into circuit with a pulse generator via an "ideal" switch. The pulse generator is set to deliver logic pulses at a 5ms period with a pulse width of 50%.
The a.c. input to the bridge is fed via an inductor of 1mH or 35mH depending on selected load. The inductor helps to reduce initial inrush transient current to the capacitor.

3.12.4 Simulation block "Switching Controller"

Refer to Appendix C: "Switching Controller"

At the centre of the switching controller is the MATLAB function "Switch_Control3a.m" which is included in Appendix D. An input multiplexer and output de-multiplexer pass signals to and from the m-function.

The m-function is primarily responsible for setting up the sliding surface and implementing the DSM algorithm i.e. evaluating the next active phase or passive phase and setting the switch states appropriately. As part of this process the Reachability criteria (eqn {3.49}, eqn {3.51}) are used to determine whether or not to switch the "fast" inductor L1 into circuit.

I_f and I_{fref} are each put through a discrete gradient function $\frac{z-1}{Tz}$ to give the required derivative of these variables.

The signal "Ifref_gate" is generated which is used to gate the non-absorbed and passive modes of I_{fref} into the integration path to obtain V_{capref} (see section 3.12.6 on "Sliding Surface").

V_{cap} is taken to a delay unit of 20ms and a zero order hold of 20ms so that at each sample interval the m-function can have values for the capacitor Voltage at the most recent 20ms interval and the previous 20ms interval which can be used to determine K using eqn {3.32} and eqn {3.35}.

V_{capref} is passed through a 20ms holding function to ensure that the value remains steady for subsequent sample intervals. This ensures that the capacitor Voltage calculation is only updated at 20ms intervals. V_{capref} is filtered before sampling to remove any glitches using a 1^{st} order digital filter with a time constant of 2ms. Also a matching filter is used to filter V_{cap} prior to sampling. These filters simulate the effect of removing noise in a real system.

The K output form the MATLAB Function will depend significantly on the value of λ where λ is entered into the MATLAB workspace prior to running the simulation.

If λ is zero then the MATLAB function will reference the capacitor Voltage to its previous value to evaluate ΔE in the calculation of K. There will be no absolute control of V_{cap}. K-control ensures that the net energy change in the capacitor is zero.

At steady state, K will be stable and V_{cap} at the beginning and end of a cycle of τ will be unchanged.
When λ is non-zero V_{capref} replaces V_{capold} in eqns {3.31 and 3.32}
If λ is non-zero then ΔE is calculated (at the sample time τ) relative to V_{capref} at that sample instant where V_{capref} has been derived using the method developed in section 3.6.5.

3.12.4.1 Details of "switch_control3a.m"

Refer to Appendix D.
Lines 6 to 10 contain variable assignments.
Lines 12 to 31 assign variables to input parameters.

Lines 33 to 37 check the signal; "flag" which is a logic signal, fed through a delay unit of 20ms. K takes on the value 0.05 as default for the first 20ms otherwise it assumes the value of Kold, which is the previous value of K (i.e. K delayed by one cycle (20ms)). This initial condition for K is a fairly arbitrary choice, but should be set higher than the expected conductance range of the load to rapidly establish working conditions by forcing sufficient energy into the capacitor. In practice this value must be chosen as a compromise between quickly establishing working conditions and excessive inrush current.

Lines 38 to 43 evaluate the capacitor difference Voltage (dependent on λ) used in the iterative K calculation.

Lines 47 to 49 override any K calculation. If the initial value of K set in lines 33 to 37 was insufficient to set the capacitor to the correct working Voltage then K is lifted further. 0.01 is added to K every period τ until the capacitor Voltage reaches 550 V. By increasing K, I_{sref} increases which forces the APF to absorb more energy.

Lines 51-56 and 57-64 iteratively calculate K making use of the external 20ms delay unit. This section is activated after the initial 20ms start up transient by using "flag". Each time K is updated, I_{sref} is evaluated in line 65. The energy calculation is dependent on whether λ is zero or non-zero as described in section 3.12.4.

It is necessary to determine if the previous mode was passive, this is accomplished in line 66 with signal “check_sw”.

Lines 67-72 determine the state of Alpha. A dead band of +/0- 0.1 V of V_s is set which prevents dither at the zero crossing point, (important in a real practical situation where a bigger hysterisis band may be needed).

Line 74 is a default zero-order sliding space for the condition when Alpha is neither +1 nor –1 (i.e. in the zero crossing area of V_s) – important in a practical situation. (xdot is the error in APF current $(I_{fref} - I_f)/C$).

Lines 75 – 80 set up the sliding surface S(t) as dictated by equation {3.43}.

Lines 82 – 85 reset all four of the active state indicators.

All switch states are fed through an external delay unit of T. The old switch states indicate the previous mode of the system and are used in lines 88-99 to preset the active mode indicators. The active mode variables are as follows:

- pos_del_inc = positive mains cycle with power actively increasing from APF to source
- pos_abs_inc = positive mains cycle with power increasing and actively absorbed by the APF from the source
- neg_del_inc = negative mains cycle with power actively increasing from APF to source
- neg_abs_inc = negative mains cycle with power increasing and actively absorbed by the APF from the source

All 4 main switch variables (of the basic H Bridge) are reset to zero in lines 101-104.

Lines 105-120 set up Ifref_gate assuming that the next mode is passive.

The source current error is calculated in line 121.

Lines 130-179 determine the next mode of the system by checking whether the system is above or below the switching surface. If the next mode is active then the switches for the basic H-Bridge (s1 to s4) are set as required. The code here follows the principles of the flow chart set out in figure 3.14 for discrete sliding mode. This

code also uses the reachability conditions (eqn {3.49}, {3.51}) to set or clear the fast inductor status "fast_inductor". Additionally the signal "Ifref_gate" is cleared to zero when the system enters the active-absorbed-increasing modes or set to 1 when the system enters the active-delivered-increasing modes. "Ifref_gate" is then used in the "sliding surface" block in the evaluation of the capacitor reference as given in table 3.5. If the next switched mode is passive then after leaving this section of code, all switches s1-s4 will all be logic 0.

Lines 182 – 185 will reset the fast inductor switches (s1a, s3a) if the next mode is passive. This ensures that energy in L1 will be transferred back to the capacitor via the diode bridge in the passive mode.

Lines 188 - 192 implement the fast inductor if required by copying the state of sw1 to s1a and s3 to s3a.

Lines 195-202 ensure that all switches default to 0 in the first sample period T.

Finally the output signals are copied to the output parameters of the m-function in lines 204 to 213.

3.12.5 Simulation block "Switch Sampler"

Refer to Appendix C: Switch Sampler
Calculation of switch states in the m-file switchControl3a.m are updated every period T and this is accomplished with the "Switch Sampler" delay block.
All switch output signals s1 – s4 and s1a, s3a are passed through delays of T. This ensures that the m-function always has access to the most recent switch information to enable the next switching mode to be determined.

3.12.6 Simulation block "Sliding Surface"

Refer to Appendix C: Sliding Surface
The APF reference current error I_{fref} is obtained using eqn {3.30} and from this the error current $\tilde{I}_f$ is obtained then scaled by 1/C (scaling and unit conversion of Amps to Volts per sec as given by equation 3.8) and is fed through "Zero Order Hold 1 of T" before being presented to a block-port output as xdot which is used in the m-

function (section 3.12.4.1) to calculate S(t). “Zero Order Hold 1 of T” ensures a steady value and avoids computational errors. I_{fref} is gated in a multiplier by “Ifref_gate” (derived from the m-function described in section 3.12.4.1) and then multiplied by Alpha before entering the integration processing stages as described in fig 3.20. V_{capref} is obtained with reference to section 3.6.5 in particular eqns {3.44}, {3.45} and {3.46} from the dc decoupling and integration of I_{fref}. The output of the I_{fref} integral processing stage has to be passed via “Unit Delay1 of T” otherwise the solver cannot converge to a solution.
Alpha is obtained by passing V_s through a sign detecting switch function.

3.12.7 Simulation block “Measurements”

Refer to Appendix C: Measurements
For ease of use, all relevant measurement points are brought to one block.
In order to observe the progress of the states in sliding, an XY plot has been incorporated. The “x-axis” is driven from a signal derived in the block “sliding surface” which is the capacitor error Voltage switched by Alpha so that it is in the same phase as the calculation for S(t) performed in the m-function. The “y-axis” is driven from *xdot* (described in 3.12.6).
The “Measurements” block also contains the evaluation of the Reachability condition (see section 3.7.3).

3.13 Simulations and Results for a Zero and First Order control system using MATLAB function switch_control3a.m

Refer to Appendix C for the MATLAB model of the entire system and section 3.12 for a full description.

Throughout this section the switching controller will be using switch_control3a.m as described in section 3.12.4.1 to implement the DSM algorithm, handle switch-on transients and provide general system control.

For three different non-linear load conditions, the MATLAB simulation was run for a zero order ($\lambda = 0$) and a first order ($\lambda > 0$) DSM switching control giving six sets of results which are provided in Appendix F.

	Diode Bridge	Inductor	cload	Rload switched1	Rload	λ	Result set	Notes
Non-Linear Load 1	D2 open	1mH	open	open	30Ω	0	Appendix F: Result Set 1a	No V_{cap} control
						> 0	Appendix F: Result Set 1b	
Non-Linear Load 2	D2 in circuit (full bridge)	1mH	80μF	open	30Ω	0	Appendix F: Result Set 2a	No V_{cap} control
						> 0	Appendix F: Result Set 2b	
Non-Linear Load 3	D2 in circuit (full bridge)	35mH	40μF	30Ω	open	0	Appendix F: Result Set 3a	No V_{cap} control
						> 0	Appendix F: Result Set 3b	

Table 3.6: *Non-Linear Loads used for simulation*

The zero order switching control ($\lambda = 0$) is where the Voltage of the capacitor V_{cap} is not controlled, only I_f (the APF current) and hence I_s (the source current) is controlled. The condition $\lambda = 0$ is included only for comparison purposes i.e. it is of theoretical interest only. Since the capacitor Voltage is uncontrolled then the absolute value will be totally dependent on initial conditions.

The first order switching system ($\lambda > 0$) uses the discrete sliding mode principle to control both V_{cap} and I_f where $V_{capconst}$ (the demand value of V_{cap}) has been preset to 550V.

Before running the simulation, T and lambda must be assigned in the MATLAB workspace.
The effect of setting lambda to zero nulls the effect of the capacitor Voltage on the switching control. The capacitor is used as a sensor and its Voltage is used iteratively to control K by an energy calculation each cycle of the source Voltage (eqn {3.35}) When lambda = 0, V_{cap} will eventually settle to some Voltage which is dependent on initial conditions and load. System performance (i.e. system bandwidth) depends on V_{cap} so the switch_control3a algorithm will ensure that V_{cap} is at least 500V by initially adjusting K upwards if necessary, to increase the capacitor energy.

If lambda is set to a positive value, the capacitor will be controlled by discrete sliding, and the iterative K calculation will be based on the deviation of the sampled capacitor Voltage from the capacitor reference as given by eqn {3.42}.

3.13.1 Producing the frequency spectrum

For each result set it is necessary to examine the frequency spectrum of I_f, I_L and I_s since THD (Total Harmonic Distortion) calculations have to be performed as a measure of the effectiveness of harmonic cancellation. Also Total Harmonic current values need to be evaluated as well as Total Harmonic Voltage based on the mains specified impedance (see section 2.2.4) The calculations are performed using the m-function “freqplot3.m” which is described in the next section. The “scope” settings in the simulation for each of these variables (see “measurements” simulation block in Appendix C) are set to pass variables as an “array with time” to the MATLAB workspace. The solver will optimise the time points where calculations are to take place but this will not occur at regular time intervals. Therefore, the data for the three current variables has to be re-sampled to a regular time interval before being passed to the FFT function for frequency analysis. Re-sampling is accomplished with the spline function.

3.13.2 M Function “freqplot3.m”

Refer to Appendix E for a listing of this m function.

The m-function freqplot3.m performs the required operations outlined in section 3.13.1.

The function requires four parameters in the following order:
I_f, I_L, I_s, timelength
I_f, I_L, and I_s are the current arrays with time,
"timelength" is the length in seconds for which the simulation has been run (which has been set to 400ms).

A description of freqplot3.m follows:

Line 3: each two dimensional current array is passed to a variable as follows:
I_f to var_array1
I_L to var_array2
I_s to var_array3

Line 4: "timesample" is a one-dimensional array of time steps in μs from 0 to "timelength".

Lines 8 to 10: each current array is re-sampled to μs resolution using the "spline" function which calculates a best fit polynomial to the given data.

The frequency analysis must ignore initial transients and reference settling times, so only the last 50% of the "splined" data is passed to the FFT function. The simulations were run for 400 ms (i.e. 20 cycles of the 50Hz source) and then the last 10 cycles (200 ms) were frequency analysed.

Lines 11, 14: "start_time" and "stop_time" are set to 50% and 100% of "timelength" respectively in μs.

Lines 18 – 20: 200,001 point FFT's are computed over the last 50% of the splined data. This means that each point of the FFT corresponds to 5Hz . (i.e. $1*10^6/2*10^5$).

Lines 25 – 27: The RMS current spectrum is obtained for each FFT array by multiplying each element by its complex conjugate.
Since the FFT is a sum of N terms over the entire sample (i.e. N terms over 0.2 sec) then to correct the magnitude of the FFT output the magnitude of each output term must be divided by N/2 to obtain the peak value for each frequency.

Lines 28 – 30: The dc term is half the peak magnitude of the FFT calculation so the dc term of each RMS freq plot must be divided by 2. Also the dc terms must be multiplied by sqrt(2) to compensate for the preceeding RMS calculation. Index 1 is the dc term; MATLAB starts indexing from 1, index 0 does not exist in the FFT output.
Line 32: freqstep is set to 5Hz assuming that N is 200,001
Line 33: Only the first 100,001 points (for N =200,001) of the FFT are meaningful so a frequency axis variable "freqaxis" is defined up to N/2.

Lines 35 – 50: subplots are used to display three RMS current spectra.

Line58: Hz50step is the number of points between 50 Hz steps, which here will be 10 steps (50/freqstep where freqstep = 5). Index 1 is the dc term, index 11 is the 50Hz term, index 21 is the 100Hz term etc.

Lines 53 to 56 extract the fundamental and up to 40 harmonics of 50Hz.

THD calculations are performed over 40 harmonics (see eqn {2.4}) for IL in lines 63 to 74 and for Is in lines 80 to 97. These line also include Total Harmonic current calculation and Total Harmonic Voltage calculations based on R and L (lines 76, 77) (see section 2.2 and eqn {2.3}).

Lines 100 to 102: transpose the 50Hz harmonic arrays of RMS currents to columns ready for printing

Finally the THD calculations are printed together with the table of RMS current harmonics for If, IL and Is from the fundamental up to the 40^{th} (i.e. 2000 Hz).

3.13.3 Results Simulation Set 1a and 1b

(See Appendix F: Result Set 1a, Appendix F: Result Set 1b)

The two result sets 1a and 1b have the same load but set 1a uses zero mode switching ($\lambda = 0$) and set 1b uses 1st order ($\lambda > 0$) DSM switching. See table 3.6 for details.
For both simulation sets 1a and 1b the control algorithm switch_control3a.m (Appendix D) is used.

3.13.3.1 Non-Linear load used for Simulation Set 1a and 1b

The non-linear load circuit is given in Appendix C "non-linear load".
It is set up as given in Table 3.6 – non-linear load 1.
The non-linear load conditions are repeated here:

- D2: open (giving a half wave rectified load current)
- Inductor=1mH
- cload open
- Rload switched1 open
- Rload = 30 Ohm

The half wave rectified load current is of the form:

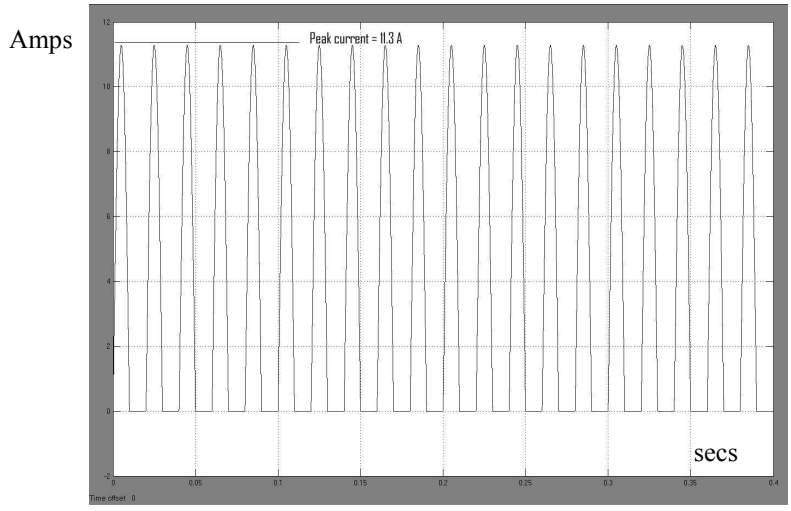


Fig 3.26: *Load current for 240V RMS source and 30 Ohm half wave load, showing a peak current of 11.31 A*

The Fourier series for this waveform is:

$$I_{Lpeak}\left[\frac{1}{\pi}+\frac{1}{2}\cos(\omega_0 t)+\frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1}{(4n^2-1)}\cos(2n\omega_0 t)\right] \quad \text{where } \omega_0 = 2\pi/T \text{ (T = 20ms)}$$

The series consists only of all the even harmonics plus a fundamental component of magnitude $0.5I_{Lpeak}$ and a dc term of $(1/\pi)I_{Lpeak}$.

The APF should therefore force the peak of the source current I_s to be 0.5 of 11.31 Amps = 5.66 Amps (or 4.0 A RMS). i.e. the APF should prevent the components of the load current only carrying reactive power from flowing in the source. It will be seen that this is the case in the next section.

3.13.3.2 Simulation Set 1a

See Results in Appendix F: Result set 1a

A zero-order switching space is used ($\lambda = 0$).

Once the capacitor has reached 500V the capacitor is no longer forced by a control system to any particular Voltage, the capacitor settles at a Voltage where the energy change per source cycle is zero.

The simulation was run for 400ms (20 cycles of 50Hz source).

The last 50% of the output was analysed for harmonic content using freqplot3.m (i.e. once initial transients have settled).

The following plot shows the resulting spectrum for Simulation Set 1a:

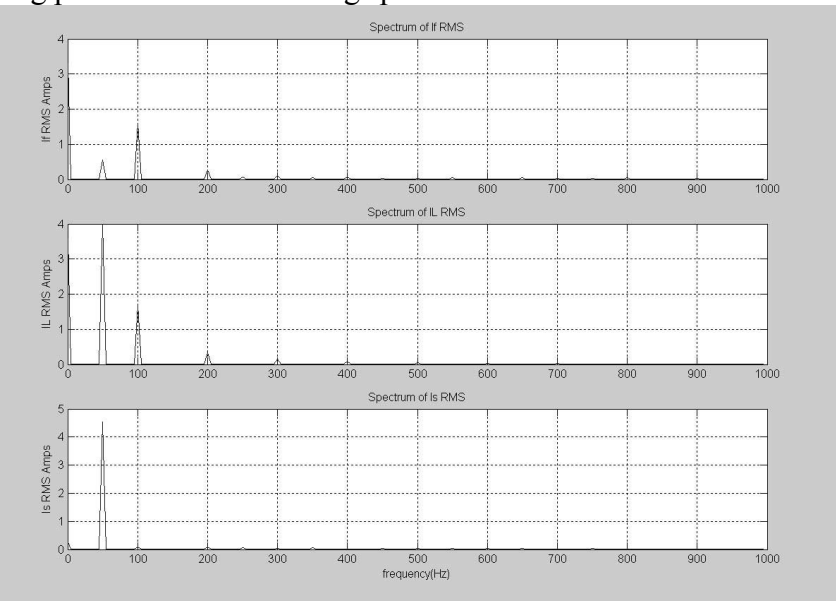


Fig 3.27: *Spectrum of If, IL, Is up to 1kHz for Result Set 1a*

The Total harmonic results for Simulation Set 1a are as follows:

- THD of I_L = 0.43747
- THD of I_s = 0.041918
- Total harmonic current for IL = 1.7425 A RMS
- Total harmonic current for Is = 0.19034 A RMS
- THD of Vs = 0.0020828
- Total harmonic Voltage = 0.49987 V RMS (for R= 0.25 Ohm, L = 796 μH)

The results indicate that a considerable improvement has taken place especially in the even harmonics. Note that the values of the fundamental of IL and Is are very close indicating that the source is providing the real power component of the load.
The peak of current I_s and $I_{s\,ref}$ can be seen to be approximately 5.7 Amps as expected from the Fourier harmonic analysis.
The THD has been reduced from 44% to 4.2% indicating a significant improvement.
The Total harmonic Voltage is considerably less than the allowable worst case (calculated in section 2.2 as 4.2307 VRMS).
K has reached a steady value of 0.0166 Mho (60 Ohm) which is the correct pure resistive load in this case. Note that K has stabilised from a switch on transient in a relatively short time of 0.1 sec.

3.13.3.3 Simulation Set 1b

See Results in Appendix F: Result set 1b

The 1^{st}-order discrete sliding space is used to control both I_f and V_{cap} with $\lambda = 1100$.

The simulation was run for 400ms (20 cycles of 50Hz source)
The last 50% of the output was analysed for harmonic content using freqplot3.m (i.e. once initial transients have settled).
The following plot shows the resulting spectrum for Simulation Set 1b:

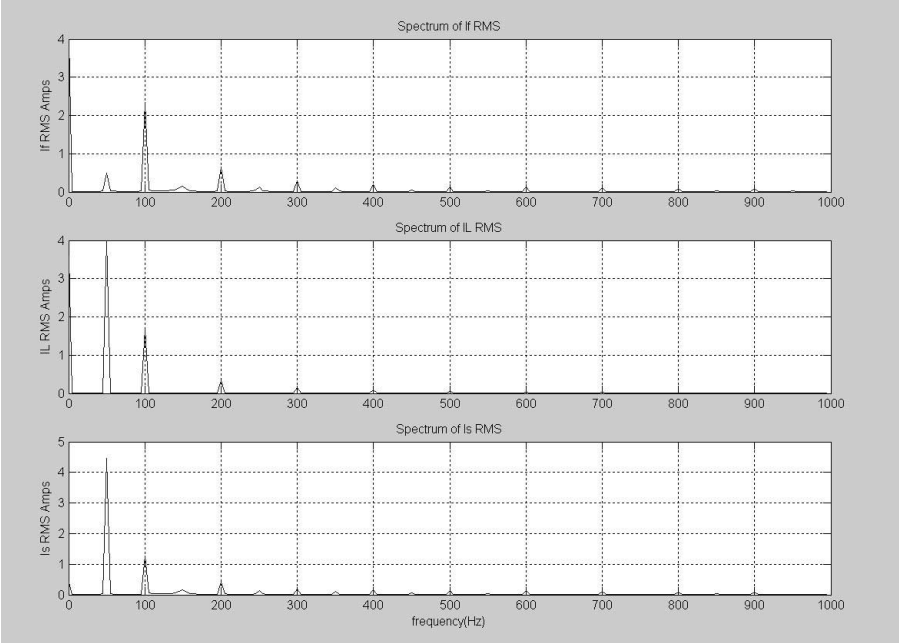


Fig 3.28: *Spectrum of If, IL and Is up to 1kHz for Result Set 1b*

The Total harmonic results for Simulation Set 1b are as follows:

- THD of I_L = 0.43747
- THD of I_s = 0.31799
- Total harmonic current for IL = 1.7425 A RMS
- Total harmonic current for Is = 1.4211 A RMS
- THD of Vs = 0.0070557
- Total harmonic Voltage = 1.6934 V RMS (for R= 0.25 Ohm, L = 796 μH)

It can be seen that the peak of I_{sref} is approximately 5.7 Amps as expected from the Fourier harmonic analysis shown in section 3.13.3.1. Current I_s attempts to follow this reference, however distortion occurs since a reference is being imposed onto the capacitor Voltage via the sliding control surface thereby preventing the capacitor Voltage from settling quickly to a stable value. The long settling time can be seen from the K plot where convergence to the ideal 0.0166 Mho for this case is taking the whole simulation time. Since bandwidth is being shared between I_f and V_{cap} correction then a longer settling time would be expected. To understand these effects in more detail requires further analysis from a different perspective. This analysis will be dealt with later.

The results indicate that an improvement in THD but only from 44% to 32%. The fundamental of IL (3.98 A) is very close to that of Is (4.47 A) and the If fundamental

is fairly small (0.49A) indicating that the source is providing the real power and not the APF (i.e. as required). This system is not as effective as system 1a where $\lambda = 0$..

3.13.4 Results Simulation set 2a and 2b

The two result sets 2a and 2b have the same load but 2a uses zero mode switching ($\lambda = 0$) and 2b uses 1st-order ($\lambda > 0$) discrete sliding space switching.
For both simulation sets 2a and 2b the control algorithm switch_control3a.m (Appendix D) is used.

3.13.4.1 Non-Linear load used for Simulation Set 2a and 2b

The non-linear load circuit is given in Appendix C "non-linear load".
It is set up as given in Table 3.6 – non-linear load 2.
The non-linear load conditions are repeated here:

- Full diode bridge connected
- Inductor = 1mH
- cload in circuit = 80μF
- Rload switched1 left open
- Rload = 30 Ohm

3.13.4.2 Simulation Set 2a

See Results in Appendix F: Result set 2a

A zero order switching space used ($\lambda = 0$). Once the capacitor has reached 500V the capacitor is no longer forced by a control system to any particular Voltage, the capacitor settles at a Voltage where the energy change per source cycle is zero.

The simulation was run for 400ms (20 cycles of 50Hz source)
The last 50% of the output was analysed for harmonic content using freqplot3.m (i.e. once initial transients have settled).

The following plot shows the resulting spectrum for Simulation Set 2a:

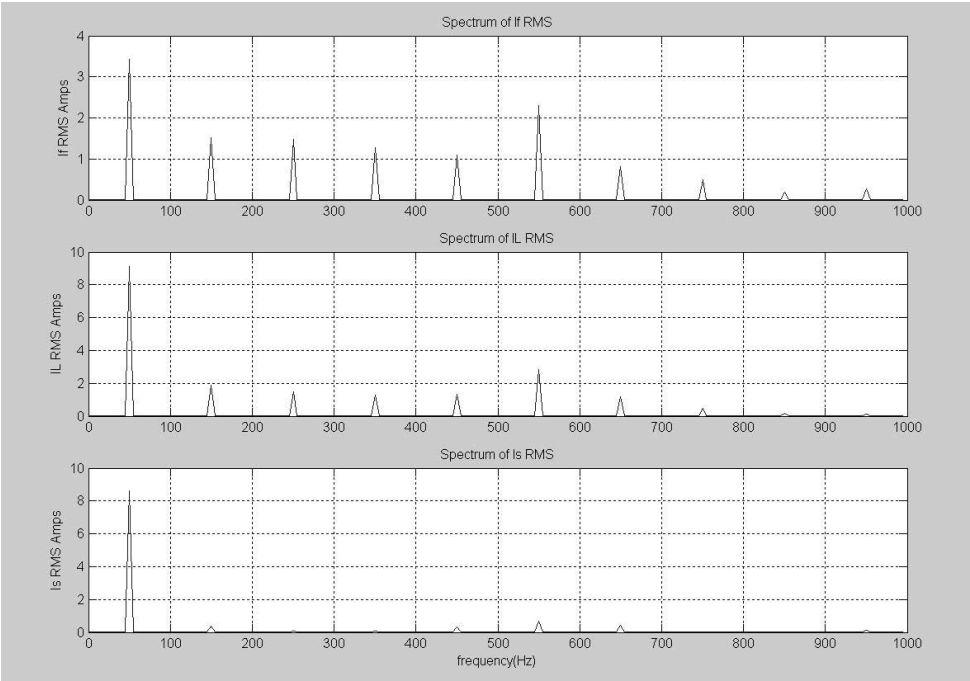


Fig 3.29: *Spectrum of If, IL and Is up to 1kHz for Simulation Set 2a*

The Total harmonic results for Simulation Set 2a are as follows:

- THD for I_L = 0.4771
- THD for I_s = 0.1197
- Total harmonic current for IL = 4.3592 A RMS
- Total harmonic current for Is = 1.0338 A RMS
- THD of Vs = 0.0152
- Total harmonic Voltage = 3.6375 V RMS (for R= 0.25 Ohm, L = 796 μH)

The results for set 2a indicate a considerable improvement in THD from 48% to 12% with significant reductions of Is in the odd harmonics. The Total Harmonic Voltage is however fairly close to the calculated limit of 4.23 V (section 2.2).

3.13.4.3 Simulation set 2b

See Results in Appendix F: Result set 2b

1st order discrete sliding space used to control both I_f and V_{cap} (with $\lambda = 1100$).

The simulation was run for 400ms (20 cycles of 50Hz source)
The last 50% of the output was analysed for harmonic content using freqplot3.m (i.e. once initial transients have settled).
The following plot shows the resulting spectrum for Simulation Set 2b:

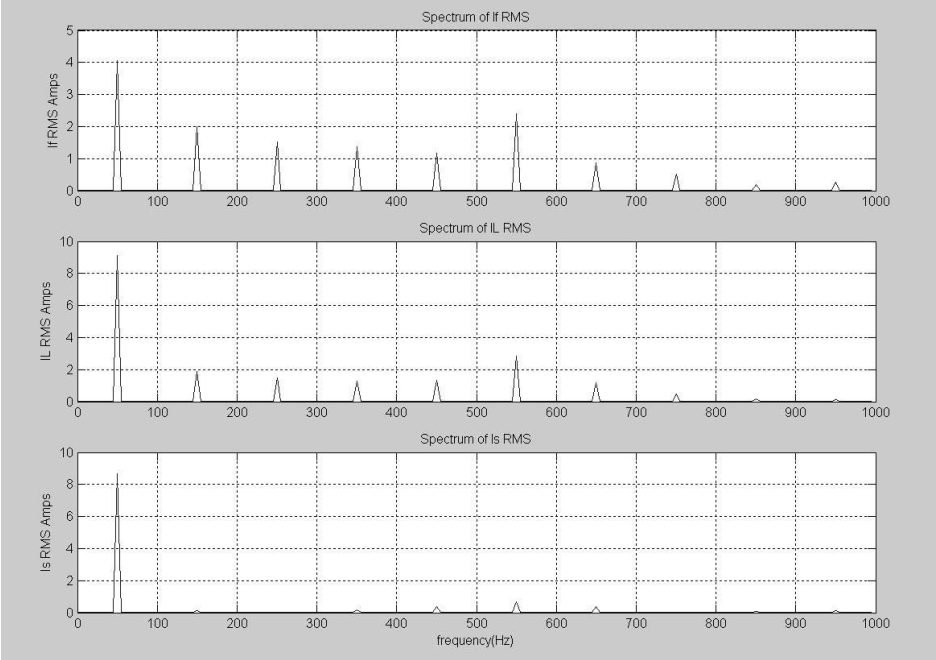


Fig 3.30: *Spectrum of If, Il and Is up to 1kHz for Simulation Set 2b*

The Total harmonic results for Simulation Set 2b are as follows:

- THD for $I_{L=}$ 0.47708
- THD for I_s = 0.10857
- Total harmonic current for IL = 4.3592 A RMS
- Total harmonic current for Is = 0.9415 A RMS
- THD of Vs = 0.012858
- Total harmonic Voltage = 3.086 V RMS (for R= 0.25 Ohm, L = 796 μH)

The results indicate an improvement in the THD from 48% to 11% with significant reduction in odd harmonic levels. The improvement of THD of result set 2b over result set 2a is due to the fact that the capacitor Voltage is higher (compare average value of V_{cap} of result set 2a = 535V with that of result set 2b of 550V). A higher V_{cap} gives a higher system bandwidth and hence an enhanced ability to suppress reactive currents.

3.13.5 Simulation set 3a and 3b

The two result sets 3a and 3b have the same load but 3a uses zero mode switching ($\lambda = 0$) and 3b uses 1^{st}-order ($\lambda > 0$) discrete sliding space switching.
For both simulation sets 3a and 3b the control algorithm switch_control3a.m (Appendix D) is used.

3.13.5.1 Non-Linear load used for Simulation Set 3a and 3b

The non-linear load circuit is given in Appendix C "non-linear load".

It is set up as given in Table 3.5 – non-linear load 3.

The non-linear load conditions are repeated here:

- Full diode bridge connected
- Inductor = 35mH
- cload in circuit = 40μF
- Rload switched1 of 30 Ohm in circuit
- Rload open

The load consists of a capacitively loaded full wave bridge rectifier which in turn is loaded by a resistor of 30 Ohm. This resistor is periodically switched into circuit for 2.5ms and removed for 2.5ms. The whole load is connected via a 35mH inductor which adds some resonance.

3.13.5.2 Simulation 3a

See Results in Appendix F: Result Set 3a

Zero order switching space used ($\lambda = 0$). No forced capacitor Voltage reference.

The Simulation was run for 400ms (20 cycles of 50Hz source)

The last 50% of the output was analysed for harmonic content using freqplot3.m (i.e. once initial transients have settled).

The following plot shows the resulting spectrum for Simulation Set 3a:

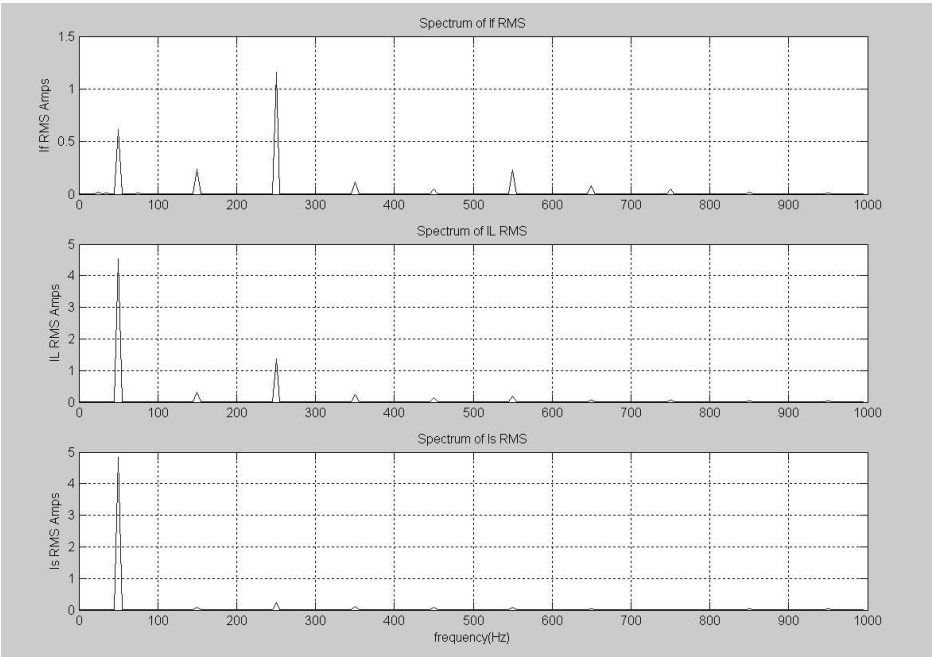


Fig 3.31: *Spectrum of If, IL and Is up to 1kHz for Result Set 3a*

The Total harmonic results for Simulation Set 3a are as follows:

- THD for I_L = 0.32078
- THD for I_s = 0.065851
- Total harmonic current for IL = 1.4551A RMS
- Total harmonic current for Is = 0.3191 A RMS
- THD of Vs = 0.0031813
- Total harmonic Voltage = 0.76352 V RMS (for R= 0.25 Ohm, L = 796 μH)

The results indicate a considerable improvement in THD from 32% to 6.6%, with a major improvement of the 5th harmonic. The calculated total harmonic Voltage is significantly lower than the worst case level of 4.23V (section 2.2)

3.13.5.3 Simulation set 3b

See Results in Appendix F: Result Set 3b

1st-order discrete sliding space used to control both I_f and V_{cap} (λ = 1100).

The simulation was run for 400ms (20 cycles of 50Hz source)
The last 50% of the output was analysed for harmonic content using freqplot3.m (i.e. once initial transients have settled).
The following plot shows the resulting spectrum for Simulation Set 3b:

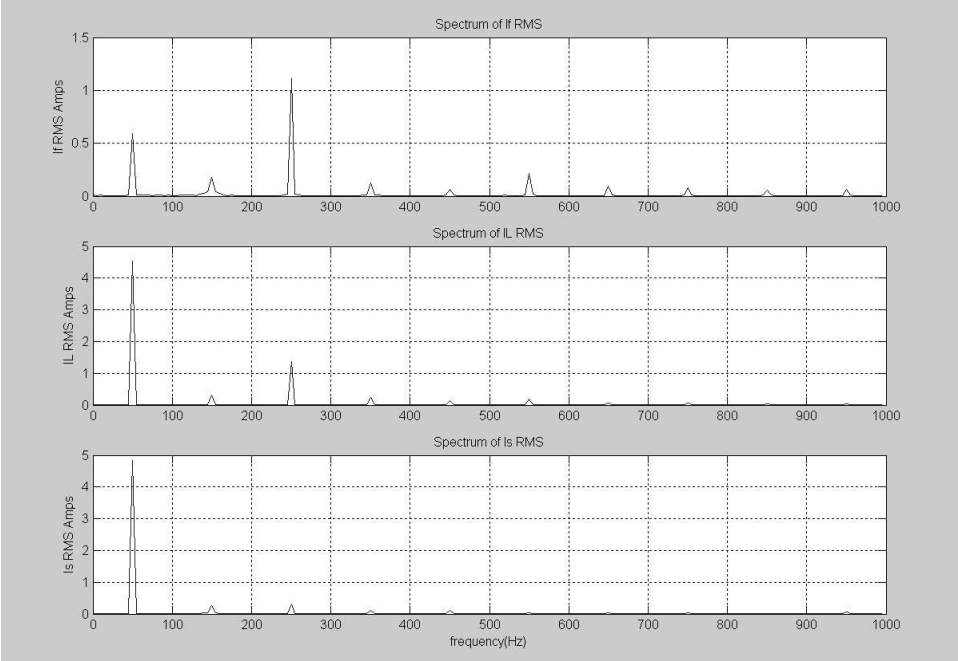


Fig 3.32: *Spectrum of If, IL and Is up to 1kHz for Result Set 3b*

The Total harmonic results for Simulation Set 3b are as follows:

- THD for I_L = 0.32074
- THD for I_s = 0.095965
- Total harmonic current for IL = 1.4553 A RMS
- Total harmonic current for Is = 0.46358 A RMS
- THD of Vs = 0.0041065
- Total harmonic Voltage = 0.98557 V RMS (for R= 0.25 Ohm, L = 796 μH)

The APF has made the fundamental of Is and IL almost the same (4.54 A and 4.83A respectively) and there is considerable improvement in THD from 32% to 9.6% . The performance indication of result set 3b is slightly worse than that of result set 3a. Comparing the average value of V_{cap} of result set 3a (580V) with that of result set 3b (550V) indicates that the higher V_{cap} then the better the APF's ability to suppress unwanted harmonics of the load by increasing the system bandwidth. The total harmonic Voltage is within the calculated limits of section 2.2.

3.13.6 Conclusion of results of section 3.13.3 to 3.13.5

It is evident that zero order switching where only I_f (and hence I_s) is controlled, allowing the capacitor to "float" to a value determined only by energy balance per source cycle and initial conditions, give consistently good Total harmonic results. These systems are presented for theoretical purposes only. An uncontrolled capacitor Voltage would not be acceptable in a practical system since it could easily float to a level above its rated maximum working Voltage and could cause damage to the bridge transistors. Conversely it could float to a level too low to maintain a fast enough $\dot{I}_f(t)$. The 1st-order DSM control achieves the objectives of controlling two state variables (I_f and V_{cap}). The reference level chosen for the capacitor Voltage must be high enough to maintain adequate bandwidth for harmonic suppression and hence THD reduction. Higher capacitor Voltage tends towards a better THD performance.
In general, the THD levels are worse with 1st-order DSM compared to zero-order control.

It can be seen from the K traces for result sets 1b, 2b and 3b that a major problem with first order DSM appears to be the time taken for K to stabilise which will affect transient recovery times. It will be shown in section 4.3.5 that the proposed 1st order

DSM results in "outer loop" instability (see definition of loops in section 4.3). This has a detrimental effect on the "inner loop" which is the reason for increased K settling time.
In summary:
The use of the 1st-order DSM will control both filter current and capacitor Voltage but at a price:

- Slow conversion to a steady K value and hence steady working conditions
- Distribution of available bandwidth between two variables and therefore slightly higher errors in both variables
- Performance dependent on choice of λ

The dependence of a 1st order DSM system on λ requires more investigation. It has been shown that for very small λ the system reverts to zero order and there is no control of V_{cap} and conversely for large λ the error in I_f could become unacceptable.

Additional work was carried out (which is not reported in this thesis) to investigate a possible hybrid solution. An APF design was considered that used zero-order switching space and reverted to 1st order switching space if the capacitor Voltage were to deviate from a given preset level. After much work this technique was rejected. Essentially lambda would be switched between zero and a non-zero value, causing transient shifts in the current reference. Such shifts in the current reference had a significant detrimental effect on the APF's THD performance.
The Sliding Control method imposes control of the capacitor Voltage and hence influences the effectiveness of the energy calculation used to obtain K (eqn 3.32). The effect of sliding control of the capacitor Voltage on the overall system response has yet to be investigated. This is a very important area and will be subject for much discussion in chapter 4 using the principles of the flow of Real Power.

3.14 Study and comparison of results with existing methods

It is the intention of this section to review existing methods of APF control and compare the results to those already obtained from simulation. There is currently a vast array of techniques as can be seen from the references and bibliography sections of this thesis. Existing sliding techniques ([5.2], [5.3], [5.6]) are highly relevant to the methods used here and will be used as the starting point for investigation. It is also

apparent that the use of low-pass smoothing filters and a PI controller ([4.1], [4.2], [4.3], [4.4], [5.2], [5.3], [5.6]) is also made. Since these linear functions have significant impact on dynamic performance a section of this work is devoted their study. In addition to evaluating the system in the steady state, it is very important to investigate the transient recovery time following a load change. Therefore this section will run simulations involving step changes in load so that a full comparison of control techniques can be made. A quicker recovery time allows the APF system to harmonically correct quickly changing non-linear loads. It is not unreasonable to expect an APF to establish steady state conditions of both input conductance and capacitor Voltage following a load change after 3 to 4 cycles of the source. Most APF designs based on a linear feedback technique would violate the principle of source current harmonic elimination during the transient response. The system proposed here maintains resistive synthesis even during the transient phase (see section 3.10) since sampling and K update takes place at the zero crossing point of the source. This is an important consideration for rapidly changing loads e.g. loads changing every 200ms, where the transient response is about 30 to 40% of the load period.

3.14.1 The PI controller

An example system using a PI controller is shown in fig 3.33. The integral part of the PI control block can be interpreted as the means of obtaining K (the ideal input conductance) from the capacitor error Voltage. It has been shown in eqn {3.35} that K is obtained in the discrete system using an accumulative function and therefore in the linear system an integral function would be appropriate. However, eqn {3.35} accumulates an energy function rather than a Voltage function. The energy function can be seen from eqn {3.32} to be non-linear. If the sliding controller of fig 3.33 is removed the system reduces to the basic controller as presented in ref [4.3]. Ref [4.3] linearises the system by assuming that the deviation in capacitor Voltage is small so that a linear transfer function for the system can be assumed. If the same assumption is made here then by re-writing eqn {3.32}:

$$\Delta E = \frac{1}{2} C\left(V_{capnew} - V_{capold}\right)\left(V_{capnew} + V_{capold}\right)$$

Assuming that there is little movement of the capacitor Voltage then the following assumption is made:

$$V_{capave} \approx \frac{1}{2}\left(V_{capnew} + V_{capold}\right) \quad \text{-----\{eqn 3.67\}}$$

Therefore the energy function becomes:

$$\Delta E \approx V_{capave} C\left(V_{capnew} - V_{capold}\right) \quad \text{-----\{eqn 3.68\}}$$

Provided V_{capave} remains steady and close to the desired level $V_{capaconst}$ then a linearised energy function can be written:

$$\Delta E \approx V_{capconst} C\left(V_{capnew} - V_{capold}\right) \quad \text{-----\{eqn 3.69\}}$$

i.e. ΔE is now a proportional to the changes in capacitor Voltage.

Furthermore, V_{capold} can be replaced by V_{capref} so that the energy function is dependent on the error Voltage:

$$\Delta E \approx V_{capconst} C\left(V_{capnew} - V_{capref}\right) \quad \text{-----\{eqn 3.70\}}$$

Fig 3.33 shows that the capacitor Voltage is passed through a low pass filter. This is normal practice in linear systems. The low pass filter prevents large swings of capacitor Voltage entering the control system by smoothing the capacitor Voltage presented to the PI controller which aids the approximation necessary for eqn {3.70} to hold. The time constant of the low pass filter must therefore be long enough to effectively reduce the fundamental component (50Hz component) present in V_{cap}.

The discrete system method of updating K implies that K will always depend on the *change* in capacitor Voltage (and hence change in energy) in the *previous* cycle and K is therefore always delayed by one cycle of the source.
Linear systems employing the PI controller will similarly introduce a delay into the K signal path due to the integrator and this delay must be of at least one cycle (for a practical design it will be several cycles) in order to have a break point low enough to remove the fundamental component from the capacitor Voltage wave.
The discrete system method does not require a low pass filter to filter V_{cap}. For a steady load, all APF currents are periodic and multiples of the fundamental frequency. A periodic sampler (synchronised to the mains waveform) will always sample the same point (and hence the same Voltage) from the V_{cap} waveform.
When the load changes and the average energy changes in the capacitor, the change in the sampled Voltage allows the energy change to be calculated (i.e. the actual measuring point on the V_{cap} wave is irrelevant since it is the change that matters when

evaluating ΔE in eqn {3.32}). The discrete system must not have any significant delay in the V_{cap} sampling path since this will cause a small instability in that the capacitor Voltage will "hunt" about the reference.

3.14.2 A study of existing sliding control methods and linear control methods

Reference [5.4] is used for preliminary investigation.
In this section variable designations are taken from the reference.
Refer to fig 3.33 for a system block diagram.

The same approach is used as in this thesis by setting the source reference current to be proportional to the source Voltage:

$$i_{sref} = \frac{v_s}{R_{eq}} \text{ where } \frac{1}{R_{eq}} = K \text{ = ideal input conductance (as used in this thesis)}$$

The sliding surface is created as a second order surface by forming the input power, its integral and the second integral as follows:

$$S = (i_s - i_{sref})v_s + \lambda_i \int v_s (i_s - i_{sref})dt + \lambda_0 \int\int v_s (i_s - i_{sref})dt$$

$$S = \left(i_s - \frac{v_s}{R_{eq}}\right)v_s + \lambda_i \int v_s \left(i_s - \frac{v_s}{R_{eq}}\right)dt + \lambda_0 \int\int v_s \left(i_s - \frac{v_s}{R_{eq}}\right)dt$$

The sliding equation is intended to force the APF energy function to behave in a linear fashion and satisfy a second order differential equation.
Note that the integral terms are synthesised directly and not obtained from actual system measurements. Conversely this thesis uses the bridge energy storage capacitor as the integrator by using the capacitor Voltage as a state variable.

Although the integral is synthesised it does not alter the fact that switching about the sliding surface will affect the capacitor Voltage which is being used as the sensor to correct K.
The following equation relates the source Voltage (v_s) to the capacitor Voltage (v_f):

$\frac{v_f}{v_s} = \frac{1}{\langle u \rangle}$ where $\langle u \rangle$ is the average of the switching variable (u = 0 or 1). This equation assumes that the H-bridge converter has the same behaviour as a boost converter.

Compare $\langle u \rangle$ from the referenced paper with eqn{3.56} of this thesis: $\beta_{eq} = \frac{|V_s(t)|}{V_{cap}(t)}$ where β_{eq} takes the place of $\langle u \rangle$.

It follows that $i_{sref} = \frac{v_f \langle u \rangle}{R_{eq}}$

However it should be noted that this result is only obtained when the system errors are zero (i.e. when steady state is reached).

The following block diagram is taken from the referenced paper:

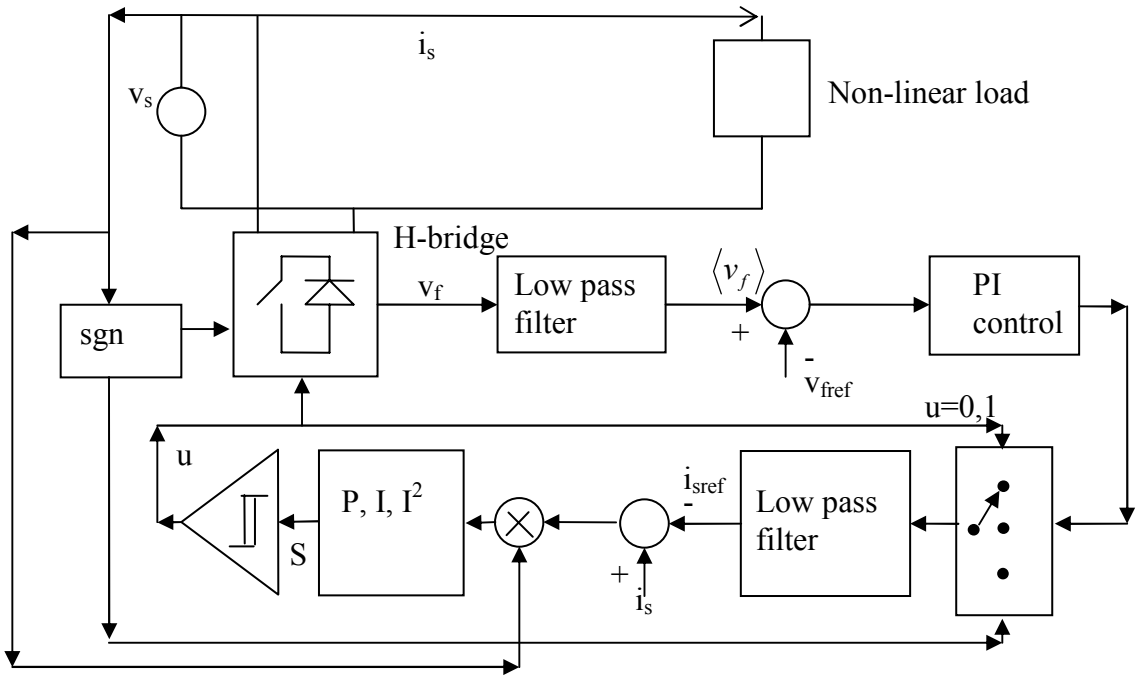


Fig 3.33*: Example APF system using a PI and sliding mode controller*

The capacitor Voltage (v_f) is averaged by the low pass filter to give $\langle v_f \rangle$. The capacitor reference is a d.c. value of v_{fref}. The capacitor error Voltage is passed through a PI controller and then multiplied by the average value of u to give i_{sref}.

$i_{sref} = \langle u \rangle \left(k_p \left(\langle v_f \rangle - v_{fref} \right) + k_i \int \left(\langle v_f \rangle - v_{fref} \right) dt \right)$ where k_i and k_p are constants of the PI.

It follows that

$$\frac{1}{R_{eq}} = \frac{\left(k_p\left(\left\langle v_f \right\rangle - v_{fref}\right) + k_i \int \left(\left\langle v_f \right\rangle - v_{fref}\right) dt\right)}{v_f}$$

The integrator in this equation is the analogue equivalent of the recursive function used in this thesis (eqn {3.35}) (see discussion section 3.14.1).

The discrete method used in this thesis requires a time dependent tracking capacitor reference (see fig 3.20). Linear systems avoid the problem of deriving a capacitor reference as a function of time by using the filtered and delayed average value capacitor Voltage $\left\langle v_f \right\rangle$ when then a simple dc value can be used as the capacitor reference.

The following table compares key differences between the methods used in this thesis and the referenced paper:

Referenced paper methods	**Methods used in this thesis**
Entirely an analogue method	Discrete step method
Average capacitor Voltage used; obtained with long low pass filter introducing a delay	Time dependent capacitor tracking reference derived by integrating the APF reference current directly
Sliding surface of 2nd order derived from synthesising the integrals of the APF power function	Sliding surface of 1st order derived using actual measured parameters
Input ideal resistance derived continuously using the PI function	Input conductance derived discretely every period of the source giving a smooth source reference current

Table 3.7: *Comparing the analogue methods of reference [5.4] with the discrete methods developed in chapter 3*

If the sliding mode controller is removed from fig 3.33 and the bridge drive is replaced with a PWM drive circuit, the system reduces to that of fig 3.34. Fig 3.34 is a generic linear APF based on the work in ref [4.3]:

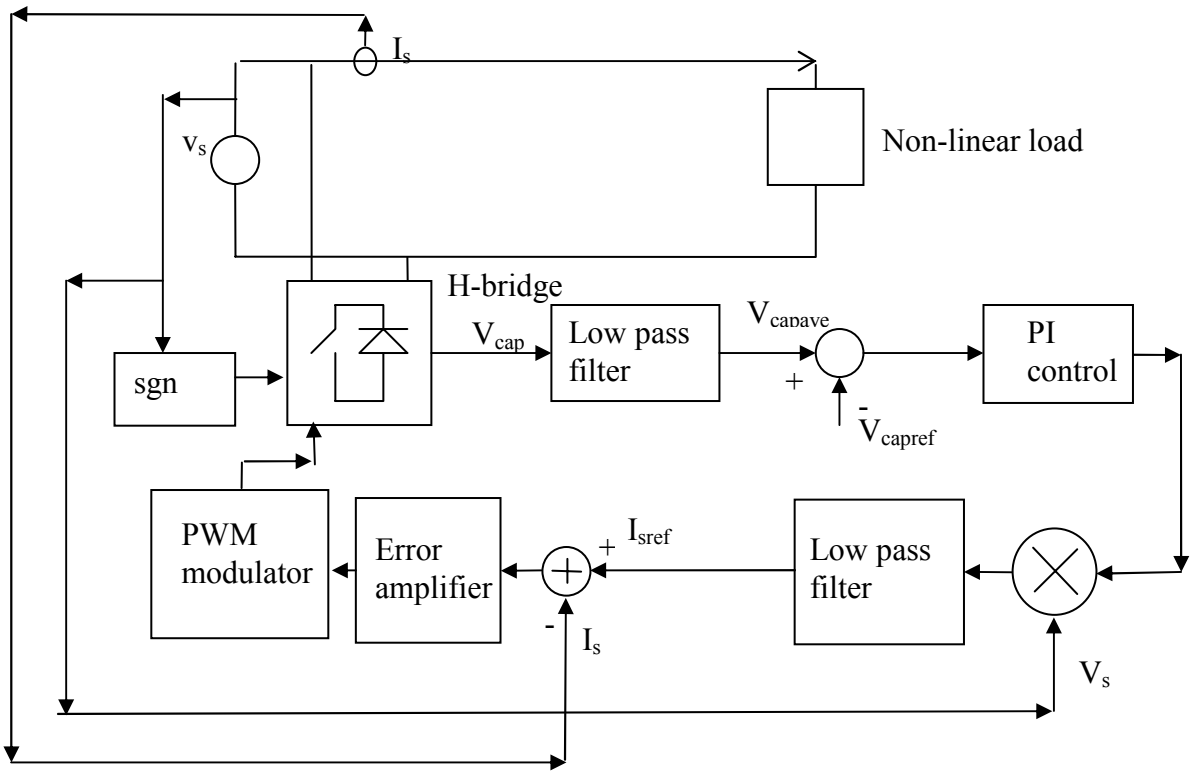


Fig 3.34: *Linear APF control incorporating a PI controller*

The output from the PI controller (assumed proportional to K) is multiplied by Vs to obtain K directly rather than using a signal $\langle u \rangle$ derived from the bridge driving function. The systems outlined in figs 3.33 and 3.34 will be simulated in the following section.

3.14.3 Simulation of APF methods incorporating a PI controller

In order to remain compatible with the APF model described in section 3.12 it was decided to retain the Active/Passive method of driving the H-bridge and retain the digital sampling approach based on the simulation sampling time T=20μs. Therefore all integrators and low pass filters have been described in their z-domain form. Rather than using the PWM approach of fig 3.34, the same techniques are used here as in the model used in section 3.12 but now driven from a new S function derived from the sliding space part of the model and as shown in fig 3.33.

The following block diagram is an overview of the system to be used for simulation to assess the performance of the techniques encompassed by the linear PI controller approach with or without a sliding controller:

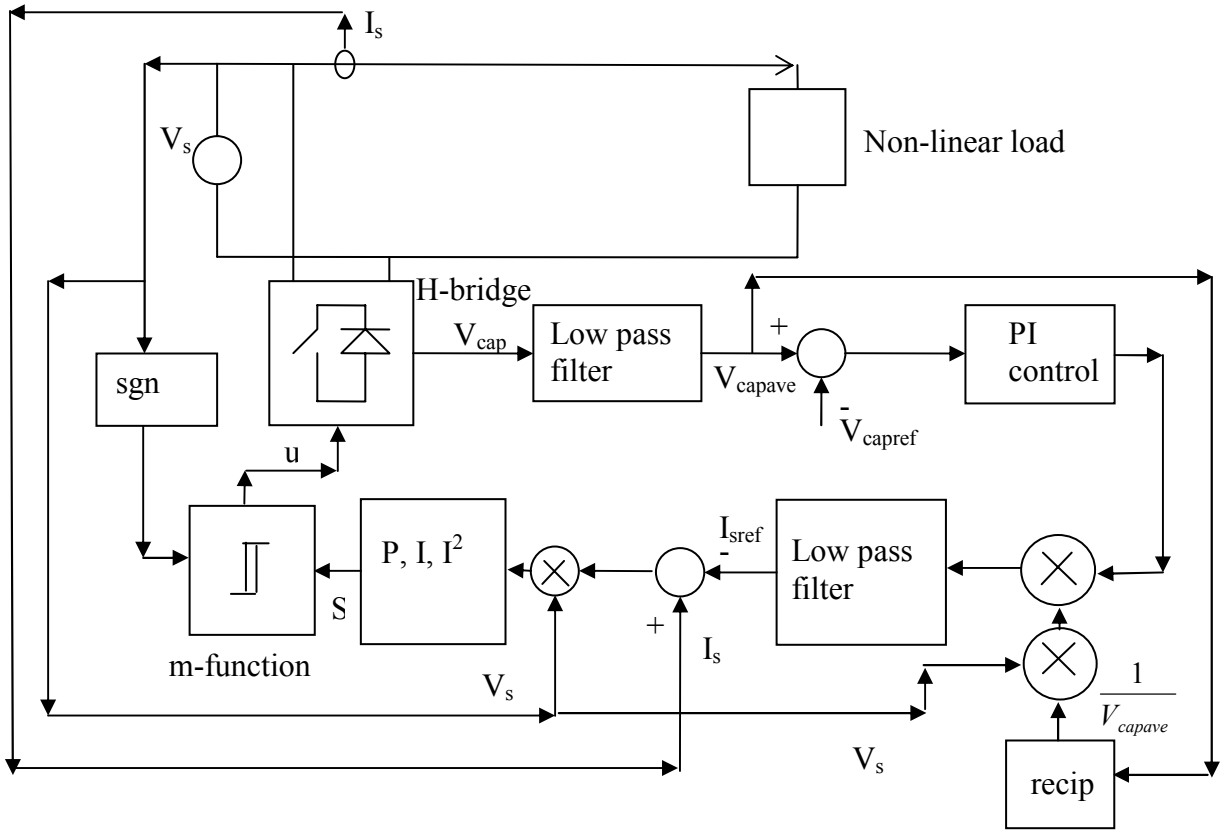


Fig 3.35: *Block diagram of the system used for simulation with PI controller*

The system of fig 3.33 multiplies the output of the PI controller by $\langle u \rangle$ and in order to simulate this effect, fig 3.35 multiplies the output of the PI controller by the equivalent function: V_s/V_{capave}.

3.14.3.1 Matlab simulation of fig 3.36

The complete system diagrams for the Matlab model using Simulink and Sim-Power-System toolbox is similar to the model already descried in section 3.12 and given in Appendix C. For clarity, the new complete model is given in Appendix G and the switching m-file control algorithm (referenced as switch_control6.m) is given in Appendix H. The m – function of Appendix E (freqplot3.m) (with minor alterations) was used to frequency analyse the last 200ms of the current arrays and obtain total harmonic results.

3.14.3.2 Simulation parameters

The control parameters are mainly taken from ref [5.4] and are as follows:

- V_s set to 120V peak at 50Hz
- V_{capref} = 350V
- Bridge capacitor = 1300μF
- Bridge sampling time = 20μs giving a maximum switching frequency of 25kHz (period = 2T).

Reference [5.4] sets the bridge input inductor at 1.8mH which would require a much higher switching speed; therefore the input inductor has been set to the levels used in section 3.12

- Therefore bridge input inductor = 21mH.
- PI proportional control value = - 0.1
- PI integral control value = -1
- Cut off frequency for both low-pass filters = 86Hz
- Sliding function proportional element coefficient = 1
- Sliding function integral element coefficient (λ_i) = 15000
- Sliding function double integral element coefficient (λ_0) = 200

3.14.3.3 Low pass filters and integrators

The low pass filters used in the Matlab simulation (Appendix G) are expressed in Z domain as follows:

$\frac{540Tz}{z-e^{-540T}}$ where 540 = 2*π*86 rad/s

The integrators used are given in Z domain as:

$\frac{T}{Z-1}$

3.14.3.4 Load and simulation parameters

The non-linear load was arranged as a half wave rectifier feeding two resistors in parallel. One resistor was set to 30 Ohms and permanently connected and the other was a 30 Ohm resistor which was switched into circuit at 0.5secs from start up and switched out at 0.8secs from start-up.

The simulation was run for 1.5secs to enable the system long enough to find a steady working state and then to observe the system's transient response.

3.14.3.5 Results of simulation for system block diagram 3.35

Using the sliding mode controller together with a PI controller and averaging filters

Thorough investigation led to the conclusion that the system proposed in fig 3.35 using an integral and double integral term in the formation of the sliding function would not allow convergence to a meaningful solution. The reason for this was found to be due to the fact that integral terms store the residual area under the function that they are integrating and therefore would require extra filters to deal with these unwanted values. Note that a similar problem arose in section 3.6.5 in the derivation of the capacitor reference when additional filters had to be used to remove unwanted integral terms (see diagram 3.20).

Using the PI controller only with averaging filters

The simulation parameters used in the block diagram of fig 3.35 were modified by setting the integral and double integral coefficients in the formation of S to zero and thereby reducing the sliding function to zero order. This reduces the system to a "generic" low pass filter as proposed in ref [4.3]. The results are as follows:

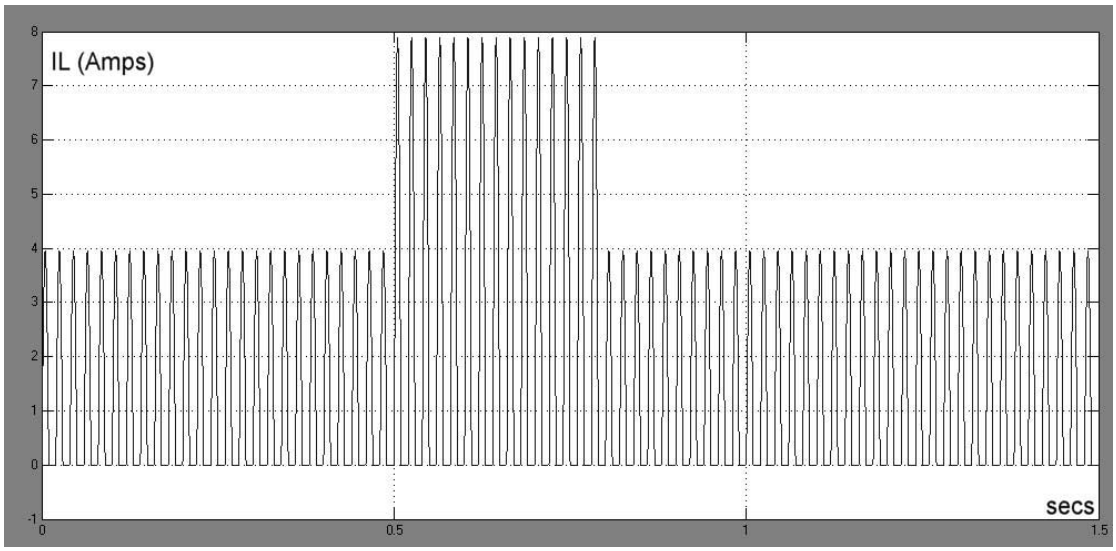


Fig 3.36: *Load current IL in simulation system using PI controller only*

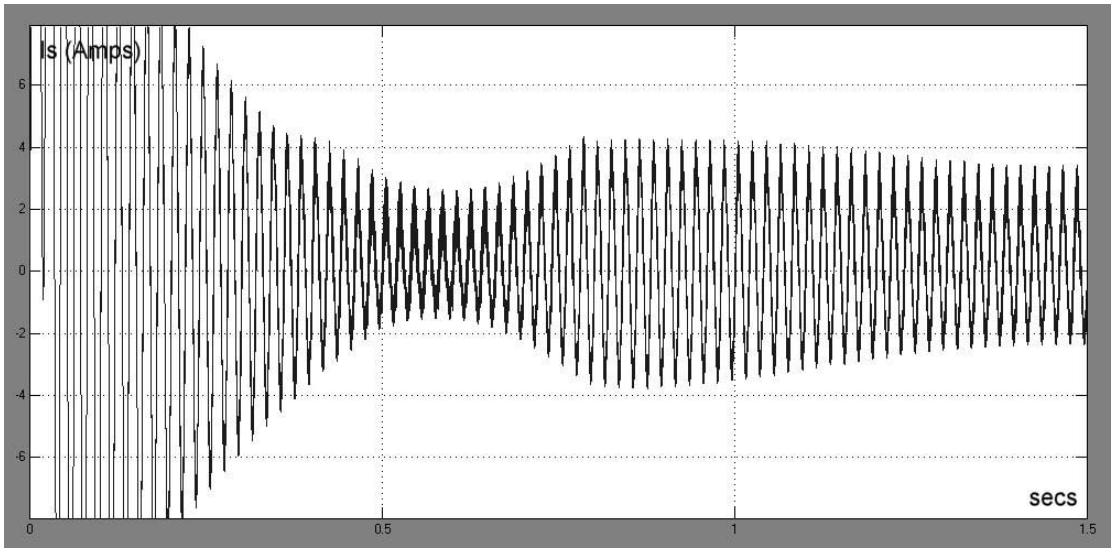


Fig 3.37: *Source Current Is in simulation system using PI controller only*

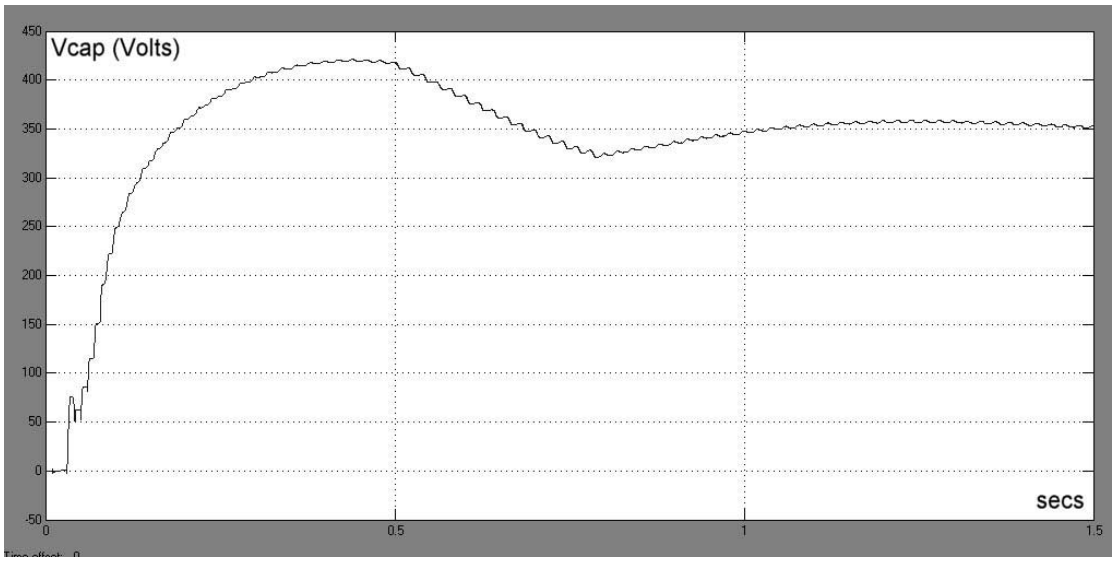


Fig 3.38 *Capacitor Voltage Vcap in simulation system using PI controller only*

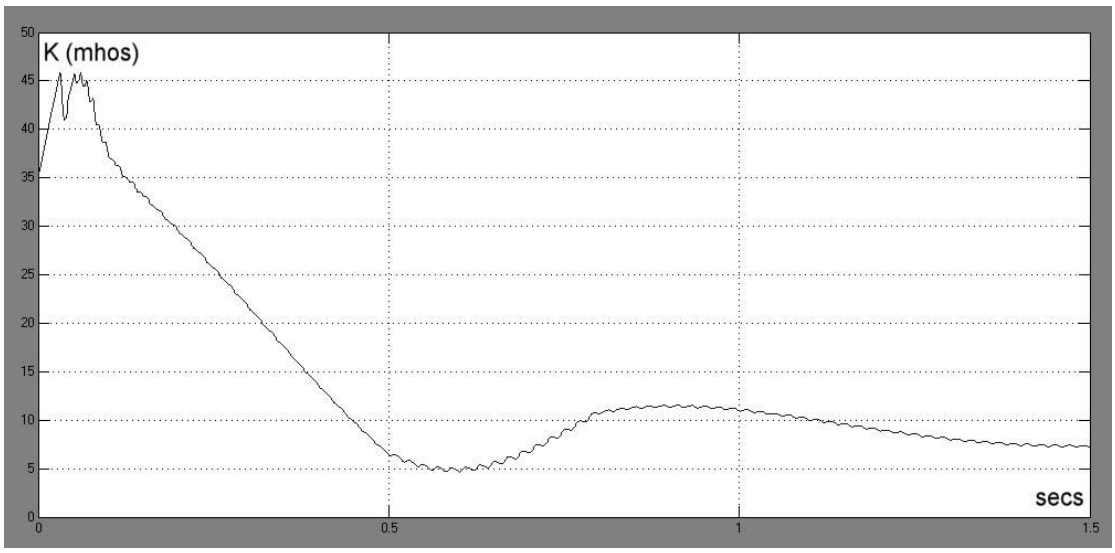


Fig 3.39: *Conductance K in simulation using PI controller only*

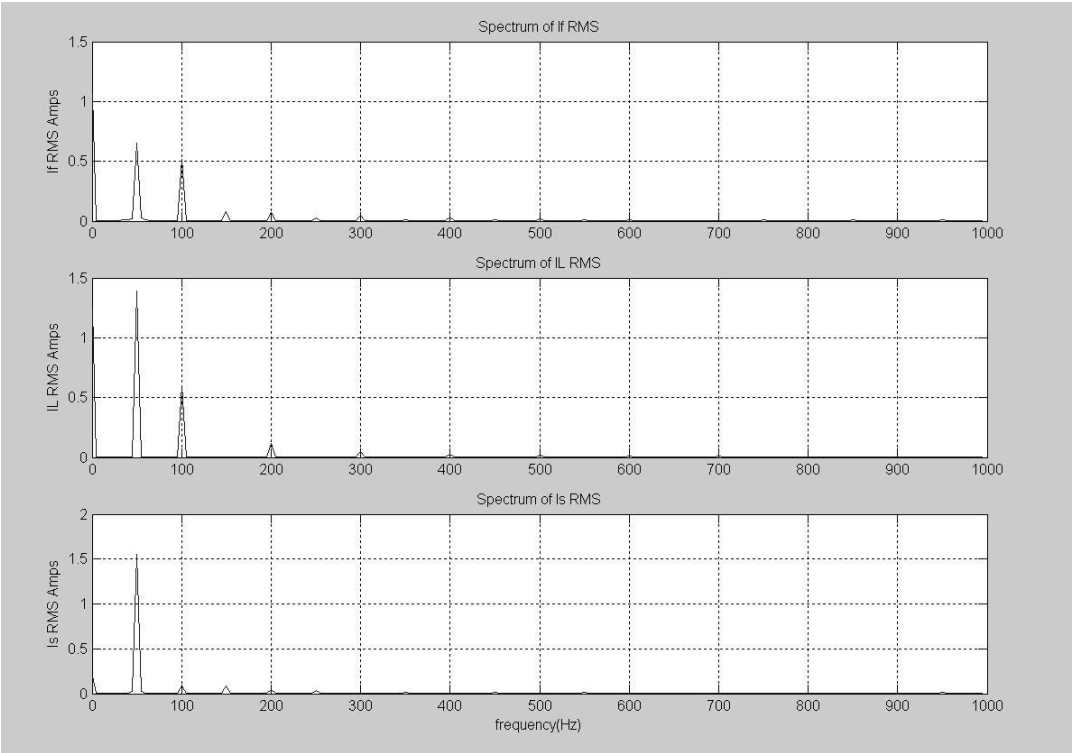


Fig 3.40: *Current frequency spectra for system using PI controller only*

Total harmonic results (for the last 200ms of the data):

- THD for IL = 0.4417
- THD for Is = 0.0888
- Total harmonic current for IL = 0.6149A RMS
- Total harmonic current for Is = 0.1374 A RMS
- Total harmonic source Voltage = 0.2407 V RMS
- THD source Voltage = 0.001 (based on the standard source impedance of R= 0.25Ohm and L = 796μH)

The results indicate a good improvement in THD (from 44% to 8.9%) and a Total harmonic Voltage less than the worst case (section 2.2). The transient response is slow – taking 800ms for the majority of the transient to die away. This is comparable to the results given in ref [5.4] indicating that the linear control circuit with no sliding integral terms is just as effective as the system with sliding control proposed in the referenced paper.

Note that the capacitor Voltage does eventually reach the set value V_{capref} = 350V.

3.14.3.6 Tuning the PI controller

The reason for the long transient result in section 3.15.2.5 is that the loop low pass filters act as integrators (since their time constants are relatively long to provide V_{cap} smoothing). Further integration in the loop is not required. Therefore the integral term

of the PI controller must be set to zero. It is then necessary to set the proportional term to a value that optimises the energy transfer to and from the capacitor following a load step change. Using the linearising approximations (section 3.14.1) it is possible to fine tune the PI controller and obtain a faster transient response.

The procedure:

- Remove the integral term form the PI controller and rely on the integral effects of the loop low pass filters
- Assume that the time-dependent value V_{capave} = the constant value $V_{capconst}$. (This is only true if V_{capdev} is small and the system has reached steady state).
- Using eqn {3.70} and eqn {3.35} determine the proportional coefficient of the PI controller

Examination of eqn {3.70} and eqn {3.35} the PI proportional coefficient is given by:

$$-\frac{V_{capref}C}{\tau V_{sRMS}^2}$$

Furthermore, to remain compatible with fig 3.35 (which was derived in part from ref [5.4]), where the output of the PI controller is multiplied by $1/V_{capref}$ then the PI proportional coefficient has to be scaled by V_{capref}.

Therefore:

PI proportional coefficient = $-\frac{V_{capref}^2 C}{\tau V_{sRMS}^2}$ -----{eqn 3.71}

To demonstrate the effectiveness of the fine tuning process, the values for the system based on that specified in section 3.14.3.2 were used.

- $V_{capref} = V_{capconst} = 350V$
- Bridge storage capacitor C = 1300μF
- V_s (peak) = 120V, V_{sRMS} = 84.85 V RMS
- τ = 20ms

Using eqn {3.71}: PI proportional coefficient = -1.106

The complete set of design parameters for simulation:

- V_s set to 120V peak at 50Hz
- V_{capref} = 350V
- Bridge sampling time = 20μs giving a maximum switching frequency of 25kHz (period = 2T).
- Bridge input inductor = 21mH.
- PI proportional control value = - 1.106
- PI integral control value = 0
- Cut off frequency for both low-pass filters = 86Hz
- Sliding function proportional element coefficient = 1
- Sliding function integral element coefficient (λ_i) = 0
- Sliding function double integral element coefficient (λ_0) = 0
- Load: half wave rectified 30 Ohm from 0 to 500ms, then half wave rectified 15 Ohm from 500 to 800 ms then half wave rectified 30 Ohm from 600ms to 1.5s

The Matlab model of Appendix G with the control algorithm of Appendix H gave the following results:

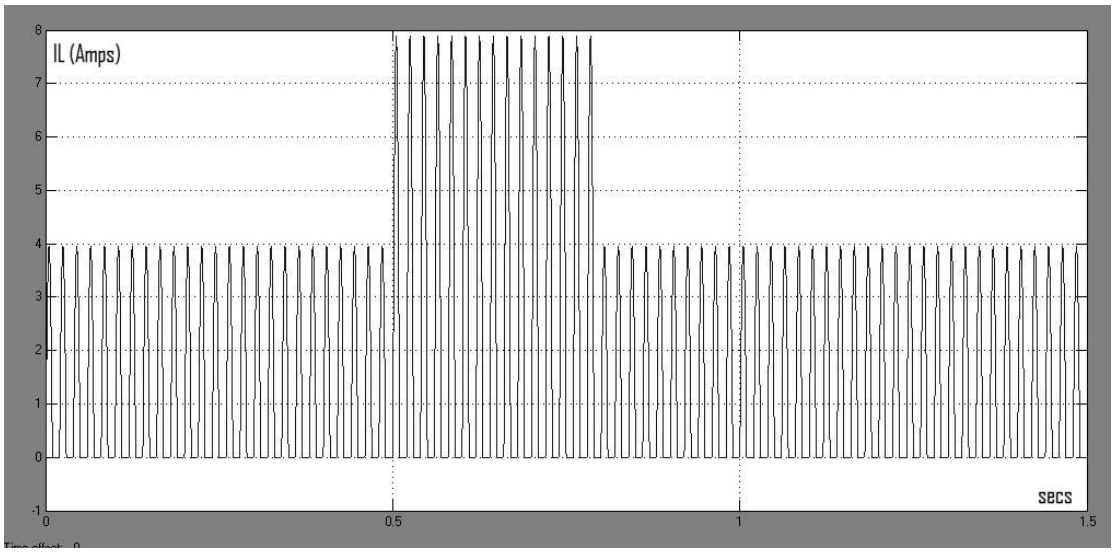


Fig 3.41: *Load current IL in simulation system using tuned PI controller only*

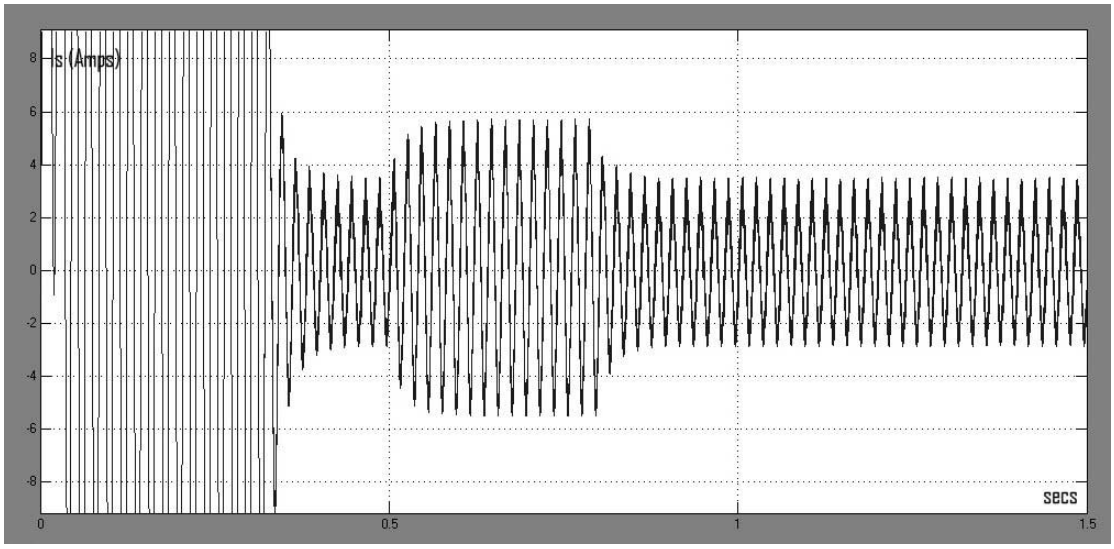


Fig 3.42: *Source Current Is in simulation system using tuned PI controller only*

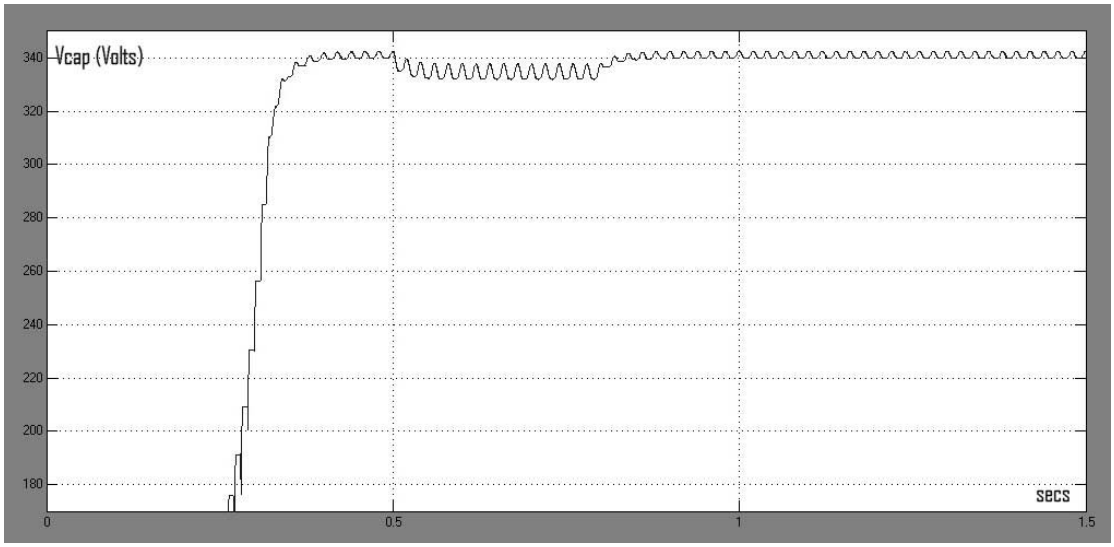


Fig 3.43: *Capacitor Voltage Vcap in simulation system using tuned PI controller only*

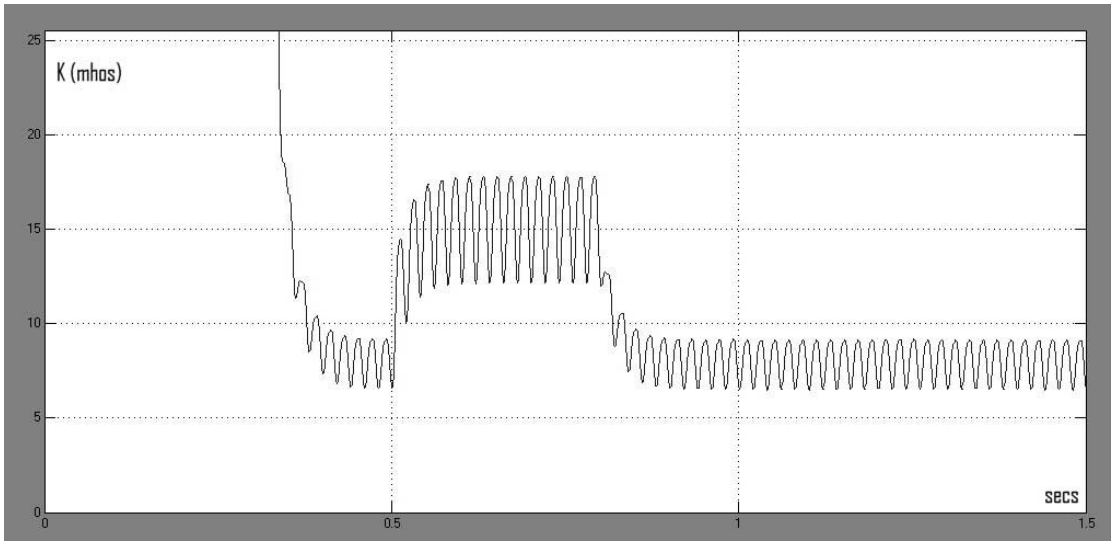


Fig 3.44: *Conductance K in simulation using tuned PI controller only*

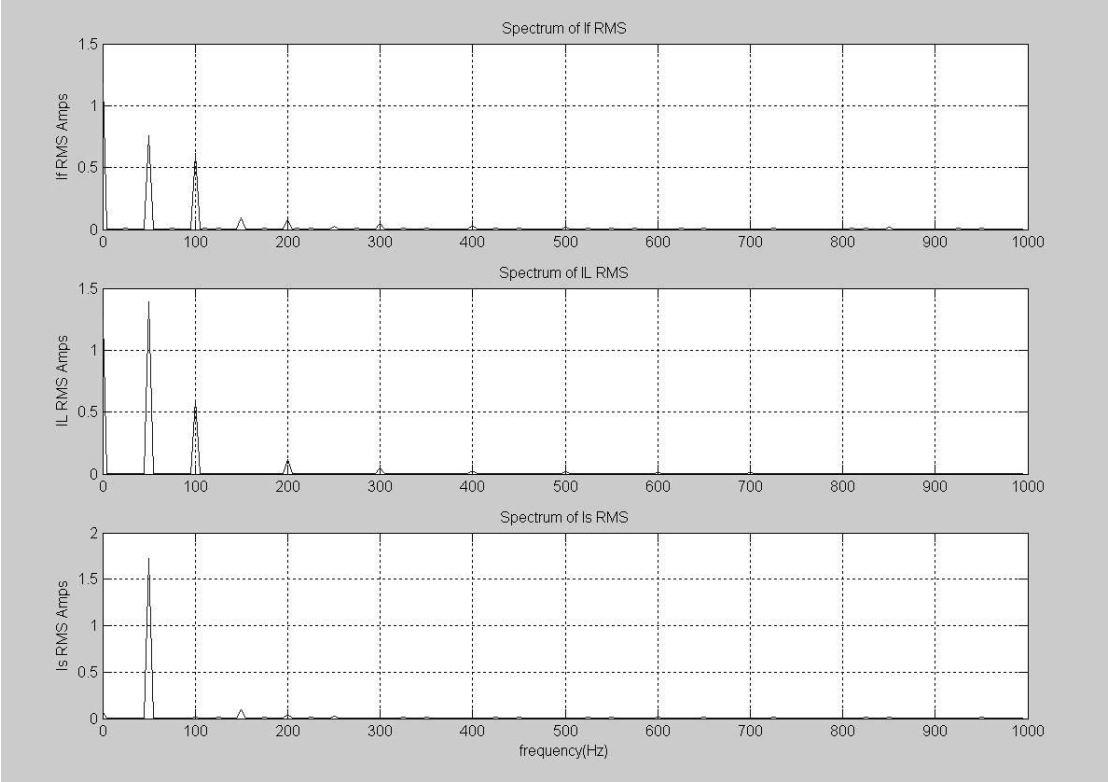


Fig 3.45: *Current frequency spectra for system using tuned PI controller only*

Total harmonic results (for the last 200ms of the data):

- THD for IL = 0.4417
- THD for Is = 0.072394
- Total harmonic current for IL = 0.6149A RMS
- Total harmonic current for Is = 0.12457 A RMS
- Total harmonic source Voltage = 0.29904 V RMS
- THD source Voltage = 0.00125 (based on the standard source impedance of R= 0.25Ohm and L = 796μH)

The results are very similar to those obtained in section 3.15.2.5 except that the transient response is now vastly improved; taking only 4 mains cycles for steady state to be achieved indicating that the tuning process has been successful.

3.14.4 Comparison of results

The results show that although it was not possible to simulate the system of fig 3.35 with a sliding function containing an integral and double integral, comparable results were obtainable with a reduced order sliding function and a PI controller indicating that the linear part of the feedback loop is primarily responsible for the dynamics of the system. When compared to the DSM system (results 1b, 2b, 3b, from Appendix F)

the DSM system gives superior control of the capacitor Voltage but has an equally slow transient response. The results of a tuned PI linear system have been shown to give superior results with good steady state THD performance and transient performance. Further analysis will be needed to thoroughly understand the mechanisms responsible for the behaviour of the DSM system to determine if its performance can be improved.

3.15 Chapter 3: Conclusions

Chapter three of this thesis commenced with an introduction to Sliding Mode and progressed through the various stages of development with supporting theory, to arrive at methods for the design of a DSM controlled APF. To test the theory an extensive APF model was constructed in Simulink, making use of many of the built in functions of MATLAB and also making extensive use of the SimPowerSystems toolbox to allow integration of physical models of electrical components.
Some encouraging results have been obtained indicating that this method may have some potential.
A comparison of the methods using a sampled discrete approach was made with existing relevant research carried out using linear techniques.

The methods differ from existing work in the following areas:

- Discrete rather than analogue approach
- Enhanced H-Bridge to cater for higher current gradients; using the reachability condition to engage the higher rates and avoid unnecessary current overshoot
- Use of the bridge energy storage capacitor as an integrator to form the switching surface
- Deriving the capacitor reference from the integral of the source reference current
- Enhanced source current reference through the use of a continuous function which helps to reduce the reference harmonic distortion
- Discrete iterative function to obtain the ideal input conductance

Problems were found with some of the physical SimPowerSystems models which were reported in Chapter 3 along with solutions to these problems.

A study of existing linear systems was carried out – in particular the use of a PI controller. Some good results and transient recovery times were achieved through the use of PI tuning. It was shown that a PI controller relies on some linearising approximations to overcome the inherent non-linearity of the APF system.

The results presented in existing research work based on a second order sliding function could be replicated with a linear PI controller alone, which cast some doubt over the effectiveness of the proposed sliding controller.

It has been seen from results 1b, 2b, and 3b (Appendix F) that when $\lambda > 0$ for a 1st order sliding space, the transient response is unacceptably long. Section 4.3.4 will show that the proposed DSM has instability in the outer loop (see loop description in section 4.3). It will be shown that whereas the entire system comprising inner and outer loops is stable, the outer loop alone is unstable, which is the primary reason for the long K response time. When using sliding control of order greater than zero to affect the capacitor Voltage (the capacitor is used as a sensor), this has an effect on the feedback signal used in the energy difference calculation to obtain K by iteration. Any sliding system that uses a function obtained from the integral of the filter error current will inevitably affect the energy changes in the capacitor which in turn must have an effect on the control system's ability to converge to a steady input conductance.
To quantify the exact effect on K due to the incorporation of capacitor Voltage into the sliding equation requires the analysis presented in Chapter 4.

Chapter 4 Real Power Flow Analysis, Proportional Hysterisis switching and the Energy Compensation Method

It is evident from the results and conclusions of Chapter 3 that more insight is required before a proper judgement can be made of the suitability of the sliding mode technique for control of the APF, in particular the effect on K of using sliding space orders greater than zero. The discrete system approach to the APF will be maintained throughout this chapter where the DSM sample interval T will be used as the delay time, enabling further analysis to be carried out in the Z-domain.

The approach taken in this chapter will be to form an overview of the system from an *energy-per-cycle* perspective and will be referred to as "Real Power Flow Analysis". This analysis method uses the principle that provided the switching bandwidth is high enough, it is not necessary to view all aspects of all current waveforms and all Voltage waveforms to assess the system dynamics.

Sub section 1 of this chapter introduces Real Power Flow Analysis.
Sub section 2 of this chapter investigates the simpler zero-order system ($\lambda = 0$) using Real Power Flow Analysis and compares the results of a load step response with those obtained using the APF model developed in section 3.12, noting that there is no capacitor control under these conditions and so is intended for theoretical study only.
Sub section 3 of this chapter deals with the complexity of the 1^{st} order system ($\lambda > 0$) and draws conclusions about the success of 1^{st}-order DSM applied to the APF.
Sub Section 4 of this chapter introduces a new control method referred to as "Energy Compensation". The Principles of Real Power Flow Analysis are used to study the behaviour of this technique to show the benefits it provides.
Sub section 5 of this chapter introduces the concept of proportional hysterisis switching control and shows how this can be used in conjunction with "energy compensation" to produce an optimal solution for APF control.

4.1 An Introduction to Real Power Flow Analysis

The concept of real power flow is an extension of the concept of power averaging. Only those currents that deliver real power are of concern since these have a direct impact on the dynamic behaviour of the APF. The components that handle reactive or harmonic power are eliminated from system analysis since the power components they carry average to zero over one source cycle (τ) and have no bearing on the dynamic APF performance.

When the APF reaches a stable operating condition i.e. when the source supplies a steady real power component of the load there are two conditions to consider with regard to the APF current as discussed in sections 2.4.3.1 and 2.4.3.2. If the source is purely sinusoidal then the APF provides only the reactive and harmonic power components. However, if the source is distorted then there may be a component of source current that has to be frequency converted by the APF before it provides real load power.

If it is assumed that the source Voltage is undistorted, then once K has settled to a steady level, the APF current can only consist of a possible fundamental reactive component at 90 deg to the source and higher order harmonics - none of which supply any real power when averaged over a complete source cycle (τ). Therefore any energy taken from the APF storage capacitor is returned resulting in no net energy change over a mains cycle. These current components flow only between APF and load.

If the source Voltage is distorted then for a steady K, the APF current will consist of a possible reactive component at 90 deg to each of the respective Voltage components as well as higher order harmonics none of which will supply any real power when averaged over a source cycle (τ). These components flow only between APF and load. There is another possible component that flows into the APF from the source at one frequency and from the APF to the load at another frequency giving no net change in APF storage energy per cycle. Therefore the total APF energy change averages to zero over a mains cycle giving no net energy change in the APF storage capacitor.

It follows that if only the real power handling components are considered then under steady state conditions (i.e. steady K) for both the undistorted and distorted source Voltage conditions, the average APF real power handling current flow is zero.
It will be assumed that the bandwidth of the switching system is high enough so that I_s follows the profile of I_{sref}. A small amount of loss through the switching system is tolerated in the analysis but this is treated as linear attenuation such that no additional harmonics are introduced into I_{sref}. Since this reference is proportional to V_s (eqn {3.29}) and K is updated every τ at the zero crossing point of the source cycle (eqn {3.35}), then it will be further assumed that the source provides no reactive or harmonic component to the load or APF.
Since K is updated periodically at the zero crossing point of the source then the I_{sref} is a continuous (C^0) function which contains fewer harmonic compared to a system that updates K periodically at a point other than at the zero crossing (see section 3.10). Furthermore, by switching K at the zero crossing point of the source, the power input is always real (there are no reactive terms) since the Voltage and current remain proportional over the cycle τ. Additionally, since the power input is always real then all of the harmonic components of the current reference brought about by K changing periodically will sum to zero over one period of τ.
During the transient settling time as the capacitor is charging (or discharging), energy is being transferred to (or removed from) the APF. This constitutes real power and only occurs during the transient following switch-on or a load change to raise (or lower) the capacitor to its working average Voltage ($V_{capconst}$). This real power must be passed by an APF current component which has a power factor of +/-1. This important current will be designated $I_{f1}(t)$ – the in-phase (or 180 deg out-of phase) fundamental component of $I_f(t)$.
It is not necessary to consider any of the other harmonics of I_f since on a per-cycle basis they carry no real power and therefore will not affect the system dynamics.
A further assumption is made that V_s is purely a sinewave. This simplifies the analysis in that I_{f1} is a single non-reactive fundamental component. If V_s were to contain harmonic distortion then additional higher harmonic non-reactive components of I_f would need to be considered, themselves having +/- 1 power factor with respect to their generating source harmonic Voltages. *There is no loss in generality of the analysis by assuming V_s to be a pure sinewave.*

As the system stabilises (i.e. as K stabilises) I_{f1} must decay to zero. The dynamics of I_{f1} and K are therefore central to the analysis and therefore it is necessary to derive a system loop to analyse these parameters.

4.2 Zero-order system analysis ($\lambda = 0$)

Initially the (theoretical) system is analysed (where no capacitor Voltage control is imposed).

Re-writing eqn 3.35 as a function of z:

$$K(z) = z^{-1}K(z) - \frac{\Delta E(z)}{\tau . V_{sRMS}^2} \qquad \text{-----\{eqn 4.1\}}$$

ΔE is the energy entering the APF per cycle and being stored in the capacitor.

Also the energy entering the APF can be derived from the RMS quantities:

$$\Delta E(z) = z^{-1} I_{f1RMS}(z) . V_{sRMS} . \tau \qquad \text{-----\{eqn 4.2\}}$$

I_{f1RMS} is the RMS value of the 1st harmonic component of I_f with power factor of +/-1 and the energy change in the capacitor is based on the value of I_{f1} in the previous cycle τ.

From eqn {3.30}:

$I_{fref}(t) + I_L(t) = I_{sref}(t)$

It follows that for the 1st harmonics (with +/-1 power factor) of each current component:

$I_{f1ref}(t) + I_{L1}(t) = I_{s1ref}(t)$ and $I_{f1refRMS} + I_{L1RMS} = I_{s1refRMS}$

The source current reference is derived from V_s and K from eqn {3.29}

$I_{sref}(t) = K.V_s(t)$ and $I_{srefRMS} = K.V_{sRMS}$

Provided V_s is purely sinusoidal then $I_{s1ref}(t) = I_{sref}(t)$ and therefore $I_{s1refRMS} = I_{srefRMS}$

Therefore: $I_{f1refRMS}(z) + I_{L1RMS}(z) = K(z).V_{sRMS}$ -----{eqn 4.3}

Eqn {4.3} assumes that V_{sRMS} remains constant and $I_{f1refRMS}$, I_{L1RMS}, and K are time dependent.

Note: There is no loss in generality of the "Real Power Flow" analysis technique by making V_s a sinusoid (see section 4.1). The purpose of this modelling technique is to investigate dynamic response so complexity is deliberately kept to a minimum.

Combining eqns {4.1, 4.2, 4.3} into a sampled system:

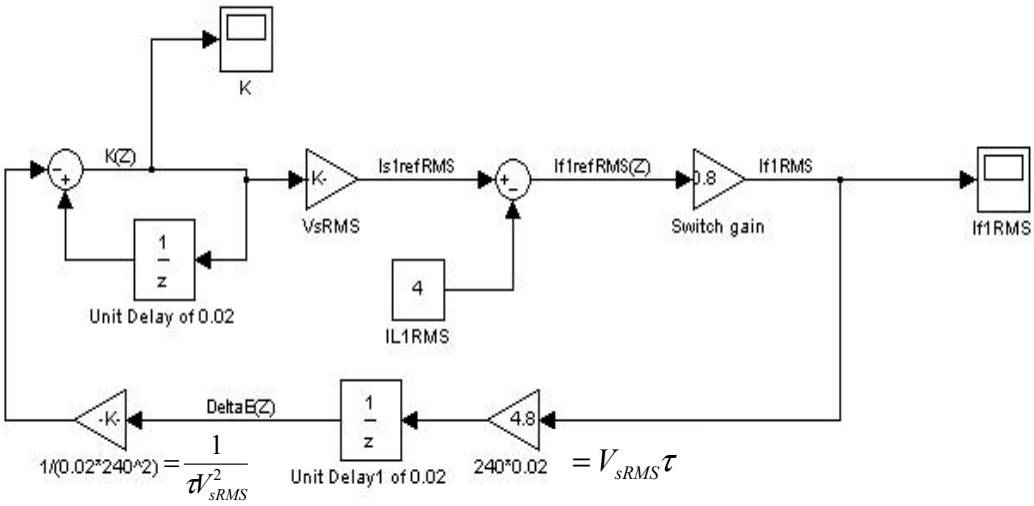


Fig 4.1*: Real Power signal flow diagram for a zero order APF system ($\lambda = 0$)*

Simulink has been used to simulate the system with $V_{sRMS} = 240$ and $I_{L1RMS} = 4A$ (i.e. the load fundamental in-phase component is 4A for a real power of 960 W).
A discrete fixed-step solver has been used and the simulation time has been set to 0.5s. The sample time for the delay blocks is set to $\tau = 20ms$.

It may be seen that the zero-order APF switching line has been represented as a linear gain block "switch gain" which in the analysis is represented as g ($0 < g \leq 1$). It is assumed that the switching system produces an output that on average is proportional to the input and therefore the switching system can be considered as an amplifier (typically with gain less than unity), furthermore it is interesting to investigate how the system behaves for a range of g values.
To analyse the system with an initial condition for K, eqns 4.1, 4.2 and 4.3 are re-written in difference equation form:

$$K(N\tau) = K((N-1)\tau) - \frac{\Delta E(N\tau)}{\tau V_{sRMS}^2}$$

$$\Delta E(N\tau) = I_{f1RMS}((N-1)\tau).V_{sRMS}.\tau$$

$$I_{f1refRMS}(N\tau) = I_{s1refRMS}(N\tau) - I_{L1RMS}(N\tau) = K(N\tau)V_{sRMS} - I_{L1RMS}(N\tau)$$

Switch gain:
$I_{f1RMS} = gI_{f1refRMS}$

$$\therefore K(N\tau) = K((N-1)\tau) - \frac{I_{f1RMS}((N-1)\tau)V_{sRMS}\tau}{\tau V_{sRMS}^2} = K((N-1)\tau) - \frac{gI_{f1refRMS}((N-1)\tau)}{V_{sRMS}}$$

$$\therefore K(N\tau) = K((N-1)\tau) - \frac{g}{V_{sRMS}}(V_{sRMS}K((N-1)\tau) - I_{L1RMS}((N-1)\tau))$$

Shift left:

$$K((N+1)\tau) = K(N\tau) - gK(N\tau) + \frac{g}{V_{sRMS}}I_{L1RMS}(N\tau)$$

Taking Z transforms:

$$z(K(z) - K(0)) = K(z)(1-g) + \frac{g}{V_{sRMS}}I_{L1RMS}(z)$$

$$\therefore K(z)(z-1+g) = \frac{gI_{L1RMS}(z)}{V_{sRMS}} + zK(0)$$

$$\therefore K(z) = \frac{gI_{L1RMS}(z)}{V_{sRMS}}\frac{1}{(z-1+g)} + \frac{zK(0)}{(z-1+g)}$$

Since the load is specified (from time zero) and remains unchanged then let the 1st harmonic in-phase component be given by $I_{L1RMS} = I_{LOAD1}\left(\frac{z}{z-1}\right)U(z)$ for a fixed load taking a resistive RMS current I_{LOAD1}. U(z) is the unit step function.

$$K(z) = \frac{gI_{LOAD1}}{V_{sRMS}}\left(\frac{z}{(z-1)}\right)\left(\frac{1}{z-(1-g)}\right)U(z) + \frac{zK(0)}{(z-(1-g))}U(z)$$

Applying the final value theorem:

Final value of K = $\lim_{z\to 1}(z-1)K(z) = \frac{I_{LOAD1}}{V_{sRMS}}$

Applying the initial value theorem:

Initial value of K = $\lim_{z\to\infty} K(z) = K(0)$ as required.

$$K(z) = \frac{I_{LOAD1}}{V_{sRMS}}\left(\frac{1}{(z-1)} - \frac{(1-g)}{(z-(1-g))}\right)U(z) + \frac{zK(0)}{(z-(1-g))}U(z)$$

$$K(z) = \frac{z^{-1}I_{LOAD1}}{V_{sRMS}}\left(\frac{z}{(z-1)} - \frac{z(1-g)}{(z-(1-g))}\right)U(z) + \frac{zK(0)}{(z-(1-g))}U(z)$$

Inverse Z transform gives:

$$K(N\tau) = U((N-1)\tau)\frac{I_{LOAD1}}{V_{sRMS}}\left(1-(1-g)(1-g)^{N-1}\right) + U(N\tau)(1-g)^N K(0)$$

$$K(N\tau) = U((N-1)\tau)\frac{I_{LOAD1}}{V_{sRMS}}\left(1-(1-g)^N\right) + U(N\tau)(1-g)^N K(0)$$

Where U(Nτ) = 1 for N $\geq$ 0 , U(N) = 0 for N < 0

When N = 0, K(0) = 0 + K(0) = K(0)

When N = 1, $K(\tau) = \frac{I_{LOAD1}}{V_{sRMS}}g + (1-g)K(0)$

When N = 2, $K(2\tau) = \frac{I_{LOAD1}}{V_{sRMS}}\left(1-(1-g)^2\right) + (1-g)^2 K(0)$ etc.

Let a = 1 - g

Therefore:

$$K(N\tau) = U((N-1)\tau)\frac{I_{LOAD1}}{V_{sRMS}}\left(1-a^N\right) + a^N K(0)$$

With the simulation values used the final value of K = 4/240 = 0.01667

Note that as K approaches its final value, I_{S1RMS} will approach I_{L1RMS} causing I_{f1RMS} to approach zero as required. The purpose of the APF is to provide reactive power only, therefore the real power flow in the APF represented by the in-phase 1st harmonic I_{f1RMS} must decay to zero.

If g = 1 (a = 0) representing a lossless APF switch, then the final value is achieved immediately at the first sample, i.e. K(τ) = I_{LOAD1}/V_{sRMS}.

For $0 < g < 1$ (a lossy switching system) then $0 < a < 1$ and $K(N\tau)$ will approach the final value from the initial condition as the transient a^N dies away.

The following example results were obtained from Simulink:

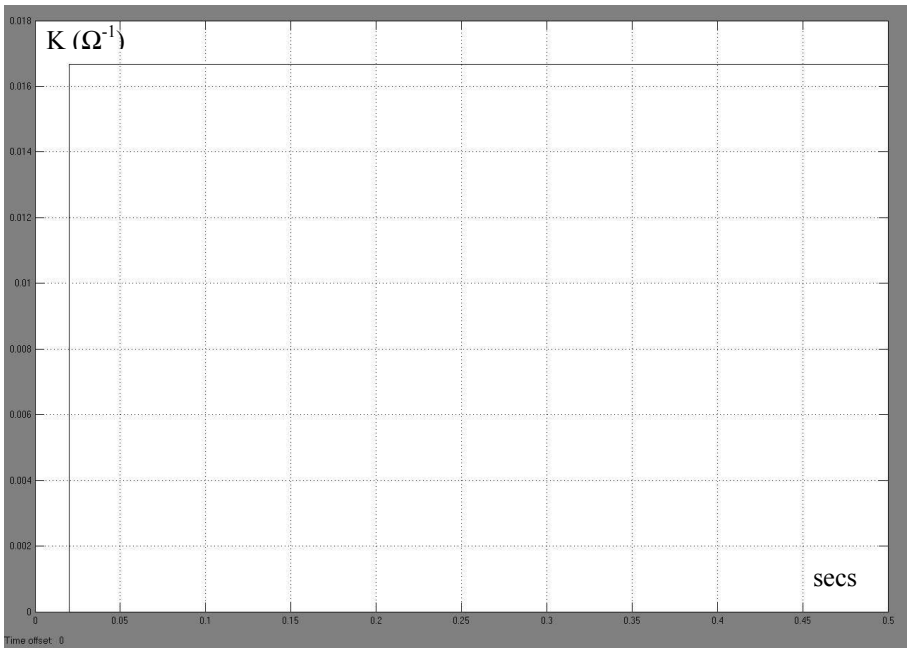


Fig 4.2*: Plot of K with K(0) = 0, g = 1*

As predicted, K reaches its final value when N = 1 ($t = \tau$).

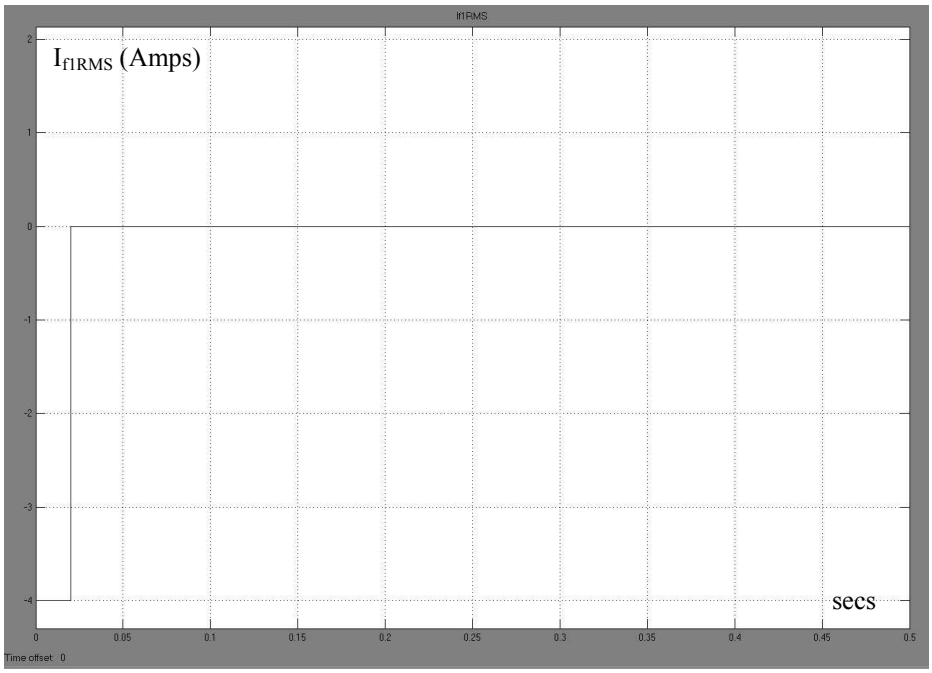


Fig 4.3*: Plot of I_{f1RMS} with K(0) = 0 , g = 1*

I_{f1RMS} achieves its final value of 0 when N = 1.

Note that the current is an RMS quantity but the simulation assigns an initial –ve value to the current. The concept of a –ve RMS quantity must be interpreted here as power flowing in the opposite direction (i.e. leaving the APF) i.e. a –ve RMS quantity due to I_{f1RMS} being in anti-phase with V_s (i.e. a power factor of -1).

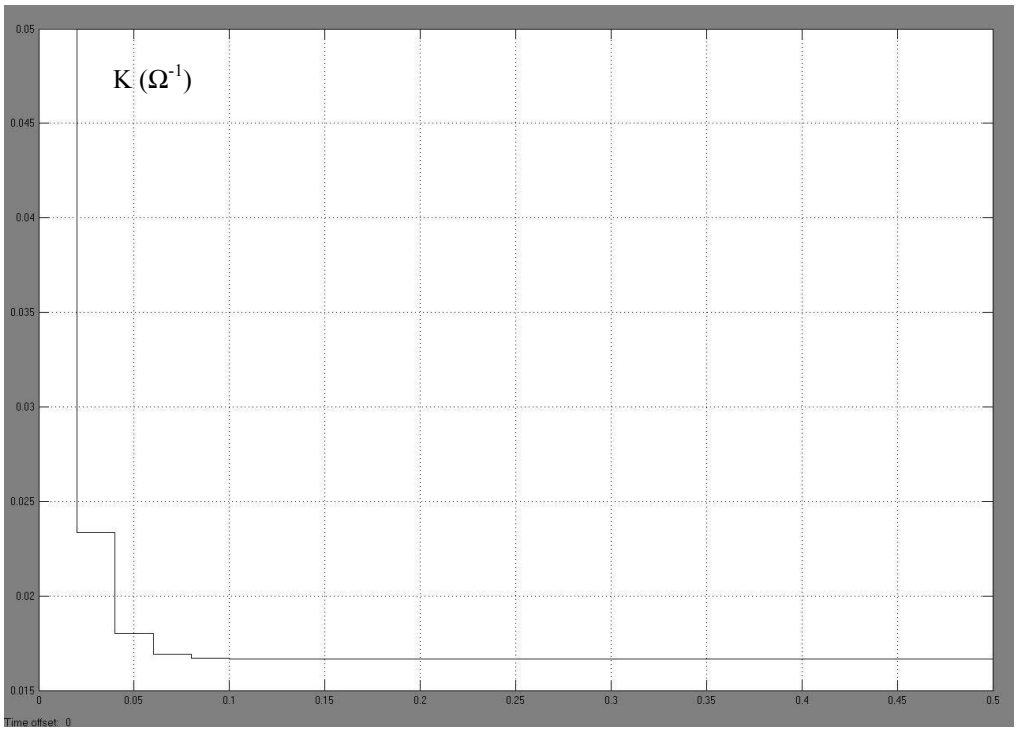


Fig 4.4*: Plot of K with K(0) = 0.05, g = 0.8*

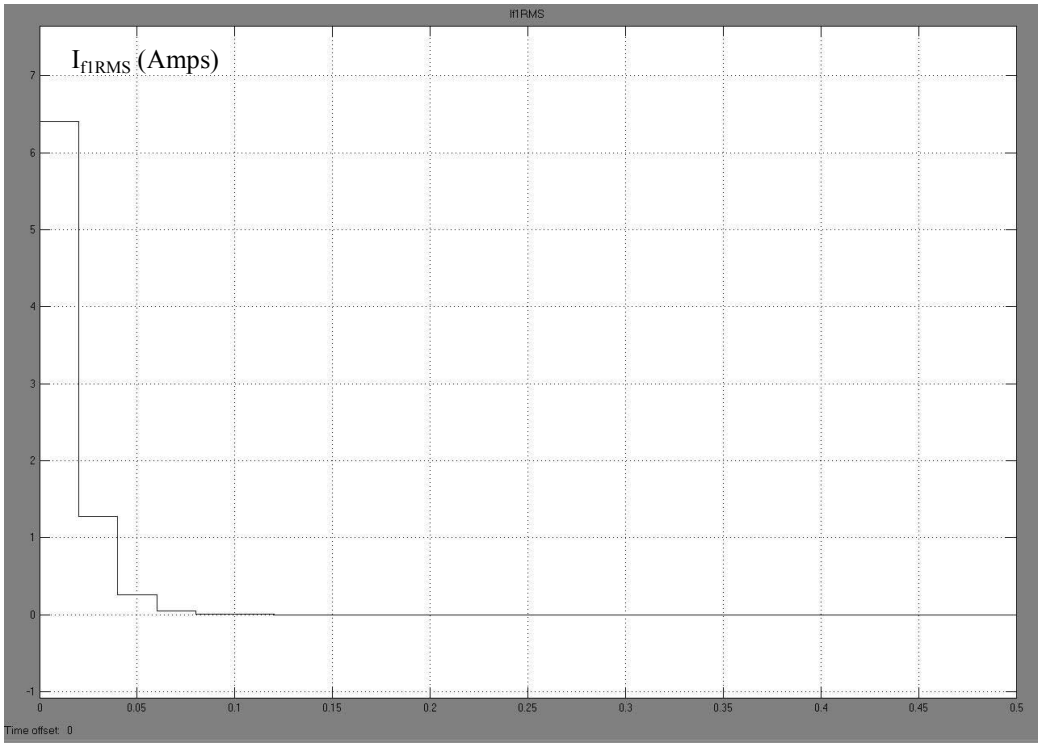


Fig 4.5*: Plot of I_{f1RMS} with K(0) = 0.05, g = 0.8*

It can concluded that the greater the accuracy of the APF switching system to force I_f to follow I_{fref} (i.e. the higher the bandwidth of the system) then the quicker the response time to a stable K value.

4.2.1 Investigation of a load step when $\lambda = 0$

This section investigates the performance of the APF to a step change in load when $\lambda = 0$ (i.e. the zero-order switching space).

Two sets of results are presented.

Section 4.2.1.1 evaluates the effect of a step change in load on the full MATLAB APF model (as described in section 3.12 and given in Appendix C).

Section 4.2.1.1 evaluates the effect of the same step change in load on the system derived using Real Power Flow analysis and based on the system given in fig 4.1

The two sets of results are then compared.

4.2.1.1 Step change of load in the MATLAB model of Appendix C with $\lambda = 0$

The APF model given in Appendix C and fully detailed in section 3.12 was simulated with the following non-linear load:

- D2: open (giving a half wave rectified load current)
- Inductor = 1mH
- cload: open
- Rload switched1: in circuit
- Rload = 30 Ohm

The control algorithm switch_control3.m (Appendix D) is used.

The following parameters were set up in the MATLAB workspace:
T = 20μs and lambda = 0, V_{sRMS} = 240.

The generator driving Rload switched1 was set so that from 0 to 200ms Rload switched1 was open (allowing the system to stabilise) and at 200ms Rload switched1 was switched into circuit.
For the first 200ms only Rload is in circuit and conducts half wave giving I_{LOAD1} = 4A RMS. From 200ms to 400ms both Rload and Rload1 are switched into circuit also conducting half wave giving I_{LOAD1} = 8A RMS.

From 0 to 200ms the non-linear load is the same as "non-linear load 1" as described in table 3.5 therefore the results will match those of Appendix F: Result Set 1a, however after 200ms the model changes as the current is doubled.

Inspection of K from Appendix F: Result Set 1a will show that K reaches a steady value at 100ms. From the transient decay of K to its new value, it is possible to estimate a value of g (effective gain) for the APF. Since the APF bandwidth will depend on V_{cap} which is uncontrolled when $\lambda = 0$, this value of g will not necessarily always be the same.

MATLAB APF Simulation results for the load step:

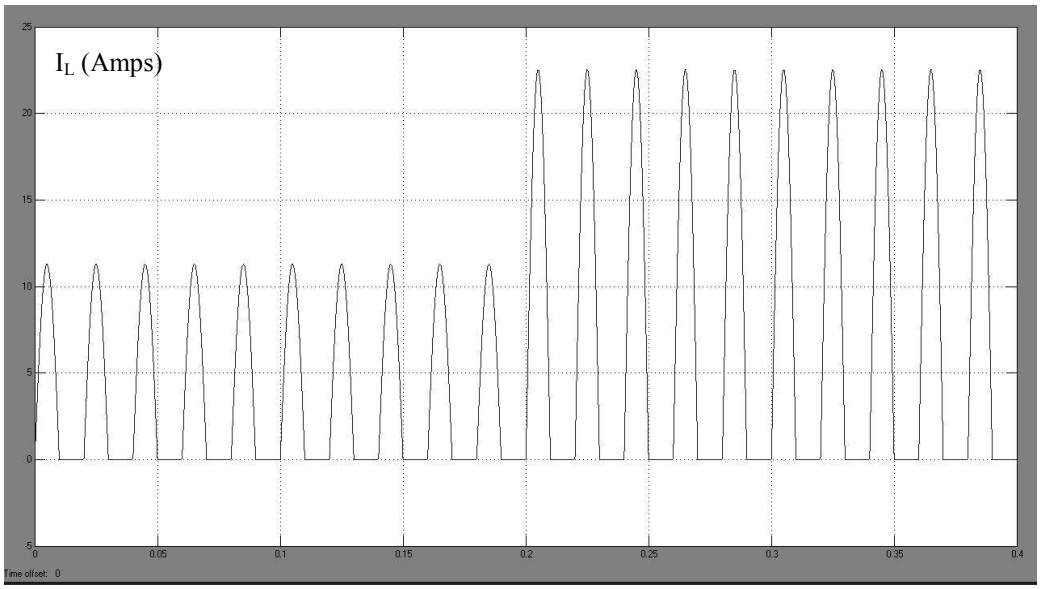


Fig 4.6: *Plot of I_L (load current) for load step change ($\lambda = 0$)*

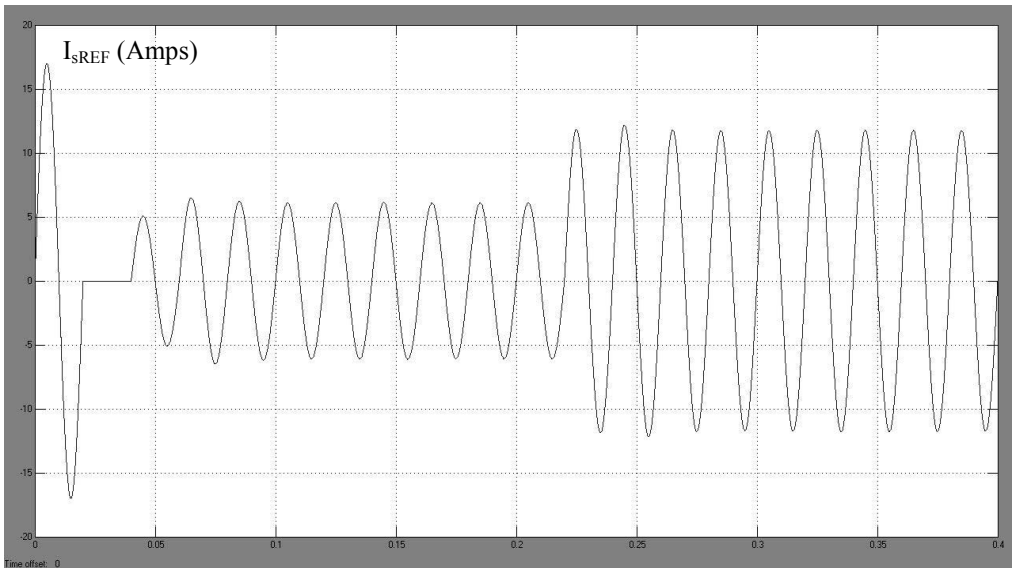


Fig 4.7*: Plot of I_{sREF} (source reference) for load step change ($\lambda = 0$)*

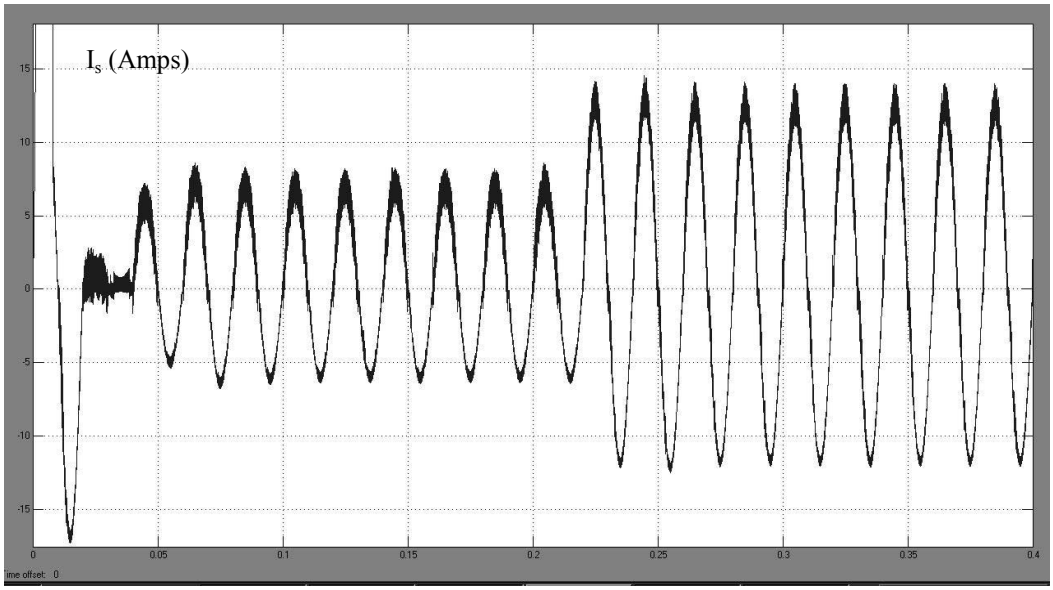


Fig 4.8: *Plot of I_s (source current) for load step change ($\lambda = 0$)*

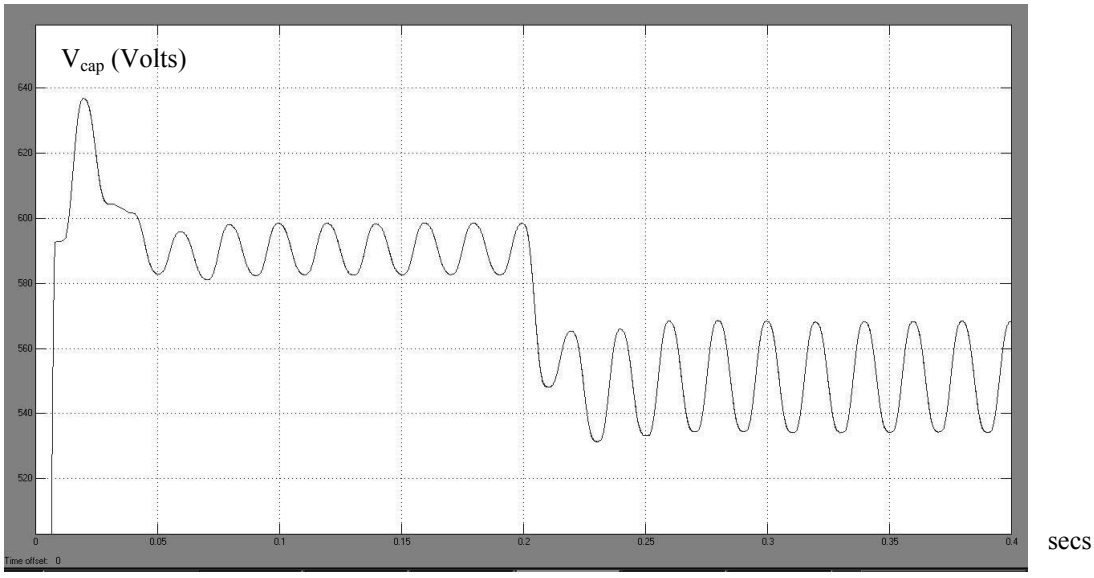


Fig 4.9: *Plot of V_{cap} for load step change ($\lambda = 0$)*

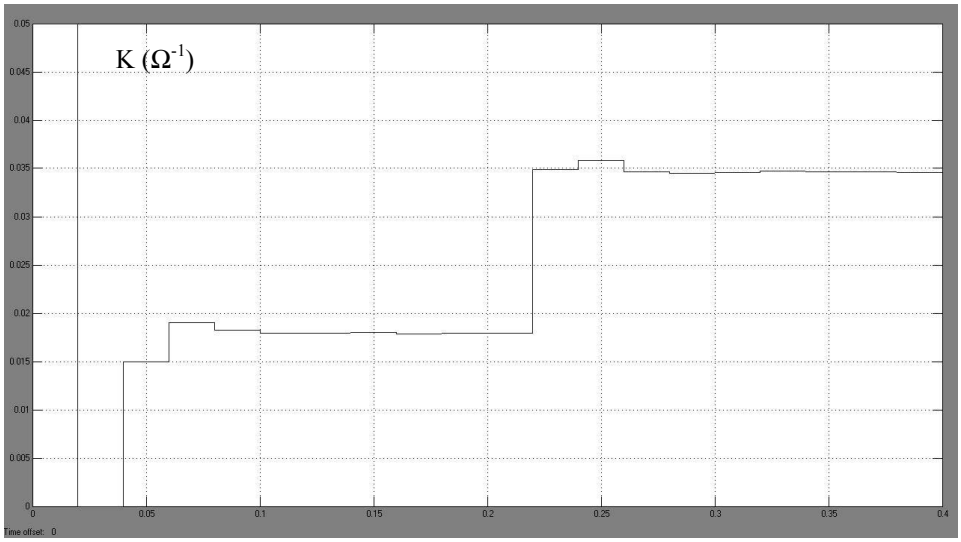


Fig 4.10*: Plot of K (input conductance) for a load step change*

It can be seen that K changes after a delay of τ following 200ms. K is always delayed by τ since it uses ΔE from the previous mains cycle to calculate the new value.

V_{cap} moves from 590 to 550V since it is not controlled when $\lambda = 0$.
Examination of K indicates that it almost reaches the final value in the 1st sample period and settles after 4 sample periods of τ.

4.2.1.2 Step Change of Load using Real Power Flow model of fig 4.1

A simulation of fig 4.1 was performed to investigate how K responds to a step change in load. The following parameters were used:

- K(0) = 0.01666
- I_{LOAD1} = 8A
- g = 0.94
- V_s = 240

The initial value of K is set to 0.01666 which is the steady value achieved in fig 4.10 at 200ms. The reaction of K to the new load step of 4A to 8A after a period τ should be similar to the step just after 200ms in fig 4.10.
After the first sample period of τ, K will move from 0.01666 to its new value corresponding to the value of I_{LOAD1}.

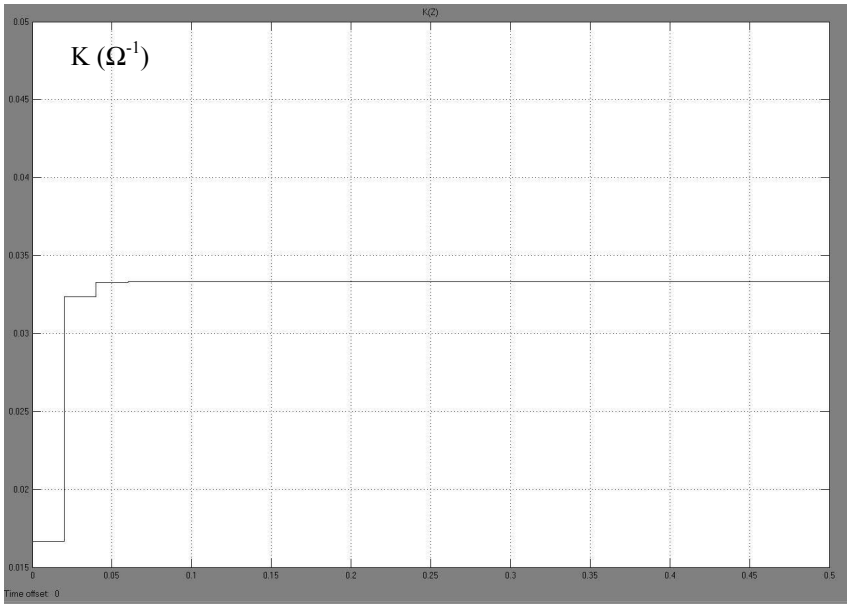


Fig 4.11*: A plot of K (input conductance) for the Real Power Flow signal loop of fig 4.1 (when $\lambda = 0$)*

K settles to its new value of 0.0333 in a similar number of steps of τ as that in fig 4.10. Any small differences between fig 4.10 and 4.11 are due to the inability of the APF MATLAB model to exactly follow the APF current reference which is a system bandwidth limitation.

The similarity of fig 4.10 (at 200ms) with fig 4.11 indicates that it was reasonable to use an APF gain g = 0.94.

4.3 Real Power Flow Analysis of a DSM First Order System ($\lambda > 0$)

An additional loop was added to Fig 4.1 in order to control the capacitor Voltage and increase the order of the sliding space to 1. There are effectively two control loops linked together via the sliding line.

- The *APF current control loop* (Fig 4.1) will be referred to as the "**outer**" loop
- The *capacitor Voltage control loop* (Fig 4.12) will be referred to as the "**inner**" loop

A note on loop designation

The loop designations used in most existing research work are normally chosen such that the outer loop is associated with capacitor Voltage control and has slower convergence and the inner loop is associated with APF current control and has faster convergence. For example, linear systems employing long time-constant averaging

filters and the PI controller as discussed in section 3.15.2 have a slow Voltage control loop and generally (see ref [5.4] for example) consider the Voltage control to be the outer loop and current control to be the inner loop. The DSM system used in this thesis updates the current reference every mains period τ (20ms) whereas the capacitor energy control is included in the DSM equation which is sampled at period T (set in this thesis at 20μs). From this perspective it is logical to consider current control in the outer loop and Voltage control in the inner loop.

The link between the inner and outer loops assumes that the system remains on the sliding surface. From eqn 3.39:

$$S(t) = \frac{I_{fref}(t)}{C} - \frac{I_f(t)}{C} + \alpha\lambda\left(V_{capref}(t) - V_{cap}(t)\right) = 0$$

Provided the switching bandwidth is high enough for a sampled spectrum to be continuously occupied (see section 3.2.1) then DSM is periodic and consists of an active phase followed by a passive phase. Energy transfer will take place over two sample periods of T. The effective sampling period to be used for the inner signal flow loop is therefore 2T (i.e. a sampling rate of 1/2T). The inner loop sampling period will be referred to as Tinner = 2T.

Since two systems are being combined where one is sampled at τ and the other sampled at 2T then it is necessary to distinguish between them. The inner loop is switched at a much higher rate than the outer loop and this must be taken into account in the model for the results to be meaningful.
Therefore in the Z domain, two notations for z will be introduced:

- z_τ for the outer loop
- z_{2T} for the inner loop

The equation that links the inner loop and the outer loop is derived from eqn 3.39 and must default to the higher sampling rate. This is allowable since T is chosen so that τ is an integer multiple of T and for some variable X a sampled sequence is:

$$X(N\tau), X(N\tau + 2T), X(N\tau + 4T) \ldots X(N\tau + \tau - 2T), X((N+1)\tau)$$

Therefore in the Z_{2T} domain eqn 3.39 can be rewritten:

$$\left(I_{f1refRMS}(z_{2T}) - I_{f1RMS}(z_{2T})\right) + C\lambda\left(V_{capconst}(z_{2T}) - V_{cap}(z_{2T})\right) = 0 \qquad \text{-----\{eqn 4.4\}}$$

It should be noted that since only real power flow is being considered, the input capacitor reference is the constant value $V_{capconst}$ and *not* that given by eqn {3.42} since eqn {3.42} is the reference that tracks around the capacitor Voltage wave taking all APF current components into account – both real power and reactive power components of current.

The variable V_{cap} takes on a new meaning in that it is no longer a continuous function of time but a sampled variable (sampled at 2T) which changes in relation to the accumulation of energy in the capacitor as a result of current component I_{f1RMS}. Furthermore $I_{f1RMS}(2T)$ must be understood to be the sampled RMS of the fundamental component of I_f i.e. the square root of the average value of the square of I_{f1} over period τ taking the sign of the power factor (i.e. negative if in anti-phase with V_s) and sampled at period 2T.

When steady state conditions have been reached for a constant load, and I_{f1RMS} has fallen to zero, V_{cap} will remain at a constant value.

The polarity switching variable α need not be included in eqn {4.4} since RMS values and energy per source cycle are the only considerations here.

K control in the outer loop is derived from eqn 4.1 but re-written using the new definition of z:

$$K(z_\tau) = Z^{-1}K(z_\tau) - \frac{\Delta E(z_\tau)}{\tau . V_{sRMS}^2} \qquad \text{-----\{eqn 4.5\}}$$

K control in the outer loop relies on calculating the change of energy in the capacitor every period τ which itself is accumulating at a period of 2T; therefore a meaningful model must incorporate energy accumulation. This causes problems from an analytical point of view since the model becomes non-linear.

To proceed with the analysis, initially the inner loop will be considered

- Section 4.3.1: Analyse the inner loop using linearising approximations to gain an appreciation of the dynamics of the inner loop alone.
- Section 4.3.2: A non-linear analysis of the inner loop for the purpose of simulation and comparison with the actual APF model (Appendix C).

The inner and outer loops will then be combined:

- Section 4.3.3: Analysis of the combined inner and outer loop.

In an attempt to obtain the required response, the inner loop feedback is modified by using an energy difference signal:

- Section 4.3.4: Analysis of the combined inner and outer loop using a modified energy-difference calculation in the outer loop

Problems are encountered with the modified energy-difference feedback signal:

- Section 4.3.5: Combined Inner and Outer loops.

  Outer Loop Instability Investigation using the Modified Energy-Difference Feedback Signal

4.3.1 Inner loop dynamics using a linearising approximation ($\lambda > 0$)

From eqn {3.32}

$$\Delta E = \frac{1}{2} C V_d \left(V_{capnew} + V_{capold} \right) \quad \text{where } V_d = V_{capnew} - V_{capold}$$

In order to linearise the system (compare eqns {3.69 }, {3.70}), the following approximation is required:

$$V_{capave} = \frac{1}{2}\left(V_{capnew} + V_{capold} \right) \text{ (= average capacitor Voltage)}$$

Therefore:

$$\Delta E(N2T) = V_{capave} C\left(V_{cap}(N2T) - V_{cap}((N-1)2T) \right)$$

In the Z_{2T} domain:

$$\Delta E(z_{2T}) = V_{capave} C\left(V_{cap}(z_{2T}) - z_{2T}^{-1} V_{cap}(z_{2T}) \right) = \left(1 - z_{2T}^{-1}\right) V_{capave} C V_{cap}(z_{2T})$$

-----{eqn 4.6}

The change in energy per cycle is given in terms of I_{f1RMS} (see eqn {4.2}) but must now be considered as sampled at 2T (not τ)

$$\Delta E(z_{2T}) = 2T V_{sRMS} z_{2T}^{-1} I_{f1RMS}(z_{2T})$$

-----{eqn 4.7}

(= The input average power * sample period)

From eqns {4.6, 4.7}

$$\therefore z_{2T}^{-1} I_{f1RMS}(z_{2T}) . V_{sRMS} . (2T) = \left(1 - z_{2T}^{-1}\right) V_{capave} C V_{cap}(z_{2T})$$

-----{eqn 4.8}

Eqns 4.4 and 4.8 can form the following linearised inner loop:

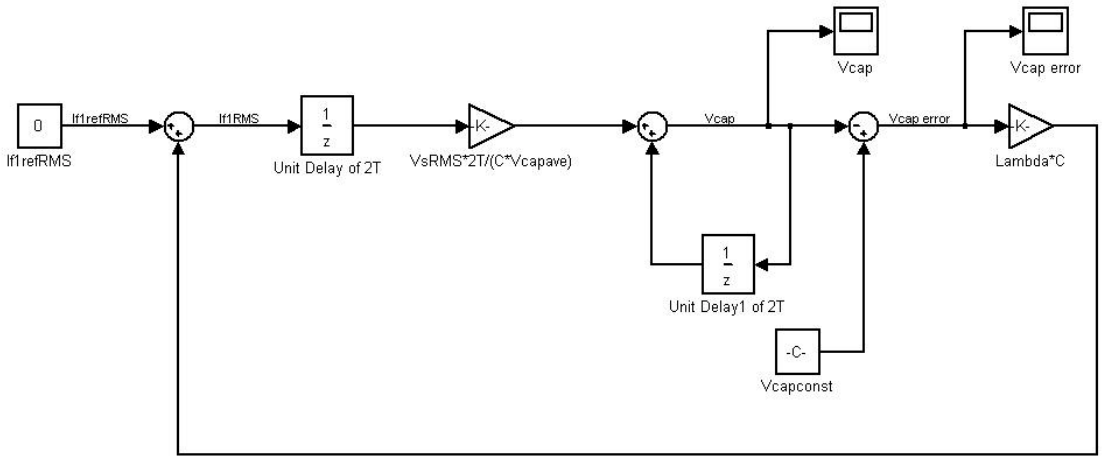


Fig 4.12*: Inner loop using Real Power signal Flow and a linearising approximation*

4.3.1.1 MATLAB simulation of the Inner Loop with linearising approximation

The following parameters were used in the simulation of fig 4.12:

C = 1000μF
Lambda = 1100
V_{sRMS} = 240
$I_{f1refRMS}$ initially set to 0
$V_{capconst}$ = 550
V_{capave} = 550

Unit delays set to Tinner where Tinner = 2T = 40μs

Use fixed step discrete solver

The initial values of "Unit Delay of 2T" and "Unit Delay1 of 2T" set to zero.

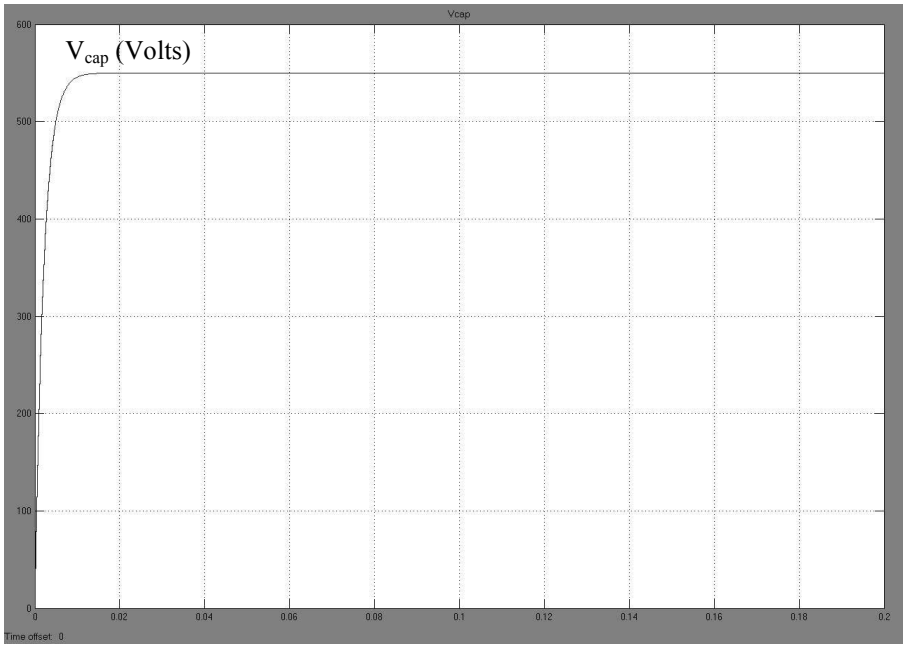


Fig 4.13: *Vcap response for the inner loop(fig 4.12) with the initial value of Vcap=0*

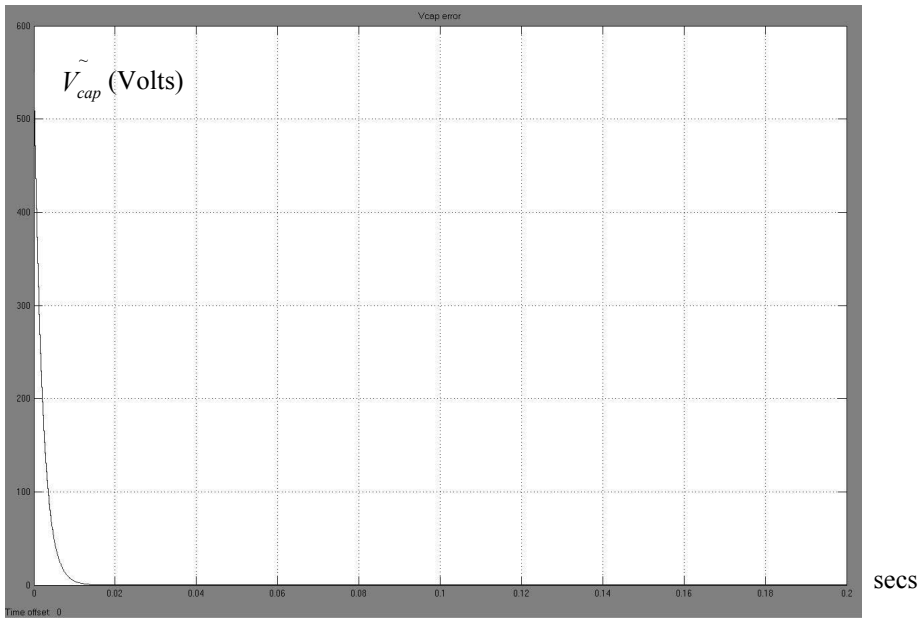


Fig 4.14*: Vcap error* ($\tilde{V}_{cap}$) *response for the inner loop (fig 4.12) with the initial value of Vcap = 0*

With the values given, steady state is achieved in about 10ms.

4.3.1.2 Analytical derivation of the inner loop response with linearising approximation

Deriving the loop equation for fig 4.12:

$$\tilde{V}_{cap}(z_{2T}) = V_{capconst}(z_{2T}) - V_{cap}(z_{2T}) = V_{capconst}(z_{2T}) - I_{f1RMS}(z_{2T})\frac{2T.V_{sRMS}}{C.V_{capave}}\frac{1}{z_{2T}}\frac{z_{2T}}{(z_{2T}-1)}$$

$$\therefore \tilde{V}_{cap}(z_{2T}) = V_{capconst}(z_{2T}) - \left(I_{f1refRMS}(z_{2T}) + \lambda C\tilde{V}_{cap}(z_{2T})\right)\frac{2T.V_{sRMS}}{C.V_{capave}}.\frac{1}{(z_{2T}-1)}$$

$$\therefore \tilde{V}_{cap}(z_{2T})\left(\frac{V_{capave}.(z_{2T}-1)+2T.\lambda V_{sRMS}}{V_{capave}.(z_{2T}-1)}\right) = V_{capconst}(z_{2T}) - I_{f1refRMS}(z_{2T}).\frac{2T.V_{sRMS}}{C.V_{capave}}.\frac{1}{(z_{2T}-1)}$$

$$\therefore \tilde{V}_{cap}(z_{2T}) = \frac{V_{capconst}(z_{2T}).V_{capave}.(z_{2T}-1)}{V_{capave}.(z_{2T}-1)+2T.\lambda.V_{sRMS}} - I_{f1refRMS}(z_{2T}).\frac{2T.V_{sRMS}}{C\left(V_{capave}.(z_{2T}-1)+2T.\lambda.V_{sRMS}\right)}$$

-----{eqn 4.9}

In practice the outer loop will maintain $I_{f1refRMS}$ at a steady value for period τ and it has been seen that the inner loop steady state is typically achieved in 10ms so it is reasonable to let $I_{f1refRMS}$ equal a constant value for t > 0:

$$I_{f1refRMS}(z_{2T}) = \frac{z_{2T}.I_{f1refCONST}}{(z_{2T}-1)}U(z_{2T})$$

(U is the unit step function at t = 0)

Also, $V_{capconst}$ is a constant value for t > 0 and this will be the average steady state value (= V_{capave}):

$$V_{capconst}(z_{2T}) = \frac{z_{2T}V_{capave}}{(z_{2T}-1)}U(z_{2T})$$

Applying the final value theorem:

$$\lim_{t\to\infty}\left(\tilde{V}_{cap}(t)\right) = \lim_{Z_{2T}\to 1}(z_{2T}-1)\tilde{V}_{cap}(z_{2T}) = -I_{f1refCONST}(z_{2T}).\frac{1}{C.\lambda}$$

Hence the error in capacitor Voltage in steady state depends on the value of the RMS of the APF reference current.

Substituting step input values for $V_{capconst}$ and $I_{f1refRMS}$ into eqn {4.9} gives:

$$\tilde{V}_{cap}(z_{2T}) = \frac{z_{2T}V_{capave}^2}{V_{capave}.(z_{2T}-1)+2T\lambda.V_{sRMS}}U(z_{2T}) - I_{f1refCONST}.z_{2T}\left(\frac{2TV_{sRMS}}{C}\right)\left(\frac{1}{z_{2T}-1}\right)\left(\frac{1}{(z_{2T}-1).V_{capave}+2T\lambda.V_{sRMS}}\right)U(z_{2T})$$

$$= \frac{z_{2T}V_{capave}}{z_{2T}-1+\frac{2T\lambda V_{sRMS}}{V_{capave}}}U(z_{2T}) - \frac{z_{2T}^{-1}I_{f1refCONST}}{C\lambda}\left(\left(\frac{z_{2T}}{z_{2T}-1}\right)-\left(\frac{z_{2T}\left(1-\frac{2T\lambda V_{sRMS}}{V_{capave}}\right)}{z_{2T}-1+\frac{2T\lambda V_{sRMS}}{V_{capave}}}\right)\right)U(z_{2T})$$

Therefore:

$$\tilde{V}_{cap}(N2T) = V_{capave}\left(1-\frac{2T\lambda V_{sRMS}}{V_{capave}}\right)^N U(N) - \frac{I_{f1refCONST}}{C\lambda}\left\{1-\left(1-\frac{2T\lambda V_{sRMS}}{V_{capave}}\right)\left(1-\frac{2T\lambda V_{sRMS}}{V_{capave}}\right)^{N-1}\right\}U((N-1)2T)$$

Therefore to remain stable: $0 < \frac{2T\lambda V_{sRMS}}{V_{capave}} < 2$

and to avoid oscillations : $0 < \frac{2T\lambda V_{sRMS}}{V_{capave}} < 1$ -----{eqn 4.10}

With $V_{sRMS} = 240$, $V_{capave} = 550$ and $T = 20*10^{-6}$ then to remain stable:

λ must be +ve and $< 1.146 * 10^5$

and to avoid oscillations $\lambda < 5.73 * 10^4$

Eqn. {4.10} provides an upper bound for λ for design purposes. However, the upper value of λ obtained is much larger than the practical value (section 3.11.5 step 10) and would result in gross errors in I_f (see section 3.1.4).

Using the simulation values of section 4.3.1.1 the transient decay for the inner loop is:

$$\left(1-\frac{2T\lambda V_{sRMS}}{V_{capave}}\right)^N = 0.98^N$$

With $2T = 40*10^{-6}$, after 5ms (i.e. N = 125) the transient term dies to 8.9% and after 10ms (i.e. N = 250) the transient term dies to 0.785%

This is in agreement with the simulation (section 4.3.1.1, fig 4.14) that the transient error is less than 1% after 10ms (i.e. $\tau/2$)

4.3.2 Inner Loop dynamics ($\lambda > 0$) without linearising approximations

This section re-visits the inner loop equations without making the linearising approximations of section 4.3.1. Comparisons are made of the simulations of the loop so obtained with the responses obtained in section 4.3.1.1.

The following necessary equations are re-stated. For the non-linear function the time domain is retained and the discrete time variable N2T is used. This variable indicates that sampling is taking place in the inner loop at integer multiples of 2T.

Eqn 4.7

$$\Delta E(z_{2T}) = z_{2T}^{-1} I_{f1RMS}(z_{2T}).V_{sRMS}.(2T)$$

Eqn 4.4

$$\left(I_{f1refRMS}(z_{2T}) - I_{f1RMS}(z_{2T})\right) + C\lambda\left(V_{capconst}(z_{2T}) - V_{cap}(z_{2T})\right) = 0$$

For the capacitor in the inner loop:

$$\Delta E(N2T) = \frac{1}{2} C\left(V^2{}_{cap}(N2T) - V^2{}_{cap}((N-1)2T)\right) \qquad \text{-----\{eqn 4.11\}}$$

The Real Power Flow simulation loop for these equations is as follows:

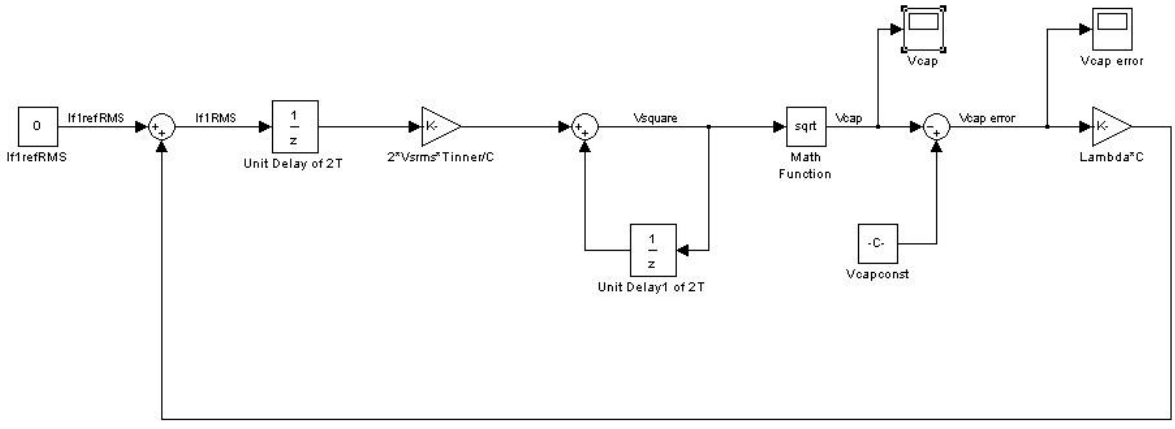


Fig 4.15: *Inner loop using Real Power signal Flow – no linearising approximations made*

For simulation, the same parameters as section 4.3.1.1. are used:

C = 1000µF
Lambda = 1100
V_{sRMS} = 240
$I_{f1refRMS}$ initially set to 0
$V_{capconst}$ = 550

Unit delays set to Tinner where Tinner = 2T = 40µs

Use fixed step discrete solver

The initial conditions of V_{square} and hence V_{cap} are set to zero and $I_{f1refRMS}$ = 0.

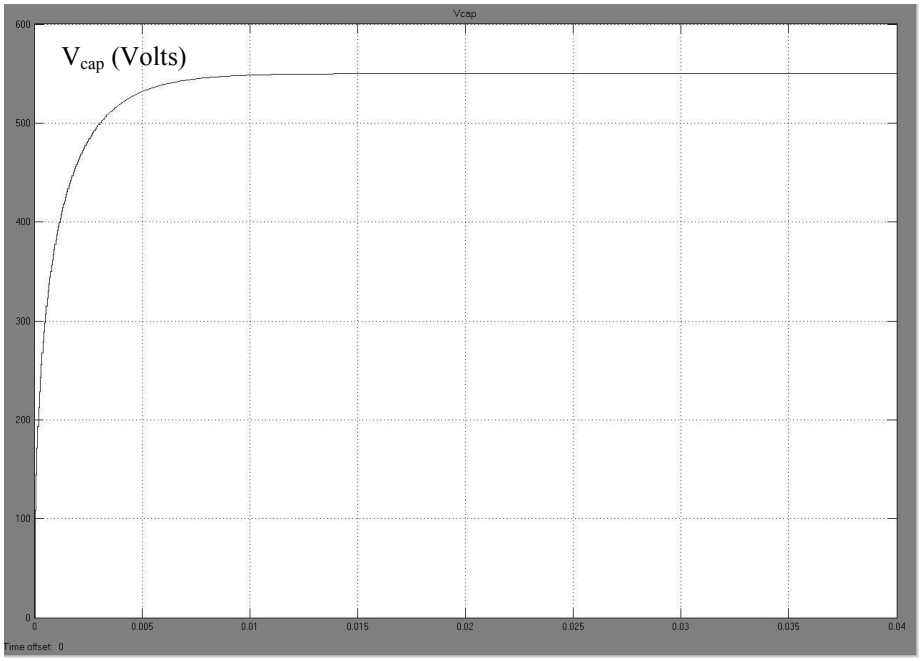


Fig 4.16: *Vcap response for fig 4.15*

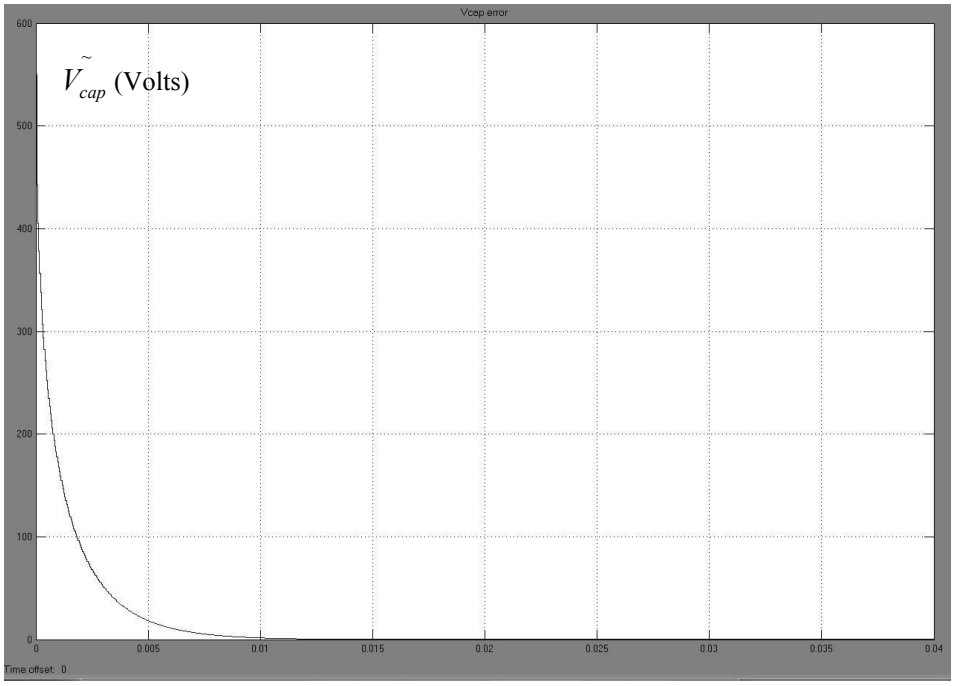


Fig 4.17: *Vcap error* ($\tilde{V}_{cap}$) *response for fig 4.15*

Comparing figures 4.13 with 4.16 and 4.14 with 4.17 it can be seen that the responses obtained are very similar i.e. the transient in both cases has virtually died away to an insignificant level in 10ms. Therefore the use of equation 4.10 to assess the inner loop transient for practical values of λ is acceptable for the non-linear condition. However it has been found that for extreme values of λ expression 4.10 is not so accurate. For example, it has been found through simulation that by varying λ and keeping all other parameters fixed, the given system results in a boundary between non-oscillatory transient decay and oscillatory decay for λ = 28500 rather than λ = 57300 (eqn {4.10}) when using the linearising approximation, however this is of no concern since (as already stated) the use of such large values of λ are not practical.

4.3.3 Combining the inner and outer loops (λ > 0)

In this section the inner and outer loops are brought together to provide a simulation of the system from a Real Power Flow perspective (i.e. ignoring all reactive and harmonic current components).

The following equations will be required for the inner loop:

Eqn 4.7

$$\Delta E(z_{2T}) = z_{2T}^{-1} I_{f1RMS}(z_{2T}).V_{sRMS}.(2T)$$

Eqn 4.4

$$\left(I_{f1refRMS}(z_{2T}) - I_{f1RMS}(z_{2T})\right) + C\lambda\left(V_{capconst}(z_{2T}) - V_{cap}(z_{2T})\right) = 0$$

Eqn 4.11

$$\Delta E(N2T) = \frac{1}{2} C\left(V^2{}_{cap}(N2T) - V^2{}_{cap}((N-1)2T)\right)$$

The following equations are required to complete the outer loop (for K control):

Eqn {4.5}:

$$K(z_\tau) = z_\tau^{-1} K(z_\tau) - \frac{\Delta E(z_\tau)}{\tau.V_s^2}$$

Eqn {4.3}: written in terms of z_τ:

$I_{f1refRMS}(z_\tau) + I_{L1RMS}(z_\tau) = K(z_\tau).V_{sRMS}$ -----{eqn 4.12}

Eqn {4.11} (but used in the outer loop as a sampled function of τ):

$$\Delta E(N\tau) = \frac{1}{2} C\left(V^2{}_{cap}(N\tau) - V^2{}_{cap}((N-1)\tau)\right)$$ -----{eqn 4.13}

Notes:
Eqn {4.11} for the inner loop describes the average energy flow into and out-of the capacitor. Eqn {4.13} describes the change in energy per source cycle and will be used in an attempt to control K.

In addition to the above equations the following additions will be made:

A switch gain function will be added in the path for I_{f1RMS} (see discussion of g in section 4.2) to simulate a lossy switching system. Also to add some non-linearity to the switching system, the signal $\tilde{V}_{cap}\,\lambda C$ is subjected to a slight offset (see section 3.1.7) by applying the following function:

Output= u+0.5*sgn(u) (for input u):

Plot of non-linear function to offset $\tilde{V}_{cap}$:

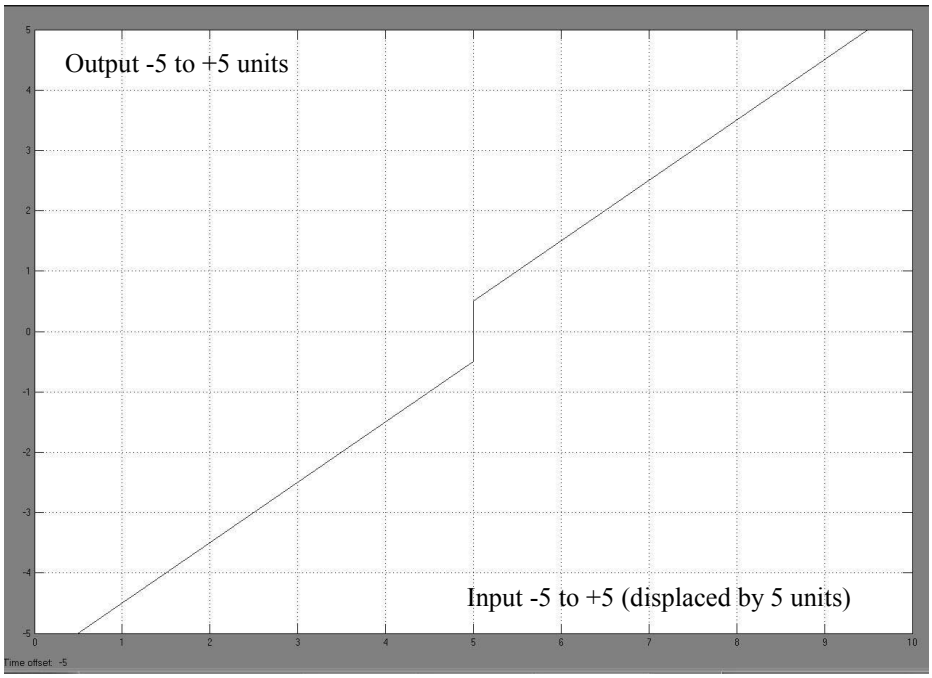


Fig 4.18*: non-linearity introduced into the path of Vcap error. (Input offset of -5 units shown)*

This function will add +/- 0.5 A of uncertainty to the value of I_{f1RMS} in the steady state.

Furthermore, a saturation function (set to upper limit = 1 and lower limit = 0) will be placed in the K signal to prevent K exceeding these limits (a negative K is unacceptable).

The combined inner and outer control loops:

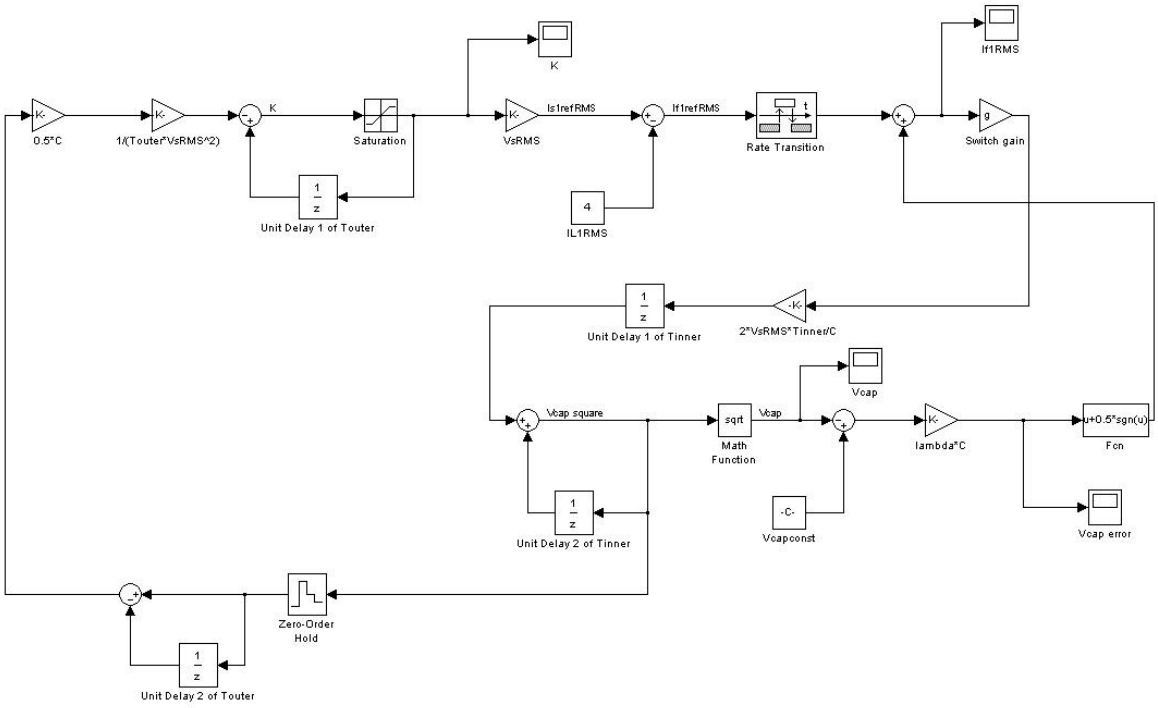


Fig 4.19*: The combined Inner and Outer Real Power signal flow loops*

In order to link together the inner loop sampled at 2T and the outer loop sampled at τ, a rate transition block (slow to fast) is included and a "Zero-Order Hold" (handling the fast to slow) is included.

The following values are used:

C = 1000μF
Lambda = 1100
V_{sRMS} = 240
$V_{capconst}$ = 550
I_{L1RMS} = 4
g = 0.95
Initial value of V_{cap} = 0 (set "Unit Delay1 of Tinner" = 0 and "Unit Delay2 of Tinner" = 0)
Unit delays set to Tinner where Tinner = 2T = 40μs and Touter = 20ms.
Fixed step discrete solver used.
Initial value of K set to 0.05 i.e. the initial value of "Unit Delay 1 of Touter" (the initial target value used in the APF switch controller "switch_control3a.m" - see Appendix D).

With I_{L1RMS} = 4A the ideal target value for K should be 0.01666

The simulation results are as follows:

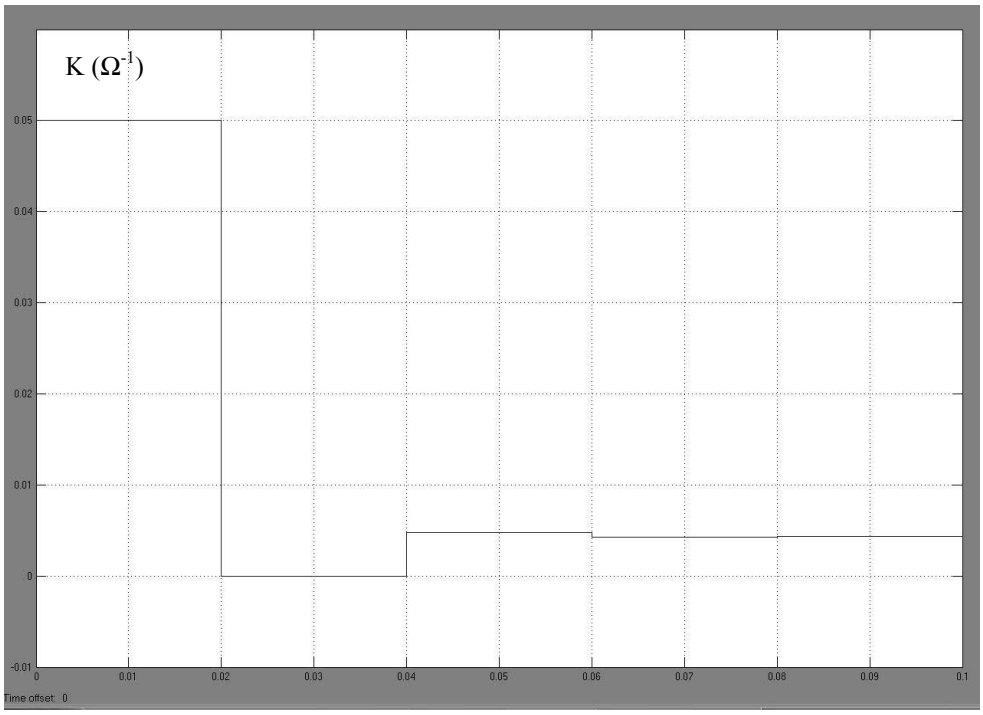


Fig 4.20*: Plot of K for fig 4.19 (K(0) = 0.05, $V_{cap}(0) = 0$, $\lambda = 1100$)*

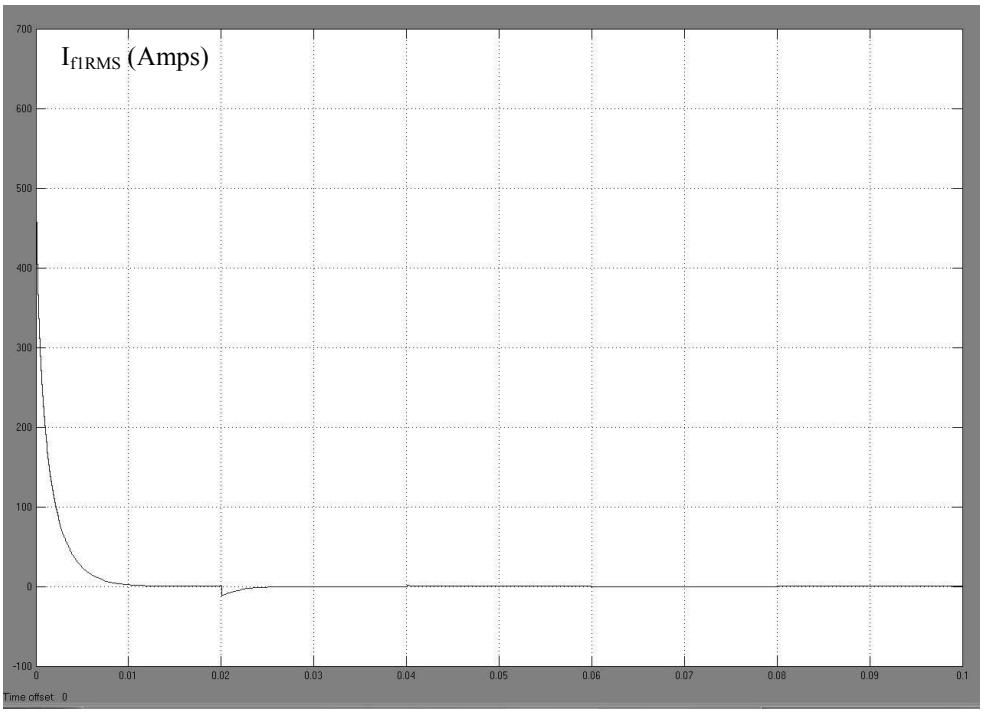


Fig 4.21*: Plot of I_{f1RMS} for fig 4.19 (K(0) = 0.05, $V_{cap}(0) = 0$, $\lambda = 1100$)*

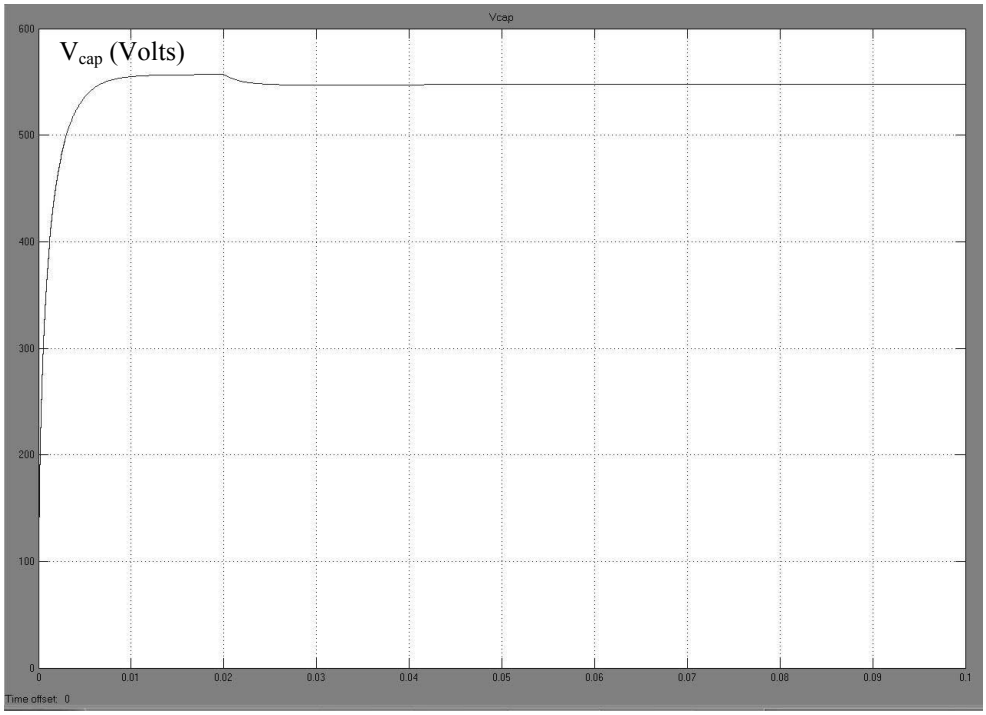


Fig 4.22*: Plot of V_{cap} for fig 4.19 (K(0) = 0.05, $V_{cap}(0) = 0$, $\lambda = 1100$)*

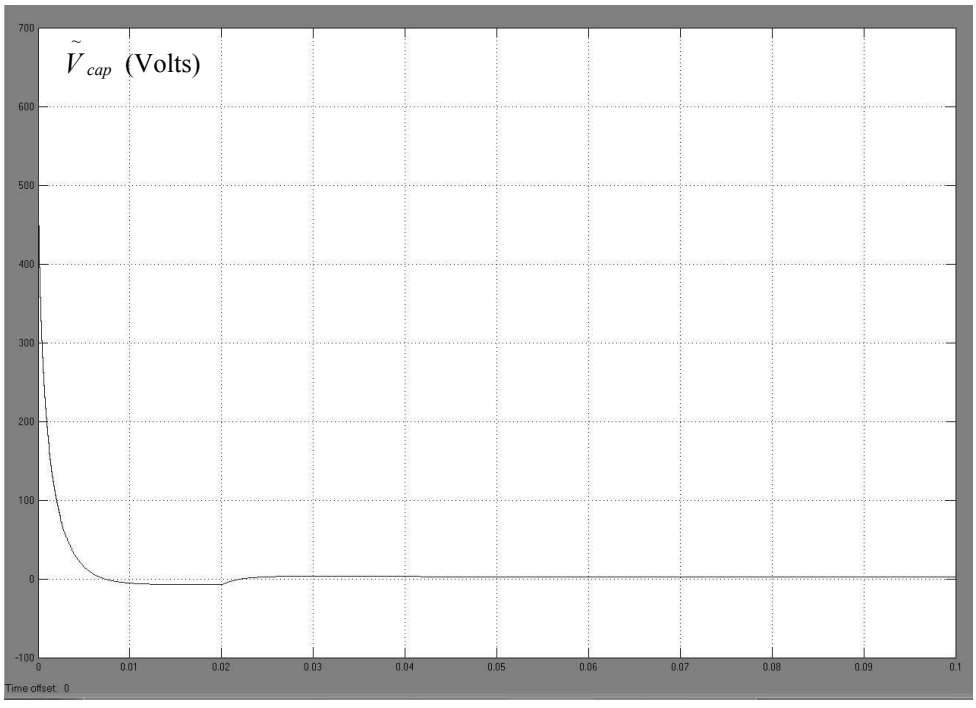


Fig 4.23*: Plot of $\tilde{V}_{cap}$ for fig 4.19 (K(0) = 0.05, $V_{cap}(0) = 0$, $\lambda = 1100$)*

The results indicate that K settles to a completely wrong value (= 4.336 * 10^{-3}). The fast settling time of V_{cap} has effectively removed the feedback signal in the outer loop. In fact K is completely dependent on initial conditions. V_{cap} settles to a steady value but there is a steady state error as indicated in Fig 4.23 and I_{f1RMS} reaches zero (as

required) indicating that no more energy is flowing into or out-of the capacitor. In practice, this APF solution would have failed to harmonically correct the source current.

If V^2_{cap} is given an initial condition of 250,000 (i.e. $V_{cap}(0) = 500V$) then a different set of plots is obtained. The initial condition of 250,000 is set into "Unit Delay 2 of Tinner".

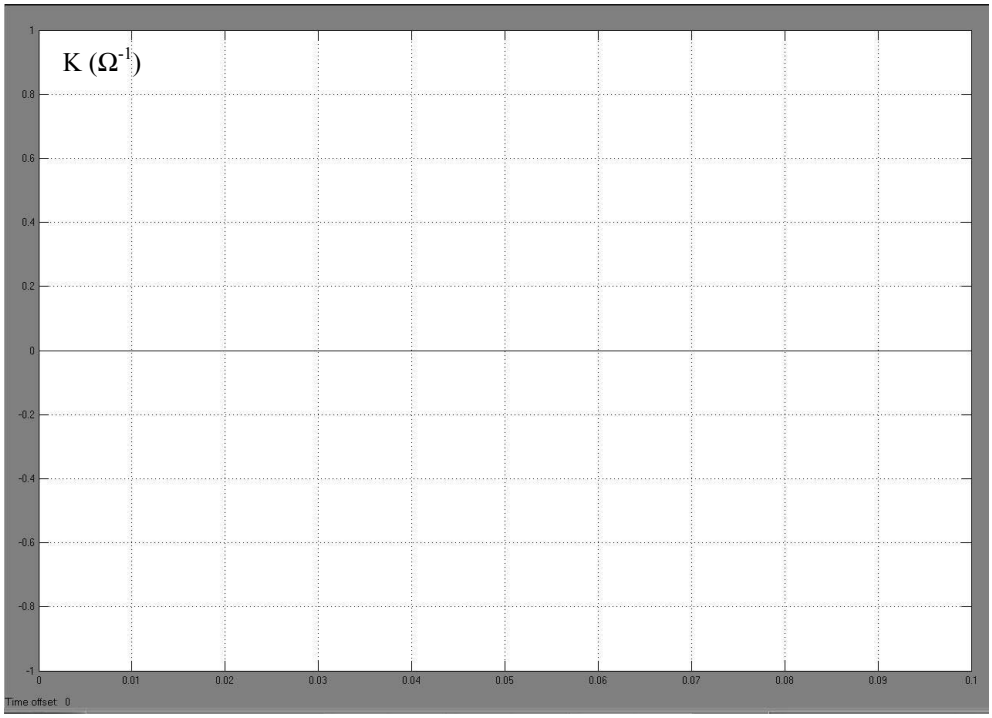
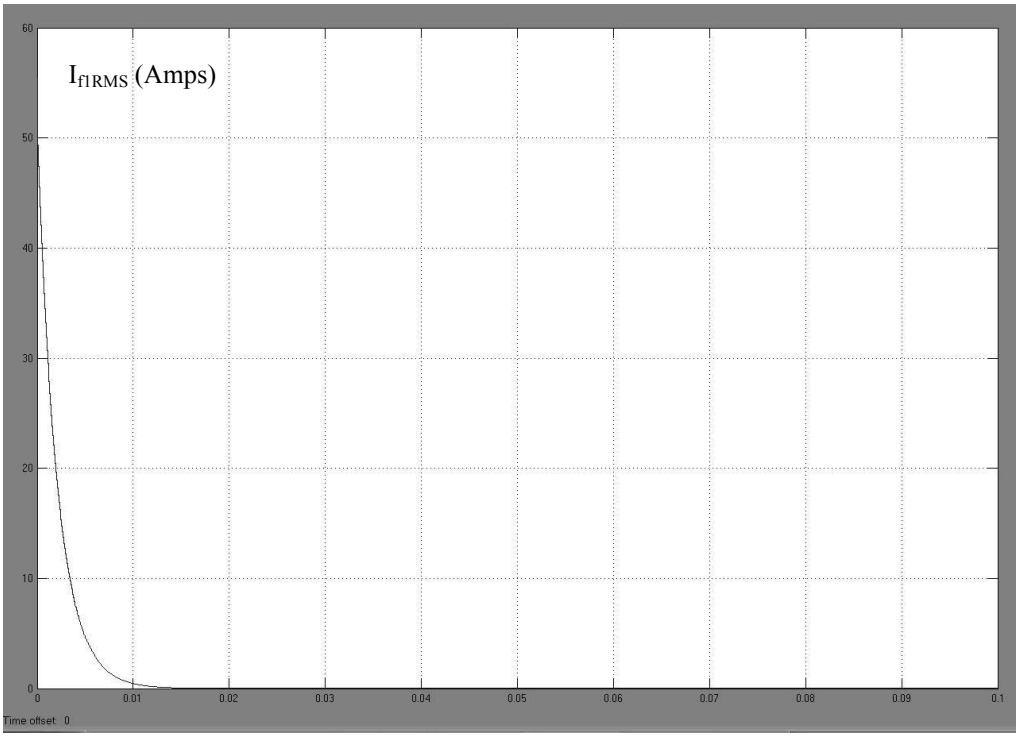
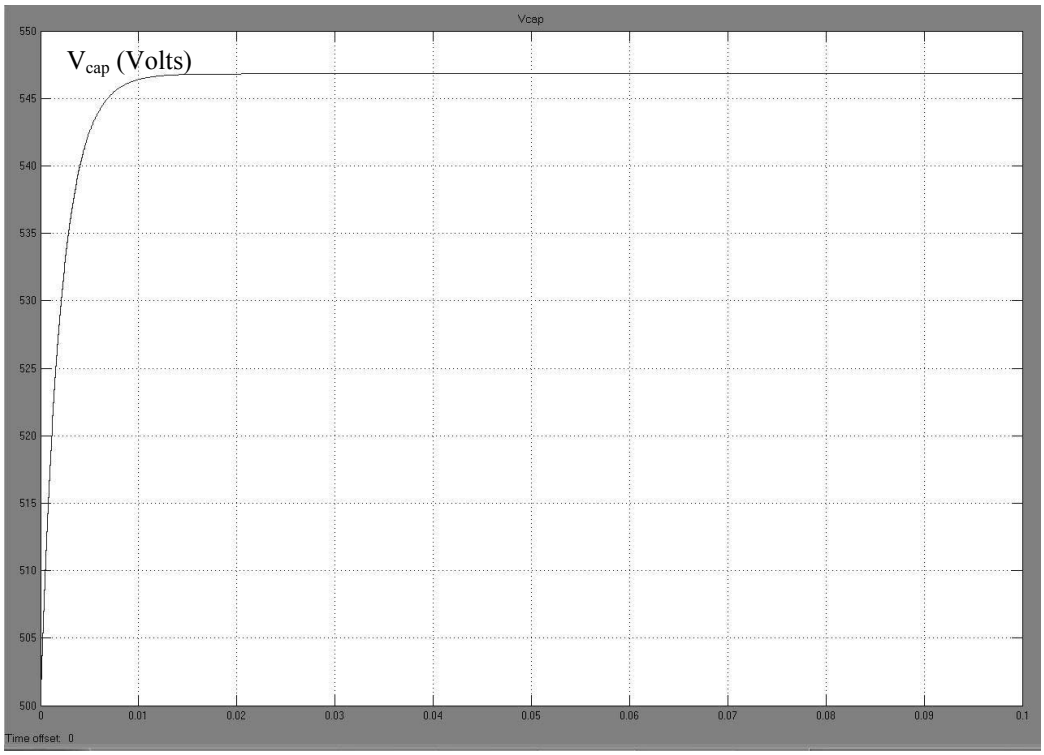


Fig 4.24*: A plot of K for fig 4.19 (K(0) = 0.05, $V_{cap}(0) = 500$, $\lambda = 1100$)*



secs

Fig 4.25*: A plot of I_{f1RMS} for fig 4.19 (K(0) = 0.05, $V_{cap}(0)$ = 500, λ = 1100)*



secs

Fig 4.26*: A plot of V_{cap} for fig 4.19 (K(0) = 0.05, $V_{cap}(0)$ = 500, λ = 1100)*

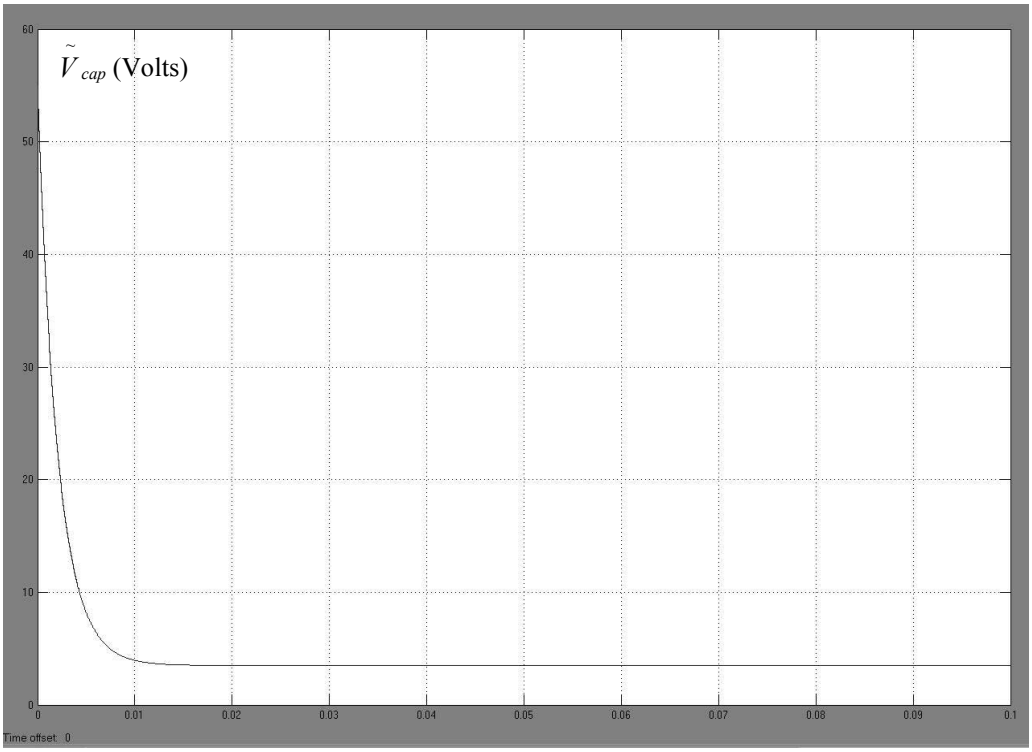


Fig 4.27*: A plot of $\tilde{V}_{cap}$ for fig 4.19 (K(0) = 0.05, $V_{cap}(0)$ = 500, λ = 1100)*

It can be seen that when V_{cap} is given an initial condition close to $V_{capconst}$, K is forced to saturate to zero from which it never recovers. Again I_{f1RMS} decays to zero (as required) and V_{cap} settles to a steady value; however there is a larger steady state error in V_{cap} (see Fig 4.27) since K is zero. As before, the practical APF would fail to correct harmonic distortion.

The following simulation investigates the effect of reducing λ.

Inner loop analysis provided an approximate transient delay rate governed by:

$\left(1-\frac{2T\lambda V_{sRMS}}{V_{capave}}\right)^{N}$ Setting λ (for example) to 200 and keeping all other parameters fixed at previous values results in a transient decay rate of 0.9965^{N}. When N = 500 (500*2T = τ = 20ms), the transient has decayed to 17.4%.

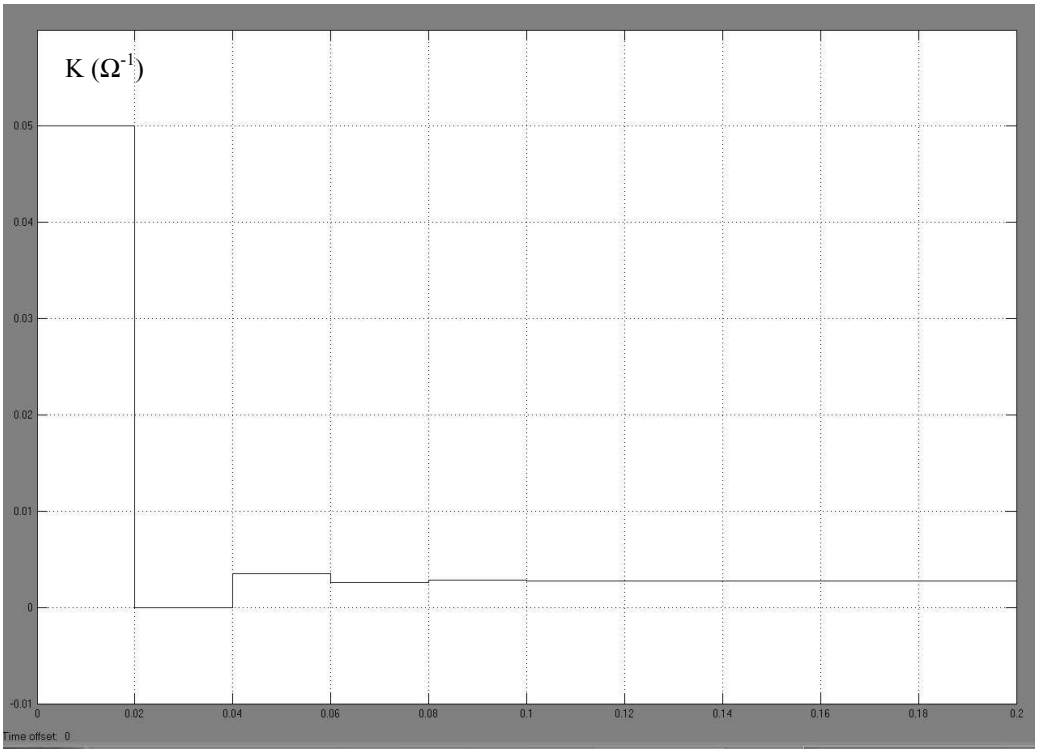


Fig 4.28: *A plot of K for fig 4.19 (K(0) = 0.05, $V_{cap}(0) = 500$, $\lambda = 200$)*

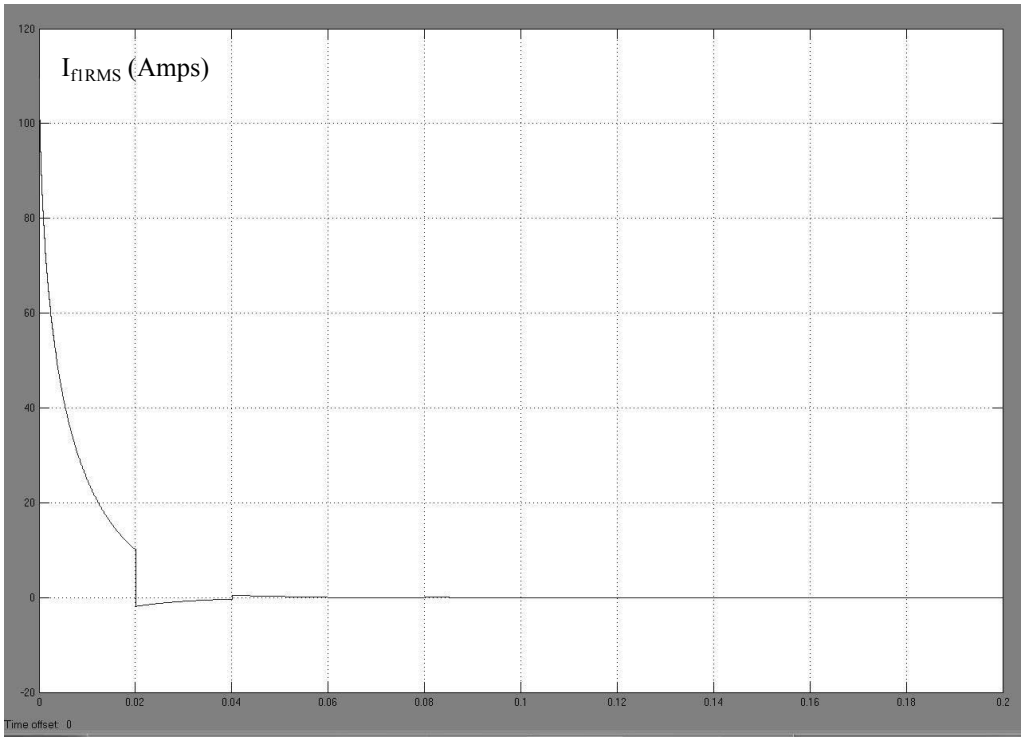


Fig 4.29*: Plot of I_{f1RMS} for fig 4.19 (K(0) = 0.05, $V_{cap}(0) = 500$, $\lambda = 200$)*

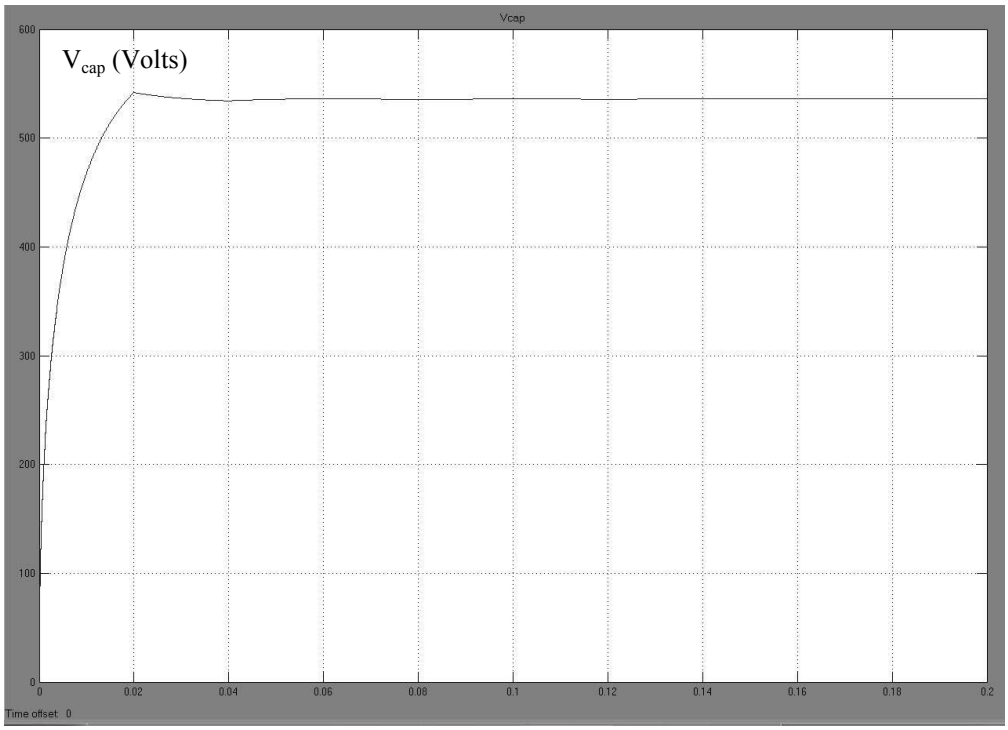


Fig 4.30: *A plot of V_{cap} for fig 4.19 (K(0) = 0.05, $V_{cap}(0)$ = 500, λ = 200)*

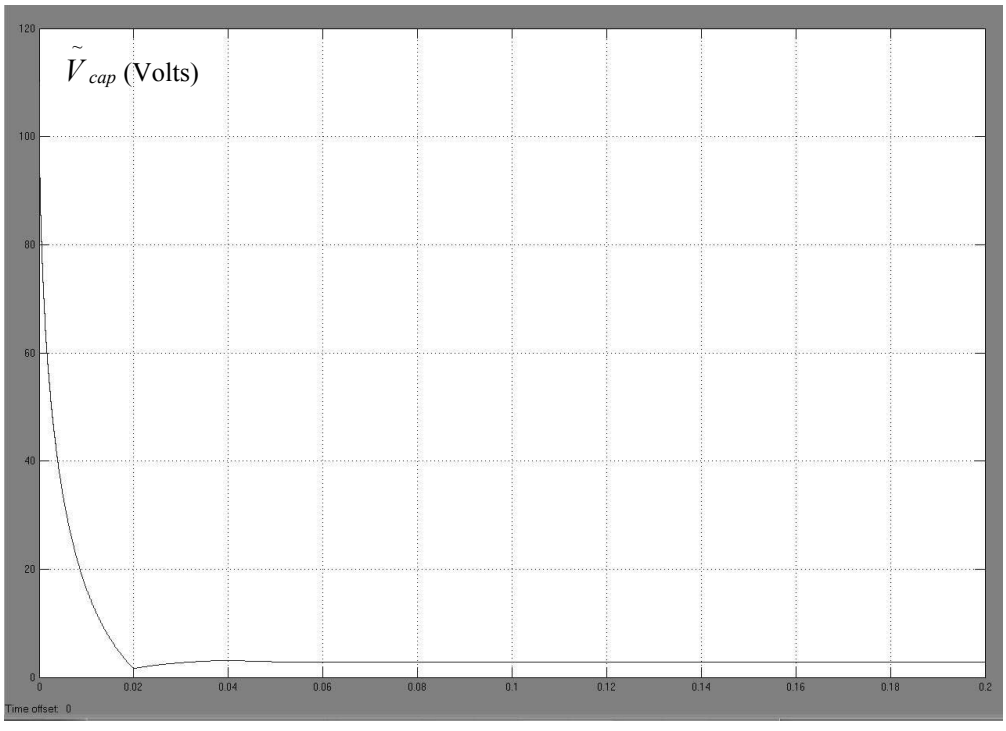


Fig 4.31*: A plot of $\tilde{V}_{cap}$ for fig 4.19 (K(0) = 0.05, $V_{cap}(0)$ = 500, λ = 200)*

With a reduced value of λ, V_{cap} takes longer to reach steady state (as expected from the result of section 4.3.1.2). I_{f1RMS} reduces to zero and there is a small steady state

error in V_{cap}. The effect in the outer loop is detrimental to K resulting in erroneous results (steady state K = 2.767 *10^{-3} instead of the required value of 0.01667).

In an attempt to correct the errors of K caused by the combining of the inner and outer control loops, an important modification will be made to the outer loop feedback and this is dealt with in the next section.

4.3.4 Combined the inner and outer loop with a modified feedback energy-difference signal in the outer loop

Section 4.3.3 illustrated conclusively that by adding the inner capacitor control loop (i.e. letting λ take on a positive value) prevents K in the outer loop from converging to the correct value. The outer loop will be modified in an attempt to correct this problem.

This modification is applied to eqn {4.13}. Instead of measuring the absolute energy change in the capacitor every period τ, the energy change is calculated with respect to the capacitor reference Voltage. This is exactly the method used in the APF MATLAB model control algorithm (see Appendix D, switch_control3a.m lines 42 and 55) which are executed when $\lambda > 0$.

As in section 4.3.3 the following equations are required for the inner loop:

Eqn {4.7}:

$$\Delta E(z_{2T}) = z_{2T}^{-1} I_{f1RMS}(z_{2T}).V_{sRMS}.(2T)$$

Eqn {4.4}:

$$\left(I_{f1refRMS}(z_{2T}) - I_{f1RMS}(z_{2T})\right) + C\lambda\left(V_{capconst}(z_{2T}) - V_{cap}(z_{2T})\right) = 0$$

Eqn {4.11}:

$$\Delta E(N2T) = \frac{1}{2} C\left({V_{cap}}^2(N2T) - {V_{cap}}^2((N-1)2T)\right)$$

The following equations are required to complete the outer loop (for K control):

Eqn {4.5}:

$$K(z_\tau) = z_\tau^{-1} K(z_\tau) - \frac{\Delta E(z_\tau)}{\tau . V_s^2}$$

Eqn {4.3}:

$I_{f1refRMS}(z_\tau) + I_{L1RMS}(z_\tau) = K(z_\tau).V_{sRMS}$

The new equation for outer loop feedback:

$$\Delta E(N\tau) = \frac{1}{2} C\left(V^2{}_{cap}(N\tau) - V_{capconst}{}^2(N\tau)\right) \qquad \text{-----\{eqn 4.14\}}$$

Notes:

Eqn {4.14} applies an energy feedback signal relative to the energy contained in the capacitor for a given V_{capave} where V_{capave} is the steady value of the step input $V_{capconst}$. The MATLAB APF model control algorithm (switch_control3a.m of Appendix D) uses $V_{caprefnew}$ as the reference Voltage (for $\lambda > 0$ in lines 42 and 55 of switch_control3a.m). $V_{caprefnew}$ is the sampled value of V_{capref} , which is a complex capacitor reference derived from I_{fref} together with a gating signal I_{fref_gate} (see table 3.5) but essentially consists of a reference level ($V_{capconst}$) with other terms containing the reactive and harmonic components. Since the analysis here is only concerned with the real power components (first harmonic components with +/-1 power factor) then $V_{caprefnew}$ is replaced with $V_{capconst}$ to obtain eqn {4.14}.

It was decided to remove the non-linear function (fig 4.18) from the inner loop (i.e. assume a near perfect switching function) since the loop dynamics are more complex than those investigated so far, and any additional uncertainty may lead to confusion. The updated combined inner and outer loop system is:

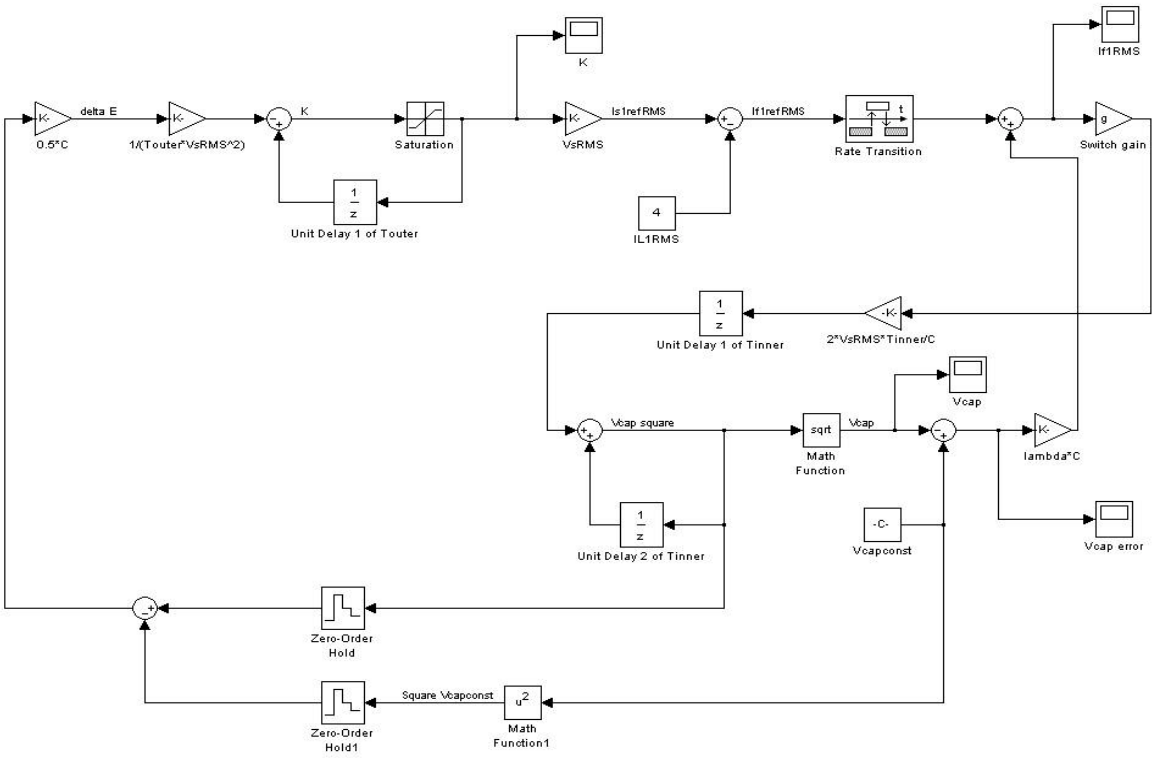


Fig 4.32*: The combined Inner and Outer Real Power signal flow loops with modified energy-difference feedback (given by eqn 4.14) in the outer loop*

The simulation of Fig 4.32 uses the same simulation parameters as in section 4.3.3. The following values are used:

C = 1000μF
lambda = 1100
V_{sRMS} = 240
$V_{capconst}$ = 550
I_{L1RMS} = 4
g=0.95

The rate transition block provides the interface from the outer loop (sampled at period τ) with the inner loop (sampled at period 2T). Blocks "Zero-Order Hold" and "Zero-Order Hold1" provide the interface form the inner loop to the outer loop.

The initial value of V_{cap} = 0 (set "Unit Delay 2 of Tinner" = 0 and "Unit Delay 1 of Tinner" = 0)
Unit delays set to Tinner where Tinner = 2T = 40μs and Touter = 20ms.
The fixed step discrete solver is used.
The initial value of K is determined by the initial value of "Unit delay 1 of Touter" and the outer loop feedback path. The initial value of "Unit Delay 1 of Touter" is set to 0.05 (the initial target value used in the APF switch controller switch_control3a.m" - see Appendix D).
With I_{L1RMS} = 4A the ideal target value for K should be 0.01666 (= 4/240).

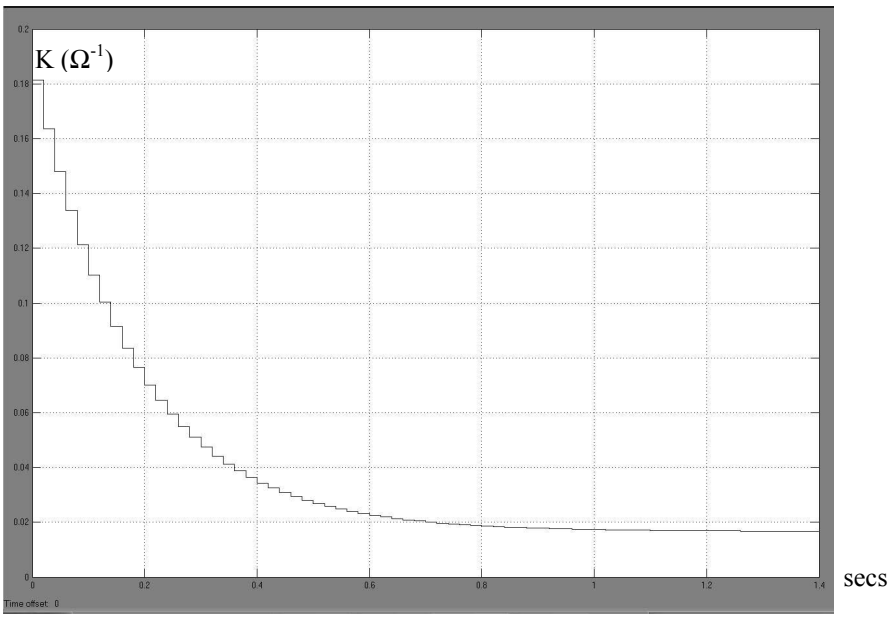


Fig 4.33*: A plot of K ($V_{cap}(0)$=0, λ = 1100) using a modified energy-difference feedback signal*

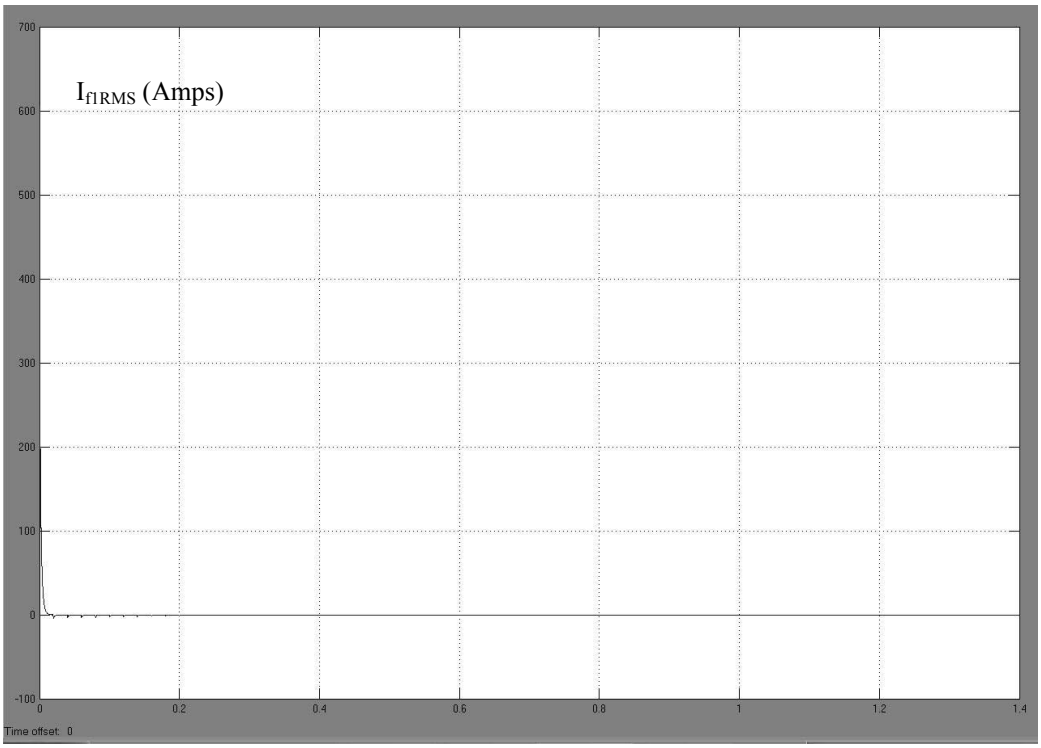


Fig 4.34*: A plot of I_{f1RMS} ($V_{cap}(0)=0$, $\lambda = 1100$) using a modified energy-difference feedback signal*

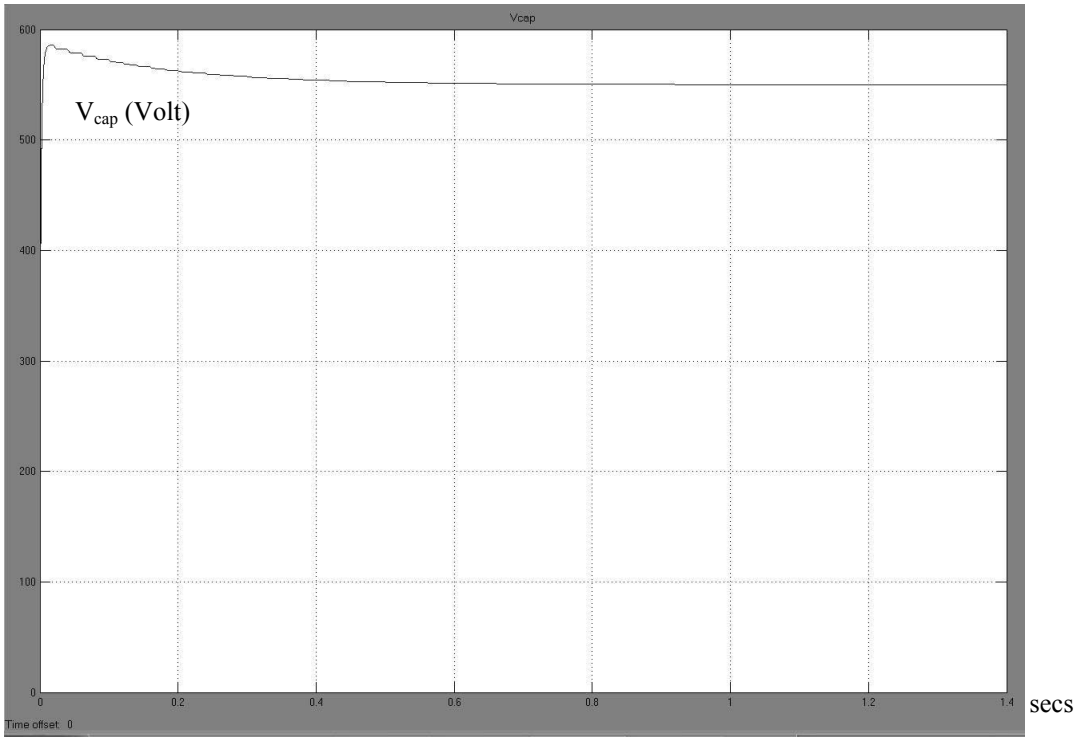


Fig 4.35*: A plot of V_{cap} ($V_{cap}(0)=0$, $\lambda = 1100$) using a modified energy-difference feedback signal*

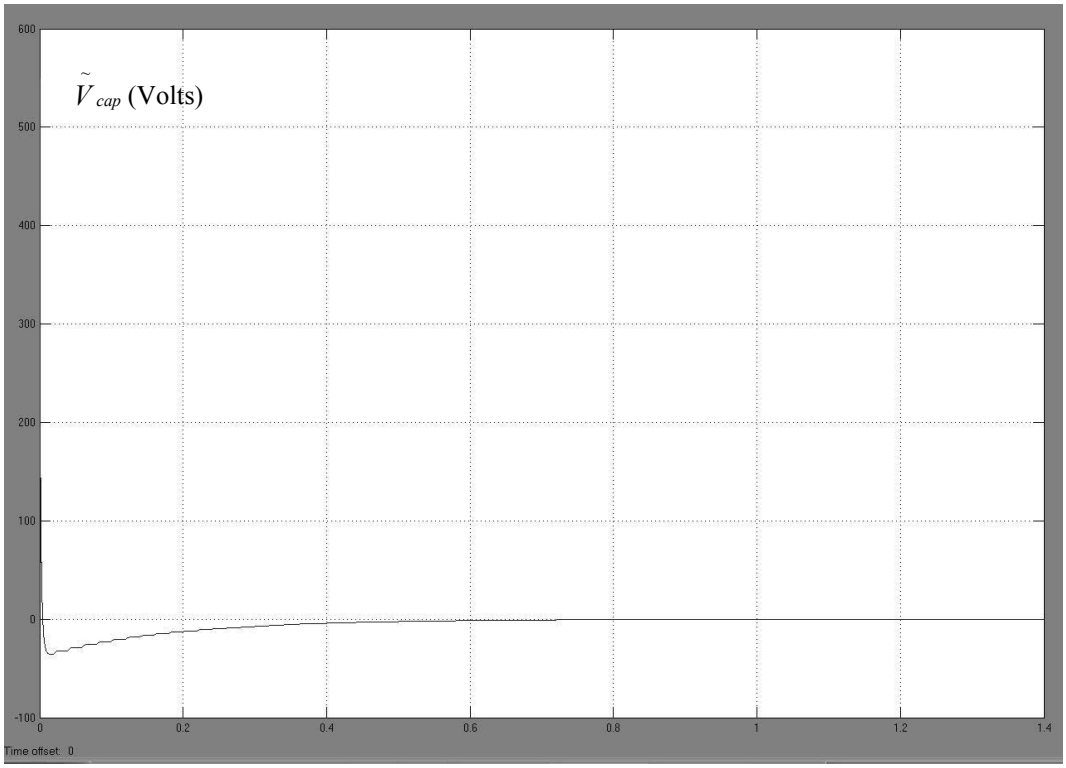


Fig 4.36*: A plot of $\tilde{V}_{cap}$ ($V_{cap}(0)=0$, $\lambda = 1100$) using a modified energy-difference feedback signal*

The above plots indicate that with the modified feedback (relative to $V_{capconst}$) V_{cap} *does* achieve the desired value and K *does* arrive at the correct value despite a relatively quick V_{cap} transient.

By comparing fig 4.33 with the K responses from the full APF model (see Appendix F for the K responses for Result Set 1b, 2b and 3b when $\lambda = 1100$) there can be seen a marked similarity.

The effect of the new feedback arrangement has allowed K to reach its target value with the transient decaying in about 1 sec. However, from a practical point of view this is an unacceptably long time.

A consequence of the new feedback arrangement that is not immediately obvious is that since a unit delay of τ (Touter) is missing from the outer loop (compare figs 4.32 and 4.19 [Unit Delay 2 of Touter]), then the outer loop is no longer stable on its own.

One of the advantages of using real power component analysis is the ability to investigate each loop separately within the system; the ability to reduce the control loop to reveal aspects that are otherwise hidden.

4.3.5 Combined Inner and Outer loops: Outer Loop Instability Investigation using the Modified Energy-Difference Feedback Signal

The previous section (4.3.4) showed how to obtain control of both V_{cap} and I_f using a modified energy-difference feedback signal given by eqn {4.14} and resulting in fig 4.32.

It is necessary to investigate the reason for such a long transient settling time for K in the response of fig 4.32. This can be achieved by removing the connection between the inner and outer loops.

The following loop takes figure 4.32 and removes the connection between the inner and the outer loop (a constant zero value and a terminator are required to prevent simulation warnings):

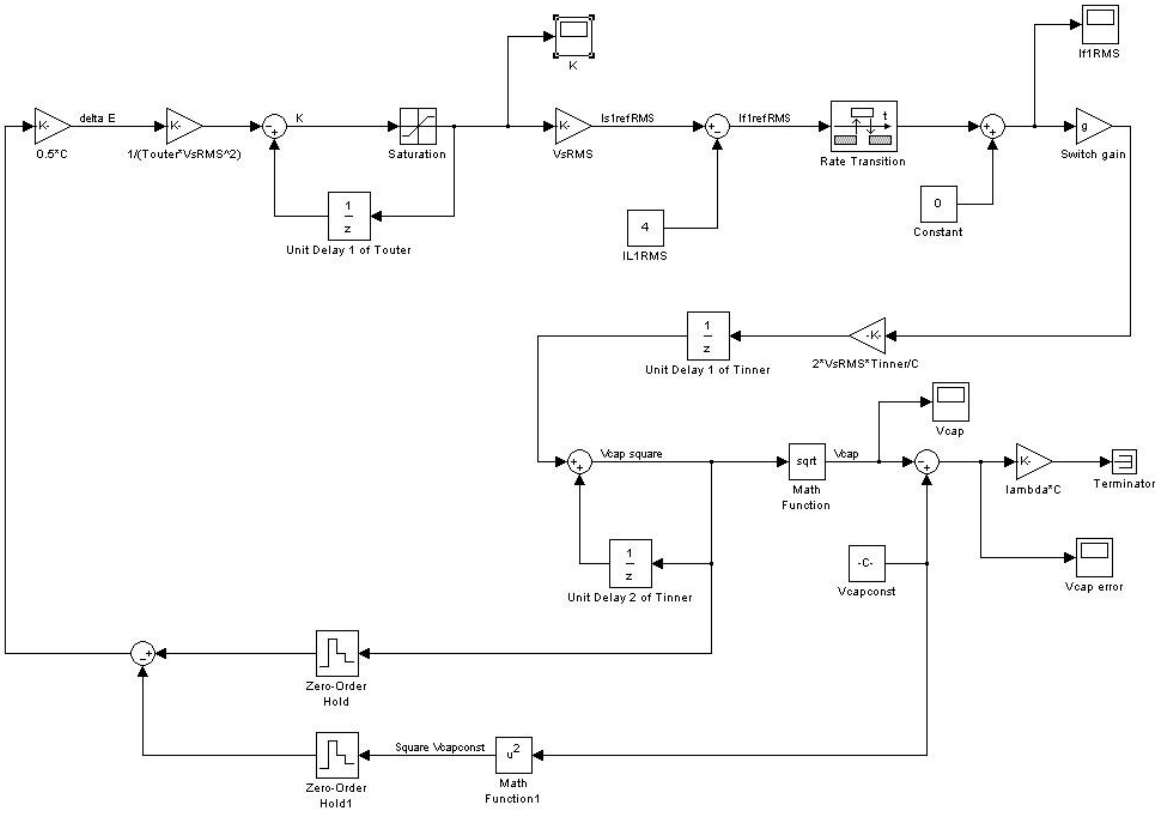


Fig 4.37*: Breaking the inner and outer loop of fig 4.32*

The same simulation parameters are used as in section 4.3.4

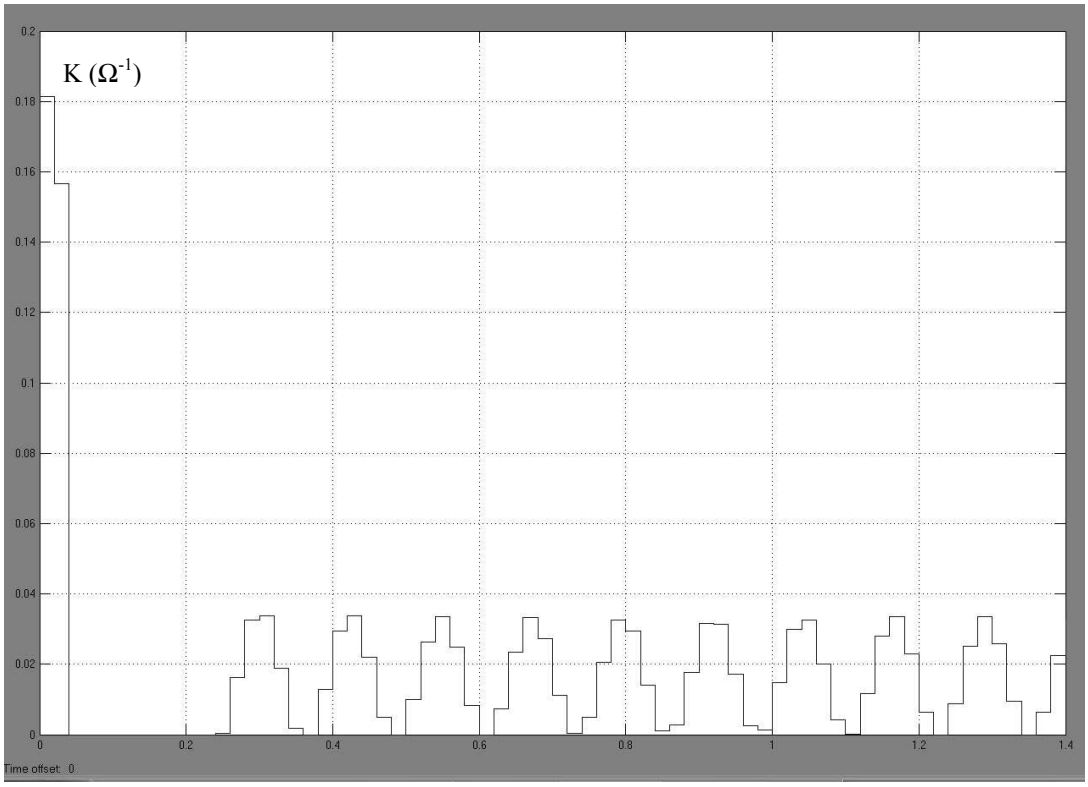


Fig 4.38*: K response ($V_{cap}(0)=0$, $\lambda = 1100$) for fig 4.37*

Fig 4.38 clearly indicates that the outer loop is unstable on its own and relies on the inner loop to maintain stability of K.

It is now clear that the use of sliding mode (i.e. the use of eqn. 4.4) to link the inner and outer loops creates problems with regard to system performance, in particular the stabilisation of K.

Apart from the problems of bandwidth sharing due to sliding control and the associated larger errors in the state variables prior to reaching steady state the problems are due to:

- The use of a capacitor reference to derive the energy difference to create $\tilde{x}$ (i.e. $\tilde{V}_{cap}$) variable of the sliding surface which in turn interferes with the iteration to converge to the correct value of K
- The use of a capacitor reference in the outer loop instead of the delayed actual capacitor Voltage results in the removal of the feedback delay in the outer loop causing outer loop instability
- Outer loop stability relies on the inner loop connection

However, the responses analysed and presented in section 4.2 (when $\lambda = 0$) looked very promising with regard to the control of I_f and deserve further consideration. Building on the knowledge gained form the Real Power Flow analysis technique it is possible to construct a system that achieves the goals of I_f and V_{cap} control and have acceptable and well defined dynamics. The sliding control will be reduced to zero order ($\lambda = 0$) i.e. the capacitor error Voltage will be removed from the switching space and a new concept of "energy compensation" will be used.

4.4 Control of both I_f and V_{cap} using the outer loop and "Energy Compensation"

Section 4.4 and associated sub-sections describes a method of using the outer loop to control both K (and hence I_f) and also V_{cap} and avoid the problems associated with linking the inner loop via the sliding surface for $\lambda > 0$ (eqn. {4.4}).
It is possible however, to control both I_f and V_{cap} while $\lambda = 0$. When $\lambda = 0$ all of the switching bandwidth is focussed onto forcing the error of I_f to zero. The Energy Compensation method ensures that in subsequent periods of τ following a load change, K is updated to a new value which ensures sufficient real power flow into the APF to keep the average value of $V_{cap} = V_{capave}$. K finally settles to a steady state value that allows only the real power component of the load current to be taken from the source.
The Energy Compensation method compares the energy stored in the capacitor at the sample instant with the energy needed for a given average capacitor Voltage and uses this additional "compensating" energy component to modify eqn. 4.13.

Outline of section 4.4
Section 4.4.1 provides the preparatory theory and develops the Real Power Flow control loop.
Section 4.4.2 investigates the system response using the Real Power Flow method when the compensating energy attenuation (ε) = 1.
Section 4.4.3 develops the theory of the Energy Compensation method by considering the equivalent system sampled at period τ. This allows a general expression to be derived for the system response of K in terms of the Energy Compensation Attenuation (ε) and the switching system gain (g).

Section 4.4.4 applies the simplification of considering the system all sampled at period τ to the general expression for K to analytically derive the ideal response for K to a step change in load.

4.4.1 Developing the Real Power Flow Control Loop incorporating Energy Compensation

The sliding function is reduced to zero order (i.e. λ) is set to zero. This breaks the feedback link between the inner and outer loops.
Re-writing eqn {4.14} as used in section 4.3.4:

$$\Delta E_{comp}(N\tau) = \frac{1}{2}C\left(V^2{}_{cap}(N\tau) - V^2{}_{capconst}(N\tau)\right) \qquad \text{-----\{eqn 4.15\}}$$

$\Delta E_{comp}(N\tau)$ *is now used as an additional compensating energy- difference component*.

Modifying eqn {4.1} and writing as a difference equation in terms of sample time τ, the new control equation in the outer loop becomes:

$$K(N\tau) = K((N-1)\tau) - \frac{1}{\tau V_{sRMS}^2}\left(\Delta E(N\tau) + \varepsilon \Delta E_{comp}(N\tau)\right) \qquad \text{-----\{eqn 4.16\}}$$

ε is a gain constant that allows investigation of the optimum amount of energy compensation to be used in the control loop.
$\Delta E(N\tau)$ in the outer loop, is the energy difference sampled at period τ and (similar to eqn {4.11}) takes the form:

$$\Delta E(N\tau) = \frac{1}{2}C\left(V^2{}_{cap}(N\tau) - V^2{}_{cap}((N-1)\tau)\right) \qquad \text{-----\{eqn 4.17\}}$$

Although the link between inner and outer loop has been broken, the inner loop still exists to transfer charge to the capacitor at the rate 1/(2T).

Re-stating eqn {4.11} for the inner loop:

$$\Delta E(N2T) = \frac{1}{2}C\left(V^2{}_{cap}(N2T) - V^2{}_{cap}((N-1)2T)\right)$$

Additionally the following equation is required for the inner loop:
Eqn {4.7}:

$$\Delta E(z_{2T}) = z_{2T}{}^{-1} 2TV_{sRMS} I_{f1RMS}(z_{2T})$$

The following figure (4.39) uses Real Power signal flow to show the control loop which controls K, V_{cap} and I_f by using Energy Compensation in the outer loop:

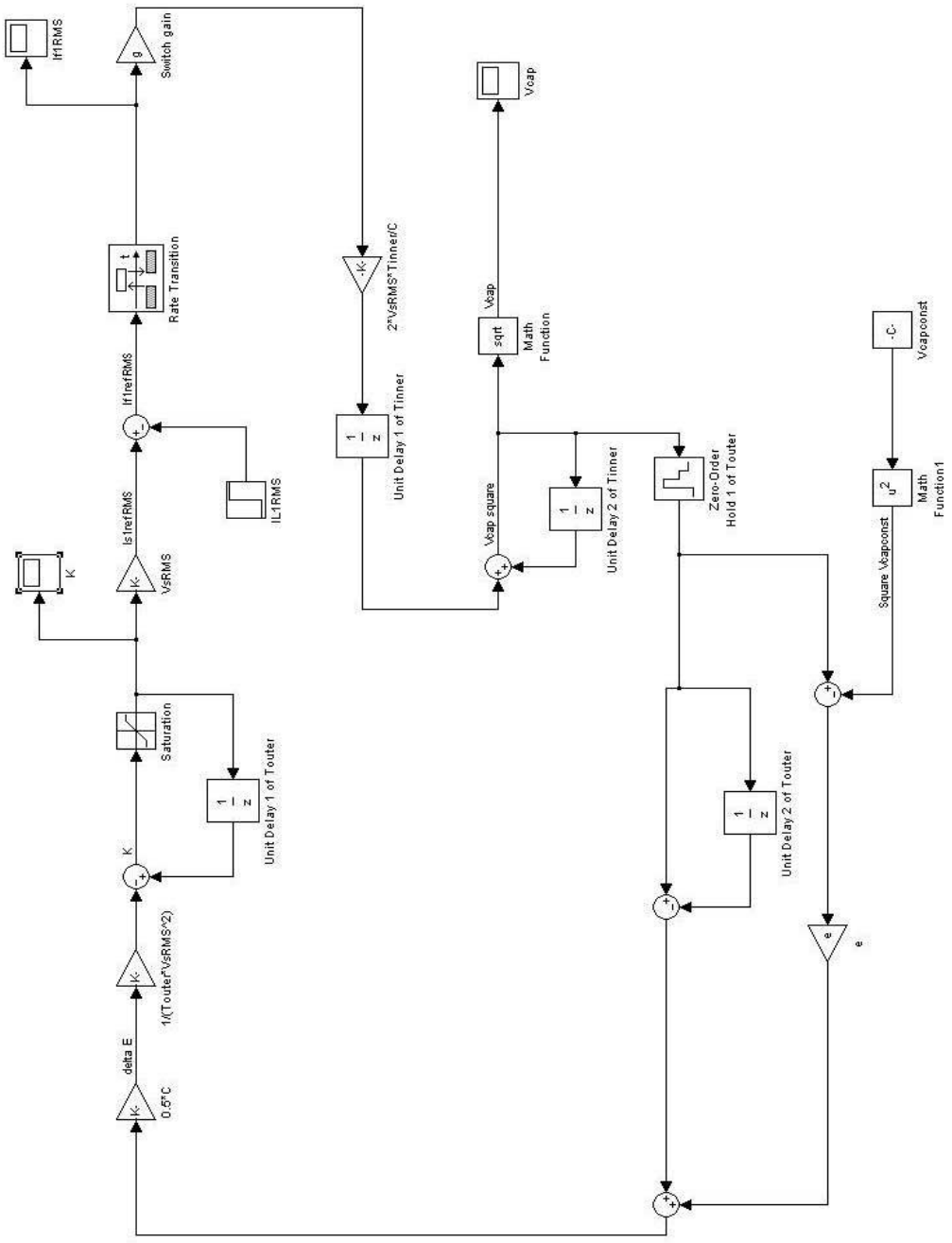


Fig 4.39*: Using "Energy Compensation" in the outer loop to control K, V_{cap} and I_f*

(Note that fig 4.39 uses symbol "e" instead of ε).

4.4.2 Real Power Flow Simulation of the APF using Energy Compensation with ε = 1

This section investigates the response of fig 4.39 with ε = 1 under ideal conditions (i.e. assume that the switch gain g = 1).

The following values are used for simulation:

- C = 1000μF
- lambda = 1100
- V_{sRMS} = 240
- $V_{capconst}$ = 550
- g = 1 (assume no loss in the APF switching system)
- Unit delays set to Tinner where Tinner = 2T = 40μs and Touter = 20ms = τ
- Fixed step discrete solver used

Since the initial target value of K used in the APF switch controller (see Appendix D) is 0.05, the initial value of "Unit Delay 1 of Touter" was set to 0.05.

Initial value of V_{cap} = 0 (set "Unit Delay 2 of Tinner" = 0)

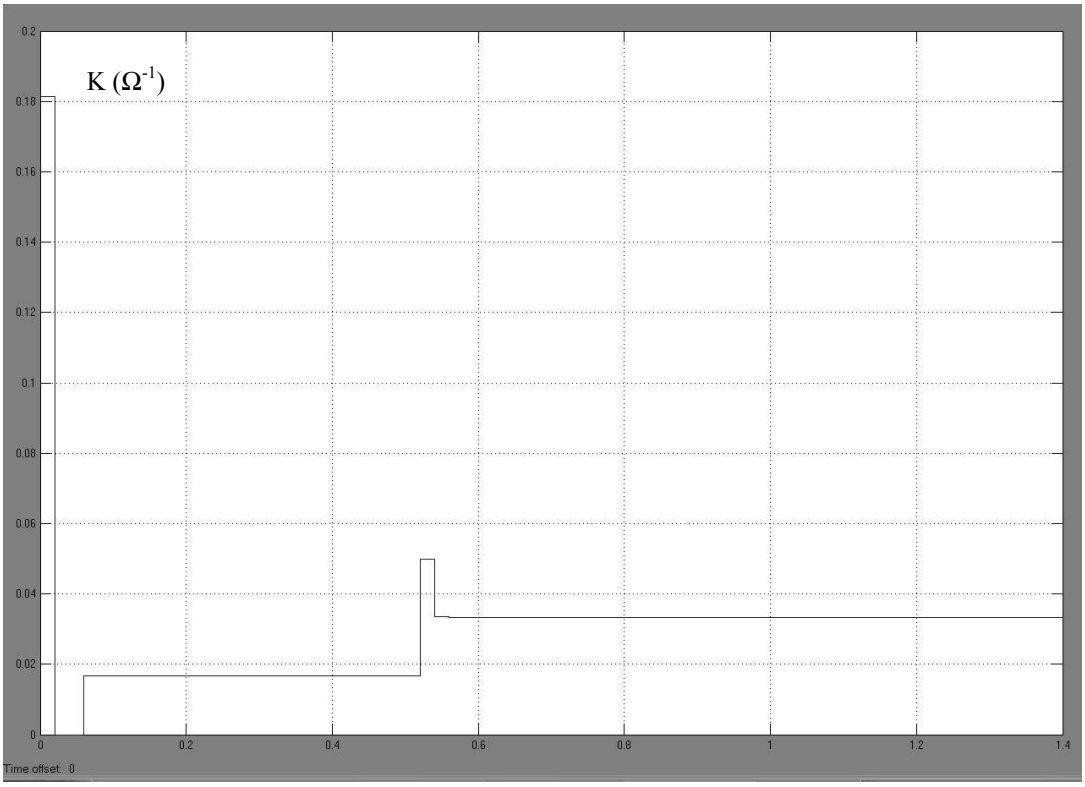
Gain ε (e in fig 4.39) = 1

I_{L1RMS} uses a step generator set to 4 at t = 0 and 8 at t= 0.5. This allows a transient to be observed after the capacitor has reached 550V

The simulation should resolve the first target value for K as 0.01666 (= 4/240) and at 0.5 s a target value for K as 0.0333 (8/240).

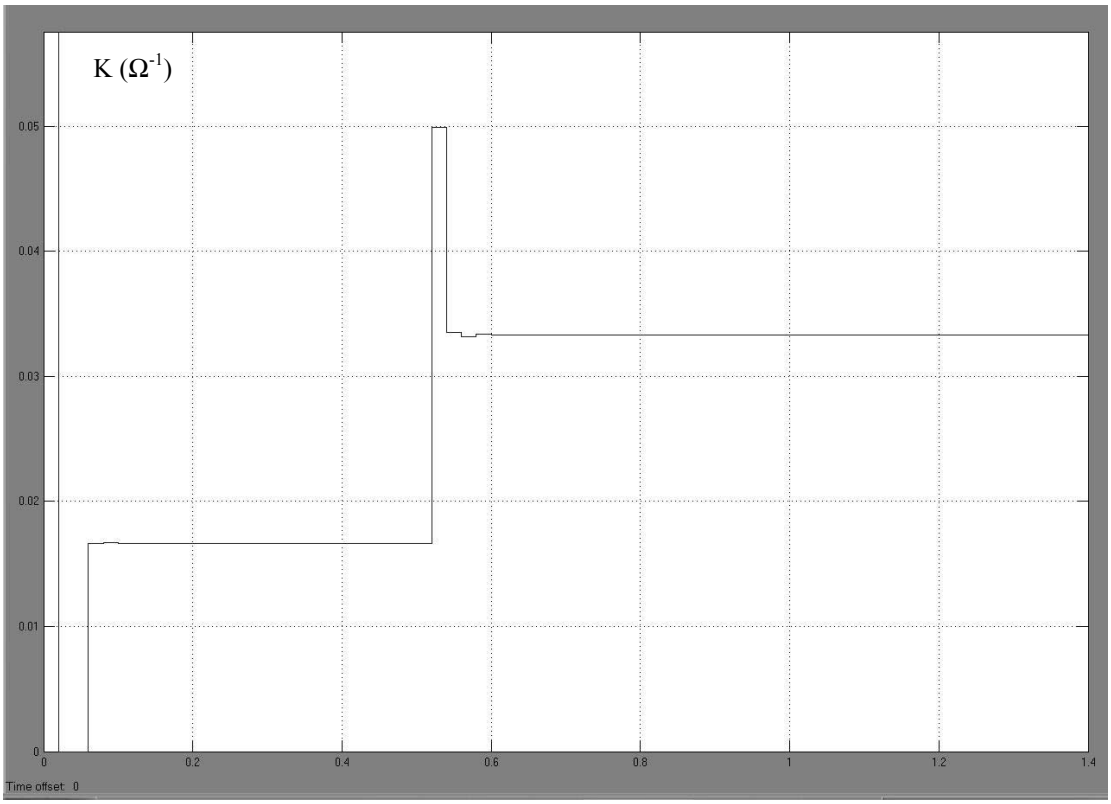
Since the response of the loop is now dependent on two energy components it was decided to simplify the loop by setting g to 1. The dynamics of the outer loop as they depend on g with one energy component was thoroughly investigated in section 4.2. It will be also be necessary to investigate the dynamics due to the additional compensating energy component as it depends on ε. This is left to the following section.

Results of simulation:



secs

Fig 4.40*: Plot of K for fig 4.39*



secs

Fig 4.41: *Expanded plot of K for fig 4.39*

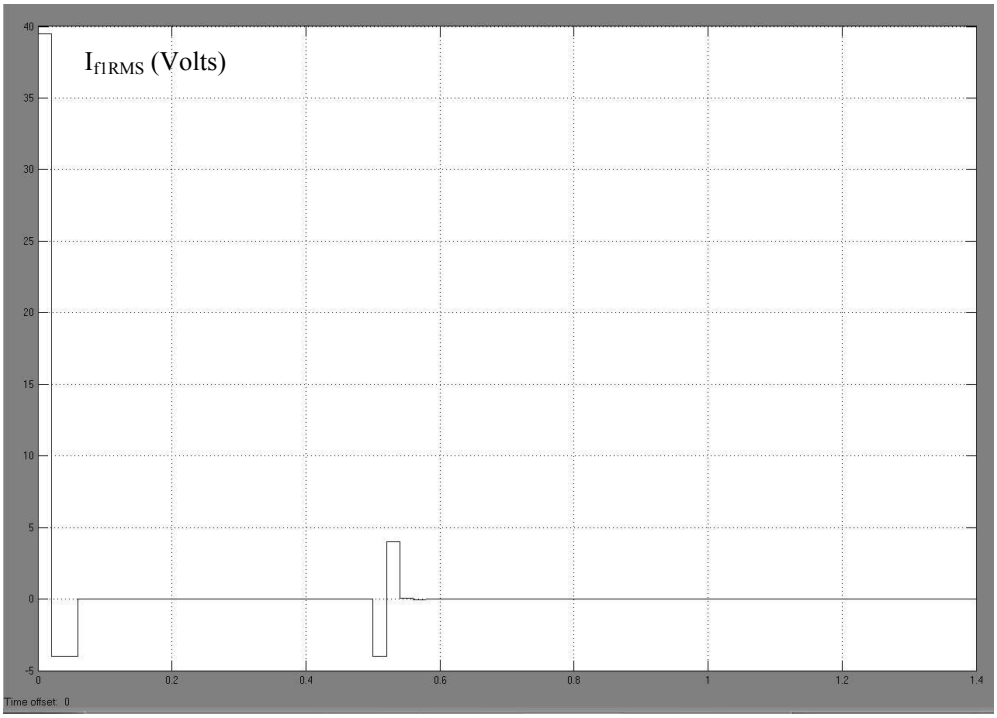


Fig 4.42*: Plot of I_{f1RMS} for fig 4.39*

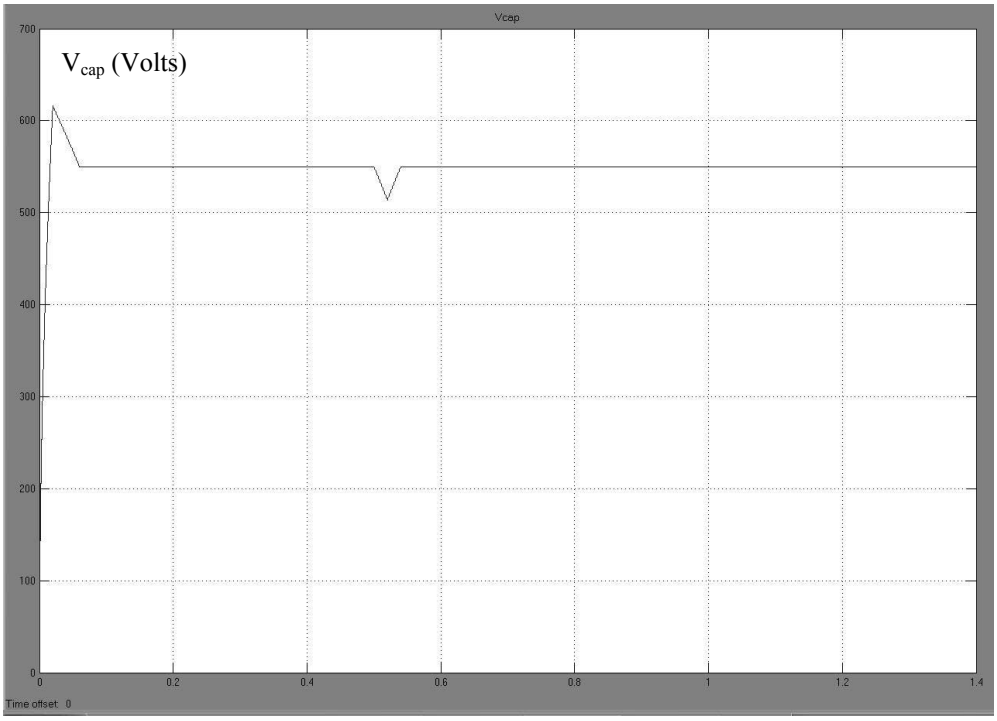


Fig 4.43*Plot of V_{cap} for fig 4.39*

The results indicate that K reaches its target value of 0.01666 and then of 0.0333 in about two periods of τ after the step change in load. I_{f1RMS} reaches zero after two periods of τ and V_{cap} deviates from its target value for only two periods of τ.

The response from this system is as near optimum as can be expected. It would not be possible to improve on this system using the discrete approach since there will always be a delay of τ to correct K owing to the fact that the capacitor must be sampled once every period τ to obtain the energy feedback signal.

It is necessary to investigate how the dynamics depend on ε which is the carried out in section 4.4.3.

4.4.3 Real Power Flow Analysis of the APF dynamics using Energy Compensation with 0 < ε < 1

Before analysis can continue an intermediate step is required to remove the inner loop from fig 4.39 sampled at 2T. The system can then be written entirely as a function of z_τ. Since the capacitor is sampled at τ and the feedback connecting the inner loop to the outer loop is no longer connected (i.e. λ = 0 in the sliding function), then the inner loop can be replaced by a connection that transfers the equivalent amount of energy in period τ.

The following equations are required for this purpose:

Eqn {4.16}:

$$K(N\tau) = K((N-1)\tau) - \frac{1}{\tau V_{sRMS}^2}\left(\Delta E(N\tau) + \varepsilon \Delta E_{comp}(N\tau)\right)$$

Eqn {4.2} re-written in terms of z_τ:

$$\Delta E(z_\tau) = z_\tau^{-1} I_{f1RMS}(z_\tau).V_{sRMS}.\tau \qquad \text{-----\{eqn 4.18\}}$$

Eqn {4.12}:

$I_{f1refRMS}(z_\tau) + I_{L1RMS}(z_\tau) = K(z_\tau).V_{sRMS}$

Eqn {4.17}:

$$\Delta E(N\tau) = \frac{1}{2} C\left(V^2{}_{cap}(N\tau) - V^2{}_{cap}((N-1)\tau)\right)$$

Eqn {4.15}:

$$\Delta E_{comp}(N\tau) = \frac{1}{2} C\left(V^2{}_{cap}(N\tau) - V^2{}_{capconst}(N\tau)\right)$$

The following fig 4.44 shows the complete system using the Real Power Flow analysis principle and incorporating Energy Compensation with all parameters sampled at τ.

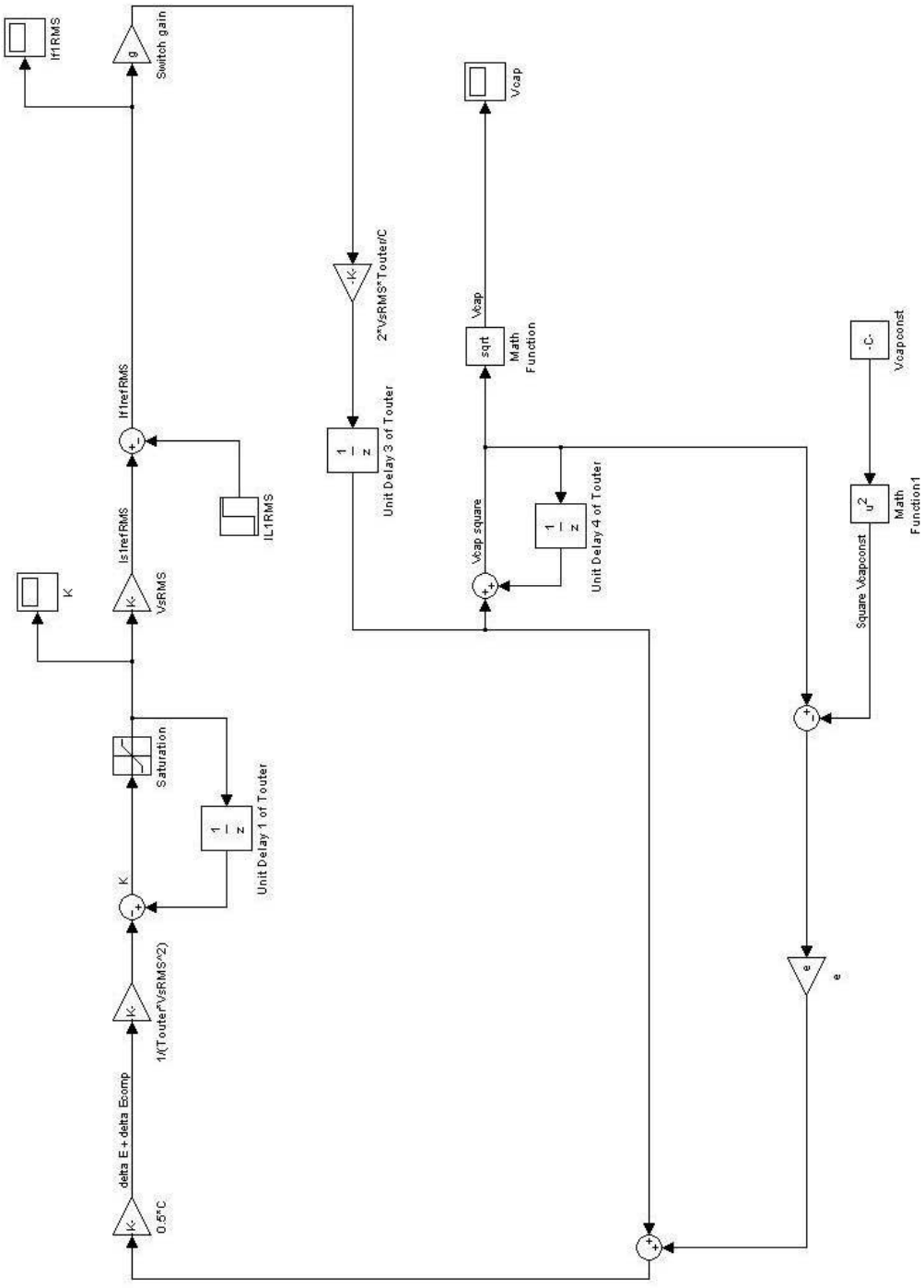


Fig 4.44*: A loop that is equivalent to fig 4.39 but is entirely sampled at* τ

Analysis of the loop response is now possible since the equivalent system is all sampled at τ.

Re-writing Eqn {4.17} as a function of z_τ:

$$\Delta E(z_\tau) = \frac{C}{2}\left(\mathrm{Z}\left(V^2{}_{cap}(N\tau)\right) - z_\tau^{-1}.\mathrm{Z}\left(V^2{}_{cap}(N\tau)\right)\right) \qquad \text{-----\{eqn 4.19\}}$$

Where $\mathrm{Z}\left(V^2{}_{cap}(N\tau)\right)$ is the Z transform of the non-linear squared function of V_{cap} sampled at τ.

and eqn {4.15} re-written (as a function of z_τ):

$$\Delta E_{comp}(z_\tau) = \frac{C}{2}.\left(\mathrm{Z}\left(V^2_{cap}(N\tau)\right) - \mathrm{Z}\left(V^2_{capconst}(N\tau)\right)\right) \qquad \text{-----\{eqn 4.20\}}$$

Where $\mathrm{Z}\left(V^2{}_{capconst}(N\tau)\right)$ is the Z transform of the squared function of $V_{capconst}$ sampled at τ.

Eqn {4.16} as a function of z_τ becomes:

$$K(z_\tau) = z_\tau^{-1}K(z_\tau) - \frac{1}{\tau V^2_{sRMS}}\left(\Delta E(z_\tau) + \varepsilon \Delta E_{comp}(z_\tau)\right) \qquad \text{-----\{eqn 4.21\}}$$

Eliminating $\mathrm{Z}(V^2{}_{cap}(N\tau))$ from eqns {4.19} and {4.20} and substituting into eqn {4.21} gives:

$$K(z_\tau)\left(1 - z_\tau^{-1}\right) = -\frac{1}{\tau V^2_{sRMS}}\left(\Delta E(z_\tau) + \frac{\varepsilon.\Delta E(z_\tau)}{\left(1 - z_\tau^{-1}\right)} - \frac{C\varepsilon}{2}.\mathrm{Z}\left(V^2_{capconst}(N\tau)\right)\right)$$

Substitute for $\Delta E(z_\tau)$ from eqn {4.18}:

$$K(z_\tau)\left(1 - z_\tau^{-1}\right) = -\frac{1}{\tau V^2_{sRMS}}\left(z_\tau^{-1} I_{f1RMS}(z_\tau).V_{sRMS}.\tau\left[1 + \frac{\varepsilon}{1 - z_\tau^{-1}}\right] - \frac{C\varepsilon}{2}.\mathrm{Z}\left(V^2_{capconst}(N\tau)\right)\right)$$

The concept of a switching gain as introduced in section 4.2 is specified as:

$$I_{f1RMS}(z_\tau) = g I_{f1refRMS}(z_\tau) \qquad \text{-----\{eqn 4.22\}}$$

Eliminate I_{f1RMS} using eqn {4.22} and use eqn {4.12} to eliminate $I_{f1refRMS}$ gives:

$$K(z_\tau)\left(1 - z_\tau^{-1}\right) = -z_\tau^{-1} g K(z_\tau)\left(1 + \frac{\varepsilon}{1 - z_\tau^{-1}}\right) + \frac{I_{L1RMS}(z_\tau).z_\tau^{-1} g}{V_{sRMS}}\left(1 + \frac{\varepsilon}{1 - z_\tau^{-1}}\right) + \frac{C\varepsilon}{2\tau V^2_{sRMS}}.\mathrm{Z}\left(V^2_{capconst}(N\tau)\right)$$

$$\therefore K(z_\tau)=\frac{I_{L1RMS}(z_\tau)g}{V_{sRMS}}\left(\frac{z_\tau(1+\varepsilon)-1}{(z_\tau-1)(z_\tau-1+g)+g\varepsilon z_\tau}\right)+\frac{C\varepsilon}{2\tau V_{sRMS}^2}Z\left(V_{capconst}^2(N\tau)\right)\frac{z_\tau(z_\tau-1)}{(z_\tau-1)(z_\tau-1+g)+g\varepsilon z_\tau}$$

-----{eqn 4.23}

Appling step inputs to both I_{L1RMS} and $V_{capconst}$:

$$I_{L1RMS}(z_\tau)=I_{L1CONST}\cdot\frac{z_\tau}{(z_\tau-1)} \qquad Z\left(V_{capconst}^2(N\tau)\right)=V_{capave}^2\cdot\frac{z_\tau}{(z_\tau-1)}$$

(Note that if $V_{capconst}$ is a step function from 0 to V_{capave} then $V^2_{capconst}$ is a step function from 0 to V^2_{capave})

This gives $K(z_\tau)$ as:

$$K(z_\tau)=\frac{I_{L1CONST}g}{V_{sRMS}}\frac{z_\tau}{(z_\tau-1)}\left(\frac{z_\tau(1+\varepsilon)-1}{(z_\tau-1)(z_\tau-1+g)+g\varepsilon z_\tau}\right)+\frac{C\varepsilon}{2\tau V_{sRMS}^2}V_{capave}^2\frac{z_\tau^{\,2}}{(z_\tau-1)(z_\tau-1+g)+g\varepsilon z_\tau}$$

-----{eqn 4.24}

4.4.4 Ideal analytical response for K for g = 1

It has already been noted that by placing g = 1 a simplified response can be obtained. Provided the switching system is efficient and the transistors are able to switch the demand current at the maximum sample rate, then this is a reasonable simplification. Therefore with g =1 eqn {4.24} simplifies to:

$$K(z_\tau)=\frac{I_{L1CONST}}{V_{sRMS}}\frac{(z_\tau(1+\varepsilon)-1)}{(z_\tau-1)(z_\tau-1+\varepsilon)}+\frac{C\varepsilon}{2\tau V_{sRMS}^2}V_{capave}^2\frac{z_\tau}{(z_\tau-(1-\varepsilon))}$$

$$\therefore K(z_\tau)=\frac{I_{L1CONST}}{V_{sRMS}}\left\{\frac{1}{(z_\tau-1)}+\frac{\varepsilon}{z_\tau-(1-\varepsilon)}\right\}+\frac{C\varepsilon}{2\tau V_{sRMS}^2}V_{capave}^2\frac{z_\tau}{(z_\tau-(1-\varepsilon))}$$

-----{eqn 4.25}

The Final Value Theorem gives:

$$\lim_{Z_\tau\to 1}(Z_\tau-1)K(Z_\tau)=\frac{I_{L1CONST}}{V_{sRMS}}$$

Inverse transform of eqn {4.25} for $0<\varepsilon<1$ and g = 1 gives

$$K(N\tau)=\frac{I_{L1CONST}}{V_{sRMS}}\{U((N-1)\tau)\}+\frac{I_{L1CONST}}{V_{sRMS}}\left\{\varepsilon(1-\varepsilon)^{N-1}U((N-1)\tau)\right\}+\frac{C\varepsilon V_{capave}^2}{2\tau V_{sRMS}^2}(1-\varepsilon)^N U(N\tau)$$

-----{eqn 4.26}

Inverse transform of eqn {4.25} for ε = 1 gives:

$$K(N\tau)=\frac{I_{L1CONST}}{V_{sRMS}}\{U((N-1)\tau)\}+\frac{I_{L1CONST}}{V_{sRMS}}\{\delta((N-1)\tau)\}+\frac{CV_{capave}^2}{2\tau V_{sRMS}^2}\delta((N)\tau)$$

-----{eqn 4.27}

Interpreting equations {4.26} and {4.27}:

First term: $\frac{I_{L1CONST}}{V_{sRMS}}U((N-1)\tau)$

The first term of the RHS of both equation gives exactly the same result as that obtained in section 4.2 for g =1 i.e. that the final value is achieved when N =1 and has the value $\frac{I_{L1CONST}}{V_{sRMS}}$.

Second terms: $\frac{I_{L1CONST}}{V_{sRMS}}\{\varepsilon(1-\varepsilon)^{N-1}U((N-1)\tau)\}$ for $0 < \varepsilon < 1$

and $\frac{I_{L1CONST}}{V_{sRMS}}\delta((N-1)\tau)$ for $\varepsilon = 1$

The second term of the RHS of the equations represents the change in K necessary to replace (or remove) the energy in the capacitor following a change in the load. Note that the change starts when N = 1. As expected, the energy cannot be replaced (or removed) until a period of τ has passed and the change in energy is measured from the change in V_{cap}. When ε = 1 the energy adjustment takes place in one period from N = 1 to N = 2 but when 0 < ε < 1 the energy adjustment takes place as a decaying function of K of the form $\frac{I_{L1CONST}\varepsilon}{V_{sRMS}}\left\{\underset{N=1}{1},\underset{N=2}{(1-\varepsilon)},\underset{N=3}{(1-\varepsilon)^2}\ldots\right\}$.Note that the sum of the area under this decaying function as N $\rightarrow\infty$ equals the area under $\frac{I_{L1CONST}}{V_{sRMS}}\delta((N-1)\tau)$ which equals $\frac{I_{L1CONST}}{V_{sRMS}}$.

Note: $\sum_{N=1}^{\infty}\varepsilon(1-\varepsilon)^{(N-1)}=1$ for all ε: $0 < \varepsilon < 1$ -----{eqn 4.28}

The decaying function for 0 < ε < 1 therefore has the same energy transfer effect as the impulse function lasting for 1 period of τ when ε = 1.

It is important to note that the energy transferred to the capacitor by K control using this term starting at N = 1 must be at least equal to the energy demand of a step

change in load over a complete cycle. For example, if the load changes from 1kW to 1.5kW at a sample time N_1 then between N_1 and N_1+1 the capacitor has to have sufficient energy to support the additional 500W of load. The energy will be replaced by the second term of the equations starting at sample point N_1+1. In this example (and taking $\tau = 20ms$) the energy stored in the capacitor would have to be at least 10J.

Third terms: $\frac{C\varepsilon V_{capave}^2}{2\tau V_{sRMS}^2}(1-\varepsilon)^N U(N\tau)$ for $0 < \varepsilon < 1$

and $\frac{CV_{capave}^2}{2\tau V_{sRMS}^2}\delta((N)\tau)$ for $\varepsilon = 1$

The third terms of the RHS of the equations represent the change in K needed to initially establish the energy on the capacitor to reach V_{capave}. The energy can either be transferred in one period of τ form N = 0 to N = 1 by making $\varepsilon = 1$ or over several periods using the decaying function by making $0 < \varepsilon < 1$. The two functions transfer the same energy due to eqn{4.28}

Further practical considerations:

It is important to establish the energy to charge the capacitor to V_{capave} as quickly as possible. However if the transistor switches are not rated to carry sufficient current to charge the capacitor in one period of τ then it is possible to lower ε to a value between 0 and 1 and allow the capacitor to charge gradually by using the decaying function of the third term of the RHS of the equations for K.

Considerations of the ε value

The second term and third terms of the RHS of eqn 4.26 are stable with no oscillation provided $1 > \varepsilon > 0$.

The term is stable but oscillates with period τ if $1 < \varepsilon < 2$. For ε outside of these limits the system is unstable.

From a practical point of view it would be of no use to have an oscillating system this would put unnecessary stress on the switching transistors.

Provided the switching H-Bridge transistors are sufficiently rated then the optimum value for $\varepsilon = 1$. For this value (provided g =1), K is restored to the steady state value in two periods of τ following a step change in load. This is one period more than the

effect on the K response compared to that obtained for the outer loop ($\lambda = 0$) as in section 4.2 where there was no control of V_{cap}.

4.5 Proportional Hysterisis Control with Energy Compensation

In this section the theory of Proportional Hysterisis Control incorporating Energy Compensation is developed.
An optimum solution is provided for K given in eqn {4.24} to minimise transient settling time to a step change in load for a given energy compensation coefficient ε. A relationship is obtained between the switching gain g and ε. This is then used to specify the switching boundaries for a hysterisis switching system.

All of the work in this thesis up to this point has assumed that switching takes place at the sample interval following a change in sign of APF error where the error is either the sliding line equation for S ($\lambda > 0$) or $I_{fref} - I_f$ ($\lambda = 0$). This effectively places the error switching boundary at zero as seen from table 3.2 where an Active/Passive switching pair depends on the sign of S(mT) (i.e. the sliding error at the m^{th} sample interval).
In this system (where $\lambda = 0$), hysterisis control forces an active/passive pair to switch between two limits of error, where one limit is zero and the other is a proportion of I_{fref} ($= \rho.I_{fref}$). Table 3.2 is rewritten using a proportional hysterisis boundary as follows:

Mode reference	Category	Error condition to enter mode ($0 < \rho < 1$)	Polarity of V_s	Sign of I_f	Sign of $dI_f(t)/dt$	Transistors enabled	Conducting devices
1	Active	$I_{fref}(mT) - I_f(mT) < \rho I_{fref}(mT)$	+	-	-	Q1, Q4	Q1, Q4
2	Passive	$I_{fref}(mT) - I_f(mT) > 0$	+	-	+	none	D2,D3
3	Active	$I_{fref}(mT) - I_f(mT) > \rho I_{fref}(mT)$	+	+	+	Q3	Q3, D4
4	Passive	$I_{fref}(mT) - I_f(mT) < 0$	+	+	-	none	D1, D4
5	Active	$I_{fref}(mT) - I_f(mT) > \rho I_{fref}(mT)$	-	+	+	Q3, Q2	Q3, Q2
6	Passive	$I_{fref}(mT) - I_f(mT) < 0$	-	+	-	none	D1, D4
7	Active	$I_{fref}(mT) - I_f(mT) < \rho I_{fref}(mT)$	-	-	-	Q1	Q1, D2
8	Passive	$I_{fref}(mT) - I_f(mT) > 0$	-	-	+	none	D3, D2

Table 4.1 *Active/Passive bridge modes using proportional hysterisis error boundaries*

If it is assumed that dI_f/dt is constant throughout a switching interval (i.e. the time between an active and a passive mode) which can be seen from figs 4.45, 4.36 and 4.47 to be reasonable assumption, then on average:

$$I_{frefRMS}(z_\tau) - I_{fRMS}(z_\tau) = \frac{\rho}{2} I_{frefRMS}(z_\tau) \qquad \text{-----\{eqn 4.29\}}$$

giving:

$$I_{fRMS}(z_\tau) = I_{frefRMS}(z_\tau)\left(1 - \frac{\rho}{2}\right) = gI_{frefRMS}(z_\tau) \qquad \text{-----\{eqn 4.30\}}$$

where $\rho = 2(1-g)$ -----{eqn 4.31}

g is now formalised as the gain through the H-bridge where $0 < \rho < 1$ giving:
$0.5 < g < 1$.

It will be shown in the following work that g depends on ε.

The effect of using proportional hysterisis switching can be seen in the following example (figs 4.45, 4.46, 4.47), which shows both I_f and I_{fref} obtained from simulation and from the practical test system (to be presented in Chapter 5).

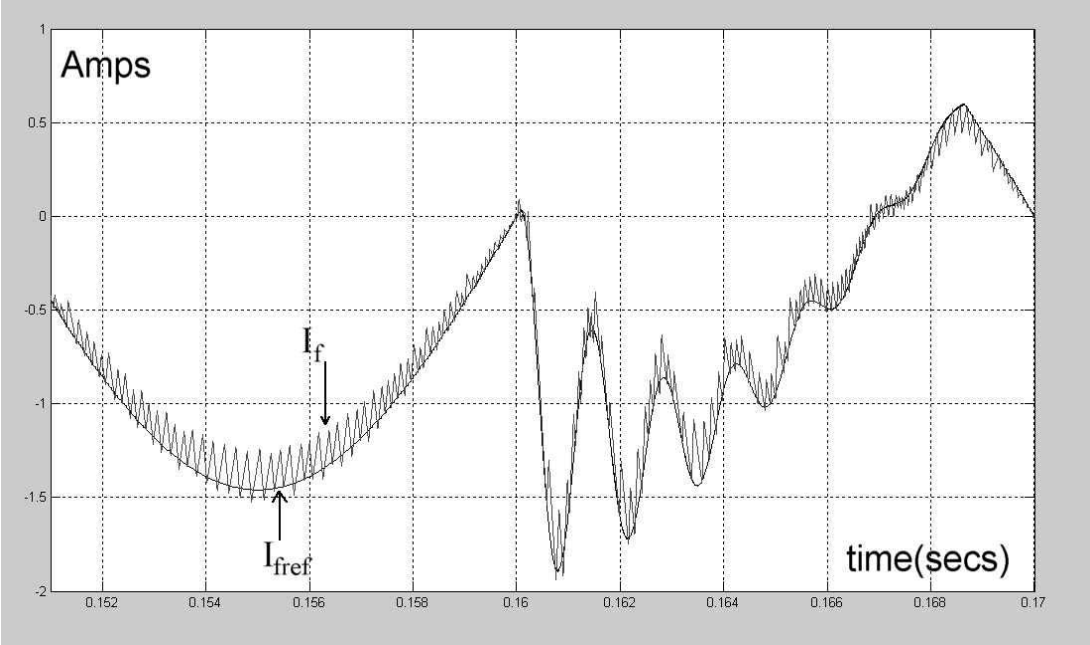


Fig 4.45: *A simulated plot of I_{fref} and I_f showing the effect of proportional hysterisis switching*

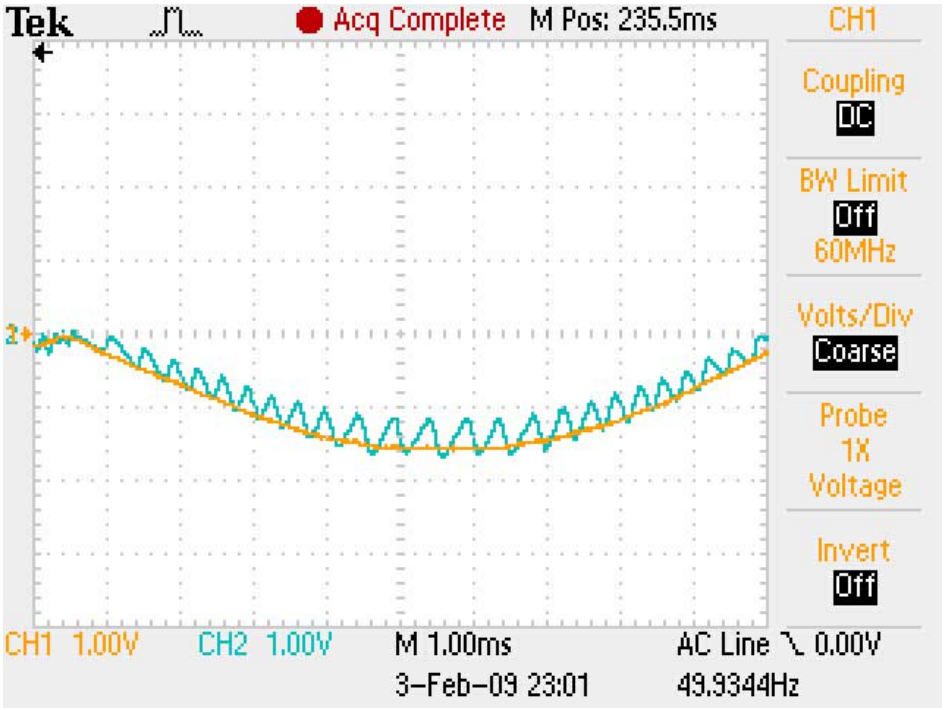


Fig 4.46: *Scope trace of Ifref and If showing the effect of proportional hysterisis switching (ε= 0.5)*

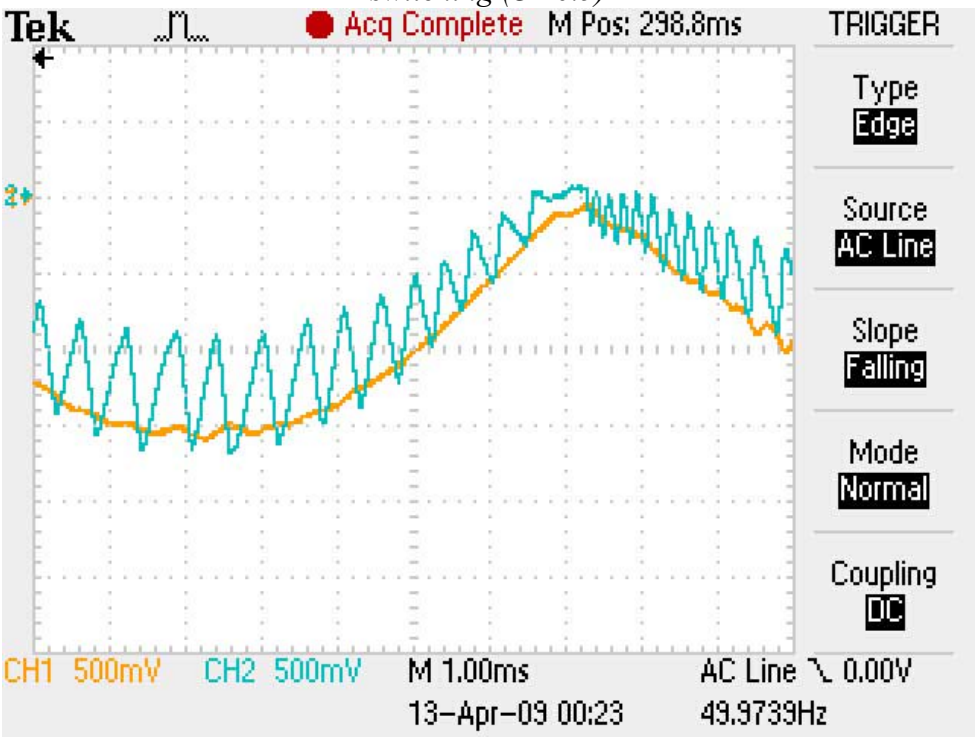


Fig 4.47: *Scope trace of Ifref and If showing the effect of proportional hysterisis switching (ε= 0.4)*

It can be seen that as the magnitude of the APF current increases, the hysterisis boundary increases in proportion. This has the effect of lowering the switching frequency at higher current levels which helps to reduce switching losses.
Note that I_f only strays outside of the switching boundaries until the next sample instant. As I_{fref} goes to zero, the switching frequency increases but cannot exceed the rate set by the sampling period (T) and therefore the maximum switching frequency for low currents is 1/(2T) Hz.
I_f is constrained by the switching boundary to reside inside the profile of I_{fref} i.e. $abs(I_f) \leq abs(I_{fref})$ which gives the effective gain $g < 1$.

Examining the poles of eqn {4.23}, a pole pair exists at:

$$z_\tau = \frac{1}{2}\left[2 - g\varepsilon - g \pm \sqrt{g^2(\varepsilon+1)^2 - 4g\varepsilon}\right] \qquad \text{-----\{eqn 4.32\}}$$

An example of a locus of the poles on the z plane for ε = 0.7 is given in fig 4.48 as g varies from 0 to 1.

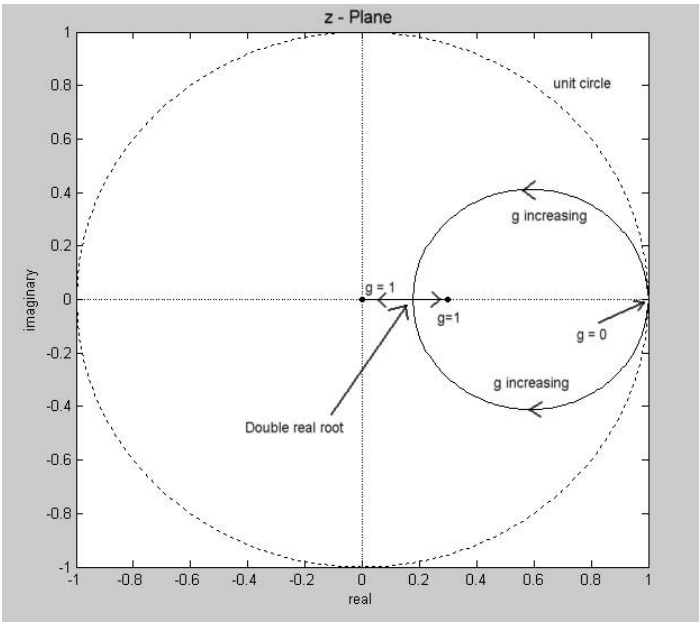


Fig 4.48: *z – plane showing the locus of system poles as g varies from 0 to 1*

The optimum solution for minimum settling time is when both poles are closest to the origin of the z-plane which exists at the double real root.
The double real root exists when:

$$g = \frac{4\varepsilon}{(\varepsilon+1)^2} \qquad \text{-----\{eqn 4.33\}}$$

Applying the constraints of g into eqn {4.33} gives the constraints of ε as:

$0.172 < \varepsilon < 1$

Substituting g from eqn {4.33} into eqn {4.31} gives:

$$\rho = 2\left(1 - \frac{4\varepsilon}{(\varepsilon+1)^2}\right) \qquad \text{-----\{eqn 4.34\}}$$

Substituting g from eqn {4.33} into eqn {4.32} gives the double real root as:

$$z_\tau = \frac{1-\varepsilon}{1+\varepsilon} \qquad \text{-----\{eqn 4.35\}}$$

Substituting for the double real root into eqn {4.24} gives:

$$K(z_\tau) = \frac{I_{LCONST}}{V_{sRMS}}\left(\frac{4\varepsilon}{(\varepsilon+1)^2}\right)\left(\frac{z_\tau}{z_\tau - 1}\right)\frac{(z_\tau(1+\varepsilon)-1)}{\left(z_\tau - \left(\frac{1-\varepsilon}{1+\varepsilon}\right)\right)^2} + \frac{C\varepsilon}{2\tau V_{sRMS}^2}V_{capave}^2\frac{z_\tau^2}{\left(z_\tau - \left(\frac{1-\varepsilon}{1+\varepsilon}\right)\right)^2}$$

-----{eqn 4.36}

Eqn {4.36} can be re-written as:

$$K(z_\tau) = \frac{I_{LCONST}}{V_{sRMS}}\left(\frac{z_\tau}{z_\tau - 1} + \frac{z_\tau}{\left(z_\tau - \left(\frac{1-\varepsilon}{1+\varepsilon}\right)\right)^2} - \frac{z_\tau}{z_\tau - \left(\frac{1-\varepsilon}{1+\varepsilon}\right)} - \frac{z_\tau\left(\frac{1-\varepsilon}{1+\varepsilon}\right)}{\left(z_\tau - \left(\frac{1-\varepsilon}{1+\varepsilon}\right)\right)^2}\right) + \frac{C\varepsilon}{2\tau V_{sRMS}^2}V_{capave}^2\left(\frac{z_\tau}{\left(z_\tau - \left(\frac{1-\varepsilon}{1+\varepsilon}\right)\right)} + \frac{z_\tau\left(\frac{1-\varepsilon}{1+\varepsilon}\right)}{\left(z_\tau - \left(\frac{1-\varepsilon}{1+\varepsilon}\right)\right)^2}\right)$$

-----{eqn 4.37}

The general sampled time domain solution for K is:

$$K(N\tau) = \left(\frac{I_{LCONST}}{V_{sRMS}}\right)U(N\tau)\left\{1 + \left(\frac{1-\varepsilon}{1+\varepsilon}\right)^N\left[\frac{2.\varepsilon.N}{(1-\varepsilon)} - 1\right]\right\} + \frac{C\varepsilon}{2\tau V_{sRMS}^2}V_{capave}^2(N+1)\left(\frac{1-\varepsilon}{1+\varepsilon}\right)^N U(N\tau)$$

-----{eqn 4.38}

Normalising the terms:

$\frac{I_{LCONST}}{V_{sRMS}} = 1$ and $\frac{C\varepsilon}{2\tau V_{sRMS}^2}V_{capave}^2 = 1$, and setting zero initial conditions, the responses for K for various values of ε are shown in fig 4.49:

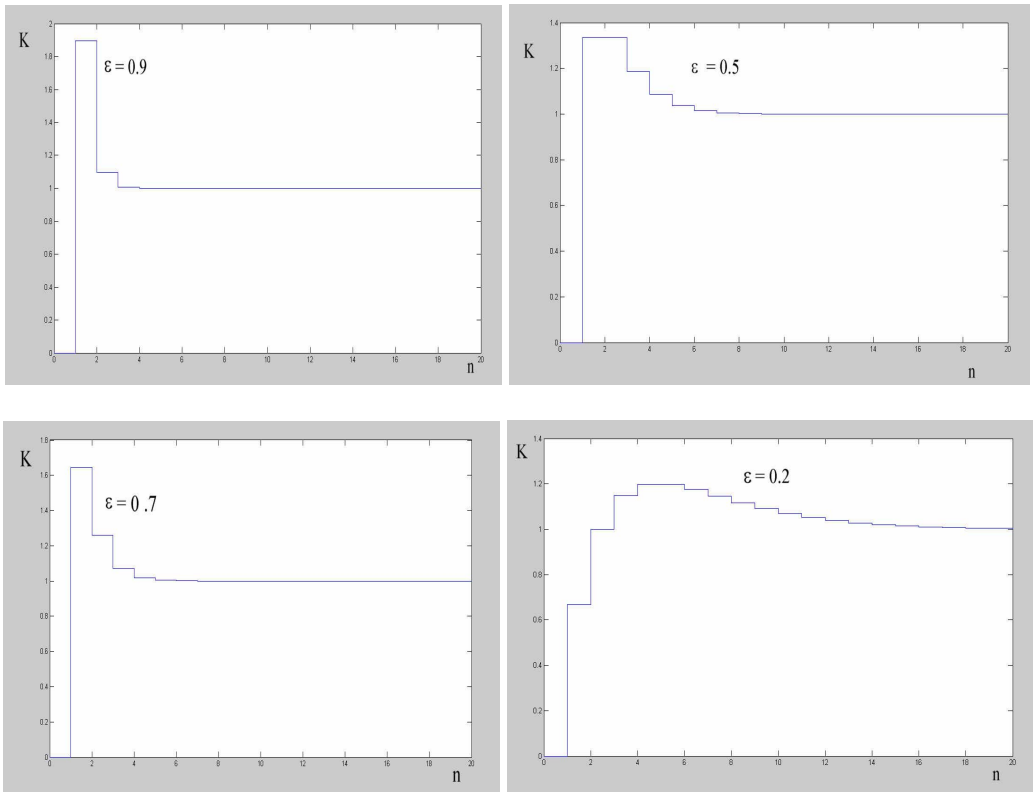


Fig 4.49: *Plots of K (from eqn 4.37) normalised to 1 for various values of ε*

It can be seen from Fig 4.49 that as ε approaches 1 the system converges to the ideal system response given in figs 4.40 and 4.41.

The choice of ε determines the value of g from eqn {4.33} and hence the switching error boundary coefficient ρ from eqn {4.31} which in turn controls the switching losses at the higher current levels of the APF.

Chapter 5 Design and Construction of an APF using Proportional Hysterisis switching with Sampled Energy Compensation Control

5.1 Introduction

Chapter 5 deals with the design and construction of an APF using proportional hysterisis switching and Energy Compensation control as detailed in section 4.5.

Chapter 5 is organised as follows:

- Proposed system overview
- Practical approach to system implementation
- Hardware description
- Details of the control implementation and software details
- Development of a simulation model
- Simulation results
- Practical results
- Proportional hysterisis switching with energy compensation control: Conclusions

5.2 Proposed system overview

The proposed system is detailed in the following block diagram (fig 5.1):

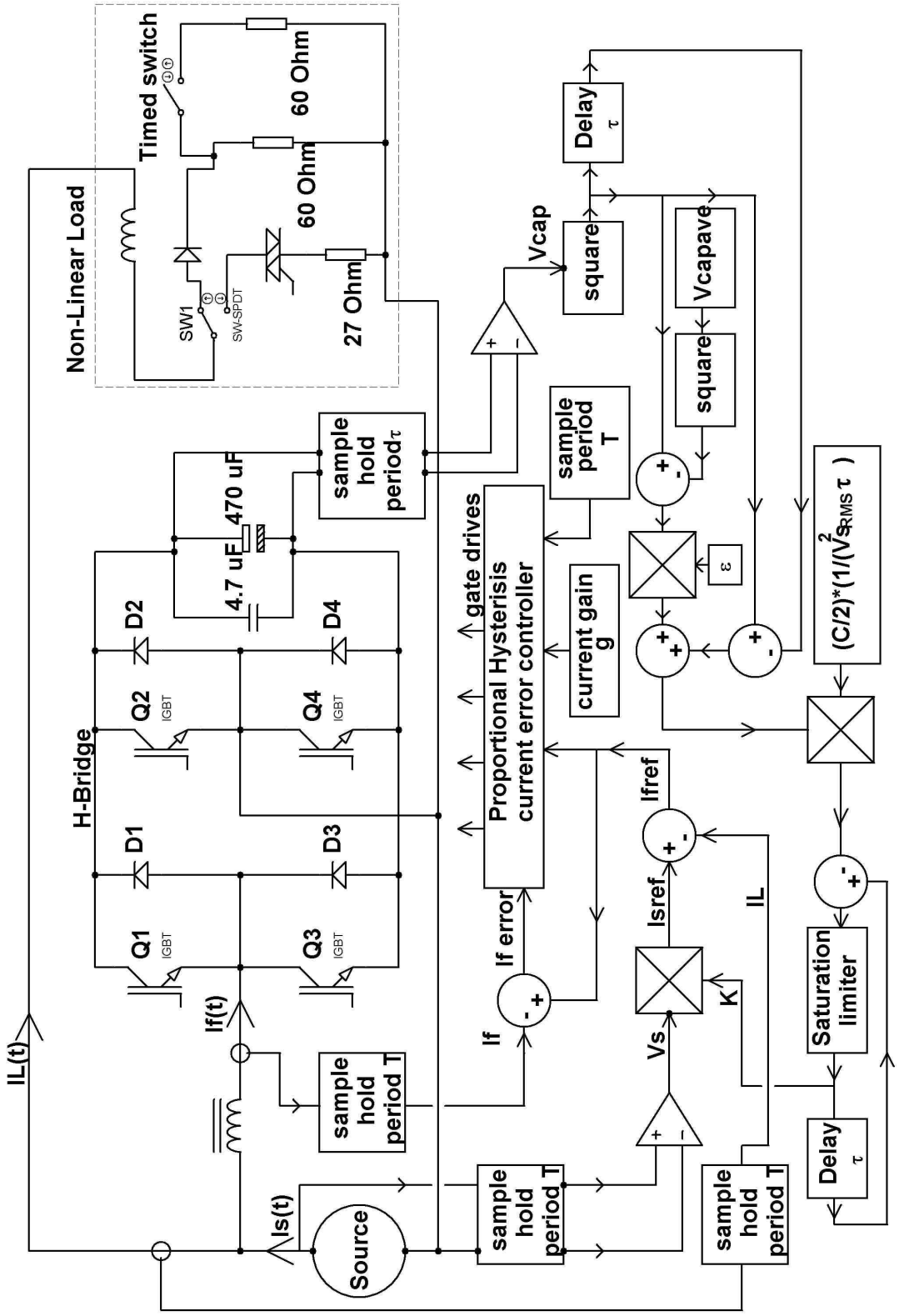


Fig 5.1: *Block diagram of the APF using proportional hysterisis switching and energy compensation control*

It was decided that an economical hardware implementation would be carried out based on an embedded micro-controller owing to the original intention to design an APF for a domestic situation where component cost would be a major factor. The reduced calculation speed of an embedded micro-controller compared to that of a high speed DSP imposes a small compromise of the energy compensation algorithm and the design must therefore minimise the effect of such limitations.

As a demonstration unit the design must incorporate a user interface to allow changes to significant control parameters and to also monitor important signal values as the APF converter is running, therefore a keypad, LCD display and associated user interface software was required.

The main purpose of the design was to demonstrate the effectiveness of the control method based on Proportional Hysterisis and Energy Compensation, so it was decided to ease the requirements of the unit by running from a reduced Voltage (using a 200VA transformer with a quoted 48V secondary but actually having a nominal 53 to 54V secondary) as the source. Furthermore it was specified that the current demand of the filter (i.e. the bridge and energy storage inductor) would not be required to exceed 5A. Since the primary concern of this chapter was to demonstrate the effectiveness only of the energy compensation principle, then the 3/2 H-bridge design (i.e. the extra arm and extra inductor described in section 3.8) was not included.

Two types of non-linear load were considered; a half wave rectified load and a triac phase-controlled load. The half wave rectified load was arranged to be switched between two values of 60 Ohm and 30 Ohm using a MOSFET at a rate determined through the software so that transient performance could be assessed and the triac load was set to 27 Ohm.

5.3 Practical approach to System implementation

The following block diagram (fig 5.2) is the practical implementation of the functional block diagram (fig 5.1):

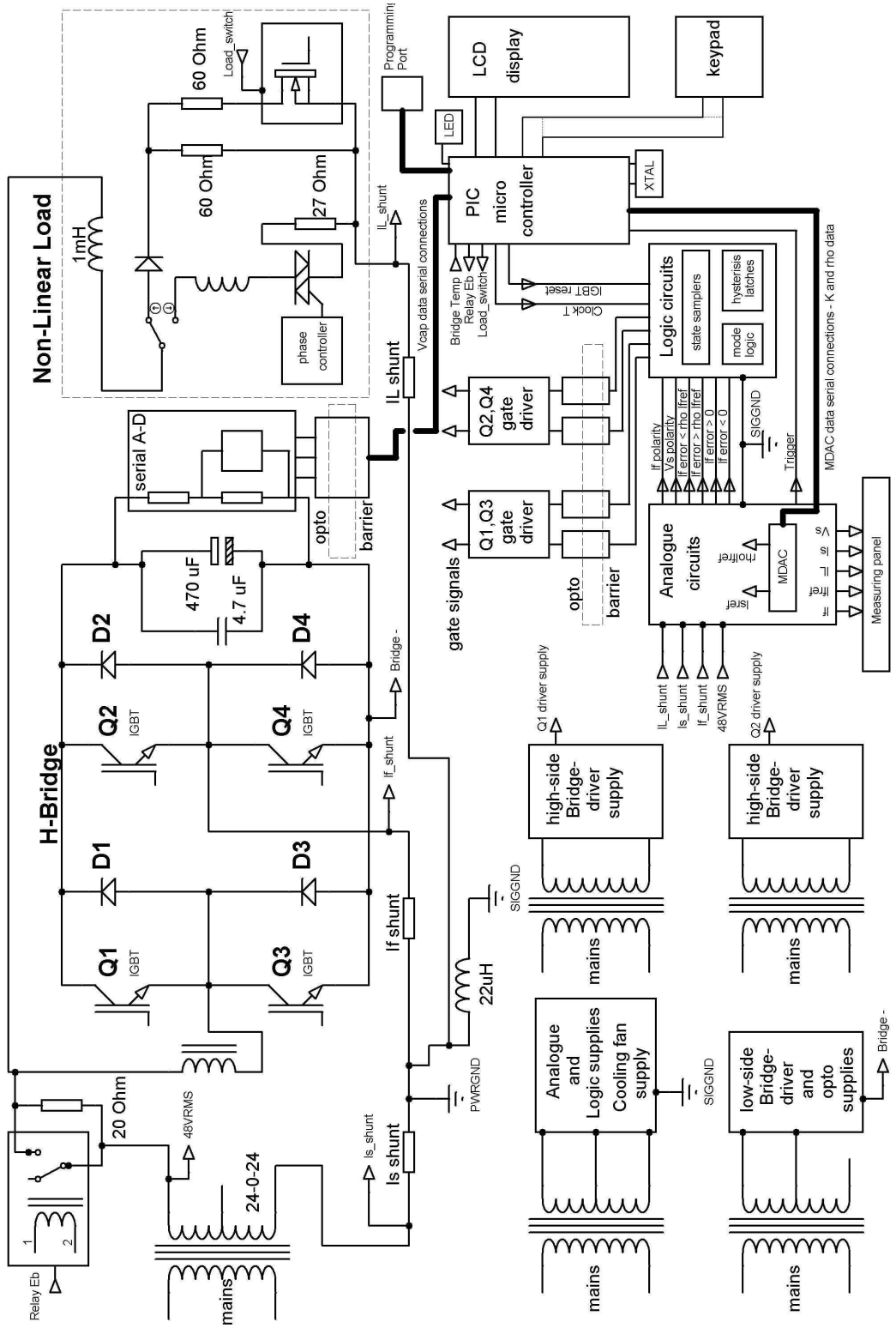


Fig 5.2: *Block diagram of the practical implementation of the APF using proportional hysterisis and energy compensation*

The PIC processor (Microchip 16F877) is at the heart of the system and provides a user interface via the LCD display. A menu system allows the following parameters to be altered from their default values:

- Epsilon (ε)
- Capacitor reference voltage (no time dependence therefore $V_{capave} = V_{capref}$)
- Sampling time (T) for updating switching control values for the H bridge IGBTs
- Source RMS voltage (V_{sRMS})

The menu allows the following controls and monitors:

- Switching the converter on/off
- Monitor K while the system is running (and final value when converter is stopped)
- Monitor the capacitor Voltage while converter is running or stopped
- Monitor bridge temperature

The majority of the system is built onto a PCB (see PCB layout in Appendix J) with the larger components mounted off the PCB but in close proximity it. See Appendix J for a photograph of the complete functional system.

5.4 Hardware Description

5.4.1 Overview

See Appendix I for a complete set of circuit schematics.
A block diagram overview of that part of the system built onto the PCB is given in Appendix I (sheet 1 of 11) from which it can be seen that the system has been sub-divided into various functional areas.
Additionally, hardware that resides off the PCB is also detailed in Appendix I ("circuit components mounted off the PCB sheets 1 - 5").

5.4.2 Power and Signal Supplies and power-up considerations

Refer to Appendix I (sheet 8)
The system is in two parts i.e. that referenced to one side of the source and that referenced to the –ve side of the H-bridge.
The system referenced to the source is split into two parts i.e. that part referenced to PWRGRD and that referenced to SIGGND. To reduce noise coupling the two grounds are connected together at one point via a 22μH inductor (L3). The inductor provides a high impedance path to ground noise coupling.

U26 and U27 provide a balanced +/- 12V supply for the analogue control circuits and U28 provides the +5V supply mainly for the logic elements. This section of the power supply is fed from an independent transformer with a 15-0-15 secondary (external component TR5) and is reference to SIGGND. External transformer TR5 also supplies the power to an external fan supply used to cool the two rectified loads.

U23 and U30 provide two auxiliary supplies at +15V and +5V. These provide the rails for those components referenced to the –ve side of the H-bridge. This section of the power supply is fed form one 0-15 tapping of an independent transformer (external component TR6). The second tapping of the same transformer (TR6) is referred to the +ve side of the H-bridge (sheet 8 - J15) to reduce the common mode current pulse fed back to the primary as the bridge transistors switch.

The source current is fed via a 20 Ohm power resistor connected to J23 to eliminate the surge current into the H-bridge DC side energy storage capacitor. The APF software reset routine contains a check of the capacitor Voltage by waiting for it to charge via the diode bridge and then performing two checks of the capacitor Voltage 5ms apart. Provided it has charged to a preset level, the software will close relay RL1 to short J23 allowing direct connection of the load and APF to the source. Ensuring that the capacitor is fully charged before switching on the APF converter will help to eliminate the possibility of high Voltage transients affecting the bridge and associated components.

R78 provides the current shunt for measuring I_s via amplifier U33A which gives a signal of 1V/Amp.

5.4.3 Switched Non-Linear load

Refer to Appendix I (sheet 6 of 11).

There are two non-linear loads selected by toggle switch SW1: a half-wave rectified resistive load or a triac controlled resistive load.

The half-wave rectified load comprises diode D8, a power resistor of 60 Ohm connected to J19 and a FET controlled load in parallel with J19. The FET controlled (auxiliary) load comprises Q8 and a power resistor of 60 Ohms connected to J20. The FET which switches the auxiliary load is under software control via signal Load_switch. The alternative load, which is mounted off the PCB, is a triac with variable phase control in series with a 27 Ohm power resistor.

R57 is a shunt resistor for measuring IL via amplifier U24:A which gives a signal of 1V/Amp.

Amplifier U24:B is a difference amplifier which gives signal Ifref = Isref – IL (see eqn 3.30) also at 1V/Amp.

5.4.4 Cap ADC and Interface

Refer to Appendix I (sheet 3 of 11)

The purpose of this section is to measure the capacitor Voltage. Measurement is achieved using a serial A to D (U2) which is referenced to Bridge-. The capacitor Voltage is sensed using potential divider R1 and R2 with transient spike and reverse protection zener D12.

The PIC processor accesses the A to D via an opto-interface consisting of U3, U4 and U5.

The bridge side of U3, U4 and U5 are powered from the auxiliary 5V supply (+5Vaux) and the controller side of the opto barrier is supplied from the 5V supply (+5V) referenced to SIGGND.

U2 is a Burr-Brown device (ADS7818) which is an externally clocked successive approximation 12-bit converter. The PIC internal SPI module is used to access U2. The processor initiates conversion using a signal vcap_conv via opto barrier U5 and then generates a clock (vcap_clock) via opto U4.

Data (vcap_data) is returned to the processor via opto barrier U3.
The processor hardware clocks data to its internal data registers in synchronism with vcap_clock.
Optos U3, U4 and U5 (HCPL4503) are chosen for their high common mode dV/dt rejection rating (specified to 15000 V/µs) which is essential to eliminate false triggering by capacitive coupling across the opto barrier.

5.4.5 Vs and If sign comparators

Refer to Appendix I (sheet 11 of 11).
This section extracts the sign of Vs, the sign of Ifref and also provides the triggering signal that initiates the periodic K update energy calculation.
Comparators U14:A and U14:B extract the sign of Ifref (a small amount of hysterisis is added to avoid jitter at the switching point). The signal level is made TTL compatible (R53, R54 D7) and is then sampled by the sampling clock (clock T) in U29:B
Comparator U35:A extracts the sign of Vs from "Vsbuf" (a buffered signal from U31:A sheet 4 of 11). Since Vs is a fairly clean filtered source then hysterisis is not added to this circuit, however filtering is provided to ensure no glitches (C36). The level is converted to TTL (R85, R86 and D11) and then sampled by the sampling clock (clock T) in D-type U29:A.
Comparators U13:A and U13:B provide a trigger pulse (low to high) to initiate an edge triggered interrupt of the PIC. The triggered interrupt routine performs data collection and calculation and then updates the rho and K values for the next mains cycle. The Trigger pulse goes high when Vs reaches -7.68V and goes low before the zero crossing of Vs (i.e. when Vs reaches -2.48V).
When the APF converter is running noise will appears on the main 48V supply due to the impedance of the source supply transformer. This can cause unwanted feedback and therefore this must be filtered to obtain "Source ref" = Vs. Filtering must not shift the phase of Vs relative to the 48V RMS source. "Source ref" (=Vs) is therefore provided by a step-down transformer (external component TR4 – Appendix I external sheet 4) and two low-inductance polypropylene capacitors (external components C11 and C12). Further protection against transients and noise is provided by external zener diodes D11 and D12.

5.4.6 Proportional Hysterisis Controller A

Refer to Appendix I (sheet 9 of 11).

The signal "If_shunt" from resistor R3 (sheet 2 of 11) is buffered and filtered by U1:A. Filtering is necessary to remove noise form the signal. The break point is set so that the delay through the filter at 2kHz (the 40^{th} harmonic) is not significant. Any significant phase shift at this point will compromise the compensating APF filter current. U1:A delivers a signal that is 1V/Amp.

U1:B is a differential amp that derives Iferror = Ifref – If.

Iferror is compared with rhoIfref (i.e. ρ.Ifref) and 0V to obtain the four hysterisis identifiers:

- a: Iferror < rhoIfref
- b: Iferror > rhoIfref
- c: Iferror > 0
- d: Iferror < 0

These four signals determine the hysterisis boundaries within mode pairs as given in the following table:

Mode reference	Category	Error condition to enter mode $(0 < \rho < 1)$	Hysterisis Identifier	Polarity of V_s	Sign of I_f	Sign of $dI_f(t)/dt$	Transistors enabled	Conducting Devices
1	Active	$I_{fref}(mT) - I_f(mT) < \rho I_{fref}(mT)$	a	+	-	-	Q1, Q4	Q1, Q4
2	Passive	$I_{fref}(mT) - I_f(mT) > 0$	c	+	-	+	none	D2,D3
3	Active	$I_{fref}(mT) - I_f(mT) > \rho I_{fref}(mT)$	b	+	+	+	Q3	Q3, D4
4	Passive	$I_{fref}(mT) - I_f(mT) < 0$	d	+	+	-	none	D1, D4
5	Active	$I_{fref}(mT) - I_f(mT) > \rho I_{fref}(mT)$	b	-	+	+	Q3, Q2	Q3, Q2
6	Passive	$I_{fref}(mT) - I_f(mT) < 0$	d	-	+	-	none	D1, D4
7	Active	$I_{fref}(mT) - I_f(mT) < \rho I_{fref}(mT)$	a	-	-	-	Q1	Q1, D2
8	Passive	$I_{fref}(mT) - I_f(mT) > 0$	c	-	-	+	none	D3, D2

Table 5.1: *Switching modes showing the hysterisis identifiers for Active/Passive mode pairs*

The four hysterisis identifier signals are filtered to remove transient spikes and converted to TTL levels.

The eight operational modes shown in table 5.1 are grouped into 4 Active/Passive mode pairs and are decoded from the sampled signals If sign and Vs sign using the and-gates of U12 and inverters of U11.

5.4.7 Proportional Hysterisis Controller B

Refer to Appendix I (sheet 10 of 11)
The bridge will reside in one of the hysterisis bands corresponding to the 4 mode pairs (see table 5.1) with signals Mode 1/2, Mode 3/4, Mode 5/6, Mode 7/8 determined from the sampled signals If sign and Vs sign. The required hysterisis mode enables one of four memory latches formed from U15, U16, U17 and U18. Each latch stores the state of the system corresponding to hysterisis identifier signals a, b, c and d derived on sheet 9.
The latched outputs are sampled in U19 and U21 using the software selectable sample clock (clock T) to obtain the IGBT gate drive signals Gate 1, Gate 2, Gate 3 and Gate 4. The or-gates of U20 are used to logically derive the Gate-drive signals with reference to the "Transistors Enabled" column of Table 5.1. An overriding signal IGBT reset allows the processor to turn the APF converter on or off.

5.4.8 IGBT driver interface

Refer to Appendix I (sheet 5 of 11)
This section provides an opto barrier for each signal using the device HCPL 4503 (chosen for the high specification of dV/dt – minimising the risk of a capacitively coupled trigger feedback). The control side of the opto barrier is powered from +5V and bridge side of the opto barrier is powered from +5V aux.

5.4.9 H-Bridge and drivers

Refer to Appendix I (sheet 2 of 11)
The gate signals from the opto-barrier on sheet 5 are sent to two high/low side drivers (U22 and U23 – IR2106). The high side driver part of U22 and U23 are intended to be powered from bootstrap capacitors (C5 and C6), but this proved to be too unreliable so separate external 15V supplies were attached across each capacitor. Details of the external supplies for this purpose are given in Appendix I: circuit components mounted off the PCB (Hi-side supplies, external sheet 3 of 5). Since the low side IGBT's are referenced to bridge –, then both low side drivers are powered from the +15V auxiliary supply (Appendix I sheet 8 of 11).

5.4.10 DAC control and temperature monitor

Refer to Appendix I (sheet 4 of 11)

U37 is a dual MDAC (MAX532). The function of this device is:

- To receive a buffered Vs and transmit K.Vs = Isref
- To receive Ifref, and transmit rhoIfref (= ρ.Ifref)

Both signals are inverted to their correct sense and buffered by U32A and B.

U31:B provides a buffered source reference signal equal to 0.1 of the actual source voltage which is used only for monitoring purposes.

U31:A provides a buffered Vs ("Vs_buf") to the Vs sign detection circuit (page 10 of 11).

An external temperature monitor based on an Analogue Devices TMP01 sends an analogue signal back to the PIC processor via J21 where it is connected to the PIC's AN0 (Analogue port 0) input for monitoring the H-Bridge temperature.

The MDAC (U37) is a serially controlled device which receives two 12-bit words from the PIC. When low, signal $DA\overline{CS}$ enables the MDAC. Data signal Da Data is clocked synchronously with clock Da Clk. 12-bits of rho are transmitted first followed by 12-bits of K. Data is latched into the MDAC internal register with signal $DA\overline{LD}$. The PIC internal USART is used to serially shift data to the MDAC.

5.4.11 PIC and User Interface

Refer to Appendix I (sheet 7 of 11)

U25 (PIC16F877 from Microchip) provides all of the control and user interface functionality. It is clocked from crystal X1 at 4MHz giving an instruction rate of 1MIP. LED D10 indicates when the H-bridge converter is operational. User commands are provided by a 12-key keypad arranged in rows and columns and scanned by software. User feedback is provided via LCD1 (2 rows of 20 characters) which is arranged on a 4-bit data interface together with control lines RS, RW and E form PIC port D. The PIC's internal SPI module is used to serially access the capacitor Voltage (signals Vcap_conv, Vcap_clock and Vcap_data). The internal USART module is used to send serial data to the MDAC for updating K and rho (signals $DA\overline{CS}$, $DA\overline{LD}$, DA data and DA Clk). Some additional logic is needed to ensure the correct logical sense of DA Clk which is provided by U11:E C D, U20:C and U34:A.

5.4.12 IGBT H-Bridge and inductor

Refer to Appendix I (external component sheet 1 of 5)

The H-bridge module is a Semikron SK 30 GH 123 mounted in a Semitop package.

Absolute maximum bridge values

V_{CES} = 1200V

I_F (diode current0 = 37A

I_c (IGBT current) = 33A

The inductor L1 is rated at 5A up to 25kHz and was custom built by AGW Electronics Ltd.

5.4.13 Additional System Details

5.4.13.1 Measuring Ground

Five BNC sockets were mounted onto a conductive measuring panel. Each signal (IL, Is, Ifref If and Vs) were connected using screened cable to the BNC sockets with the screen connected to SIGGND at each connection point of the PCB. Ground noise was effectively reduced by grounding the measuring panel to the SIGGND connection point of ground-inductor L3 (Appendix I: sheet 8 of 11).

5.4.13.2 High side IGBT driver Supplies

The supplies to power the high side IGBT driver of each of U22 and U23 are derived from 50Hz mains transformers TR1 and TR2 (Appendix I external component sheet 3). The capacitance between primary and secondary of these transformers can be significant giving a capacitively coupled common mode current back to the source. To eliminate this it was suggested (Nottingham University Power Lab standard practice) to use low capacitance DC-DC converters. However, since the source is derived from a 200VA transformer, the effect of a common mode current in this particular circumstance is significantly reduced.

5.4.13.3 H-Bridge DC connections

See Appendix I: circuit components mounted off the PCB sheet 2.

The bridge dc side storage capacitor is an off-PCB chassis mounted radial 470µF electrolytic capacitor rated to 250V. The inherent inductance of such a device causes

severe problems due to the high dI_f/dt requirements; therefore a very low inductance 4.7uF polypropylene capacitor was connected directly across the bridge. The electrolytic has to be placed as close as possible to the H-bridge to further reduce inductance. The power current flows through these short direct connections. Voltage sensing wires are connected between the capacitor and the PCB.

5.4.13.4 System Transients and their effect on Control

Voltage transients across the bridge are inevitable at the IGBT switching times. For this reason currents are often measured using non-contact Hall-effect sensors. To reduce cost it was decided to use current shunts to measure the system currents. This causes switching transients to be coupled into the controller ground reference. Transient coupling was reduced by including two 1mH inductors (external components L2 and L3) in series with the bridge ac terminals (Appendix I external component sheet 2). Furthermore, careful placement of logic supply decoupling capacitors (10µF tantalums), strategic signal filtering and the inclusion of the ground inductance (L3 Appendix I sheet 8) helped to reduce the ground noise to an insignificant level. Furthermore, the switching transients and subsequent ringing only last for about 3µs, so by setting the sample time at a minimum of 20µs allows the ringing to die away well before the next sample clock edge. This allows sufficient time for the control signals (hysterisis identifiers a, b, c and d of Appendix I sheet 9) to settle to their correct values.

5.5 Details of control implementation and software details

5.5.1 Calculating K

A new value of K is calculated towards the end of a mains cycle ready for the next cycle and this operation is initiated by a “trigger”.
An edge interrupt of the PIC is referred to here as a “trigger”. Trigger processing occurs once every cycle of the source Voltage. The system Voltage is sensed and a trigger signal is developed which occurs just before the source Voltage reaches the -ve peak (see Appendix I: sheet 11 of 11 for “trigger” circuit). At the instant the PIC is triggered and the trigger is validated in software, all processor time is devoted to

collecting system data and evaluating and updating K and rho. The following activities form the trigger event:

- Serially sensing the capacitor voltage
- Performing energy calculations (see eqn {4.15} and eqn {4.17})
- Calculating the new value for K (see eqn {4.16})
- Serially updating K and rho

The trigger event takes between 3 to 4 ms to execute. The K calculation based on the two energy difference equations (eqns {4.15} and {4.17}) rely on V_{cap} information based on a complete cycle (between zero crossings of the source cycle). It is therefore impossible to satisfy the energy calculation algorithm exactly, so a compromise situation has been developed. Following a trigger event, a software delay is executed so that data is accessed about 3.5ms before the positive going source zero crossing. Following relevant calculations to obtain K, both K and rho are serially updated within one ms after the positive going zero crossing. Once the capacitor Voltage is within 1.5 Volts of the set reference, the energy compensation component of the K calculation (in eqn 4.16) is set to zero for the following cycle. This scheme has been found to work very successfully.

Energy calculations are mostly performed using integer arithmetic to speed up processing time. The final results for K and rho are sent serially to an MDAC (Appendix I: sheet 4 of 11, U37) where the values affect the analogue control signals.

5.5.2 Signal Scaling and Calculations

This section details some important areas relating to calculations performed within the software.

5.5.2.1 Vs and K scaling

Signal Vs is scaled to the source voltage (signal 48VRMS) as:

$$Vs = \frac{48VRMS}{8.56} \qquad \text{-----\{eqn 5.1\}}$$

The input conductance principle gives:

Is = K x 48VRMS

As far as the system is concerned, Is is measured in Volts where 1V represents 1Amp

Therefore

Is = 8.56 x K x Vs -----{eqn 5.2}

The MDAC (U37) data is scaled to 4096 (12 bit full scale) i.e. the output signal equals the input signal * MDAC data register/4096

Therefore let Kscaled = 4096 x 8.56 x K = 35062 x K -----{eqn 5.3}

5.5.2.2 Capacitor Voltage scaling

The resistor ratio sensing the capacitor Voltage is 1 : 40 (Appendix I sheet 3 of 11, R1 and R2).

For the A-D converter see U2 (Appendix I sheet 3 of 11).

The A-D converter performs a 12-bit conversion relative to 5V therefore:

$$\frac{A-DBinaryValue}{4096}\times 5 = \text{Voltage into ADC}$$

$$\therefore \frac{A-DBinaryValue}{4096}\times 5\times 40 = \text{Actual Capacitor Voltage}$$

Therefore V_{cap_binary} . 20/409 ≈ V_{cap} -----{eqn 5.4}

The same ratio will be applied to the capacitor reference:

V_{capref_binary} . 20/409 = V_{capref} -----{eqn 5.5}

Assuming that the capacitor never exceeds 159.96V (i.e. an A-D binary value of 3276) then the approximation of eqn {5.4} will allow 16 bit unsigned integer arithmetic to be used (i.e. 20 * 3276 < 65535).

5.5.2.3 Energy and K calculation details

From eqns {3.31} and {3.32}

$$\Delta E = \frac{1}{2}C\left(V_{cap}-V_{capold}\right)\left(V_{cap}+V_{capold}\right)$$

C = 470μF

Using eqns {5.4, 5.5}

$$\therefore \Delta E = \frac{1}{2}\times 470\times 10^{-6}\left(V_{cap\_binary}-V_{capold\_binary}\right)\left(V_{cap\_binary}+V_{capold\_binary}\right)\times\frac{20^2}{409^2}$$

$$\therefore \Delta E = 0.5619\times 10^{-6}\left(V_{cap\_binary}-V_{capold\_binary}\right)\left(V_{cap\_binary}+V_{capold\_binary}\right)$$

-----{eqn 5.6}

Similarly

$$\Delta E_{comp} = 0.5619\times 10^{-6}\left(V_{cap\_binary}-V_{capref\_binary}\right)\left(V_{cap\_binary}+V_{capref\_binary}\right)$$

-----{eqn 5.7}

From eqn {4.16}

$$K = K_{old} - \left(\Delta E + \varepsilon \Delta E_{comp}\right)\frac{1}{\tau V_s^2} \qquad \text{-----\{eqn 5.8\}}$$

Using eqn {5.3}, let Kold_scaled = 35062 x K_{old}

Combining eqns {5.6}, {5.7} and {5.8}:

$$Kscaled = 35062 \times K = Koldscaled - \left(\frac{0.5619 \times 10^{-6} \times 35062}{\tau V_s^2}\right)$$

$$\times \left\{\left(V_{cap\_binary} - V_{capold\_binary}\right)\left(V_{cap\_binary} + V_{capold\_binary}\right) + \varepsilon\left(V_{cap\_binary} - V_{capref\_binary}\right)\left(V_{cap\_binary} + V_{capref\_binary}\right)\right\}$$

-----{eqn 5.9}

In keeping with the notation used in the C-listing for the PIC let:

$$deltaE = \left(V_{cap\_binary} - V_{capold\_binary}\right)\left(V_{cap\_binary} + V_{capold\_binary}\right) \qquad \text{-----\{eqn 5.10\}}$$

and

$$deltaEcomp = \left(V_{cap\_binary} - V_{capref\_binary}\right)\left(V_{cap\_binary} + V_{capref\_binary}\right) \qquad \text{-----\{eqn 5.11\}}$$

With τ = 20ms eqn {5.9} approximates to:

$$Kscaled = Koldscaled - \frac{1}{V_s^2}\left(deltaE + \varepsilon.deltaEcomp\right) \qquad \text{-----\{eqn 5.12\}}$$

Note that evaluation of deltaE and deltaEcomp as given by eqns {5.6} and {5.7} reduces the calculation time by reducing the number of 16 bit multiplications.

5.5.2.4 Bridge Temperature Calculations

The temperature sensor returns 1.49 V at 25 degC and the device Voltage changes by 5mV/deg C.

For the PIC 10 bit A-D converter and a 5V reference:

[(Temp sensor Voltage -1.49)/0.005 + 25] = actual bridge temperature in deg C

At 25 deg C when device Voltage = 1.49 the binary result = 1.49*1024/5 = 305

The change in binary value per deg C relative to 25 deg C is:

(Change in sensor Voltage)*1024/5

= change in binary value of 205 per Volt change

Therefore for a 5mV change, the binary value changes by 1 bit,

i.e. relative to 25 deg C the binary result changes 1 LSB per degC.

Therefore to evaluate temperature use:

(Binary Value read from A-D converter – 305) + 25 = Bridge Temperature in deg C

5.5.3 Software Details

See Appendix K

The software was developed as two collections of routines APF.c and utility.c together with library functions for handling the keypad and LCD display module.

5.5.3.1 C listing apf.c (Appendix K)

The following routines are contained within apf.c

- Declarations and definitions
- Interrupt handling routines for timer 0 and the edge interrupt. Timer 0 generates a 1ms interrupt rate when required to switch the non-linear load so that transient performance can be measured. The edge interrupt contains the routines for the energy difference calculations and updating K and rho. It is initiated by the "trigger" signal
- The APF reset function checks that the capacitor and bridge is basically functioning correctly (i.e. it has charged to almost the peak of the source) before switching a relay to short out the source input surge limiter resistor. All registers and variables used in the PIC are initialised. Additionally, library routines are called to initialise the LCD display to 4-bit data operation.
- The main function calls the reset function and then the modes function
- The modes function sequentially goes through all the menu items in turn in response to keypad entries. When selected, the particular menu function is called from the utility.c collection

5.5.3.2 C listing utility.c (Appendix K)

The following functions are contained within utility.c

- A selection handling function
- A function "sample_rate" for setting the sample rate (clock T) which controls the rate at which the gate signals to the IGBT's are updated
- A function "Kscaler" for scaling K as given by eqn {5.3} i.e. returning the actual value of K from Kscaled

- A function “rhocalc” for calculating the binary scaled value of rho for outputting to the MDAC using eqn 4.34 and floating point arithmetic
- A function “mdac_out” for transferring rho and K to the MDAC using function “outdac”
- A function “outdac” for formatting the data for transferring to the MDAC
- A function “Vcap_ADC” for reading back the capacitor Voltage. The value returned is the binary value for V_{cap} (i.e. V_{cap_binary} see eqn {5.4})
- A function “stop_APF” which stops the converter by resetting the signal igbt_reset and turning off the converter-running indicator LED
- A function “start_APF” that resets K back to 0.01, sets igbt_reset to enable conversion and turns on the LED converter-running indicator
- A function “set_epsilon” which allows epsilon to be incremented or decremented in steps of 0.05 between the limits of 0.4 and 0.9
- A function “set_T” which allows the sample rate to be set in steps of 1μs between the limits of 20 and 40μs. Note that the variable T is one less than the actual sample rate.
- A function “set_load_rate”. The user is asked if the auxiliary load is required. This enables the user to put an additional continuous 60 Ohm load in parallel with the permanent 60 Ohm load as part of the half wave rectified non-linear load. The user is also offered the option of periodically switching the auxiliary 60 Ohm load so that transient performance can be observed. The time between switching on and off can be set between 15 and 250ms in steps of 5ms. This is deliberately not synchronised to the source cycle.
- A function “set_capref” that allows the user to set the reference value for the capacitor voltage (V_{capref}). The default value is 100V and can be set between the limits of 95 and 150V in steps of 5V (i.e. a step scaled binary value of 103)
- A function “measure_cap_volt” which interrogates the capacitor A to D using function “Vcap_ADC” and displays the Voltage on the LCD display
- A function “display_K” that displays the current K value on the LCD display either dynamically as the converter is running or the previous value when the converter is stopped.
- A function “display_temp” that displays the H-bridge temperature on the LCD display

- A function “enter_RMS” that allows the user to enter the RMS Voltage for the system for use in the energy difference calculation. The default value is 54V but can be altered in steps of 1V between the limits of 38V and 58V
- A function “capvoltscaler” that is used to implement equations {5.4} and {5.5}
- A function “outchar” for use with the printf function that outputs one character at a time to the display.

5.6 Development of a simulation model

The Matlab/simulink/SimPwrSystems model described in this section will use discrete proportional hysterisis switching and energy compensation control with a half wave rectified switched load. The results will be compared in section 5.8 with those obtained from the practical system.
This section highlights the modifications necessary to the simulation model (apf3.mdl) given in Appendix C and described in section 3.12 in order to obtain predictions of the output of the practical system. Four non-linear load conditions will be used for assessment

- Steady 30 Ohm rectified load with $\varepsilon = 0.9$
- Transient performance obtained by switching every 150ms between 30 and 60 Ohm half wave rectified load with $\varepsilon = 0.9$
- Transient performance obtained by switching every 150ms between 30 and 60 Ohm half wave rectified load with $\varepsilon = 0.5$
- A phase controlled load using a triac and a 27 Ohm load where the triac is set to fire at approximately 54^0 and 234^0 (i.e. 30% of the half period from the zero crossing).

5.6.1 The Simulation System

The system is almost identical to the system given in Appendix C and described in section 3.12 with the following changes:

- The "fast" inductor of the 3/2 H-bridge is disconnected and throughout the simulation, sw1a and sw3a are kept at zero.
- The section that derives Vcapref is not used. A constant value of Vcapconst is fed directly in to the switching algorithm (switch_control5_53V.m as shown in Appendix L).
- Lambda is no longer used which disables the 2nd order sliding space. The switching function S is only dependent on the filter current If (where xdot = If/C).

5.6.2 The switching control m-file

The switching controller (referenced as switch_control5_53V.m) is contained in Appendix L. It is very similar to the switch control function of Appendix D – and described in section 3.12.4.1. The main differences are as follows:

- All conditions of lambda are removed so that the switching is only dependent on If
- Proportional hysterisis conditions are imposed on the H-Bridge switching, based on the value of rho which is calculated from epsilon in accordance with eqn {4.34}. The switching implementation is based on table 5.1.

To mimic the practical demonstration system, for **all** of the simulations the following key parameters are maintained:

- H-Bridge input inductor = 20mH
- RMS value of Vs = 53V
- C = 470μF

The following values need to be set in the Matlab workspace:

- T (the sample period)
- Epsilon (ε the energy compensation coefficient)
- Vcapconst (required target Voltage of Capacitor)

5.7 Simulation results

This section contains the results for the simulation system described in section 5.6.

5.7.1 Constant 30 Ohm half wave rectified load ε = 0.9

The following values were used in the workspace:

- Epsilon = 0.9
- T = 20μs
- Vcapconst = 100V

The simulation time was set to 400ms.

The results are shown in Appendix M: "Constant 30 Ohm half wave load ε = 0.9"

The steady state value for K is read as 0.0166 Ω^{-1}

The results were post analysed using freqplot3.m (see Appendix E).

Total harmonic results (for the last 200ms of the data):

- THD for IL = 0.4404
- THD for Is = 0.0167
- Total harmonic current for IL = 0.3842 A RMS
- Total harmonic current for Is = 0.0157 A RMS
- Total harmonic source Voltage = 0.0451 V RMS
- THD source Voltage = 8.51 x 10^{-4} (based on the standard source impedance of R= 0.25Ohm and L = 796μH)

The results indicate a very good improvement in THD and that the capacitor voltage remains steady around 100V.

5.7.2 Switched half-wave resistive load ε = 0.9

The following values were used in the workspace

- Epsilon = 0.9
- T = 20μs
- Vcapconst = 100V

The half-wave load was switched between 30 Ohms and 60 Ohms every 150ms.
The simulation time was set to 600 ms.

The results are shown in Appendix M: "Switched resistive load ε = 0.9"

The results indicate good correlation to the expected theoretical response given in fig 4.49 (with ε = 0.9). There is a distinct transient overshoot following the step in load

with the system stabilising very quickly in 2 cycles of the source. Similarly the capacitor Voltage remains stable around 100V with deviations for 2 source cycles.

5.7.3 Switched half-wave resistive load ε = 0.5

The following values were used in the workspace

- Epsilon = 0.5
- T = 20μs
- Vcapconst = 100V

The half-wave load was switched between 30 Ohms and 60 Ohms every 150ms. The simulation time was set to 600 ms.

The results are shown in Appendix M: "Switched resistive load ε = 0.5"

The results indicate good correlation to the expected theoretical response given in fig 4.49 (with ε = 0.5). There is less overshoot following the step in load with the system stabilising in 4 cycles of the source. The deviations in If and Is are more pronounced owing to the larger hysterisis boundary with a reduced value of ε.

5.7.4 Phase Controlled load ε = 0.9

The following values were used in the workspace

- Epsilon = 0.9
- T = 20μs
- Vcapconst = 130V

The load was set to 27 Ohms and switched and phase controlled so that the switching point was 30% of a half period of the mains corresponding to switching angles of 54^0 and 234^0.

The results are shown in Appendix M: "Phase controlled load ε = 0.9"

The results were post analysed using freqplot3.m (see Appendix E).

Total harmonic results (for the last 200ms of the data):

- THD for IL = 0.3210
- THD for Is = 0.1695
- Total harmonic current for IL = 0.5521 A RMS
- Total harmonic current for Is = 0.2996 A RMS
- Total harmonic source Voltage = 1.0563 V RMS
- THD source Voltage = 0.0199 (based on the standard source impedance of R= 0.25Ohm and L = 796μH)

Owing to the higher demand on dI_f/dt, the value of Vcapconst was increased to 130 V for the triac controlled load to give the switching system a higher bandwidth.
The results for the phase controlled load indicate an improvement in THD. The capacitor Voltage remains stable near 130V as required.

5.8 Practical Results

The Practical test rig was set up to perform the same sequence of test as performed in the simulation (section 5.7). The set of tests performed were as follows:

- Steady 30 Ohm rectified load with ε = 0.9
- Transient performance obtained by switching every 150ms between 30 and 60 Ohm half wave rectified load with ε = 0.9
- Transient performance obtained by switching every 150ms between 30 and 60 Ohm half wave rectified load with ε = 0.5
- A phase controlled load using a triac and a 27 Ohm load where the triac is set to fire at approximately 54^0 and 234^0 (i.e. 30% of the half period from the zero crossing).

Access to all of the relevant signals is available from the measurement panel (see photograph of test rig Appendix J).
The results were captured using a Tektronix TDS2002B 1GS/s storage oscilloscope.

5.8.1 Constant 30 Ohm half wave rectified load ε = 0.9

Using the user interface menu, the following values were used for the practical test:

- Epsilon = 0.9
- T = 20μs
- Vcapconst = 99V
- Aux load switched into circuit so that the total half wave rectified load is 30 Ohm.
- System Voltage set to 53V

The results are shown in Appendix N: "Constant 30 Ohm half wave rectified load ε = 0.9"

Total harmonic results were evaluated from the captured data:
- THD for IL = 0.4466 (over 8 harmonics of 50 Hz)
- THD for Is = 0.0632 (over 8 harmonics of 50 Hz)

- Total harmonic current for IL = 0.3995 A RMS
- Total harmonic current for Is = 0.0649 A RMS
- Total harmonic source Voltage = 0.0467 V RMS
- THD source Voltage = 8.8197 x 10^{-4} (based on the standard source impedance of R= 0.25Ohm and L = 796μH)

K value read from system while the converter running = 0.0196 to 0.0198

The results indicate a very good improvement in THD. All THD and total harmonic results are in close agreement with the simulated results of section 5.7.1.

Also all results (time and frequency domain) are very close to the expected results obtained from simulation (section 5.7.1).

The trace showing the capacitor Voltage indicates that the control system is maintaining an average value of around 100V as required.

The 'scope trace showing Is and Vs demonstrates that they are in phase resulting in unity power factor.

5.8.2 Switched half-wave resistive load ε = 0.9

Using the user interface menu, the following values were used for the practical test:

- Epsilon = 0.9
- T = 20μs
- Vcapconst = 100V
- System Voltage set to 53V

The half-wave load was switched between 30 Ohms and 60 Ohms every 150ms.

The results are shown in Appendix N: "Switched resistive load ε = 0.9".

The step inputs cause the source current to quickly stabilise in 2 cycles of the source. The profile of Is is similar to that obtained from simulation (see section 5.7.2) and there is reasonable correlation of the envelope with the theoretical response given in fig 4.49 (with ε = 0.9) where the transient dies away rapidly compared to lower values of ε. Also a capacitor Voltage trace is shown which shows clearly that the average Voltage is 100 V with deviations for 3 cycles when the transient load change occurs and is very similar to the capacitor waveform obtained from simulation (section 5.7.2).

5.8.3 Switched half-wave resistive load ε = 0.5

Using the user interface menu, the following values were used for the practical test:

- Epsilon = 0.5
- T = 20μs
- Vcapconst = 100V
- System Voltage set to 53V

The half-wave load was switched between 30 Ohms and 60 Ohms every 150ms.

The results are shown in Appendix N: "Switched resistive load ε = 0.5"

The step inputs cause the source current to stabilise in about 4 cycles of the source. The profile of Is is similar to that obtained from simulation (see section 5.7.3) and there is reasonable correlation of the envelope to the expected theoretical response given in fig 4.49 (with ε = 0.5).

5.8.4 Phase Controlled load ε = 0.9

Using the user interface menu, the following values were used for the practical test:

- Epsilon = 0.9
- T = 20μs
- Vcapconst = 130V
- System Voltage set to 53V

The constant load was set to 27 Ohms

The results are shown in Appendix N: "Phase controlled load ε = 0.9"

Total harmonic results were evaluated from the captured data

- THD for IL = 0.3556 (over 8 harmonics of 50 Hz)
- THD for Is = 0.0835 (over 8 harmonics of 50 Hz)
- Total harmonic current for IL = 0.4401 A RMS
- Total harmonic current for Is = 0.1564 A RMS
- Total harmonic source Voltage = 0.2517 V RMS
- THD source Voltage = 0.0047 (based on the standard source impedance of R= 0.25Ohm and L = 796μH)

Owing to the higher demand on dI_f/dt, the value of Vcapconst was increased to 130 V for the triac controlled load to give the switching system a higher bandwidth.

The results for the phase controlled load indicate an improvement in THD. There is reasonably good correlation to the simulated results (section 5.7.4) in both time and frequency domain with small variations in harmonic results due to the slight variation in firing angle between the practical and simulated system.

5.9 Proportional hysterisis switching with Energy Compensation Control: Conclusions

Chapter 5 has been concerned with the implementation of the proportional hysterisis switching system using energy compensation control as proposed in section 4.5.
A simulation model was adapted from a model described in 3.12 but using a new switching control algorithm (detailed in Appendix L) including the proportional switching technique. It has been shown that there is good agreement between simulated results and the results obtained from the demonstration practical system (detailed in sections 5.4 and 5.5) for static loads (half wave rectified and phase controlled) and transient loads. The transient responses are also in agreement with the type of response predicted through the use of real-power-flow analysis, in particular equation {4.38} (see predicted responses fig 4.49).
Overall the responses obtained are a significant improvement over the reported results using sliding control [5.4] and at least as good as other reported results using a similar sliding control technique [5.7]. For example, the reported results in [5.7] exhibit a transient recovery similar to that of a system using energy compensation with $\varepsilon = 0.4$ which is probably due to the sliding control space interfering with the capacitor energy which in turn affects the recovery of K following a step change in load (see discussion section 3.13.6). The energy compensation system can perform at least as well as the "generic" PI controller systems (see ref [4.3]). It was seen (section 3.14.3.6) that after tuning, a PI controller (incorporating a low pass filter for capacitor Voltage smoothing) good THD results could be obtained and a transient recovery was possible in approximately 4 cycles of the source. This is approximately equivalent to an energy compensation system with $\varepsilon = 0.7$.
The availability of inexpensive microcontrollers to implement the energy compensation algorithm, the good steady state characteristics and a transient response that is easily controlled with one coefficient suggests that this control technique should be given serious consideration for future developments.

Chapter 6 Conclusions and Further work

6.1 Conclusions

The work presented in this thesis has provided an in-depth analysis and design of a system for actively removing the harmonic and reactive components of a non-linear load connected to an ac single phase mains supply.

The thesis describes methods to develop sliding mode control for a Voltage fed Active Power Filter (APF) based on an H-bridge configuration in order to compensate the reactive power components of an undefined non-linear load. The underlining theory of application has been dealt with and a thorough analysis of all internal H-bridge switching states has been presented. Further, the application of sliding mode has been modified through the use of sample states by the introduction of Discrete Sliding Mode (DSM). First-order DSM was developed which required two references to produce the two error signals that span the sliding space. The two chosen references were I_{fref} and V_{capref}. The details for developing the error signals to define the sliding line are presented to show how integral constants are removed prior to the construction of the sliding function. A full discussion and analysis has been presented for DSM including an algorithm for implementation.

It has been shown that at any time the H-bridge resides in one of 8 modes. It is shown that there are two methods of driving the bridge – either unipolar or active/passive. The active/passive mode was chosen since it complements the DSM algorithm which in turn prevents "chattering" normally associated with pure sliding mode.

The APF is connected in parallel with the load with the intention of presenting a pure resistance to the mains supply. The current flowing in the mains supply must therefore be proportional to the mains Voltage where the constant of proportionality is the input conductance (K). Optimum control of K has been central to the APF development.

The objective throughout the APF development has been to force the mains current to be proportional to the supply Voltage and not necessarily a sinewave as used by some researchers in this area. Any distortion of the mains supply Voltage will then appear proportionally in the mains current.

A reasonable assumption is made that the non-linear load remains steady for several periods of the mains cycle (typically at least 4 cycles); it is then possible to measure energy change within the APF and use this as a feedback signal to control K.

The H-Bridge used extensively by researchers in this area was enhanced by the introduction of an extra pair of diodes and switches resulting in the "3/2 H-Bridge". The introduction of the 3/2 H-Bridge enabled the system to cater for a wider range of harmonics without unnecessarily incurring large current overshoots. Using the principle of reachability enabled the dynamics of the 3/2 H-Bridge to be optimally switched with respect to the sliding surface. It is impossible to cater for all load conditions so there will inevitably be load harmonics that cannot be removed and these appear as a violation of the reachability condition.

The capacitor was used as a sensor so that energy balancing could be used to provide the necessary feedback signals to establish the input conductance and hence the current reference. The capacitor Voltage reference was found by integrating the APF current reference and compensating for unwanted components of integration by filtering. The resulting capacitor Voltage reference had to be gated by a signal that was derived from an algorithm built into the control system to compensate for the active and passive phases and also the rectification effect of the bridge.

Through the use of a detailed model using MATLAB, Simulink and the SimPowerSystems toolbox, the system using DSM was successfully demonstrated for both zero λ and non-zero λ conditions (where λ is the gradient of the switching surface).

For theoretical purposes only, tests were performed with λ set to zero. Very good control of just the APF current was achieved (indicated by good THD results), however the Voltage of the capacitive energy store was dependent on initial conditions and therefore would not be suitable as a practical system.

When λ was non-zero, DSM maintained control of the two internal state variables i.e. APF current and the Voltage of the internal APF energy store and good THD results were obtained. However convergence of K to a steady state solution was too slow to be of practical use. A thorough investigation was carried out of the approaches taken by other researchers. It was found that a "generic" system using a linear feedback approach could be built based on a linearising approximation which gave acceptable results. Linear system can pose practical difficulties owing to the necessity to digitise signals so that they can pass through an opto isolation barrier. In this respect, and due to the availability of inexpensive microcontrollers, a discrete system has significant advantages.

A discrete system using the DSM algorithm to control the APF remained inconclusive and a new approach was required to analyse the system.

In order to continue the analytical work of the APF so that the dynamic response could be studied in depth, it was necessary to develop a technique based on the principle of current averaging which has been referred to as "Real Power Flow Analysis". Through the use of this technique the reasons for the poor performance using DSM became clearer. It was shown that the DSM system can be represented as two loops (an inner and an outer loop) joined via the sliding surface equation. The conclusion was that by forcing the capacitor Voltage to follow a reference via the sliding surface leads to instability in the outer loop and further interferes with the feedback energy signal needed to obtain the current reference. The conclusion was that the Sliding Mode principle was unsuitable for APF control and that further work was necessary to find a more suitable control method.

Using the insight provided by Real Power Flow Analysis enabled a new system to be developed that allowed both control of the APF current and the capacitor energy store Voltage using an additional term called "Energy Compensation". It was proved analytically using Real Power Flow that with this system, the dynamics could be better controlled to give the desired response. It was shown that by making the "Energy Compensation" feedback factor unity it would not be theoretically possible to achieve a better dynamic response of the APF.

The concept of "proportional hysterisis" control was introduced in order to reduce switching losses at higher current levels. The switching boundary for the APF current was made proportional to the APF current. This enabled the switching system to act, on average, as an amplifier with a gain related to the switching boundary. It was shown that optimal placement of the poles of the discrete system transfer function for K enabled the switching boundary to be specified in terms of the energy feedback factor. The system referred to as "proportional hysterisis switching with energy compensation control" was the basis for the development of a practical demonstration system.

A practical demonstration system was built which was fed from a 53V source. The control algorithm and user interface software was run in a PIC microcontroller. A MATLAB simulation model was developed to perform the same function as the practical system. Static non linear loads and transient test were performed on both the practical system and the simulation system. Good correlation was achieved between

the simulation model and the practical system, and proved the validity of the underling theory using the Real Power Flow equations.

6.2 Further Work

It has been shown that Sliding Mode Control of both APF current and the Internal Capacitor Voltage is not a suitable technique therefore further work should focus on other control methods.
Although it is unlikely that the use of a current fed APF would be suitable for a domestic application owing to the physical size of the inductive energy store, it would be beneficial to investigate the application of "Energy Compensation" in this context.
The use of the 3/2 H-bridge provides an improved response through the dynamic switching of the effective system bandwidth which helps to reduce overshoot. However there are still instants when the reachability condition fails. Small improvements in switching bandwidth and hence improvement of THD can be achieved by altering the average capacitor Voltage. Assuming that the load remains periodic and steady for several mains cycles, it would be beneficial to investigate whether a signal derived by filtering the reachability condition could be used to "fine tune" the response through the adjustment of V_{capave}.

When a step change in load occurs, there must be sufficient energy stored in the APF capacitor to support the load change for a complete mains cycle. The limitation imposed by this requirement could be removed by replacing the capacitor with a rechargeable battery. Careful adjustment of ε (see fig 4.49) may be necessary to control the rate of energy recovery.

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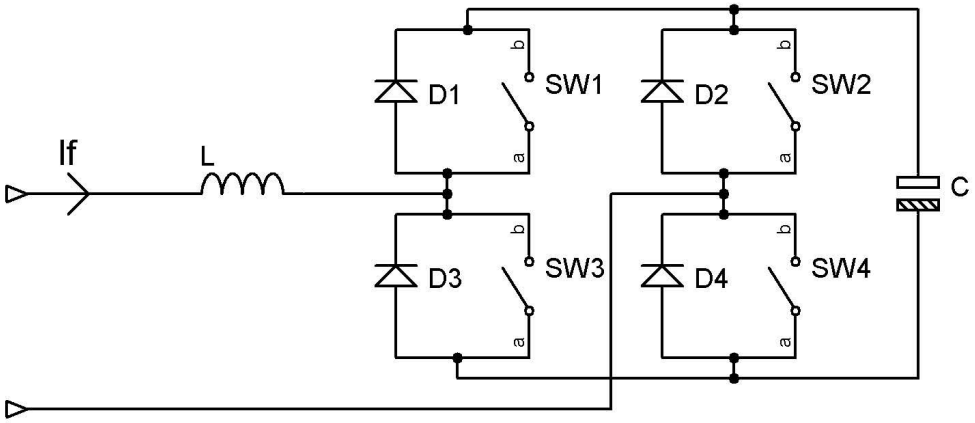
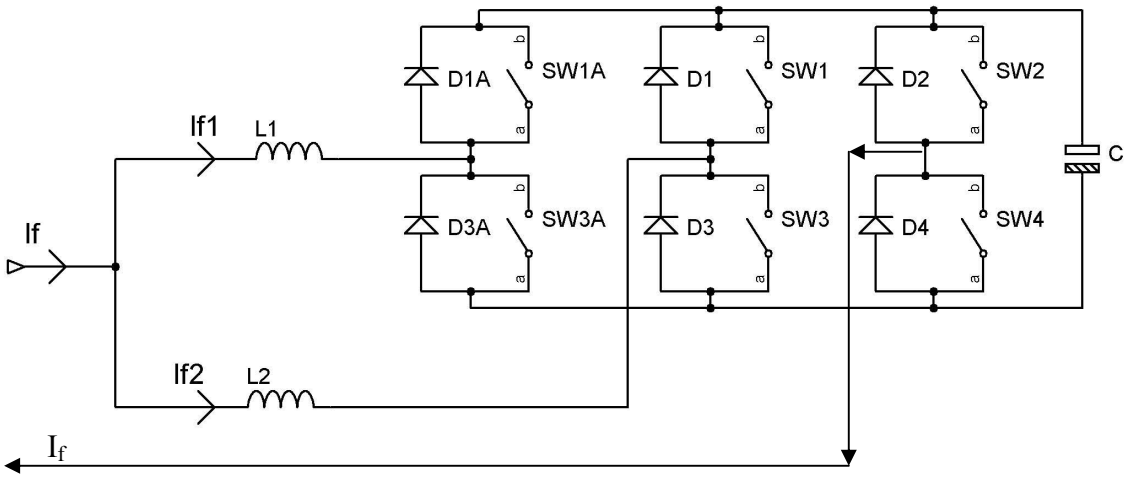
Appendix A: The Single Phase H-Bridge



Single Phase H-Bridge

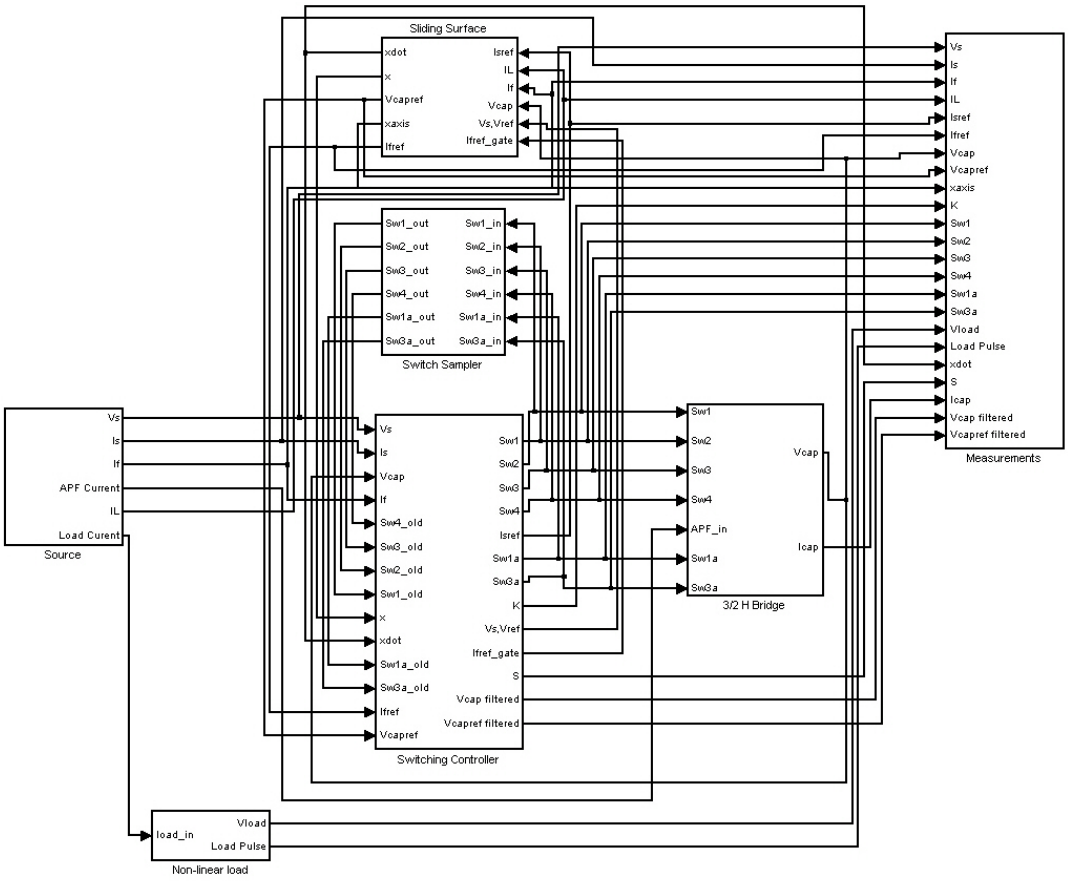
Appendix B: The Single Phase 3/2 H-Bridge



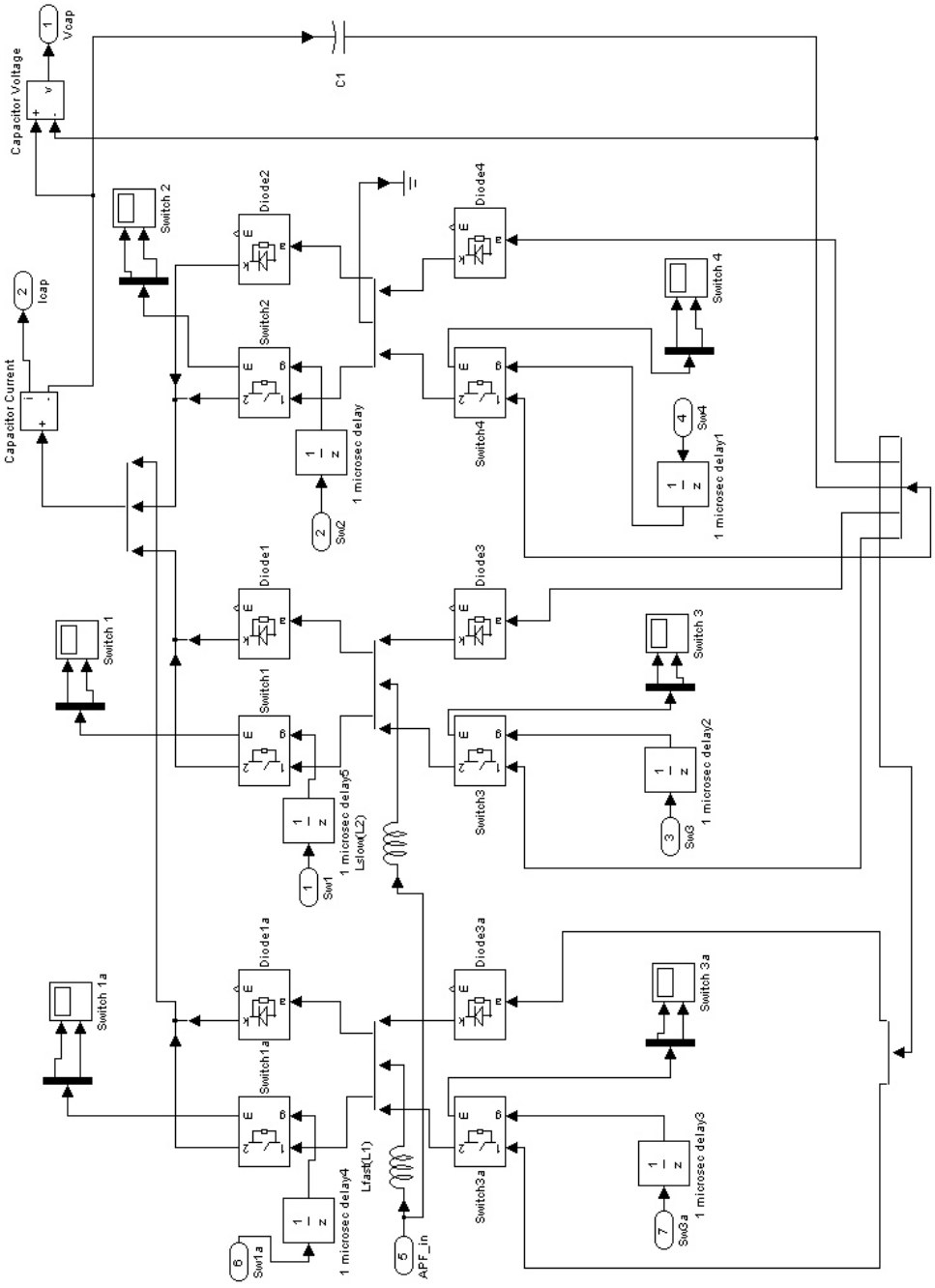
Single phase 3/2 H-Bridge

Appendix C: MATLAB Model (APF3.mdl) used to investigate zero and 1st order sliding control

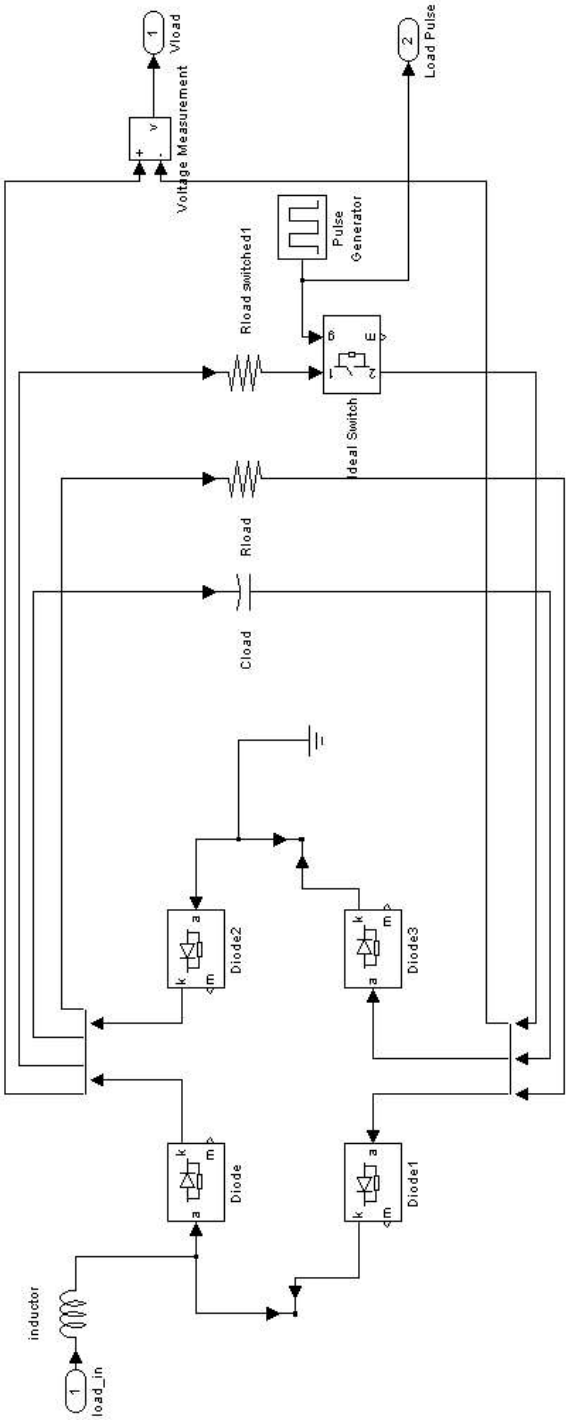
Appendix C: APF Block Connections



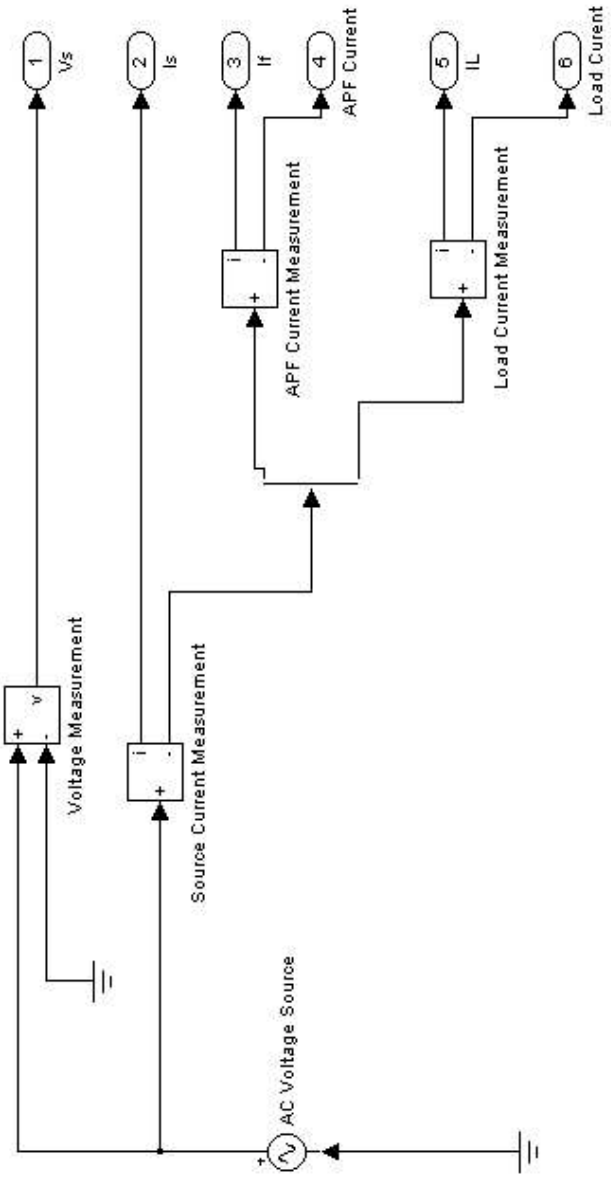
Appendix C: 3/2 H-Bridge



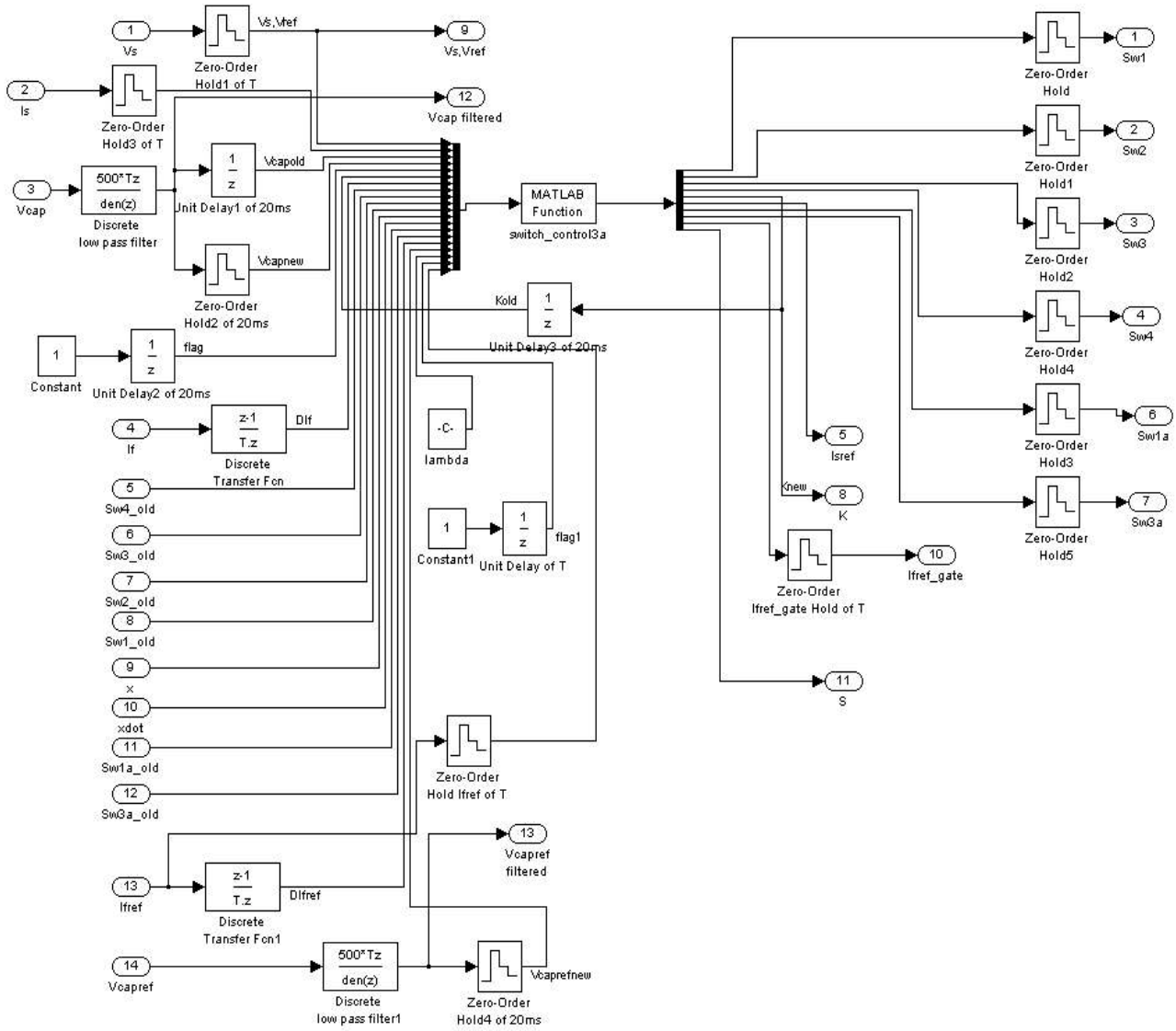
Appendix C: Non-Linear Load



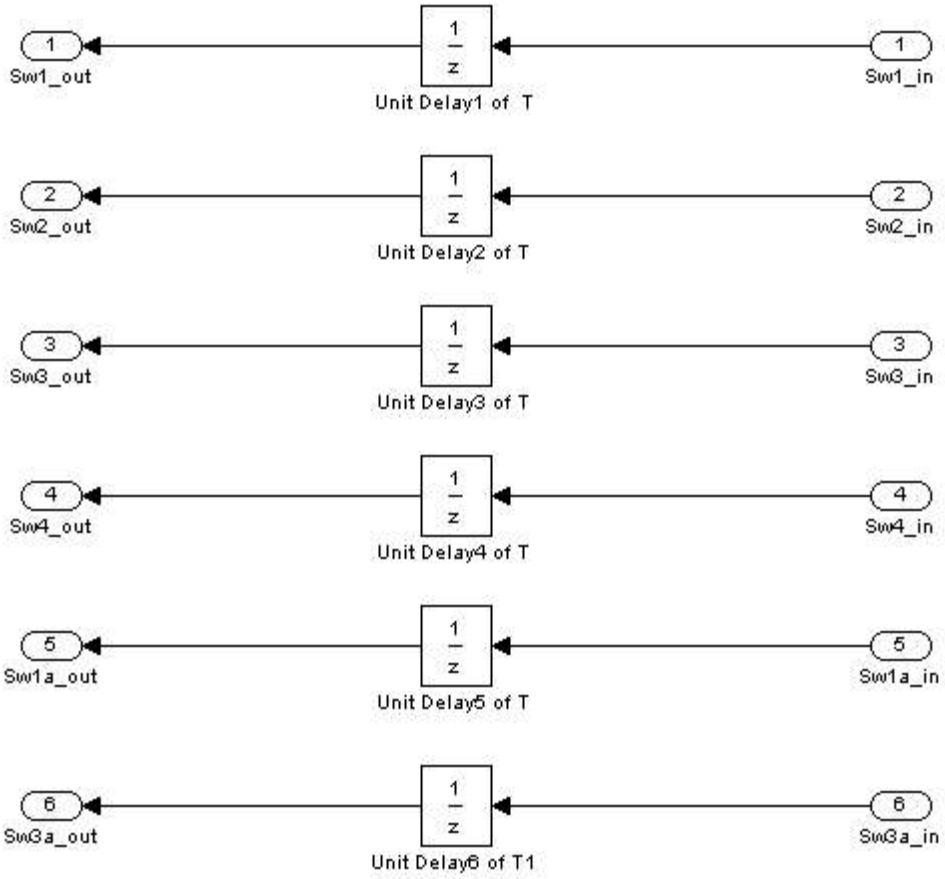
Appendix C: Source



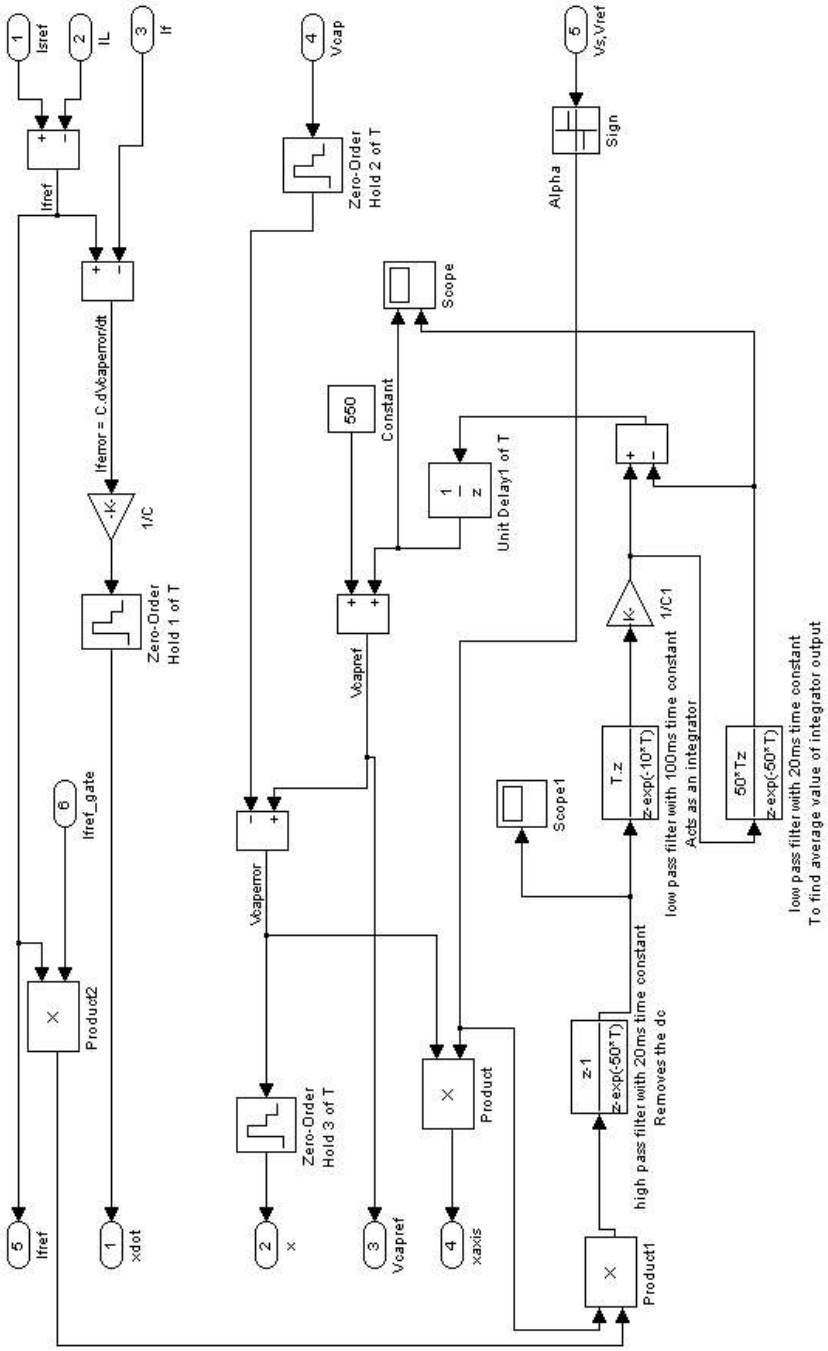
Appendix C: Switching Controller



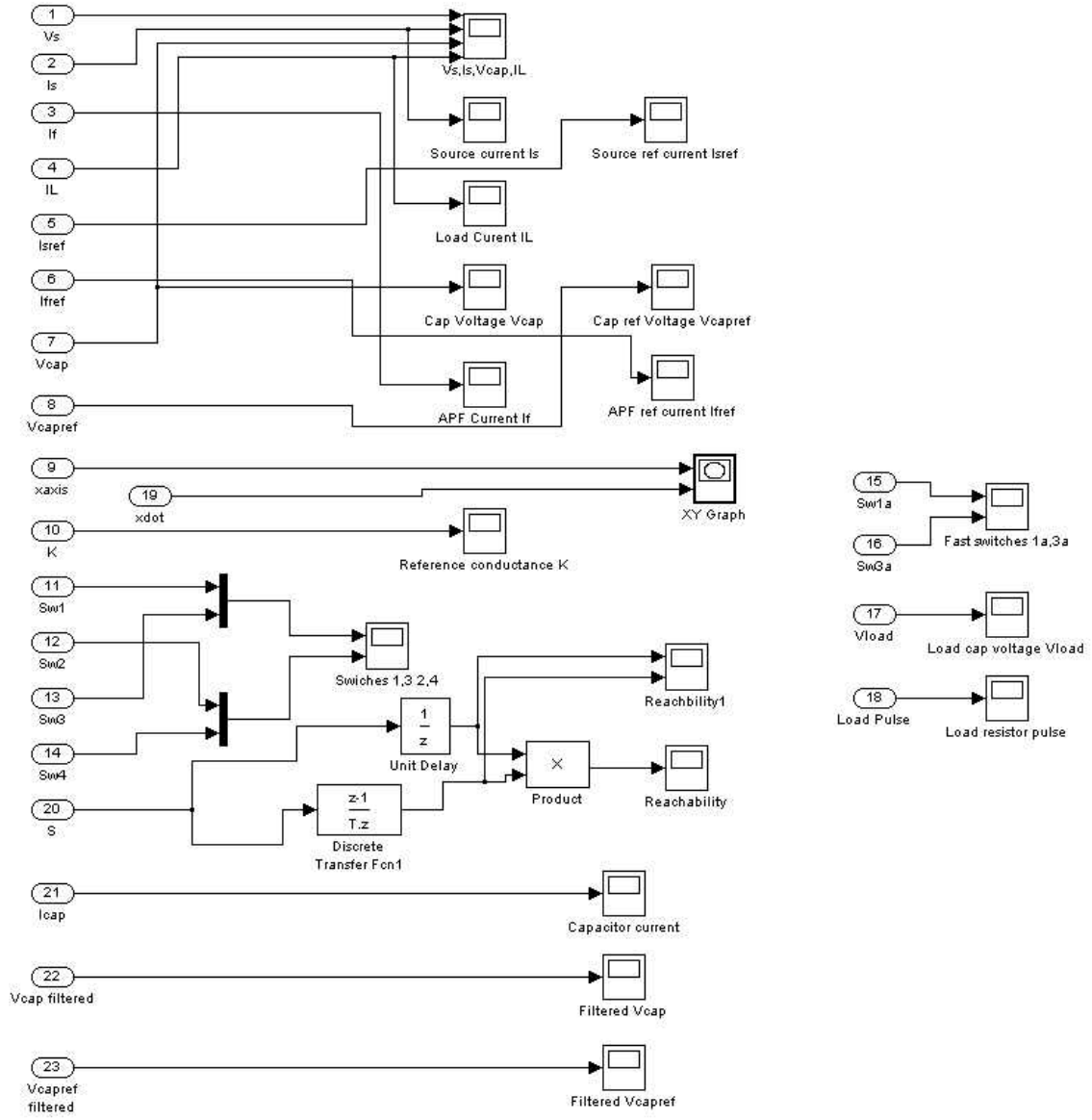
Appendix C: Switch Sampler



Appendix C: Sliding Surface



Appendix C: Measurements



Appendix D: M File switch_control3a.m (algorithm used in conjunction with Matlab model of Appendix C)

```
function [y]=switch_control3a(u)
%This function uses the sliding mode principle to set the positions of 6
%3/2H-Bridge switches
%T and lambda must be set in the workspace



%Constants and initial value defaults
C=1000e-6;
fast_inductor=0;
%not_absorbed=1; %default value

pos=0;
neg=0;

%Input variable assignment
Vref=u(1);
Is=u(2);
Vc_old=u(3);
Vc_new=u(4);
flag=u(5);
DIf=u(7);
%sw's take on old values (from last sample period)
s4=u(8);
s3=u(9);
s2=u(10);
s1=u(11);
x=u(12);
xdot=u(13);
s1a=u(14);
s3a=u(15);
DIfref=u(16);
Vcaprefnew=u(17);
lambda=u(18);
flag1=u(19);
Ifref=u(20);

%Check flag: 1 cycle start up hold-off
if(~flag)
    Kold=0.05; %initial value of conductance
else
    Kold=u(6);
end


if(lambda == 0)
    Vd=Vc_new-Vc_old; %(used when capacitor is allowed to settle to optimum
                %    value i.e. when lambda = 0)
else
    Vd=Vc_new-Vcaprefnew; %Used for sliding control of capacitor Voltage
end


%Ensure sufficient energy transfer to get capacitor almost to target Voltage.
```

```
%Forcing the capacitor Voltage above the target Voltage will increase
%the settling time of K
if((flag) && (Vc_new < 500))    %500V < 550 reference Voltage
   Kold=Kold+0.01;
end

if(flag)
if(lambda == 0)
      E=0.5*C*Vd*(Vc_old + Vc_new); %(used when capacitor is allowed to settle to optimum
                                    % value i.e. when lambda = 0)
   else
      E=0.5*C*Vd*(Vcaprefnew + Vc_new);
   end



Knew=Kold-E/1152;    %1152=240*240*0.02
   if(Knew < 0)
      Knew = 0;       %Prevent phase reversal of Isref when capacitor Voltage has large
 %                    positve increments
end
else
   Knew=Kold;
end

Isref=Knew*Vref;



check_sw=~(s1|s2|s3|s4); %check_sw is 1 only if all sw's are 0 i.e. end of a passive phase


if(Vref > 0.1)
   pos=1; %corresponding to Alpha = 1
end

if(Vref < 0.1)
   neg=1; %corresponding to Alpha = -1
end

%Assign "S" to the sliding surface
S=xdot; %default sliding surface

if(pos)
   S=x*lambda+xdot;    %Sliding surface when Alpha = 1
end
if(neg)
   S=-x*lambda+xdot;   %Sliding surface when Alpha = -1
end


% The following four variables are active phase indicators
pos_del_inc=0; %reset positive supply, power delivered to source, increasing
pos_abs_inc=0; %reset positive supply, power absorbed from source, increasing
neg_del_inc=0; %reset negative supply, power delivered to source, increasing
neg_abs_inc=0; %reset negative supply, power absorbed from source, increasing

%Use the previous sample switch states (from switch sampler) to assign
%values to the active phase indicators.
if(s1&&s4&&~s2&&~s3)
```

```
    pos_del_inc=1;
end

if(s3&&~s1&&~s2&&~s4)
    pos_abs_inc=1;
end

if(s3&&s2&&~s1&&~s4)
    neg_del_inc=1;
end

if(s1&&~s2&&~s3&&~s4)
    neg_abs_inc=1;
end


%now reset all sw's
s1=0;
s2=0;
s3=0;
s4=0;

Ifref_gate=0; %defualt value
%The following four IF conditions assume a passive state and set
%Ifref_gate accordingly. Ifref_gate may later be overridden if the state is
%active.
if(pos && (Ifref > 0)) %passive state and energy flowing into capacitor
    Ifref_gate = 1;
end
if(neg && (Ifref < 0))  %passive state and energy flowing into capacitor
    Ifref_gate = 1;
end
if(pos && (Ifref < 0))  %passive state and energy flowing out of capacitor
    Ifref_gate = -1;    %reverse current reference to match that flowing into capacitor
end
if(neg && (Ifref > 0))  %passive state and energy flowing out of capacitor
    Ifref_gate = -1;    %reverse current reference to match that flowing into capacitor
end

Is_error = Isref-Is; % error in source current, also equal to error in APF current (Ifref - If)

%The next section checks the system state against the sliding surface and
%decides if the next state should be active and then sets the switches
%accordingly.
%A signal "Ifref_gate" is produced to gate Ifref before integration to
%produce Vcapref
%Also the reachability condition is used to determine if the the fast
%inductor is required to increase the rate of change of APF current.

%Supply Voltage positive (Alpha = 1)
    if(pos)
        if(S < 0)
            if(check_sw||pos_del_inc)
                % delivered increasing
                s1=1;
                s4=1;
                Ifref_gate=1;   % active delivered state
            end
            %check reachability condition and switch "fast_inductor" if necessary
            if(abs(DIfref)-abs(DIf) > -lambda*abs(Is_error))
```

```
140.              fast_inductor = 1;
141.           end
142.        end

143.       if(S > 0)
144.           if(check_sw||pos_abs_inc)
145.              % Absorbed increasing
146.              s3=1;
147.              Ifref_gate=0; % active absorbed state
148.           end
149.           %check reachability condition and switch "fast_inductor" if necessary
150.           if(abs(DIfref) > abs(DIf))
151.              fast_inductor=1;
152.           end
153.        end
154.    end

155.%Supply Voltage negative (Alpha = -1)
156.    if(neg)
157.       if(S > 0)
158.           if(check_sw||neg_del_inc)
159.              % delivered increasing
160.              s3=1;
161.              s2=1;
162.              Ifref_gate = 1; % active delivered state
163.           end
164.           %check reachability condition and switch "fast_inductor" if necessary
165.           if(abs(DIfref)-abs(DIf) > -lambda*abs(Is_error))
166.              fast_inductor=1;
167.           end
168.        end

169.      if(S < 0)
170.           if(check_sw||neg_abs_inc)
171.              % absorbed increasing
172.              s1=1;
173.              Ifref_gate=0; %active absorbed state
174.           end%check reachability condition and switch "fast_inductor" if necessary
175.           if(abs(DIfref) > abs(DIf))
176.              fast_inductor=1;
177.           end
178.        end
179.    end

180.%At this point, if all switches are zero then the next phase will be
181.%passive.

182.if(~(s1||s2||s3||s4)) %clear fast inductor at start of passive phase
183.    s1a=0;
184.    s3a=0;
185.end


186.%fast half bridge control
187.%To satisfy Lyapunov reachability condition S(t).Sdot(t) < 0
188.if(fast_inductor)
189.%Copy s1 to s1a and s3 to s3a so L1 and L2 operate in parallel
190.    s1a=s1;
191.    s3a=s3;
192.end
```

```
%override switch control for first sample period of T to allow bridge to
%initialise
if(~flag1)
    s1=0;
    s2=0;
    s3=0;
    s4=0;
    s1a=0;
    s3a=0;
end

%Update all output variables
y(1)=s1;
y(2)=s2;
y(3)=s3;
y(4)=s4;
y(5)=Knew;
y(6)=Isref;
y(7)=s1a;
y(8)=s3a;
y(9) = Ifref_gate;
y(10)=S;
```

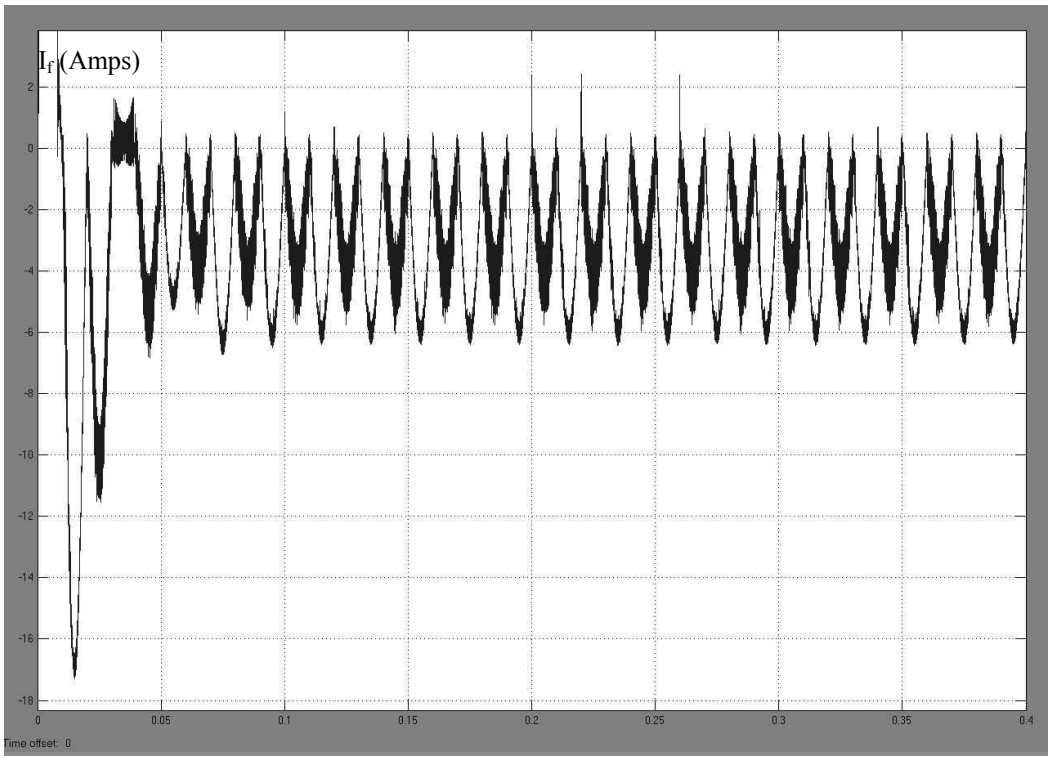
Appendix E: M File freqplot3.m (used to analyse the output of the Matlab model of Appendix C and Appendix G)

```
%parameter arrays in the order If,IL,Is,timelength
%timelength is normally 400ms
function [y]=freqplot3(var_array1,var_array2,var_array3,timelength)
timesample=0:1e-6:timelength; %each step is 1us
%resample data to an even time step
%effective sample rate is 1MHz

var_resample1=spline(var_array1(:,1),var_array1(:,2),timesample);%resample If
var_resample2=spline(var_array2(:,1),var_array2(:,2),timesample);%resample IL
var_resample3=spline(var_array3(:,1),var_array3(:,2),timesample);%resample Is
start_time=timelength*0.5*1e6;   % reject 1st half of waveform-typically first 200ms of
                                 %timesample are not used. Start time in us

stop_time=timelength*1e6;        % 100% of timelength in us
N=stop_time - start_time;        %N = no of sample points after resampling (typically N=200000)
%N corresponds to typically 200ms with each sample point correspndng to 1us
%The fundamental frequency of the following FFT is 1/200ms or 5Hz
freqplot1=fft(var_resample1(start_time:stop_time),N); %freq plot for If
freqplot2=fft(var_resample2(start_time:stop_time),N); %freq plot ofr IL
freqplot3=fft(var_resample3(start_time:stop_time),N); %freq plot for Is

%evaluate RMS values for If, Il Is
%magnitude plot = (2/N)*sqrt(freqplot.*conj(freqplot))
%RMS magnitude plot = (2/N)*sqrt(freqplot.*conj(freqplot)/2)
If_RMS_frqplot=(2/N)*sqrt(freqplot1.*conj(freqplot1)/2); %spectrum of If RMS
IL_RMS_frqplot=(2/N)*sqrt(freqplot2.*conj(freqplot2)/2); %spectrum of IL RMS
Is_RMS_frqplot=(2/N)*sqrt(freqplot3.*conj(freqplot3)/2); %spectrum of Is RMS
If_RMS_frqplot(1)=If_RMS_frqplot(1)*0.5*sqrt(2);   %correct dc term
IL_RMS_frqplot(1)=IL_RMS_frqplot(1)*0.5*sqrt(2);   %correct dc term
Is_RMS_frqplot(1)=Is_RMS_frqplot(1)*0.5*sqrt(2);   %correct dc term

freqstep=1e6/N; %typically freqstep is 5Hz
freqaxis=(0:N/2)*freqstep; %each freq point represents 5 Hz with typical input parameters
%Only plot up to 200 frequency points (i.e. typically 1kHz)
subplot(3,1,1);
plot(freqaxis(1:200),If_RMS_frqplot(1:200))
title('Spectrum of If RMS');
ylabel('If RMS Amps');
grid on;
subplot(3,1,2);
plot(freqaxis(1:200),IL_RMS_frqplot(1:200))
title('Spectrum of IL RMS');
ylabel('IL RMS Amps');
grid on;
subplot(3,1,3);
plot(freqaxis(1:200),Is_RMS_frqplot(1:200))
title('Spectrum of Is RMS');
xlabel('frequency(Hz)');
ylabel('Is RMS Amps');
grid on;
% store RMS levels for the first 40 harmonics of 50Hz
Hz50step=50/freqstep;   %freqstep is typically 5Hz
IfRMS_50Hz_harm=If_RMS_frqplot(1+Hz50step:Hz50step:1+40*Hz50step);  %index 1 is the dc
```

```
                                                                    %term
ILRMS_50Hz_harm=IL_RMS_frqplot(1+Hz50step:Hz50step:1+40*Hz50step);
IsRMS_50Hz_harm=Is_RMS_frqplot(1+Hz50step:Hz50step:1+40*Hz50step);

%Evaluate THD for IL and Is
%This is the sq root of the sum of ratio of the mean square value of the 50Hz harmonics (harm nos
% 2 to 40) relative to the mean square value of the fundamental 50Hz component

%evaluate THD for IL using the first 40 harmonics of 50Hz (i.e. up to 2000Hz)
sum1=0;
sum2=0;
fundamental_mean_sq = (IL_RMS_frqplot(Hz50step+1))^2;
for count=2:40
    index=count*Hz50step + 1;   %index 1 is dc term, index 11 is fundamental 50Hz term
    rms_current=IL_RMS_frqplot(index);
    meansq=rms_current^2;
   sum1=sum1+(meansq/fundamental_mean_sq); %sum of ratios relative to 50Hz fundamental
    sum2=sum2+meansq; %sum of mean squares of IL
end
thdIL=sqrt(sum1)
Total_harm_current_IL=sqrt(sum2)

R=0.25; %mains source resistance
L=796e-6; %mains source inductance

%evaluate THD for Is using the first 40 harmonics of 50Hz (i.e. up to 2000Hz)
sum1=0;
sum2=0;
voltsq=0;
fundamental_mean_sq = (Is_RMS_frqplot(Hz50step+1))^2;
for count=2:40
    index=count*Hz50step + 1;   %index 1 is dc term, index 11 is fundamental 50Hz term
    rms_current=Is_RMS_frqplot(index);
    meansq=rms_current^2;
    sum1=sum1+(meansq/fundamental_mean_sq); %sum of ratios relative to 50Hz fundamental
    sum2=sum2+meansq; %sum of mean squares of Is
    volt_real=rms_current*R;
    volt_imag=rms_current*2*pi*L*50*count;
    voltsq=voltsq+(volt_real^2 + volt_imag^2);
end
thdIs=sqrt(sum1)
Total_harm_current_Is=sqrt(sum2)
Total_harm_voltage=sqrt(voltsq)
THD_voltage = Total_harm_voltage/240

%transpose to columns
IfRMS_50Hz_harm=IfRMS_50Hz_harm';
ILRMS_50Hz_harm=ILRMS_50Hz_harm';
IsRMS_50Hz_harm=IsRMS_50Hz_harm';

freqcount=50:50:2000;
freqcount=freqcount';

format short g
y=[IfRMS_50Hz_harm,ILRMS_50Hz_harm,IsRMS_50Hz_harm,freqcount];
```

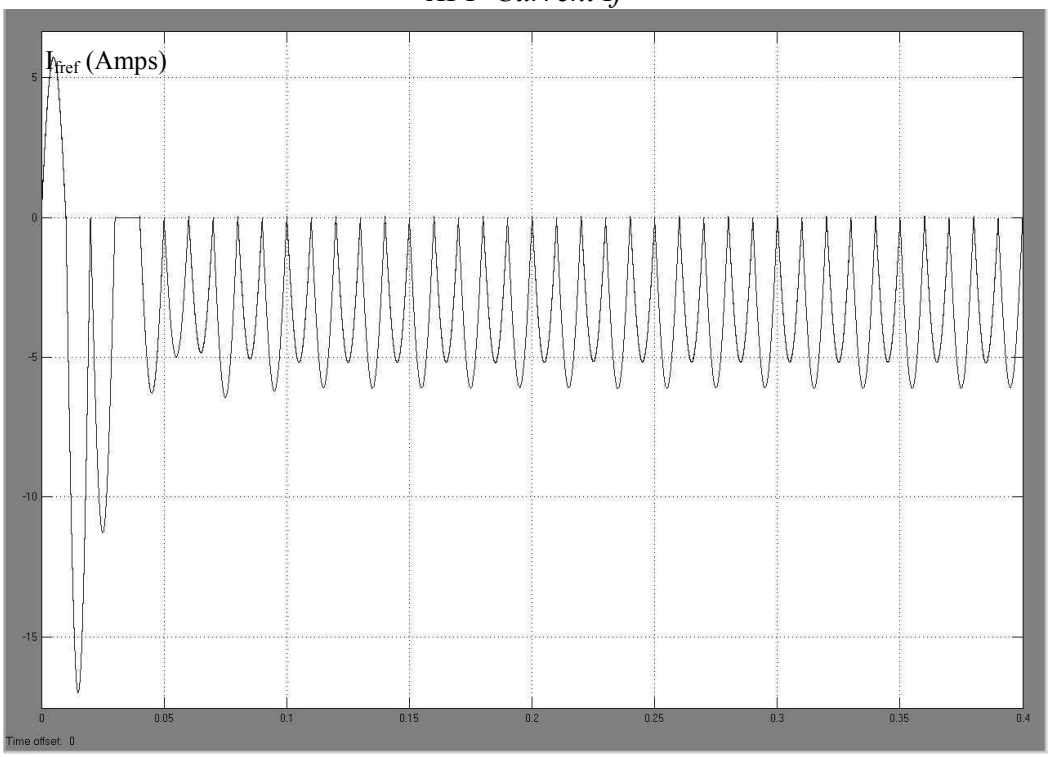
Appendix F: Result sets for sections 3.13.3, 3.13.4 and 3.13.5

Appendix F: Result Set 1a



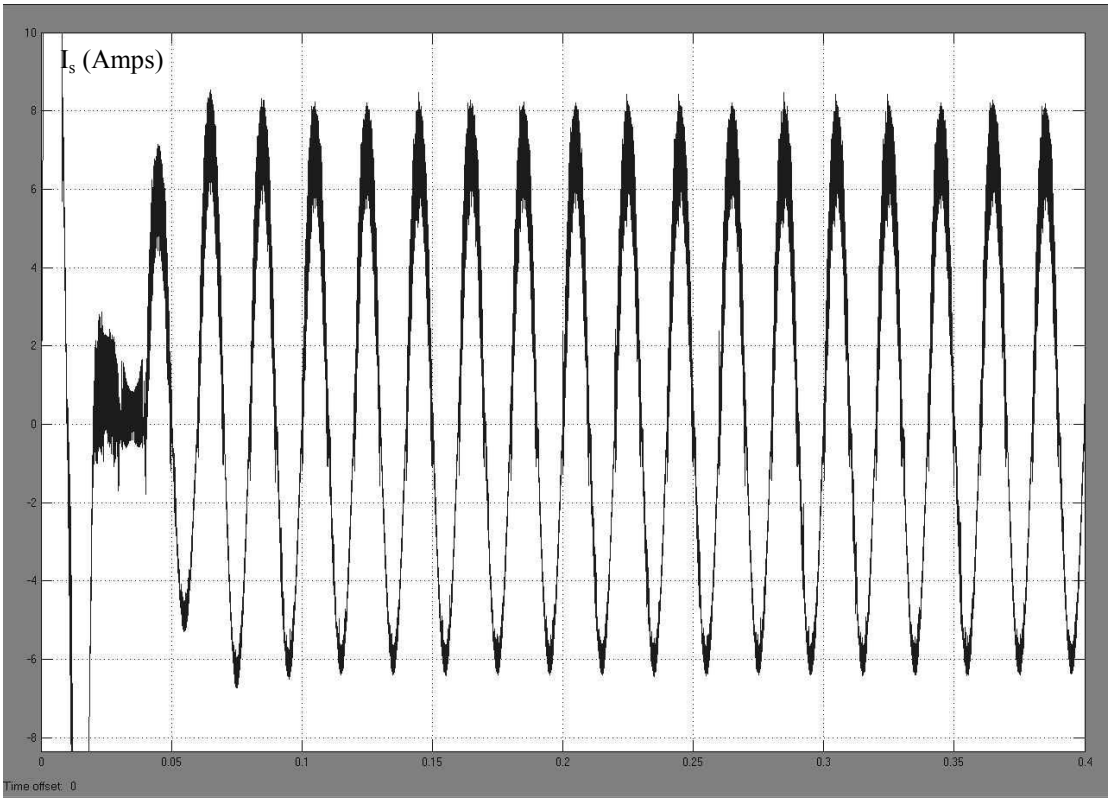
secs

APF Current If



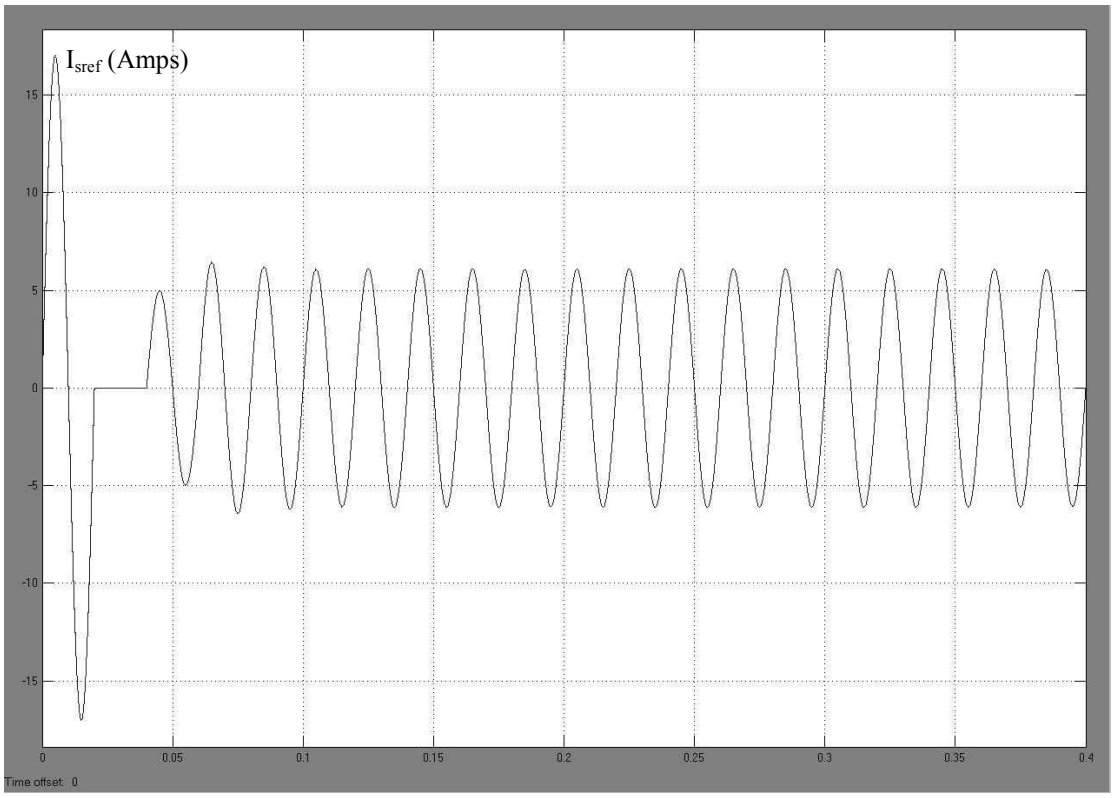
secs

APF reference current Ifref



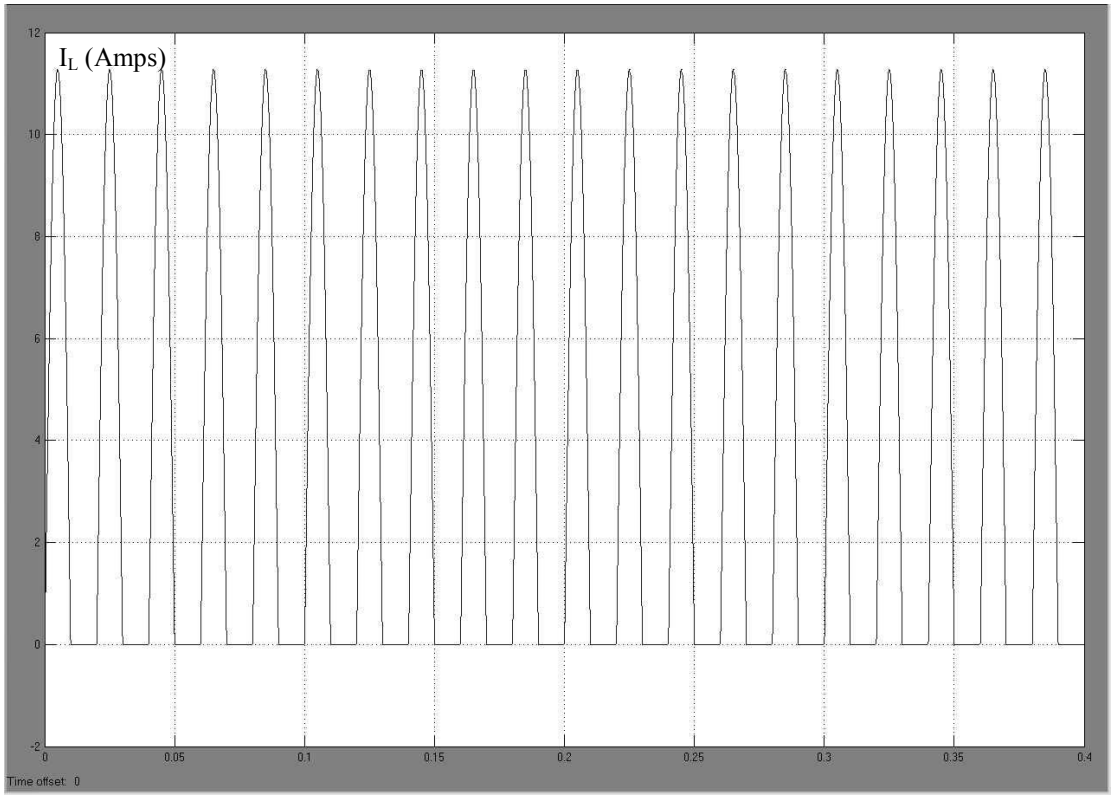
secs

Source current Is



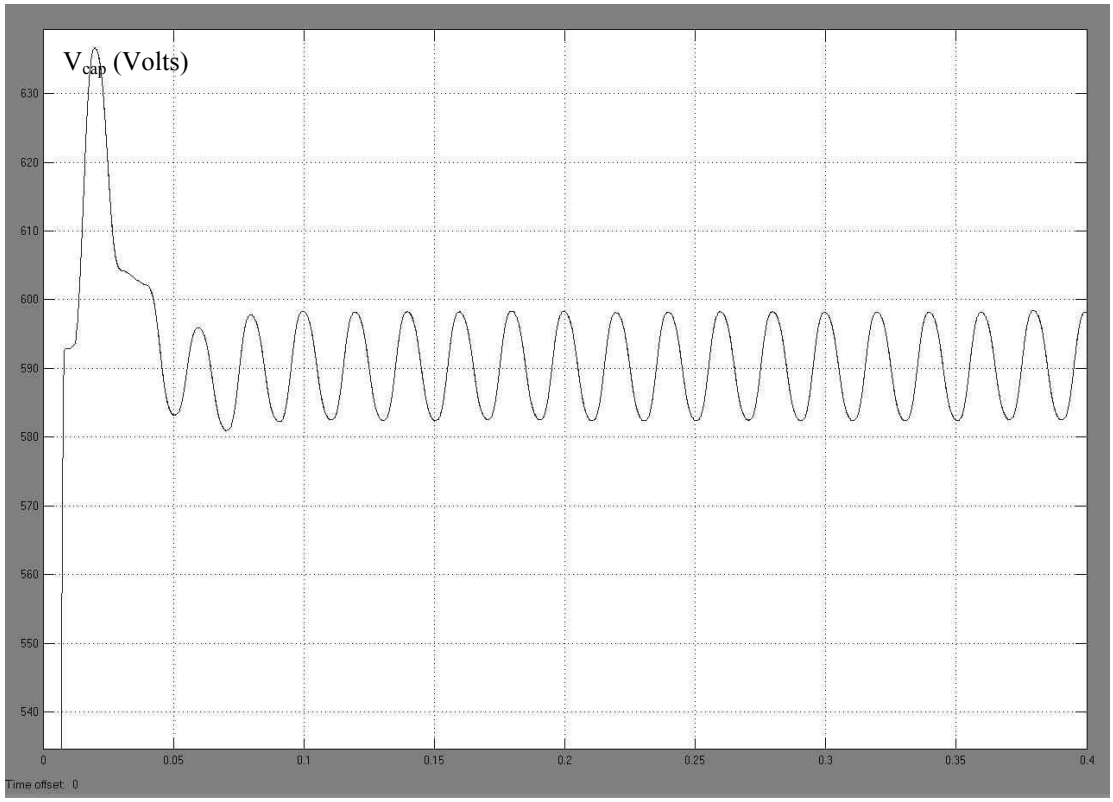
secs

Source reference current Isref



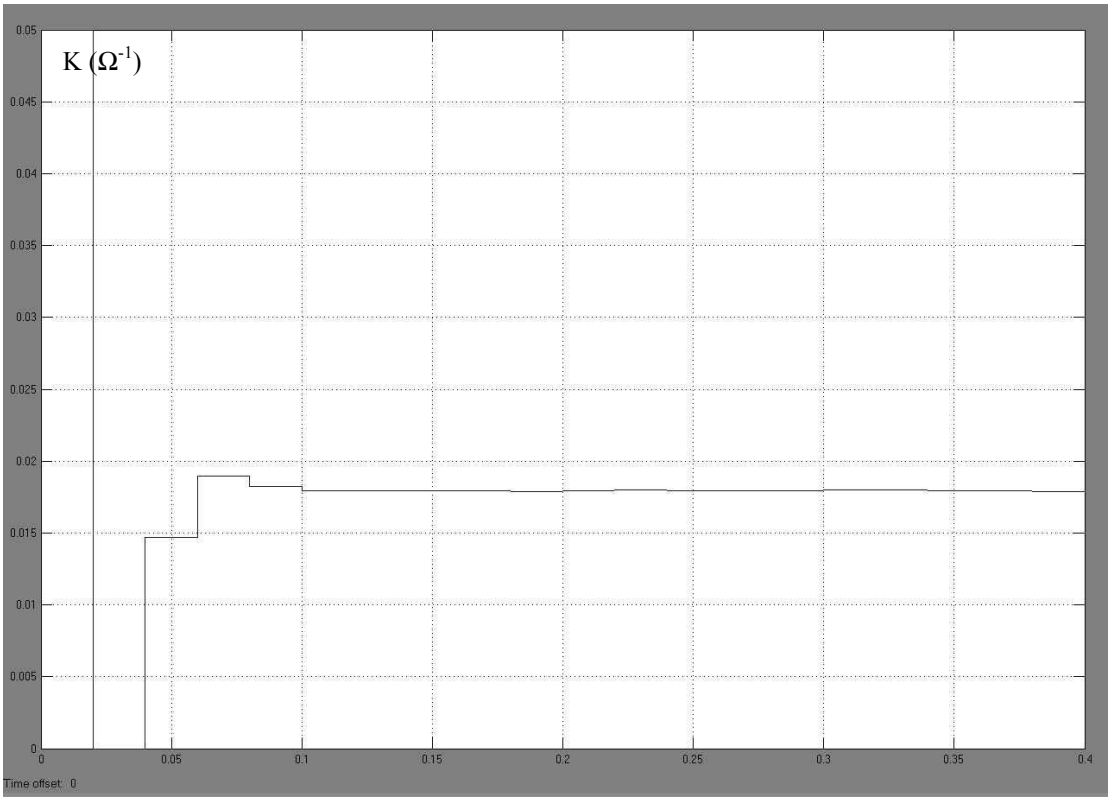
secs

Load current IL



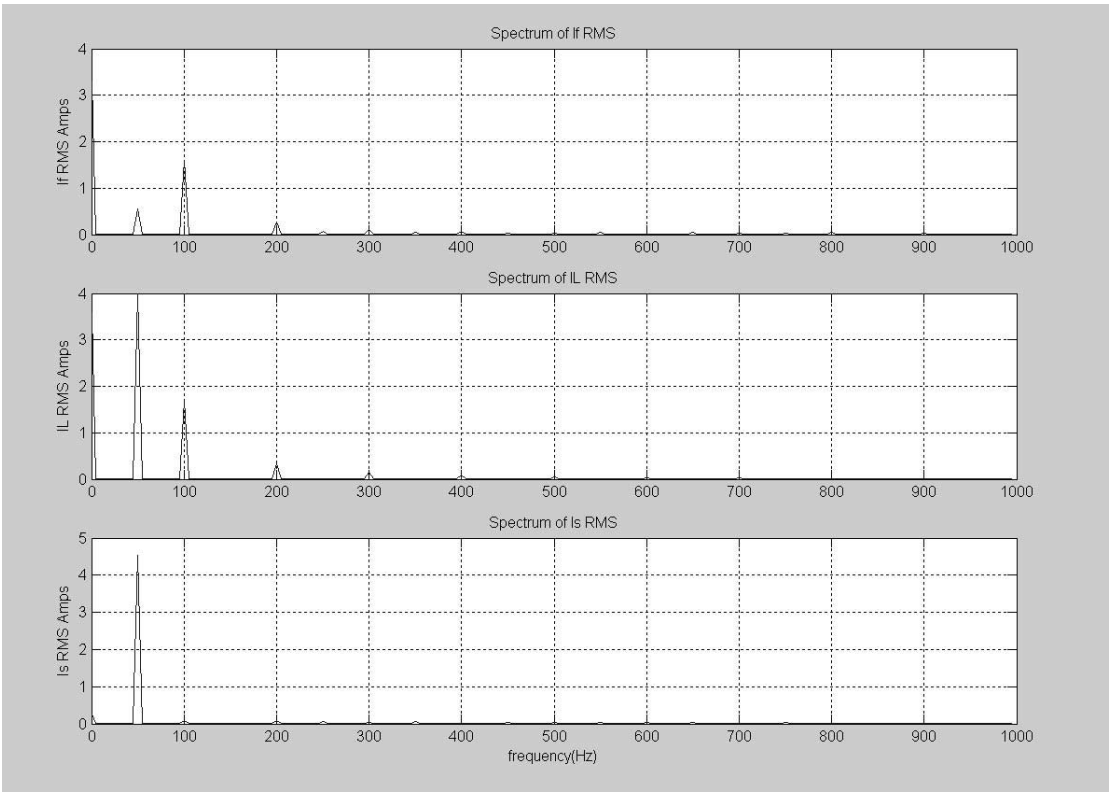
secs

Capacitor Voltage Vcap



secs

Conductivity of load (K)

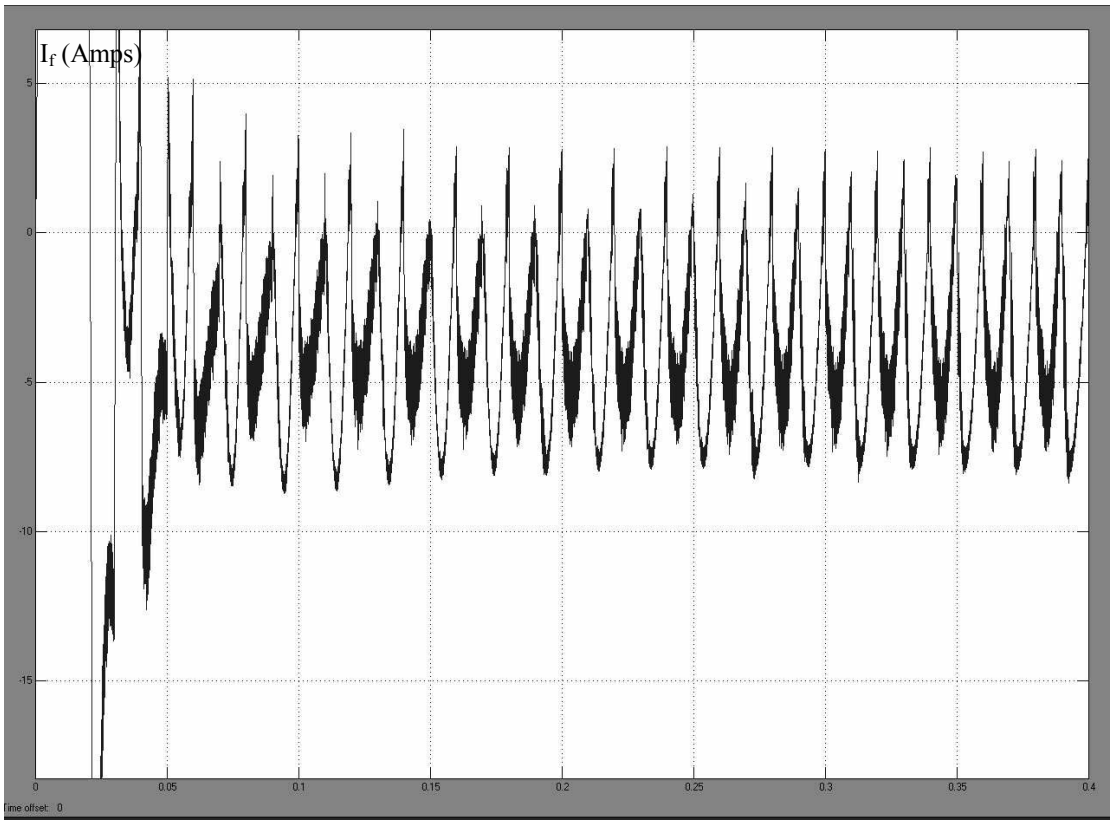


Spectrum of If, IL, Is up to 1kHz

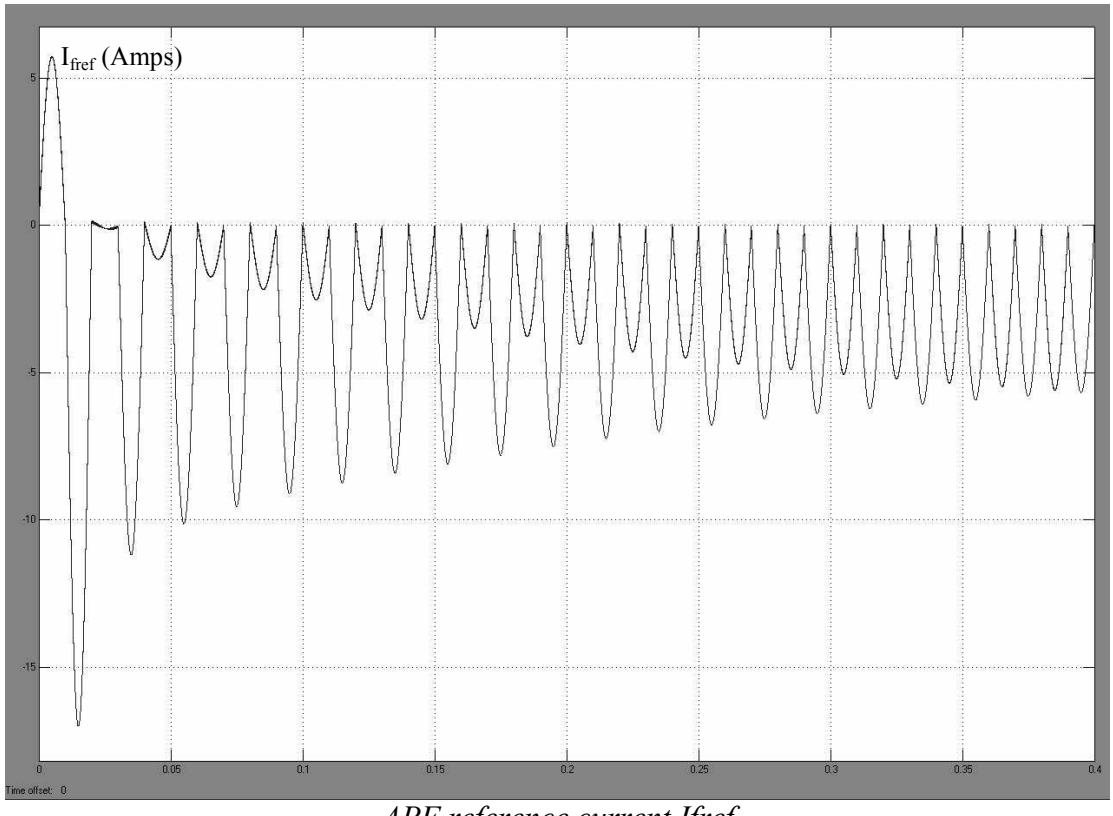
Table of RMS current Harmonics:

Table of RMS current Harmonics for Result Set 1a							
If RMS	IL RMS	Is RMS	Freq(Hz)	If RMS	IL RMS	Is RMS	Freq(Hz)
0.55775	3.9831	4.5407	50	0.0019011	0.0009766	0.0028638	1050
1.6028	1.6992	0.099389	100	0.019175	0.01038	0.010331	1100
0.018291	0.0069945	0.023803	150	0.0068322	0.00088759	0.0059481	1150
0.26565	0.33969	0.078856	200	0.016498	0.0086929	0.0084835	1200
0.063636	0.0041929	0.067829	250	0.006425	0.00081266	0.005914	1250
0.10754	0.14548	0.037959	300	0.018944	0.007381	0.012239	1300
0.048519	0.0029912	0.051505	350	0.01339	0.00074844	0.01265	1350
0.073479	0.080741	0.011247	400	0.007418	0.0063407	0.0073511	1400
0.027925	0.0023223	0.030244	450	0.0044245	0.00069302	0.0038743	1450
0.025387	0.051315	0.033189	500	0.0049503	0.0055023	0.010328	1500
0.041025	0.0018961	0.042879	550	0.0075862	0.00064439	0.0082275	1550
0.013041	0.035471	0.025195	600	0.001578	0.0048166	0.0063093	1600
0.044205	0.0016002	0.04579	650	0.020748	0.00060165	0.021308	1650
0.030559	0.025965	0.0077282	700	0.018366	0.004249	0.01417	1700
0.032052	0.0013828	0.03343	750	0.011389	0.00056349	0.011895	1750
0.041899	0.019814	0.02226	800	0.013634	0.0037736	0.0098609	1800
0.0058895	0.001216	0.0070914	850	0.014065	0.00052946	0.014117	1850
0.03001	0.015606	0.015143	900	0.0094916	0.0033718	0.0099115	1900
0.007566	0.0010839	0.0073212	950	0.004684	0.00049869	0.0051062	1950
0.018236	0.012601	0.0074512	1000	0.0067983	0.0030291	0.0053128	2000

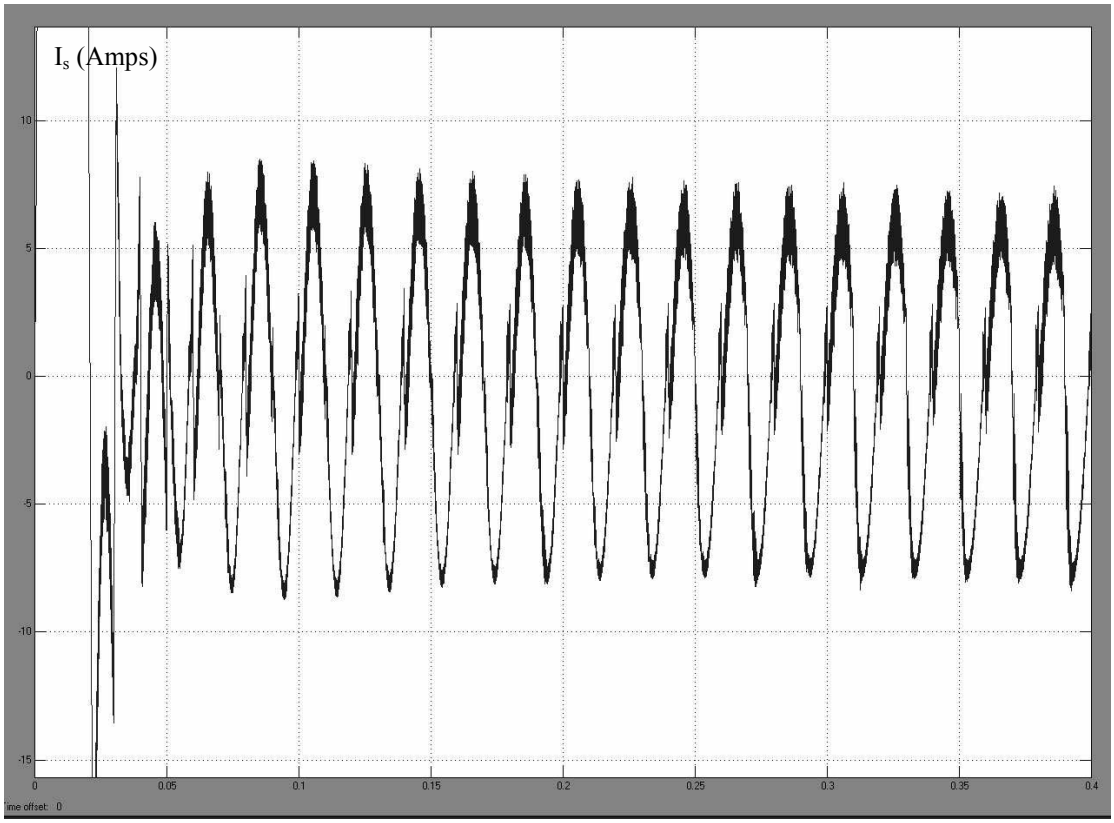
Appendix F: Result Set 1b



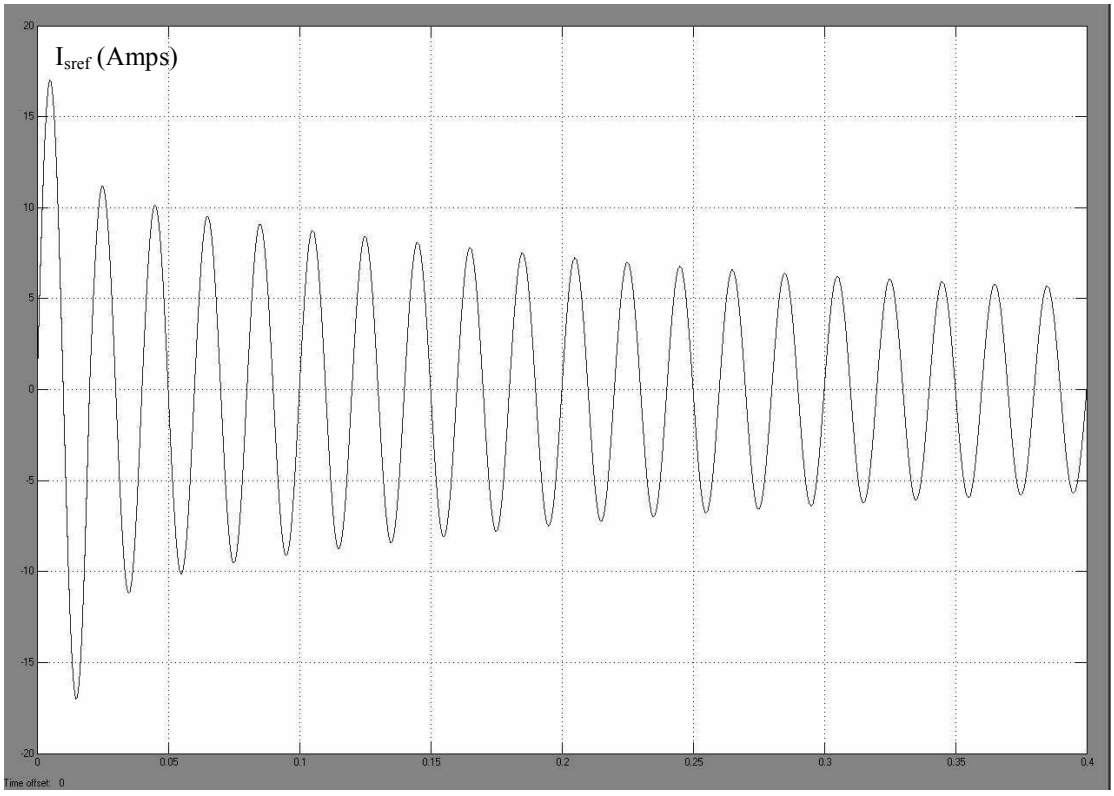
APF current If



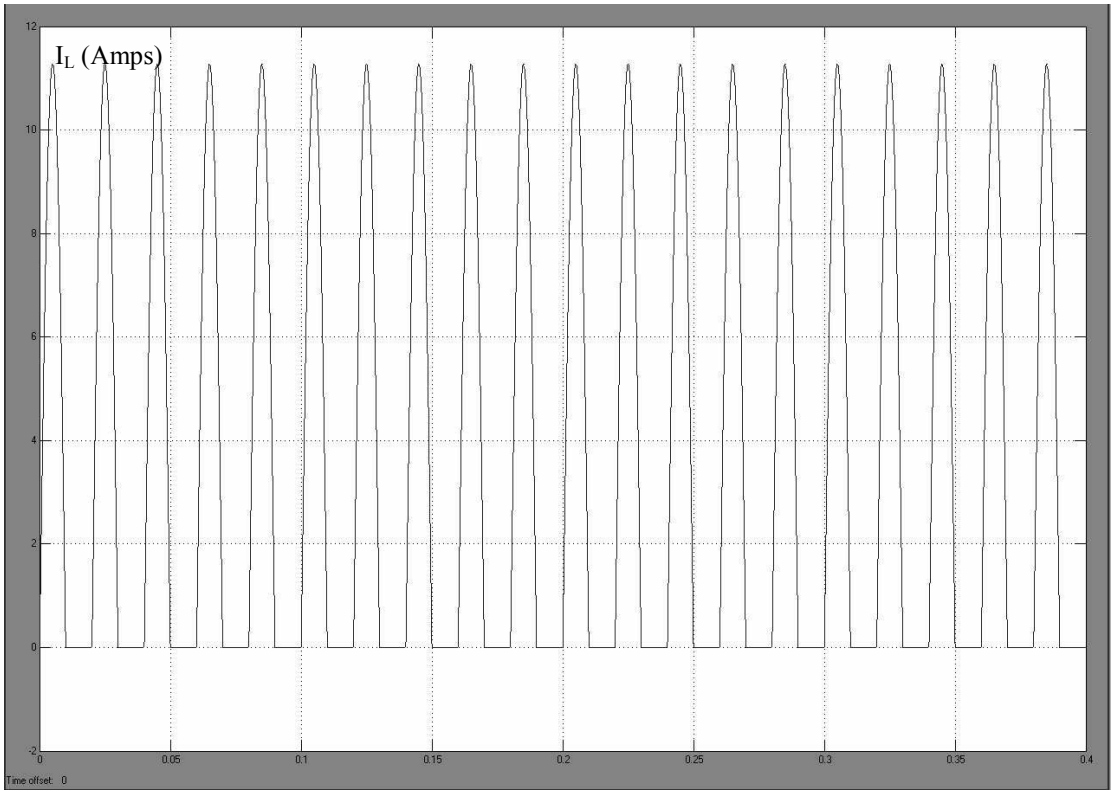
APF reference current Ifref



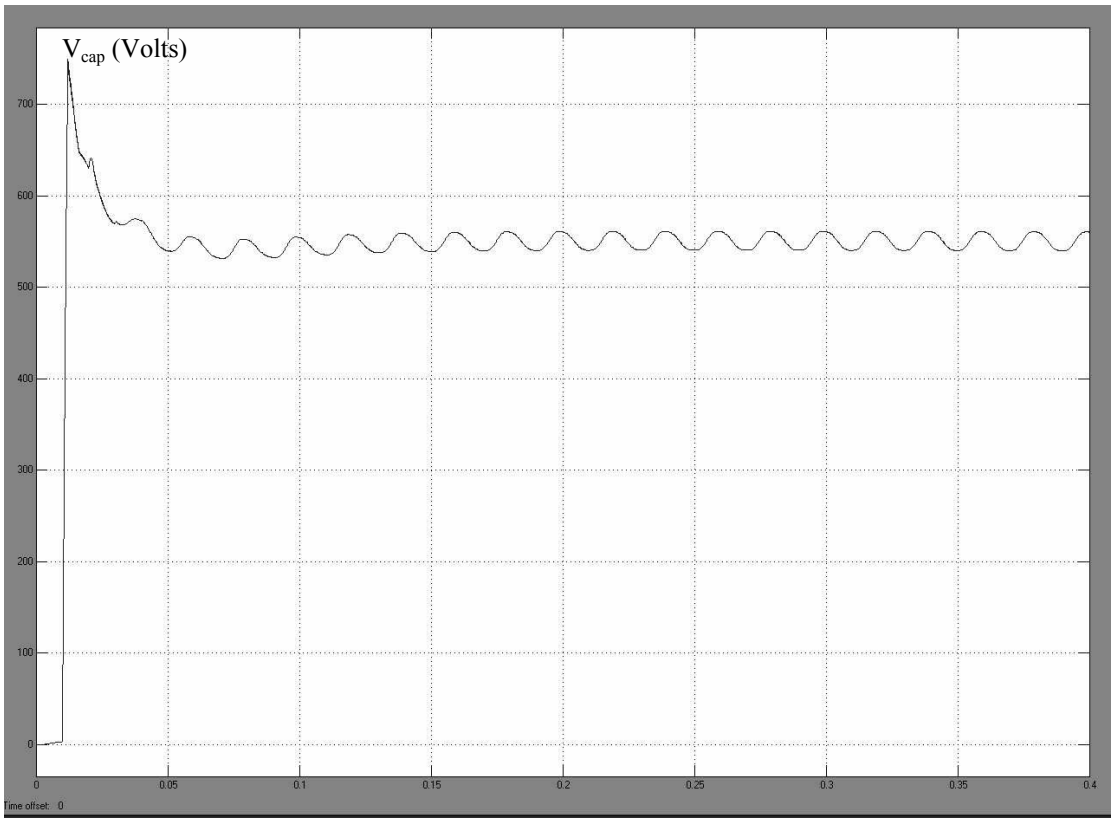
Source current Is



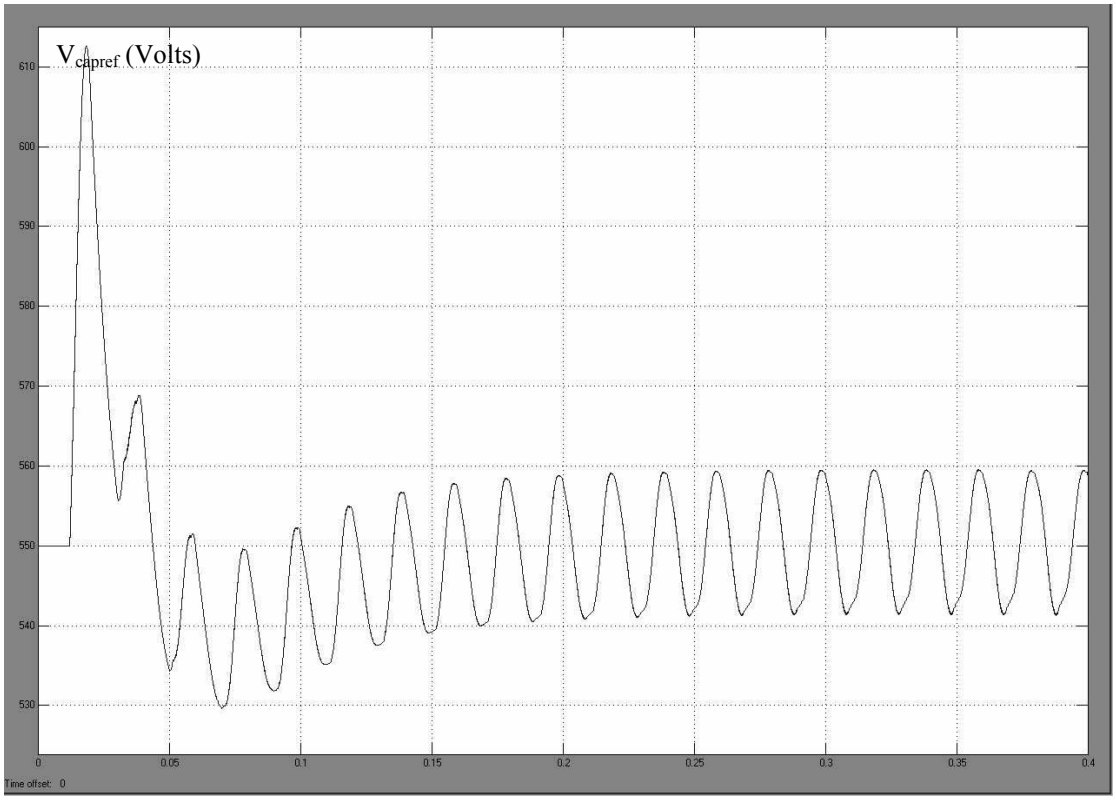
Source reference current Isref



Load current IL

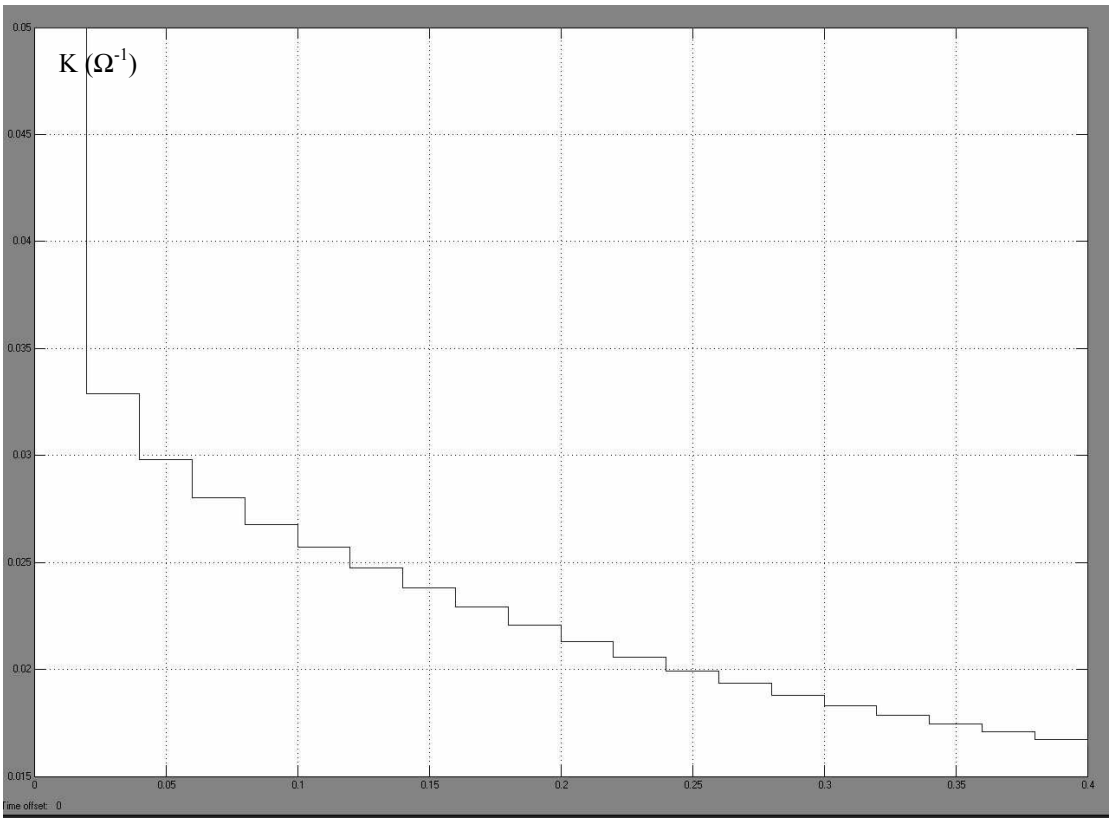


Capacitor Voltage Vcap



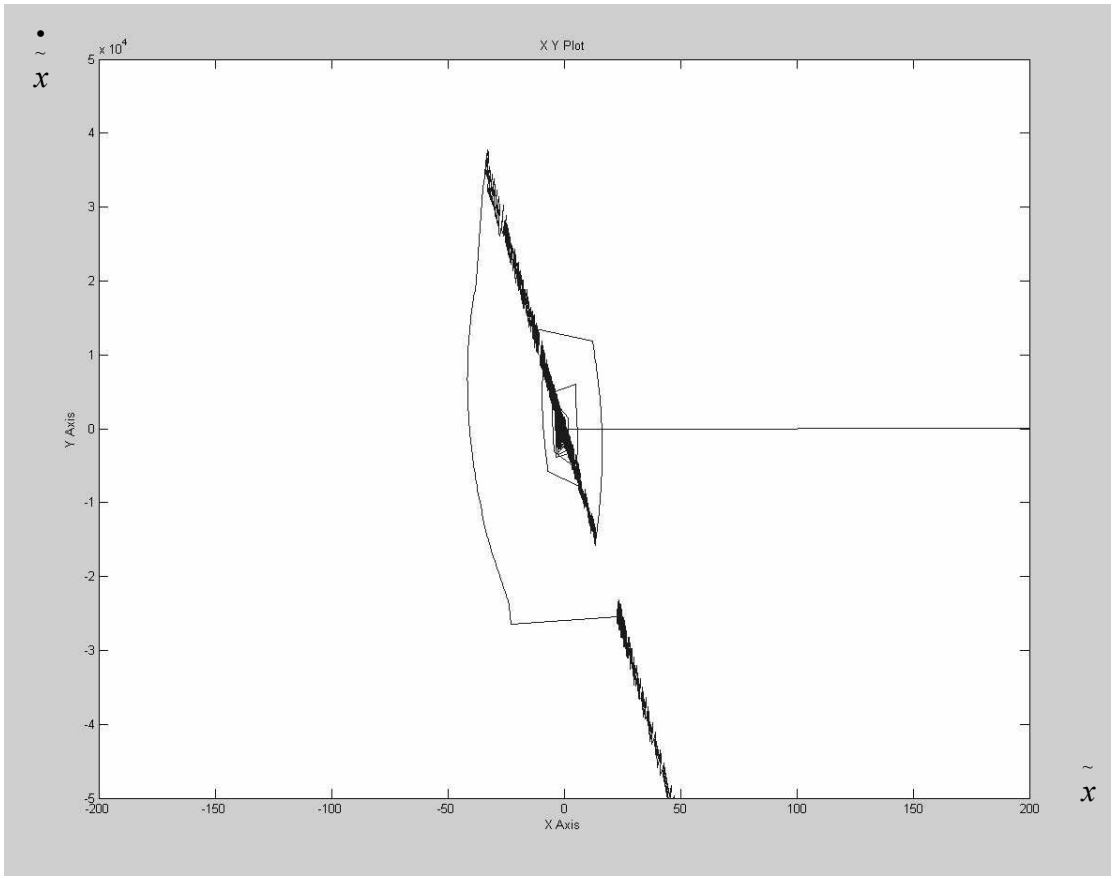
secs

Capacitor reference Voltage Vcapref

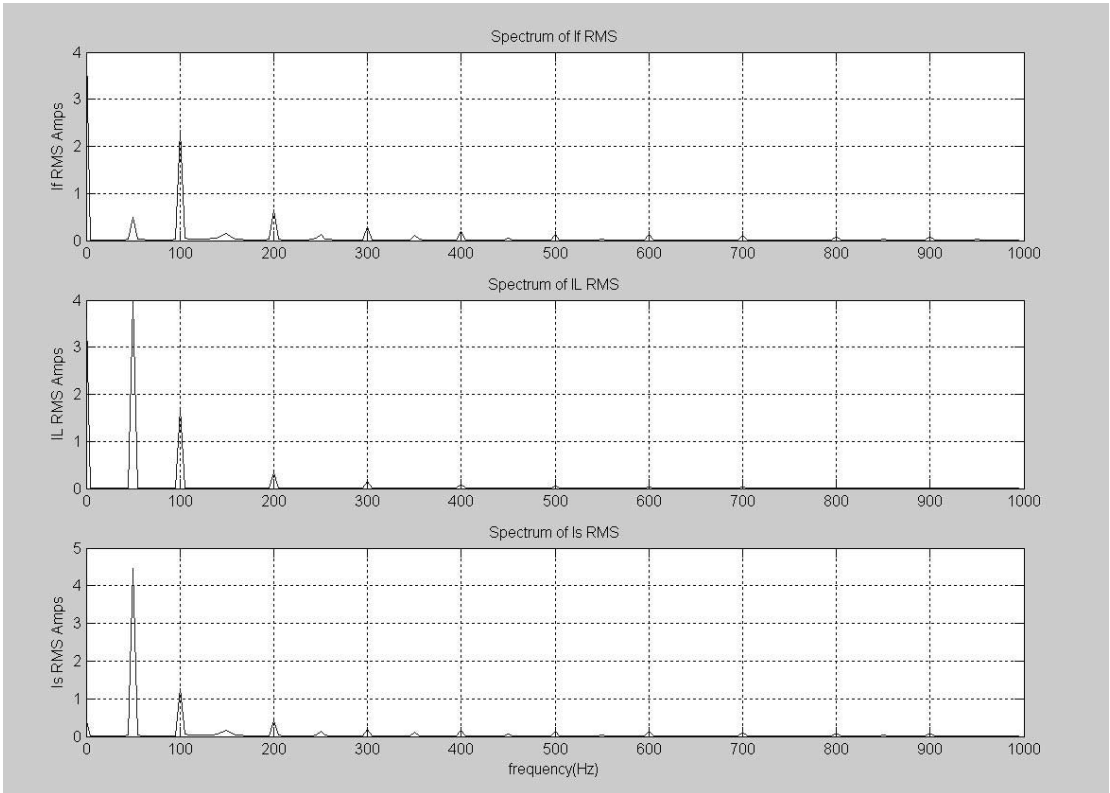


secs

Conductivity of load (K)



Sliding in state space

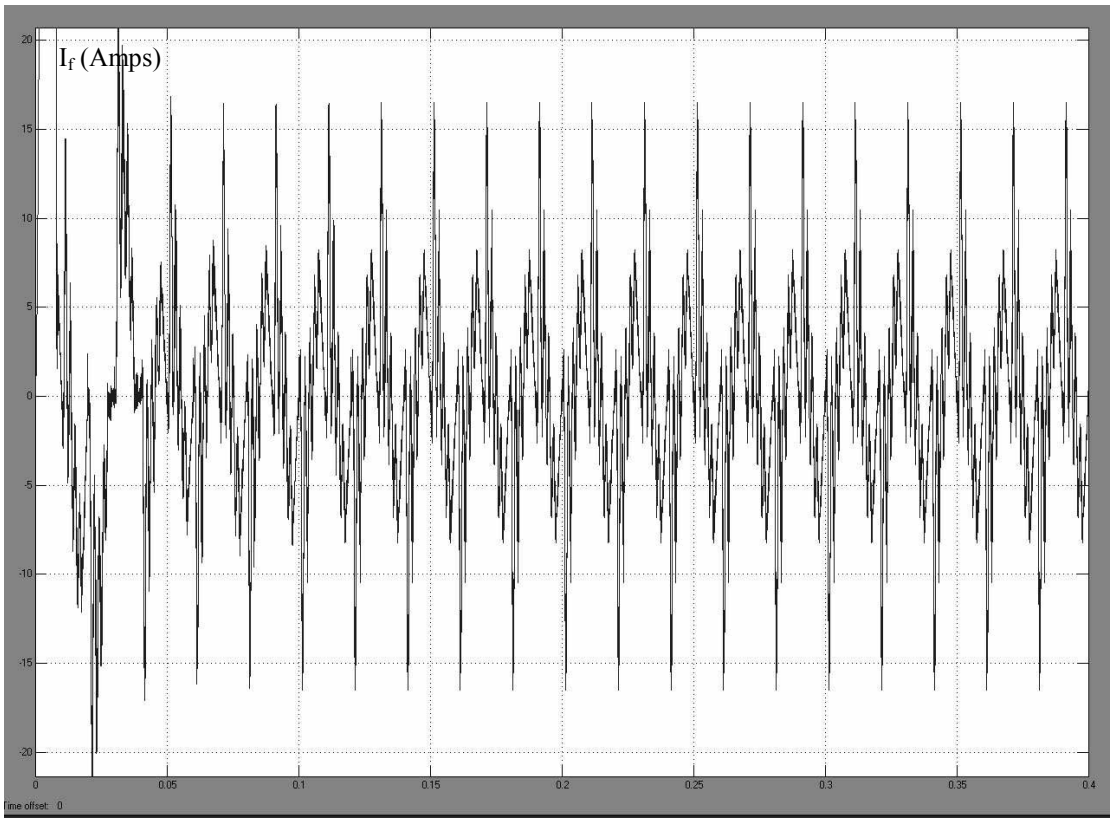


Spectrum of If, IL and Is up to 1kHz

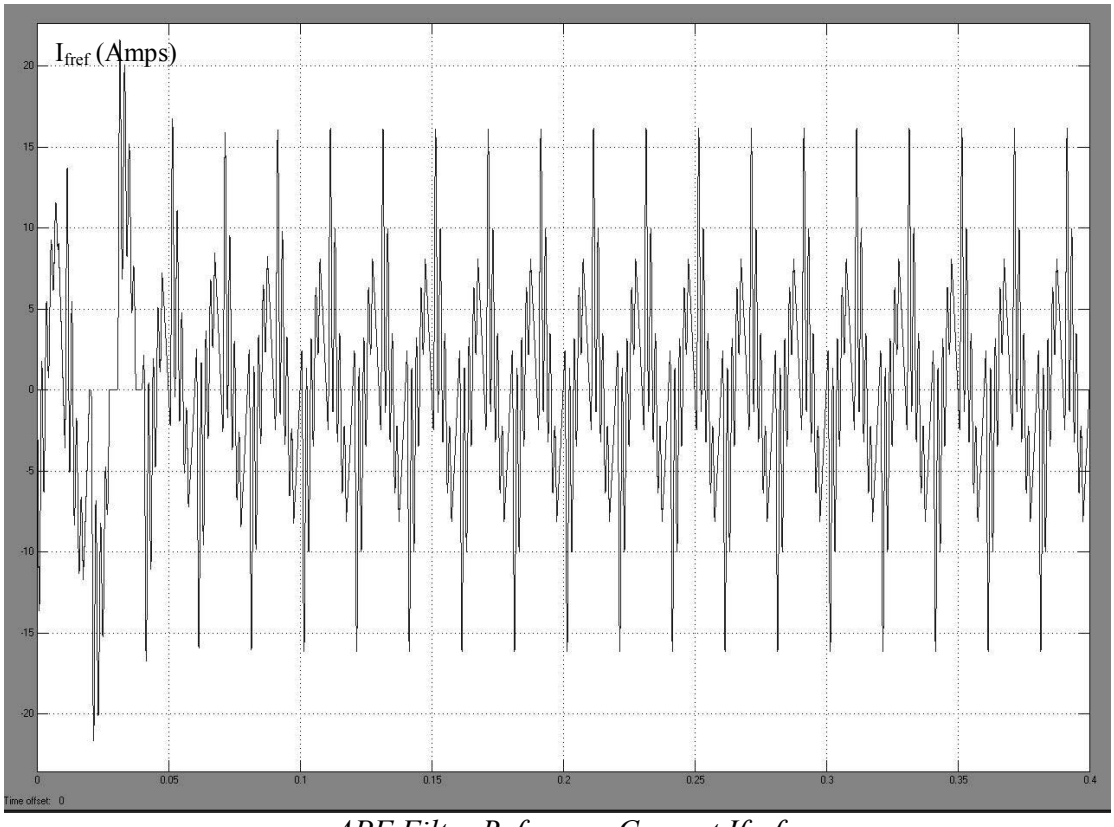
Table of RMS current Harmonics:

Table of RMS current Harmonics for Result Set 1b								
If RMS	IL RMS	Is RMS	Freq(Hz)		If RMS	IL RMS	Is RMS	Freq(Hz)
0.49354	3.9831	4.469	50		0.030611	0.0009766	0.031564	1050
2.3457	1.6992	1.2738	100		0.051654	0.01038	0.046041	1100
0.1608	0.0069945	0.16267	150		0.022008	0.00088759	0.022876	1150
0.65628	0.33969	0.42692	200		0.060688	0.0086929	0.055397	1200
0.13501	0.0041929	0.13883	250		0.018774	0.00081266	0.019114	1250
0.28945	0.14548	0.20084	300		0.066606	0.007381	0.061947	1300
0.10601	0.0029912	0.109	350		0.013535	0.00074844	0.013834	1350
0.18956	0.080741	0.15837	400		0.047331	0.0063407	0.043528	1400
0.059526	0.0023223	0.061354	450		0.022054	0.00069302	0.022701	1450
0.13756	0.051315	0.13269	500		0.03865	0.0055023	0.034544	1500
0.035807	0.0018961	0.036936	550		0.031054	0.00064439	0.031695	1550
0.13398	0.035471	0.12712	600		0.030377	0.0048166	0.026617	1600
0.01901	0.0016002	0.018471	650		0.020159	0.00060165	0.0207	1650
0.11928	0.025965	0.11307	700		0.021269	0.004249	0.020301	1700
0.0095256	0.0013828	0.010087	750		0.016726	0.00056349	0.01718	1750
0.098862	0.019814	0.091241	800		0.02477	0.0037736	0.024324	1800
0.026109	0.001216	0.026827	850		0.026926	0.00052946	0.027351	1850
0.086273	0.015606	0.078684	900		0.024397	0.0033718	0.023374	1900
0.020241	0.0010839	0.021319	950		0.029623	0.00049869	0.029976	1950
0.060681	0.012601	0.055058	1000		0.022998	0.0030291	0.022324	2000

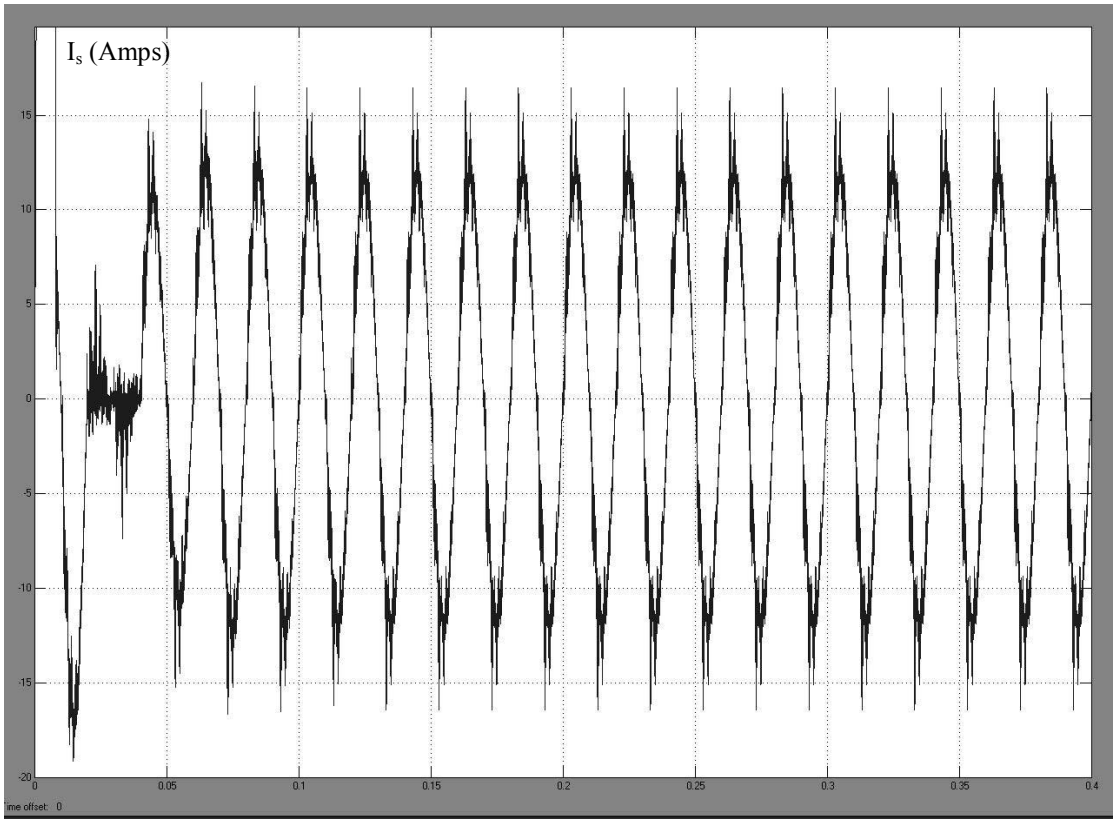
Appendix F: Result Set 2a



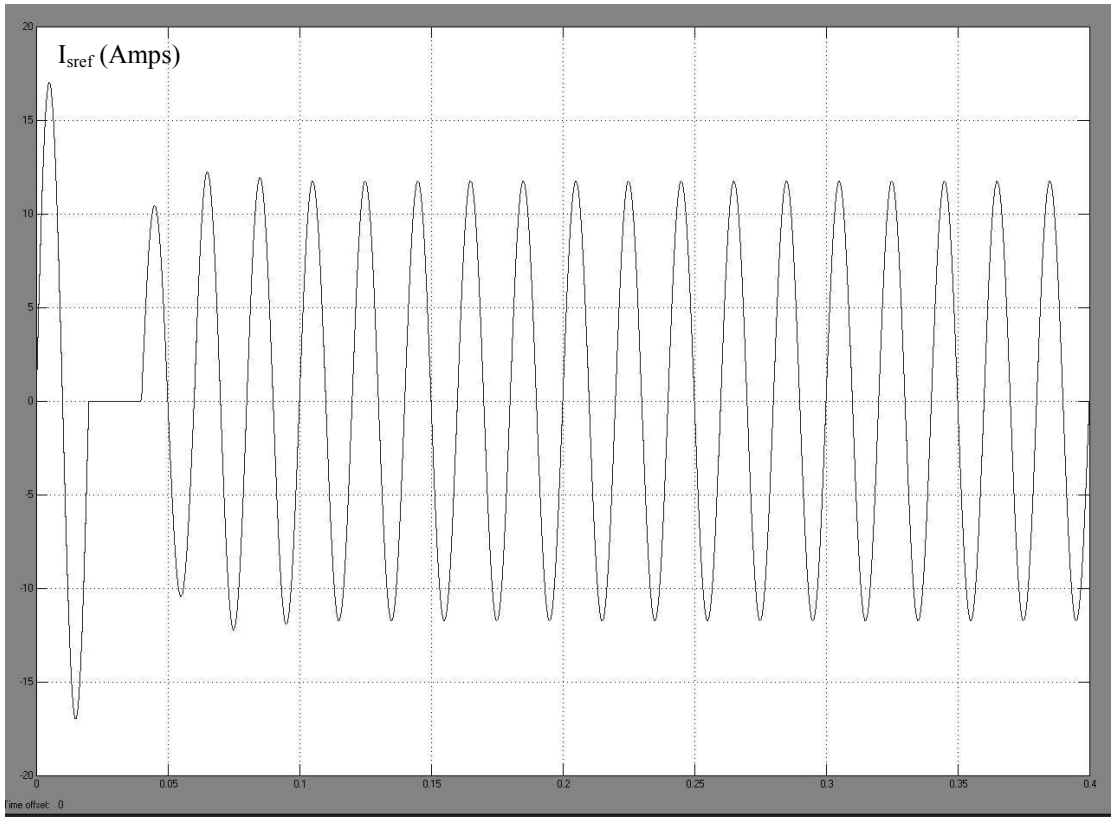
APF Filter Current If



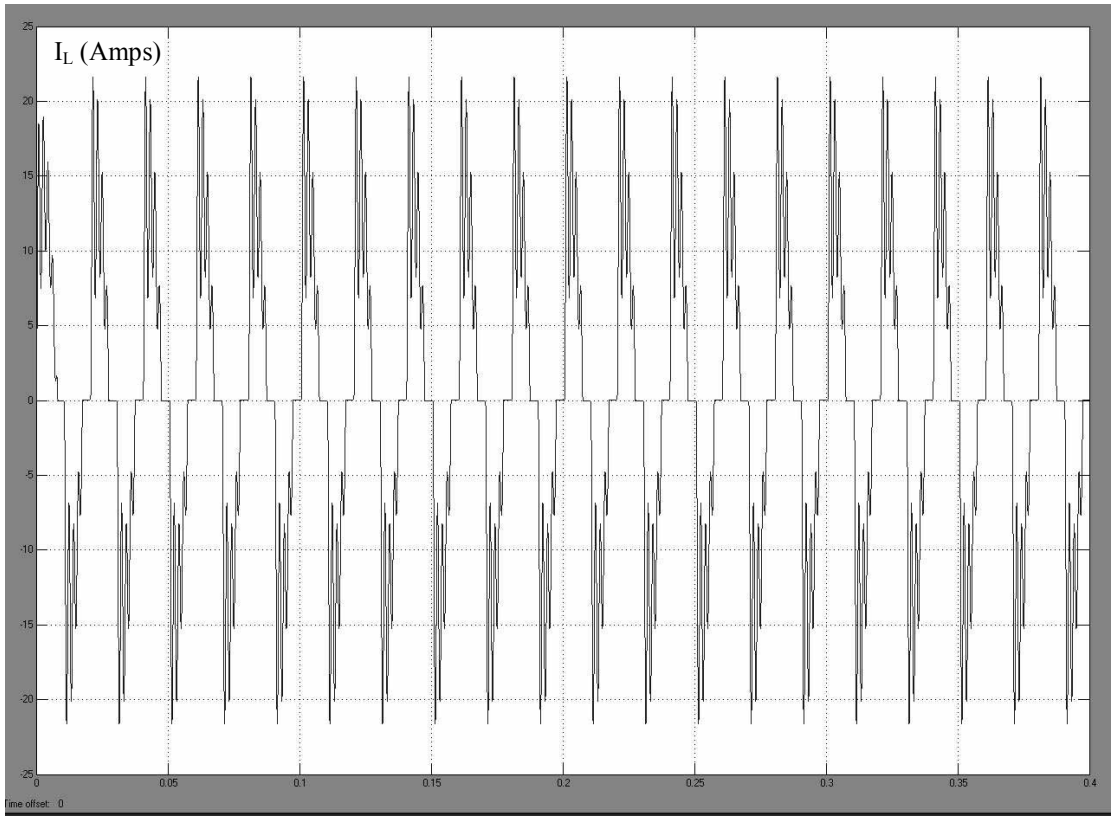
APF Filter Reference Current Ifref



Source Current Is

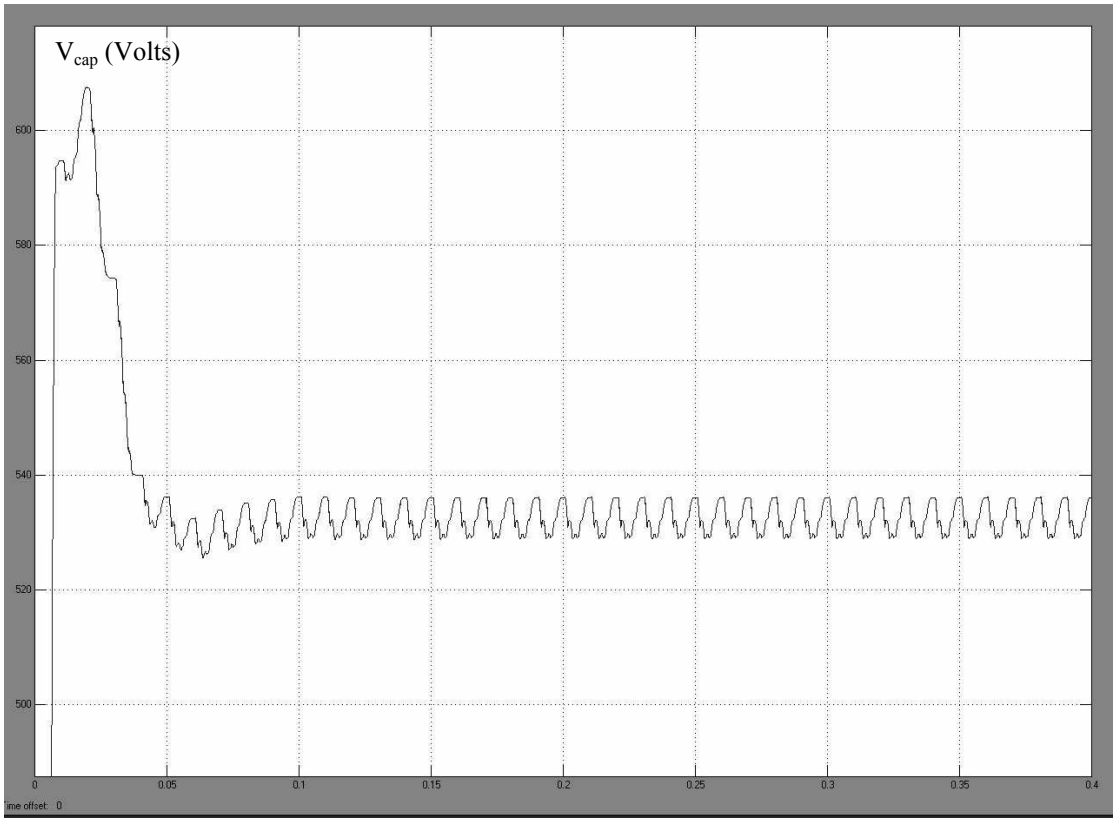


Source Reference Current Isref



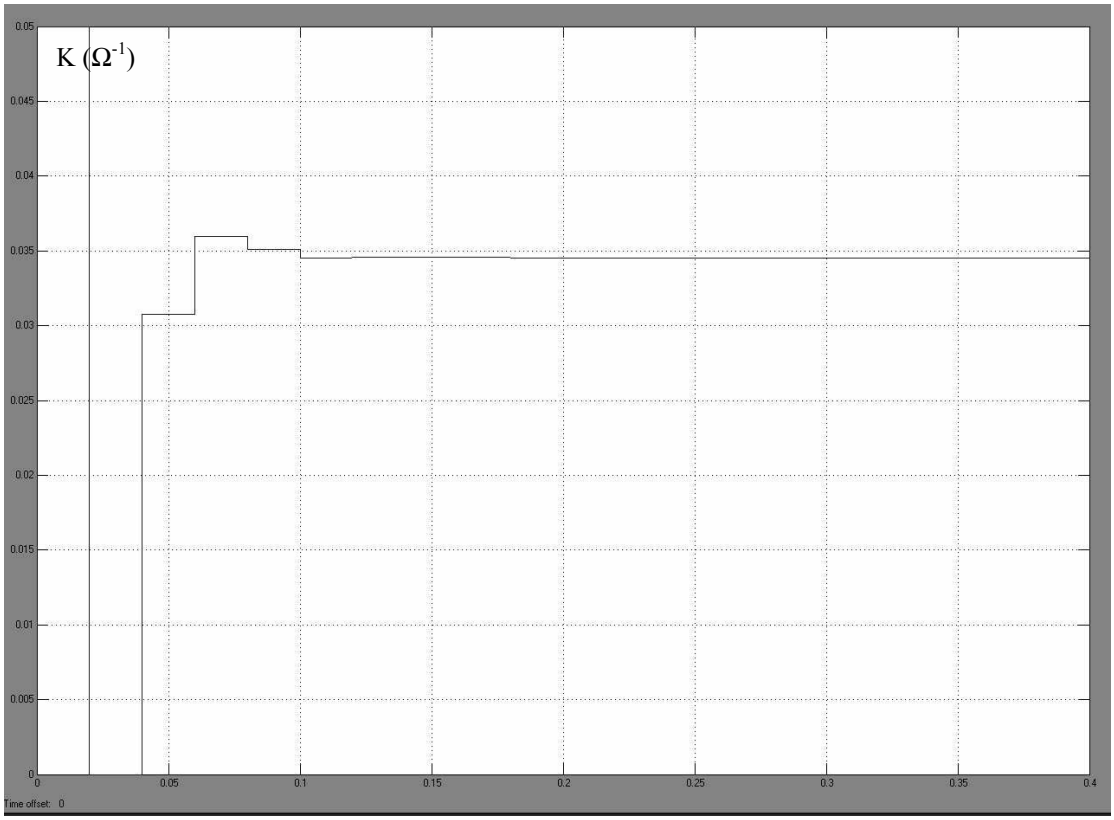
secs

Load Current IL



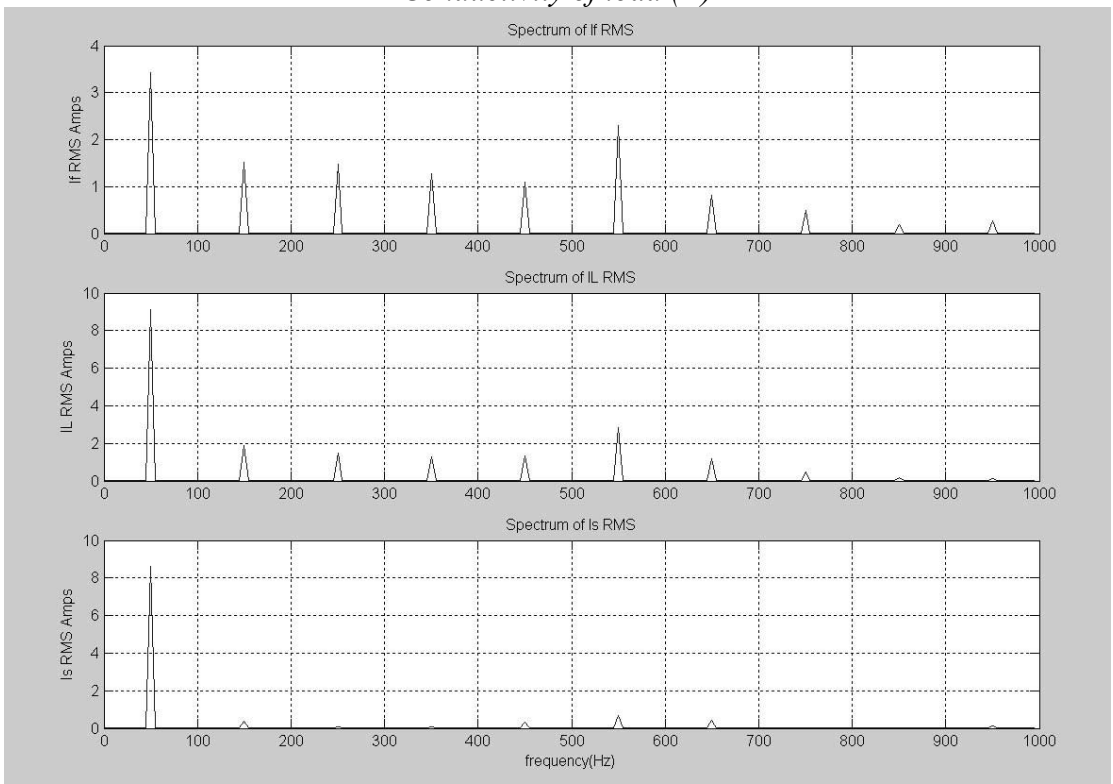
secs

Capacitor Voltage Vcap



secs

Conductivity of load (K)

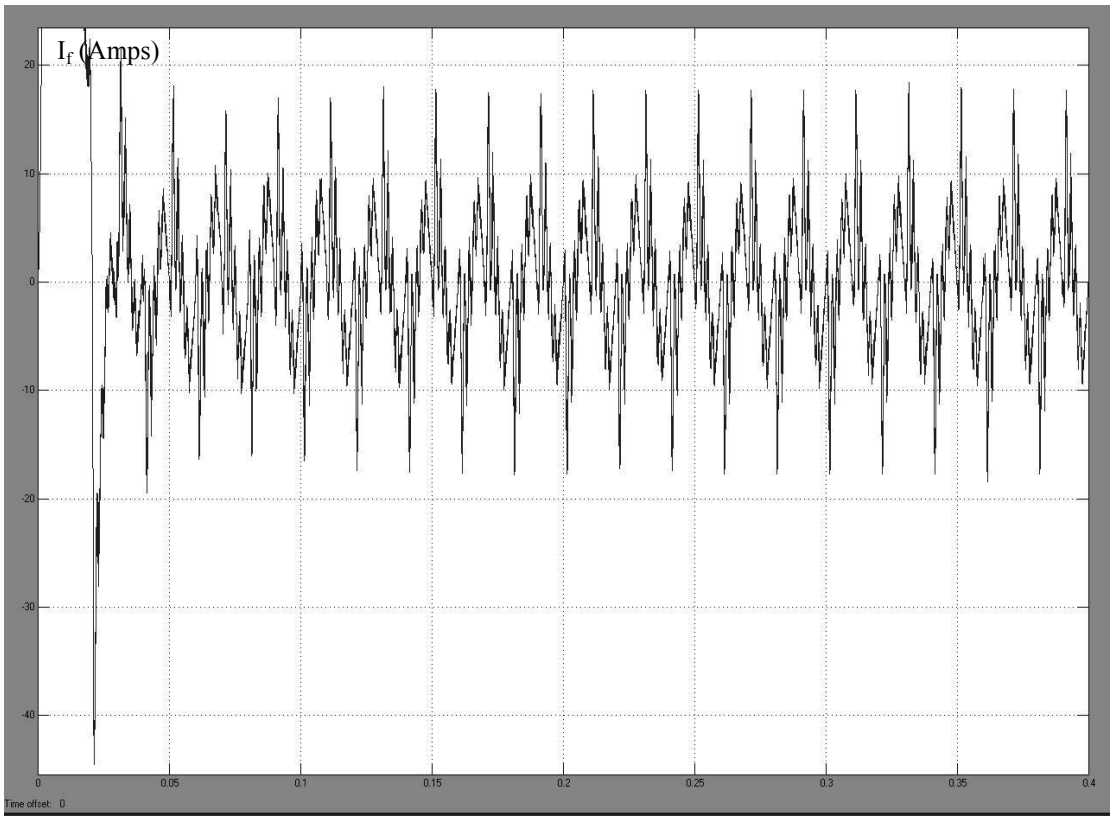


Spectrum of If, IL and Is up to 1kHz

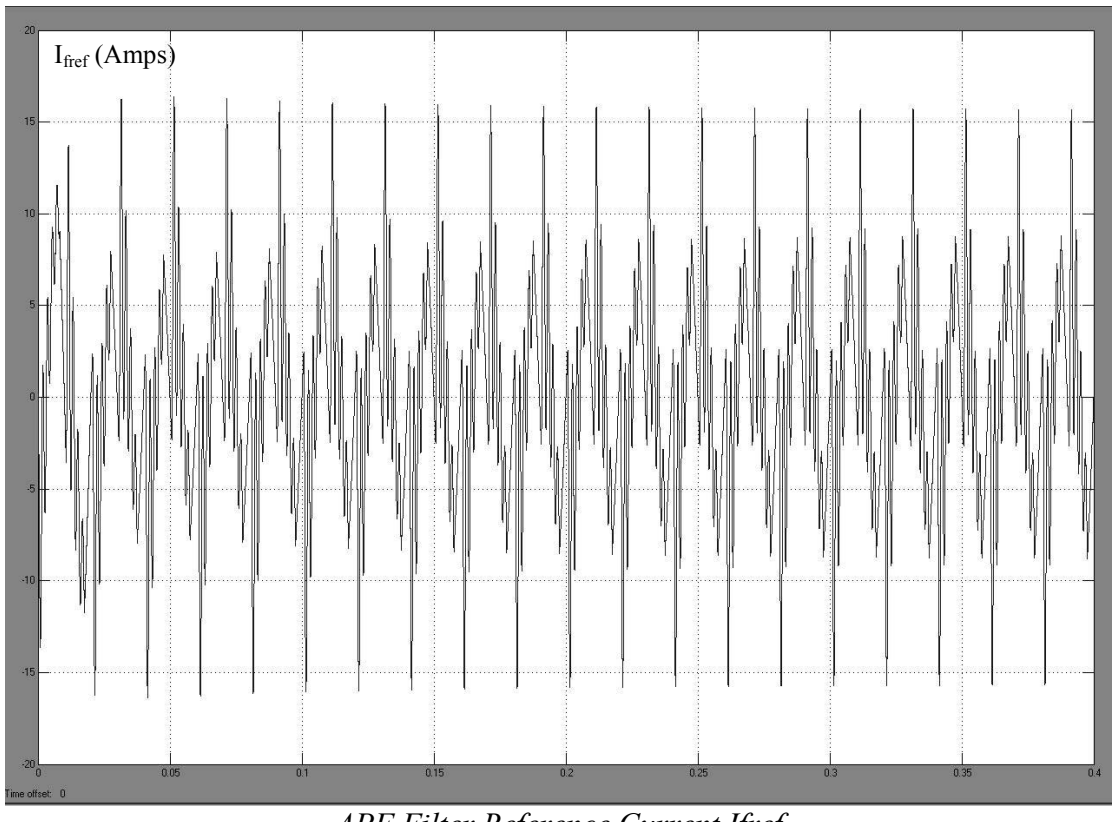
Table of RMS current Harmonics:

Table of Harmonics for Result Set 2a							
If RMS	IL RMS	Is RMS	Freq(Hz)	If RMS	IL RMS	Is RMS	Freq(Hz)
3.4362	9.1371	8.6344	50	0.070701	0.1326	0.14374	1050
0.00010739	3.65E-09	0.0001074	100	9.18E-05	1.45E-09	9.18E-05	1100
1.5201	1.9032	0.38822	150	0.079117	0.05946	0.0295	1150
0.00012325	1.24E-09	0.00012325	200	9.11E-05	4.23E-09	9.11E-05	1200
1.4827	1.4912	0.084934	250	0.11122	0.034523	0.091555	1250
0.00010861	2.26E-09	0.0001086	300	8.40E-05	2.71E-09	8.40E-05	1300
1.2815	1.2594	0.089277	350	0.099038	0.057862	0.057565	1350
0.00010822	5.02E-09	0.00010822	400	7.33E-05	7.49E-10	7.33E-05	1400
1.101	1.3525	0.34252	450	0.089182	0.037198	0.10147	1450
9.75E-05	1.11E-08	9.75E-05	500	6.89E-05	3.01E-09	6.89E-05	1500
2.2939	2.8329	0.7023	550	0.051452	0.0079294	0.054472	1550
0.00010563	2.22E-08	0.00010563	600	5.18E-05	3.66E-09	5.18E-05	1600
0.80696	1.1837	0.40816	650	0.08723	0.028818	0.05864	1650
9.73E-05	6.25E-09	9.73E-05	700	5.12E-05	8.62E-10	5.12E-05	1700
0.49284	0.49278	0.0061897	750	0.1793	0.025754	0.1995	1750
9.89E-05	4.96E-09	9.89E-05	800	3.31E-05	2.98E-09	3.31E-05	1800
0.19285	0.15442	0.038896	850	0.10297	0.005037	0.10351	1850
9.19E-05	5.54E-09	9.19E-05	900	3.61E-05	3.03E-09	3.61E-05	1900
0.2633	0.13678	0.13462	950	0.059551	0.014591	0.07412	1950
9.82E-05	2.09E-09	9.82E-05	1000	1.97E-05	1.89E-09	1.97E-05	2000

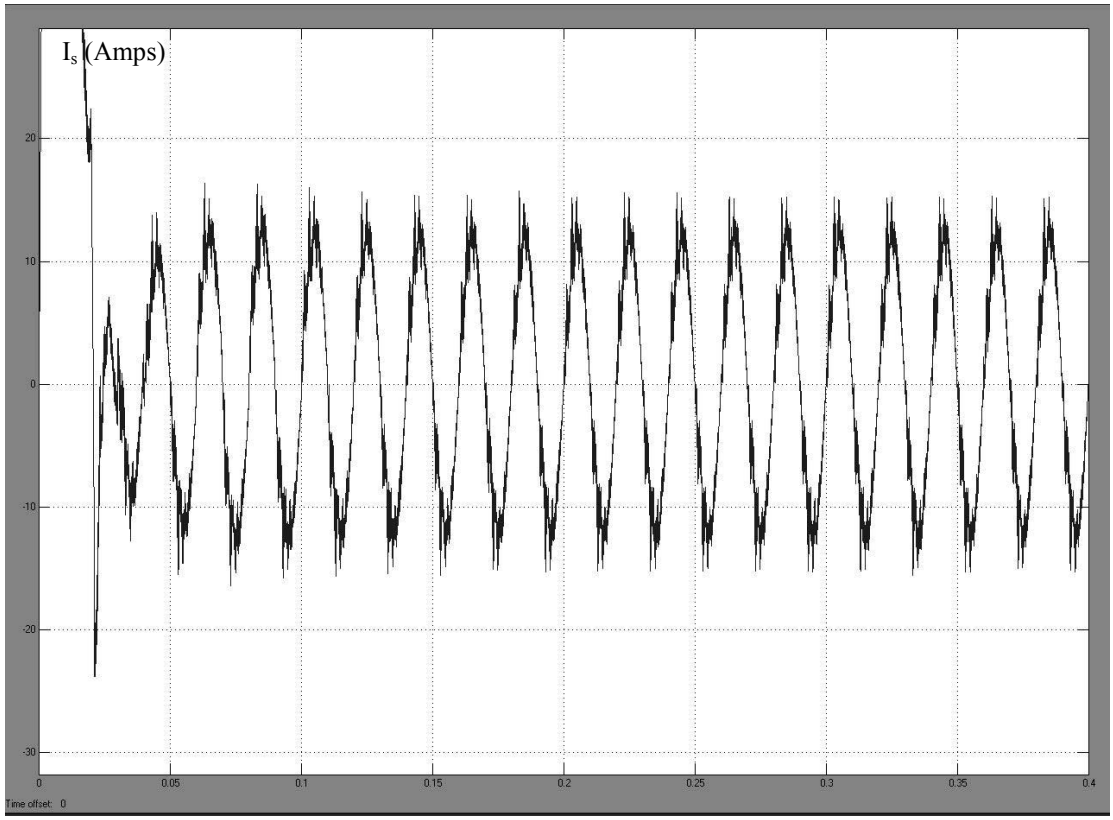
Appendix F: Result Set 2b



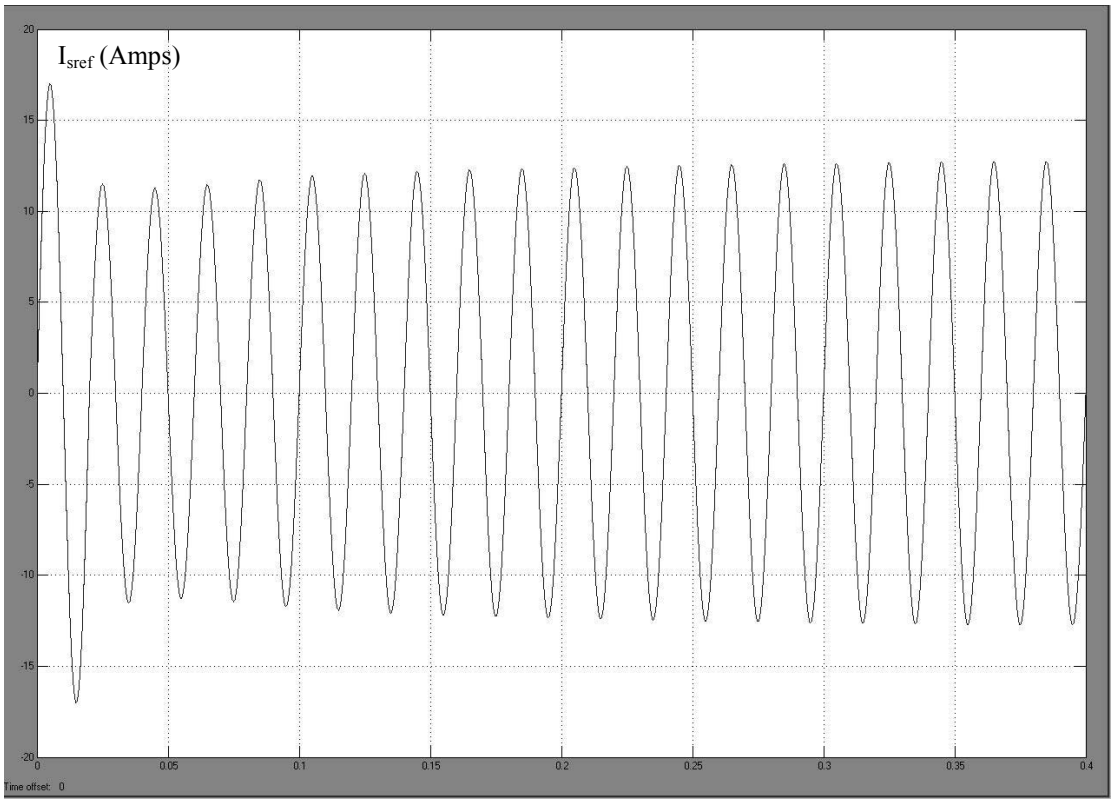
APF Filter Current If



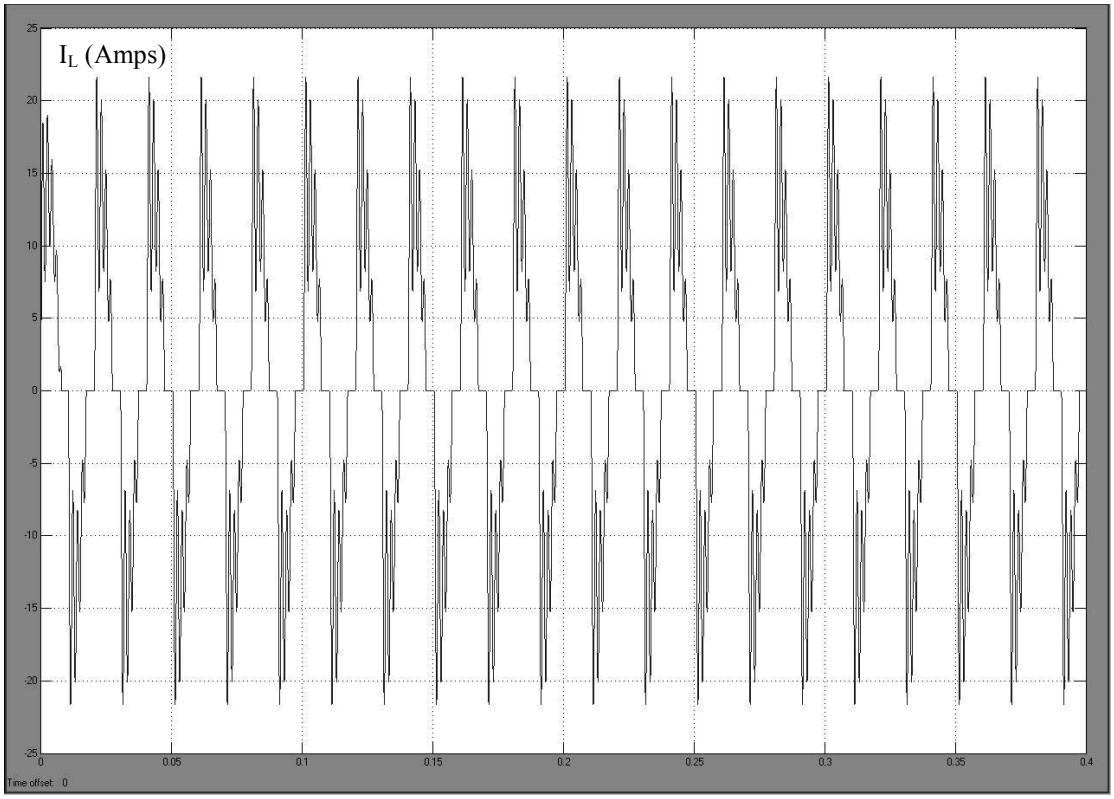
APF Filter Reference Current Ifref



Source Current Is

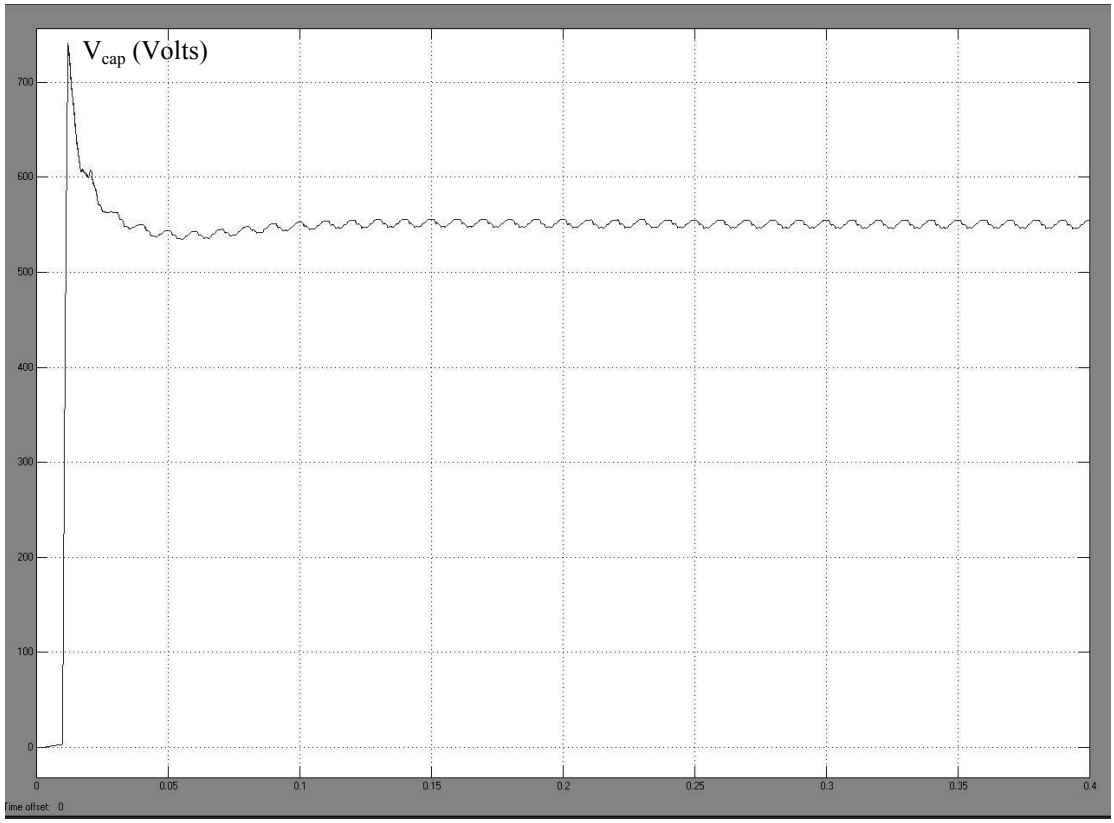


Source Reference Current Isref



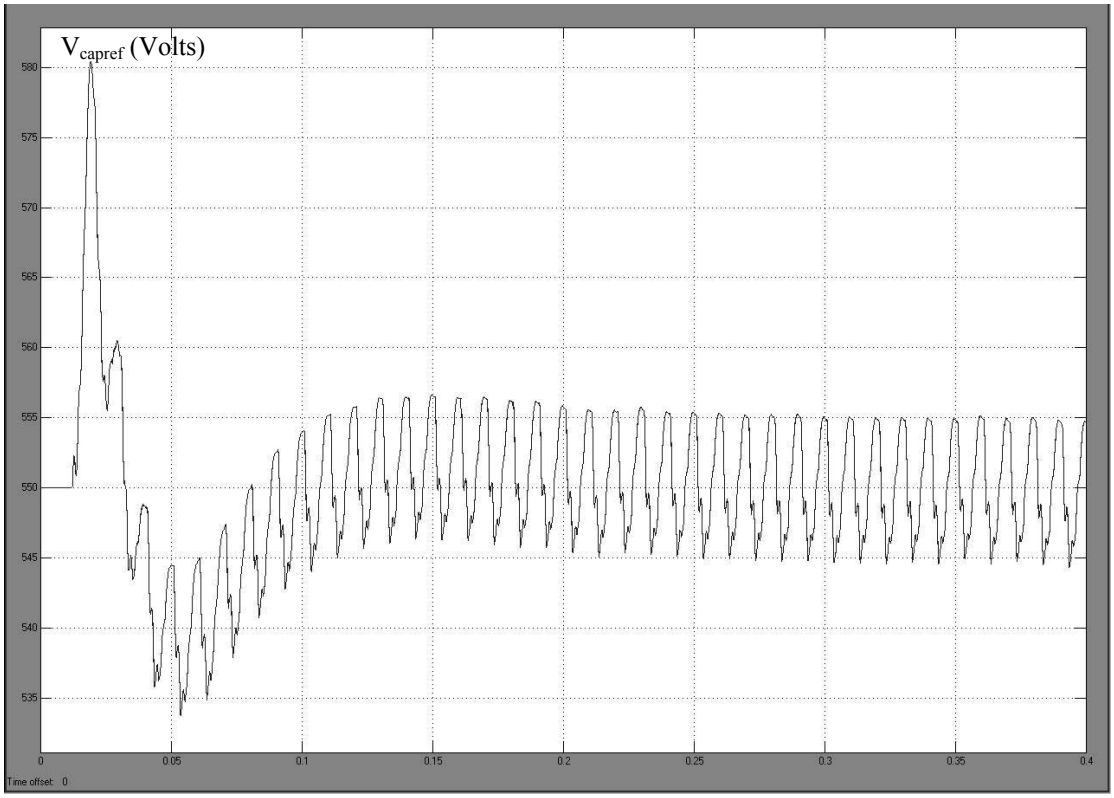
secs

Load Current IL

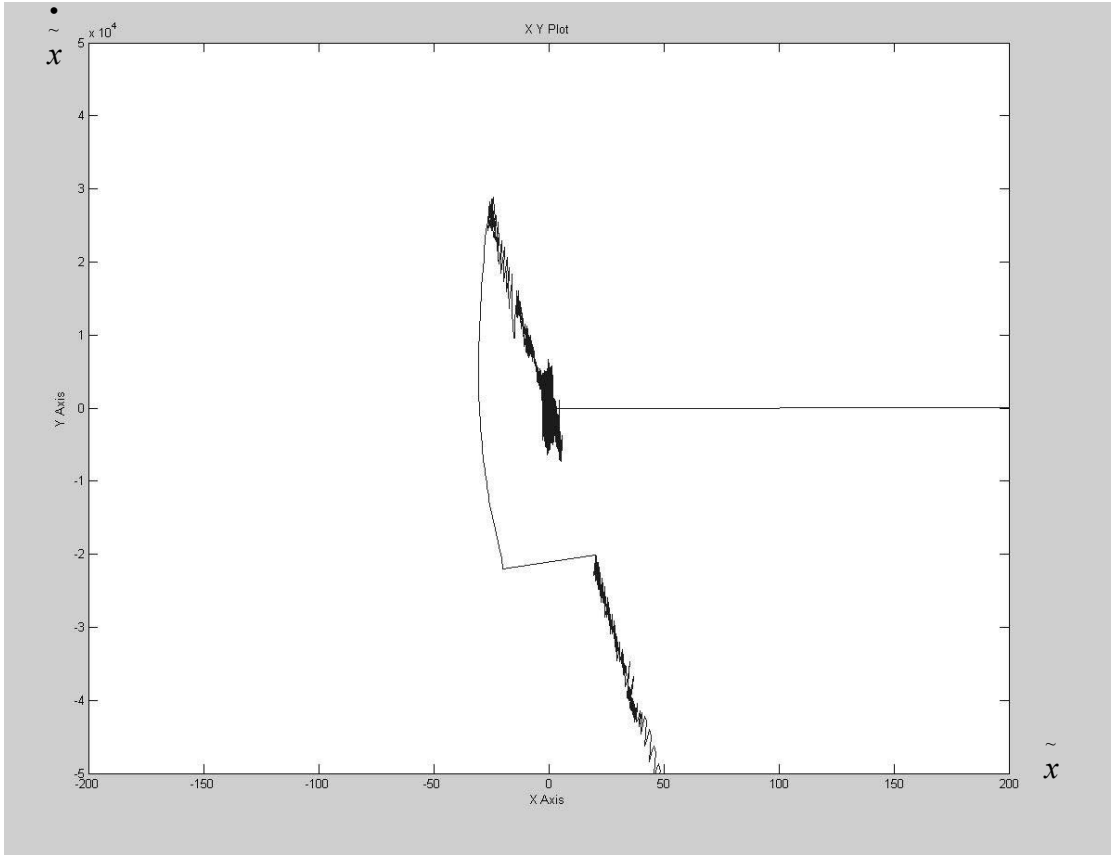


secs

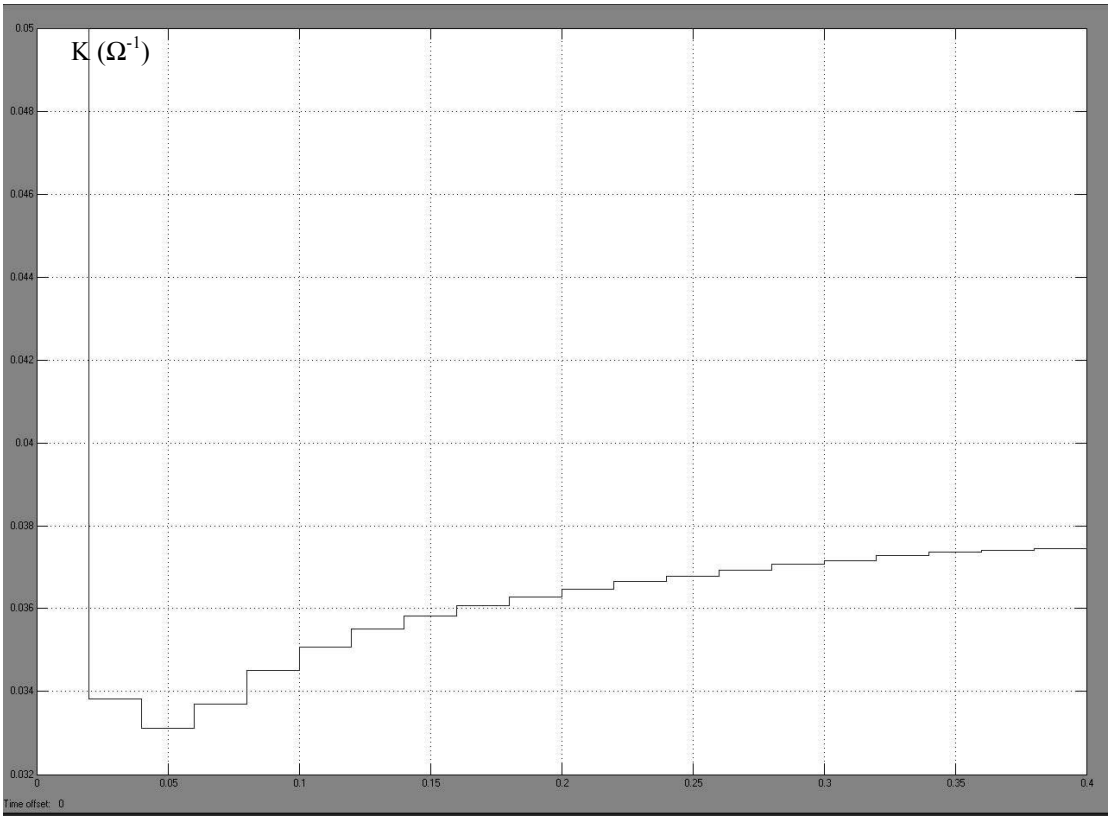
Capacitor Voltage Vcap



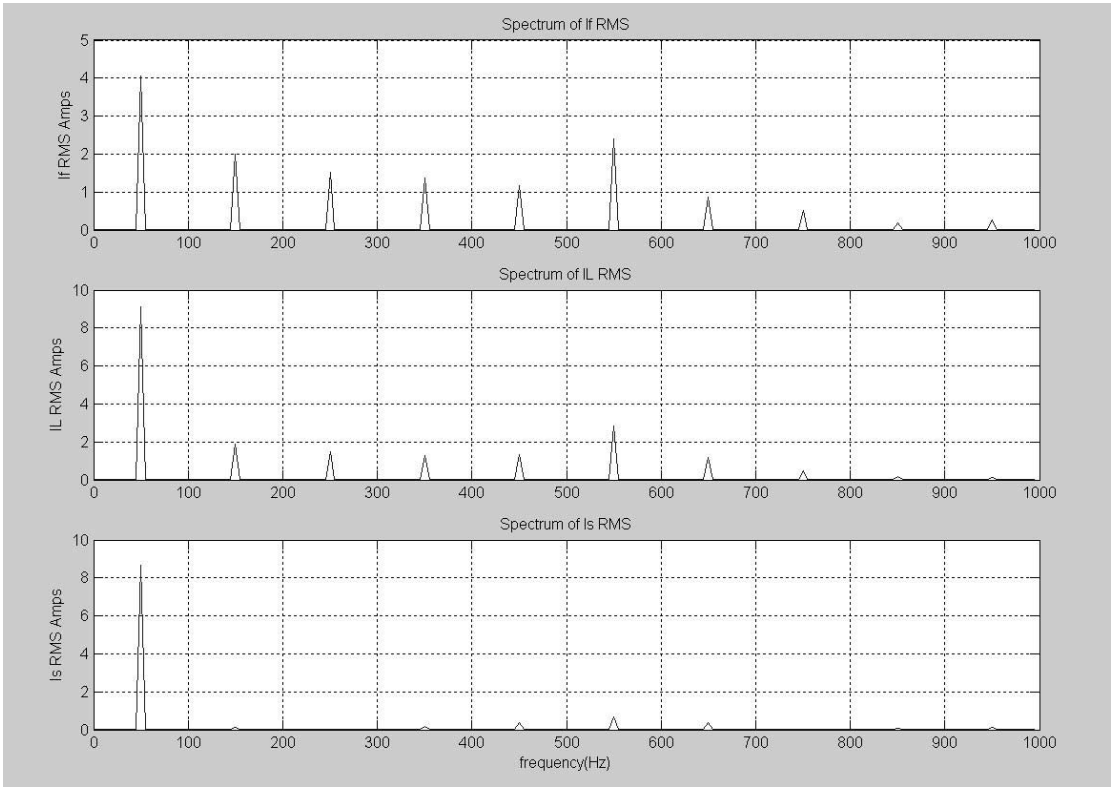
Capacitor Reference Voltage Vcapref



Sliding in State Space



Conductivity of load (K)

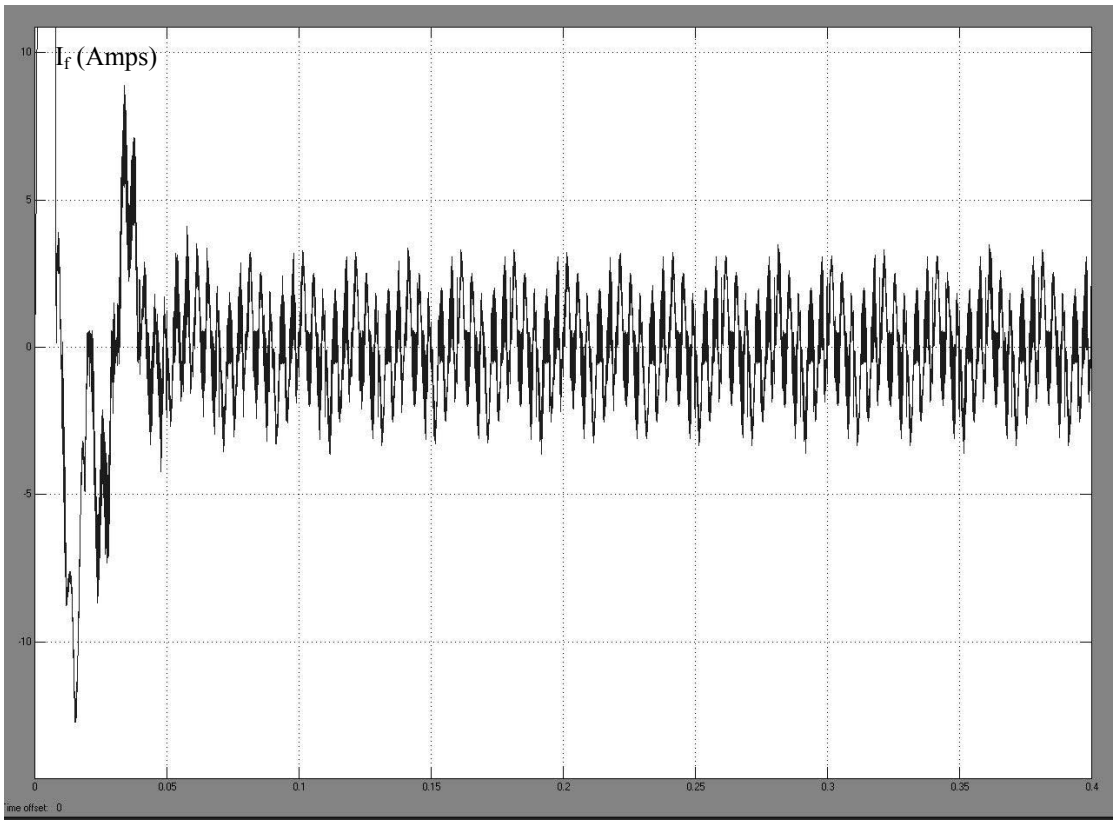


Spectrum of If, Il and Is up to 1kHz

Table of RMS current Harmonics:

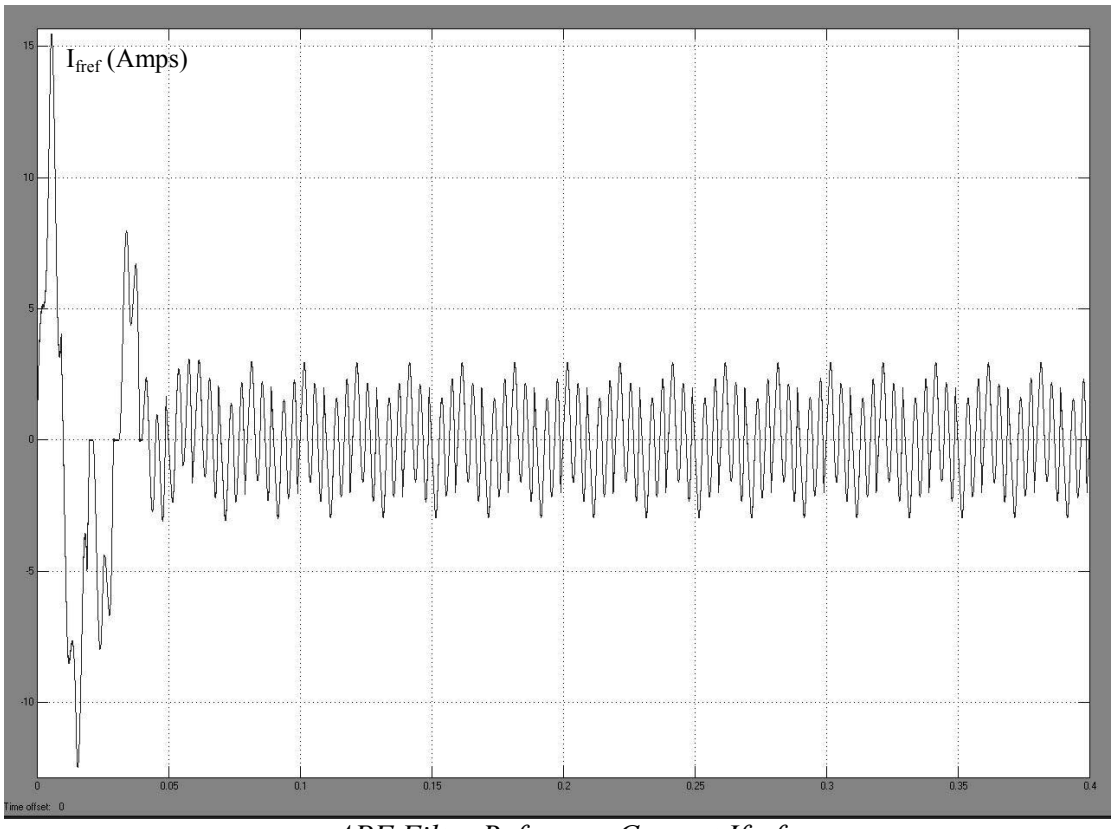
Table of Harmonics for Result Set 2b								
If RMS	IL RMS	Is RMS	Freq(Hz)		IF RMS	IL RMS	Is RMS	Freq(Hz)
4.0456	9.1371	8.6719	50		0.10632	0.1326	0.14957	1050
0.0044775	2.96E-09	0.0044775	100		9.50E-03	4.22E-09	9.50E-03	1100
1.9967	1.9032	0.1251	150		0.025891	0.05946	0.044247	1150
0.0041591	4.53E-09	0.0041591	200		9.61E-03	3.28E-09	9.61E-03	1200
1.5156	1.4912	0.03701	250		0.0829	0.034523	0.061506	1250
0.0063238	5.03E-09	0.0063238	300		5.55E-03	2.58E-09	5.55E-03	1300
1.3624	1.2594	0.18876	350		0.096064	0.057862	0.069415	1350
0.010276	9.81E-09	0.010276	400		3.72E-03	3.46E-09	3.72E-03	1400
1.1749	1.3525	0.37288	450		0.034542	0.037198	0.036883	1450
1.13E-02	1.71E-08	1.13E-02	500		1.49E-03	3.79E-09	1.49E-03	1500
2.3943	2.8329	0.67572	550		0.023325	0.0079295	0.01836	1550
0.0071312	2.37E-08	0.0071313	600		1.05E-02	3.31E-09	1.05E-02	1600
0.8601	1.1837	0.39089	650		0.088785	0.028818	0.062141	1650
1.00E-02	1.26E-08	1.00E-02	700		7.25E-03	3.89E-09	7.25E-03	1700
0.51117	0.49278	0.048374	750		0.086262	0.025754	0.11168	1750
1.02E-02	4.64E-09	1.02E-02	800		1.10E-02	3.09E-09	1.10E-02	1800
0.19784	0.15442	0.067985	850		0.079699	0.005037	0.074716	1850
7.68E-03	1.25E-09	7.68E-03	900		1.37E-02	3.35E-09	1.37E-02	1900
0.25396	0.13678	0.13792	950		0.043477	0.014591	0.037963	1950
5.03E-03	3.61E-09	5.03E-03	1000		3.43E-03	3.46E-09	3.43E-03	2000

Appendix F: Result Set 3a



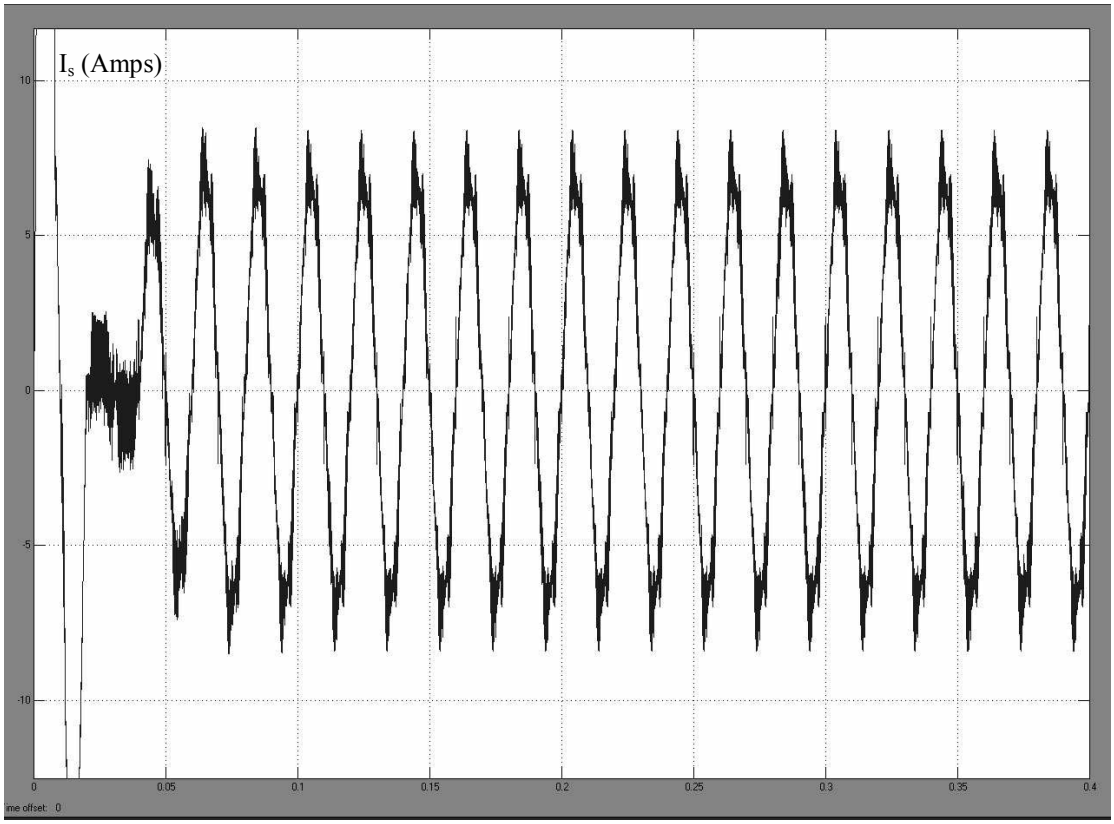
secs

APF Filter Current If

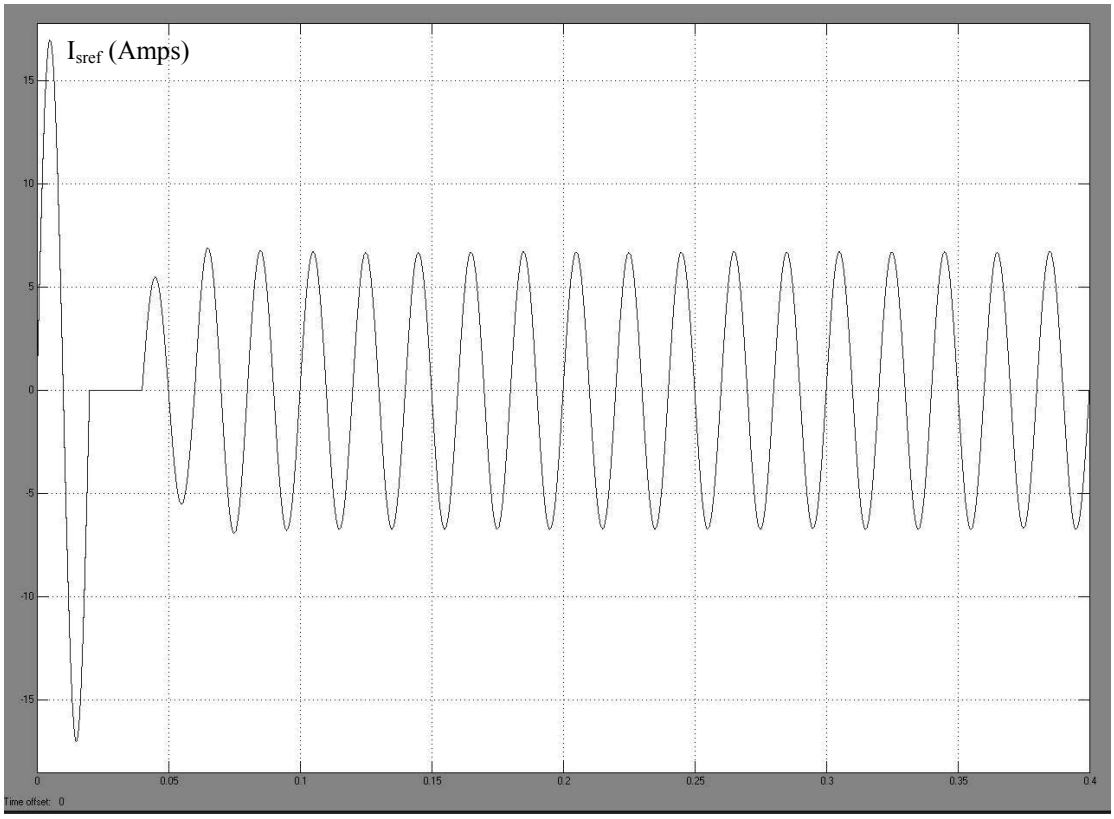


secs

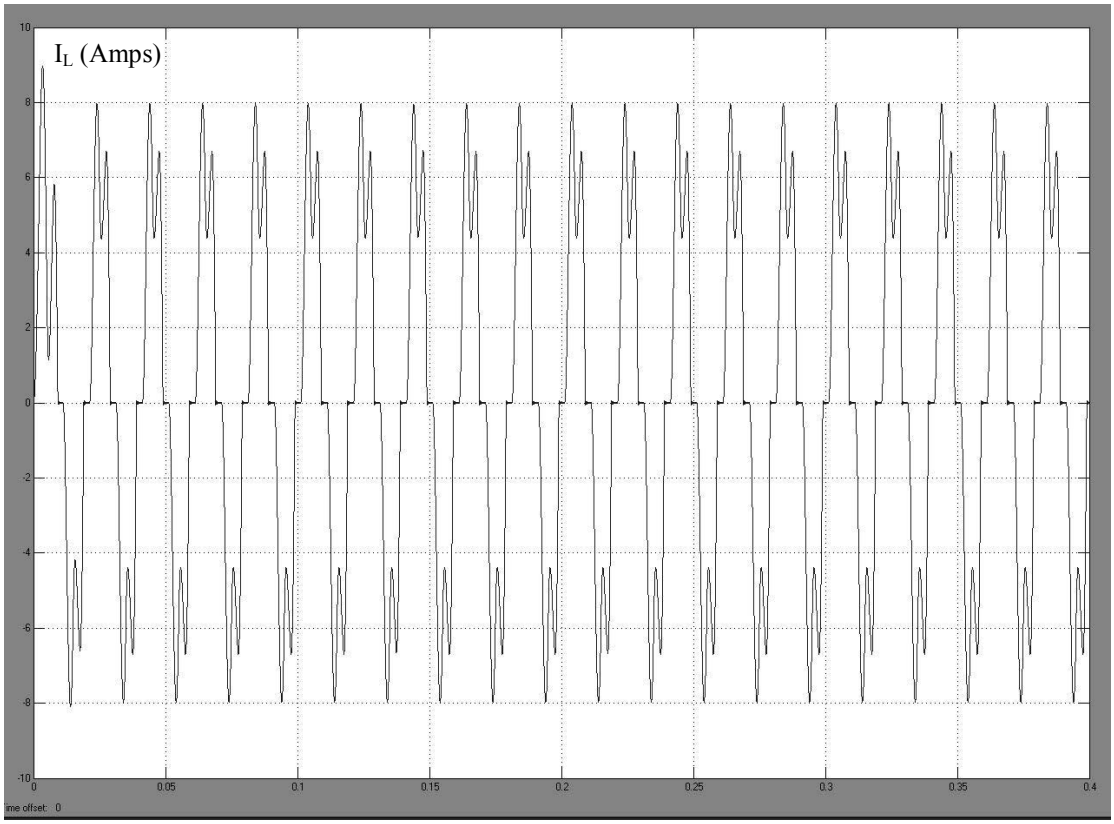
APF Filter Reference Current Ifref



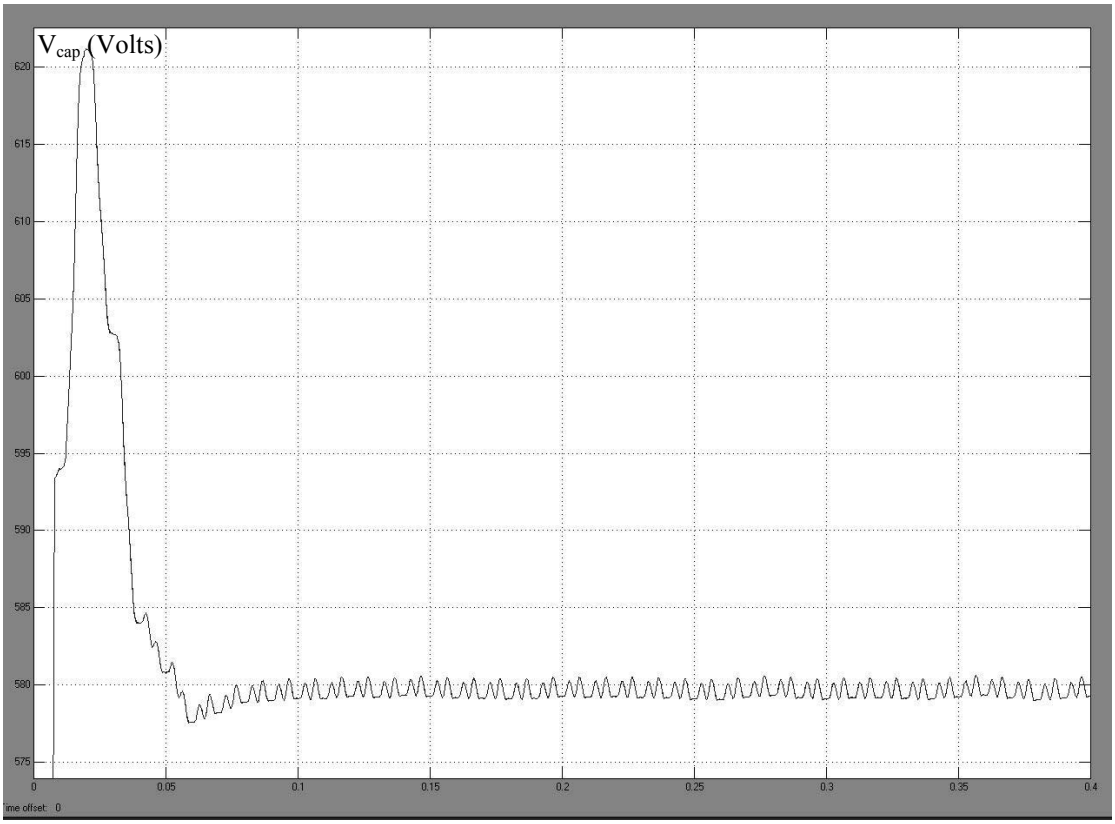
Source Current Is



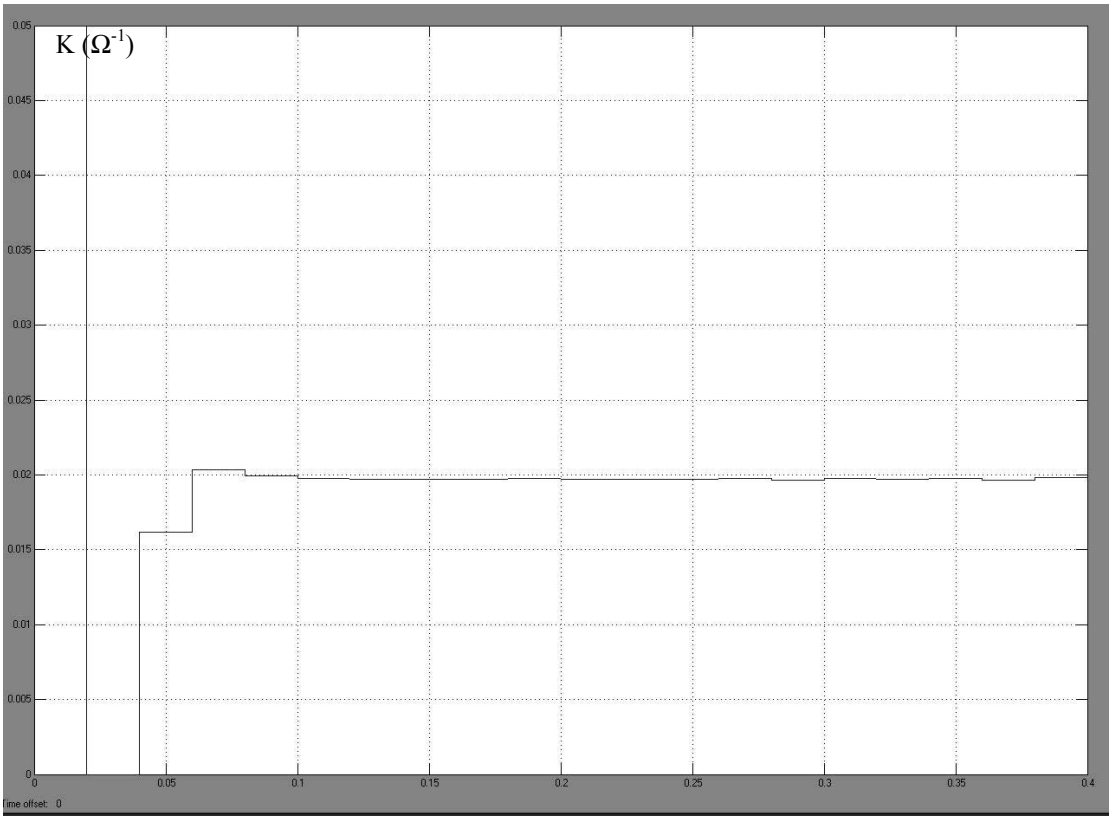
Source Reference Current Isref



Load Current IL

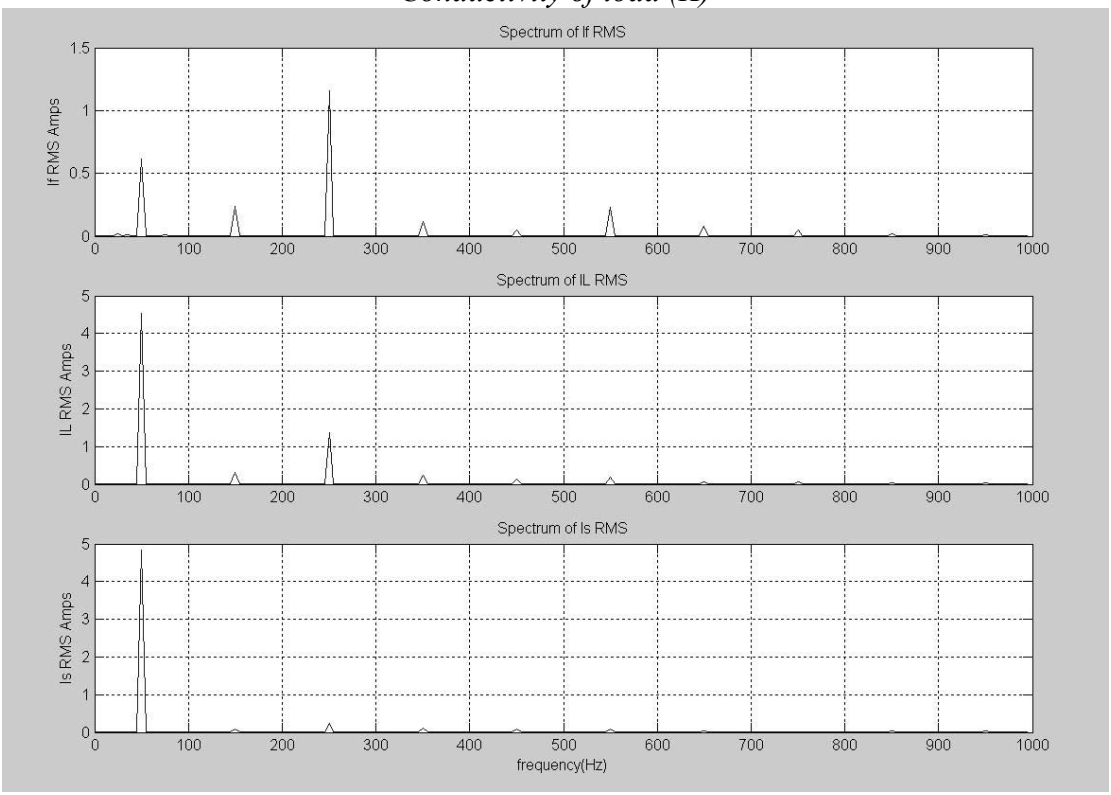


Capacitor Voltage Vcap



secs

Conductivity of load (K)

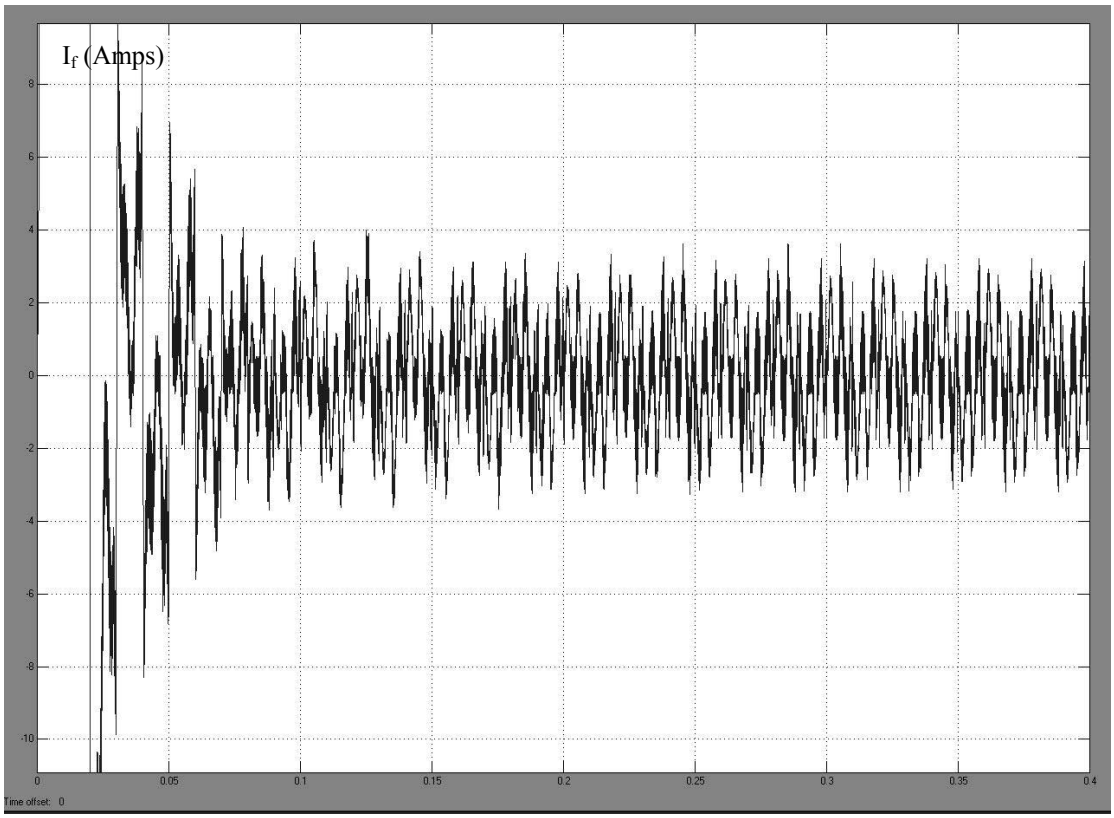


Spectrum of If, IL and Is up to 1kHz

Table of RMS current Harmonics:

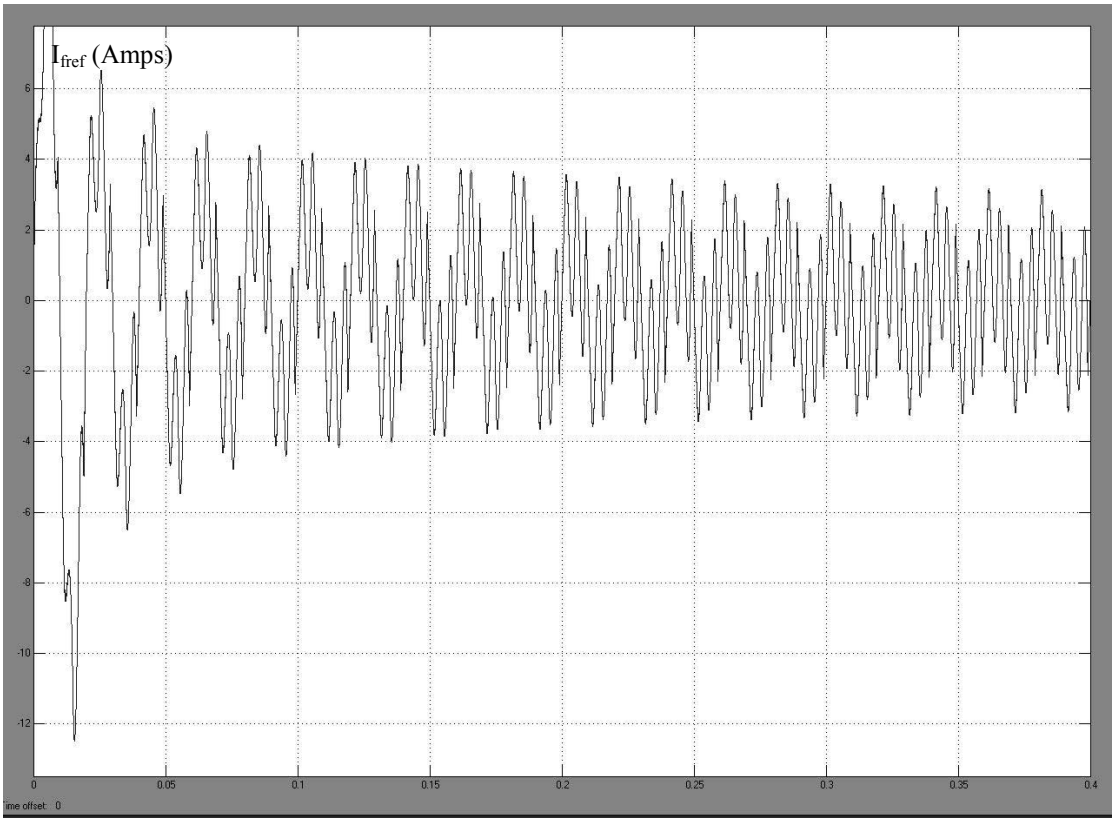
Table of Harmonics for Result Set 3a							
If RMS	IL RMS	Is RMS	Freq(Hz)	If RMS	IL RMS	Is RMS	Freq(Hz)
0.61401	4.5361	4.8457	50	0.04336	0.038411	0.010792	1050
0.0032675	1.71E-03	0.0031277	100	3.91E-03	2.65E-04	3.96E-03	1100
0.23681	0.31694	0.080583	150	0.019103	0.020062	0.0068181	1150
0.0022209	1.15E-03	0.0033263	200	4.60E-03	2.36E-04	4.82E-03	1200
1.1557	1.3775	0.23618	250	0.025669	0.019347	0.010718	1250
0.0017285	1.15E-03	0.00086867	300	1.02E-03	1.98E-04	8.29E-04	1300
0.11731	0.23866	0.12333	350	0.025008	0.016669	0.040347	1350
0.0018713	9.40E-04	0.0010151	400	5.39E-04	1.68E-04	6.78E-04	1400
0.04545	0.13244	0.10037	450	0.0073005	0.013423	0.0088696	1450
1.11E-03	7.01E-04	6.24E-04	500	7.47E-04	1.56E-04	8.95E-04	1500
0.22927	0.18361	0.076813	550	0.0015426	0.013972	0.015114	1550
0.0012768	4.88E-04	0.0010461	600	3.24E-03	1.60E-04	3.18E-03	1600
0.077941	0.052884	0.033345	650	0.003888	0.0094705	0.010804	1650
2.54E-03	3.44E-04	2.44E-03	700	1.05E-03	1.62E-04	1.21E-03	1700
0.051749	0.052898	0.012938	750	0.018484	0.010771	0.014166	1750
8.79E-04	2.78E-04	7.23E-04	800	3.50E-03	1.53E-04	3.35E-03	1800
0.016223	0.037756	0.037482	850	0.027947	0.0091973	0.036469	1850
1.36E-03	2.67E-04	1.44E-03	900	2.83E-03	1.38E-04	2.87E-03	1900
0.014314	0.029839	0.0374	950	0.0098699	0.0079324	0.017695	1950
1.47E-03	2.71E-04	1.23E-03	1000	8.26E-04	1.23E-04	9.48E-04	2000

Appendix F: Result Set 3b



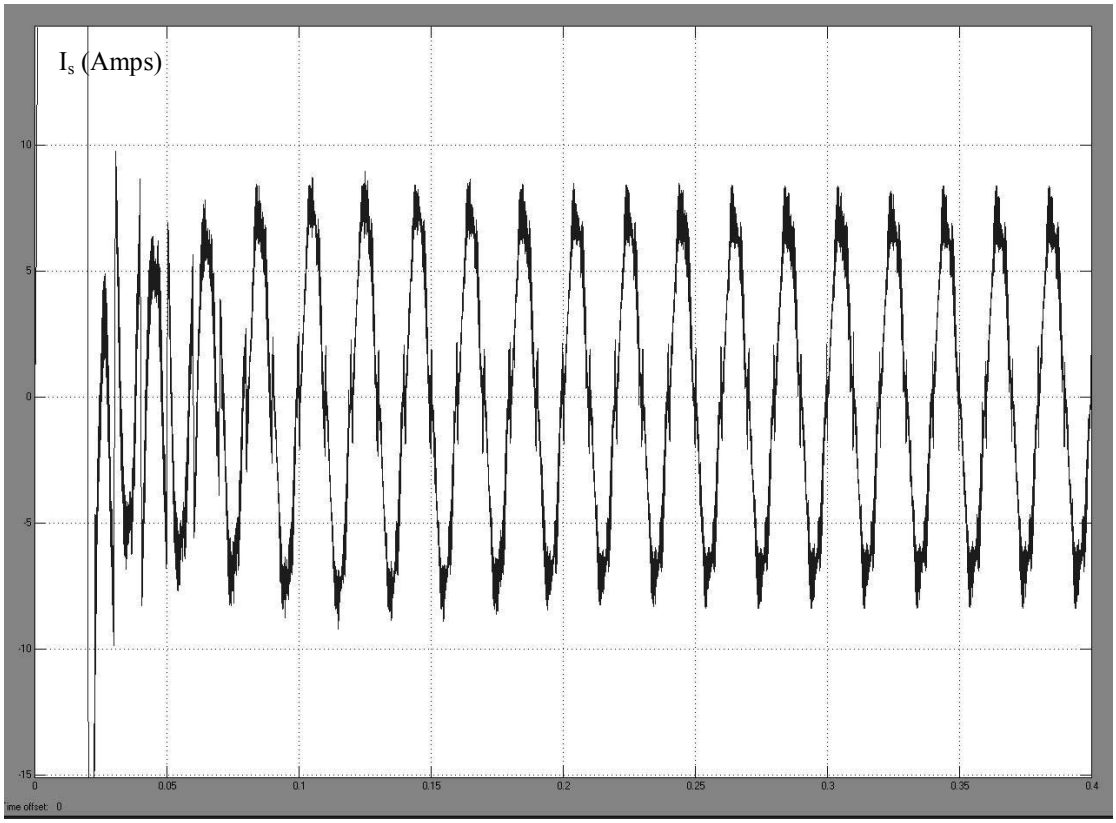
secs

APF Filter Current If

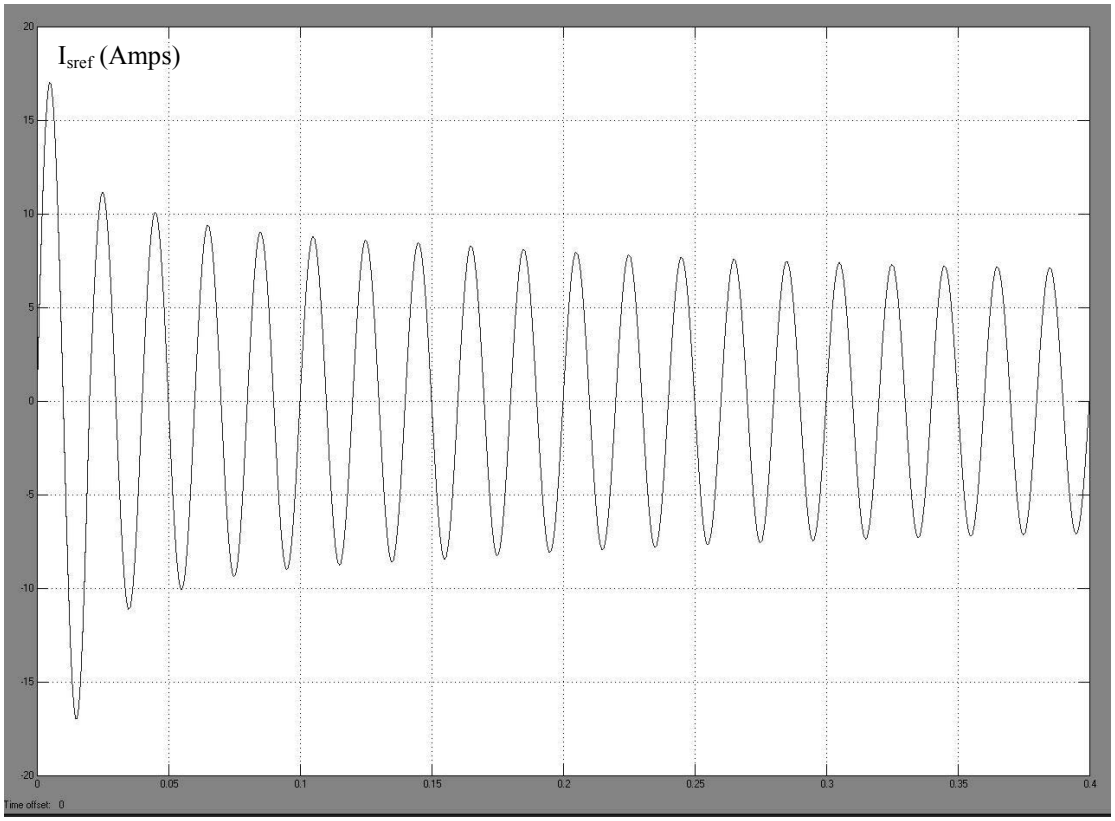


secs

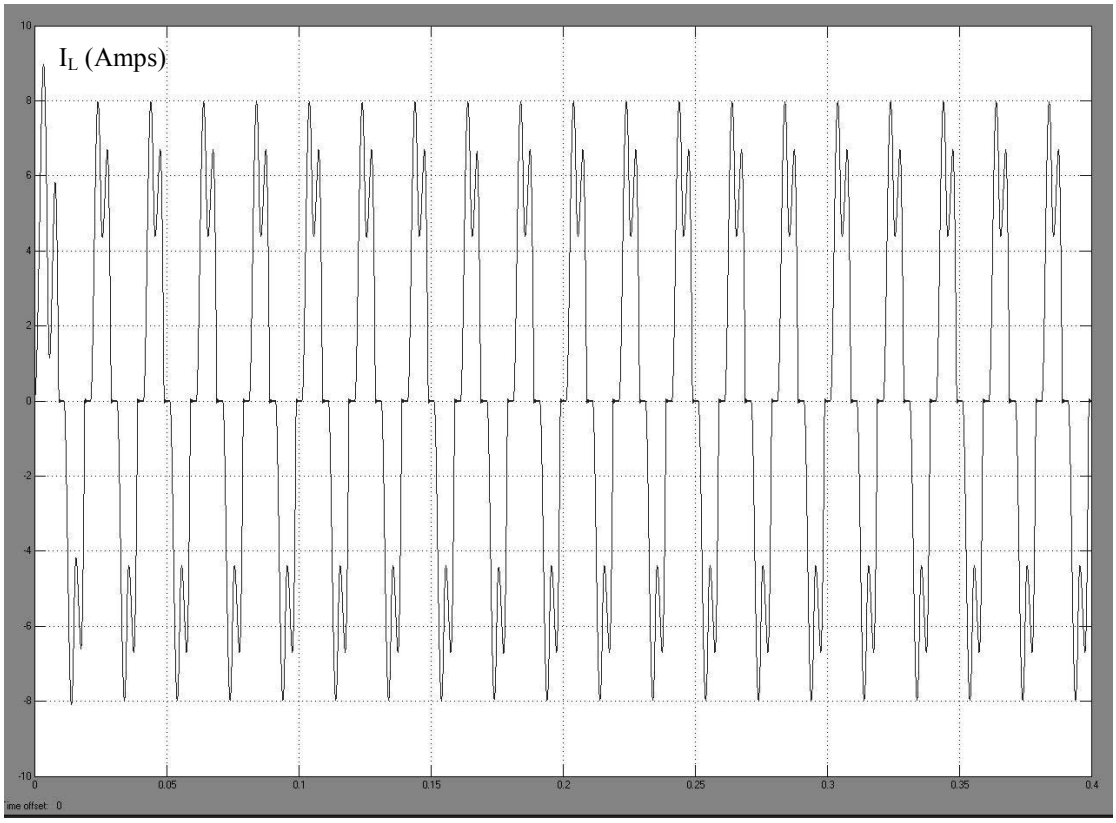
APF Filter Reference Current Ifref



Source Current Is

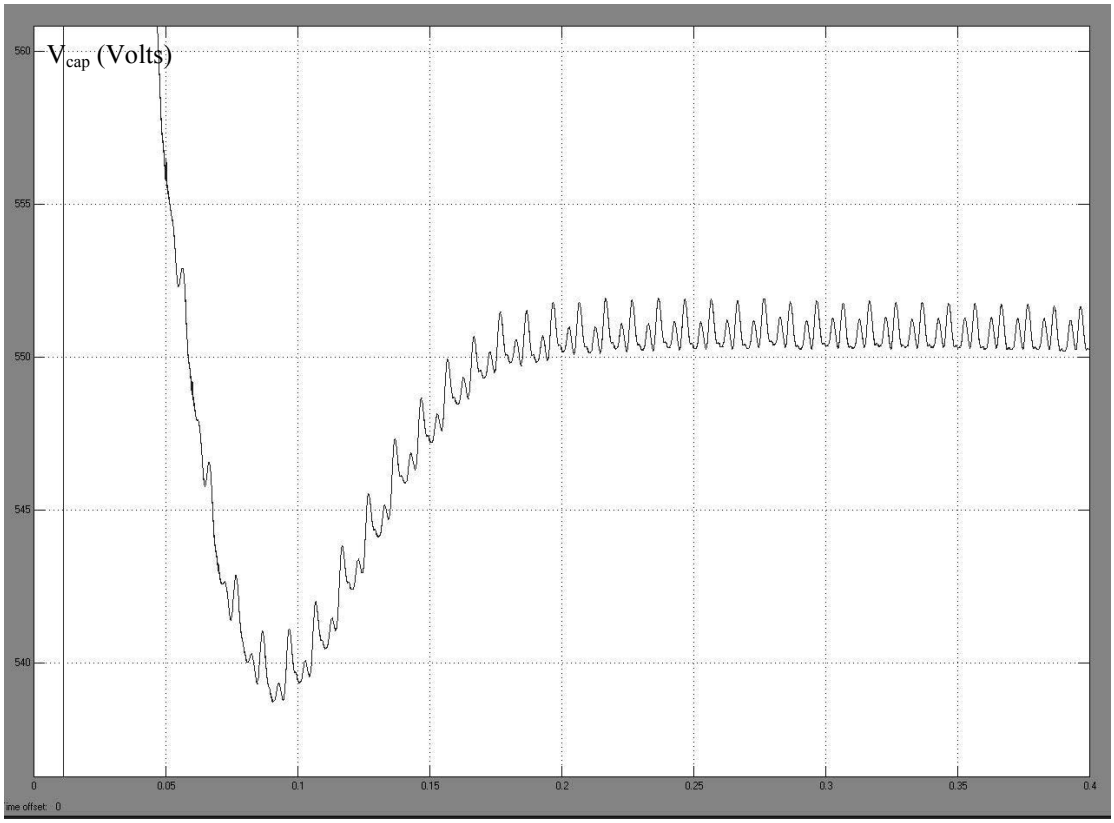


Source Reference Current Isref



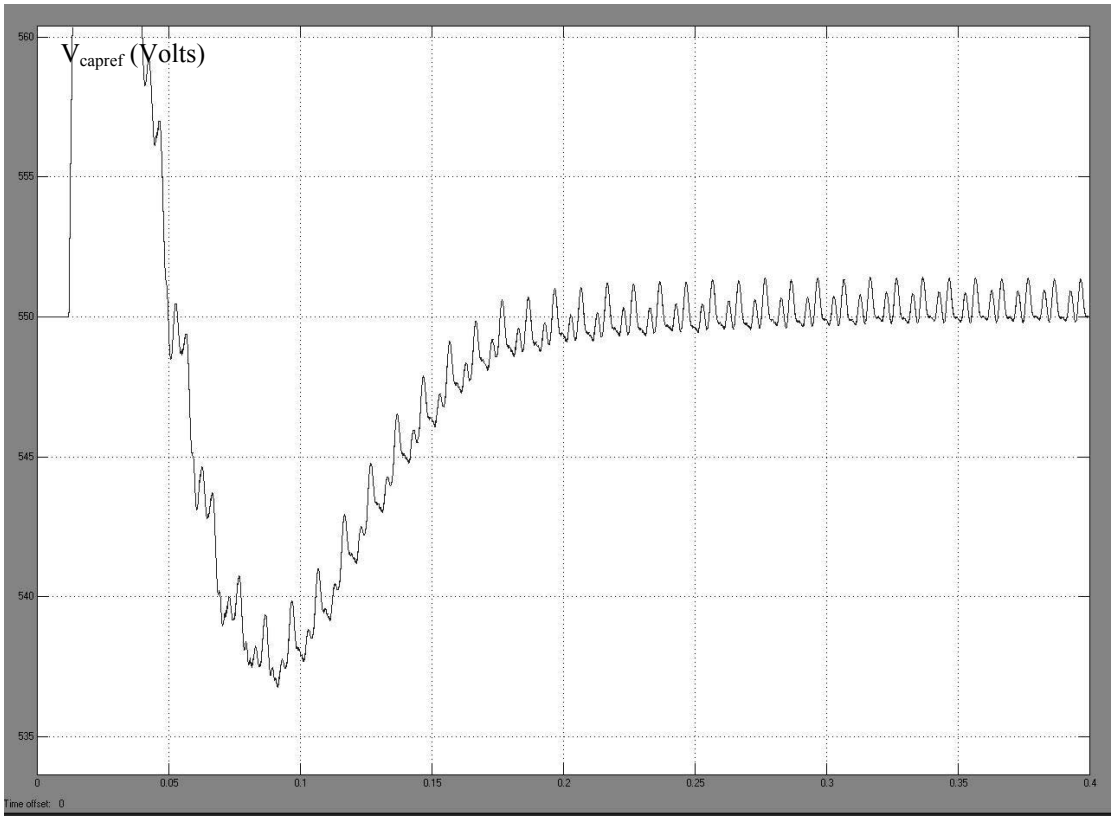
secs

Load Current IL

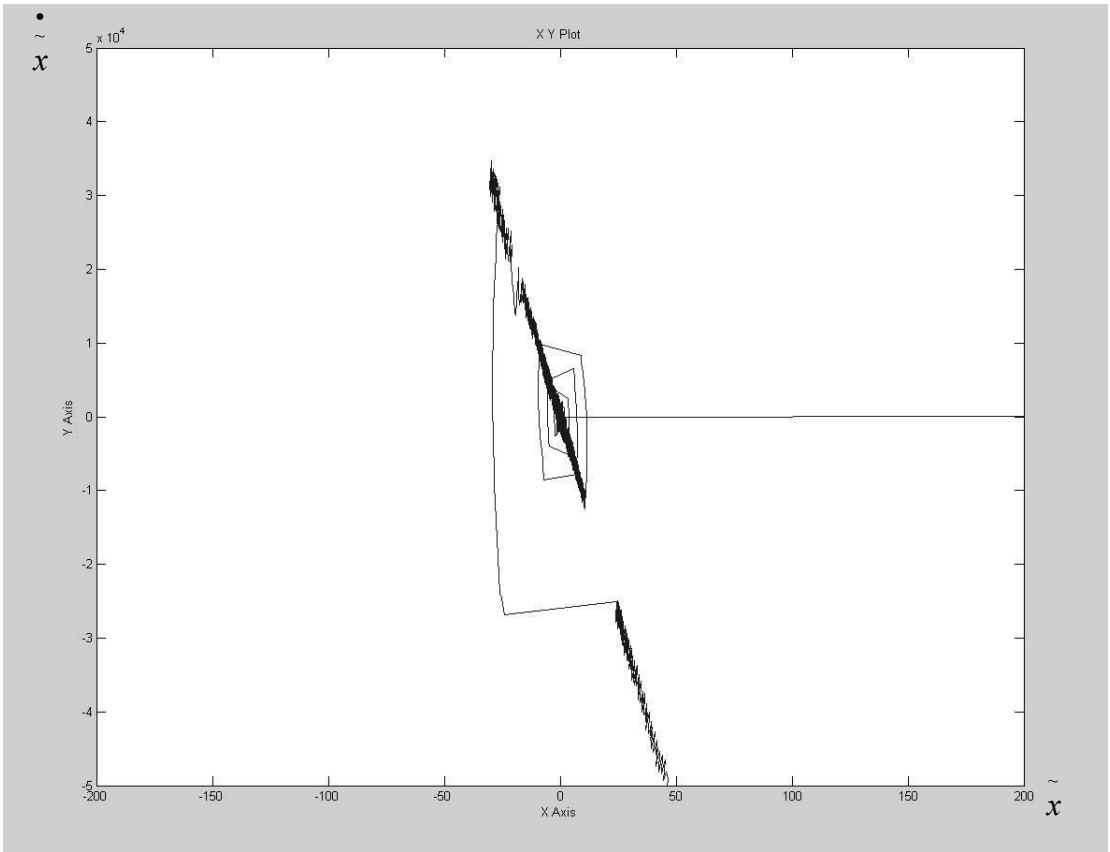


secs

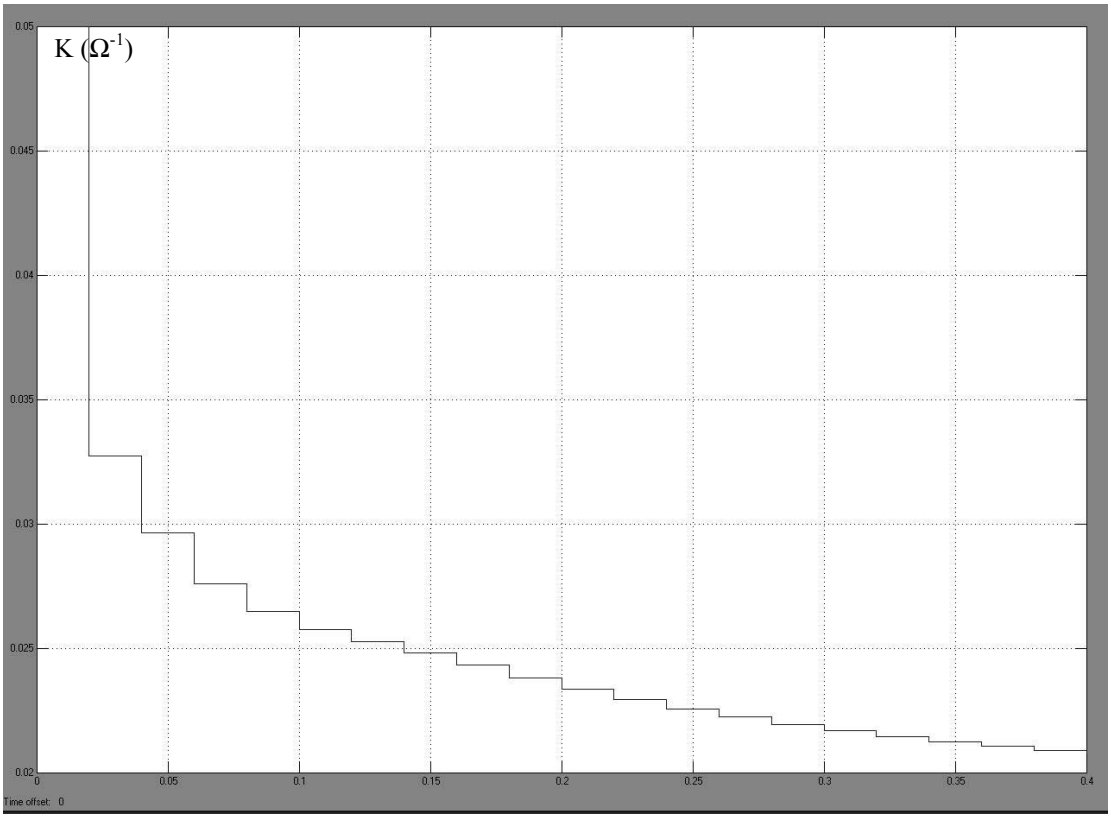
Capacitor Voltage Vcap



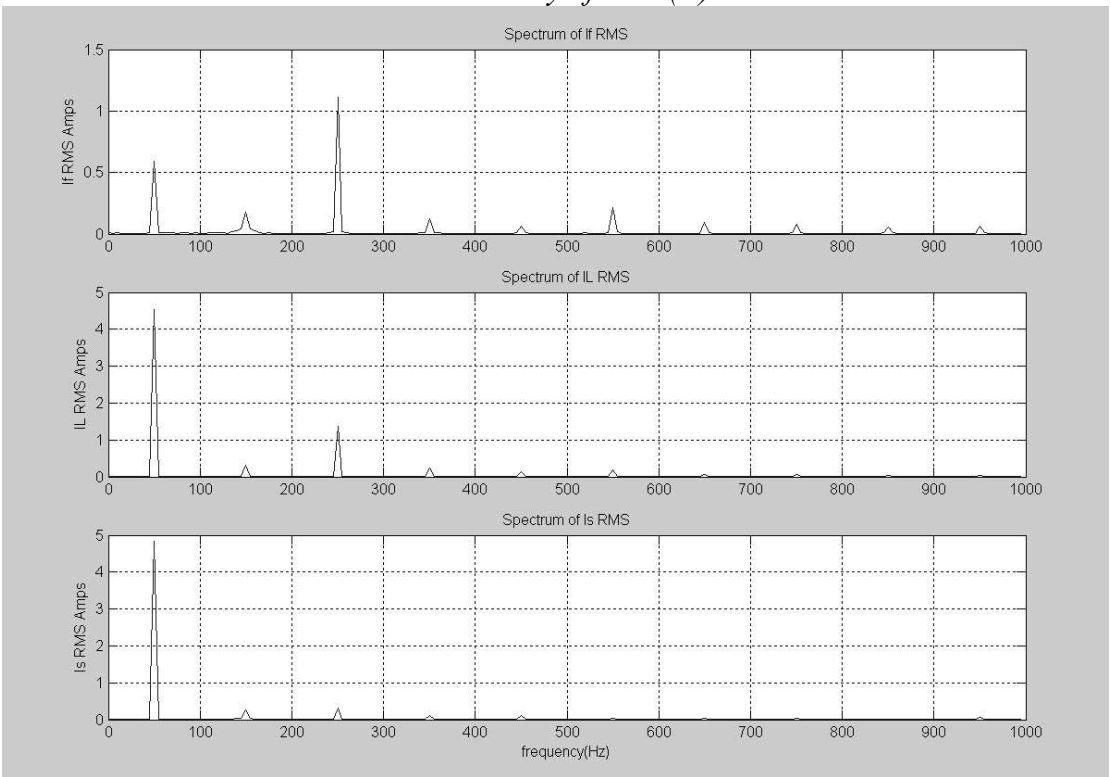
Capacitor Reference Voltage Vcapref



Sliding in State Space



Conductivity of load (K)



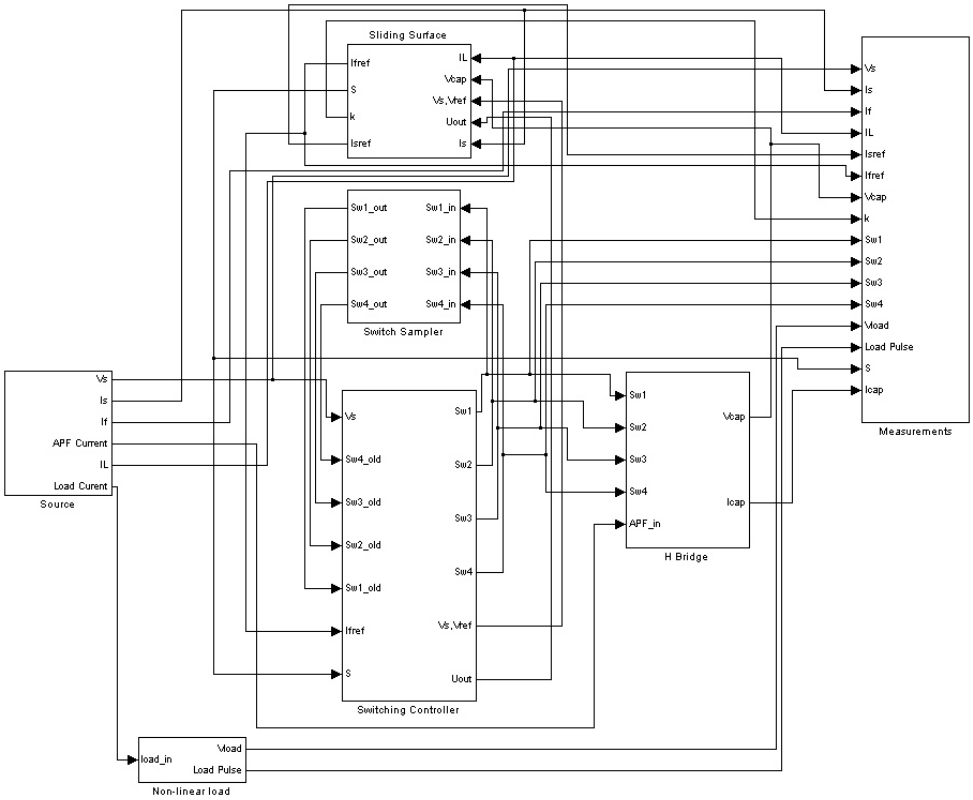
Spectrum of If, IL and Is up to 1kHz

Table of RMS current Harmonics:

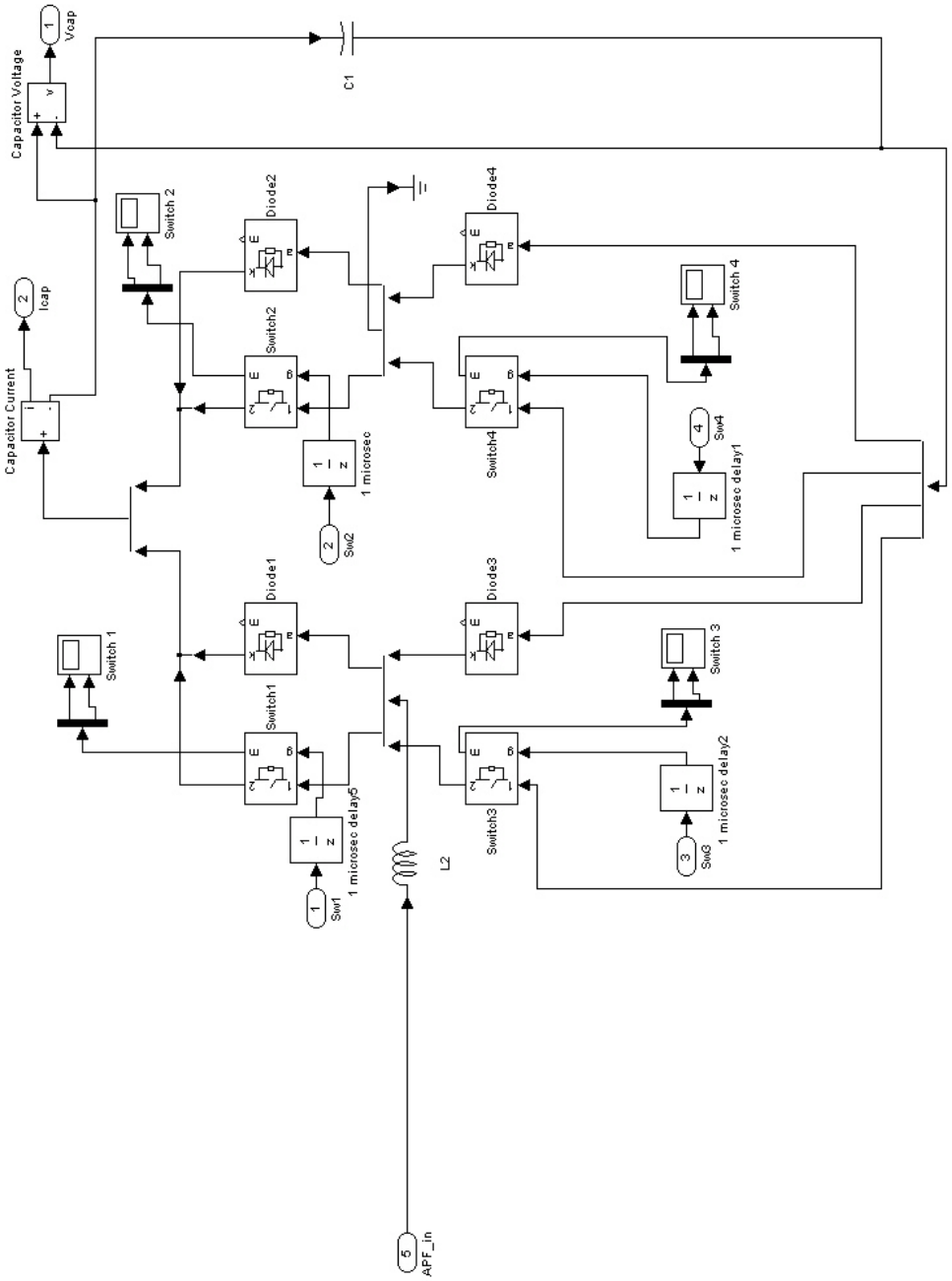
Table of Harmonics for Result Set 3b							
If RMS	IL RMS	Is RMS	Freq(Hz)	If RMS	IL RMS	IS RMS	Freq(Hz)
0.59229	4.5373	4.8308	50	0.067664	0.038417	0.044881	1050
0.0043403	3.28E-04	0.0044819	100	9.80E-04	5.11E-05	9.68E-04	1100
0.17453	0.31621	0.25172	150	0.031827	0.020104	0.042311	1150
0.0025813	2.24E-04	0.0024021	200	5.11E-03	4.55E-05	5.07E-03	1200
1.1084	1.378	0.32003	250	0.024139	0.019409	0.037967	1250
0.0051432	2.24E-04	0.0051226	300	2.75E-03	3.80E-05	2.72E-03	1300
0.12555	0.23799	0.12525	350	0.028078	0.016637	0.043475	1350
0.0043063	1.83E-04	0.0041336	400	3.69E-03	3.21E-05	3.66E-03	1400
0.063327	0.13255	0.12508	450	0.007072	0.013467	0.019584	1450
3.67E-03	1.34E-04	3.69E-03	500	7.28E-03	3.04E-05	7.26E-03	1500
0.2158	0.18364	0.034127	550	0.022785	0.013987	0.011139	1550
0.0074238	9.33E-05	0.0074739	600	2.42E-03	3.14E-05	2.40E-03	1600
0.090556	0.05293	0.044886	650	0.031723	0.0094891	0.023736	1650
2.49E-03	6.56E-05	2.46E-03	700	1.94E-03	3.17E-05	1.91E-03	1700
0.077328	0.053063	0.028308	750	0.047898	0.010798	0.037592	1750
1.97E-03	5.37E-05	2.01E-03	800	5.30E-03	2.96E-05	5.33E-03	1800
0.05499	0.037654	0.01981	850	0.023118	0.0091891	0.014031	1850
2.14E-03	5.23E-05	2.19E-03	900	6.16E-03	2.63E-05	6.19E-03	1900
0.062986	0.029873	0.050453	950	0.034102	0.0079742	0.02619	1950
3.87E-03	5.28E-05	3.88E-03	1000	5.12E-03	2.35E-05	5.12E-03	2000

Appendix G: Matlab model for APF (APF6.mdl) incorporating a PI controller

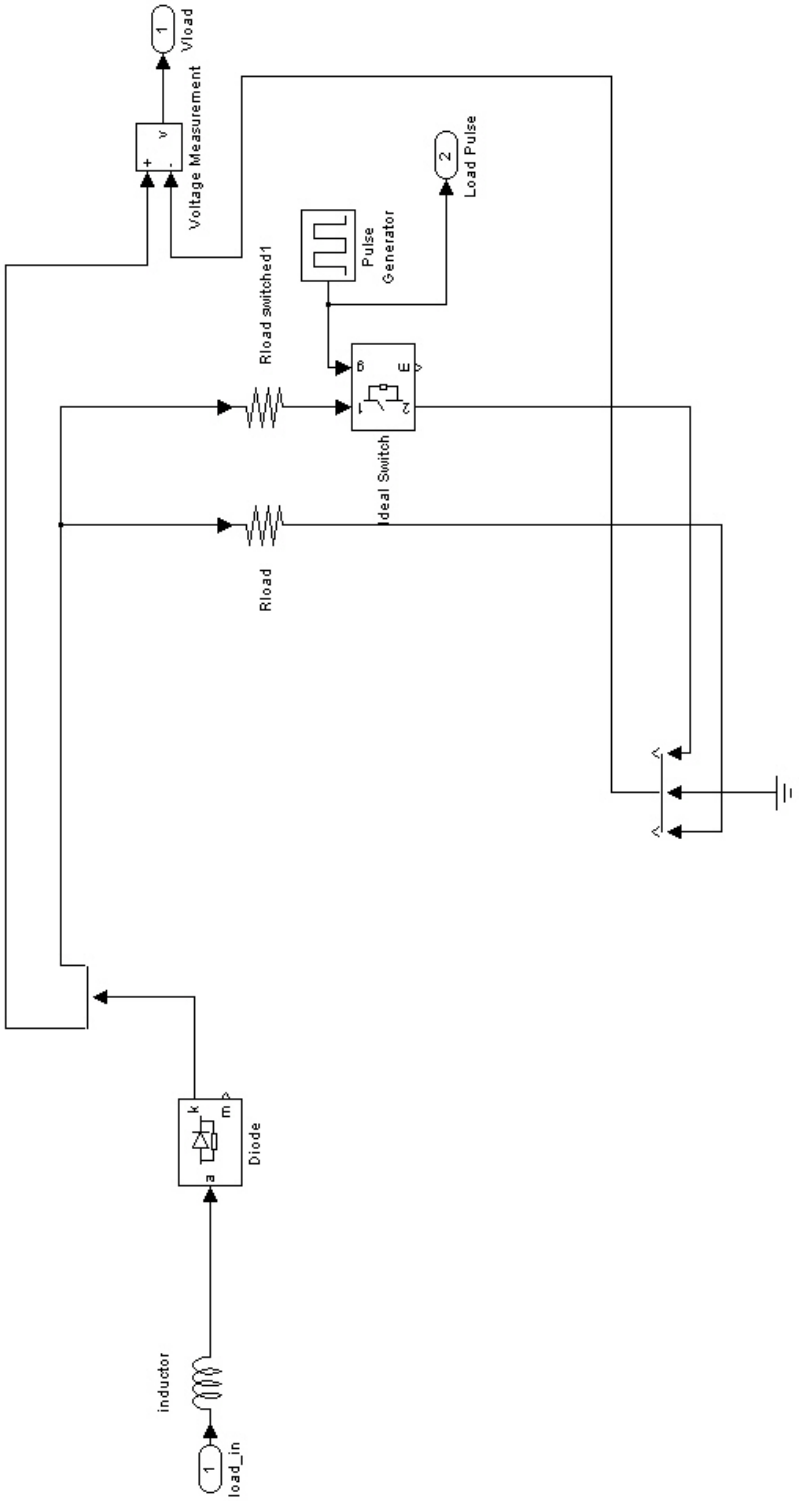
Appendix G: block Connections



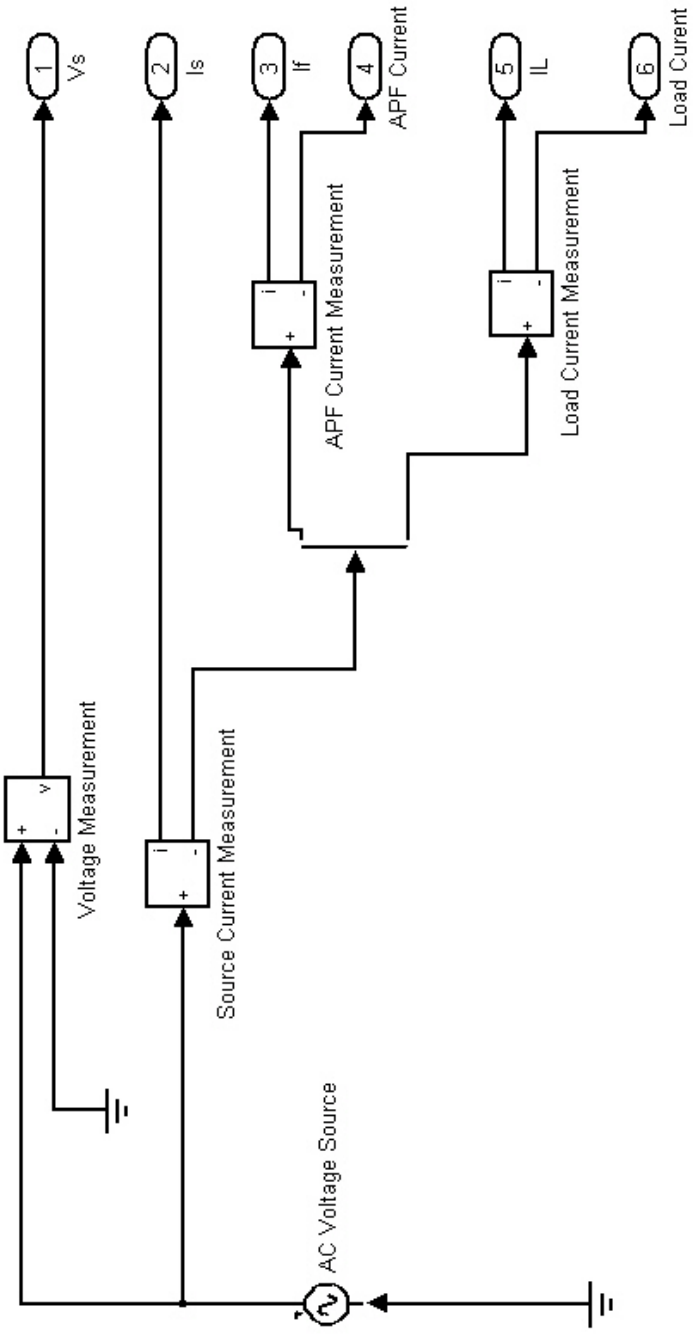
Appendix G: H-Bridge



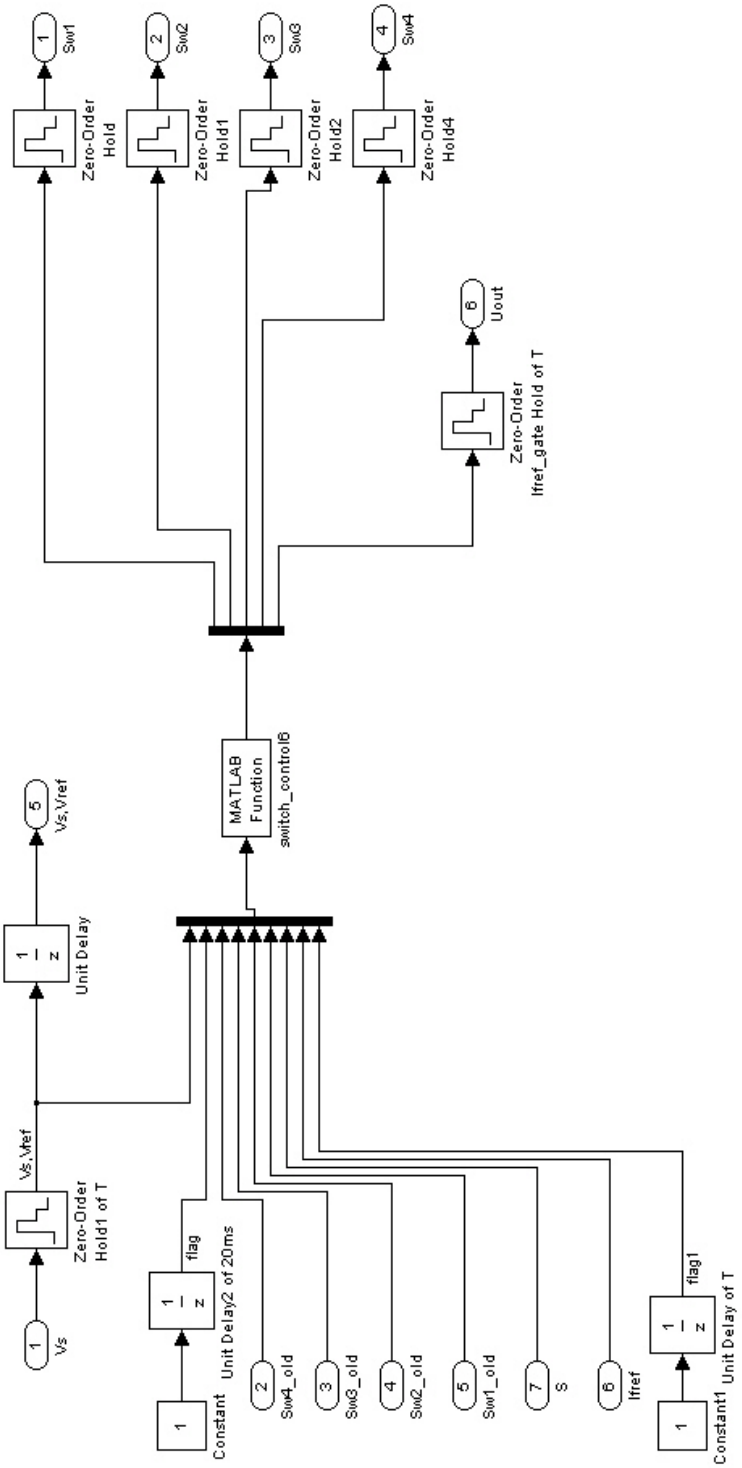
Appendix G: non-linear load



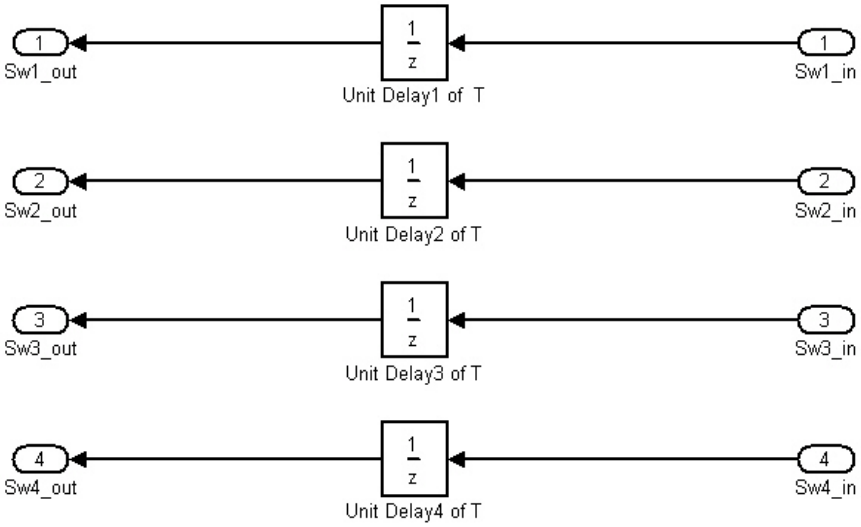
Appendix G: source



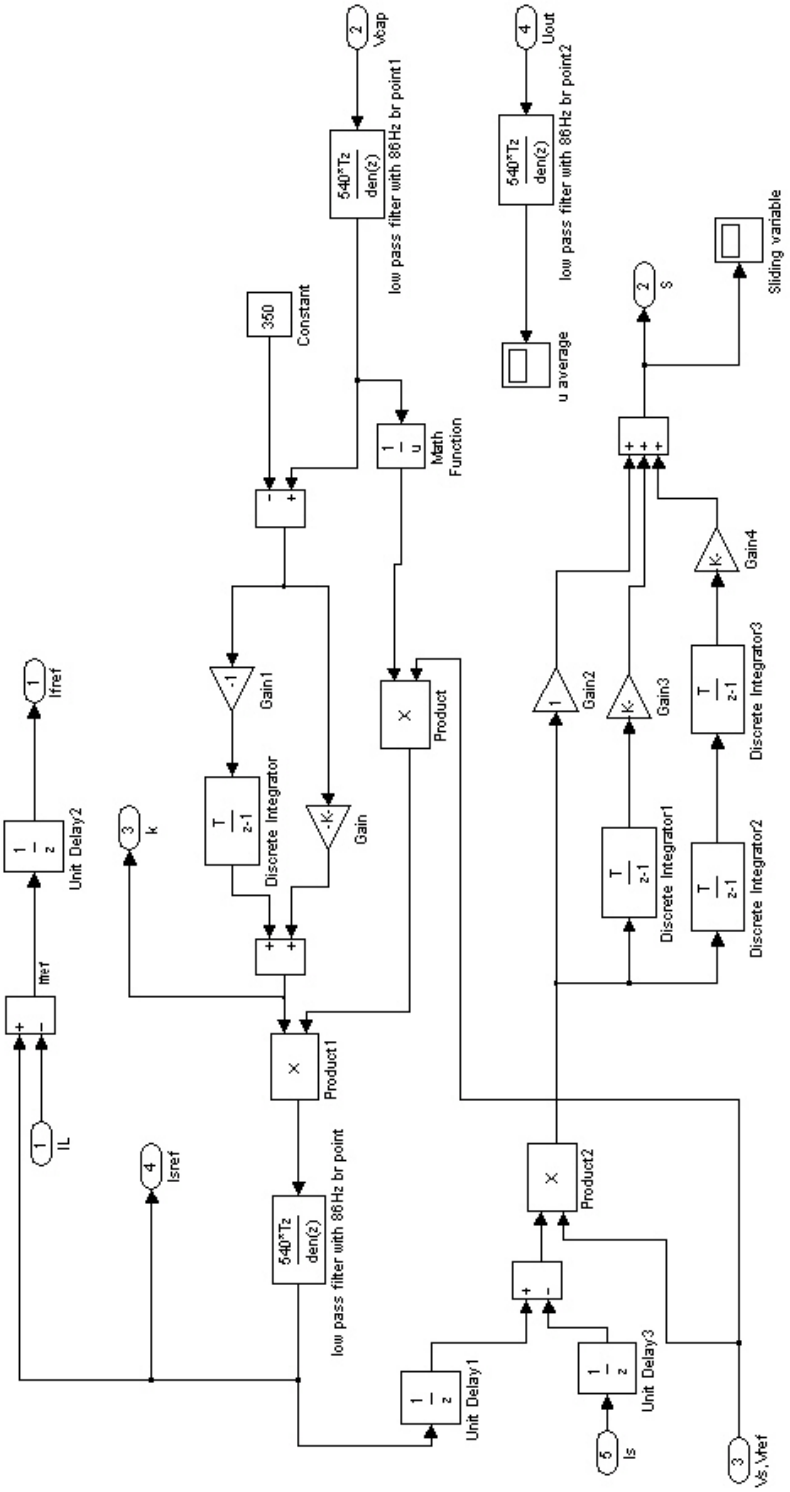
Appendix G: Switching Controller



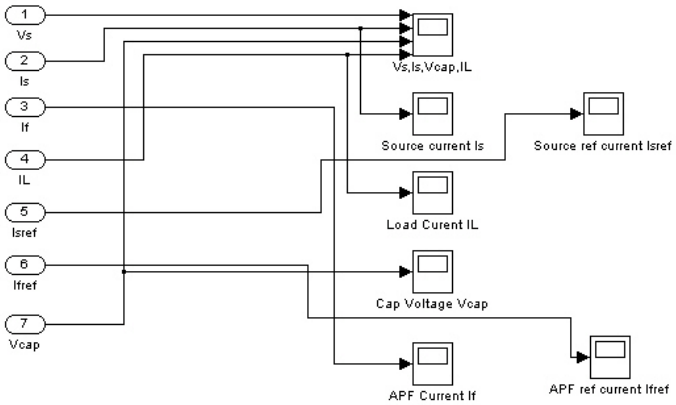
Appendix G: Switch Sampler

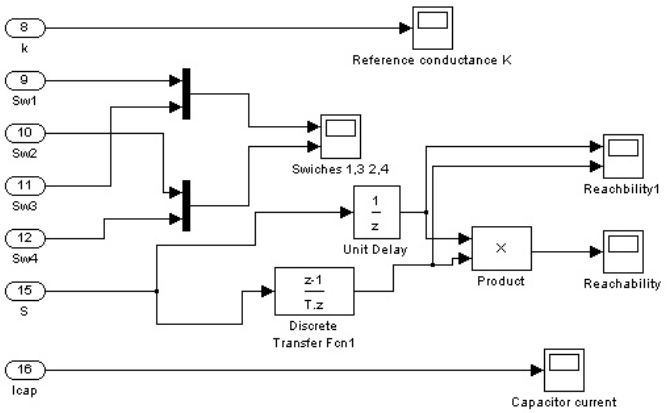


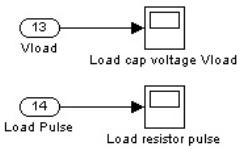
Appendix G: Sliding Surface



Appendix G: Measurements







Appendix H: Matlab control algorithm switch_control6.m (for use with APF6.mdl given in Appendix G)

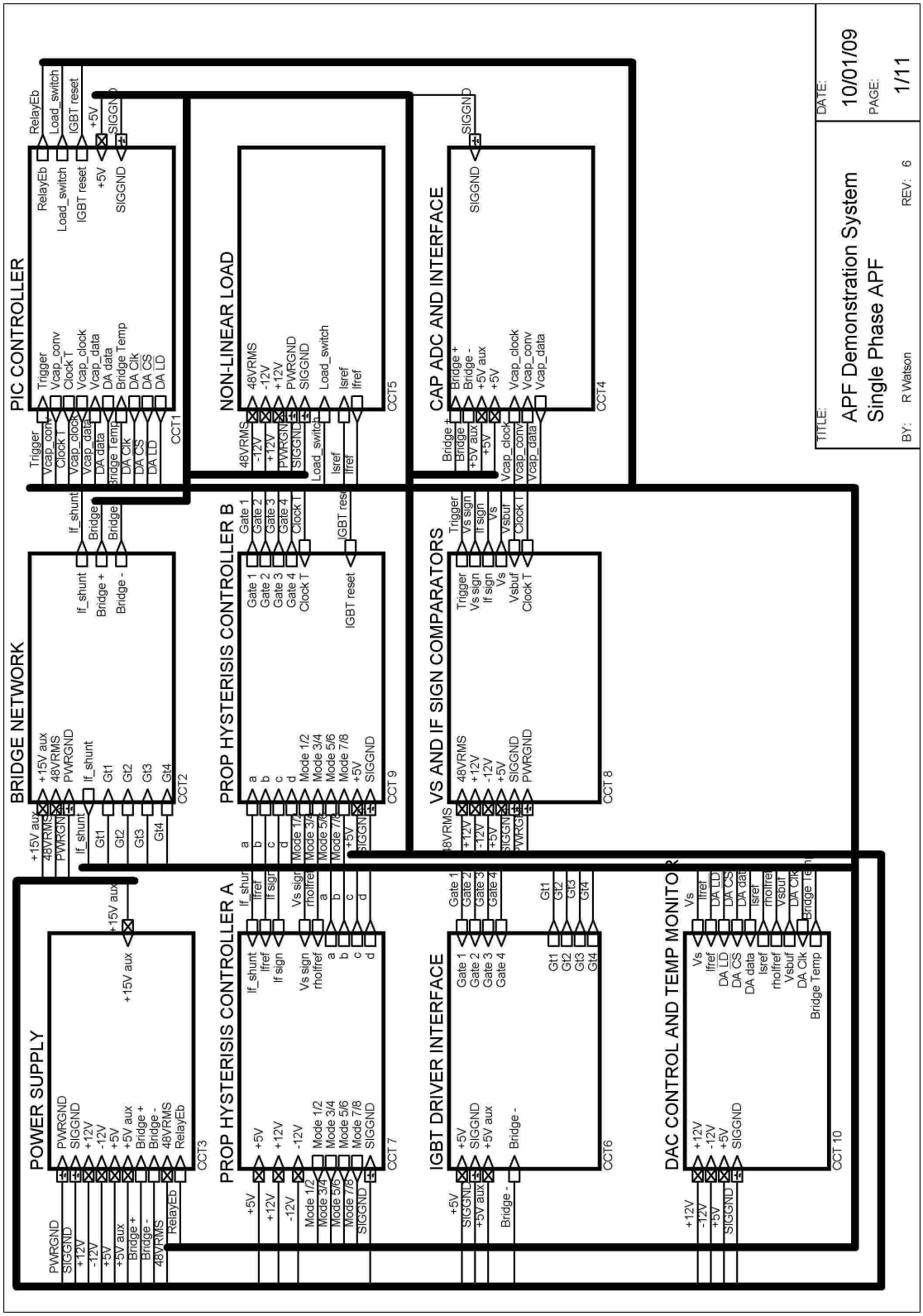
```
function [y]=switch_control6(u)

%This function is fir use with APF6.mdl given inAppendix G
%The sliding equation is extededed to second order
%The system incorporates a PI controller as discussed in section 3.15.2
%T must be set in the workspace

%Input variable assignment
Vref=u(1);
flag=u(2);
%sw's take on old values (from last sample period)
s4=u(3);
s3=u(4);
s2=u(5);
s1=u(6);
S=u(7);
Ifref=u(8);
flag1=u(9);

pos=0;
neg=0;
U=0;
check_sw=~(s1|s2|s3|s4); %check_sw is 1 only if all sw's are 0 i.e. end of a
                         %passive phase

if(Vref > 0.1)
   pos=1; %corresponding to Alpha = 1
end

if(Vref < 0.1)
   neg=1; %corresponding to Alpha = -1
end

% The following four variables are active phase indicators
pos_del_inc=0; %reset positive supply, power delivered to source, increasing
pos_abs_inc=0; %reset positive supply, power absorbed from source, increasing
neg_del_inc=0; %reset negative supply, power delivered to source, increasing
neg_abs_inc=0; %reset negative supply, power absorbed from source, increasing

%Use the previous sample switch states (from switch sampler) to assign
%values to the active phase indicators.
if(s1&&s4&&~s2&&~s3)
   pos_del_inc=1;
end

if(s3&&~s1&&~s2&&~s4)
   pos_abs_inc=1;
end

if(s3&&s2&&~s1&&~s4)
   neg_del_inc=1;
end

if(s1&&~s2&&~s3&&~s4)
```

```
    neg_abs_inc=1;
end

%now reset all sw's
s1=0;
s2=0;
s3=0;
s4=0;

%The following four IF conditions assumme a passive state and set
%U accordingly.
%U may later be overriden if the stsate is active.
if(pos && (Ifref > 0)) %passive state and energy flowing into capacitor
    U = 1;
end
if(neg && (Ifref < 0))  %passive state and energy flowing into capacitor
    U = 1;
end
if(pos && (Ifref < 0))  %passive state and energy flowing out of capacitor
    U = -1;    %reverse current reference to match that flowing into capacitor
end
if(neg && (Ifref > 0))  %passive state and energy flowing out of capacitor
    U = -1;    %reverse current reference to match that flowing into capacitor
end

%The next section checks the system state against the sliding surface and
%decides if the next state should be active and then sets the switches
%accordingly.
%A signal U is produced to which is the ratio of source Voltage/cap voltage

    %Supply voltage positive (Alpha = 1)
    if(pos)
        if(S < 0)
            if(check_sw||pos_del_inc)
                % delivered increasing
                s1=1;
                s4=1;
                U=1;   % active delivered state
            end
        end

        if(S > 0)
            if(check_sw||pos_abs_inc)
                % Absorbed increasing
                s3=1;
                U=0; % active absorbed state
          end
        end
    end

   %Supply voltage negative (Alpha = -1)
    if(neg)
        if(S < 0)   %S < 0 not S > 0 since current error multiplied by Vs to form S
            if(check_sw||neg_del_inc)
                % delivered increasing
                s3=1;
                s2=1;
                U = 1; % active delivered state
            end
        end
```

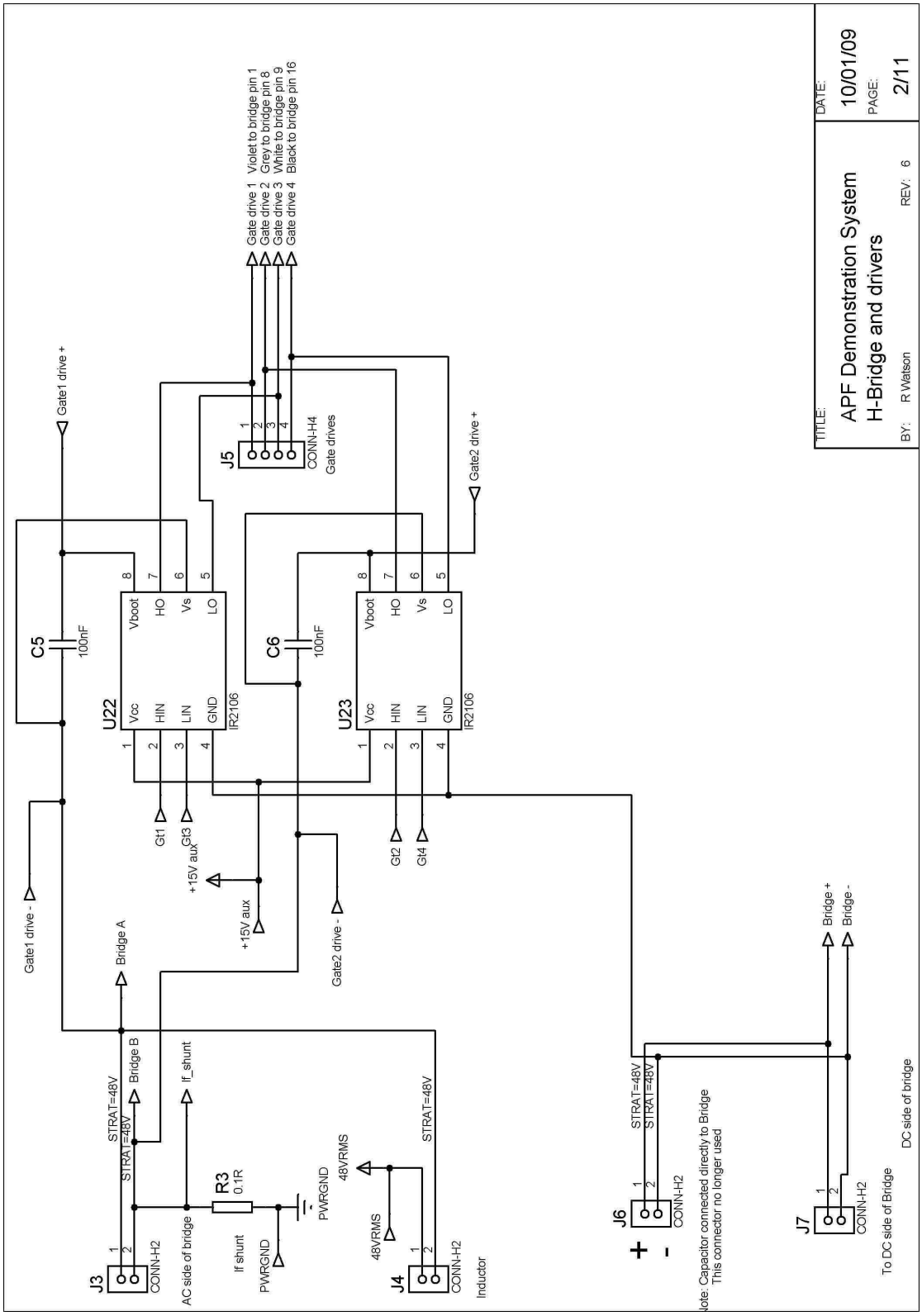
```
115.
116.        if(S > 0)   %S > 0 not S < 0 since current error multiplied by Vs to form S
117.            if(check_sw||neg_abs_inc)
118.                % absorbed increasing
119.                s1=1;
120.                U=0; %active absorbed state
121.            end
122.        end
123.    end
124.
125.%At this point, if all switches are zero then the next phase will be
126.%passive.
127.
128.%override switch control for first sample period of T to allow bridge to
129.%initialise
130.if(~flag1)
131.    s1=0;
132.    s2=0;
133.    s3=0;
134.    s4=0;
135.end
136.
137.%Update all output variables
138.y(1)=s1;
139.y(2)=s2;
140.y(3)=s3;
141.y(4)=s4;
142.y(5) = U;
```

Appendix I: Circuit diagrams for Practical demonstration system using Proportional hysterisis and energy compensation

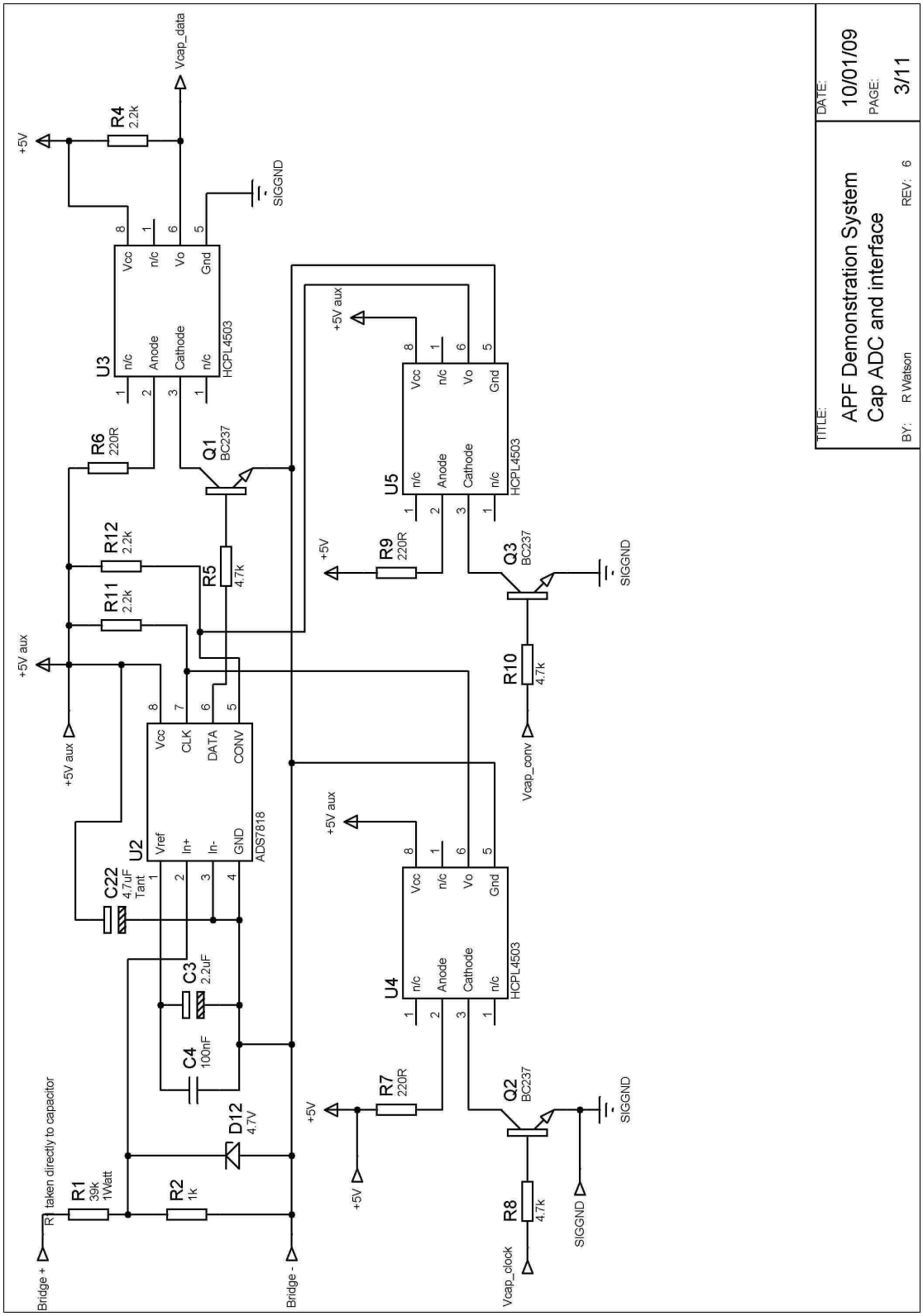
Appendix I: sheet 1



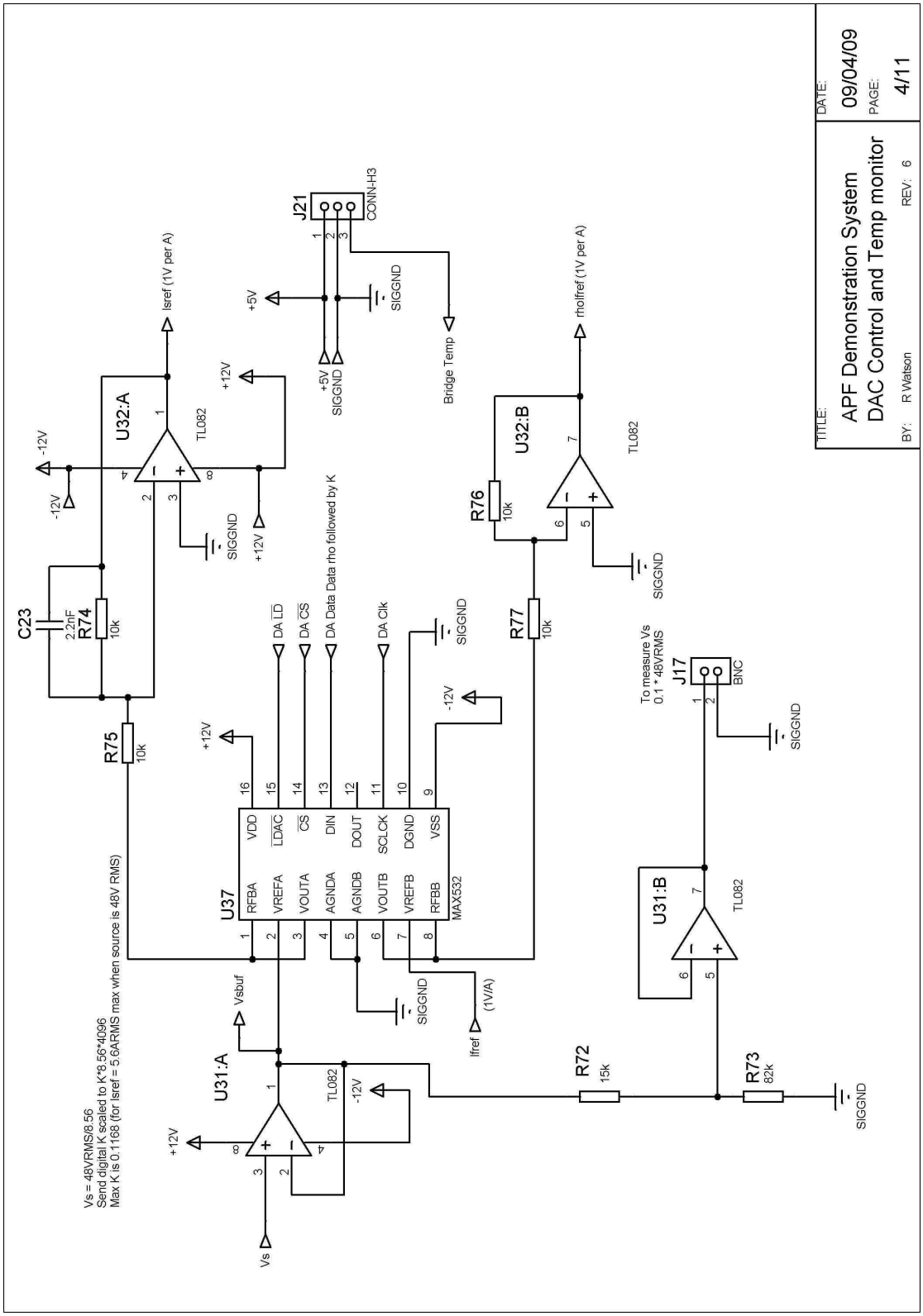
Appendix I: sheet 2



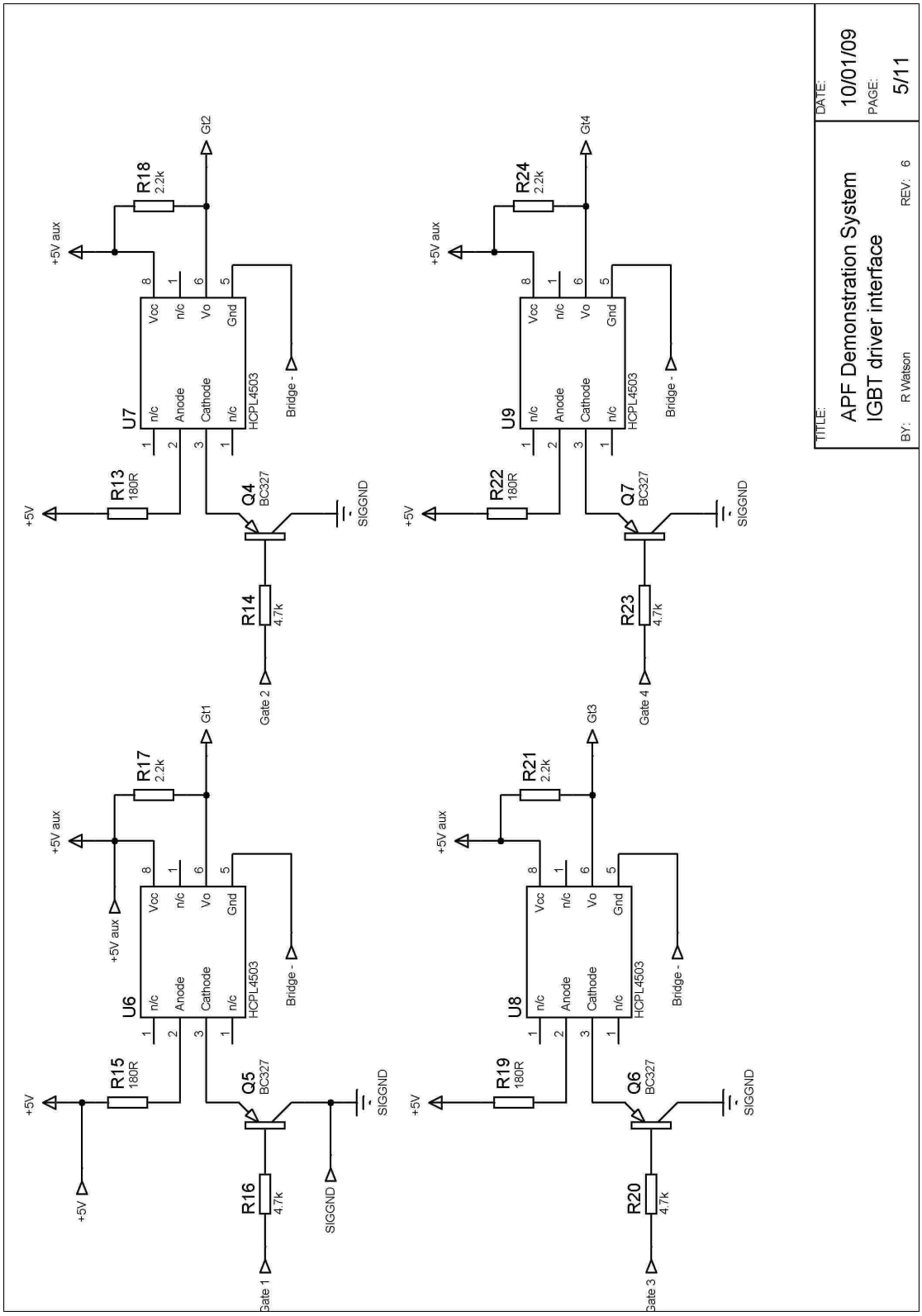
Appendix I: sheet 3



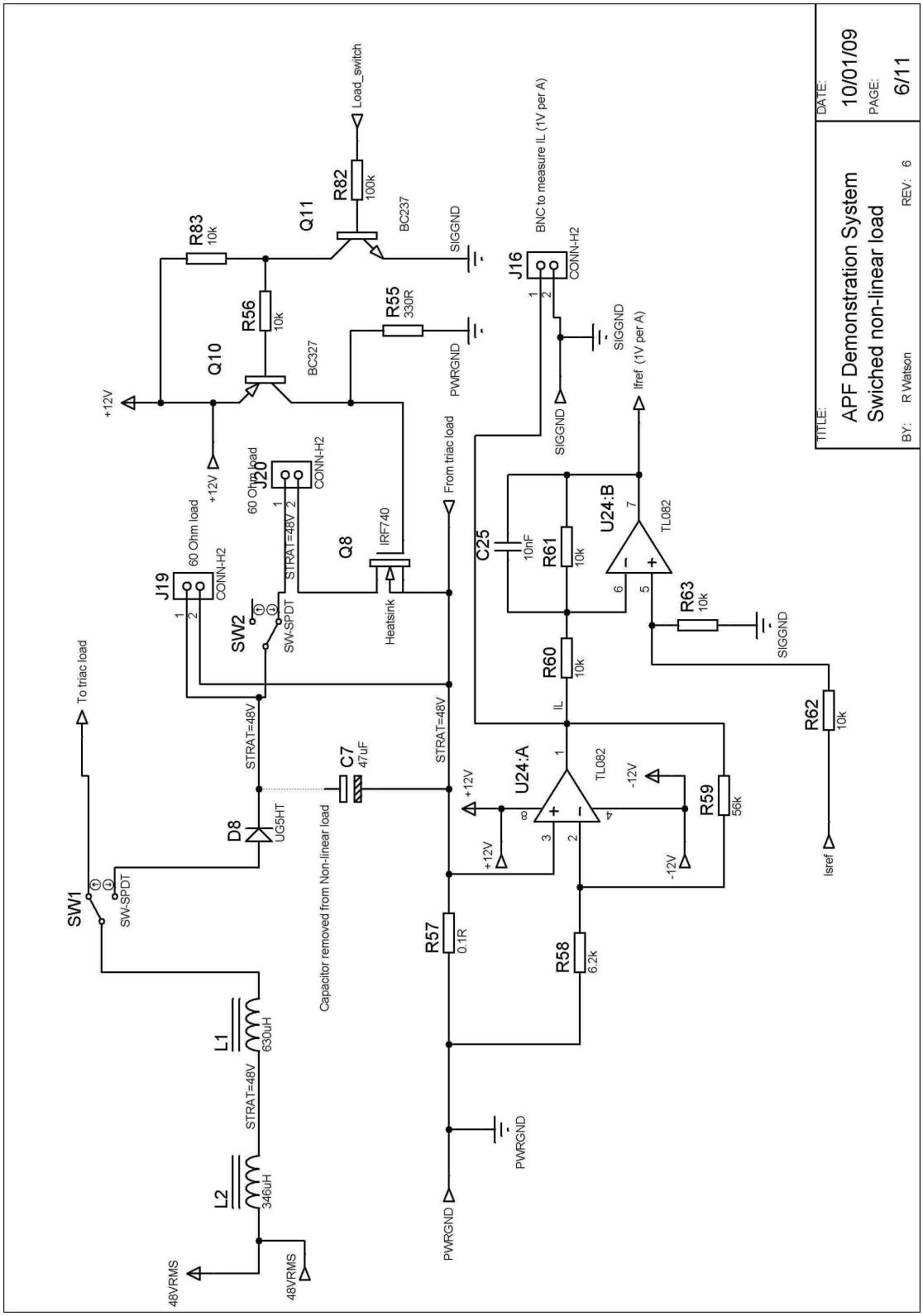
Appendix I: sheet 4



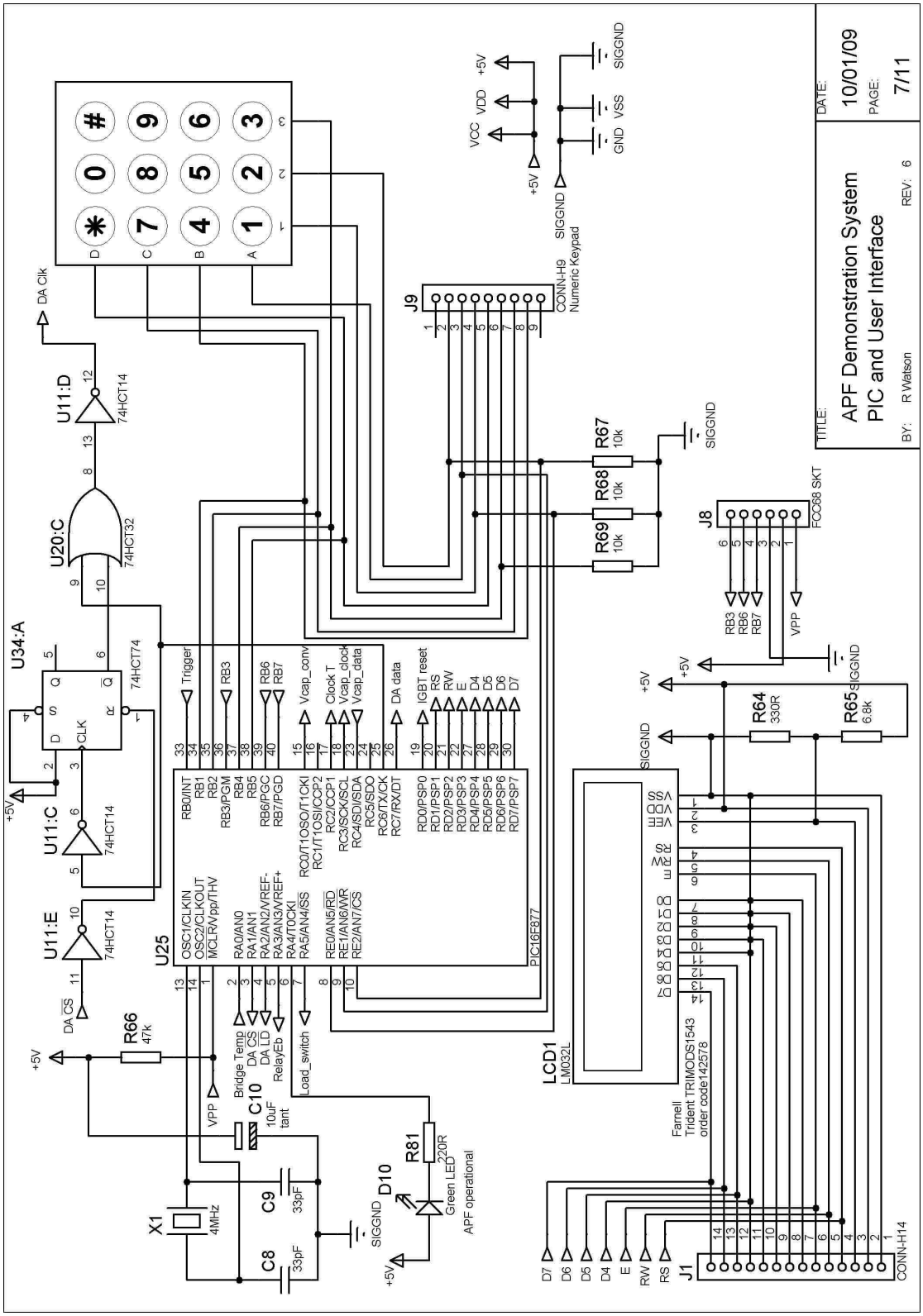
Appendix I: sheet 5



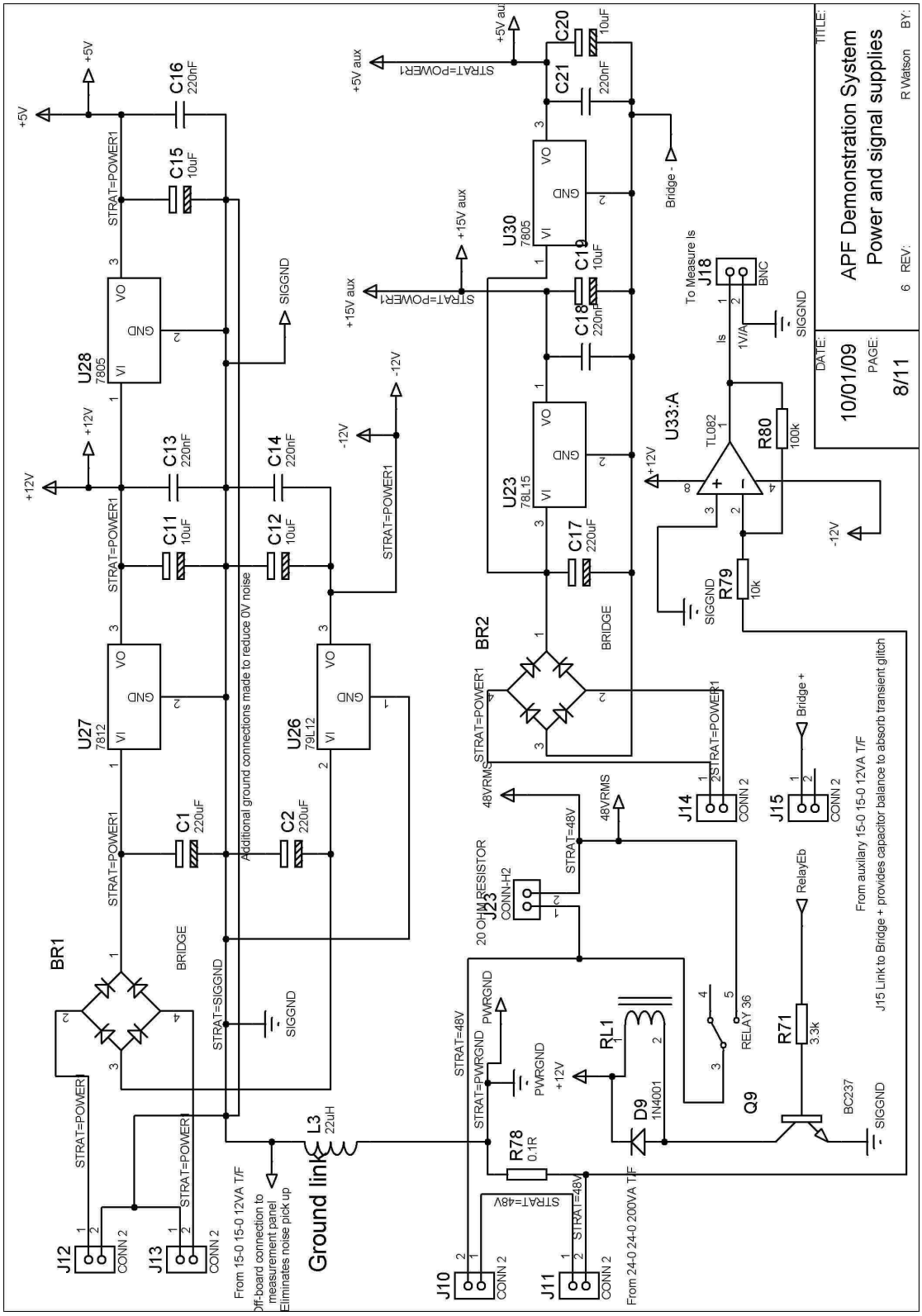
Appendix I: sheet 6



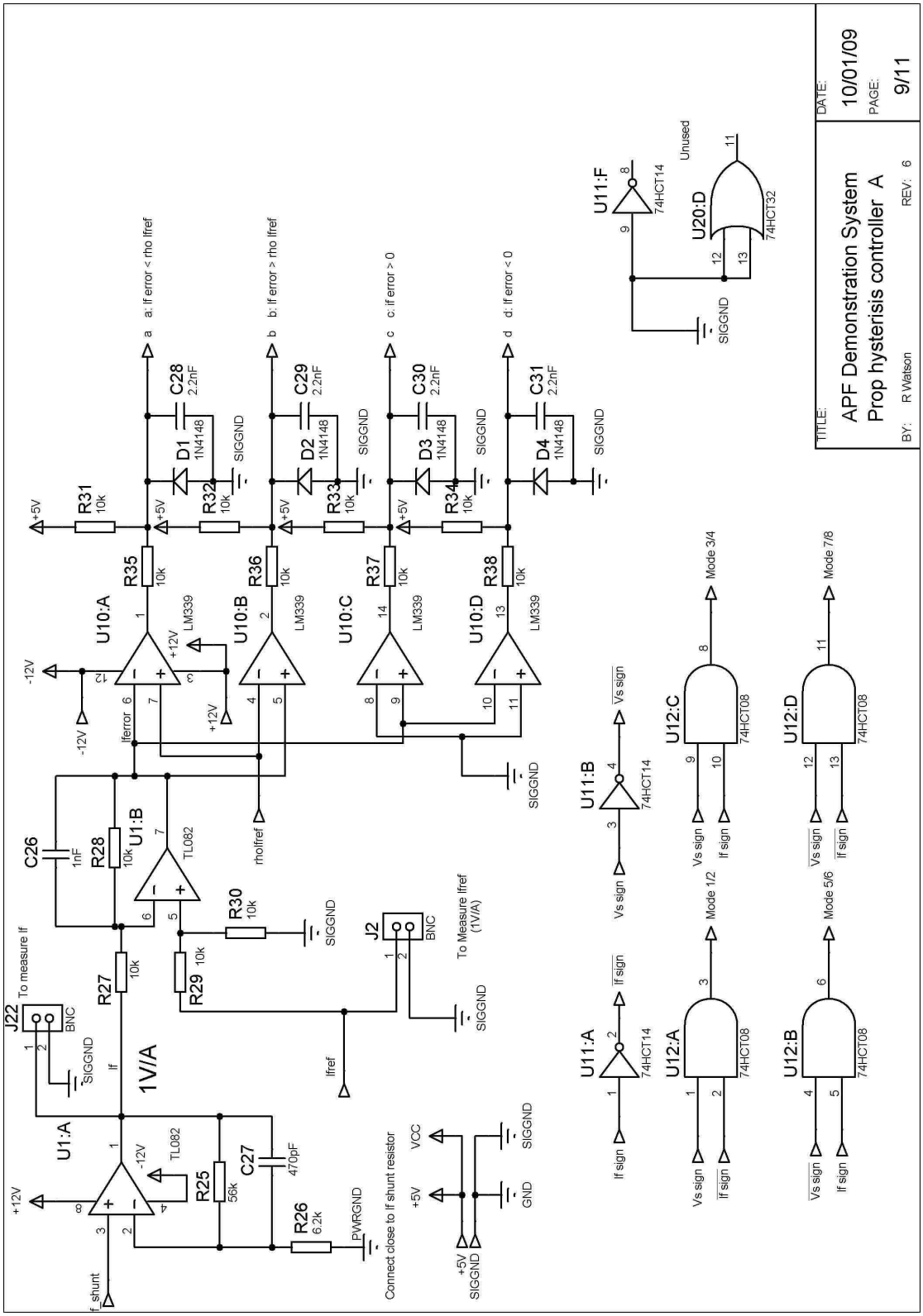
Appendix I: sheet 7



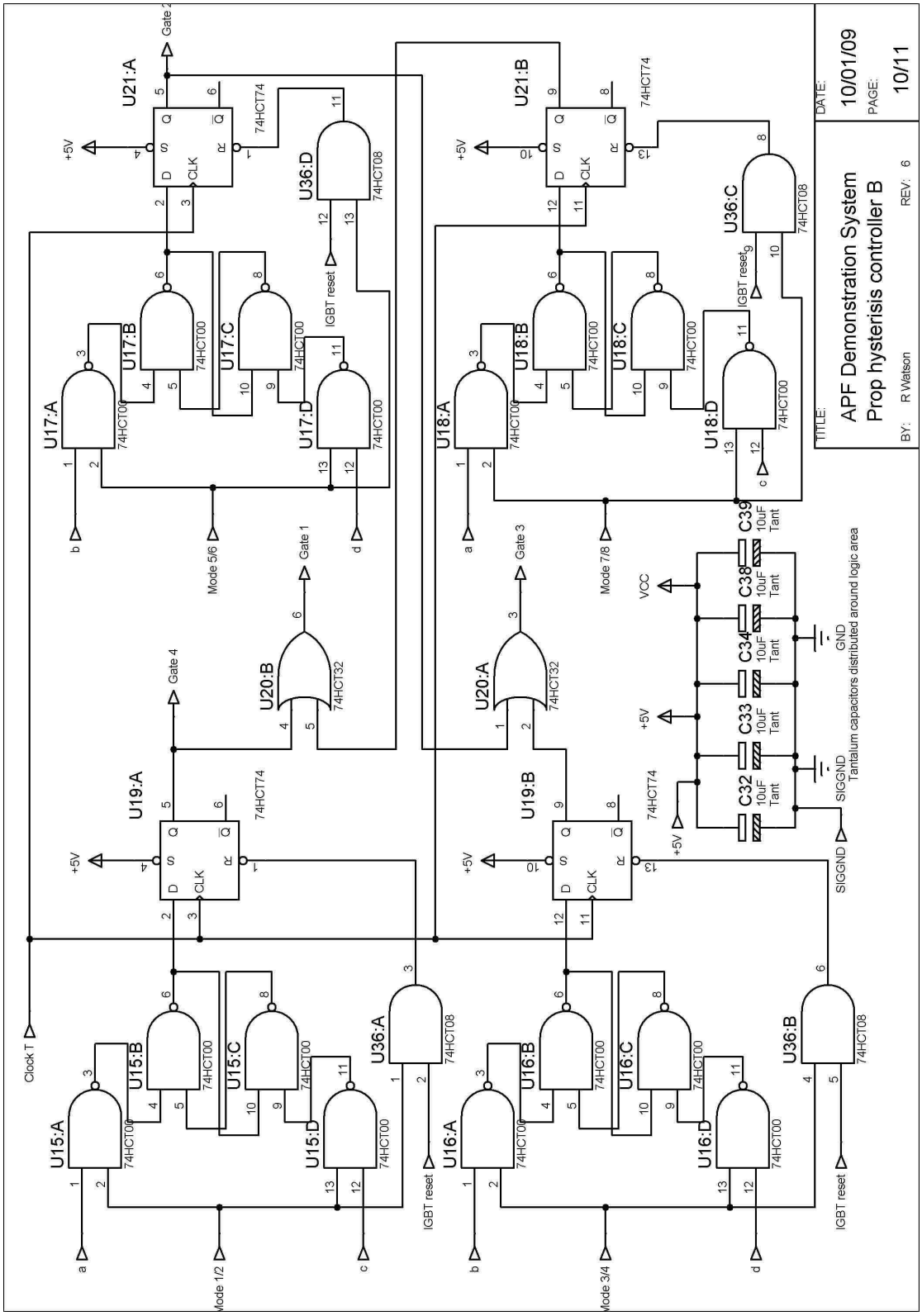
Appendix I: sheet 8



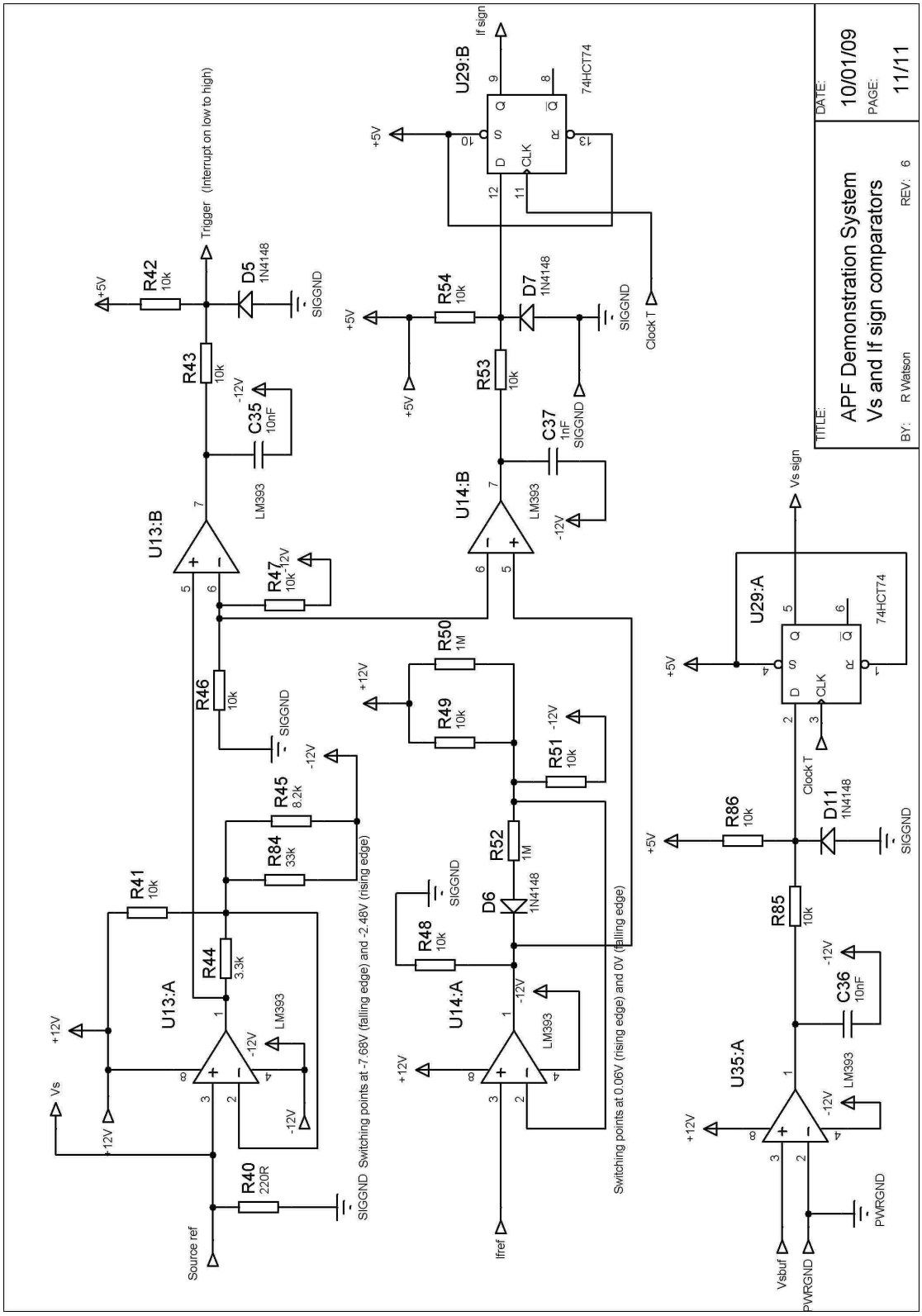
Appendix I: sheet 9



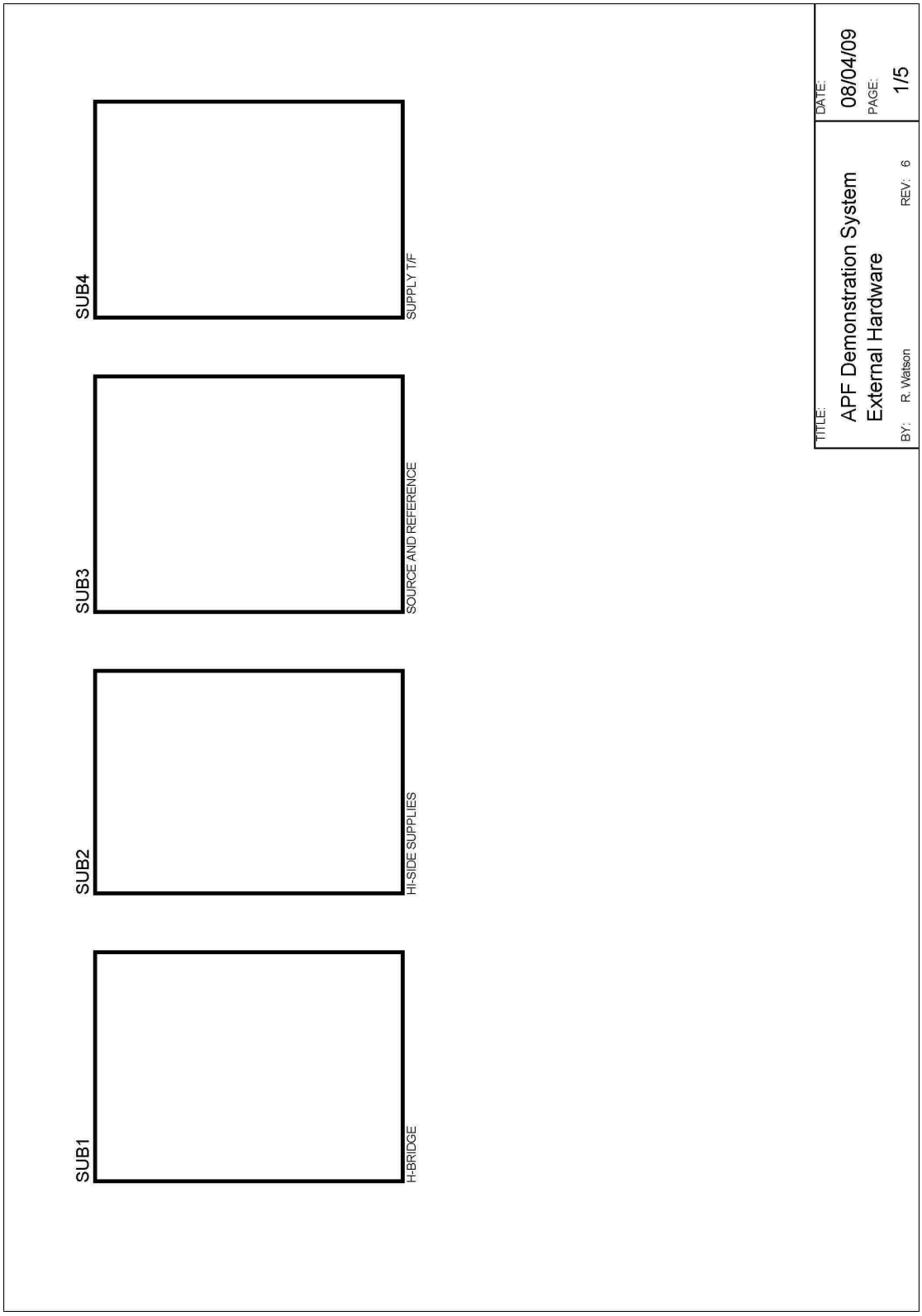
Appendix I: sheet 10



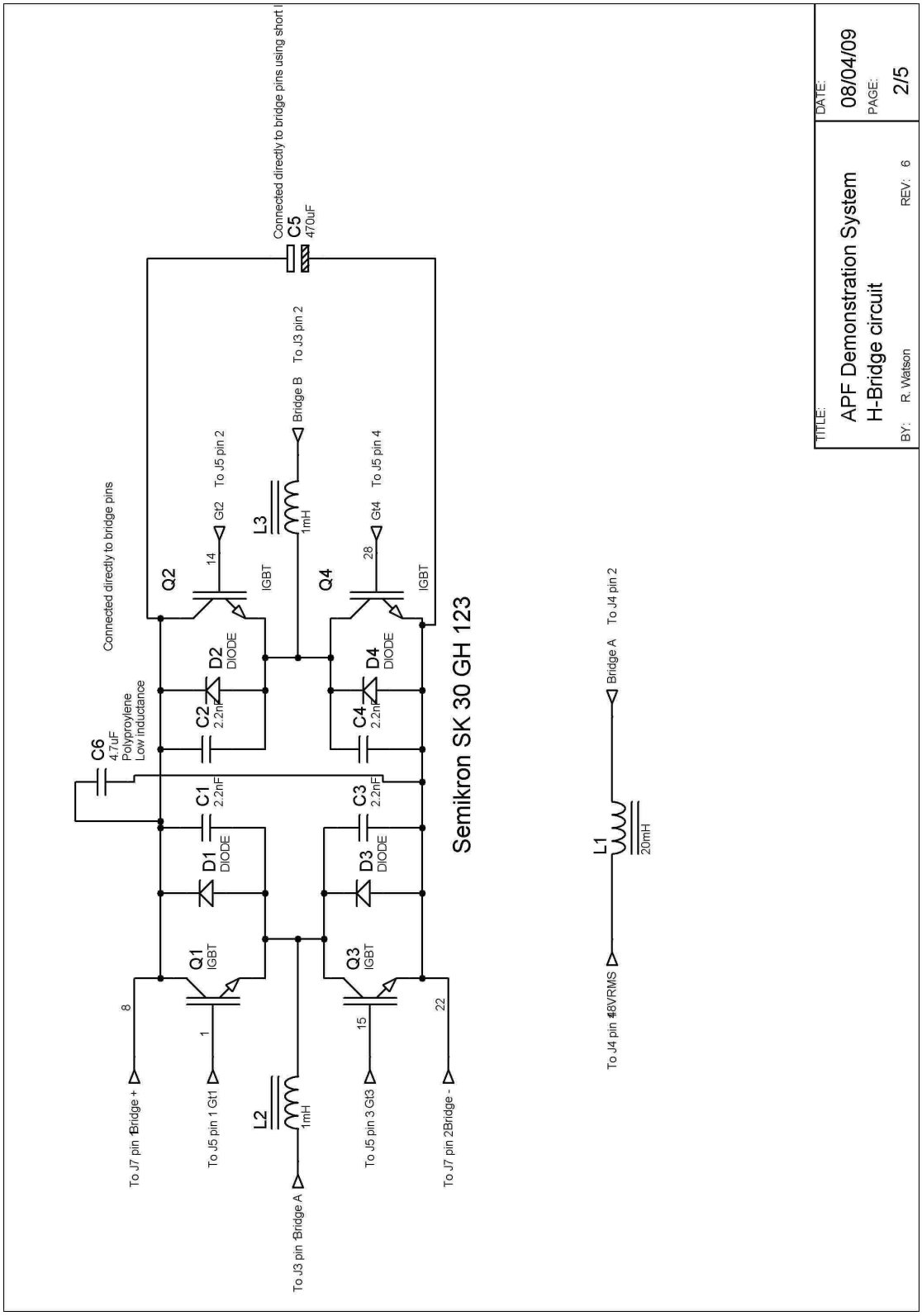
Appendix I: sheet 11



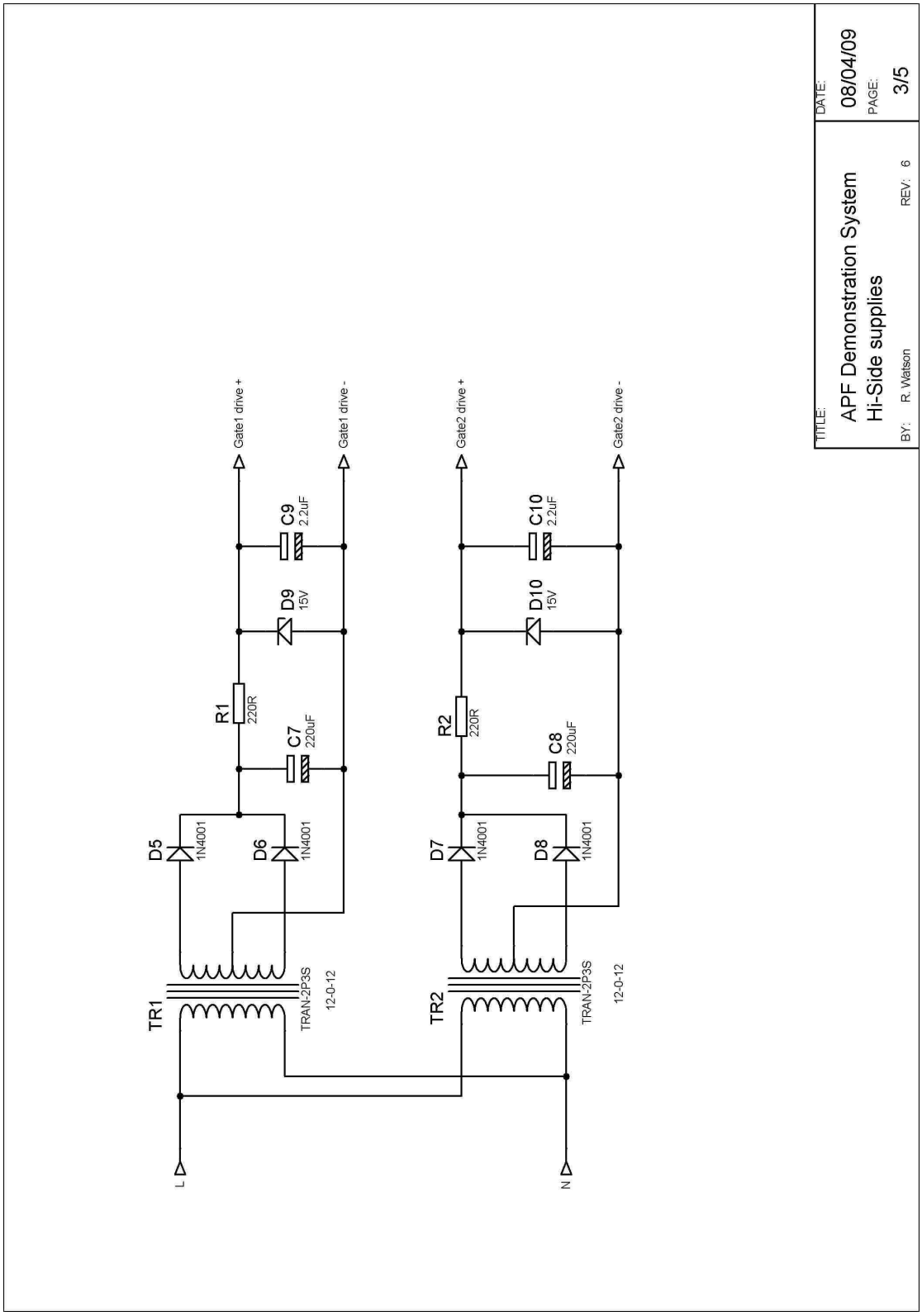
Appendix I: circuit components mounted off the PCB sheet 1



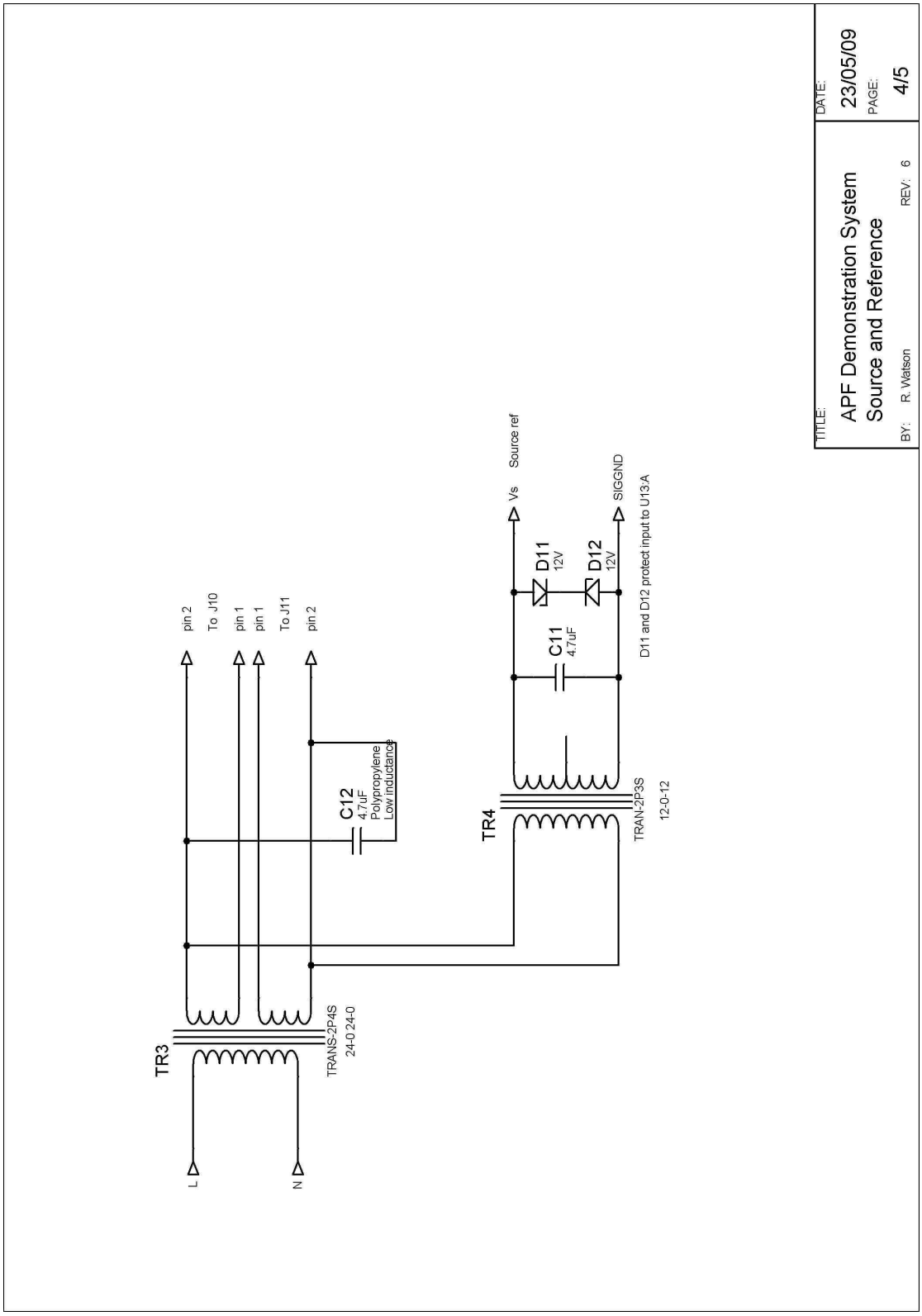
Appendix I: circuit components mounted off the PCB sheet 2



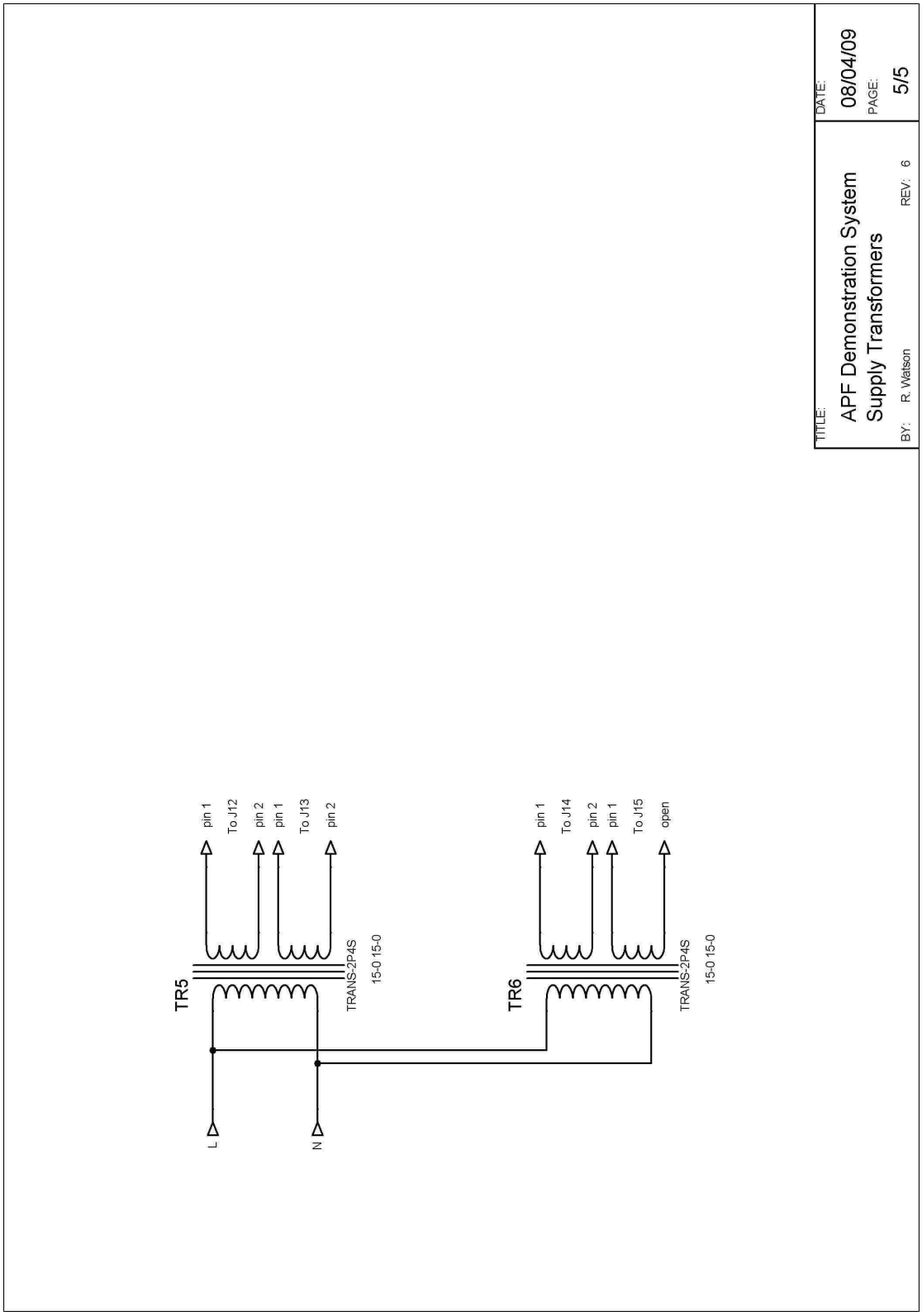
Appendix I: circuit components mounted off the PCB sheet 3



Appendix I: circuit components mounted off the PCB sheet 4



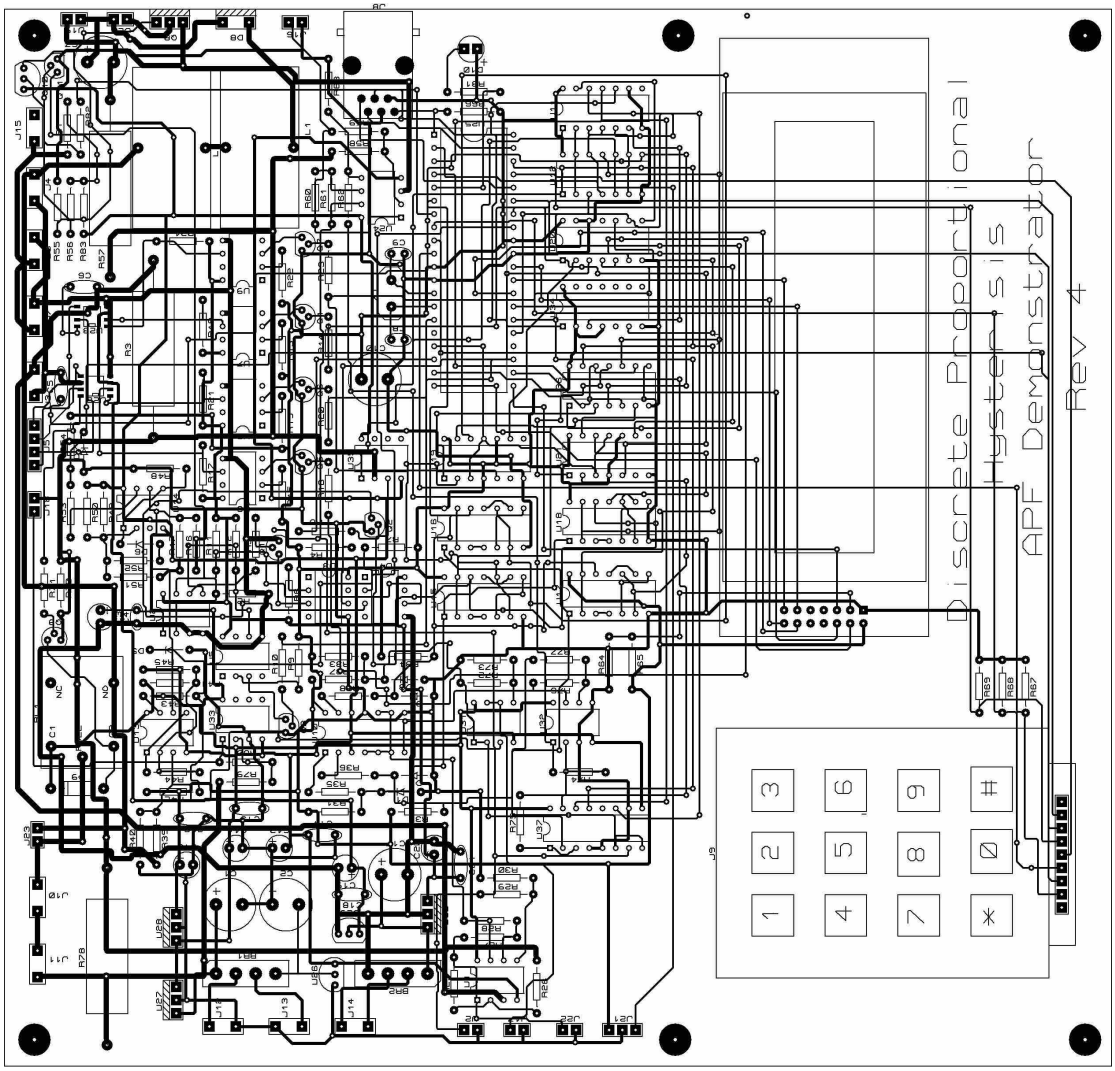
Appendix I: circuit components mounted off the PCB sheet 5



Appendix J: Demonstration system PCB layout and construction

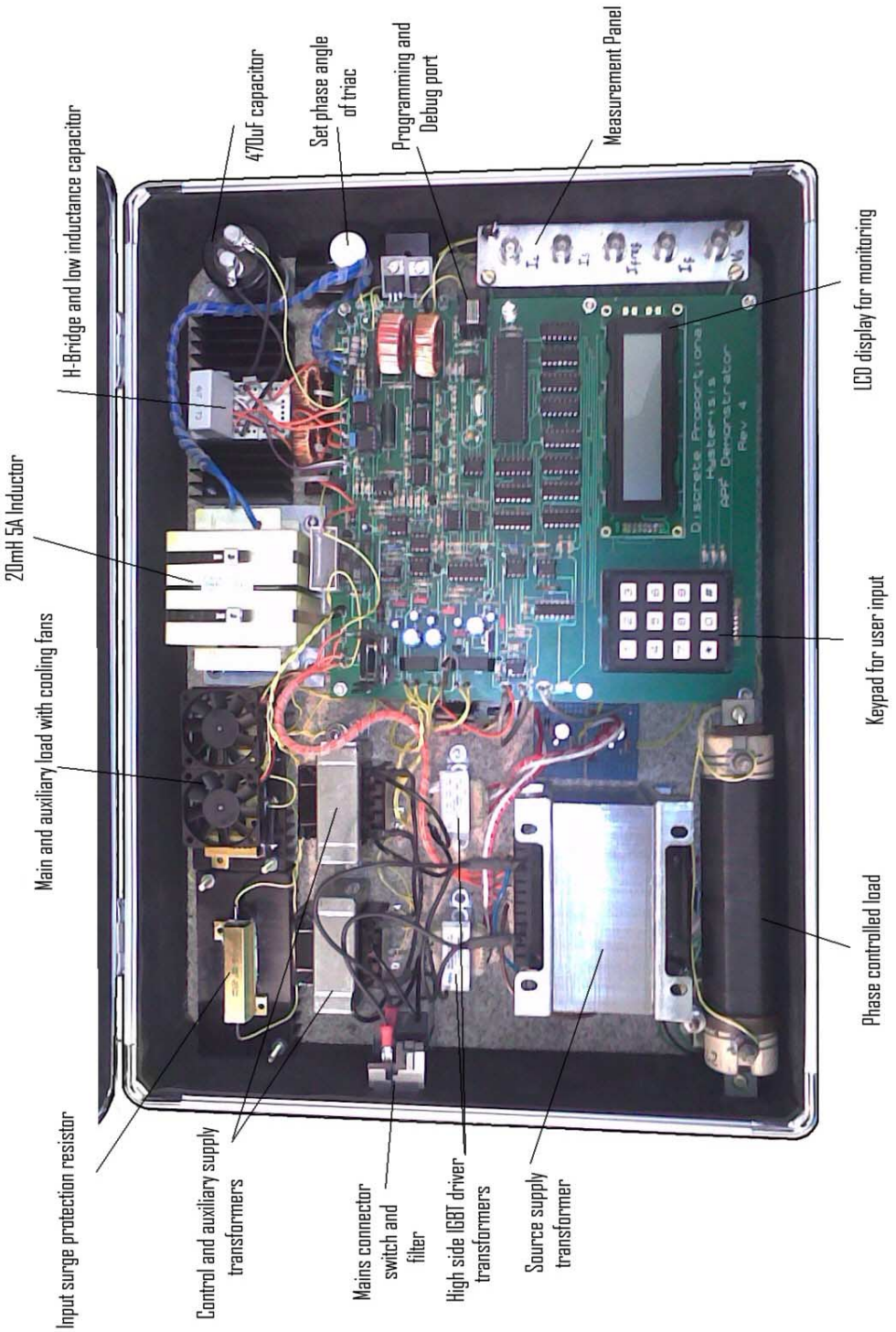
Appendix J: Layout

The following diagram details the PCB layout for use in the Demonstration system using Discrete Proportional Hysterisis switching and Energy Compensation control.



Appendix J: Construction

The following photograph shows the completed and functional APF demonstration system using discrete proportional hysterisis switching with energy compensation control. The demonstration system is equipped with two non-linear loads – a switched half-wave rectified load (for examining transient response) and a triac load with variable phase angle.



Appendix K: C listing for APF demonstration system

Appendix K: apf.c

This is the c listing for the code APF.c running in the PIC processor of the demonstration system. The code provides both control and user interface.

```
/*
**************************************
*  APF control and user interface                *
*                                                 *
*            R.V.Watson                           *
**************************************
*/

#device PIC16F877
#fuses
XT,NOWDT,PUT,NOPROTECT,NOBROWNOUT,NOLVP,NOCPD,NOWRT
#include <16F877a.h>  //R.Watson's header file for pic16f877
#include <DIS_LCD.h>  //R.Watson's header file for display functions
#include <keypad.h>   //R.Watson's header file for the keypad
#use delay(clock=4000000)


/*
*********************
* APF Global data          *
*                          *
*********************
*/

void reset_APF();
void APF_modes();
void sample_rate(int);
void Kscaler(void);
void rhocalc(void);
void mdac_out(void);
long Vcap_ADC(void);
short selection(void);
void stop_APF(void);
void start_APF(void);
void outchar(char);
void set_epsilon(void);
void set_T(void);
void set_load_rate(void);
int capvoltscaler(long);
void measure_cap_volt(void);
void display_K(void);
```

```
void outdac(int);
char text[21]; //text array to be displayed
long Kscaled,rho,vcapref,vcap,vcapold;
float K, epsilon;
short APF_ON,ld,load,load_on;
int T,load_delay,Vs,phase;
char const message[20] = "1 inc, 3 dec, # ret";

#define igbt_reset portd.pin0
#define da_ck portc.pin6
#define da_data portc.pin7
#define da_cs porta.pin1
#define da_ld porta.pin2
#define relayeb porta.pin3
#define led porta.pin4
#define load_switch porta.pin5
#define bridge_temp porta.pin0
#define vcap_conv portc.pin0
#define vcap_clock portc.pin3
#define vcap_data portc.pin4
#define clock_t portc.pin2
#define trigger portb.pin0

/*
**********************************
*APF external interrupt Function          *
*Occurs on rising edge of Trigger                  *
**********************************
*/

#int_ext
void Ra0_ext_interrupt()
{
signed long vcapdiff,vcapsum,deltaE,deltaEcomp;
float temp;
int n,checkcount;
//check for false trigger
for (checkcount = 0; checkcount < 20 ; checkcount++);
if(trigger == 0)
        {
        intcon.intf=0;
        return;
        }
phase = phase + 6; //add 6ms to load rate timer period
for (n=0; n < 2 ; n++)
        {
        for (checkcount = 0; checkcount < 255 ; checkcount++);
        }
vcap = Vcap_ADC();
vcapdiff = vcap - vcapold;
```

```
vcapsum = vcap + vcapold;
deltaE=vcapsum/Vs;
temp=vcapdiff/Vs;      //greater precision required therefore use float
deltaE=temp*deltaE;

vcapdiff = vcap - vcapref;
if ((vcapdiff > 30)||(vcapdiff < -30)) // +-1.5V error allowed
        {
        vcapsum = vcap + vcapref;
        deltaEcomp=vcapsum/Vs;
        temp=vcapdiff/Vs;
        deltaEcomp=temp*deltaEcomp;
        deltaEcomp=deltaEcomp*epsilon;
        }
else
        {
        deltaEcomp = 0;
        }
//Kscaled is unsigned but deltaE and deltaEcomp are signed

deltaE = deltaE + deltaEcomp;

if(deltaE < 0) //deltaE -ve
        {
        deltaE = -deltaE; //reverse sign
        Kscaled = Kscaled + deltaE;
        if (Kscaled > 1402)
                {
                Kscaled = 1402; // restrict K to 0.04 so that max Is = 1.92A
                }
        }
else
        {
        if(deltaE < Kscaled) //deltaE +ve
                {
                Kscaled = Kscaled - deltaE;
                }
        else
                {
                Kscaled = 0; //saturation limiter K = 0
                }
        }
// wait until trigger goes low
while(trigger);
vcapold = vcap;
mdac_out(); //updare two channel mdac
intcon.intf=0;
}
```

```
#int_timer0                //used to control load switching rate
void interrupt_function()
{
tmr0 = 197;
phase++;
if (phase > load_delay)
          {
          load = !load;
          load_switch=load;
          phase = 0;
          }
intcon.t0if=0;             //clear timer0 flag
}


#include <utility.c>


/*
**********************
*APF reset Function      *
*                        *
**********************
*/

void reset_APF()
{
int loopcount;
short error1,error2;
trisb=0xd9;
trisc=0x32;
trisd=0x00;
trise=0x05; //trise.pin4 to be 0 to disable PSPMODE
trisa=0x01;

//set up timer 0
option_reg.t0cs=0; //enable clock source as fosc/4
option_reg.psa=0; //select prescaler
option_reg.ps = 3; //programmable prescaler set to divide by 16: 16us period
intcon.gie=1;//enable global interrupt
intcon.peie=1;//peripheral interrupts enabled
intcon.t0ie=0;//disable timer0 interrupt

option_reg.intedg=1;  //interrupt on low to high on RB0

load_delay = 200;      //200ms default load switch period

vcapref=2044;          //equivalent to 100V

Vs=54;                 //default supply RMS voltage
```

```
phase=0;

APF_ON = 0;          //status test bit
relayeb=0;           //relay off for power up condition
load_switch=0;       //turn off switched load
ld=0;
load=0;
load_on=0;
igbt_reset=0;         // hold igbts in reset
led = 1;             //APF running status indicator - led off
da_ld = 1;           //disable mdac load
da_cs = 1;           //disable mdac chip sel and hence set mdac clock = 0
vcap_conv = 0;       //stop cap adc conversion
vcap_clock=0;

//set up timer 2 and PWM mode
t2con.tmr2on=0;      //ensure timer2 is off
t2con.t2ckps=0;      //prescaler set to 1
t2con.toutps=0;       //post scaler set to 1-not needed for pwm
pie1.tmr2ie=0;
//timer 2 now clocked at 1 MHz
ccp1con.ccp1m=0xC; // select PWM mode

T=19; //microsecs - default of 20 us sample rate
//transfer period to PWM module
sample_rate(T);      //set default sample rate
t2con.tmr2on = 1;    //turn on pwm output

//set up spi module
//spi is used to read cap voltage
vcap_clock=0;
sspcon.sspen=1;      //enable synch serial port
sspcon.ckp = 0;      //idle state clock is low
sspstat.cke=0;       //transmission of clock on idle to active state
sspcon.sspm=2;       //select fosc/64 as clock rate
sspstat.smp=1;       // sample data at start of next clock pulse (data sheet fig 9.2)

//set up A-D
adcon1.adfm = 1;      //right justify 10 bit result
adcon1.pcfg = 0xE;   // Only RA0 as analogue input
//for clock 4MHz
adcon0.adcs = 1;     //A-D conversion clock = Fosc/8
adcon0.adon = 1;     //turn on A-D
adcon0.chs = 0;      //A-D mux to RA0

//mdac is used to transfer K and rho
//set up USART for MDAC
//Use USART synchronous master mode baud rate generator:
```

```
txsta.brgh=0;
spbrg=1;         //clock = 500kHz
txsta.sync = 1; //synchronous mode
rcsta.spen=1;   //configure rc6 to clock and rc7 to data
txsta.csrc=1;    //enter master mode
pie1.txie=0;
pie1.rcie=0;
txsta.tx9=0;     //transmit enabled
txsta.txen=0;    //temporarily gate off transmit clock
rcsta.sren=0;   //don't require serial receive enabled
rcsta.cren=0;    //don't require continuous receive enable



//set up K and epsilon
Kscaled = 351; //set up Kscaled with K = 0.01
epsilon=0.4;    //default value
//evaluate rho
rhocalc();         //evlauate rho from epsilon

//send Kscaled and rho to MDAC
MDAC_out();

//set up lcd display
init_display();
clear_display();
set_display_add(0,0x05);
strcpy(text,"APF Reset");
print_display(9,text);

//perform system check
for (loopcount=0;loopcount<8;loopcount++)
          {
          delay_ms(250); //cap charging time
          }
error1=error2=1;
vcap=Vcap_ADC();
if (vcap > 1227) error1 = 0;    // 60Volts * 409/20
delay_ms(5);
vcap=Vcap_ADC();
vcapold=vcap;
if (vcapold > 1227) error2 = 0;
if(error1 || error2)                  //error found-cap hasn't charged
          {
          clear_display();
          strcpy(text,"Cap Voltage low");
          set_display_add(0,2);
          print_display(15,text);
          strcpy(text,"Fault: APF disabled");
          set_display_add(1,0);
```

```
        print_display(19,text);
        while(1);
        }
relayeb=1;      //system healthy - short input surge protection resistor

clear_display();
set_display_add(0,2);
strcpy(text,"APF System Ready");
print_display(16,text);
set_display_add(1,0);
strcpy(text,"Press # for modes");
print_display(17,text);
//check for a # from keypad
while(readkey() != '#');
while(readkey() == '#');        //wait for key release
return;
}



/*
*********************
*APF modes Function    *
*                      *
*********************
*/

void APF_modes()
{
char inkey;
clear_display();
if (APF_ON)
        {
        strcpy(text,"* To Stop APF ");
        }
else
        {
        strcpy(text,"* To Start APF");
        }
set_display_add(0,3);
print_display(14,text);
set_display_add(1,1);
strcpy(text,"# For set-up modes");
print_display(18,text);
while(((inkey=readkey()) != '#') && (inkey != '*'));
while (readkey() != '\0');      //wait for key release
if (inkey == '*')
        {
        if(APF_ON)
                {
```

```
                stop_APF();
                }
        else
                {
                start_APF();
                }
        return;
        }
//Next menu item
clear_display();
strcpy(text,"Set epsilon");
set_display_add(0,5);
print_display(11,text);
if (selection())
        {
        set_epsilon();
        return;
        }
//Next menu item
clear_display();
strcpy(text,"Set sample period T");
set_display_add(0,0);
print_display(19,text);
if (selection())
        {
        set_T();
        return;
        }
//Next menu item
clear_display();
strcpy(text,"Set load change rate");
set_display_add(0,0);
print_display(20,text);
if (selection())
        {
        set_load_rate();
        return;
        }
//Next menu item
clear_display();
strcpy(text,"Set cap volt-ref");
set_display_add(0,2);
print_display(16,text);
if (selection())
        {
        set_capref();
        return;
        }
//Next menu item
clear_display();
```

```
strcpy(text,"Measure cap voltage");
set_display_add(0,0);
print_display(19,text);
if (selection())
        {
        measure_cap_volt();
        return;
        }

//Next menu item
clear_display();
strcpy(text,"Display K");
set_display_add(0,5);
print_display(9,text);
if (selection())
        {
        display_K();
        return;
        }
//Next menu item
clear_display();
strcpy(text,"Display bridge temp");
set_display_add(0,0);
print_display(19,text);
if (selection())
        {
        display_temp();
        return;
        }
//Next menu item
clear_display();
strcpy(text,"Enter source RMS");
set_display_add(0,0);
print_display(16,text);
if (selection())
        {
        enter_RMS();
        return;
        }
}
```

```
/*
********************
*APF main Function      *
*                       *
********************
*/


void main(void)
{

reset_APF();                    //perform system reset and system check
while(1)
        {
        APF_modes();            //enter user interface menu system
        }
}

#include <DIS_LCD.c>
#include <keypad.c>
```

Appendix K: utility.c

This is the c listing for the code utility.c running in the PIC processor of the demonstration system. The code provides the controllers called from apf.c.

```
/*
*******************************
* APF selection Function      *
* returns 1 for a *           *
* returns 0 for a #           *
*******************************
*/
short selection()
{
char inkey;
set_display_add(1,0);
strcpy(text,"* setup, # next mode");
print_display(20,text);
while(readkey() == '\0');
inkey=readkey();
while(readkey() != '\0');
if (inkey == '*')
        {
        return(1);
        }
else
        {
        return(0);
        }
}

/*
*******************************
* APF sampling clock Function *
*  (using PIC PWM module)     *
*******************************
*/

void sample_rate(int period)
{
//clock running at 1 MHz
pr2 = period;
//2 least sig bits of ccp1con affecting duty cycle
period=period/2; //1:1 duty cycle
ccp1con.ccp1y=0;
ccp1con.ccp1x=0;
ccpr1l=period;
}
```

```
/*
*********************************
* APF K scaling function Function         *
*                                         *
*********************************
*/

void Kscaler()
{
K=Kscaled; //copy long to float
K = K/35062; //35062 = 8.56 * 4096
}


/*
*****************************************
* APF rho calulating Function                          *
* (evaluates rho to be used in the MDAC)          *
*****************************************
*/

void rhocalc()
{
float temp;
temp=1+epsilon;
temp=4*epsilon/(temp*temp);
temp=2*(1-temp);
rho = 4096*temp;
}


/*
**************************
* APF mdac output Function      *
*                                 *
**************************
*/

//Transfer rho into DAC B then Kscaled into DAC A
void mdac_out()
{
int tx_data;
long temp;
temp=rho;
temp = temp >> 4;
tx_data=temp; //tx_data = bits 4 to 11 of rho
outdac(tx_data);
temp = Kscaled;
temp = temp >> 8;
```

```
tx_data=temp;
temp=rho;
temp=temp<<4;
tx_data=tx_data+temp; // tx_data= bits 0 to 3 of rho then bits 8 to 11 of Kscaled
outdac(tx_data);
tx_data=Kscaled; // tx_data= bits 0 to 7 of Kscaled
outdac(tx_data);
da_cs=1; //turn off adc chip sel
da_ld=0; //update dacs
da_ld=1;
}
/*
*********************************
* Function called by mdac output function *
*                                             *
*********************************
void outdac(int data_tx)
//bit7 of tx_data transmitted first therefore byte to be inverted.
{
int count,dacdata,da;
dacdata=0;
for(count=0 ;count < 8 ; count++)
        {
        dacdata = dacdata << 1;
        da=(data_tx & 1);
        dacdata=dacdata + da;
        data_tx = data_tx >> 1;
        }
txreg=dacdata;
da_cs=0;
txsta.txen=1;
while(!txsta.trmt); //wait for transmission
txsta.txen=0;
}

/*
**************************
* APF Cap ADC read Function  *
*                                 *
**************************
*/

long Vcap_ADC()
{
int temp,data_high,data_low;
long vcapvalue;
temp=0; //dummy byte
sspcon.ckp=1; //set idle state clock high first
vcap_conv = 1; //initiate conversion - puts ADC conv pin low
delay_us(5);
```

```
ssbuf = temp; //dummy data to clock to pin rc5 (not connected)
while(!sspstat.bf); //wait for received data
data_high=ssbuf;
ssbuf = temp;
while(!sspstat.bf);
data_low = ssbuf;
vcap_conv = 0; //stop conversion
sspcon.ckp = 0; //set idle clock back to 0
//sort data
data_low = data_low ^ 0xff; //invert all bits to compensate for opto
data_high = data_high ^ 0xff;
data_low = data_low >> 3; //1st bit from ADC is invalid
//data_high contains 7 ms bits, data_low contains 5 ls bits
vcapvalue = 0;
vcapvalue = data_high;
vcapvalue = vcapvalue << 5;
vcapvalue = vcapvalue + data_low +20;//20 compensates for noise offset
//speed up system by returning the unscaled value
return vcapvalue;
}

/*
**********************
* Stop the APF converter    *
*                           *
**********************
*/
void stop_APF()
{
igbt_reset = 0;
intcon.inte = 0;//disable edge interrupt
APF_ON=0;
led = 1;
}


/*
**********************
* Start the APF converter    *
*                           *
**********************
*/

void start_APF()
{
Kscaled = 351; //reset K back to start value of 0.01
MDAC_out();
igbt_reset = 1;
intcon.inte = 1;//enable edge interrupt
APF_ON=1;
```

```
led = 0;
}

/*
*************************
* Set the epsilon coefficient     *
* for energy compensation       *
*************************
*/

void set_epsilon()
{
char key;
clear_display();
printf(outchar, "epsilon = %0.2f",epsilon);
set_display_add(1,0);
strcpy(text,message);
print_display(19,text);
while(1)
        {
        while(readkey() == '\0');
        key=readkey();
        set_display_add(0,10);
        if(key == '1')
                {
                while(readkey()=='1');
                epsilon = epsilon + 0.05;
                if (epsilon > 0.9) epsilon = 0.9;
                printf(outchar, "%0.2f",epsilon);
                rhocalc();
                mdac_out();
                }
        if(key == '3')
                {
                while(readkey()=='3');
                epsilon = epsilon - 0.05;
                if(epsilon < 0.4) epsilon = 0.4;
                printf(outchar, "%0.2f",epsilon);
                rhocalc();
                mdac_out();
                }
        if(key == '#')
                {
                while(readkey()=='#');
                return;
                }
        }
}
```

```
/*
*************************
* set the sampling clock period *
*                               *
*************************
*/

void set_T()
{
char key,T1;
clear_display();
T1=T+1;
printf(outchar, "T = %2.0u microsec",T1);
set_display_add(1,0);
strcpy(text,message);
print_display(19,text);
while(1)
        {
        while(readkey() == '\0');
        key=readkey();
        set_display_add(0,4);
        if(key == '1')
                {
                while(readkey()=='1');
                T = T + 1;
                if (T > 39) T = 39;
                T1=T+1;
                printf(outchar, "%2.0u",T1);
                sample_rate(T);
                }
        if(key == '3')
                {
                while(readkey()=='3');
                T = T - 1;
                if (T < 19) T = 19;
                T1=T+1;
                printf(outchar, "%2.0u",T1);
                sample_rate(T);
                }
        if(key == '#')
                {
                while(readkey()=='#');
                return;
                }
        }
}
```

```
/*
**************************
* Set the rate for load switching   *
* Or put auxiliary load on/off      *
**************************
*/
void set_load_rate()
{
char key;
clear_display();
if(load_on && !ld)
        {
        printf(outchar, "Put aux load off 1/0?");
        while(readkey() == '\0');
        key = readkey();
        while(readkey() == key);
        if (key == '1')
                {
                load_switch = 0;
                set_display_add(1,0);
                printf(outchar, "Load off");
                load_on=0;
                delay_ms(250);
                delay_ms(250);
                delay_ms(250);
                return;
                }
        }
if(!load_on && !ld)
        {
        printf(outchar, "Put aux load on 1/0?");
        while(readkey() == '\0');
        key = readkey();
        while(readkey() == key);
        if(key == '1')
                {
                load_switch = 1;
                set_display_add(1,0);
                printf(outchar, "Load on");
                load_on=1;
                delay_ms(250);
                delay_ms(250);
                delay_ms(250);
                return;
                }
        }

clear_display();
printf(outchar, "load delay = %3.0u ms",load_delay);
set_display_add(1,0);
```

```
strcpy(text,message);
print_display(19,text);
while(1)
        {
        while(readkey() == '\0');
        key=readkey();
        set_display_add(0,13);
        if(key == '1')
                {
                while(readkey()=='1');
                load_delay = load_delay + 5;
                if (load_delay > 250) load_delay = 250;
                printf(outchar, "%3.0u",load_delay);
                }
        if(key == '3')
                {
                while(readkey()=='3');
                load_delay = load_delay - 5;
                if (load_delay < 15) load_delay = 15;
                printf(outchar, "%3.0u",load_delay);
                }
        if(key == '#')
                {
                while(readkey()=='#');
                set_display_add(0,0);
                if(ld)
                        {
                        strcpy(text,"Switched load off?  ");
                        }
                else
                        {
                        strcpy(text,"Switched load on?   ");
                        }
                print_display(20,text);
                set_display_add(1,0);
                strcpy(text,"1 - confirm # - exit");
                print_display(20,text);
                while(1)
                        {
                        if(readkey()=='1')
                                {
                                while(readkey()=='1');
                                load_on=0;
                                set_display_add(1,0);
                                if(ld)
                                        {
                                        intcon.t0ie=0;
                                        load_switch=0;
                                        ld=0;
                                        load=0;
```

```
                                        strcpy(text,"Switched load off   ");
                                        }
                                else
                                        {
                                        intcon.t0ie=1;
                                        strcpy(text,"Switched load on    ");
                                        ld=1;
                                        }
                                print_display(20,text);
                                delay_ms(250);
                                delay_ms(250);
                                delay_ms(250);
                                delay_ms(250);
                                return;
                                }
                        if(readkey()=='#')
                                {
                                while(readkey()=='#');
                                return;
                                }
                        }
                }
        }
}

/*
*********************************
*Set the capacitor reference Voltage     *
*                                        *
*********************************
*/

#separate //prevent inline code making APF modes exceed segment
void set_capref()
{
char key;
int capvolt;
clear_display();
capvolt=capvoltscaler(vcapref);
printf(outchar, "Cap ref volt = %3.0u V",capvolt);
set_display_add(1,0);
strcpy(text,message);
print_display(19,text);
while(1)
        {
        while(readkey() == '\0');
        key=readkey();
        set_display_add(0,15);
        if(key == '1')
                {
```

```
                while(readkey()=='1');
                vcapref=vcapref+103;
                if (vcapref > 3074) vcapref=3074; //150V max
                capvolt=capvoltscaler(vcapref);
                printf(outchar, "%3.0u",capvolt);
                }
        if(key == '3')
                {
                while(readkey()=='3');
                vcapref=vcapref-103;
                if (vcapref < 1941) vcapref = 1941; //95 V min
                capvolt=capvoltscaler(vcapref);
                printf(outchar, "%3.0u",capvolt);
                }
        if(key=='#')
                {
                while(readkey()=='#');
                return;
                }
        }
}

/*
*****************************
* Measure the capacitor Voltage     *
*                                   *
*****************************
*/


void measure_cap_volt()
{
int capvolt;
long newvolt;
clear_display();
newvolt=0;
set_display_add(1,0);
strcpy(text,"press # to exit");
print_display(15,text);
while(1)
        {
        if (!APF_ON) //APF off - no edge interrupt
                {
                vcap=Vcap_ADC();
                }
        //system running - don't interfere with cap ADC
        if(vcap != newvolt)
                {
                capvolt=capvoltscaler(vcap);
                set_display_add(0,0);
```

```
                printf(outchar, "Cap voltage = %3.0u V",capvolt);
                newvolt = vcap;
                }
        if(readkey() == '#')
                {
                while(readkey() == '#');
                return;
                }
        }
}

/*
**********************
* Display the K value          *
*                              *
**********************
*/
void display_K()
{
long Knew;
Knew=0;
clear_display();
set_display_add(1,0);
strcpy(text,"press # to exit");
print_display(15,text);
while(1)
        {
        if(Kscaled != Knew)
                {
                Knew=Kscaled;
                set_display_add(0,0);
                Kscaler();
                printf(outchar,"K value = %0.4f",K);
                }
        if(readkey() == '#')
                {
                while(readkey() == '#');
                return;
                }
        }
}
/*
*****************************
* Display the bridge temperature      *
*                                     *
*****************************
*/
#separate //prevent inline code making APF modes exceed segment
void display_temp()
{
```

```
long bridgetemp,newtemp;
newtemp=0;
clear_display();
set_display_add(1,0);
strcpy(text,"press # to exit");
print_display(15,text);
while(1)
        {
        delay_us(25);
        adcon0.go_done = 1;
        while(adcon0.go_done);
        bridgetemp=adresh;
        bridgetemp = bridgetemp < 8;
        bridgetemp = bridgetemp + adresl;
//(binary eq of voltage - 305) +25 = value of temp
//1.49 V is 305 binary eq
//each degree change is 1 bit of the conversion
//i.e. 5mV/degree C
        bridgetemp=bridgetemp - 280;
        if(newtemp != bridgetemp)
                {
                set_display_add(0,0);
                printf(outchar,"Bridge temp = %3.0Lu",bridgetemp);
                newtemp = bridgetemp;
                }
        if(readkey() == '#')
                {
                while(readkey() == '#');
                return;
                }
        }
}
#separate //prevent inline code making APF modes exceed segment
void enter_RMS()
{
char key;
clear_display();
printf(outchar,"Source RMS = %2.0u",Vs);
set_display_add(1,0);
strcpy(text,message);
print_display(19,text);
while(1)
        {
        while(readkey() == '\0');
        key=readkey();
        set_display_add(0,13);
        if(key == '1')
                {
                while(readkey()=='1');
                Vs=Vs+1;
```

```
                if (Vs > 58) Vs=58; //58V max
                printf(outchar, "%2.0u",Vs);
                }
        if(key == '3')
                {
                while(readkey()=='3');
                Vs=Vs-1;
                if (Vs < 38) Vs = 38; //38 V min
                printf(outchar, "%2.0u",Vs);
                }
        if(key=='#')
                {
                while(readkey()=='#');
                return;
                }
        }
}
/*
************************************
*  This function converts a long   *
*  representing the cap voltage    *
*  to an int containing actual voltage *
************************************
*/
int capvoltscaler(long vcapbin)
{
int voltage;
vcapbin = vcapbin*20;
vcapbin = vcapbin/409;
voltage=vcapbin;
return voltage;
}

/*
*******************************
* A single character print function *
* for use with printf           *
*******************************
*/
void outchar(char c)
{
print_display(1,&c);
}
```

Appendix L: Matlab control algorithm switch_control5_53.m

This algorithm is used in conjunction with Matlab model apf3.mdl (given in Appendix C) but containing slight modifications as described in section 5.6.1. The system incorporates proportional hysterisis switching and energy compensation control for direct comparison with the results of the practical demonstration system.

```
function [y]=switch_control5_53V(u)
%53V version
%Control function for 53VRMS APF

%Although the 3/2 H-Bridge is used in the simulation, switches s3a and s1a
%have no effect since they are set to zero and the "fast" inductor has been disconnected

%The simulation is for comparison with practical results
%The switching incorporates both energy compensation and also a proportional hysterisis
%boundary i.e. that is proportional to Ifref
%Constants and initial value defaults
C=470e-6;
fast_inductor=0;
pos=0;
neg=0;
%Sample time T, epsilon and Vcapconst must be set in the workspace

%Input variable assignment
Vref=u(1);
Is=u(2);
Vc_old=u(3);
Vc_new=u(4);
flag=u(5);
DIf=u(7);
%sw's take on old values (from last sample period)
s4=u(8);
s3=u(9);
s2=u(10);
s1=u(11);
x=u(12);
xdot=u(13);
s1a=u(14);
s3a=u(15);
DIfref=u(16);
Vcaprefnew=u(17);
Vcapconst=u(18);
flag1=u(19);
Ifref=u(20);
If=u(21);
epsilon=u(22);

%Note that Vcaprefnew is not used in this simulation. Sliding mode not
%used.

%Claculate hysterisis bound for double real roots in the z-plane:
g=4*epsilon/(epsilon+1)^2;
rho=2*(1-g);
```

```
%Check flag: 1 cycle start up hold-off
if(~flag)
   Kold=0.01; %initial value of conductance
else
   Kold=u(6);
end

Vd=Vc_new-Vc_old;

if(flag)
   E=0.5*C*Vd*(Vc_old + Vc_new);
   Ecomp=0;
   Vcaperror=abs(Vcapconst-Vc_new);
   if(Vcaperror > 1.5)    %Value used in test rig software
      Ecomp = 0.5*C*(Vc_new^2 - Vcapconst^2); %energy difference
            %    corresponding to current cap voltage relative to
            %    Vcapconst
            % Only make the correction if capacitor has drifted more
            % than 1.5V
    end

   Knew=Kold-(E+(epsilon*Ecomp))/56.18;    %56.18=53*53*0.02
   if(Knew < 0)
      Knew = 0;       %Prevent phase reversal of Isref when capacitor voltage has large
                  %positve increments
   end

else
  Knew=Kold;
end

Isref=Knew*Vref;

check_sw=~(s1|s2|s3|s4); %check_sw is 1 only if all sw's are 0 i.e. end of a passive phase

if(Vref > 0.1)
   pos=1; %corresponding to Alpha = 1
end

if(Vref < 0.1)
   neg=1; %corresponding to Alpha = -1
end

%S here is the switching condition
S=xdot; %default S value

S=C*S; %compensate for external 1/C factor
%Now that hysterisis is used the true error must be used.
%The C factor was incorporated only to correctly dimension the Sliding
%space

% The following four variables are active phase indicators
pos_del_inc=0; %reset positive supply, power delivered to source, increasing
pos_abs_inc=0; %reset positive supply, power absorbed from source, increasing
neg_del_inc=0; %reset negative supply, power delivered to source, increasing
neg_abs_inc=0; %reset negative supply, power absorbed from source, increasing

%Use the previous sample switch states (from switch sampler) to assign
%values to the active phase indicators.
if(s1&&s4&&~s2&&~s3)
```

```
    pos_del_inc=1;
end

if(s3&&~s1&&~s2&&~s4)
    pos_abs_inc=1;
end

if(s3&&s2&&~s1&&~s4)
    neg_del_inc=1;
end

if(s1&&~s2&&~s3&&~s4)
    neg_abs_inc=1;
end

%now reset all sw's
s1=0;
s2=0;
s3=0;
s4=0;

Ifref_gate=0; %default value - not required in this simulation since sliding mode not used

%The next section checks the system state against the switching condition and
%decides if the next state should be active and then sets the switches
%accordingly.

    %Supply voltage positive (Alpha = 1)
    if(pos)
        if(((S < rho*Ifref)||((S < 0)&&pos_del_inc))&&(Ifref < 0))

            % delivered increasing
            s1=1;
            s4=1;
        end

        if(((S > rho*Ifref)||((S > 0)&&pos_abs_inc))&&(Ifref > 0))

            % Absorbed increasing
            s3=1;
        end
    end

    %Supply voltage negative (Alpha = -1)
    if(neg)
        if(((S > rho*Ifref)||((S > 0)&&neg_del_inc))&&(Ifref > 0))

            % delivered increasing
            s3=1;
            s2=1;
        end

        if(S < 0)
            if(((S < rho*Ifref)||((S < 0)&&neg_abs_inc))&&(Ifref < 0))
                % absorbed increasing
                s1=1;
            end
        end
    end
%At this point, if all switches are zero then the next phase will be
```

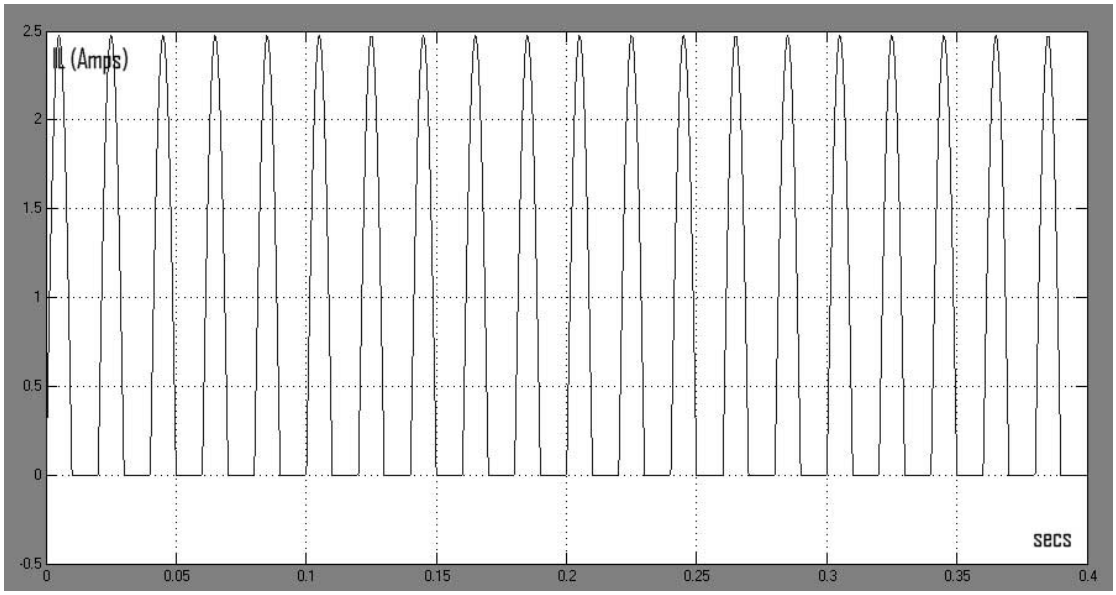
```
%passive.

%Only a basic bridge used in the practical work. No additional bridge arm required:
s1a=0;
s3a=0;

%override switch control for first sample period of T to allow bridge to
%initialise
if(~flag1)
    s1=0;
    s2=0;
    s3=0;
    s4=0;
end

%Update all output variables
y(1)=s1;
y(2)=s2;
y(3)=s3;
y(4)=s4;
y(5)=Knew;
y(6)=Isref;
y(7)=s1a;
y(8)=s3a;
y(9) = Ifref_gate;
y(10)=S;
```

Appendix M: simulation results using discrete proportional hysterisis switching and energy compensation

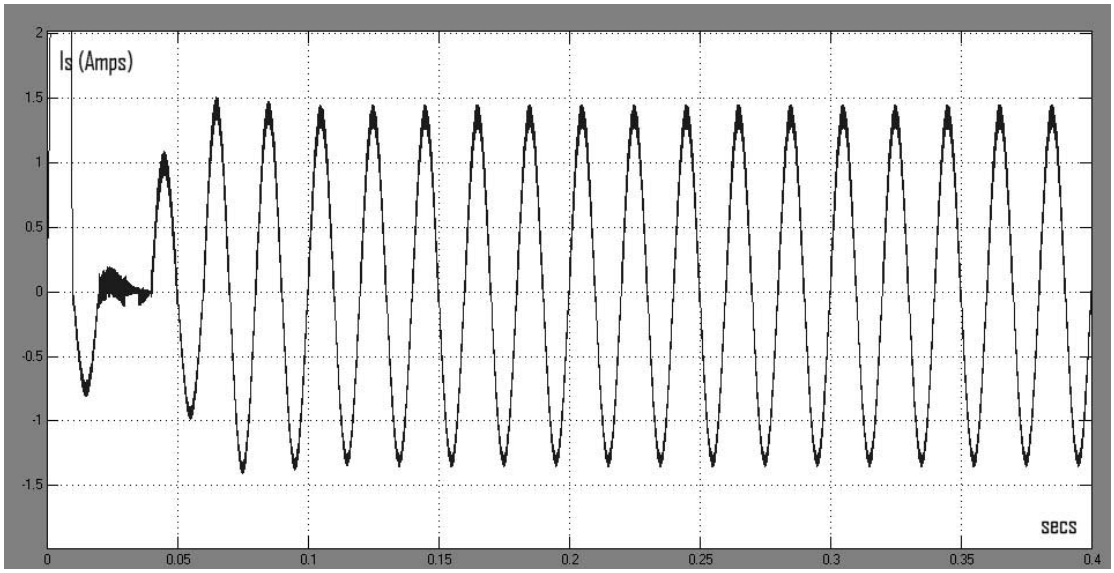
Appendix M: Constant 30 Ohm half wave rectified load $\varepsilon = 0.9$

The following system parameters are used:

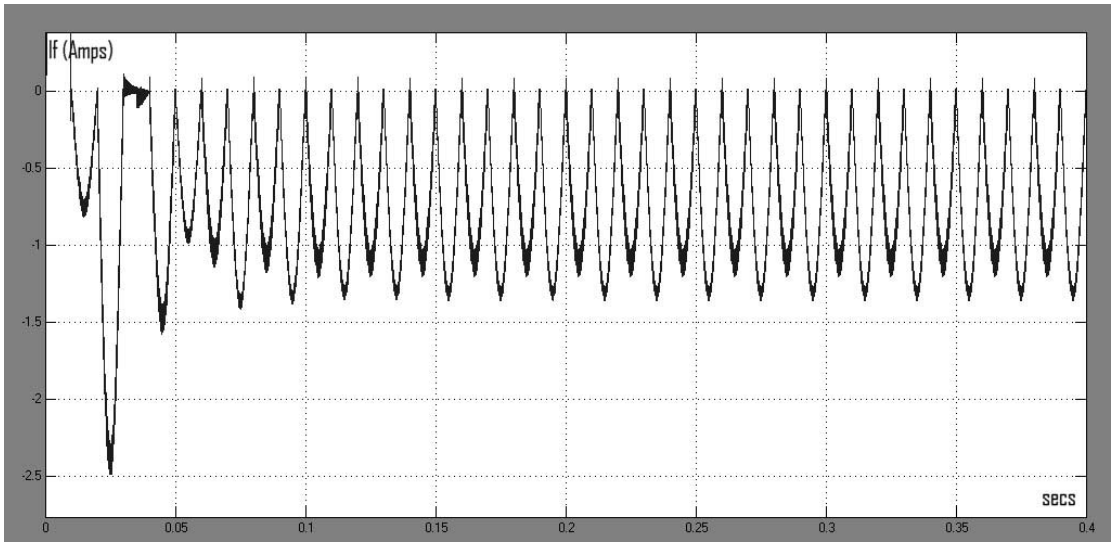
T = 20µs
Vs = 53V RMS
Simulation time = 400ms
Vcapconst = 100V
Epsilon = 0.9
Half wave constant load of 30 Ohm



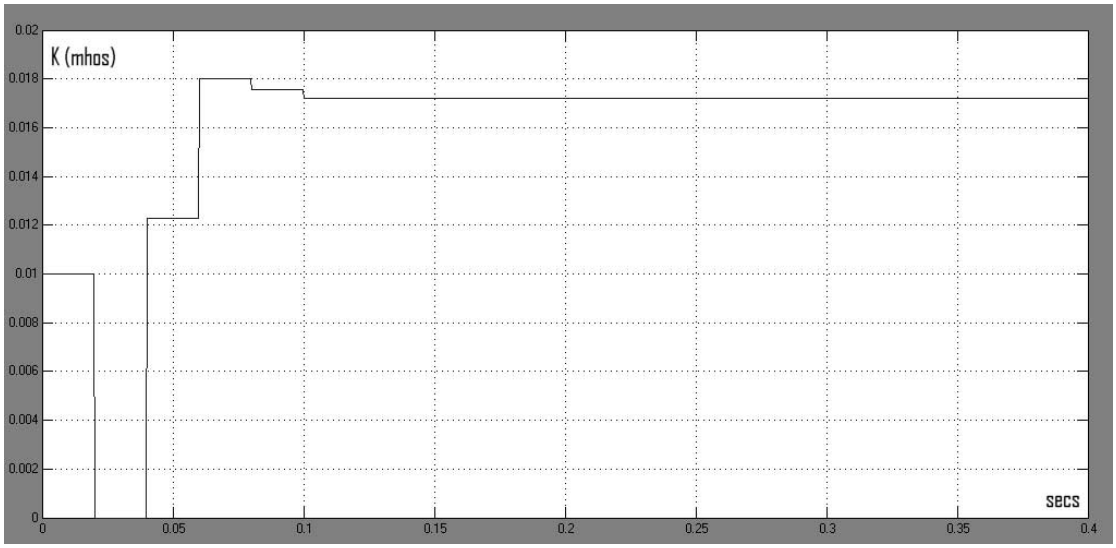
Load current IL



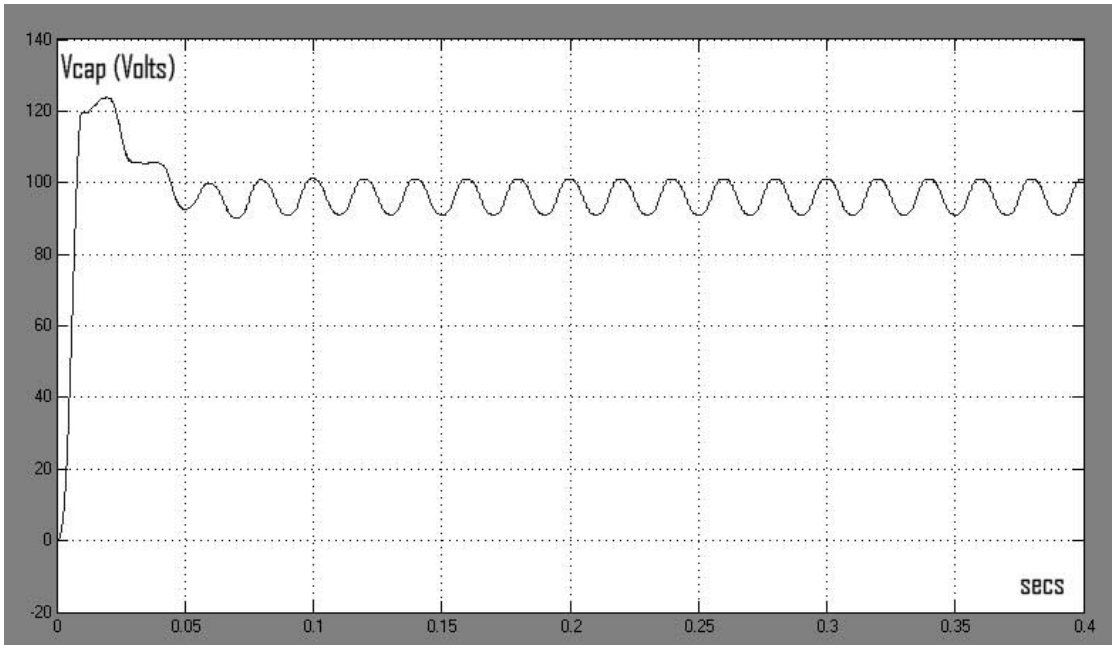
Source current Is



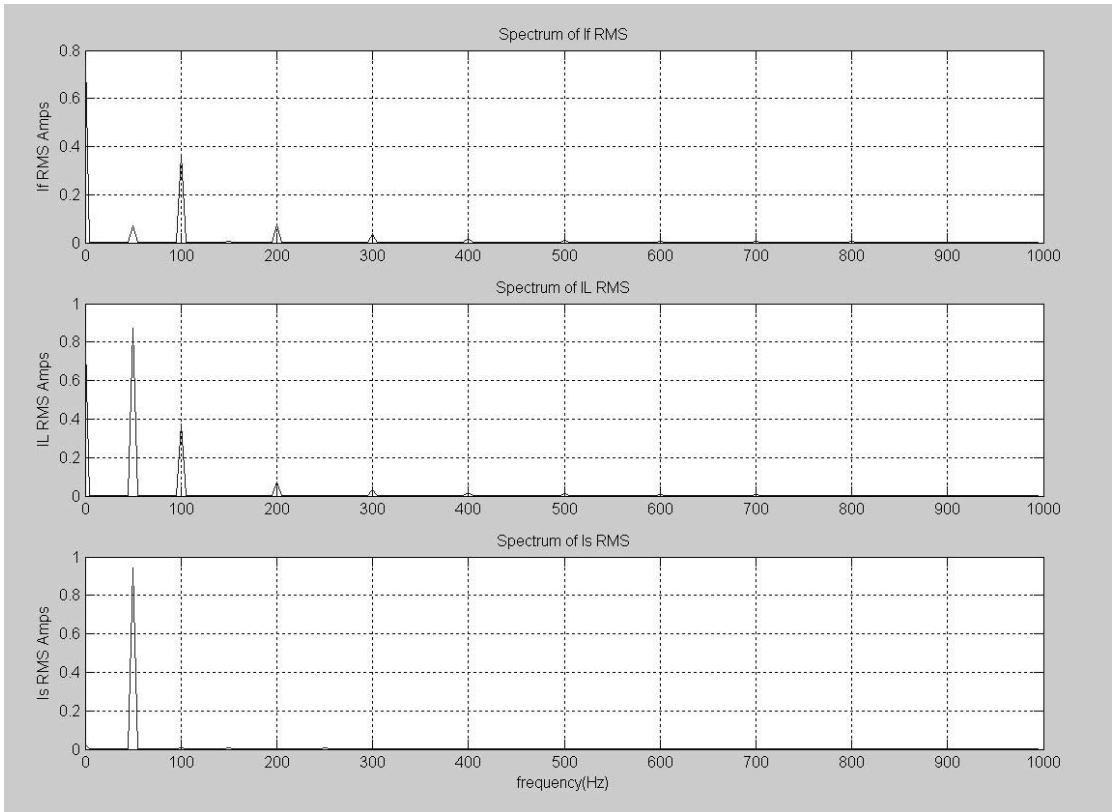
APF current If



Conductance K



Capacitor Voltage (Vcap)

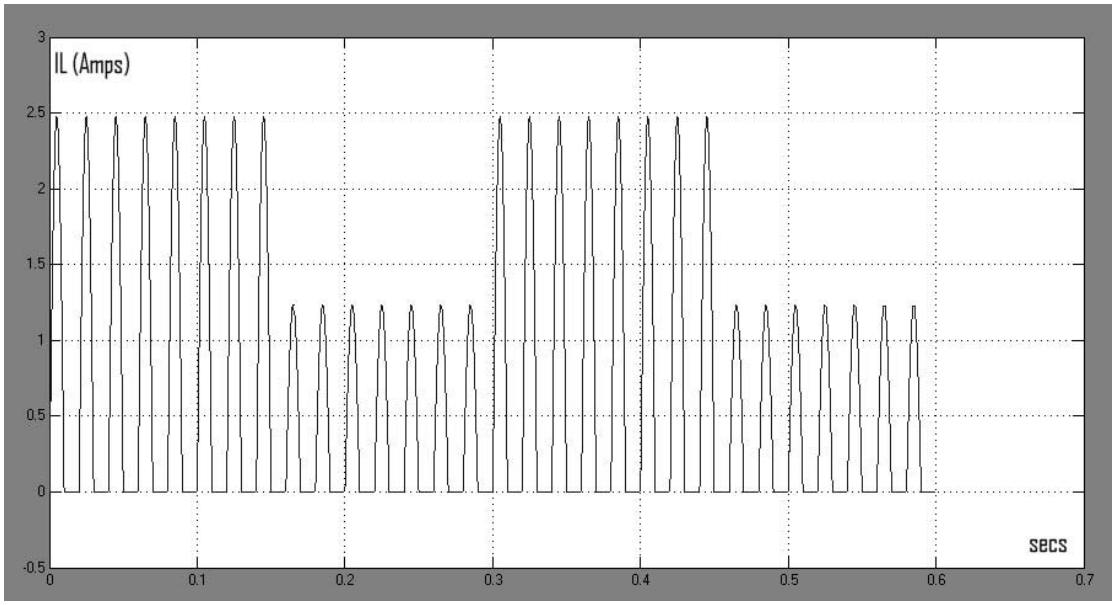


Frequency plot for If, IL and Is (Amps RMS)

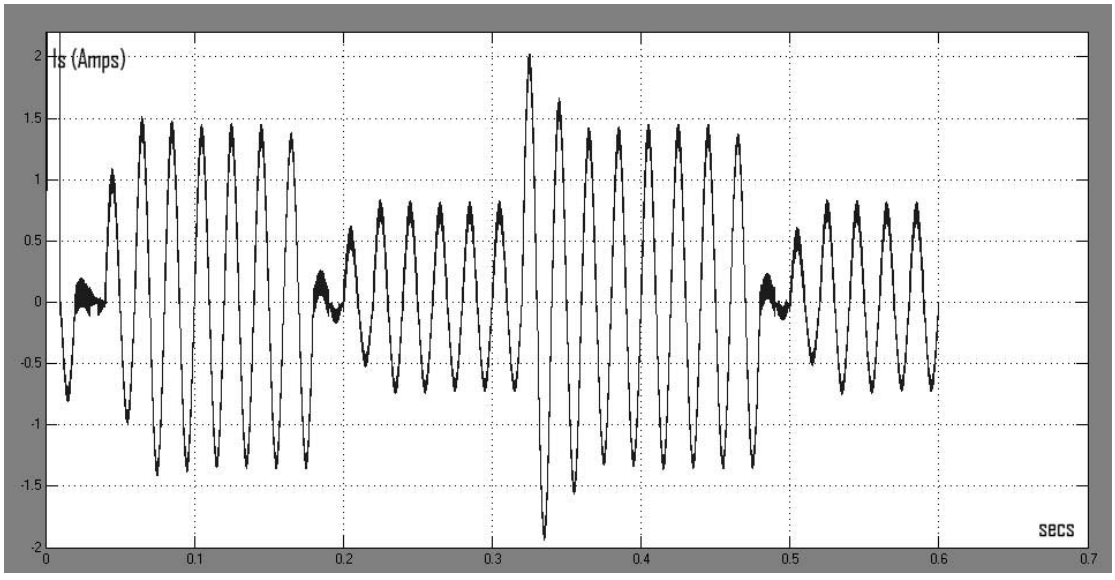
Appendix M: Switched half-wave resistive load $\varepsilon = 0.9$

The following system parameters are used:

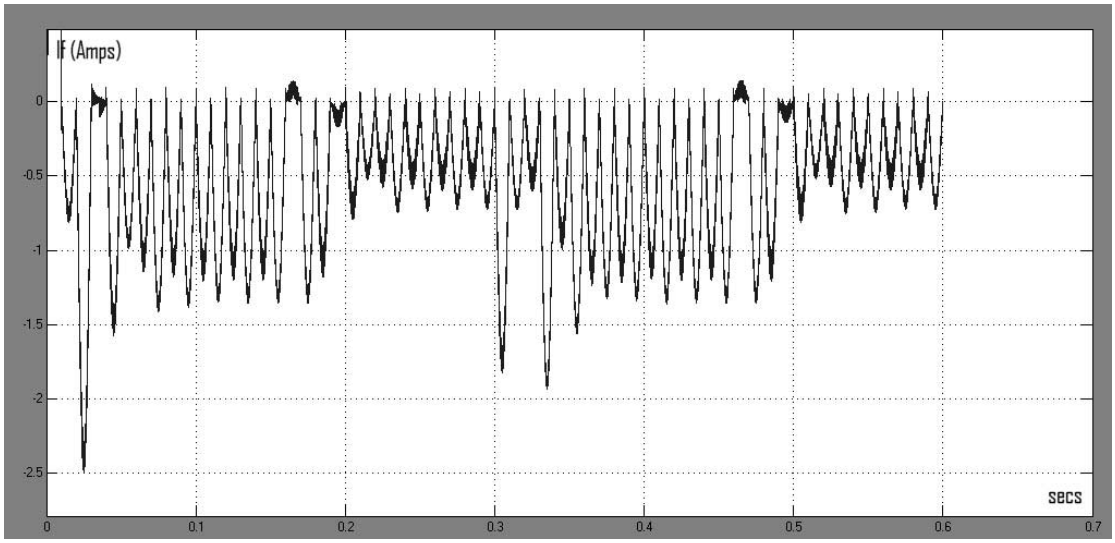
T = 20µs
Vs = 53V RMS
Simulation time = 600ms
Vcapconst = 100V
Epsilon = 0.9
Half wave load periodically switched to 30 Ohm for 150ms then switched to 60 Ohm for 150ms



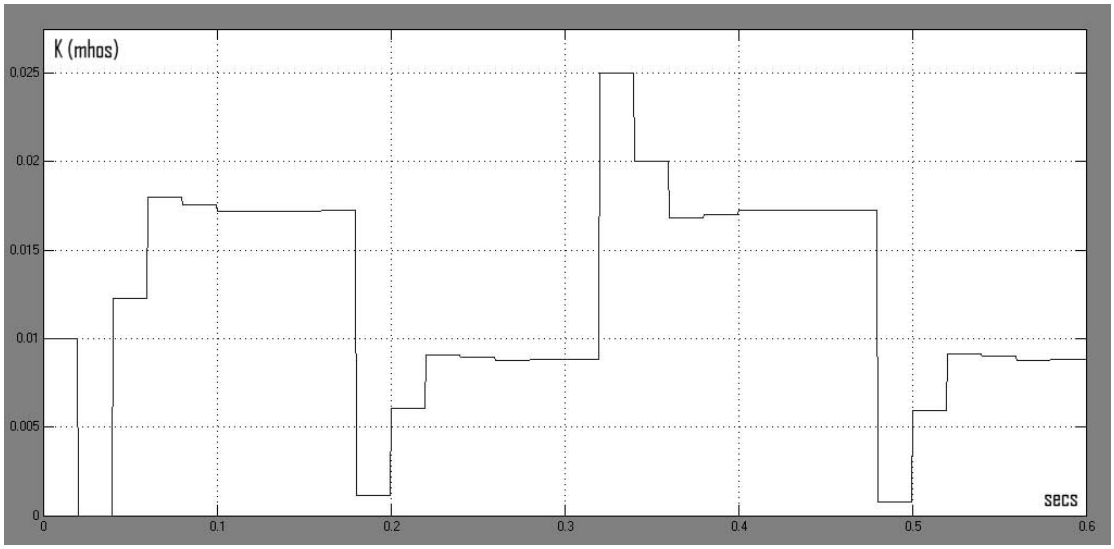
Load current IL



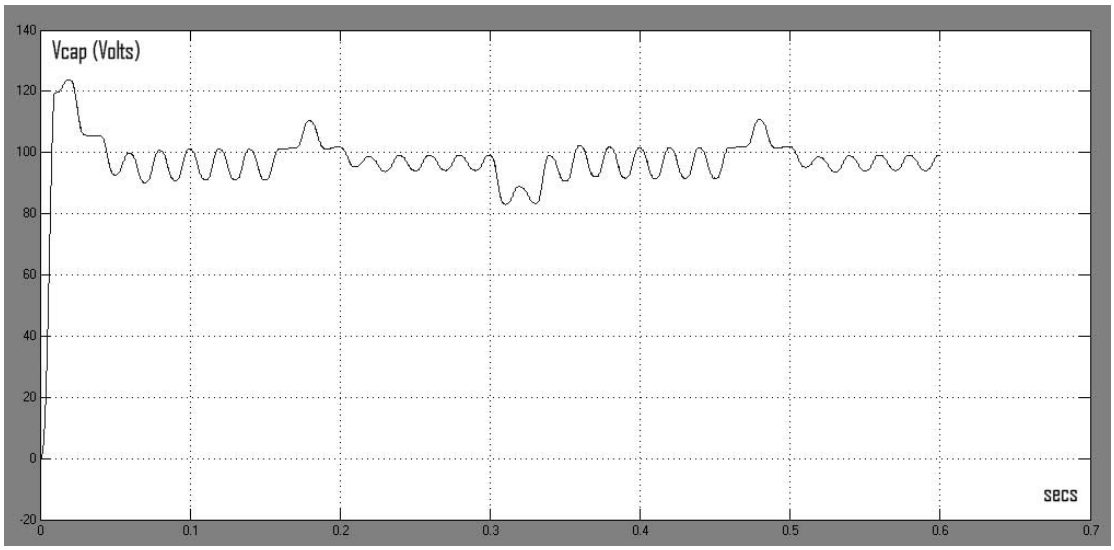
Source current Is



APF current If



Conductance K

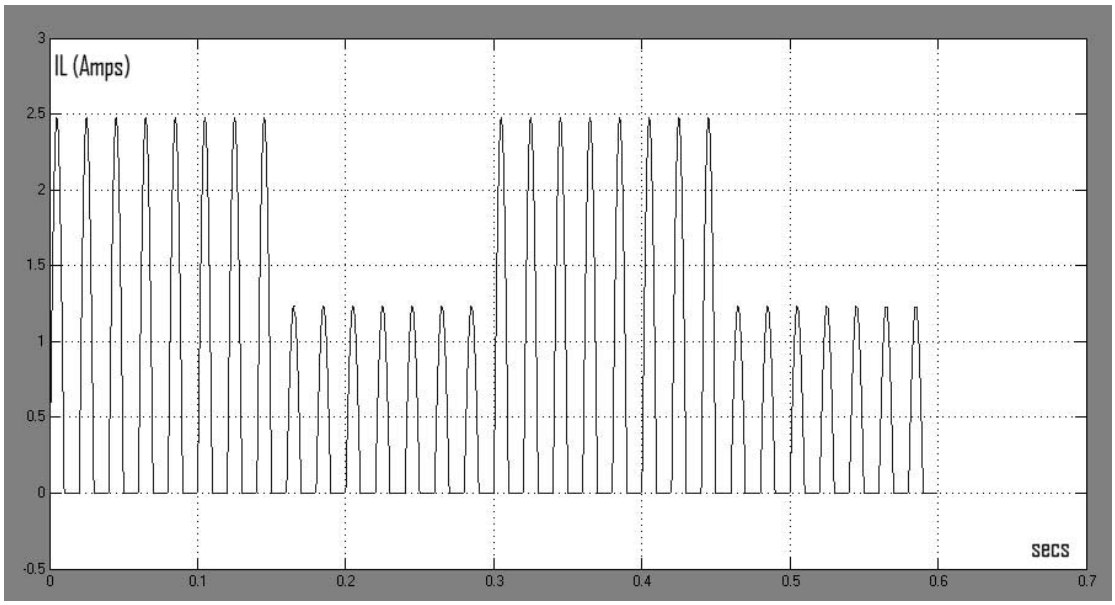


Capacitor Voltage (Vcap)

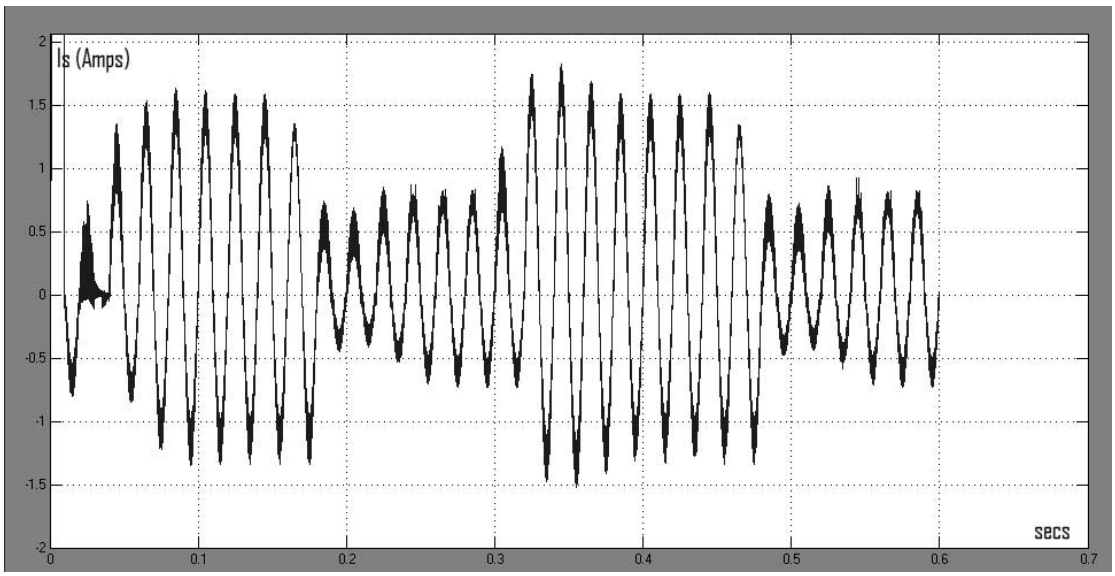
Appendix M: Switched half-wave resistive load ε = 0.5

The following system parameters are used:

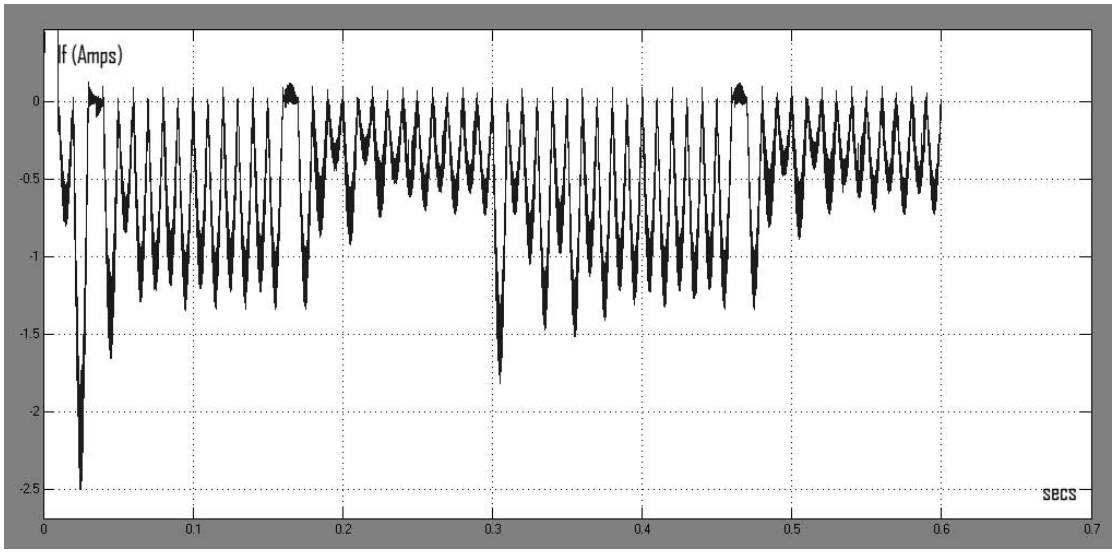
T = 20µs
Vs = 53V RMS
Simulation time = 600ms
Vcapconst = 100V
Epsilon = 0.5
Half wave load periodically switched to 30 Ohm for 150ms then switched to 60 Ohm for 150ms



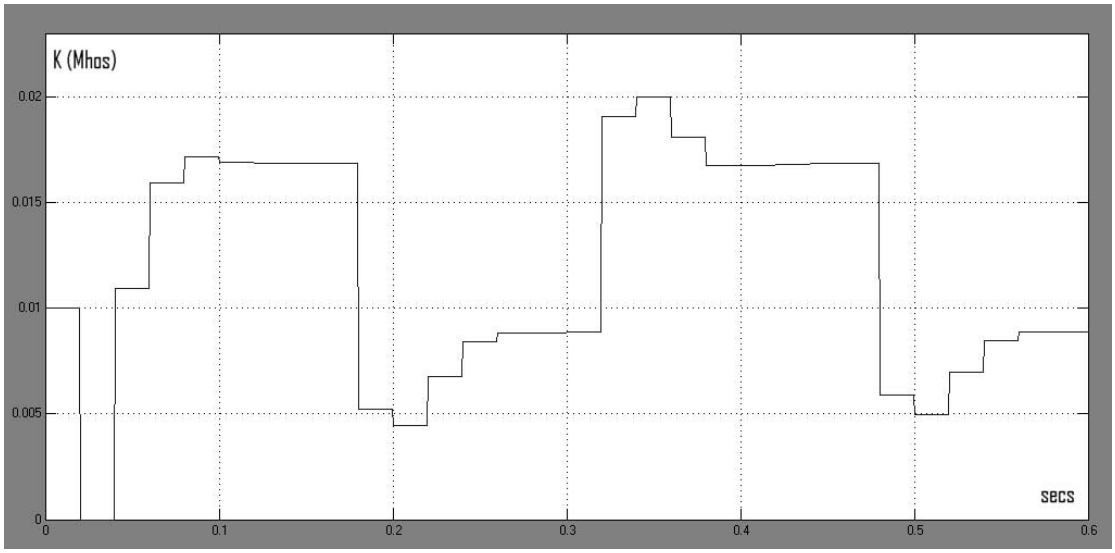
Load current IL



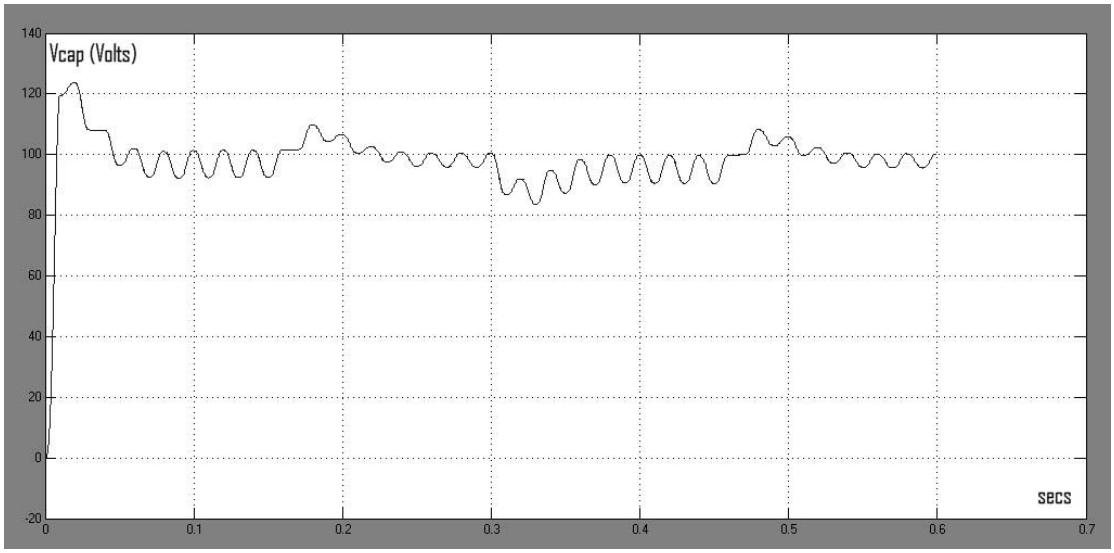
Source current Is



APF current If



Conductance K

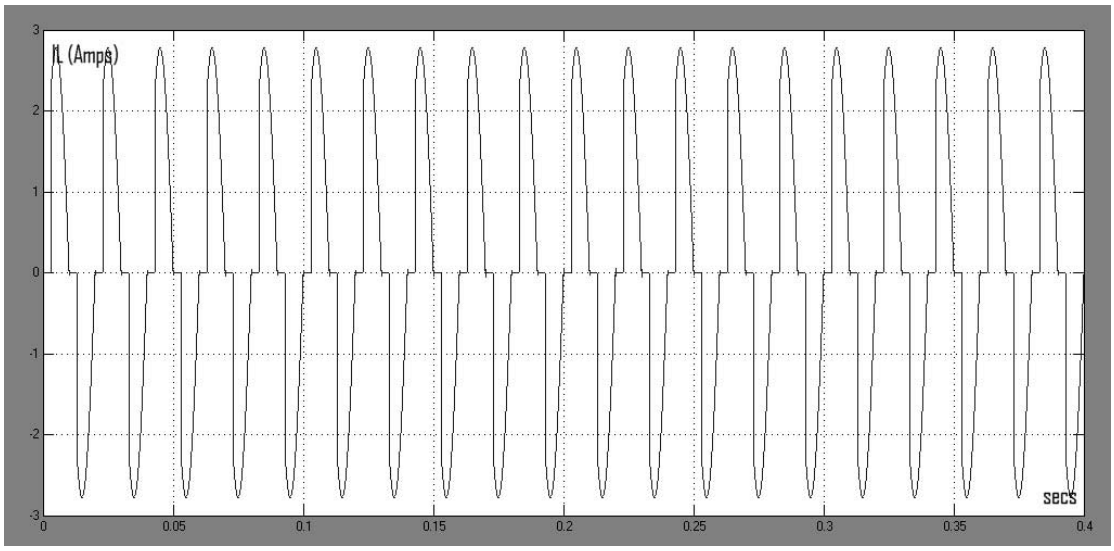


Capacitor Voltage (Vcap)

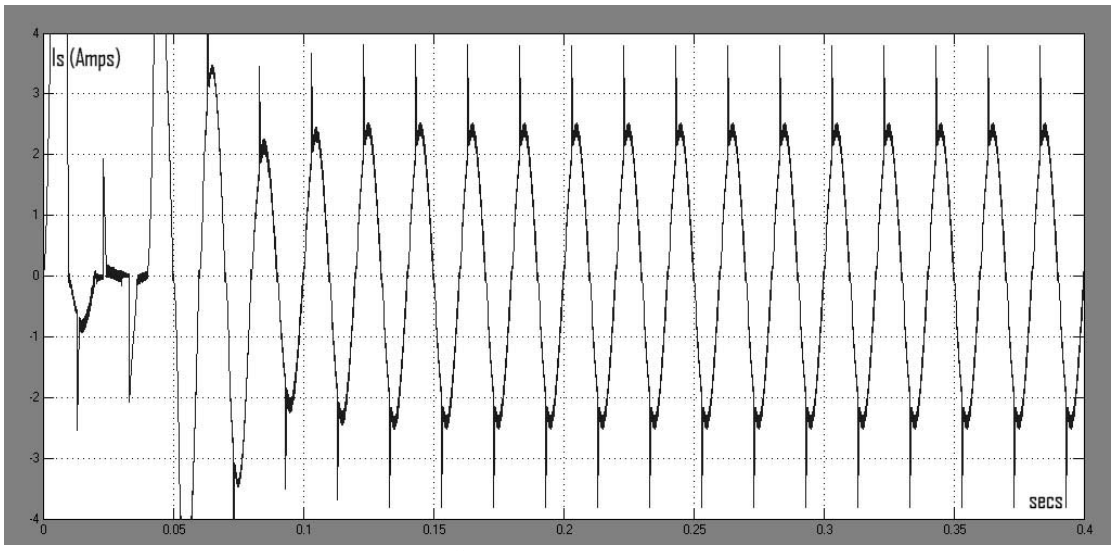
Appendix M: Phase controlled load ε = 0.9

The following system parameters are used:

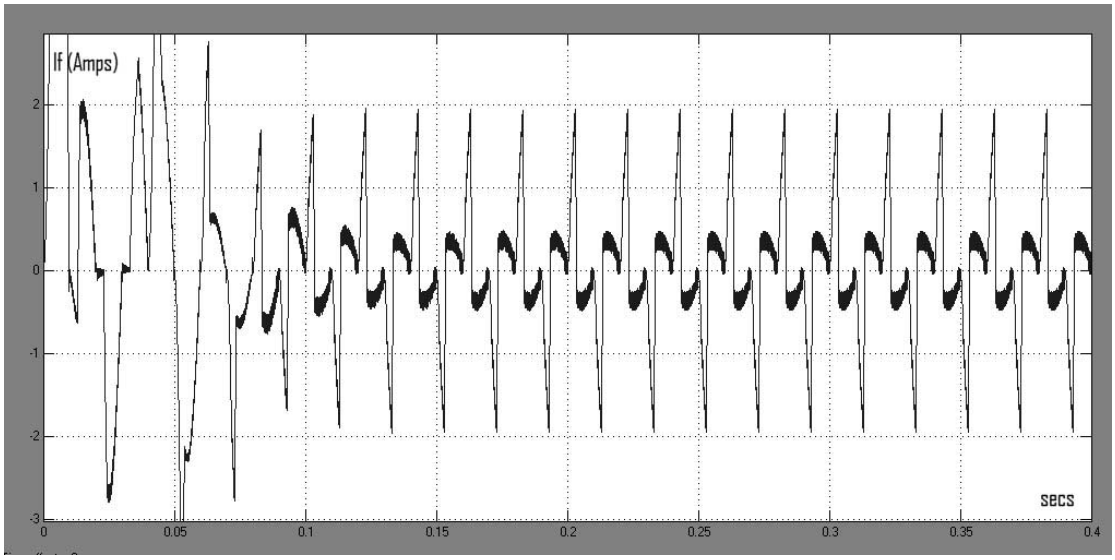
T = 20µs
Vs = 53V RMS
Simulation time = 400ms
Vcapconst = 130V
Epsilon = 0.9
Phase controlled resistive load of 27 Ohm.
Triac firing point set to 30% of a half period corresponding to a firing angle of 54 deg and 234 deg.



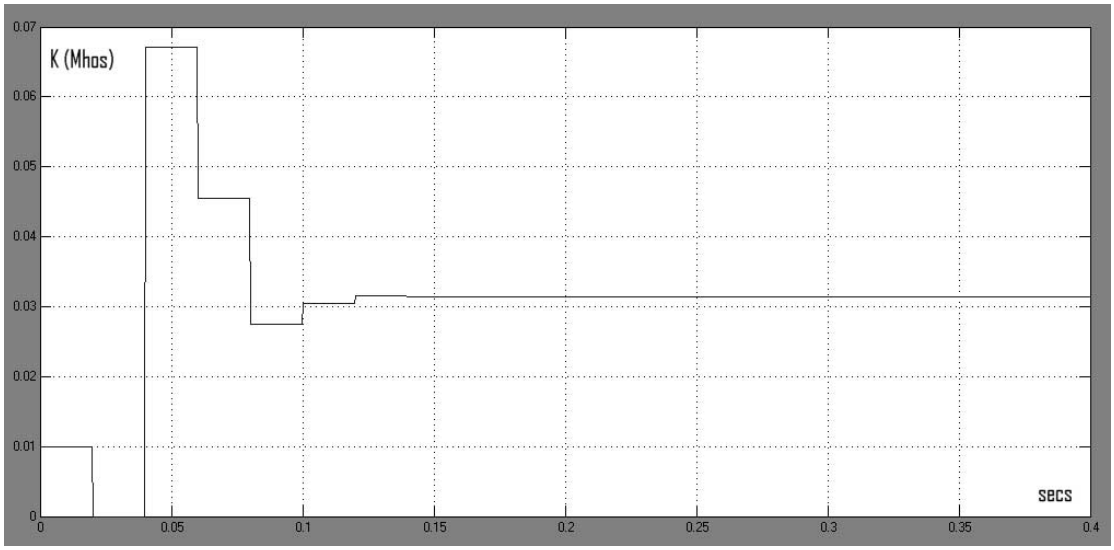
Load current IL



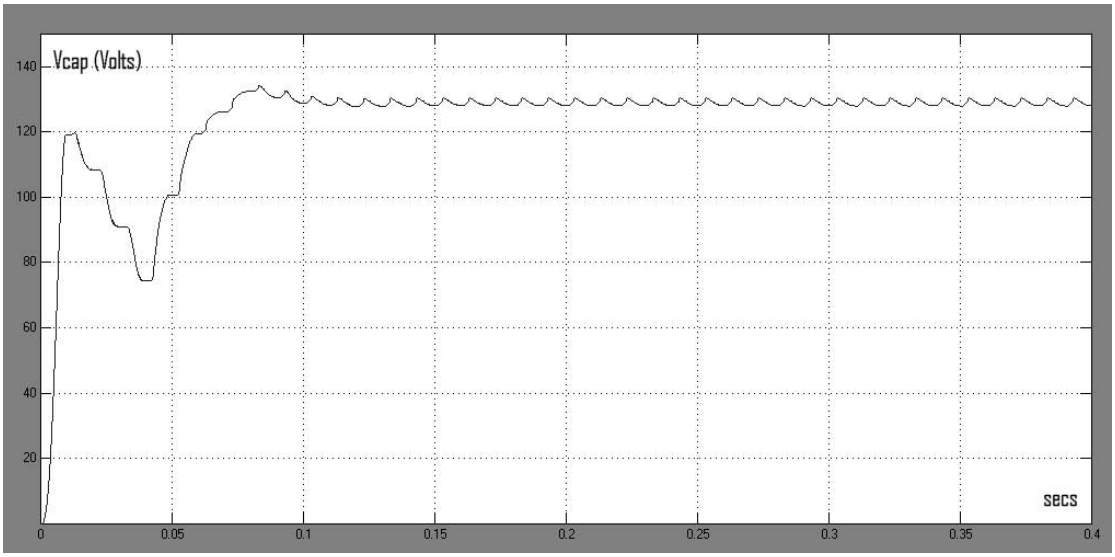
Source current Is



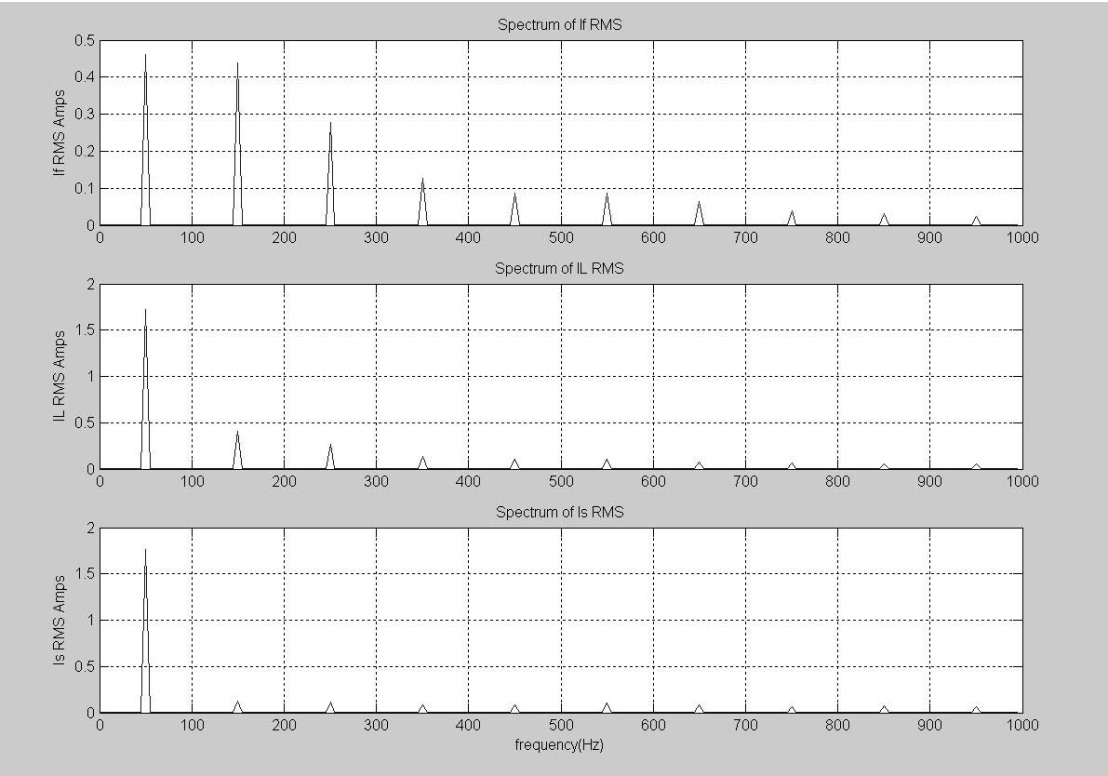
APF current If



Conductance K



Capacitor Voltage Vcap



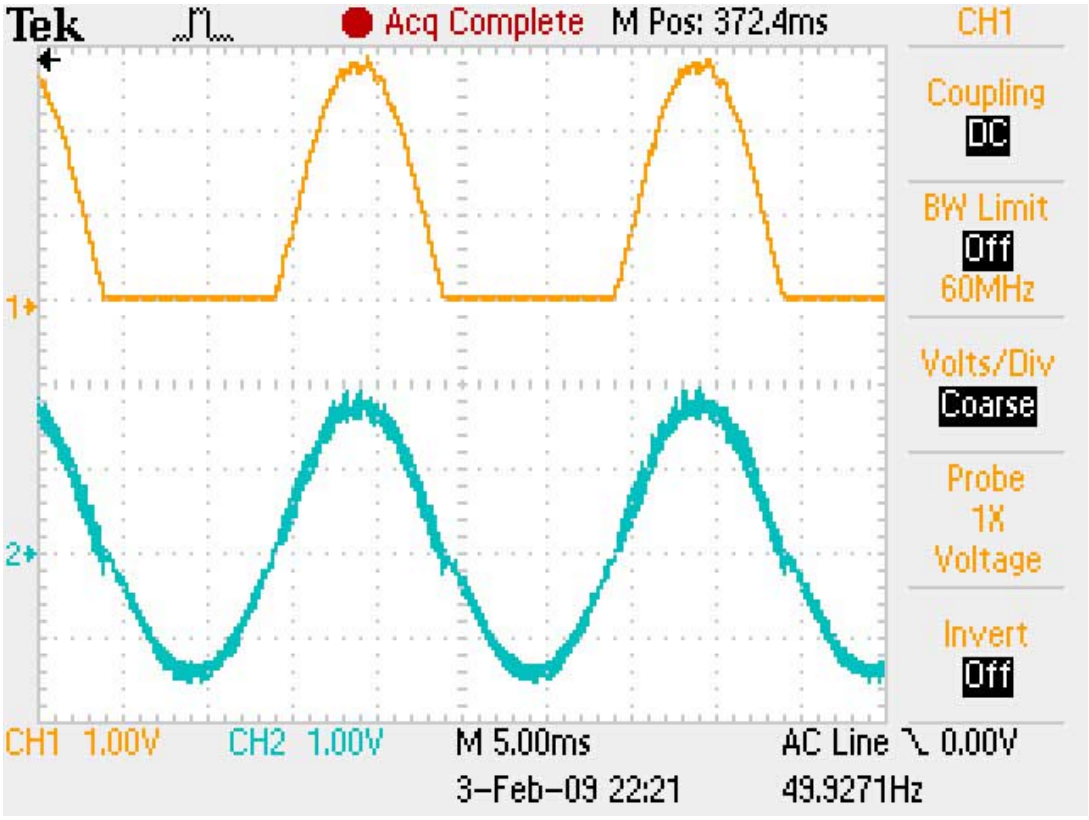
Frequency plot for If, IL, Is (Amps RMS)

Appendix N: practical results from demonstration test system using discrete proportional hysterisis switching and energy compensation

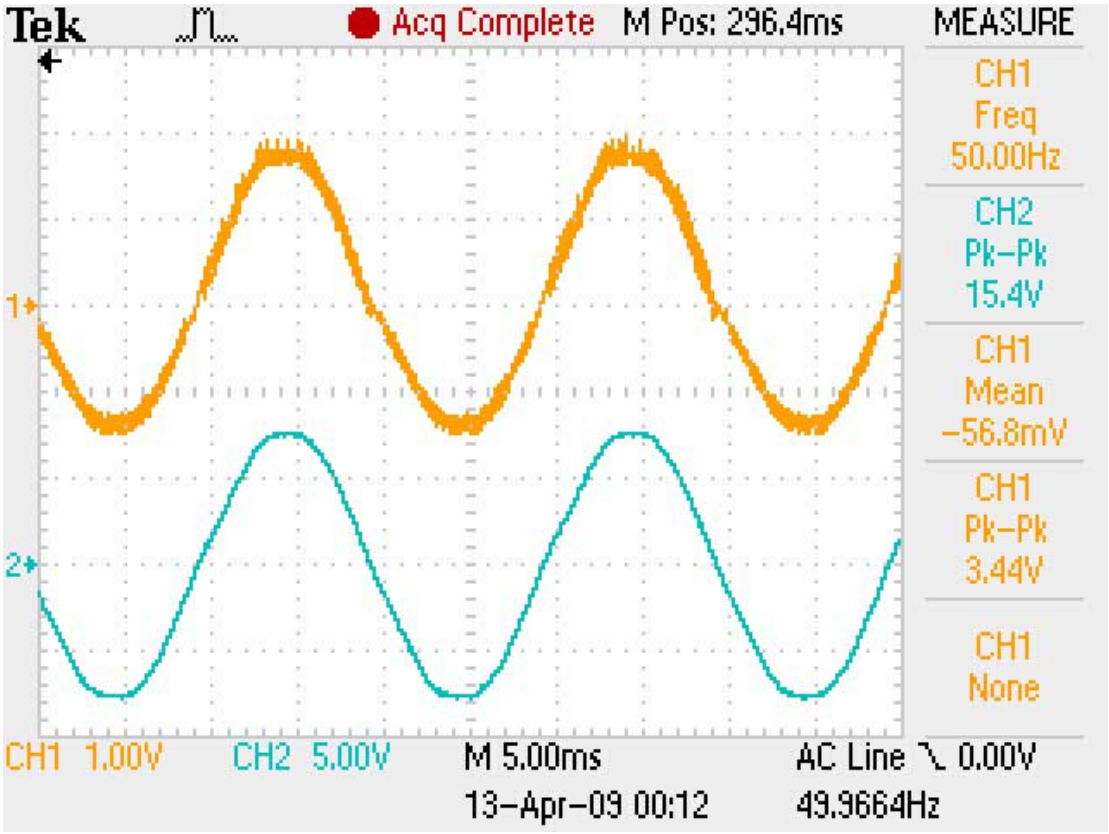
Appendix N: Constant 30 Ohm half wave rectified load $\varepsilon = 0.9$

The following system parameters are used:

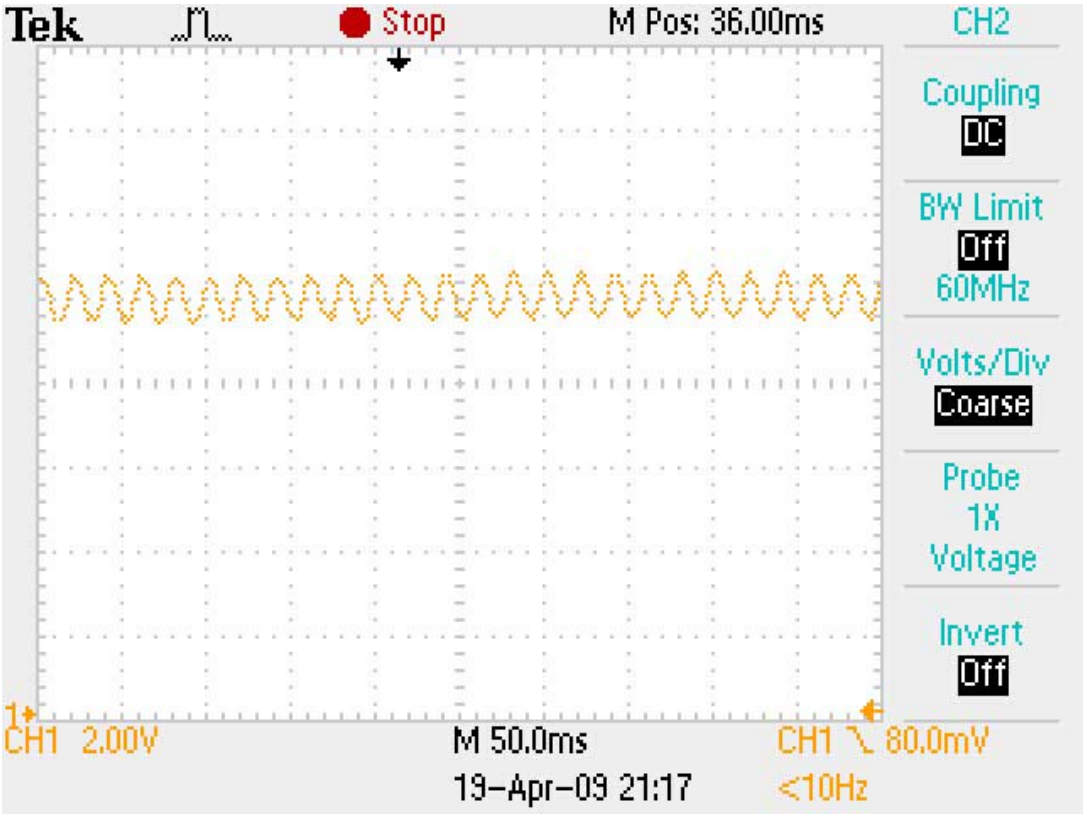
T = 20µs
Vs = 53V RMS
Vcapconst = 99V
Epsilon = 0.9
Half wave constant load of 30 Ohm



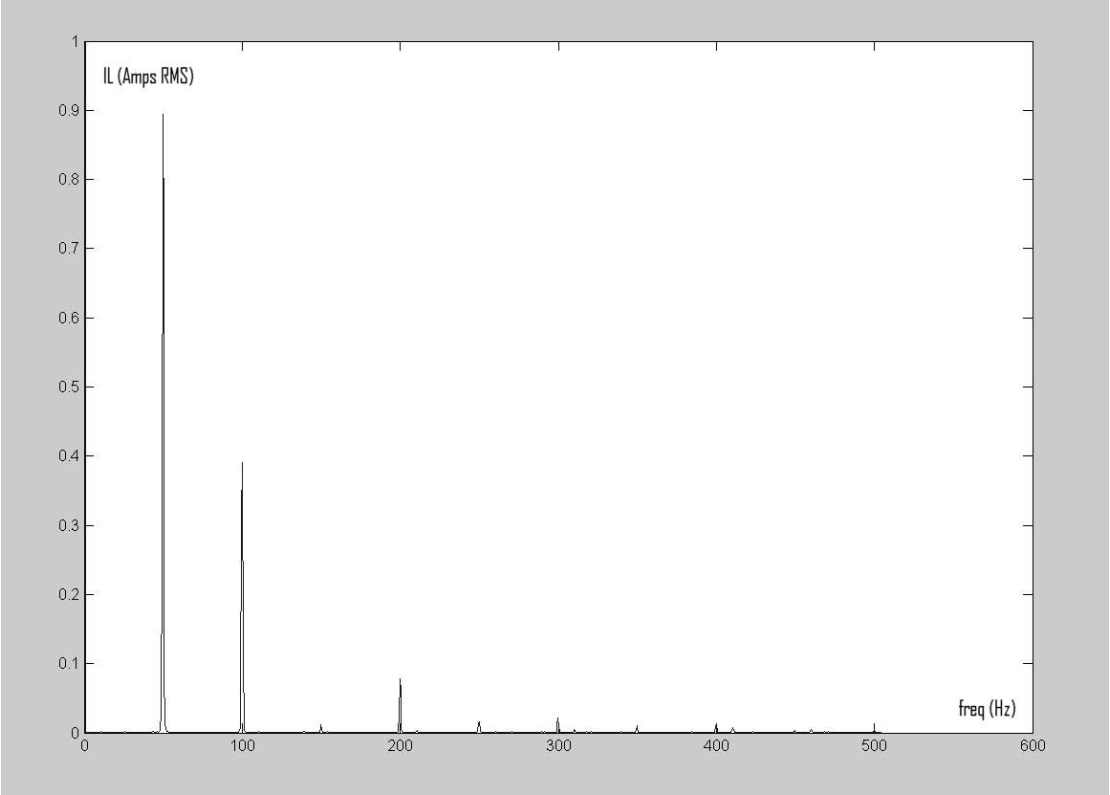
Scope trace with IL on Ch1 and Is on Ch2



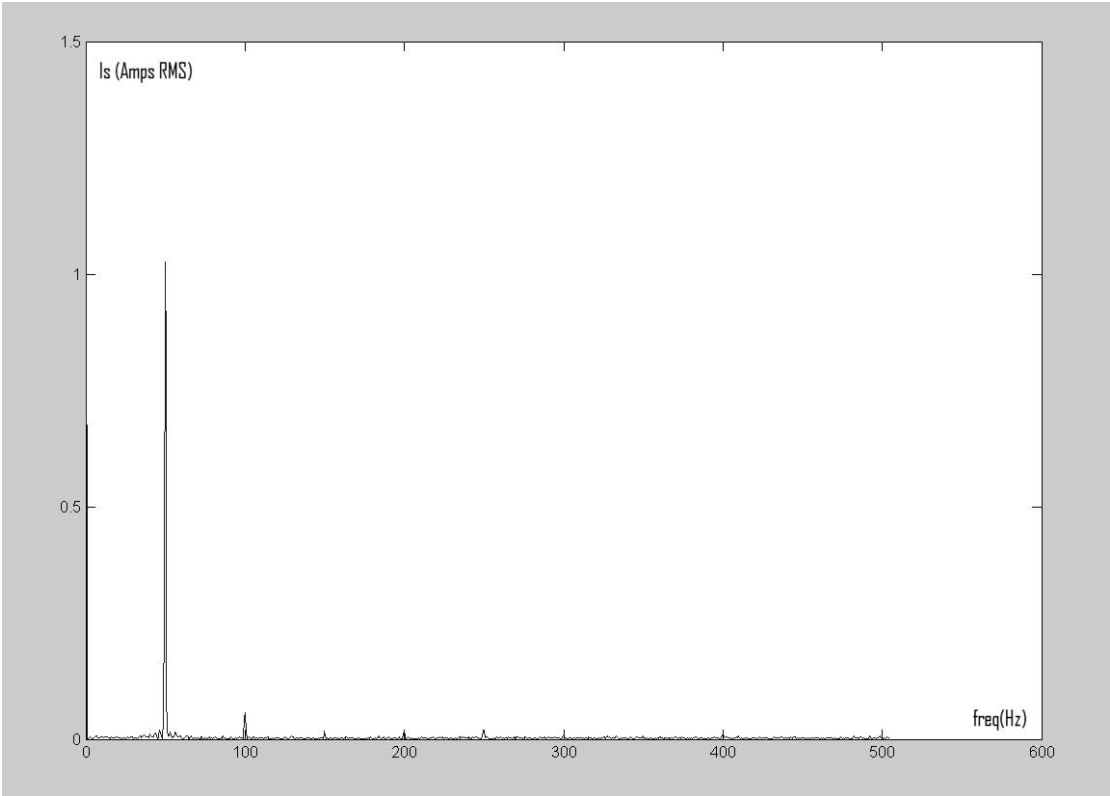
Scope trace showing Is on Ch1 (1A/div) and Vs on Ch2 (50V/div)



Scope trace showing capacitor Voltage (20V/div) averaging around 100V



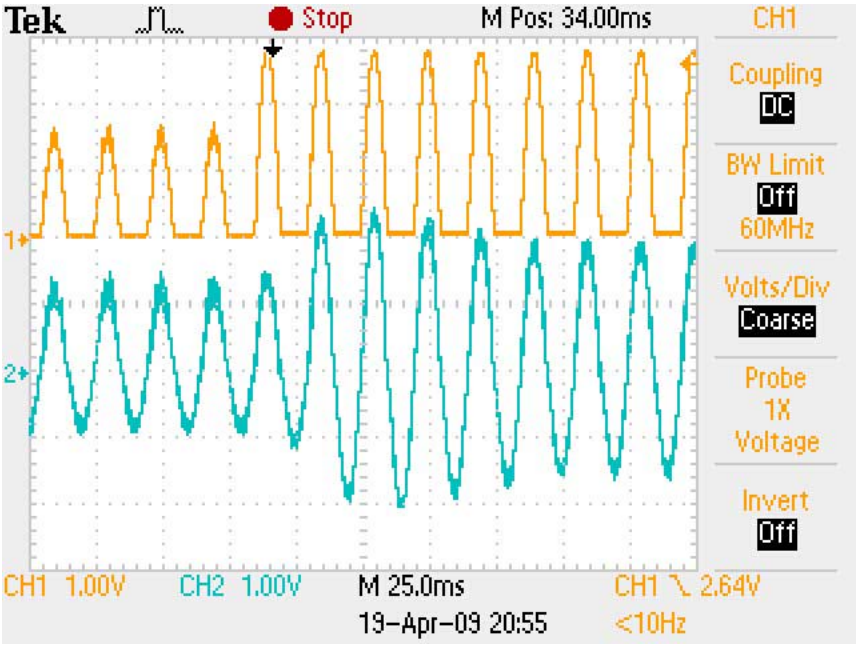
Frequency spectrum plot for IL (Amps RMS)



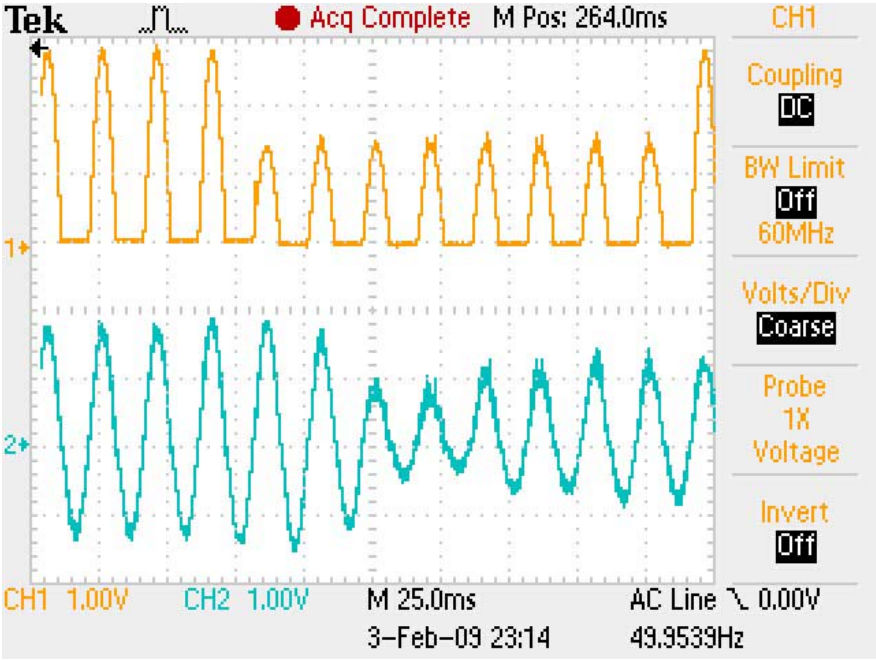
Frequency Spectrum plot for Is (Amps RMS)

Appendix N: Switched half-wave resistive load ε = 0.9

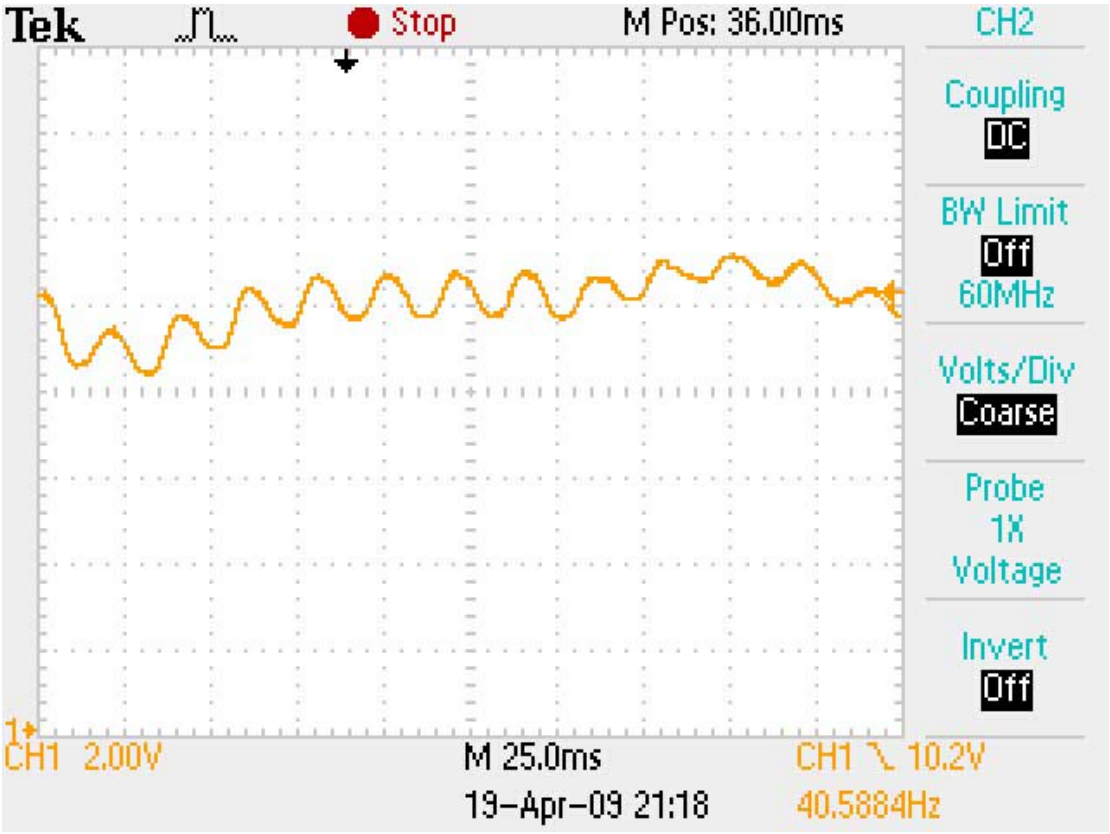
The following system parameters are used:
T = 20µs
Vs = 53V RMS
Vcapconst = 99V
Epsilon = 0.9
Half wave load periodically switched to 30 Ohm for 150ms then switched to 60 Ohm for 150ms



Scope trace showing increasing step transient with IL on Ch1(1A/div) and Is on Ch2(1A/div)



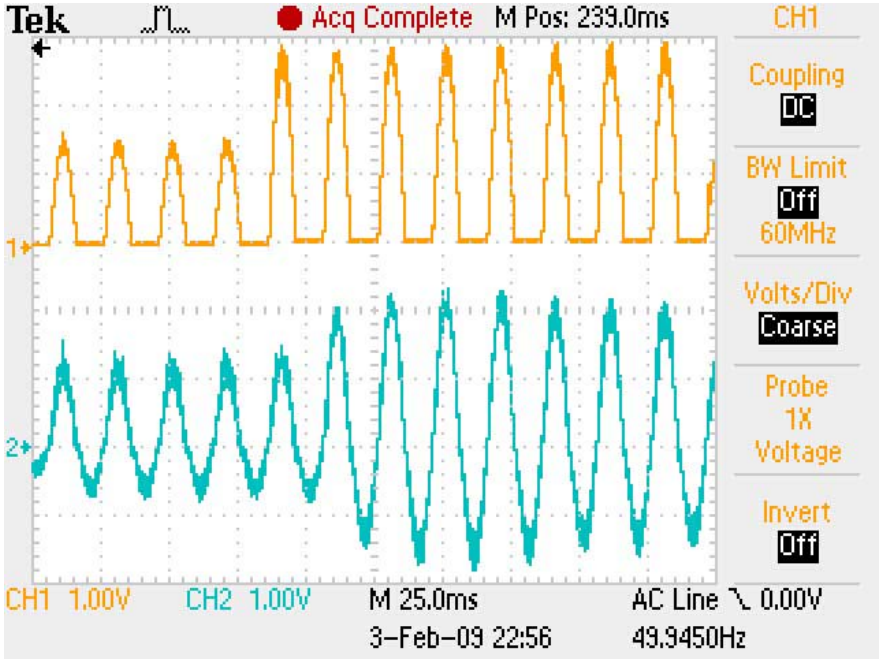
Scope trace showing reducing step transient with IL on Ch1(1A/div) and Is on Ch2(1A/div)



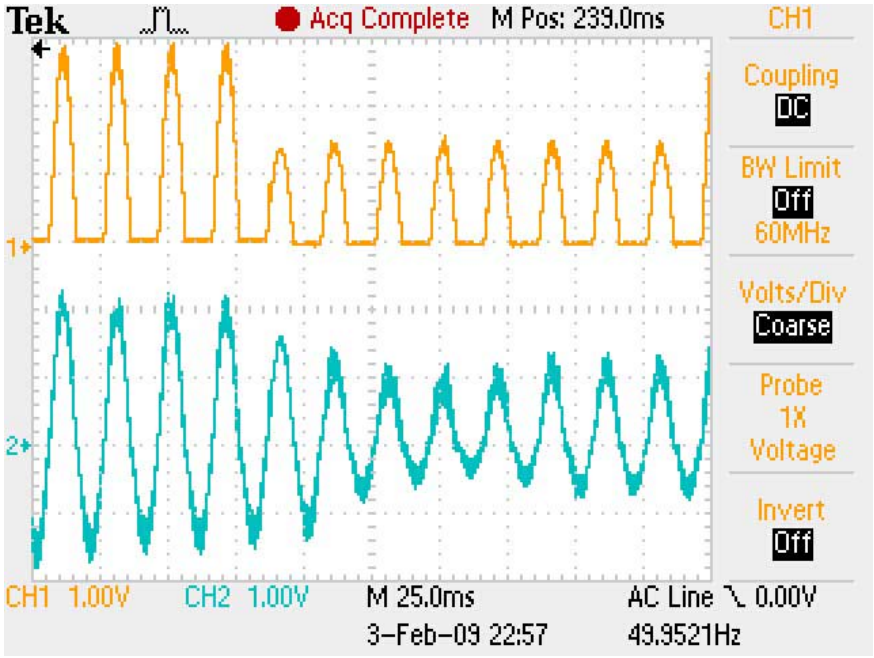
Scope trace showing capacitor Voltage (20V/div) averaging around 100V with deviations occurring as the load changes (switching period 200ms)

Appendix N: Switched half-wave resistive load ε = 0.5

The following system parameters are used:
T = 20µs
Vs = 53V RMS
Vcapconst = 99V
Epsilon = 0.5
Half wave load periodically switched to 30 Ohm for 150ms then switched to 60 Ohm for 150ms



Scope trace showing increasing step transient with IL on Ch1(1A/div) and Is on Ch2(1A/div)

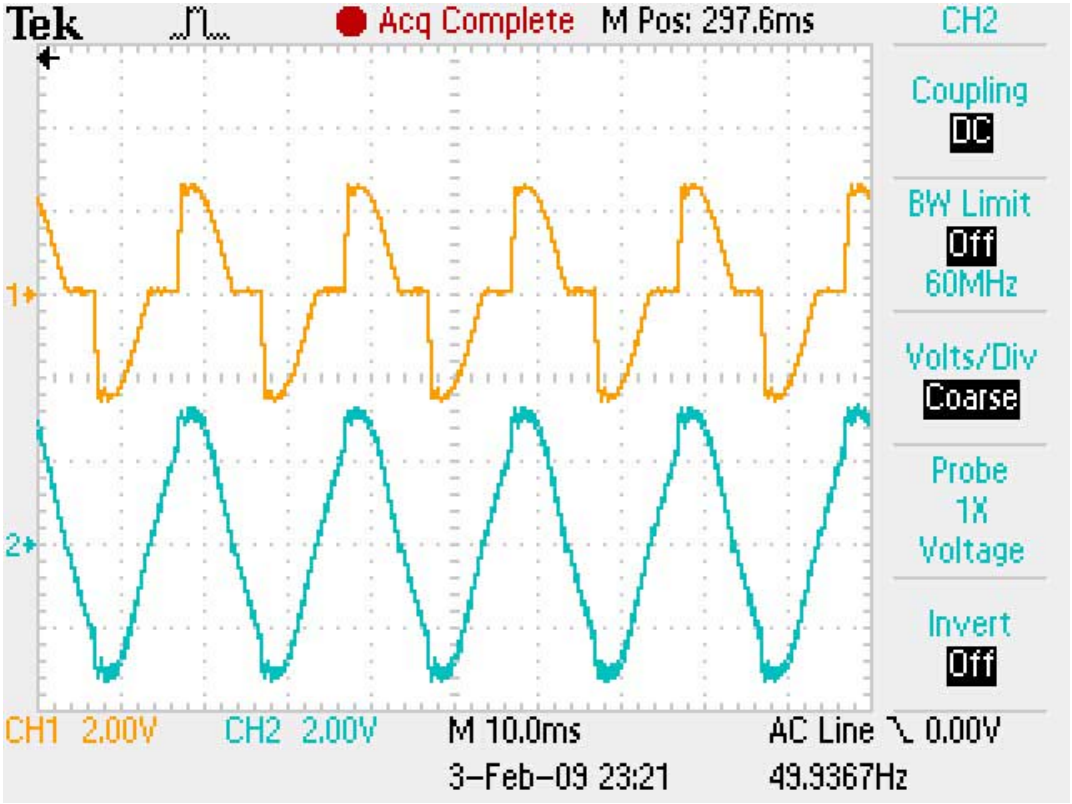


Scope trace showing reducing step transient with IL on Ch1 (1A/div) and Is on Ch2(1A/div)

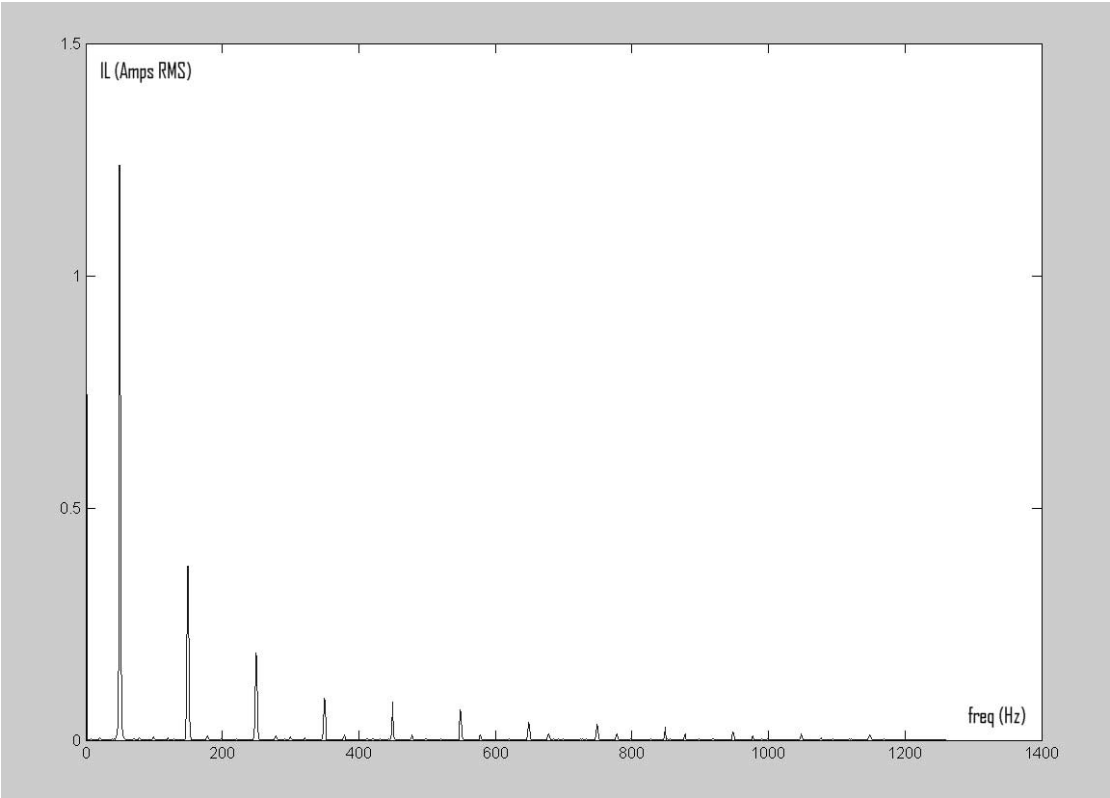
Appendix N: Phase controlled load ε = 0.9

The following system parameters are used:

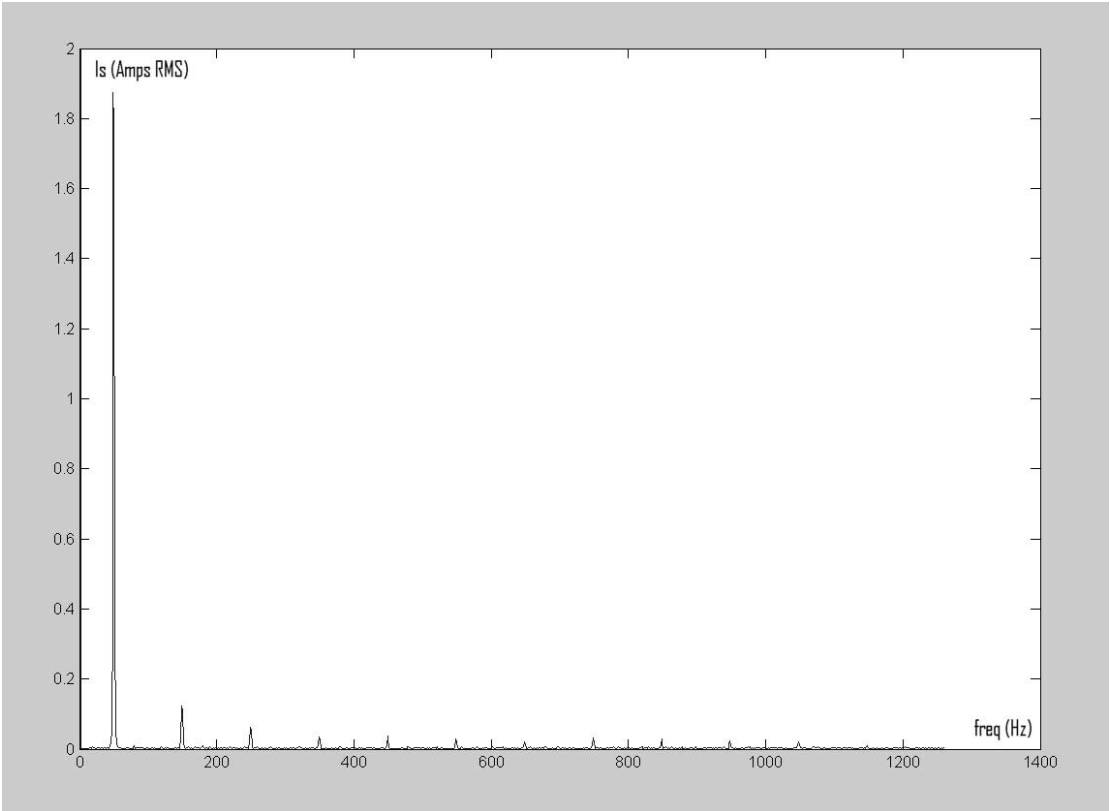
T = 20µs
Vs = 53V RMS
Vcapconst = 130V
Epsilon = 0.9
Phase controlled resistive load of 27 Ohm.



Scope trace with IL on Ch1(2A/div) and Is on Ch2(2A/div)



Frequency spectrum plot for IL (Amps RMS): phase controlled load



Frequency Spectrum plot for Is (Amps RMS): phase controlled load