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3-D Statistical Simulation Comparison of Oxide Reliability of Planar MOSFETs and FinFET

Louis Gerrer, Salvatore Maria Amoroso, Member, IEEE, Stanislav Markov, Member, IEEE, Fikru Adamu-Lema, Member, IEEE, and Asen Asenov, Fellow, IEEE

Abstract—New transistor architectures such as fully depleted silicon on insulator (FDSOI) MOSFETs and FinFETs have been introduced in advanced CMOS technology generations to boost performance and to reduce statistical variability (SV). In this paper, the robustness of these architectures to random telegraph noise and bias temperature instability issues is investigated using comprehensive 3-D numerical simulations, and results are compared with those obtained from conventional bulk MOSFETs. Not only the impact of static trapped charges is investigated, but also the charge trapping dynamics are studied to allow device lifetime and failure rate predictions. Our results show that device-to-device variability is barely increased by progressive oxide charge trapping in bulk devices. On the contrary, oxide degradation determines the SV of SoI and FinFET devices. However, the SoI and multigate transistor architectures are shown to be significantly more robust in terms of immunity to time-dependent SV when compared with the conventional bulk device. The comparative study here presented could be of significant importance for reliability resistant CMOS circuits and systems design.

Index Terms—Device modeling, FinFET, fully depleted silicon on insulator (FDSOI), nanoscale MOSFETs, reliability, variability.

I. INTRODUCTION

Discreteness of charge and matter is a major concern in contemporary and future CMOS technology generations. The Poisson statistics of the number of dopants and trapped charges determining the behavior of electronic devices makes the statistical variability (SV) increasingly important with scaling [1]. A viable solution to the variability problems is the replacement of the bulk MOSFET with new device architectures including fully depleted silicon on insulator (FDSOI) and FinFET [2], [3]. The improved gate control in FDSOI MOSFETs and FinFETs allows a drastic reduction of the channel doping and effective suppression of the random dopants fluctuations (RDFs), which is the major variability source in conventional bulk MOSFETs. However, these novel architectures are not completely immune to variability since important sources of SV, including line edge roughness (LER) and metal gate granularity (MGG) [4], [5], contribute to the dispersion in the electrical performance. Fig. 1 shows the effect of these major variability sources on the bulk, SoI, and FinFET transistors.

Beside the intrinsic (or time zero) SV, a time-dependent source of variability is the trapping of discrete charges at the interface or in the gate oxide. During the device operational, charges can be injected from the channel and captured into an existing or newly created oxidetraps leading to phenomena such as random telegraph noise (RTN) and bias temperature variations. The number of trapped charges depends on the oxide degradation and trapping dynamics. The trapping of charges into the oxide trap leads to time-dependent SV, which is two orders of magnitude higher than the intrinsic SV [6]. During the device operational, the number of trapped charges is increased by the injection and capture of charges leading to phenomena such as random telegraph noise (RTN) and bias temperature variations. The number of trapped charges depends on the oxide degradation and trapping dynamics. The trapping of charges into the oxide trap leads to time-dependent SV, which is two orders of magnitude higher than the intrinsic SV [6].

Fig. 1. Planar devices bulk, FDSOI (top) and 3-D fin (bottom) FET architectures, showing electron densities at $V_G = V_T$ when affected by SV RDF, LER and FWR.
instabilities (BTI). These are manifested in nanoscale devices as discrete and stochastic shifts in the threshold voltage $V_T$, and are responsible for the time evolution of the SV, which in turn can result in stochastic circuit failures [6]–[8].

Several papers have reported simulation studies comparing the sensitivity with SV of bulk [4], FDSoI [12], and FinFET transistors [5]. Recently, an increasing interest on reliability phenomena in nanoscale devices has resulted in the publication of a large number of experimental and simulation studies aiming to understand the interplay between the SV and the reliability in conventional bulk MOSFETs [9], [10]. However, very few papers address the interplay between the SV and the reliability in FDSoI transistors and FinFETs [11], [12]. In addition, to the best of our knowledge, all the published modeling and simulation studies only consider frozen–in–time interface charge trapping.

In this paper, we present a comprehensive simulation study of oxide reliability in the presence of SV in bulk, and FD-SoI MOSFETs and in SoI-FinFET. The latter will be named simply FinFET in the rest of this paper. By considering single-charge trapping and multiple traps degradation, we address both the RTN and BTI phenomena. Furthermore, using a kinetic Monte Carlo algorithm, we analyze the dynamic charging of oxide traps in the three architectures and estimate their lifetime statistical distribution.

II. SIMULATION METHODOLOGY

This paper is carried out using the GSS 3-D drift-diffusion simulator GARAND, which deploys density gradient quantum corrections in resolving accurately the impact of individual discrete charges [13]–[15]. The simulator has been extended to simulate the impact discrete oxide charge trapping on device performances. Each trap is defined by its position ($x_T$, $y_T$, and $z_T$), cross section $\sigma_T$, and energy level $E_T$. In this paper, we consider traps uniformly distributed at the channel/oxide interface. We also use fixed values for $\sigma_T = 10^{-14}$ cm$^2$ and $E_T = 3.2$ eV.

To allow the simulation of dynamic charge trapping (Section IV), we have developed a kinetic Monte Carlo algorithm, which is coupled to GARAND, as described in [16] and [17]. At particular bias conditions, the average capture times $\langle \tau_c \rangle$ are computed for each trap adopting the tunneling model proposed in [18] and shown in Fig. 2. An exponential prefactor is introduced for modeling a multiphonon-assisted charge injection [18], [19] allowing to reproduce the temperature dependence observed in experiments [19

$$\langle \tau_c \rangle = \exp \left( \frac{E_A}{kT} \right) \frac{q}{\int \sigma} J(x, y) dx dy. \tag{1}$$

$E_A$ is the multiphonon activation energy and is considered constant (0.6 eV) in this paper [20]. The tunneling current density $J(x, y)$ reaching each trap is obtained through a Wentzel–Krammer–Brillouin (WKB) approximation. This average time constants are used as input rates in the kinetic Monte Carlo engine, designed to choose stochastically the trap to be filled and the time interval between each charge capture [21].

The template transistors used in this paper have 22-nm channel length and are designed to meet the requirements for the 20-nm CMOS technology generation. To provide a fair comparison in terms of reliability and variability, we have calibrated the three structures to have the same nominal gate capacitance. Therefore, the gate oxide thickness is the same for the three devices ($t_{ox} = 1.2$ nm). The channel width is equal to $W = 60$ nm for the planar structures and the active fin perimeter defined $2H_F + W_F$ is also 60 nm. The FDSoI device features a 6-nm silicon layer over a 10-nm thick oxide box. The FinFET device has a width ($W$) over depth ($H$) ratio equal to 10/25 and a 20-nm thick oxide box. The transistor design parameters are summarized in Table I and the average transfer characteristics of the three transistors in both linear and saturation regimes are shown in Fig. 3.

SV is introduced using RDF and LER, implemented as in [14]. For the FinFET, both the gate LER (GLER) and the
Fig. 4. (a) and (b) Uniform devices conduction band profiles and electron concentration for a vertical cut in the middle of the device at \( V_G = V_t \) and 0.8 V. It is worth noticing that the bigger part of voltage drop is supported by oxide boxes. (c) Electron concentration in a vertical plane across the fin at \( V_G = 0.8 \) V. Notice the enhanced confinement in the corners; nevertheless, due to the rectangular shape of our simulated device the electric field does not increase in these regions.

Fig. 5. Threshold variability due to the three considered variability sources. Note that bulk devices suffer a much bigger dispersion in \( V_T \) due to random dopants in the channel. The matching factors \( AV \) are shown in Table II.

III. RESULTS AND DISCUSSION

A. Threshold Voltage Shift Variability

The conduction band edges and the relative electron concentrations in the middle of the channels for the three types of transistors are shown in Fig. 4 at threshold and at high-gate voltage (\( V_G = 0.8 \) V). It is clear that the bulk MOSFET exhibits higher electric field in the gate oxide and a more confined inversion layer (with a centroid closer to the interface) with respect to the other two architectures. It is worth noticing that the charge centroid of the inversion layer of the FDSOI transistor and the FinFET gets closer and closer to the channel interface with the increase in \( V_G \) [22], [23]. For the FinFET, the 2-D map of electron concentration in Fig. 4(c) shows the enhanced quantum confinement around the fin corners as in [11].

Fig. 5 shows the impact of SV on \( V_T \) for: due to the lack of random discrete dopants in the channel, FDSOI and FinFET exhibit much greater immunity to variability when compared with the bulk MOSFET. It is worth noting that the sensitivity of FinFET to FWR leads to a slightly higher \( \sigma V_T \) with respect to FDSOI.

Fig. 6(a) shows the \( V_T \) shifts induced by a single trap as a function of its position along the channel length in ensembles of 100 atomistic transistors at low drain bias. The bulk MOSFET exhibits the highest sensitivity, with maximum threshold voltage shifts close to 30 mV for traps located at the channel center. The trap impact on threshold voltage is significantly lower for FDSOI and FinFET devices, showing a maximum \( \Delta V_T \) close to 15 and 7 mV, respectively. The large dispersion observed for bulk devices is mainly due to random dopants in the channel, leading to a percolative conduction between the source and drain [24]–[26]. Fig. 6(b) shows the \( V_T \) shifts induced by a single trap as a function of its position along the fin width. Clearly, the fin corners are most sensitive to individual charge trapping. This explains why it is beneficial to round the corners of the fin to enhance the reliability.

Because the BTI oxide degradation in realistic conditions is due to many trapped charges [8], [9], we have studied how the impact of each single trapped charge is modified by the presence of other trapped charges [16]. Fig. 7(a) and (b) shows that the cumulative distribution of \( V_T \) shifts due to each single trapped charge is barely affected by the amount of already trapped charges in the oxide \( [5 \times 10^{11} \text{ cm}^{-2} \text{ and } 10^{12} \text{ cm}^{-2} \text{ }} \) in Fig. 7(a) and (b), respectively. This result holds for all the three analyzed architectures. It is interesting to note that the percolative conduction in the bulk MOSFET gives rise to the exponential distribution of \( V_T \) shifts. On the contrary, for the other two architectures, the threshold shifts have a bounded distribution due to the absence of random dopants in the channel. These results confirm that FinFETs and planar SoI MOSFETs are more robust to charge trapping. In particular, the SoI structure results the less sensitive to charge trapping as a consequence of the absence of the fin corner effects.

<table>
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<th>Table II</th>
<th>AV COEFFICIENT IN mV·μM−2 FOR THE THREE DEVICES WITHOUT TRAPS, WITH ( N_T = 5 \times 10^{11} \text{ cm}^{-2} ) AND ( N_T = 10^{12} \text{ cm}^{-2} ) USING ( AV = \sqrt{2} \cdot \sigma(V_T) \cdot \sqrt{\text{GATE AREA}} )</th>
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<td>( N_T = 0 \text{ cm}^{-2} )</td>
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<td>Bulk</td>
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</tr>
<tr>
<td>FDSOI</td>
<td>0.3</td>
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<tr>
<td>FinFET</td>
<td>0.5</td>
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This is because at high degradation levels, random traps start to have the same impact in FDSoI as random dopants in bulk in inducing fluctuations in the channel potential and, in turn, giving rise to a percolative behavior in the source-to-drain conduction. FinFET and FDSoI exhibit similar sensitivity to multiple trapped charges. As our channel area is not squared, the matching factors have been shown in Table II for the initial $V_T$ dispersion, and for the two investigated trap densities; as expected, the matching factor increase for $N_T = 10^{12}$ cm$^2$ is only 8.8% for the bulk, whereas it reaches 55% and 45.7% for FDSoI and FinFET. Note that in this paper, we are neglecting the higher trap concentration on the fin walls due to the $<110>$ crystal orientation [27]. In this respect, the results here reported may be regarded as the upper limit of the benefits of FinFET over planar MOSFETs, in terms of reliability.

### B. Dynamic Degradation Variability

In the previous section, we presented the results concerning the static impact of single and multiple trapped charges on the threshold voltage shift distribution of the three transistor architectures under comparison. In this section, we extend the study to consider the trap dynamics to model the time evolution of the BTI-induced variability.

Fig. 9(a) shows the distribution of capture time constants as a function of trap position along the channel length for the simulated ensembles of microscopically different devices. The difference between the FDSoI and the bulk time constants is due to both the field intensity and carrier concentration at the interface, as shown in Fig. 4. The lack of RDF in the FDSoI device results in a narrower distribution along the channel. For the FinFET, both the field and carrier concentration near the interface are far lower compared with the planar transistors. Moreover, the spatial distributions of these values vary a lot depending on trap position; in particular, Fig. 9(b) shows that the time constants and their dispersion are widely different for fin sides, top, and corners regions.

Fig. 10 shows the cumulative distribution of capture times for the three device architectures at $V_G = 1$ V, with and without SV. The geometry of the FinFET gives not only rise to a wider dispersion, but also to two different features in the distribution, due to traps located at the fin edges and at fin top, respectively: 1) the dispersion of the statistical distribution at low capture times becomes larger and 2) a new well-defined tail appears at high capture times due to corner traps. Please note that the dispersion of time constants in the bulk device is only partially due to the random dopants [17], largely screened at high gate biases, but also comes from the

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**Fig. 7.** Threshold voltage shifts cumulative distributions induced by each random trap in presence of a Poissonian number of traps evaluated at (a) $N_T = 5 \times 10^{11}$ cm$^{-2}$, (b) $N_T = 10^{12}$ cm$^{-2}$, and (c) $N_T = 10^{12}$ cm$^{-2}$ without variability. Averages ($\Delta V_T$) and standard deviation $\sigma(\Delta V_T)$ are noted for [bulk, FDSoI, and FinFET]; the same notation will be used in all the following: (a) ($\Delta V_T$) = [2.4; 2.3; 2.2] mV, $\sigma(\Delta V_T)$ = [3.8; 1.1; 1.3] mV, (b) ($\Delta V_T$) = [2.3; 2.3; 2.2] mV, $\sigma(\Delta V_T)$ = [3.8; 1.1; 1.4] mV, and (c) ($\Delta V_T$) = [2.1; 2.3; 2.3] mV, $\sigma(\Delta V_T)$ = [1.9; 1.1; 1.4] mV.

**Fig. 8.** Total threshold voltage shifts cumulative distributions induced by a Poissonian number of traps evaluated at (a) $N_T = 5 \times 10^{11}$ cm$^{-2}$, (b) $N_T = 10^{12}$ cm$^{-2}$, and (c) $N_T = 10^{12}$ cm$^{-2}$ without variability. Averages and standard deviation: (a) ($\Delta V_T$) = [12; 11; 10] mV, $\sigma(\Delta V_T)$ = [8.7; 5.6; 5.8] mV, (b) ($\Delta V_T$) = [21; 22; 21] mV, $\sigma(\Delta V_T)$ = [14; 8.4; 8.5] mV, and (c) ($\Delta V_T$) = [19; 22; 21] mV, $\sigma(\Delta V_T)$ = [8.5; 8.3; 8.7] mV.

To highlight the important role played by random dopant fluctuations on the dispersion of the threshold voltage shifts, we have repeated simulations (for a trap density of $10^{12}$ cm$^{-2}$) without variability sources. The obtained results are shown in Fig. 7(c) and highlight that 3-D electrostatic plays a main role in $\Delta V_T$ dispersion for the FDSoI MOSFETs and FinFETs, whereas RDF is mainly responsible for the large exponentially distributed $\Delta V_T$ in Bulk MOSFETs.

Fig. 8(a) and (b) shows the distribution of $\Delta V_T$ induced by a Poissonian number of charged traps corresponding to an average $5 \times 10^{11}$ and $10^{12}$ traps per cm$^2$. Fig. 8(c) shows the same distribution of trapped charges as Fig. 8(b), without SV. Although the average impact of traps is the same for both planar devices, the dispersion is wider for bulk devices due to traps interaction with RDF [16]. It is worth noting out that when increasing the trap density, the average $\Delta V_T$ impact remains identical for planar devices but the dispersion increases up to 47% for the FDSoI but only 27% for the bulk. This is because at high degradation levels, random traps start to have the same impact in FDSoI as random dopants in bulk in inducing fluctuations in the channel potential and, in turn, giving rise to a percolative behavior in the source-to-drain conduction. FinFET and FDSoI exhibit similar sensitivity to multiple trapped charges. As our channel area is not squared, the matching factors have been shown in Table II for the initial $V_T$ dispersion, and for the two investigated trap densities; as expected, the matching factor increase for $N_T = 10^{12}$ cm$^2$ is only 8.8% for the bulk, whereas it reaches 55% and 45.7% for FDSoI and FinFET. Note that in this paper, we are neglecting the higher trap concentration on the fin walls due to the $<110>$ crystal orientation [27]. In this respect, the results here reported may be regarded as the upper limit of the benefits of FinFET over planar MOSFETs, in terms of reliability.
3-D nonuniform electrostatics. Note that the limited range of dispersion compared with the experimental results [20] is due to the fixed value adopted in simulation for trap level, trap depth, and trap activation energy.

Fig. 11(a)–(c) shows the stochastic time-dependent BTI threshold voltage traces at two different trap densities with and without SV. Dispersion in the BTI charging curves comes from both the DVT variability and the time constants variability [21], [28].

As expected, planar transistors are susceptible to the largest BTI-induced threshold voltage shifts and dispersion. The differences between the bulk and SoI architectures are mainly due to different sensitivity to trap-induced $V_T$ shifts: the RDF-induced fluctuations are indeed responsible for the extreme behavior of several bulk devices. On the contrary, FinFETs gain significant advantage from both smaller dispersion of the threshold voltage shifts and higher average value of the trapping time constants. However, contrary to the planar transistors, the dispersion of BTI traces in the FinFET case is mainly due to time constants dispersion, which derives principally from the traps positions, as shown by Fig. 9. The SV impact comes mostly from LWR, as shown by Fig. 10. It is worth noting that for all devices, the dispersion is widely enhanced by the Poissonian variations in trap numbers from device to device.

With the simulation of BTI charging traces, we show in Fig. 12(a), the proportion of devices reaching a failure criterion equivalent to 30 mV of threshold voltage shift during the stress time. As suggested already by Fig. 8, for a 30-mV failure criterion the maximum number of failed bulk devices (25%) is much higher than the one of FDSOI (19%) and FinFET devices (17%). Please note that the saturation of the number of failed devices is because we are neglecting the creation of new traps during stressing time. As shown in Fig. 11 in bulk transistors, the device failure occurs almost half decade earlier than in FDSOI. For FinFETs, the first failure occurs two decades later compared with bulk. These observations are confirmed by the time-to-failure distributions shown in Fig. 12(b). The average time to failure for bulk transistors is one order of magnitude faster than for the FDSOI transistors and four orders of magnitude faster than for FinFETs. The same trend is also maintained for the standard deviation of these distributions.

Figs. 13 and 14 summarize our analysis comparing the $V_T$ variability induced by BTI for the three architectures. Fig. 13(a) shows the normalized average threshold shift
increase with the average number of charged traps, while Fig. 13(b) shows that the same 3-D capacitance determines the average impact of traps. It is very important to note that the BTI-induced $V_T$ variability is negligible when compared with the already large RDF-induced $V_T$ variability in bulk transistors [29], [30], as shown in Fig. 14(a). On the contrary, BTI plays a main role in determining the $V_T$ dispersion during stressing time in SOI and FinFET devices, as shown in Fig. 14(b). In particular, the planar SOI architecture shows the largest relative $\sigma$ $V_T$ increase due to BTI. However, in terms of absolute $V_T$ deviation due to BTI, both planar SOI and FinFET devices exhibit robustness and, in turns, both of them offer a larger reliability-aware design margin when compared with the planar bulk architectures.

IV. CONCLUSION

In this paper, we have presented a comprehensive comparison of the statistical reliability of bulk and FDSoI MOSFETs and FinFETs. The time-dependent simulation of the evolution of BTI-induced SV shows that the planar SOI and the multigate approaches to device scaling are more robust and offer more design margin when compared with the planar conventional bulk approach. The results here presented also highlight the design challenges associated with time-dependent variability next generation CMOS technologies and corresponding devices.

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