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Charge-trapping characteristics of fluorinated thin ZrO$_2$ film for nonvolatile memory applications

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The effects of fluorine treatment on the charge-trapping characteristics of thin ZrO$_2$ film are investigated by physical and electrical characterization techniques. The formation of silicate interlayer at the ZrO$_2$/SiO$_2$ interface is effectively suppressed by fluorine passivation. However, excessive fluorine diffusion into the Si substrate deteriorates the quality of the SiO$_2$/Si interface. Compared with the ZrO$_2$-based memory devices with no or excessive fluorine treatment, the one with suitable fluorine-treatment time shows higher operating speed and better retention due to less resistance of built-in electric field (formed by trapped electrons) against electron injection from the substrate and smaller trap-assisted tunneling leakage, resulting from improved ZrO$_2$/SiO$_2$ and SiO$_2$/Si interfaces. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4873388]

Metal-oxide-nitride-oxide-silicon (MONOS)-type nonvolatile memory with discrete traps in the dielectric for charge storage is considered as a promising candidate to replace its floating-gate counterpart due to stronger scaling ability and higher reliability. Recently, high-$k$ dielectrics have been proposed instead of conventional Si$_3$N$_4$ as charge-trapping layer (CTL) to achieve lower operating voltage and higher charge-trapping efficiency. Among various high-$k$ dielectrics, Hf-based oxides (e.g., HfO$_2$ and HfON) have been extensively investigated as CTL mainly because of its low conduction-band offset relative to SiO$_2$ ($\Delta E_c \sim 2.0$ eV), high $k$ value ($\sim 22$), and compatibility with CMOS processing. On the other hand, ZrO$_2$ shows similar dielectric properties as HfO$_2$ but has higher $k$ value ($\sim 37$). Consequently, there is an increasing interest in exploring ZrO$_2$ as CTL. Wu et al. studied the charge-trapping characteristics of ZrO$_2$ with and without nitridation and found that MONOS device with nitrided ZrO$_2$ showed better performance than that without nitridation due to nitrogen passivation of the ZrO$_2$ film. Besides nitrogen, fluorine is also an excellent passivant to remove oxide defects and strengthen the dielectric films due to its very high electronegativity. Therefore, fluorination is an effective way to improve the charge-trapping characteristics of dielectrics. In this work, based on MONOS capacitors, the charge-trapping characteristics of ZrO$_2$ with and without fluorine incorporation are studied. Detailed analysis of fluorine treatment on the device performance is also carried out.

MONOS capacitors with Al/Al$_2$O$_3$/ZrO$_2$/SiO$_2$/Si were fabricated on p-type (100) substrate. After the standard RCA cleaning, 2-nm SiO$_2$ tunneling oxide was grown on the wafers by thermal dry oxidation. Then 3-nm ZrO$_2$ was deposited on the SiO$_2$ by sputtering using a Zr target in an Ar/O$_2$ (8/1) mixed ambient. Following that, some samples were treated by a CHF$_3$ + O$_2$ (10 SCCM/1 SCCM) plasma at 20 W for 150 s and 400 s, respectively. The low-concentration O$_2$ was used to remove the carbon and hydrogen in the plasma. Then, 15-nm Al$_2$O$_3$ was deposited by atomic layer deposition using trimethyl-aluminum (Al(CH$_3$)$_3$) and H$_2$O as precursors at 300 °C. Following that, all the samples went through a post-deposition annealing in N$_2$ at 900 °C for 30 s. Finally, Al was evaporated and patterned as gate electrodes followed by a forming-gas annealing at 300 °C for 20 min. The sample without fluorine treatment was denoted as ZrO, while the samples with 150-s and 400-s fluorine treatment were denoted as LF-ZrO and HF-ZrO, respectively. In addition, Al/Al$_2$O$_3$/SiO$_2$/Si (denoted as MAOS) and Al/ZrO$_2$/SiO$_2$/Si (denoted as MNOS) capacitors were also fabricated by the same process to study the charge-trapping characteristics of the ZrO$_2$ film. The physical properties of the films with and without fluorine treatment were analyzed by transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), and X-ray photoelectron spectroscopy (XPS). The electrical characteristics of the devices were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer.

Fig. 1 shows the cross-sectional TEM image of the MONOS capacitors with and without the fluorine treatment, where the physical thickness remains the same after the fluorine treatment, indicating negligible etching of the ZrO$_2$ film due to the low energy of the fluorine plasma treatment. Fig. 2(a) displays the SIMS depth profile of the samples with various fluorine-treatment times to evaluate the fluorine distribution. It is clear that fluorine is mainly located in the ZrO$_2$/SiO$_2$ stack and decreases rapidly in the Si substrate, indicating strong fluorine passivation in the ZrO$_2$/SiO$_2$ stack. Also, the fluorine atoms diffuse more into the Si substrate for longer fluorine-treatment time.

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the spectrum shifts to higher binding energy by 0.5 eV, indicating that F is bonded with Zr. Moreover, the Zr spectrum can be decomposed into two components, corresponding to ZrO$_2$ (182.3 eV for Zr 3d$_{5/2}$) and Zr silicate formed by the ZrO$_2$/SiO$_2$ interfacial reaction (182.7 eV for Zr 3d$_{5/2}$). Compared with the ZrO sample, the much smaller area of the silicate component for the LF-ZrO and HF-ZrO samples indicates negligible formation of the Zr silicate interlayer due to sufficient fluorine passivation. The formation of the interlayer consumes the SiO$_2$ tunneling oxide, and also it has smaller bandgap ($\Delta E_C \sim 6.6$ eV) and more defects than thermally grown SiO$_2$ ($\sim 8.9$ eV). Therefore, an abrupt interface without interlayer is desirable for good data retention.

Fig. 3(a) displays the C-V loops under ±8 MV/cm sweeping for the MAOS and MNOS samples. The trapped-charge density ($Q_{ox}$) in the device can be calculated by the expression below

$$Q_{ox} \approx \frac{\Delta V_{FB} C_{ox}}{q},$$  \hspace{1cm} (1)$$

where $\Delta V_{FB}$ is the memory window from the C-V loops, $C_{ox}$ is the capacitance density of the samples, and $q$ is the electron charge. The $Q_{ox}$ for the MAOS and MNOS samples is about $3.5 \times 10^{10}$ cm$^{-2}$ and $1.1 \times 10^{12}$ cm$^{-2}$, respectively. The much higher $Q_{ox}$ for the MNOS sample than that for the MAOS one at the same operating condition indicates that the charge-trapping site is mainly in the ZrO$_2$ layer. In addition, compared with the MAOS sample with counterclockwise hysteresis loop, the MNOS one exhibits a clockwise hysteresis loop, suggesting that charges inject from the Al electrode into the ZrO$_2$ layer at the forward sweeping (from −8 MV/cm to +8 MV/cm) mainly due to the smaller barrier height at the Al/ZrO$_2$ interface ($\Delta E_C \sim 1.6$ eV for Al/ZrO$_2; \sim 3.0$ eV for Al/Al$_2$O$_3$). Fig. 3(b) depicts the 1-MHz C-V hysteresis loops of the MONOS devices, where the memory window for the ZrO, LF-ZrO, and HF-ZrO samples is 4.8 V, 3.8 V, and 5.1 V, respectively. The smaller window for the LF-ZrO sample than the ZrO sample is due to the suppressed formation of interlayer by fluorine passivation, while the largest window for the HF-ZrO sample suggests extra traps generated by excessive fluorine treatment. The C-V curve of the HF-ZrO sample shows more severe stretch-out characteristic than the ZrO and LF-ZrO samples, implying its higher interface-state density ($D_{it}$) at the SiO$_2$/Si interface. Using the Terman’s method, the HF-ZrO sample has an extracted $D_{it}$ of $7.4 \times 10^{12}$ cm$^{-2}$, corresponding to 8.8% and 17.5% higher than the ZrO sample ($6.8 \times 10^{12}$ cm$^{-2}$) and the LF-ZrO sample ($6.3 \times 10^{12}$ cm$^{-2}$), respectively. Appropriate fluorine incorporation can passivate the SiO$_2$/Si interface,

FIG. 1. Cross-sectional TEM image for (a) the HF-ZrO and (b) ZrO MONOS capacitors.

FIG. 2. (a) SIMS depth profile of ZrO$_2$/SiO$_2$ on Si substrate with various fluorine treatments. (b) XPS Si 2p spectrum and (c) XPS Zr 3d spectrum for the samples with and without fluorine treatments.
leading to the smallest \( D_t \) for the LF-ZrO sample. However, owing to the high electronegativity of fluorine, excessive fluorine can distort and even cleave the Si-Si bonds at the interface to form dangling Si bonds and Si-F bonds (as demonstrated in Fig. 2), resulting in the highest \( D_t \) and thus the largest window for the HF-ZrO sample.

Fig. 4(a) displays the gate leakage \( (J_G) \) of the MONOS devices as a function of electric field across SiO\(_2\) (\( E_{OX} \)) by applying positive gate voltage (\( V_G \)), corresponding to electron injection from the substrate. The LF-ZrO sample has a smaller leakage at low \( E_{OX} \) than the ZrO and HF-ZrO samples due to fewer traps at/near its interface and thus reduced trap-assisted tunneling. Moreover, the \( J_G-E_{OX} \) curve of the HF-ZrO sample presents an obvious notch (denoted as A), where \( J_G \) decreases with \( E_{OX} \) and then increases again. This is associated with its high \( D_t \) at the SiO\(_2\)/Si interface. Due to Coulomb repulsion, electrons trapped by interface states can form a built-in electric field (\( E_{in} \)) opposite to the external electric field \( E_{OX} \) induced by \( V_G \), which is approximately given by

\[
E_{in} \approx \frac{1}{4\varepsilon R} \frac{Q_a}{R} \tag{2}
\]

where \( Q_a \) is the trapped charge; \( \varepsilon \) is the permittivity of the dielectric that \( E_{in} \) passes through; and \( R \) represents the distance between the trapped-charge centroid and the substrate. \( E_{in} \) tends to block the electron injection and also electrons filled in the shallow traps near the interface would flow back into the substrate due to \( E_{in} \), both of which can offset the electron injection from the substrate. With increasing \( E_{OX} \) and establishing a balance between electron trapping and de-trapping, \( J_G \) increases with \( E_{OX} \) again. A similar notch (denoted as B) is also observed for the ZrO sample due to high trap density at the ZrO\(_2\)/SiO\(_2\) interlayer and high \( D_t \) at the SiO\(_2\)/Si interface. On the contrary, no notch in the \( J_G-E_{OX} \) curve for the LF-ZrO sample suggests that its \( E_{in} \) is weak and has little effect on electron injection, resulting from the suppressed formation of interlayer at the ZrO\(_2\)/SiO\(_2\) interface by the fluorine passivation as well as low \( D_t \) at the SiO\(_2\)/Si interface by avoiding excessive fluorine diffusion to the Si substrate. For the ZrO and HF-ZrO samples, the traps generated by the Zr-silicate interlayer and high interface states lead to larger \( V_{FB} \) shift (thus larger \( Q_a \)) at low electric field as shown in Fig. 4(b). Moreover, these trapped charges at the ZrO\(_2\)/SiO\(_2\) and SiO\(_2\)/Si interfaces make the trapped-charge centroid closer to the substrate compared with those located in the ZrO\(_2\) film, thus resulting in stronger \( E_{in} \) against electron injection according to Eq. (2). This is consistent with the phenomenon that the \( J_G \) of the LF-ZrO

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**FIG. 3.** (a) 1-MHz C-V loops of the MNOS and MAOS devices under ±8 MV/cm sweeping; (b) 1-MHz C-V loops of the MONOS devices under ±12 V sweeping.

**FIG. 4.** (a) \( J_G \) as a function of \( E_{OX} \) for the MONOS capacitors. The simulated FN tunneling current through SiO\(_2\) tunneling oxide is also shown. (b) \( V_{FB} \) shift at low (~4 MV/cm) and high (~8 MV/cm) \( E_{OX} \). \( V_{FB} \) shift is defined as \( V_{FB} - V_{FB0} \), where \( V_{FB} \) is the flat-band voltage under stress, and \( V_{FB0} \) is the flat-band voltage of the fresh device.
sample increases more rapidly with \( E_{\text{OX}} \) than those of the ZrO and HF-ZrO samples, which becomes more obvious as the Fowler-Nordheim (FN) tunneling current dominates \( I_{\text{G}} \) (FN current is exponentially proportional to electric field of \( E_{\text{OX}} \)). It should be noted that the little impact of \( E_{\text{in}} \) on electron injection from the substrate is beneficial to supplying sufficient electrons for the memory device, thus contributing to the larger \( V_{\text{FB}} \) shift (~3.1 V versus 2.8 V for ZrO, 2.5 V for HF-ZrO) at high electric field for the LF-ZrO sample in Fig. 4(b). On the other hand, small leakage at low electric field normally indicates suppressed trap-assisted tunneling under retention mode and thus is beneficial for data retention. Therefore, the steeper \( I_{\text{G}}-E_{\text{OX}} \) characteristic of the LF-ZrO sample is desirable for memory device to achieve high operating speed as well as good data retention.

Fig. 5(a) displays the retention characteristics of the MONOS capacitors, and the retention data for the ZrO sample with thicker SiO\(_2\) tunneling layer (SiO\(_2\) ~3.5 nm) are also measured to study charge-loss paths under the retention mode. The ZrO sample with thicker SiO\(_2\) shows excellent data retention with no charge loss even after \( 10^4 \) s suggests that no charge loss happens through the Al\(_2\)O\(_3\) blocking layer mainly due to its high quality with negligible traps. Moreover, compared with the ZrO sample with thicker SiO\(_2\), the ZrO one with thinner SiO\(_2\) (~2.0 nm) shows worse data retention, indicating that the charge loss is mainly determined by the tunneling SiO\(_2\) layer. As the operating temperature is raised from 25°C to 125°C, the charge-loss rate after \( 10^4 \) s (~6.8% for ZrO, ~3.4% for HF-ZrO) increases from 3.9% to 21.2% for the LF-ZrO sample; For comparison, the corresponding \( Q_{\text{loss}} \) increases from 19.9% to 32.6% and from 24.9% to 36.8% for the ZrO and HF-ZrO samples, respectively. The lower \( Q_{\text{loss}} \) of the LF-ZrO sample demonstrates its better data retention. The activation energy \( E_A \) of the charge loss is also extracted from the Arrhenius plot of the retention property in Fig. 5(b) to gain more insight on the charge-loss mechanism. The much smaller \( E_A \) of the ZrO sample (~0.041 eV) and HF-ZrO sample (~0.050 eV) indicates that the charge-loss mechanism is mainly based on tunneling process, which hardly depends on temperature. For the ZrO and HF-ZrO samples, the electrons trapped at the ZrO\(_2)/SiO\(_2\) or SiO\(_2)/Si\) interface are close to the substrate, thus easily escaping back to the substrate, because the tunneling probability increases exponentially with decreasing barrier height and tunneling distance between the trapped electrons and the substrate. Also, the traps at the ZrO\(_2)/SiO\(_2\) and SiO\(_2)/Si\) interfaces can act as a medium to facilitate the escaping of electrons from the CTL to the substrate by trap-assisted tunneling. On the contrary, the trapped electrons in the LF-ZrO sample cannot move easily by tunneling but have to be thermally activated to the conduction band of the CTL before tunneling to the substrate (due to the larger distance of the trapped charges in the ZrO\(_2\) film from the substrate as well as high-quality ZrO\(_2)/SiO\(_2\) and SiO\(_2)/Si\) interfaces), thus resulting in larger \( E_A \) (~0.17 eV) and better data retention.

In summary, the effects of fluorine treatment on the charge-trapping characteristics of thin ZrO\(_2\) film are investigated. Compared with the memory devices with no or excessive fluorine treatment, the one with suitable fluorine treatment time shows better characteristics due to suppressed interlayer growth by fluorine passivation of the ZrO\(_2)/SiO\(_2\) interface and also fewer interface states by avoiding excessive fluorine diffusion to the substrate. Therefore, ZrO\(_2\) film with appropriate fluorine incorporation is a promising candidate as CTL for high-performance nonvolatile memory applications.

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