Title	Direct AC/DC Rectifier With Mitigated Low-Frequency Ripple Through Inductor-Current Waveform Control
Author(s)	Li, S; Zhu, GR; Tan, SC; Hui, SYR
Citation	IEEE Transactions on Power Electronics, 2015, v. 30 n. 8, p. 4336-4348
Issued Date	2015
URL	http://hdl.handle.net/10722/208685
Rights	IEEE Transactions on Power Electronics. Copyright © Institute of Electrical and Electronics Engineers.

Direct AC/DC Rectifier With Mitigated Low-Frequency Ripple Through Inductor-Current Waveform Control

Sinan Li, *Member, IEEE*, Guo-Rong Zhu, *Member, IEEE*, Siew-Chong Tan, *Senior Member, IEEE*, and S. Y. (Ron) Hui, *Fellow, IEEE*

***Abstract*—In a rectification system with unity power factor, the input power consists of a dc and a double-line frequency power component. Traditionally, an electrolytic capacitor (E-Cap) is used to buffer the double-line frequency power such that the dc output presents a small voltage ripple. The use of E-Cap significantly limits the lifetime of the rectifier system. In this paper, a differential ac/dc rectifier based on the use of an inductor-current waveform control methodology is proposed such that a single-stage direct ac/dc rectification without the need of an E-Cap for buffering the double-line frequency power, and a front-stage diode rectifier circuit can be achieved. The feasibility of the proposal has been practically confirmed in an experimental prototype.**

***Index Terms*—E-capless, LED, low-frequency ripple, rectifier, single-stage, waveform control.**

I. Introduction

UNITY power factor (PF), high efficiency, high reliability, compact size, and low cost are the typical desired features of conventional ac/dc rectification systems. Traditionally, electrolytic capacitors (E-caps) of large capacitance are used to buffer the double mains frequency ripple current or power in the intermediate stage between the ac input and the dc output. The reduction of such ripple current or power is particularly important in lighting and battery-charging applications because the low-frequency current of 100 or 120 Hz could cause flickering in lighting systems and is detrimental to the storage properties of the batteries. Due to the relatively short lifetime of E-caps, many research efforts have been devoted to develop ac–dc power converter topologies without using E-caps [1]–[17]. Both active [1]–[15] and passive [16], [17] approaches have been reported in the recent literature.

For the active approach, an auxiliary circuit (typically comprising a bidirectional ac-dc switching circuit, an inductor, and a capacitor) [1]–[11] can be added to conventional diode rectifier or full bridge inverter to buffer the ripple power. The energy stored in a capacitor is $0.5\,\mathrm{C}\mathrm{V}_C^2$, where C is the capacitance and V_C is the capacitor voltage. In order to buffer the ripple power with reduced capacitor size, the general principles include:

1) charging and discharging a relatively small nonelectrolytic capacitor to a relatively high capacitor voltage in a separate ripple port [1], [3] in order to absorb the ripple power as shown in Fig. 1;
2) decoupling the ac power by linking the auxiliary circuit to either the ac input port [2], [4] or the dc ground [5], [11] or another inverter leg [6], or the output dc port [9];
3) integrating the auxiliary circuit into a standard switched mode converter [7] or switched mode rectifier [8];
4) shaping the input ac current in order to reduce the peak-to-average current ratio [12]–[14] and simultaneously meet the IEC harmonics requirements at a reduced PF;
5) storing the ripple power in an inductor instead of a capacitor [15].

For the passive approach that does not use any fully controlled active switches such as power MOSFETs, a large inductor is usually used to limit the input power into the diode bridge from the AC grid and thus the output current and power [16], [17]. A small valley-fill circuit [16] or more simply a small capacitor [17] can be used to reduce the ripple power of the dc port. Generally, some output current ripple is allowed because it has been pointed out that the luminous flux variation arising from the power fluctuation in an LED system can be reduced by proper thermal design of the heatsink [18]. Such passive LED systems are particularly suitable for outdoor applications and have reached commercialization stage for LED street-lighting systems.

In this paper, a direct (electrolytic-capacitor-free) ac/dc rectifier with mitigated low-frequency ripple through the use of an inductor-current waveform control is proposed. This method is different from the capacitor voltage waveform control reported in [19]. The proposed system allows the use of differential dc/dc converter topologies [20] to directly rectify power from the ac source to the load (i.e., a single-stage ac/dc rectification) without the need of the front-stage diode rectifier circuit and the PFC converter. The proposed rectifier is capable of automatically achieving PF correction without the need of a large input filter. The inductor-current waveform control mitigates the double-line frequency current without the need for a large capacitance in the system, thereby eliminating the need for an E-Cap.

Manuscript received February 26, 2014; revised May 11, 2014 and July 31, 2014; accepted September 9, 2014. Date of publication September 25, 2014; date of current version March 5, 2015. This work was supported by the Hong Kong Research Grant Council under Theme-based Research Project T22-715-12N. Recommended for publication by Associate Editor T. Shimizu.

S. Li and S.-C. Tan are with the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong (e-mail: sean861031@gmail.com; sctan@eee.hku.hk).

G.-R. Zhu is with the School of Automation, Wuhan University of Technology, Wuhan 430070, China (e-mail: zhgr_55@hotmail.com).

S. Y. (R.) Hui is with the Department of Electrical & Electronic Engineering, The University of Hong Kong, Hong Kong, and also with Imperial College London, London SW7 2AZ, U.K. (e-mail: ronhui@eee.hku.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2360209

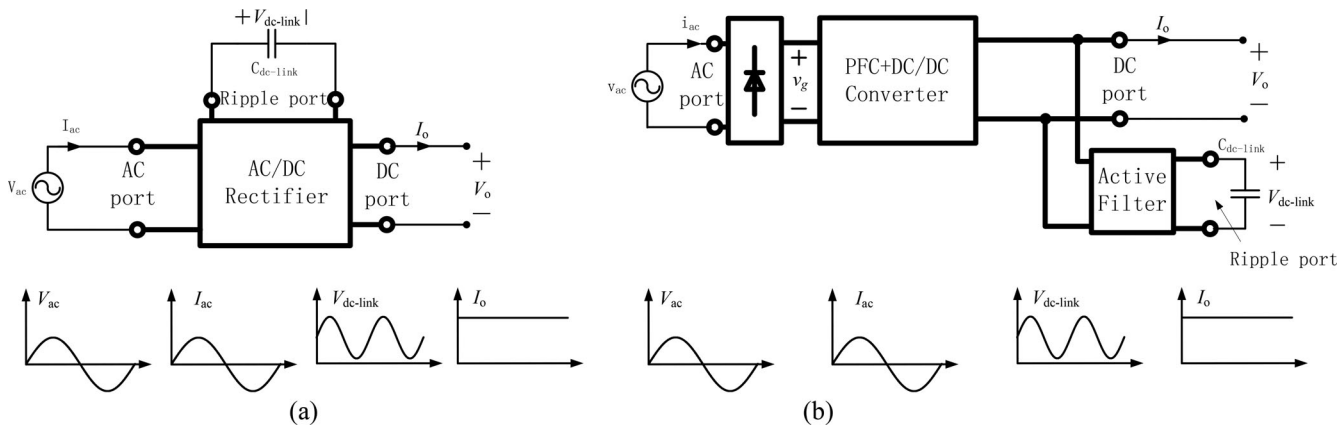


Fig. 1. (a) Conceptual diagram of three-port model of an ac/dc rectifier and (b) a rectification system with parallel active filtering.

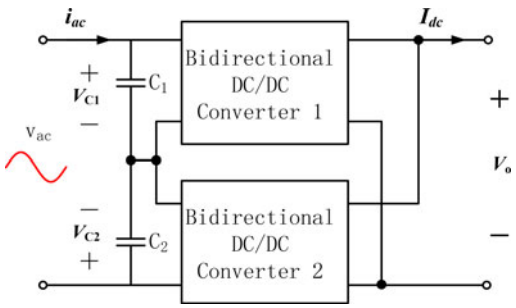


Fig. 2. Schematic of the differential rectifier system used for the inductor-current waveform control.

II. Proposed Direct AC/DC Rectifier System

A. Concept

Fig. 2 shows the general concept of the direct ac/dc differential rectification system, in which two bidirectional dc/dc converters are connected in a series-input and parallel-output configuration [20]. Here, v_{c1} and v_{c2} are, respectively, the input voltage of each of the two converters, whereby v_{c1} and v_{c2} are in opposing polarity, and their difference is a pure sinusoidal waveform that follows the shape of the input ac source $v_{\rm ac}$. It must be emphasized that

1) The proposed differential rectifier is in compliance with existing requirements for typical single-stage ac/dc power converters, e.g., conversion functionality, isolation, PF, input/output filter requirement, etc. The front-stage diode rectifier, large input filter, and the postregulation dc/dc conversion stage are not required.
2) The input voltage of the two converters, v_{c1} and v_{c2}, can be of many forms, as long as their differential value is equal to the ac voltage source $v_{\rm ac}$. This facilitates the use of the waveform control technique, which allows the system to concurrently achieve good-quality single-stage ac/dc rectification and double-line frequency ripple mitigation without the use of E-Cap.
3) In the case of adopting bidirectional dc/dc converters in the proposed configuration, the bidirectional power flow ability of the two converters implies both power rectification and inversion capability of the proposed ac/dc differential system.

B. Topology

The bidirectional dc/dc converters in Fig. 2 can be of any type, depending on the required application. They can be converters without (e.g., buck, boost, buck–boost, Cuk, Zeta) or with galvanic isolation (flyback, push–pull, forward). In fact, many existing rectifier topologies can be treated as two converters with a differential configuration. For instance, the widely applied full-bridge PWM rectifier is functionally equivalent to two bidirectional boost converters connected differentially, as shown in Fig. 3. Fig. 3(a) shows a full-bridge rectifier, whose input filter capacitors are formed by C_1 and C_2. If the joint point between C_1 and C_2 is connected to the dc ground, as indicated by the dashed line, the full-bridge rectifier can be redrawn in the form of the proposed differential rectifier configuration, as given in Fig. 3(b). In other words, a full-bridge rectifier is a boost type differential rectifier. The step-up property of the boost converter ensures that the full-bridge rectifier can only output a dc voltage with an amplitude higher than that of the ac utility.

In this paper, a buck-type differential rectifier is used as a case-study example to illustrate the concept (see Fig. 4). The rectifier comprises two bidirectional buck converters connected under the proposed differential configuration [20]. Here, C_1, C_2, and L_1, L_2 are the input capacitors and output inductors for the respective converter, and $T_1 - T_4$ are their power switches. In this system, the upper converter is called the high-side converter (formed by C_1, T_1, T_2, L_1), and the lower converter is called the low-side converter (C_2, T_3, T_4, L_2). The rectifier is capable of directly generating a dc voltage with amplitude either higher or lower than the amplitude of the ac mains. The direct step-down ability makes the buck differential rectifier an interesting solution for applications where the dc output voltage is low since the rectifier requires no further processing stage.

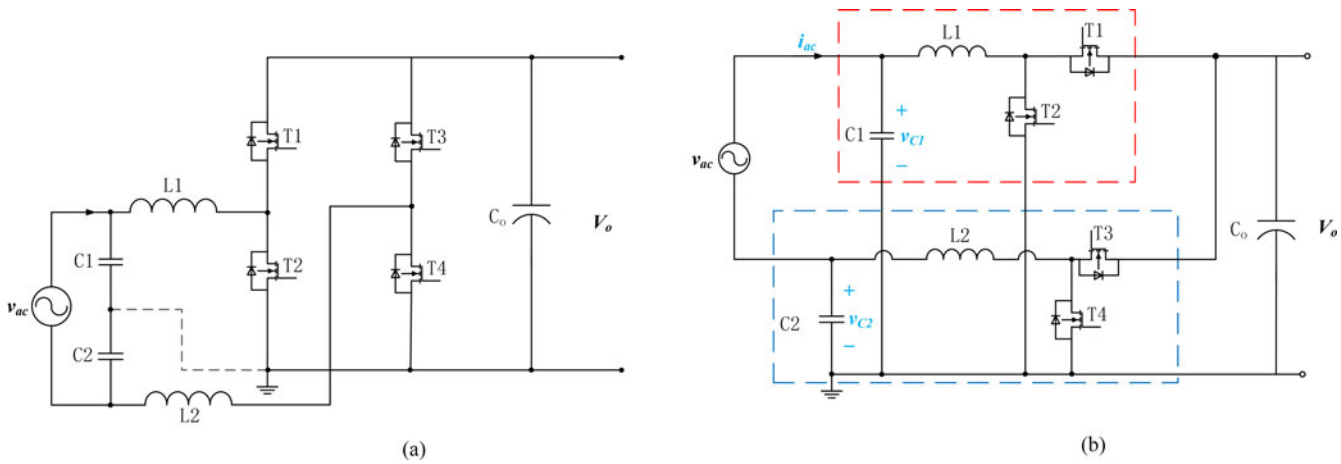


Fig. 3. (a) Conventional full-bridge PWM rectifier and (b) its equivalent differential rectifier model configuration.

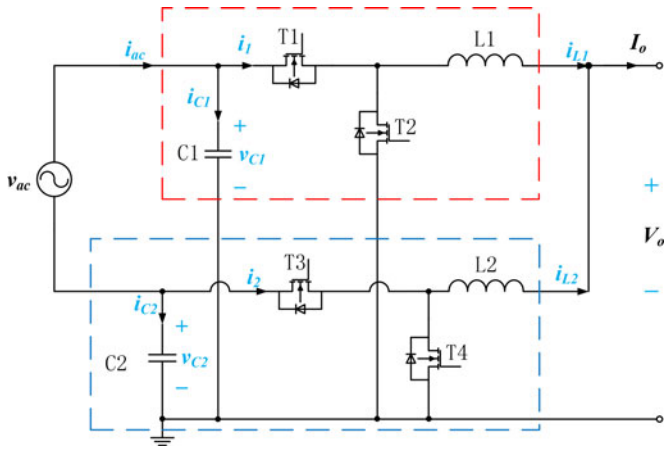


Fig. 4. Buck differential rectifier.

TABLE I
OPERATING STATES OF THE BUCK DIFFERENTIAL RECTIFIER

Switch State	T_1 (high side)	T_2 (high side)	T_3 (low side)	T_4 (low side)
S_1	OFF	ON	OFF	ON
S_2	OFF	ON	ON	OFF
S_3	ON	OFF	ON	OFF
S_4	ON	OFF	OFF	ON

C. Operation of the Buck Differential Rectifier

The capacitor-voltage waveform control method is originally proposed for differential inverters [19], the control of which involves only the regulator for the ac side capacitor voltages v_{c1} and v_{c2}. In the case of the differential rectifier, a different set of control variables and a different controller are needed.

Table I shows the four possible operating states S_1, S_2, S_3, and S_4 of the buck differential rectifier in a complete line cycle with respect to the ON/OFF states of the switches T_1-T_4. The corresponding equivalent circuits are given in Fig. 5. In order to operate the rectifier properly, it must be highlighted that it is not possible for the four states to exist at the same time in one switching cycle, neither during positive line cycle nor during the negative cycle. In the positive half of the line cycle, the possible states are S_1, S_2, and S_3, and in the negative half of the line cycle, the possible states are S_1, S_3, and S_4. This phenomenon is caused by the unbalance of the instantaneous input power (dc power plus a double-line frequency component) and the constant output power. Take the positive line cycle as an example. In this line cycle, the high-side converter is providing more power than the dc side requires. In order to keep the output power constant, the excessive energy has to be released back to the ac side into C_2. Therefore, during the interval when ac power is delivered through high-side converter (when T_1 is ON), the low-side converter always sinks power from output (T_1 ON, T_3 is ON, S_3 mode) without sourcing power to the output (T_1 ON, T_4 ON, S_4 mode). The process is physically inevitable, no matter what control techniques are used.

All possible operating conditions for switches T_1 and T_3 during the positive and negative half-line cycles are depicted in Figs. 6 and 7.

The duty cycles of the rectifier must satisfy (1) such that d_{low} (duty ratio of the low-side converter with respect to T_3) is always larger than or equal to d_{high} (duty ratio of the high-side converter with respect to T_1) during the positive half-line cycle, and vice versa. Here, only the positive half line cycle is examined since the operation is similar between the positive and negative half of the line cycle

$$\begin{cases} v_{\text{ac}} > 0 \Rightarrow d_{\text{low}} > d_{\text{high}} \\ v_{\text{ac}} < 0 \Rightarrow d_{\text{low}} < d_{\text{high}} \\ v_{\text{ac}} = 0 \Rightarrow d_{\text{low}} = d_{\text{high}}\,. \end{cases} \tag{1}$$

By setting d_1, d_2, d_3, and d_4 as the ratios of the respective time interval of each state S_1–S_4 shown in Fig. 7 over one switching period, d_{low} and d_{high} can be expressed as

$$d_{\text{low}} = d_2 + d_3 \tag{2}$$

$$d_{\text{high}} = d_3. \tag{3}$$

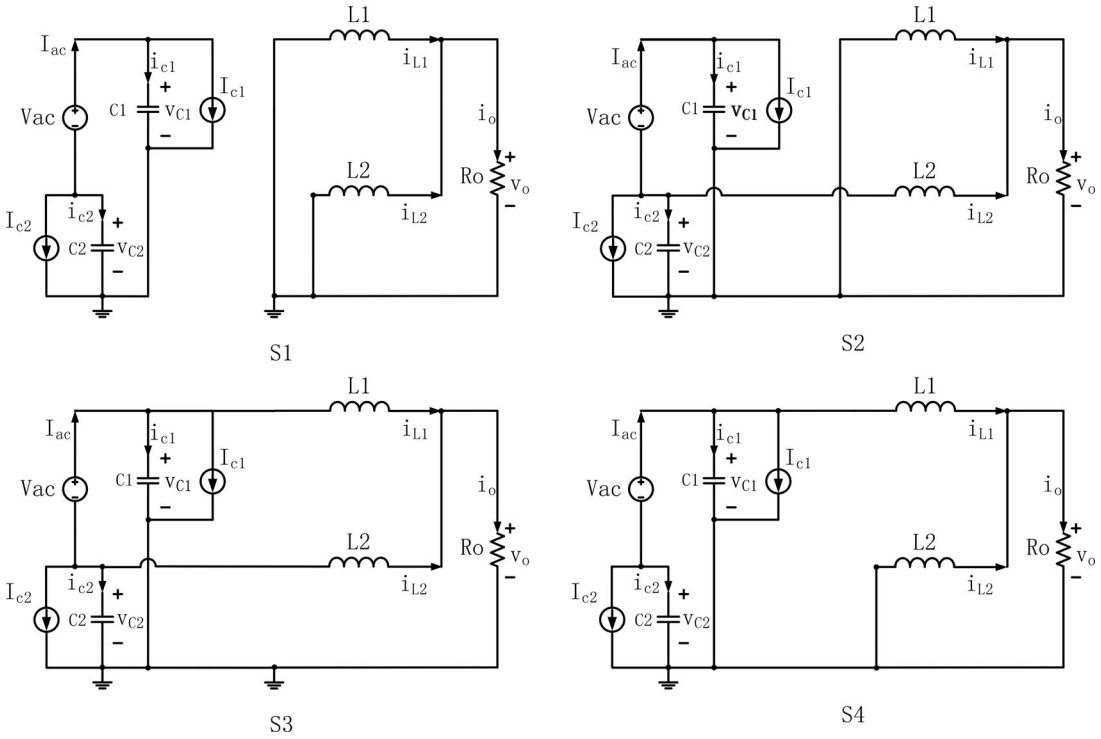


Fig. 5. Equivalent circuits of the buck differential rectifier in various operating states.

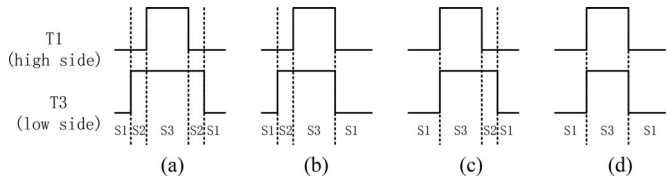


Fig. 6. Possible operation conditions during positive half-line cycle.

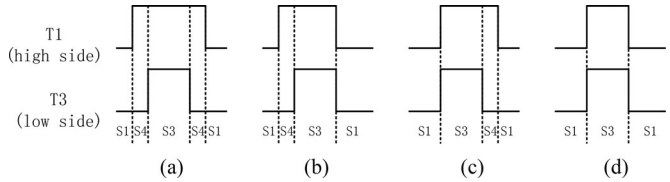


Fig. 7. Possible operation conditions during negative half-line cycle.

Assuming that the switching frequency is much higher than the line frequency, the input ac source during a switching cycle can be treated as a constant dc source. The symbol $v_{\rm ac}$ used in Fig. 4 is hence modified as $V_{\rm ac}$ in Fig. 5 to represent the dc source property over the switching cycle in which it is examined. Similarly, the ac line current over the switching cycle is assumed to be a dc current source $I_{\rm ac}$. With this consideration, the capacitor currents of C_1 and C_2 will each comprise two components, a high-frequency component (i_{C1} and i_{C2}, respectively), introduced by the switching dynamics, and a dc component (I_{C1} and I_{C2}) introduced by the ac source. In performing the control, the values for i_{C1} and i_{C2} will be determined by the waveform control method.

The state-space-averaged equation of the buck differential rectifier can be derived from Fig. 5 as

$$\begin{bmatrix} 0 \\ 0 \\ I_{C1} \\ I_{C2} \end{bmatrix} + \begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix}$$

$$= \begin{bmatrix} -R_o & -R_o & d_3 & 0 \\ -R_o & -R_o & 0 & d_2+d_3 \\ -d_3 & 0 & 0 & 0 \\ 0 & -(d_2+d_3) & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix}$$

$$+ \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} v_{\rm ac}(t) \\ i_{\rm ac}(t) \end{bmatrix} \tag{4}$$

where R_o is the load resistance, and i_{L1} and i_{L2} are the inductor currents.

The steady-state-averaged equation of the rectifier can be derived from (4), by setting $\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{dv_{C1}}{dt} = \frac{dv_{C2}}{dt} = 0$,

as

$$\begin{bmatrix} 0 \\ 0 \\ I_{C1} \\ I_{C2} \end{bmatrix} = \begin{bmatrix} -R_o & -R_o & D_3 & 0 \\ -R_o & -R_o & 0 & D_2+D_3 \\ -D_3 & 0 & 0 & 0 \\ 0 & -(D_2+D_3) & 0 & 0 \end{bmatrix} \times \begin{bmatrix} I_{L1}(t) \\ I_{L2}(t) \\ V_{c1}(t) \\ V_{c2}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} V_{\rm ac}(t) \\ I_{\rm ac}(t) \end{bmatrix} \tag{5}$$

where I_{L1}, I_{L2},, V_{C1}, V_{C2}, D_2, and D_3 are the steady-state values of i_{L1}, i_{L2}, v_{C1}, v_{C1}, d_2, and d_3.

By solving (5), V_{C1}, V_{C2}, I_{L1}, and I_{L2}, can be derived as

$$\begin{cases} V_{C1} = \dfrac{D_2+D_3}{D_2}V_{\rm ac} = \dfrac{D_{\rm low}}{D_{\rm low}-D_{\rm high}}V_{\rm ac} \\ V_{C2} = \dfrac{D_3}{D_2}V_{\rm ac} = \dfrac{D_{\rm high}}{D_{\rm low}-D_{\rm high}}V_{\rm ac} \\ I_{L1} = \dfrac{1}{D_3}(I_{\rm ac}-I_{C1}) = \dfrac{1}{D_{\rm high}}I_1 \\ I_{L2} = -\dfrac{1}{D_2+D_3}(I_{\rm ac}+I_{C2}) = \dfrac{1}{D_{\rm low}}I_2 \end{cases} \tag{6}$$

where I_1 and I_2 are the averaged input currents of the high side (i.e., T_1) and the low side (i.e., T_3) converters, respectively.

From (6), the averaged output current and voltage of the rectifier can be resolved as

$$\begin{cases} I_o = I_{L1}+I_{L2} = \dfrac{1}{D_{\rm high}}I_1 + \dfrac{1}{D_{\rm low}}I_2 \\ V_o = (I_{L1}+I_{L2})R_o = \left(\dfrac{1}{D_{\rm high}}I_1 + \dfrac{1}{D_{\rm low}}I_2\right)R_o. \end{cases} \tag{7}$$

It is found from (6) that V_{C1} and V_{C2} are coupled functions of $D_{\rm low}$ and $D_{\rm high}$. Therefore, if V_{C1} and V_{C2} are chosen as the control variables, the control is not straightforward since it involves the operation of both converters simultaneously. Here, $D_{\rm low}$ and $D_{\rm high}$ cannot be resolved explicitly with respect to V_{C1}, V_{C2}, and $V_{\rm ac}$ since there is no unique solution. Therefore, it is difficult to apply capacitor voltage waveform control.

On the other hand, inductor currents I_{L1} and I_{L2} are decoupled between the two converters and are independent functions of $D_{\rm low}$ and $D_{\rm high}$, as can be seen in (6). The duty cycles of the two converters can be easily resolved as

$$\begin{cases} D_{\rm low} = \dfrac{I_2}{I_{L2}} \\ D_{\rm high} = \dfrac{I_1}{I_{L1}}. \end{cases} \tag{8}$$

Therefore, by choosing I_{L1} and I_{L2} as control variables for the buck differential rectifier, the control becomes simple and straightforward as compared with the original capacitor–voltage waveform control [19] since the two current variables are fully decoupled from one another.

III. Application of the General Waveform Control Method to the Proposed Differential Rectifier

A. General Waveform Control Method

For the proposed differential rectifier system, a general waveform control technique for mitigating the double-line frequency power at the dc side of the circuit without using an E-cap, is proposed. This method is evolved from the work described in [20], which is originally developed for the full-bridge (boost-type differential) inverters. The waveform control method described here is general and applicable to any differential rectifier systems.

Traditionally, without waveform control, the two capacitor voltages are in the form of

$$v_{c1} = V_d + 0.5V_{\max}\sin(\omega t) \tag{9}$$

$$v_{c2} = V_d - 0.5V_{\max}\sin(\omega t). \tag{10}$$

Due to the differential connection of C_1 and C_2, their differential voltage is equal to the ac line voltage, i.e.,

$$v_{ac} = v_{c1} - v_{c2} = V_{\max}\sin(\omega t). \tag{11}$$

The dc output i_o will inevitably contain a significant level of double-line frequency current ripple $i_o(2\omega)$ as given in

$$i_o = I_o + i_{o(2\omega)}. \tag{12}$$

It is demonstrated in [20] that, given the operation waveforms described in (9) and (10), the two capacitors C_1 and C_2 do not contribute to the absorption of the double-line frequency power from the ac input, but serve only as high-frequency filters. By introducing a double-line frequency component to control v_{C1} and v_{C2}, C_1 and C_2 are able to additionally store the double-line pulsation power, thereby mitigating the double-line frequency ripple at the dc output.

Assuming that the input capacitor voltages are in the general form of

$$v_{c1} = V_d + kV_{\max}\sin(\omega t) + B\sin(2\omega t+\varphi) \tag{13}$$

$$v_{c2} = V_d + (k-1)V_{\max}\sin(\omega t) + B\sin(2\omega t+\varphi) \tag{14}$$

where *k* is the ratio of the amplitude of the line-frequency component for the high-side converter against the amplitude of the line voltage $V_{\max}$, and *B* is the amplitude of the double-line frequency components that are newly introduced into v_{C1} and v_{C2}. The double-line frequency components are injected differentially such that (11) is still satisfied.

The current flow into C_1 and C_2 can be derived, respectively, as

$$i_{c1} = C_1\frac{dv_{c1}}{dt} = kC_1\omega V_{\max}\cos(\omega t) + 2\omega C_1 B\cos(2\omega t+\varphi) \tag{15}$$

$$i_{c2} = C_2\frac{dv_{c2}}{dt} = (k-1)C_2\omega V_{\max}\cos(\omega t) + 2\omega C_2 B\cos(2\omega t+\varphi). \tag{16}$$

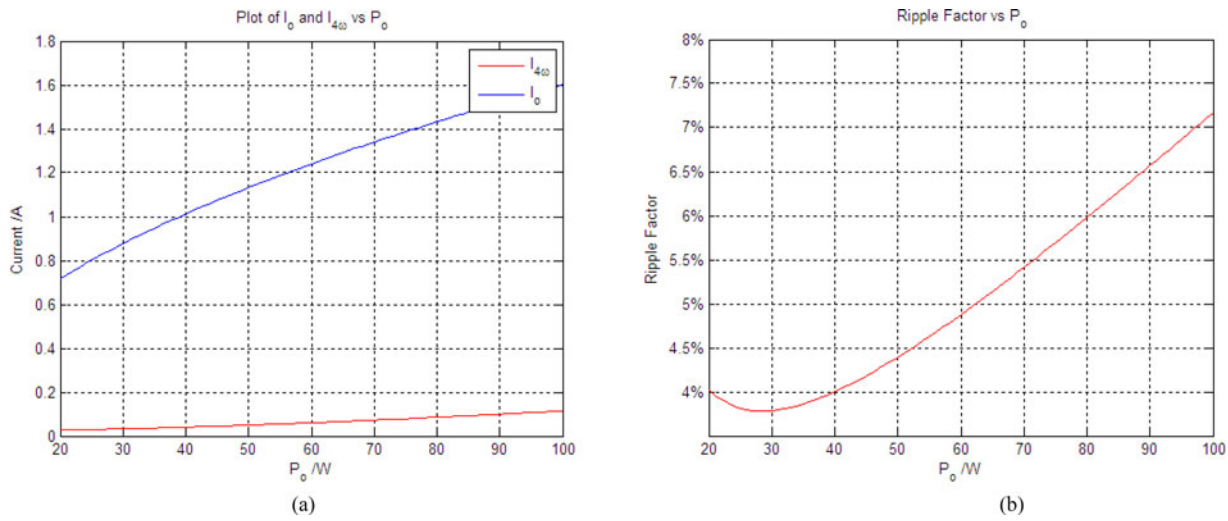


Fig. 8. Fourth-harmonic output current ripple analysis ($V_{\max} = 155.5$ V, $V_d = 200$ V, $C_1 = C_2 = 15\mu$F, and $R_o = 39\ \Omega$). (a) Averaged dc current I_o and ripple amplitude $I_{(4\omega)}$ versus output power P_o. (b) Ripple factor versus output power P_o.

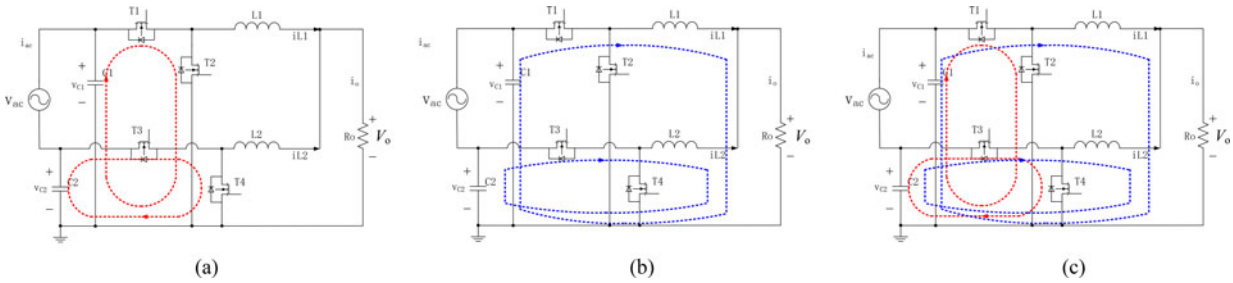


Fig. 9. Flow path of the current of double-line frequency power component in the proposed differential rectifier. (a) Through capacitors. (b) Through inductors. (c) Through capacitors and inductors.

The average input current of the converters in the rectifier can be derived as

$$i_1 = i_{ac} - i_{c1} = I_{\max}\sin(\omega t) - kC_1\omega V_{\max}\cos(\omega t) - 2\omega C_1 B\cos(2\omega t + \varphi) \quad (17)$$

$$i_2 = -i_{ac} - i_{c2} = -I_{\max}\sin(\omega t) - (k-1)C_2\omega V_{\max}\cos(\omega t) - 2\omega C_2 B\cos(2\omega t + \varphi) \quad (18)$$

where $I_{\max}$ is the peak amplitude of line current.

Assuming the converters to be lossless, the input power equals the output power, of which the inductor currents can be derived as

$$i_{L1} = \frac{i_1 \times v_{c1}}{V_o} = \frac{i_1}{d_{\text{high}}} \text{ and } i_{L2} = \frac{i_2 \times v_{c2}}{V_o} = \frac{i_1}{d_{\text{low}}}. \quad (19)$$

From (17)–(19), the total output current is given as

$$i_o = i_{L1} + i_{L2} = I_o + i_{o(\omega)} + i_{o(2\omega)} + i_{o(3\omega)} + i_{o(4\omega)} \quad (20)$$

where I_o is the dc component of total output current, and $i_{o(\omega)}$, $i_{o(2\omega)}$, $i_{o(3\omega)}$, $i_{o(4\omega)}$ are, respectively, the first-, second-, third-, and fourth-harmonic current components present in the total output current i_o. Detailed expressions of these components are given as follows:

$$I_o = \frac{I_{\max}V_{\max}}{2V_o} = \frac{P_{\text{ac\_avg}}}{V_o} \quad (21)$$

$$i_{o(\omega)} = [kC_1 - (1-k)C_2]\left(-\frac{\omega V_{\max}V_d}{V_o}\cos(\omega t) + \frac{\omega B V_{\max}}{2V_o}\sin(\omega t + \varphi)\right) \quad (22)$$

$$i_{o(2\omega)} = -\frac{I_{\max}V_{\max}}{2V_o}\cos(2\omega t) - \frac{2\omega B(C_1+C_2)V_d}{V_o} \times \cos(2\omega t + \varphi) - \left(k^2C_1 + (1-k)^2C_2\right)\frac{\omega V_{\max}^2}{2V_o}\sin(2\omega t) \quad (23)$$

$$i_{o(3\omega)} = [kC_1 - (1-k)C_2]\left(-\frac{3\omega V_{\max}B}{2V_o}\sin(3\omega t + \varphi)\right) \quad (24)$$

$$i_{o(4\omega)} = \frac{\omega B^2(C_1+C_2)}{V_o}\sin(4\omega t + 2\varphi) \quad (25)$$

where $P_{\text{ac\_avg}}$ is the average value of the source power.

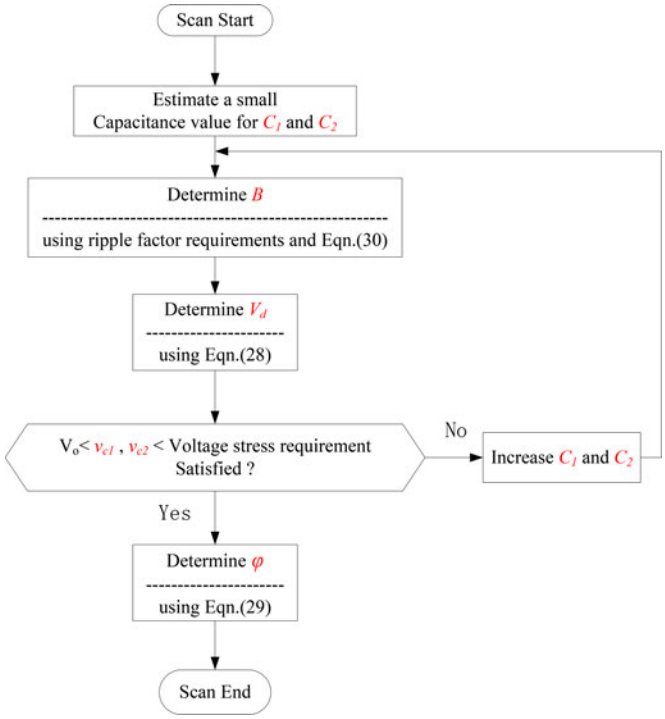


Fig. 10. Waveform control parameters determination flowchart using capacitor scanning.

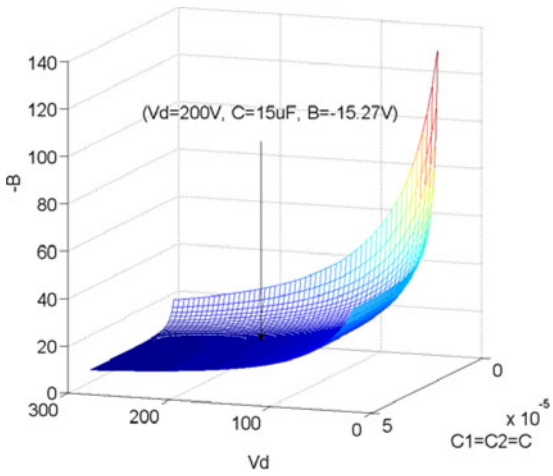


Fig. 11. Plot of C, B, and V_d (where $C = C_1 = C_2$) for a $P_o = 50$ W design that is based on (33).

Careful examination of (22) and (24) shows that $i_{o(\omega)}$ and $i_{o(3\omega)}$ will always be zero as long as

$$kC_1 = (1-k)C_2 \tag{26}$$

is satisfied.

Moreover, by equating $i_{o(2\omega)}$ in (23) to zero and combining it with (26), it can be derived that $i_{o(\omega)}$, $i_{o(2\omega)}$ and $i_{o(3\omega)}$ will be eliminated when (27) to (29) are complied

$$k = \frac{C_2}{C_1 + C_2} \tag{27}$$

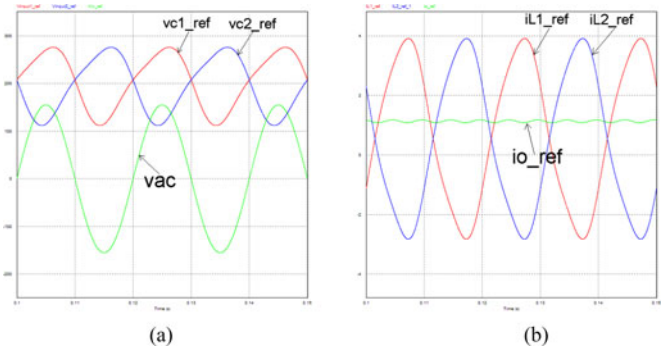


Fig. 12. Simulated reference voltage and current waveforms of the buck differential rectifier for $C_1 = C_2 = 15\,\mu$F, $P_o = 50$ W, $V_{\text{in}} = 110$ sin(ωt), $R_o = 39\,\Omega$.

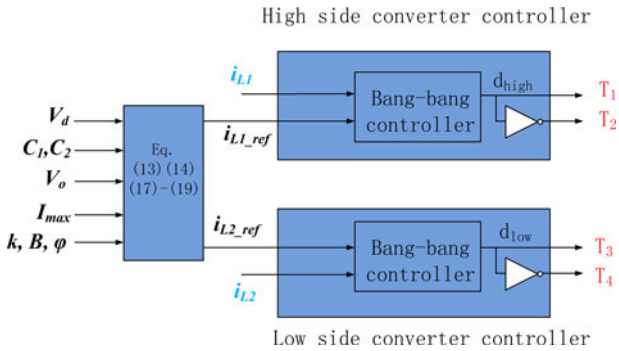


Fig. 13. Control blocks of the differential buck rectifier with a current bang–bang controller.

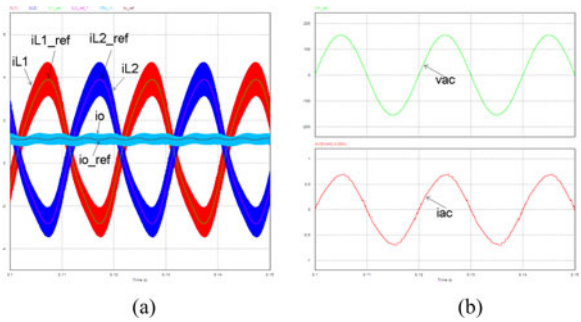


Fig. 14. Simulated operation waveforms of differential buck converter for $V_d = 200$ V, $P_o = 50$ W, $R_o = 39\,\Omega$.

$$B = -\frac{V_{\max}}{4\omega(C_1+C_2)V_d}\sqrt{I_{\max}^2 + (kC_1\omega V_{\max})^2} \tag{28}$$

$$\varphi = \frac{\pi}{2} - \sin^{-1}\frac{I_{\max}}{\sqrt{I_{\max}^2 + (kC_1\omega V_{\max})^2}}. \tag{29}$$

The component $i_{o(4\omega)}$ cannot be eliminated when only the double-line frequency component is introduced in the control of v_{C1} and v_{C2}. This component will eventually present as output current ripples. The ripple factor (which is the ratio of the current ripple amplitude over the dc averaged current) of output current can therefore be derived as shown in (30). Fig. 8 shows the calculated results of the ripple current amplitude $I_{(4\omega)}$, the

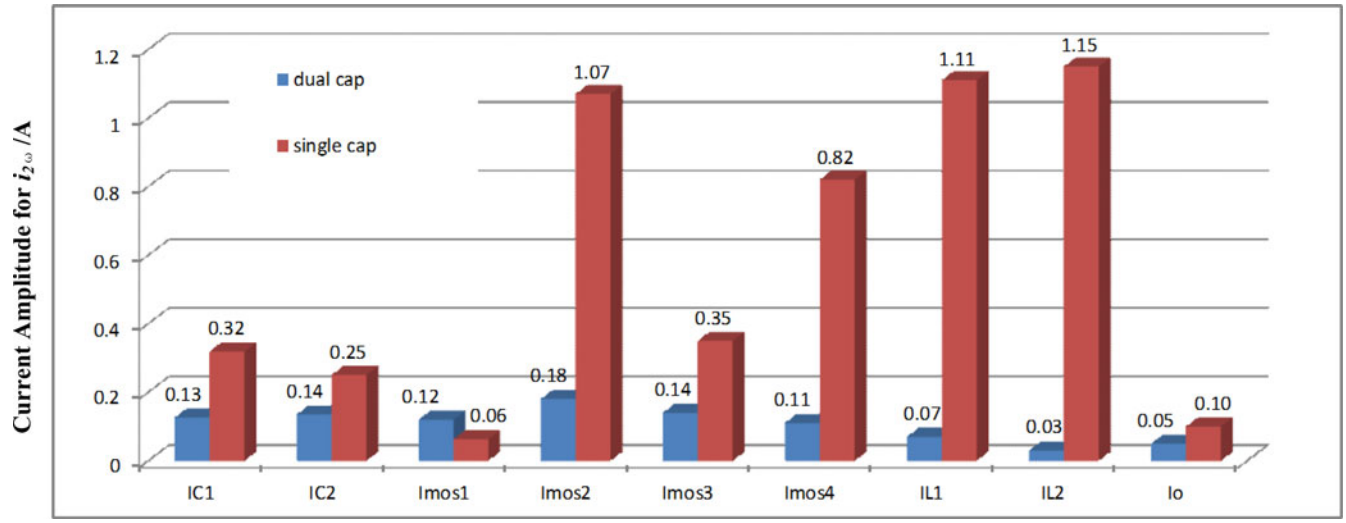


Fig. 15. Amplitude of double-line-frequency current component on the respective power devices for different combinations *of* C_1 and C_2 using waveform control (dual-cap case: $C_1 = C_2 = 15\ \mu$F, single-cap case: $C_1 = 0$, $C_2 = 30\ \mu$F).

averaged dc current I_o, and the ripple factor under the condition of $V_{\max} = 155.5$ V, $V_d = 200$ V, $C_1 = C_2 = 15\ \mu$F, and $R_o = 39\ \Omega$. It can be seen from Fig. 8(b) that the ripple factor is low over a wide power range. A more complicated form of v_{C1} and v_{C2} would be required for the full elimination of all the low-frequency ripples. However, this is often unnecessary since such ripples are normally very low. Therefore, with the proposed inductor-current waveform control method, only a small non-E-Cap is required for the dc output of the circuit

$$\text{factor}_{\text{ripple}}(i_o) = \frac{I_{4\omega}}{I_o} = \frac{2\omega B^2(C_1 + C_2)}{I_{\max} V_{\max}}. \tag{30}$$

It must be emphasized that the inductor-current waveform control method is applicable to the general family of differentially connected rectification systems (e.g., full-bridge or half-bridge topologies) for eliminating the dc-link E-Cap. Considering that many existing rectification systems have already been implemented with the full-bridge topologies, one immediate advantage of the proposed method is that, without any major hardware modification to the existing systems, the prolonging of the system's lifetime is possible with only a slight change of the control methodology.

B. Input Capacitors Optimization and Waveform Control Parameter Design

For the same system where the line voltage and current are the same, (27)–(29) indicate that a different combination of the input capacitors C_1 and C_2 will require different waveforms of v_{C1} and v_{C2}. From an efficiency viewpoint, the optimum selection of the input capacitors can be found by studying the flow path of the double-line frequency power component. Fig. 9 shows the three possible current flow paths of the double-line frequency power, i.e., either 1) through the capacitors, 2) the inductors, or, 3) both the inductors and capacitors. Since the inductors are usually more lossy than capacitors [19], it is preferable to have

TABLE II
SPECIFICATIONS OF BUCK DIFFERENTIAL RECTIFIER

Input line parasitic inductance	3.67 μH
Input voltage V_{ac} (RMS)	110 V
Output voltage V_o	43.6 V
Fundamental frequency f	50 Hz
Switch frequency f_s	around 50 kHz
Inductors (L_1, L_2)	600 μH, 6 A
Capacitors (C_1, C_2)	Dual cap case: $C_1 = C_2 = 15\ \mu$F, 600 V, film cap Single cap case: $C_2 = 30\ \mu$F, 600 V, film cap

the double-line frequency power flowing through the capacitors instead of the inductors. When the flow path in Fig. 9(a) is realized, no double-line frequency power flows through the inductors.

As L_1 and L_2 are placed on the dc side, the study of the double-line frequency power in the inductors is equivalent to the study of their respective double-line frequency current. From (19) and by considering (27)–(29), the double-line frequency content in the inductor currents can be derived as

$$i_{L1(2\omega)} = \left(\frac{C_1 - C_2}{C_1 + C_2}\right)\left(\frac{V_{\max} I_{\max}}{2V_o}\cos(2\omega t) + \frac{\omega V_{\max}^2 C_1 C_2/(C_1 + C_2)}{2V_o}\sin(2\omega t)\right) \tag{31}$$

$$i_{L2(2\omega)} = -\left(\frac{C_1 - C_2}{C_1 + C_2}\right)\left(\frac{V_{\max} I_{\max}}{2V_o}\cos(2\omega t) + \frac{\omega V_{\max}^2 C_1 C_2/(C_1 + C_2)}{2V_o}\sin(2\omega t)\right). \tag{32}$$

It is evident from (31) and (32) that the double-line frequency current component in the inductors will be simultaneously zero if C_1 and C_2 are equal. Otherwise, the double-line frequency

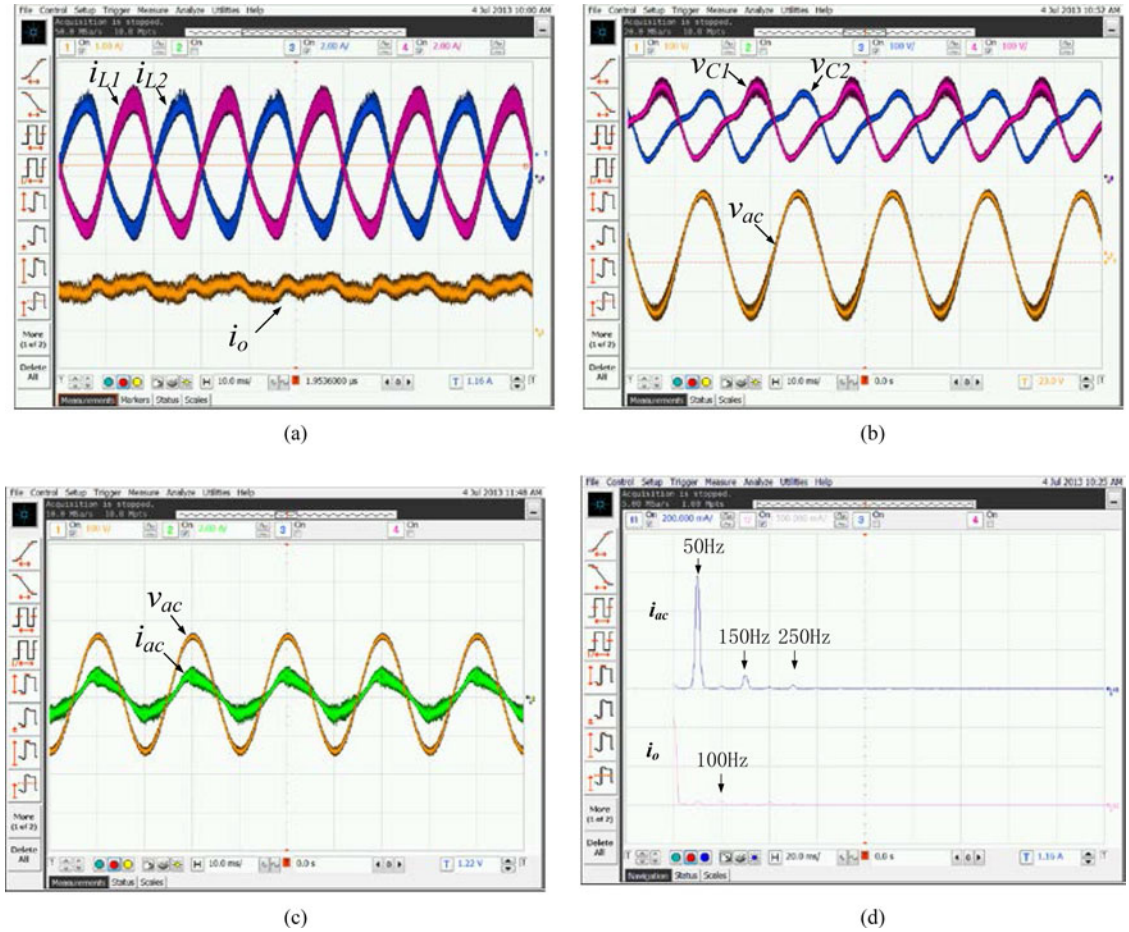


Fig. 16. Experimental results of differential buck converter with operating conditions $P_o = 50\,\mathrm{W}$, $R_o = 39\ \Omega$, $C_o = 0.47\ \mu\mathrm{F}$ for the dual-cap case of $C_1 = C_2 = 15\ \mu\mathrm{F}$. [(a) Inductor currents i_{L1} (pink), i_{L2} (blue) and output current i_o (orange), (b) v_{C1} (pink), v_{C2} (blue), v_{ac} (orange), (c) v_{ac} (orange), i_{ac} (green), (d) FFT analysis results for i_{ac} (orange) and for i_{o} (green). Scales: i_{L1}, i_{L2}: 2 A/div, i_o: 1 A/div, v_{C1}, v_{C2}, v_{ac}: 100 V/div, i_{ac}: 2 A/div, FFT for i_{ac}: 200 mA/div, FFT for i_o: 500 mA/div.

current component will flow through the inductors. If $C_1 = C_2 = C$, then *k, B,* and φ of (27)–(29) will be simplified as

$$k = \frac{1}{2} \tag{33}$$

$$B = -\frac{V_{\max}}{8V_d\omega C}\sqrt{I_{\max}^2 + \omega^2 C^2 V_{\max}^2/4} \tag{34}$$

$$\varphi = \sin^{-1}\frac{I_{\max}}{\sqrt{I_{\max}^2 + \omega^2 C^2 V_{\max}^2/4}} - \frac{\pi}{2}. \tag{35}$$

In this way, the double-line frequency power flow path described in Fig. 9(a) for reducing the conduction loss in the rectifier circuit will be realized, and a higher energy efficiency of the circuit can be obtained.

Once the optimal k parameter is determined, the optimal capacitance ratio is also derived, that is, $C_1 = C_2$. The capacitances of C_1 and C_2 should be selected in such a way that 1) the ripple factor defined in (30) satisfies the design criteria, e.g., less than 5%; 2) the capacitor voltages v_{C1} and v_{C2} in (13) and (14) are always higher than the output dc voltage V_o at all desired loading conditions, of which otherwise the two bidirectional buck converters cannot operate properly; 3) the peak value of v_{C1} and v_{C2} must be within acceptable range, e.g., within specified voltage stress range; and 4) the capacitance of C_1 and C_2 should be minimal such that the use of E-Cap in the circuit can be avoided.

Bearing in mind the above capacitor selection rules, the waveform control parameters can be designed through capacitor scanning using the flowchart shown in Fig. 10. First, estimate a small capacitor value for C_1 and C_2. Then, the maximum waveform parameter B is derived based on the ripple factor requirements according to (30). With the derived B and by using (28), parameter V_d can be determined. The capacitor voltage must fall within the limits of the output voltage and satisfy the voltage stress requirement. Otherwise, the capacitance is increased, and then, the calculation is repeated until a suitable value of the capacitance is found.

C. Simulation Verification

Based on (34), the parametric relationships of *C*, *B,* and V_d for a buck differential rectifier is derived and plotted as shown in Fig. 11 (assuming that $P_o = 50$ W, $v_{\mathrm{ac}} = 110\sqrt{2}\sin(2 * \pi * 50t)$ and $C_1 = C_2 = C$). Using the above capacitance

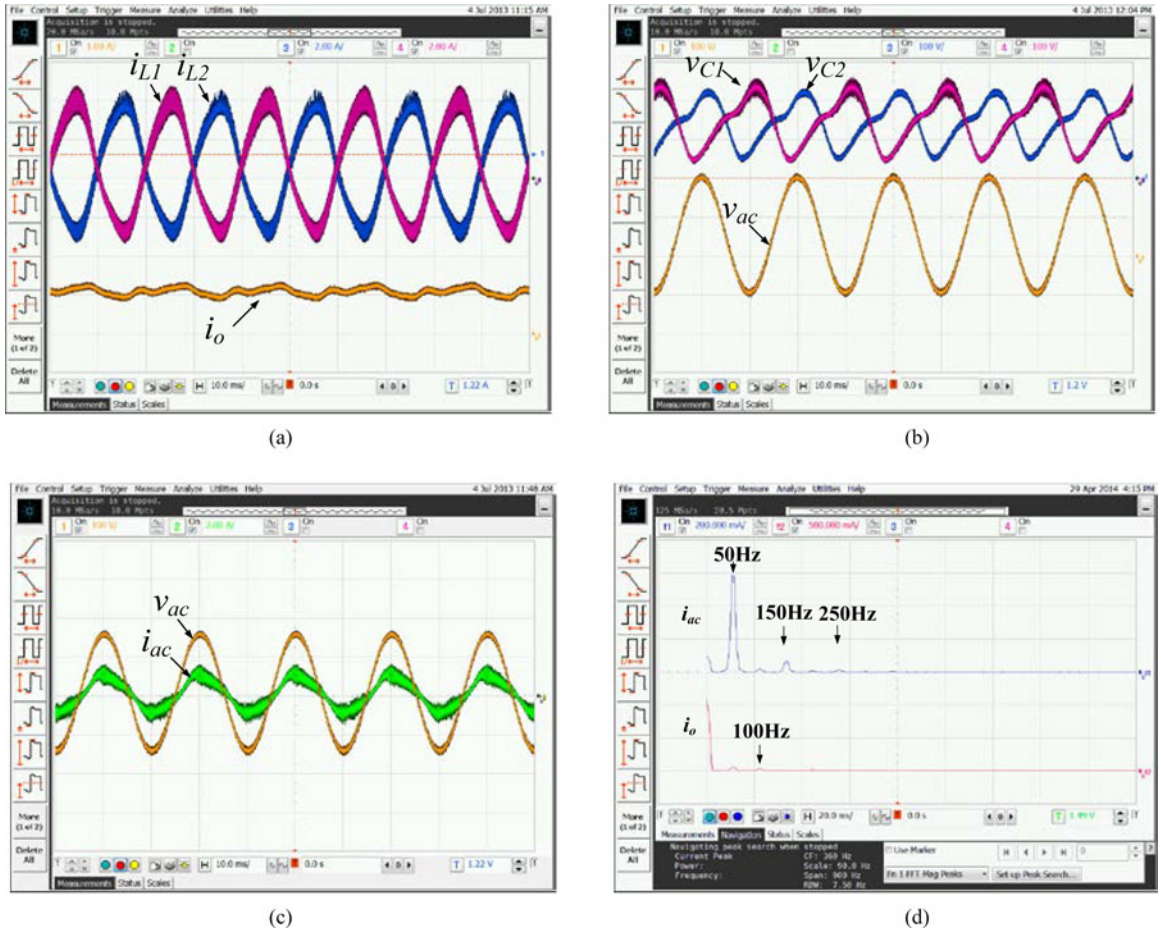


Fig. 17. Experimental waveforms of the differential buck converter with a resistive-capacitive load ($P_o = 50$ W, $R_o = 39\ \Omega$, $C_o = 47\ \mu$F, dual-cap case). [(a) inductor currents i_{L1} (pink), i_{L2} (blue) and output current i_o (orange). (b) v_{C1} (pink), v_{C2} (blue), $v_{\rm ac}$ (orange). (c) $v_{\rm ac}$ (orange), $i_{\rm ac}$ (green). (d) FFT analysis results for $i_{\rm ac}$ (orange) and for i_o (green). Scales: i_{L1}, i_{L2}: 2 A/div, i_o: 1 A/div, v_{C1}, v_{C2}, $v_{\rm ac}$: 100 V/div, $i_{\rm ac}$: 2 A/div, FFT for $i_{\rm ac}$: 200 mA/div, FFT for i_o: 500 mA/div]

selection rule and waveform control parameter design flowchart, the following parameters are chosen and applied in this study: $C_1 = C_2 = C = 15\,\mu$F, $k = 0.5$, $V_d = 200$ V, $B = -15.27$ V, and $\varphi = 0.52$ rad. The voltages across C_1 and C_2 are, respectively

$$v_{c1} = 200 + 77.78\sin(\omega t) - 15.27\sin(2\omega t - 0.52) \quad (36)$$

$$v_{c2} = 200 - 77.78\sin(\omega t) - 15.27\sin(2\omega t - 0.52). \quad (37)$$

Similarly, the inductor currents and output current can be derived from (19) and (20). The simulated reference and expected waveforms of v_{C1}, v_{C2}, i_{L1}, i_{L2}, and I_o for operating the rectifier with the waveform control are recorded in Fig. 12.

From Fig. 12(a), it is shown that the ac content of v_{C1} and v_{C2} are clearly of a distorted form, but their differential value is still the ac line voltage. From Fig. 12(b), it is shown that the low-frequency ac components of i_{L1} and i_{L2} cancel out with one another, leading to the output current i_o containing only a small portion of the low-frequency content. The amplitude of the ripple current i_o is 4.43% (0.05 A) of the average dc current (1.13 A) and is in good agreement with the calculated results shown in Fig. 8. This is in contrast to i_o that is achievable by traditional means without waveform control [refer to (12)], where the ripple amplitude is 100% (1.13 A) of the average dc current. The low-frequency ripple has been suppressed almost 23 times with the inclusion of waveform control.

Given the inductor current references in Fig. 12, two simple bang–bang controllers are then employed for regulating the inductor currents. The control blocks are shown in Fig. 13, and the simulated waveforms of the differential buck rectifier are shown in Fig. 14. As illustrated in Fig. 14(a), i_{L1} and i_{L2} are capable of tracking their respective references. The simulated output current ripple amplitude of i_o is 0.3 A, which is 27% of the average dc current of 1.13 A. It should be noted that no output capacitor is used in the system, and most of the presented ripples are actually of high-frequency content, which can be easily filtered out using an output high-frequency filter if desired. Fig. 14(b) shows the input voltage and current waveforms. A sinusoidal ac current in phase with the input line voltage is observed.

The flow of the double-line frequency current components through all devices is analyzed. The results are presented in Fig. 15. It is clear that when $C_1 = C_2$, the double-line frequency current flows mainly through C_1 and C_2, and T_1-T_4.

A small amount of $i_{L1(2\omega)}$ and $i_{L2(2\omega)}$ still exists due to control imperfection.

A different set of simulation with $C_1 = 0$, $C_2 = 30$ μF (known as single-cap case) is conducted to demonstrate the effectiveness of optimizing the capacitor combination. From (27)–(29), the waveform parameters are determined as $k = 1$, $B = -13.26$ V, $V_d = 200$ V, and $\varphi = 0$. The associated double-line frequency currents are presented in Fig. 15. The double-line frequency current flows through every device but with a higher amplitude in C_1, C_2, T_2, T_3, T_4, L_1, and L_2 than those of the dual-cap case. Higher values of $i_{L1(2\omega)}$ and $i_{L2(2\omega)}$ imply more double-line frequency power flowing through the inductors and therefore a higher power loss and lower energy efficiency of the circuit.

IV. Experimental Validation

A. Experimental Setup

A prototype of the buck differential rectifier with the waveform control and conduction loss reduction is constructed and tested. The design of the rectifier which comprises two buck converter follows that of conventional PFC buck converter design principles, but with a smaller input voltage range. To avoid obscuring the essential of this paper which is on the waveform control method, the design details of the differential rectifier will be omitted. Table II gives the rectifier's specifications. LABVIEW is used to calculate and generate the desired inductor current reference signals according to (19) based on the optimal values of *k*, *B*, and φ. Two hysteresis controllers are used to independently control i_{L1} and i_{L2} such that the respective references are tracked. It will be shown that with the proposed waveform control method, a direct ac/dc differential rectifier with mitigated double-line frequency ripple on the dc side can be realized. It must be emphasized that no E-cap is used in the experimental setup. For the dual-cap experiment ($C_1 = C_2 = 15$ μF), the adopted parameters are $k = 0.5$, $V_d = 200$ V, and $B = -15.27$ V, and $\varphi = 0.52$. For single-cap experiment ($C_1 = 0, C_2 = 30$ μF), the parameters are $k = 1$, $V_d = 200$ V, $B = -13.26$ V, and $\varphi = 0$.

B. With Resistive and Resistive-Capacitive Load (Dual-Cap Case)

Fig. 16(a)–(c) shows the measured voltage and current waveforms of the proposed buck differential rectifier in a dual-cap configuration, with the waveform control and operating at 50-W output, with a pure resistive load of $R_o = 39$ Ω. In this experiment, R_o is connected in parallel with a very small capacitor ($C_o = 0.47$ μF) to filter the high-frequency switching ripple. The capacitor does not affect the dominant resistive property of the load.

Fig. 16(a) shows the waveforms of i_{L1} and i_{L2}, and the output current i_o, which is the sum of i_{L1} and i_{L2}. With the proposed waveform control, the low-frequency current ripple at the dc output is substantially mitigated. The amplitude of output current ripple is 0.27 A (23% of average (dc) output current 1.15 A. The result is similar with that obtained in simulation (27%).

TABLE III
RMS Current in Components for Different C_1 and C_2 Combinations ($P_o = 50$ W)

	L_1	L_2	T_1	T_2	T_3	T_4	C_1	C_2
Dual-cap case (A)	2.43	2.43	1.15	2.14	1.15	2.14	0.52	0.52
Single-cap case (A)	2.57	2.23	1.07	2.34	1.1	1.9	0	0.91

TABLE IV
Current Stress on Power Devices for Different C_1 and C_2 Combinations ($P_o = 50$ W)

	T_1	T_2	T_3	T_4
Dual-cap case (A)	4.68	4.71	4.68	4.71
Single-cap case (A)	6.06	6.1	4.7	4.7

Fig. 16(b) shows the waveforms of v_{C1}, v_{C2}, and $v_{\rm ac}$. Since no direct capacitor voltage regulation is employed, the dc component of v_{C1} and v_{C2} presents some deviation from the expected value of V_d, which is attributed by the power losses of the converters. The results will be improved if a voltage regulation controller is applied, by which means the averaging voltage of v_{C1} and v_{C2}, that is V_d, can be regulated. Fig. 16(c) and (d) shows the waveforms of $v_{\rm ac}$, $i_{\rm ac}$, and the FFT spectrum of the line ($i_{\rm ac}$) and the output current (i_o), respectively. It is shown that a good PF with low-harmonic contents is achieved. Line current contains negligible (2.69%) 100-Hz (second harmonic) current component and 11.9% of the third-harmonic current component. The measured total harmonic distortion of the input current is 10.45% with a PF of 0.97. These measurements are within the limit of Class C regulation. It should be noted that only a small input filter is included in the circuit since C_1 and C_2 are adequate to filter the high-frequency content in $i_{\rm ac}$. For output current $i_{\rm o}$, the 100 Hz content is only 4.2% of the average current.

Fig. 17 shows the operation waveforms of the rectifier with a resistive-capacitive load ($R_o = 39$ Ω, $C_o = 47$ μF). Compared with the results given in Fig. 16, similar operating waveforms have been captured. With increased output capacitance, the output current ripple, especially the high-frequency components, has been further suppressed.

C. Comparative Study of Different Input Capacitors Combination

Another set of experiment with $C_1 = 0$ and $C_2 = 30$ μF (single-cap case) is carried out to validate the result of input capacitor optimization. Table III illustrates the measured *RMS* current of the inductors L_1 and L_2, capacitors C_1 and C_2, and the four active switches with an output power of 50 W. It can be seen that i_{L1} and i_{L2} in the single-cap case are 2.57 and 2.23 A, respectively; while they are both 2.43 A in the dual-cap case.

Table IV shows the current stress of various switches for both cases. Theoretically, the current stress of T_1 and T_2, as well as T_3 and T_4 should be the same. The tiny current stress differences in Table IV are mainly caused by measurement inaccuracy. It is

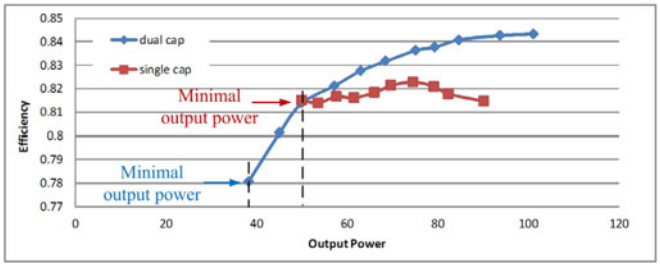


Fig. 18. Efficiency comparison between dual-cap case and single-cap case.

found that the single-cap case has a higher current stress on T_1 and T_2 than the dual-cap case. In the dual-cap case, the current stress has been suppressed by more than 22.7% (1.39 A). Also, the stress is more evenly distributed among all switches than in the single-cap case.

Finally, the system efficiency curves of both cases are compared and are shown in Fig. 18. It is observed that when the output power level is higher than 50 W, the dual-cap case has a higher energy efficiency than the single-cap case. The improvement in efficiency increases as the power level goes higher. When the output power is below 50 W, it is found that the single-cap case cannot function properly since there are instances when the input capacitor voltages v_{c1} and v_{C2} are lower than the expected output voltage, as have been discussed in Section III-B. Different capacitance and waveform parameters must be selected for the differential rectifier to operate below 50 W. For a detailed design flowchart, refer to Section III-B. As for dual-cap case, however, a wider operation range has been observed.

V. Conclusion

A type of E-cap-less ac/dc differential rectifier system with current-waveform control technique is proposed in this paper for direct rectification applications. The configuration is based on a structure of having two bidirectional dc/dc converters in series-input and parallel-output connections. To complement the feature of this rectifier configuration, waveform control is applied to mitigate the double-line frequency current ripple of the dc output, thereby allowing the removal of the electrolytic storage capacitor that is typically required in such systems. Mathematical derivations and analysis are provided in the paper to validate the concept, using the buck differential rectifier as a case study example. Moreover, the conduction loss of double-line frequency power flow can be minimized through parameter optimization. Experimental results show that the idea is feasible and workable for this configuration. The idea of the direct ac/dc differential rectifier is extendable to other combination of converters, connected differentially, with or without galvanic isolation, for single phase or multiphase applications.

References

[1] S. Wang, X. Ruan, K. Yao, S.-C. Tan, Y. Yang, and Z. Ye, "A flicker-free electrolytic capacitor-less AC–DC LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4540–4548, Nov. 2012.

[2] T. Shimizu, T. Fujita, G. Kimura, and J. Hirose, "A unity power factor PWM rectifier with DC ripple compensation," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 447–455, Aug. 1997.

[3] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[4] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1419–1429, Sep./Oct. 2000.

[5] K.-H. Chao, P.-T. Cheng, and T. Shimizu, "New control methods for single phase PWM regenerative rectifier with power decoupling function," in *Proc. Int. Conf. Power Electron. Drive Syst.*, 2009, pp. 1091–1096.

[6] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[7] W. Chen and S. Hui, "Elimination of an electrolytic capacitor in ac/dc light-emitting diode (LED) driver with high input power factor and constant output current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1598–1607, Mar. 2012.

[8] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 89–95.

[9] Y. Tang, F. Blaabjerg, and P. C. Loh, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 96–102.

[10] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[11] R. Wang, F. Wang, D. Boroyevich, R. Burgos, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[12] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less ac–dc drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592–601, Mar. 2010.

[13] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of eliminating electrolytic capacitor in ac/dc power supplies for LED lightings," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1399–1408, May 2009.

[14] X. Ruan, B. Wang, K. Yao, and S. Wang, "Optimum injected current harmonics to minimize peak-to-average ratio of LED current for electrolytic capacitor-less ac–dc drivers," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1820–1825, Jul. 2011.

[15] Y. Qin, H. Chung, D. Y. Lin, and S. Y. R. Hui, "Current source ballast for high power lighting emitting diodes without electrolytic capacitor," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, 2008, pp. 1968–1973.

[16] S. Y. Hui, S. N. Li, X. H. Tao, W. Chen, and W. M. Ng, "A novel passive offline LED driver with long lifetime," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2665–2672, Oct. 2010.

[17] W. Chen, S. N. Li, and S. Y. R. Hui, "A comparative study on the circuit topologies for offline passive light-emitting diode (LED) drivers with long lifetime and high efficiency," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 724–730.

[18] S. Y. (Ron) Hui and Y. X. Qin, "A general photo-electro-thermal theory for light emitting diode (LED) systems," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1967–1976, Aug. 2009.

[19] G.-R. Zhu, S.-C. Tan, Y. Chen, and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 779–792, Feb. 2013.

[20] I. E. Colling and I. Barbi, "Reversible unity power factor step-up/step-down AC-DC converter controlled by sliding mode," *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 223–230, Mar. 2001.

Sinan Li (M'14) was born in China, in 1986. He received the B.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2009, and the Ph.D. degree in electrical and electronic engineering from the University of Hong Kong, Hong Kong, China, in 2014.

He is currently a Research Associate with the Department of Electrical and Electronic Engineering, The University of Hong Kong. His research areas include the design and analysis of power supplies, especially interested in LED systems design and system reliability.

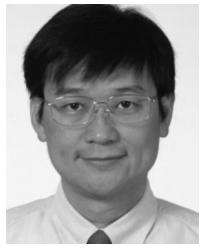
Dr. Li is one of the Founding Members of IEEE-Eta Kappa Nu (HKN) at HKU.

Guo-Rong Zhu (M'11) was born in Hunan, China. She received the Ph.D. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2009.

From 2002 to 2005, she was a Lecturer at the School of Electrical Engineering, Wuhan University of Science and Technology, Wuhan. From 2009 to 2011, she was a Research Assistant/Research Associate in the Department of Electronic and Information Engineering, the Hong Kong Polytechnic University, Kowloon, Hong Kong. She is currently an Associate Professor at the School of Automation, Wuhan University of Technology, Wuhan. Her main research interests include the power electronic converter topologies, soft-switching techniques, low-frequency ripple mitigation techniques, battery management system of hybrid electric vehicles and renewable energy system.

Siew-Chong Tan (S'00–M'06–SM'11) received the B.Eng. (Hons.) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, Singapore, in 2000 and 2002, respectively, and the Ph.D. degree in electronic and information engineering from the Hong Kong Polytechnic University, Hong Kong, in 2005.

From October 2005 to May 2012, he worked as a Research Associate, Postdoctoral Fellow, Lecturer, and Assistant Professor at the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong. From January to October 2011, he was a Senior Scientist in Agency for Science, Technology and Research (A*Star), Singapore. He is currently an Associate Professor in the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong. He was a Visiting Scholar at the Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, Champaign, from September to October 2009, and an Invited Academic Visitor of the Huazhong University of Science and Technology, Wuhan, China, in December 2011. His research interests include power electronics and control, LED lightings, smart grids, and clean energy technologies. He serves extensively as a Reviewer for various IEEE/IET transactions and journals on power, electronics, circuits, and control engineering. He is a coauthor of the book *Sliding Mode Control of Switching Power Converters: Techniques and Implementation* (Boca Raton, FL, USA: CRC Press, 2011).



S. Y. (Ron) Hui (M'87–SM'94–F'03) received the B.Sc. (Eng.) (Hons.) degree from the University of Birmingham, Birmingham, U.K., in 1984, and the D.I.C. and Ph.D. degrees from Imperial College London, London, U.K., in 1987.

He has previously held academic positions at the University of Nottingham (1987–1990), University of Technology Sydney (1991–1992), University of Sydney (1992–1996), City University of Hong Kong (1996–2011). Since July 2011, he has been holding the Chair Professorship at the University of Hong Kong, Hong Kong. Since July 2010, he has been concurrently holding the Chair Professorship at Imperial College London. He has published more than 200 technical papers, including more than 150 refereed journal publications and book chapters. More than 50 of his patents have been adopted by industry.

Dr. Hui is a Fellow of the IET. He has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1997 and an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since 2007. He has been appointed twice as an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2004 and 2006. He served as one of the 18 Administrative Committee members of the IEEE Power Electronics Society and was the Chairman of its Constitution and Bylaws Committee from 2002 to 2010. He received the Excellent Teaching Award at CityU in 1998 and the Earth Champion Award in 2008. He received an IEEE Best Paper Award from the IEEEIAS Committee on Production and Applications of Light in 2002, and two IEEE Power Electronics Transactions Prize Paper Awards for his publications on Wireless Charging Platform Technology in 2009 and on LED system theory in 2010. His inventions on wireless charging platform technology underpin key dimensions of Qi, the world's first wireless power standard, with freedom of positioning and localized charging features for wireless charging of consumer electronics. In November 2010, he received the IEEE Rudolf Chope R&D Award from the IEEE Industrial Electronics Society, the IET Achievement Medal (The Crompton Medal) and was elected to the Fellowship of the Australian Academy of Technological Sciences & Engineering.