<table>
<thead>
<tr>
<th><strong>Title</strong></th>
<th>Fast Transistor-Level Circuit Simulation and Variational Analysis via the Ultra-Compact Virtual Source Model</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Author(s)</strong></td>
<td>Zhang, Y; Chen, Q; Wong, N</td>
</tr>
<tr>
<td><strong>Citation</strong></td>
<td>The IEEE 10th International Conference on ASIC (ASICON), Shenzhen, China, 28-31 October 2013. In IEEE International Conference on ASIC Proceedings, 2013, p. 1-4</td>
</tr>
<tr>
<td><strong>Issued Date</strong></td>
<td>2013</td>
</tr>
<tr>
<td><strong>URL</strong></td>
<td><a href="http://hdl.handle.net/10722/204033">http://hdl.handle.net/10722/204033</a></td>
</tr>
<tr>
<td><strong>Rights</strong></td>
<td>IEEE International Conference on ASIC Proceedings. Copyright © IEEE.</td>
</tr>
</tbody>
</table>
Fast Transistor-Level Circuit Simulation and Variational Analysis via the Ultra-Compact Virtual Source Model

[Invited Special Session Paper]1
Yang Zhang, Quan Chen and Ngai Wong

Department of Electrical and Electronic Engineering, The University of Hong Kong
{yzhang, quanchen, nwong}@eee.hku.hk

Abstract—Virtual source (VS) transistor model surpasses the existing threshold-voltage-based and surface-potential-based models in terms of compactness, featuring an order of magnitude fewer parameters while maintaining the same accuracy. This brings about significant simulation speedup and improved ease in variational analyses. This paper demonstrates, for the first time, the quadratic linearization of a VS model into an equivalent state-space form of nonlinear differential algebraic equations. Such transformation allows fast transistor-level analog circuit simulation utilizing nonlinear model order reduction (NMOR) techniques. Moreover, device-to-system-level variational analysis is largely facilitated via the integration of parameterized NMOR and stochastic spectral collocation methods. Experimental results then verify the efficacy of the proposed macromodeling approach.

I. INTRODUCTION

Conventional transistor compact models include the threshold-voltage-based BSIM and PTM models, as well as the surface-potential-based PSP model. As technology nodes shrink into the nanometer era, the number of parameters in these models can easily exceed hundreds to incorporate the emerging physics and to achieve smooth transitions across different operating regions. Such high number of parameters lead to elevated complexity in data storage and simulation. To overcome this hurdle, the ultra-compact charge-based virtual source (VS) model is proposed [2] which contains parameters in the order of only a few tens. Such model is specifically developed for short- and ultra-short-channel devices by replacing the drift-diffusion (with velocity saturation) transport description with quasi-ballistic minority carrier transport at the virtual source.

On the other hand, a pressing issue in nanometer chip design is to quantify the propagating effects of device-level variations to the circuit or system level. For instance, as device size shrinks, the threshold voltage uncertainty becomes prominent and limits the supply voltage scaling. To characterize process uncertainties, a stochastic transistor-level simulator, such as a Monte Carlo simulator, is required. Despite the implementation simplicity, Monte Carlo simulators generally suffer from slow convergence. Even with smart sampling schemes, a large number of transistor-level simulations are still required at different sample points.

The purpose of this paper is to study the efficient use of VS model in capturing analog circuits. A key innovation is to recognize the analytic form (namely, exponential and polynomial functions) in the VS formula, which lends itself naturally to elegant differential algebraic equation (DAE) representation called the quadratic-linear DAE (QLDAE) [1]. Once this QLDAE is formulated, nonlinear model order reduction (NMOR) (e.g., [3]) can then be applied to produce a reduced-order model (ROM) for fast simulation. Moreover, when variational analysis is needed, parameterized NMOR (PNMOR) techniques and state-of-the-art spectral methods are handy for the QLDAE-transformed VS model to achieve speedy device-to-system-level uncertainty capture.

The paper is organized as follows. Section II succinctly reviews the analytic tools, viz. the VS model and QLDAE. Section III presents the main results by casting the VS equations into QLDAE and subjecting it to NMOR and PNMOR. In PNMOR, stochastic spectral methods are deployed for fast uncertainty analyses. Section IV verifies the effectiveness of the proposed framework by examples. Finally, Section V draws the conclusion.

II. BACKGROUND

A. VS MOSFET Model

For MOSFETs, the I-V characteristics over all regions of operation can be described by the single VS model [2]

\[
I_D = W Q_{i\theta} v_{F \theta} F_s,
F_s = \frac{V_{DS}}{V_{DSAT}} \left(1 + \frac{V_{DS}}{V_{DSAT}}\right)^{1/\beta},
Q_{i\theta} = C_{inv} n_{\phi i} \ln \left(1 + \exp \frac{V_{DS} - (V_T - \alpha\phi_i F_s)}{n_{\phi i}}\right),
V_{DSAT} = V_{DSAT,0} (1 - F_f) + \phi_i F_f,
F_f = \frac{1}{1 + \exp \left(\frac{V_{DS} - (V_T - \alpha\phi_i F_s)/n_{\phi i}}{\alpha_{\phi i}}\right)},
V_T = V_{T0} - \delta V_{DS},
\]

where \(I_D\) is the drain current, \(W\) the device width, \(Q_{i\theta}\) the channel charge density, \(v_{F \theta}\) the virtual source velocity, \(F_s\) the
carrier velocity saturation function, \(V_{\text{DSAT}}\) the saturation voltage, \(V_{\text{DSAT}}\) in strong inversion, \(\beta\) a saturation-transition-region fitting parameter and \(C_{\text{inv}}\) the effective gate-to-channel capacitance per unit area. \(n\) is the subthreshold coefficient, which is related to the subthreshold swing \(S\) by \(S = n\varphi_t \ln 10\). \(\varphi_t\) is the thermal voltage, \(V_{\text{TH}}\) the strong-inversion threshold voltage, \(\delta\) the drain-induced barrier lowering (DIBL) coefficient. \(\alpha\) is a constant accounting for the shift of threshold voltage in strong and weak inversion. \(F_f\) gives a smooth transition between these two values. \(V_{\text{DS}}'\) and \(V_{\text{GS}}'\) are the effective drain-source and gate-source voltages depending on the source and drain resistances. Most of these equations are strongly nonlinear posing difficulties to traditional NMOR, for which QLDAE comes to rescue.

B. QLDAE

QLDAE is a systematic way to allow the Volterra method, previously applied to mostly weakly nonlinear systems, to capture also strong nonlinearities with low-order models. For generic electrical circuits, a QLDAE takes the form [5]

\[
C\ddot{x} = G_1 x + G_2 x \otimes x + D_1 x u + bu,
\]

where \(x \in \mathbb{R}^n\) is the state vector and \(\otimes\) denotes the Kronecker product. All other matrices are of compatible dimensions and a scalar input \(u\) is assumed for notational ease whose multi-input multi-output (MIMO) generalization is trivial. The idea in QLDAE is simple: extra state variables are introduced to describe the self-referential derivatives of common electrical nonlinearities (e.g., sinusoidal and exponential functions) or represent algebraic substitutions (e.g., polynomial fractions and high-order monomial terms). For example, the fifth equation in (1) can be converted into

\[
x_k = \frac{1}{1 + x_{k+1}} \Rightarrow 0 = x_k + x_k x_{k+1} - 1,
\]

\[
\dot{x}_{k+1} = x_{k+1} - \frac{1}{\alpha \varphi_t} \left( \dot{x}_{k+2} - \ddot{x}_{k+3} \right),
\]

in which,

\[
x_k = F_f, \quad x_{k+1} = \exp\left( \frac{V_{\text{GS}} - (V_T - \alpha \varphi_t/2)}{\alpha \varphi_t} \right),
\]

\[
x_{k+2} = V_{\text{GS}}, \quad x_{k+3} = V_T.
\]

With the QLDAE transformation, any composite function of the above nonlinear responses, as is obvious in the VS model, can be similarly transformed into a QLDAE at the expense of additional state variables.

III. MAIN RESULTS

The QLDAE-transformed VS model largely facilitates direct deployment of NMOR and PNMOR techniques for fast transient simulation and variational analysis of transistor circuits. In particular, instead of using the full-scale interconnected VS models, we employ the post-NMOR QLDAE ROM to accelerate transient computation. Moreover, PNMOR is realized by reserving a portion of the state variable entries as parametric constants (i.e., with zero derivative) that can be subject to spectral methods for variational analysis.

A. System QLDAE generation

An analog circuit is first subject to QLDAE conversion of its nonlinear elements, and connected to the remaining linear part (if any) to produce a full-system QLDAE. Some parameters of the VS model are obtained by device measurements or data fitting, and are classified as variational due to the fabrication process. In order to perform variational analysis, these parameters are marked as adjustable in the ROM. One new approach proposed in this work is to designate all VS parameters as extra state variables. In other words, besides the routine QLDAE conversion, variational device parameters are also members of the state variables in the QLDAE system. Compared to the usually numerous state variables from linear networks, the order increase from the incorporation of variational parameters is insignificant, and is subject to further reduction as will be discussed later.

![Fig. 1. State vectors assignment in QLDAE.](image)

In traditional analog circuit MOR, a system is partitioned into linear and nonlinear parts. Only the linear part is processed by MOR and the nonlinear parts are unaltered. The drawback of this approach is the I/O ports at linear/nonlinear interfaces have to be kept and multi-port MOR is known to be inefficient. In the proposed NMOR flow, the linear and nonlinear subsystems are encapsulated in a single QLDAE, and therefore the explicit interfacing of linear and nonlinear subsystems are completely omitted to ease subsequent MOR and variational analysis. Fig. 1 illustrates the proposed state vector assignment.

B. NMOR

By the MOR algorithm in [3] called NORM, the original system (2) can be reduced into

\[
\ddot{C}z = \dot{G}_1 z + \dot{G}_2 z \otimes z + \dot{D}_1 z u + \dot{b} u,
\]

in which \(z \in \mathbb{R}^{n'}, \dot{C} \in \mathbb{R}^{n' \times n'}, \dot{G}_1 \in \mathbb{R}^{n' \times n'}, \dot{G}_2 \in \mathbb{R}^{n' \times n'}, \dot{D}_1 \in \mathbb{R}^{n' \times n'}\), and \(\dot{b} \in \mathbb{R}^{n'}\), where usually \(n' \ll n\). Since all variational parameters are embedded into state variables, they become transparent to external interfacing of the ROM. The NMOR is a one-off process (i.e., a finite overhead) whereas
the ROM can be used recurrently, resulting in overall saving in transient simulation.

In transient simulation, a variable-step time-domain solver is developed based on Runge-Kutta implicit method and step size adjustment mechanism. The step size is determined by keeping the numerical errors within a preset tolerance. It should be noted that these errors come from the replacements of original nonlinear functions by their self-referential derivatives during the QLDAE transformation. This is the main difference of the proposed QLDAE solver compared to a typical DAE solver. And the variational analysis can be performed on this solver with greatly reduced computation time and guaranteed numerically accuracy.

C. PNMOR with SSCM

To avoid the extensive repeated simulations in traditional Monte-Carlo-type circuit simulators for capturing the propagation of device variations to the circuit or system level, we adopt the sparse grid (SG) based stochastic spectral collocation method (SG-SSCM) [6]. SG-SSCM normally consists of three steps. In the first step the set of variational parameters \( P \), if stochastically correlated, is reduced to a set of \( D \) (\( D \leq \text{size}(P) \)) independent normal random variables \( \xi \) by the Karhunen-Loeve (K-L) expansion. Then a specific circuit- or system-level quantity of interest \( Y \) (for instance the output amplitude of an amplifier) is expressed as

\[
Y(\tilde{\xi}) \approx \sum_{|i|=0}^{k} a_{i_1,...,i_D} H_{i_1,...,i_D}(\tilde{\xi}),
\]

where \( i \) is a \( D \)-digit multi-index and \( |i| = i_1 + \ldots + i_D \). \( H_{i_1,...,i_D}(\tilde{\xi}) \) is a \( D \)-variable polynomial chaos constructed according to the probability density function (PDF) of \( Y \) [4]. The coefficients of the expression are determined by the approximated form of \( D \)-dimensional infinite integration

\[
a_{i_1,...,i_D} = \sum_{n=1}^{N_{\text{sg}}} Y(\tilde{\xi}^{(n)}) H_{i_1,...,i_D}(\tilde{\xi}^{(n)}) w^{(n)},
\]

with \( \tilde{\xi}^{(n)} \in \Theta_D, w^{(n)} \in W_D^2 \), where \( \Theta_D \) and \( W_D^2 \) are the sets of the \( N_{\text{sg}} \) sampling points and selected weights.

In (7), one \( Y \) is obtained for each sampling point by simulating the QLDAE-reduced VS model using a specific combination of parameters determined by \( \tilde{\xi}^{(n)} \). In other words, the QLDAE model is treated as a black-box solver and requires no alteration for variational analysis. Therefore, the benefits of an accelerated transient simulation resulting from the QLDAE reduction in Section 3.2 can be fully exploited. Once the coefficients \( a_{i_1,...,i_D} \) are determined, statistical moments of interest, such as mean and variance of \( Y \), can be computed in simple closed forms

\[
\mu_Y = a_{0,...,0},
\]

\[
\sigma^2_Y = \sum_{|i|=1}^{k} a_{i_1,...,i_D}^2 \left( H_{i_1,...,i_D} \right)^2.
\]

The algorithmic flow of SG-SSCM is summarized in Fig. 2.

IV. EXAMPLES

A. Single standard cell

A simple circuit example is in Fig. 3(a) wherein the NMOS transistor is described by the VS model. The power supply is 1.2V and other components are all normalized to unity.

The QLDAE-transformed model has 58 state variables, which can be reduced to 18 by the NORM method. By the variable-step QLDAE solver, the original and reduced models match extremely well in transient simulation as shown in Fig. 4 under three different \( V_{TH} \) values.

B. CMOS opamp

A CMOS opamp with schematic in Fig. 3(b) (the linear parts are not shown), is simulated by the proposed approach. The nonlinear circuit consists of 9 transistors taking up only a small
portion of the entire system (the remaining parts are linear), which is typical in analog/RF circuit design. Specifically, the dimension of the whole QLDAE system is 1726, whereby 526 state variables correspond to the QLDAE conversion of nonlinear transistors and 1200 variables are from the linear network. The NORM-reduced ROM has only 546 variables. Transient simulations by the original and ROM with different parameter values are in good agreement as shown in Fig. 5.

![Simulation results of the CMOS opamp circuit.](image)

**Fig. 5. Simulation results of the CMOS opamp circuit.**

C. Results for PNMOR

To demonstrate the capability of QLDAE model in analyzing the propagation of device-level variations to circuit level, we integrate the QLDAE-reduced VS model developed in Section 3.2 with SG-SSCM to estimate the variations of output voltage amplitude (related to the output power) of the above two amplifiers subject to parametric variations. Three VS model parameters, namely, threshold voltage $V_{T0}$, saturation-transition-region fitting parameter $\beta$ and subthreshold swing $S$, are assumed to have random variations with independent Gaussian distribution with mean values $\mu_{V_{T0},\beta,S} = [0.4, 1.8, 0.1]$. A standard deviation of 10% mean value is assumed for each variational parameter.

Table I compares the mean and standard deviation of the output amplitude computed by Monte Carlo simulation with 5000 runs and SG-SSCM. The latter achieves a comparable accuracy with the former while reducing the number of required sampling points by two orders. It also shows that the output amplitude variation of the 9-transistor amplifier is more significant than that of the 1-transistor example given the same degree of variations in individual transistors, explicitly verifying the accumulating and propagating effects of device-level variations to higher levels. The cumulative density function (CDF) plot of the CMOS opamp example is shown in Fig. 6, in which the curves from Monte Carlo and SG-SSCM are in good agreement.

**TABLE I**

| Variation of output amplitude estimated by Monte Carlo and SG-SSCM ($\mu_{V_{T0},\beta,S} = [0.4, 1.8, 0.1]$, $\sigma_{V_{T0},\beta,S} = 0.1\mu_{V_{T0},\beta,S}$). |
|---|---|---|---|---|---|
| | Monte Carlo | | | SG-SSCM | |
| | mean | std | samples | mean | std | samples |
| Amplifier | | | | | | |
| Opamp | 0.11 | 0.0010 | 5000 | 0.11 | 0.0011 | 25 |

![CDF plot of output amplitude of the CMOS opamp example.](image)

**Fig. 6. CDF plot of output amplitude of the CMOS opamp example.**

V. Conclusion

This paper has proposed and demonstrated for the first time the innovative transformation of the ultra-compact VS transistor model into an equivalent set of nonlinear DAEs, thereby largely speeding up the simulation of analog circuit modules through NMOR techniques. Efficient capture of the propagation of device-level uncertainties to the circuit and system levels has also been enabled via the integration of parametric NMOR and stochastic spectral methods. Numerical examples have confirmed the efficacy of the proposed approach.

**ACKNOWLEDGMENTS**

This work was supported in part by the Hong Kong Research Grant Council, under projects GRF HKU 718711E and AoE/P-04/08, and by the University Research Committee of The University of Hong Kong.

**REFERENCES**


