



Title	On Energy Efficiency of Switched-Capacitor Converters
Author(s)	Cheung, CK; Tan, SC; Tse, CK; Ioinovici, A
Citation	IEEE Transactions on Power Electronics , 2013, v. 28 n. 2, p. 862-876
Issued Date	2013
URL	http://hdl.handle.net/10722/196280
Rights	IEEE Transactions on Power Electronics . Copyright © Institute of Electrical and Electronics Engineers.

On Energy Efficiency of Switched-Capacitor Converters

Chun-Kit Cheung, *Student Member, IEEE*, Siew-Chong Tan, *Senior Member, IEEE*, Chi K. Tse, *Fellow, IEEE*, and Adrian Ioinovici, *Fellow, IEEE*

Abstract—The energy-efficiency issue of switched-capacitor converters is still a controversial topic that requires a more in-depth discussion. In this paper, we address the issue by dividing the analysis of the entire efficiency problem into two parts. In the first part, the efficiency of a capacitor-charging RC circuit under different aspects (partial charging, full charging, at zero capacitor voltage, at nonzero capacitor voltage, etc.) will be conducted. The efficiency analysis of a capacitor-discharging RC circuit with a resistor, capacitor, and paralleled resistor–capacitor loads will be covered. A complete evaluation of the overall efficiency is then performed in terms of both the charging and discharging efficiencies. Based on the analysis, some design rules useful for developing high-efficiency switched-capacitor converters is suggested. Additionally, it is shown that the belief that quasi-switched-capacitor converters are more lossy than switched-capacitor converters is a common misconception.

Index Terms—Charging efficiency, discharging efficiency, flying capacitor, full charging, full discharging, partial charging, partial discharging, quasi-switched-capacitor (QSC) converter, switched-capacitor (SC) converter.

I. INTRODUCTION

SWITCHED-CAPACITOR (SC) converters have the advantages of small size, lightweight, and high-power density due to the absence of magnetic components, which make them suitable for use in portable electronics like cellular phones, digital cameras, and MP3 players [1]. With the increasing demand for smaller and lighter power converters, semiconductor companies are introducing new and more advanced types of SC converters in IC packages, such as MAX5008 and LM2758, for commercial applications.

Within the research domain of SC converters, energy efficiency is still a frequently discussed and debated issue among researchers [1]–[40]. Careful review of the literature shows that there are still many conflicting viewpoints and inconsistencies.

Manuscript received January 12, 2012; revised April 2, 2012 and June 1, 2012; accepted June 1, 2012. Date of current version September 27, 2012. Recommended for publication by Associate Editor M. Vitelli.

C.-K. Cheung and C. K. Tse are with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong (e-mail: ckcheung@eie.polyu.edu.hk; encktse@polyu.edu.hk).

S.-C. Tan is with the Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam, Hong Kong (e-mail: sctan@eee.hku.hk).

A. Ioinovici was with the Holon Institute of Technology, Holon, Israel. He is now with the National Center for Power Electronics and Energy, Guangzhou, China (e-mail: adrian@hit.ac.il).

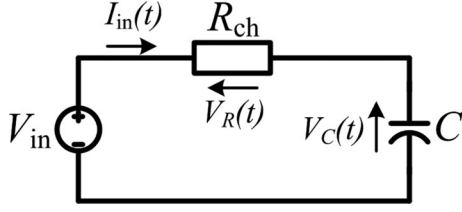
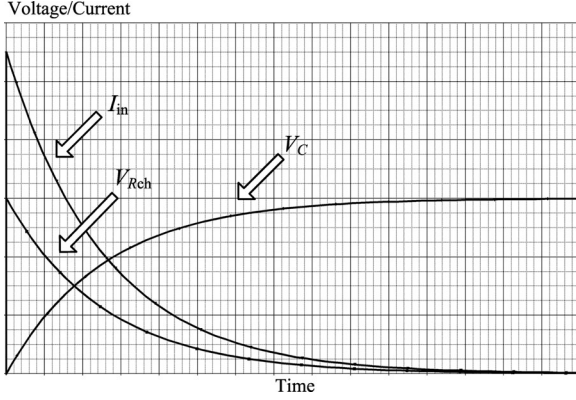
Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2012.2204903

For example, in [20], it is claimed that higher efficiency could be obtained by reducing the turn-on resistance $R_{DS(on)}$ of the power MOSFETs. In [21], it is emphasized that the insertion of a series current-sensing resistor could result in large power loss. In [22] and [23], it is realized that the switching loss will limit the overall energy efficiency. Moreover, in [24], it is argued that operating the power MOSFET of an SC converter in the saturation region so that the MOSFET serves as a constant current source and the converter operates as a quasi-switched-capacitor (QSC) converter [25], [26], will cause the converter to become highly inefficient. In [27], a resonant switched-capacitor converter, which is basically an SC converter with a small inductor included to create a zero-current switching condition so that switching loss can be reduced, is proposed.

On the other hand, in an attempt to rebut some of the claims, the discussion in [28] has revisited a number of issues. First, the overall efficiency of SC converters is resistance independent and is solely dependent on the input voltage, output voltage, and the conversion ratio n . Second, the efficiency of QSC converters is the same as that of the conventional SC converter. Yet, in [29], it is suggested that the SC converter efficiency is bounded by the expression given in [1] and [28], but will be lower if switching loss is included. Also, the theoretical work in [30] revealed that the overall converter efficiency will degrade with the increase of parasitic resistances. Furthermore, against conventional understanding that power loss is caused mainly by resistance and hard-switching actions, there are controversial claims that a bigger capacitance and a higher switching frequency can improve the overall efficiency of SC converters [31]–[33]. In [34] and [35], it is suggested that the application of the interleaved discharging and variable switching frequency can improve the power efficiency of SC converters. Finally, while many power-electronics practitioners still believe that SC converters are a class of highly inefficient converters, the IC manufacturing companies are contradicting this belief by producing SC converter ICs of an extremely high efficiency of up to 98% (LM2660).

In this paper, we attempt to address these issues altogether, by systematically analyzing from a circuit and then a system perspective, the efficiency of each individual component of the RC circuit, in the charging operation, the discharging operation, and then the entire charging-discharging operation so that a complete picture of the efficiency issue of the SC converter can be revealed. The analysis takes into consideration the different possible operating conditions, and highlights the main impacts on efficiency. In Section II, the efficiency analysis of a capacitor-charging RC circuit under different conditions will be conducted. In Section III, the charging efficiency and the possible

Fig. 1. Equivalent RC circuit of the charging process.Fig. 2. Simulated instantaneous current I_{in} , capacitor voltage V_C , and resistor voltage V_{Rch} waveforms in a full-charging process.

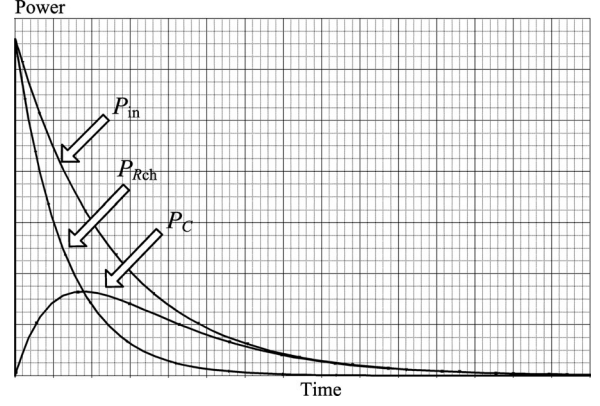
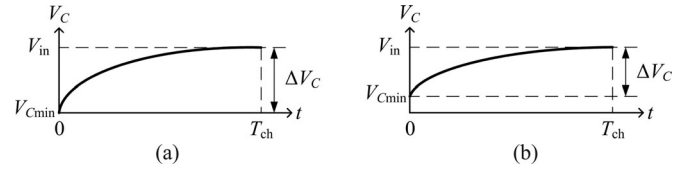
control methods of QSC converters will be discussed. In Section IV, the power loss distribution of resistors in a capacitor-charging RC circuit will be discussed. Then, in Section V, the efficiency analysis of a discharging RC circuit with resistor, capacitor and paralleled resistor-capacitor loads will be included. In Section VII, the derivation of the overall efficiency in terms of both the charging and discharging efficiencies is given. Finally, a summary of the major understandings and some design rules that are useful for achieving high efficiency in SC converters is given in Section VIII.

II. EFFICIENCY OF RC CHARGING CIRCUITS

In SC converters, the charging circuit contains only power switches and flying capacitors, which can be represented by an RC circuit [36], [37] (see Fig. 1). R_{ch} denotes the total equivalent resistance in the charging path and it is made up of the equivalent series resistance (ESR) of the capacitors R_{ESR} , the turn-on resistance of the power MOSFETs $R_{DS(on)}$, and an equivalent resistance representing the switching loss of the power MOSFETs R_{SW} . Figs. 2 and 3 show the simulated instantaneous voltages and current, and the power waveforms of the RC charging circuit, respectively. The instantaneous voltages and current can be given by

$$\begin{cases} V_C(t) &= (V_{in} - V_{Cmin})(1 - e^{-\frac{t}{R_{ch}C}}) + V_{Cmin} \\ V_{Rch}(t) &= V_{in} - V_C(t) \\ I_{in}(t) &= \frac{V_{in} - V_{Cmin}}{R_{ch}} \left(e^{-\frac{t}{R_{ch}C}} \right). \end{cases} \quad (1)$$

The energy profile and efficiency of this circuit can be classified into two categories, namely, full charging and partial charging.

Fig. 3. Simulated instantaneous power of the input voltage source P_{in} , capacitor P_C , and resistor P_{Rch} of a full-charging process.Fig. 4. Capacitor voltage waveform of a full-charging process with (a) zero initial capacitor voltage and (b) nonzero initial capacitor voltage. (a) $V_{Cmin} = 0$ V and (b) $0 < V_{Cmin} < V_{in}$.

In this paper, full charging is defined as one that has a charging time period longer than four times the charging time constant, i.e., $T_{ch} \geq 4\tau_{ch}$, and partial charging corresponds to $T_{ch} < 4\tau_{ch}$, where $\tau_{ch} = R_{ch}C$.

A. Efficiency of Full-Charging RC Circuit

In full charging, the capacitor is charged to the value of the input voltage, i.e., $V_{Cmax} = V_{in}$ regardless of its initial condition. The energy profile and the charging efficiency over a charging cycle can be expressed as

$$\begin{cases} \Delta E_C &= \int_0^{T_{ch}} V_C(t) \cdot I_{in}(t) dt = \frac{C}{2} (V_{in}^2 - V_{Cmin}^2) \\ \Delta E_{Rch} &= \int_0^{T_{ch}} V_{Rch}(t) \cdot I_{in}(t) dt = \frac{C}{2} (V_{in} - V_{Cmin})^2 \\ \Delta E_{in} &= \int_0^{T_{ch}} V_{in} \cdot I_{in}(t) dt = CV_{in} (V_{in} - V_{Cmin}) \end{cases} \quad (2)$$

$$\eta_{ch(full)} = \frac{\Delta E_C}{\Delta E_{in}} = \frac{1}{2} \left(1 + \frac{V_{Cmin}}{V_{in}} \right). \quad (3)$$

The charging process can start with two different initial conditions, i.e., zero [see Fig. 4(a)] or nonzero [see Fig. 4(b)] initial capacitor voltage, respectively.

For $V_{Cmin} = 0$ V, the charging efficiency is 50% and is independent of resistance R_{ch} in the charging path, as discussed in [28] and [38]. However, for $V_{Cmin} > 0$ V, the charging efficiency will be greater than 50%. From (3), a high charging efficiency is obtained by keeping V_{Cmin} close to V_{in} .

B. Efficiency of Partial-Charging RC Circuit

In partial charging, the capacitor is charged to a voltage less than the input voltage, i.e., $V_{Cmax} < V_{in}$. The energy profile

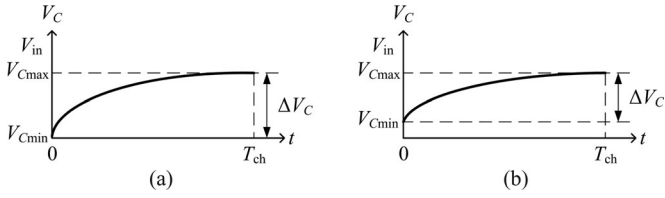


Fig. 5. Capacitor voltage waveform of a partial-charging process with (a) zero initial capacitor voltage and (b) nonzero initial capacitor voltage. (a) $V_{C\min} = 0$ V and (b) $0 \text{ V} < V_{C\min} < V_{in}$.

and charging efficiency over a charging cycle are, respectively

$$\begin{cases} \Delta E_C &= \int_0^{T_{ch}} V_C(t) \cdot I_{in}(t) dt = \frac{C}{2} (V_{C\max}^2 - V_{C\min}^2) \\ \Delta E_{R_{ch}} &= \int_0^{T_{ch}} V_{R_{ch}}(t) \cdot I_{in}(t) dt \\ &= \frac{C}{2} [(V_{in} - V_{C\min})^2 - (V_{in} - V_{C\max})^2] \\ \Delta E_{in} &= \int_0^{T_{ch}} V_{in} \cdot I_{in}(t) dt = CV_{in}(V_{C\max} - V_{C\min}) \end{cases} \quad (4)$$

$$\eta_{ch(\text{partial})} = \frac{\Delta E_C}{\Delta E_{in}} = \frac{1}{2} \left(\frac{V_{C\min} + V_{C\max}}{V_{in}} \right) \approx \frac{\overline{V_C}}{V_{in}}. \quad (5)$$

Similar to full charging, partial charging can start with a zero [see Fig. 5(a)] or nonzero [see Fig. 5(b)] initial capacitor voltage. According to (5), for $V_{C\min} = 0$ V, the charging efficiency is always less than 50% and it increases with an increasing $V_{C\max}$. For $V_{C\min} > 0$ V, a high charging efficiency can be achieved by keeping $(V_{in} - V_{C\min})$ and $(V_{in} - V_{C\max})$ small. For the same purpose, $\Delta V_C (= V_{C\max} - V_{C\min})$ should be small. From (3) and (5), some key points can be summarized.

- 1) The charging efficiency is independent of R_{ch} in the charging path. R_{ch} affects only the time constant τ_{ch} of the charging circuit, and the instantaneous peak current value of the charging response. Doubling the value of R_{ch} will reduce the peak of the charging current to half, while the charging duration will be doubled with $V_{C\max}$ unchanged [see Fig. 6(a) and (b)]. Experimental charging current waveforms of two RC charging circuits with different values of R_{ch} (0.3 and 0.4 Ω) are shown in Fig. 7(a) and (b). Time duration for the capacitor to be fully charged (charging current reached zero) is longer for the case of larger R_{ch} . Additionally, the peak value of the charging current can be expressed as $\frac{V_{in} - V_{C\min}}{R_{ch}}$. With the same value of V_{in} and $V_{C\min}$ in both circuits, the peak charging current is larger for the case of smaller R_{ch} . However, the energy dissipated in R_{ch} in both RC circuits are the same. Therefore, a larger R_{ch} suppresses the peak current value while lengthening the charging duration with no penalty on the charging efficiency (by keeping the same desired final voltage on the flying capacitor), which is consistent with the discussion in [33].
- 2) The instantaneous powers of the two charging circuits with different R_{ch} , as shown in Fig. 6(a) and (b), are not the same. However, both circuits have the same average power loss since the energy loss over the switching period will be the same in steady state.

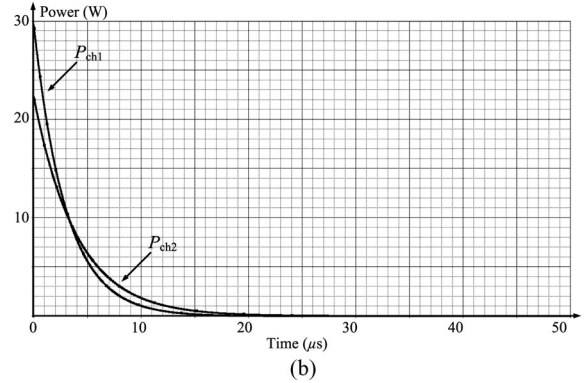
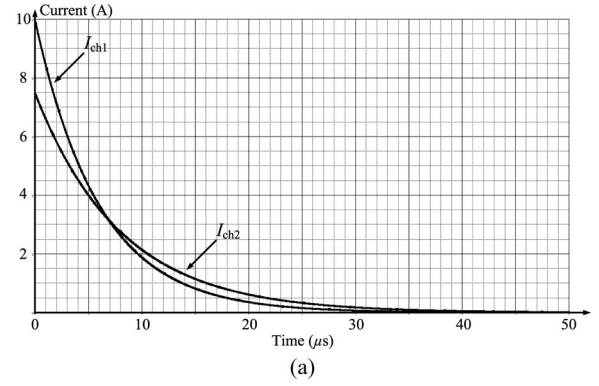


Fig. 6. Instantaneous (a) charging current and (b) power dissipated on R_{ch} of two different RC charging circuits, ch1 and ch2 (ch1: $V_{in} = 12$ V, $R_{ch} = 0.3$ Ω , $C = 20$ μF , $\tau_{ch3} = 6$ μs , $V_{C\min} = 9$ V; ch2: $V_{in} = 12$ V, $R_{ch} = 0.4$ Ω , $C = 20$ μF , $\tau_{ch3} = 8$ μs , and $V_{C\min} = 9$ V).

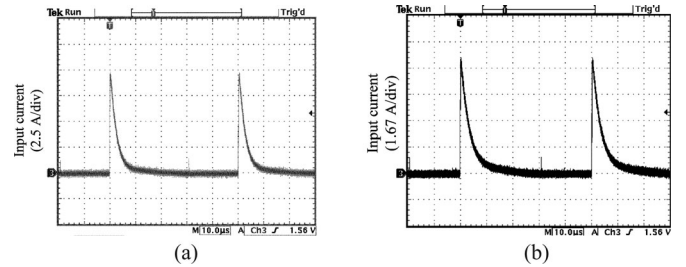


Fig. 7. Experimental results of instantaneous charging current on two different RC charging circuits: (a) ch1 and (b) ch2.

- 3) A charging efficiency of 50% appears only in full charging when $V_{C\min} = 0$ V. An efficiency lower than 50% occurs in partial charging when $V_{C\min} + V_{C\max} < V_{in}$.
- 4) A higher charging efficiency is obtained when ΔV_C is smaller and/or when $\overline{V_C}$ is nearer to V_{in} .
- 5) The charging duration should be increased for getting the same desired $V_{C\max}$ if the charging resistance is increased, while the charging efficiency is still maintained. However, there are still practical limits to achieve the aforementioned condition. For an SC converter operating at a fixed switching frequency, the maximum charging time should be less than the switching period. For variable frequency control, the increase in the charging time requires the reduction of the switching frequency, but the switching frequency has a practical lower limit.

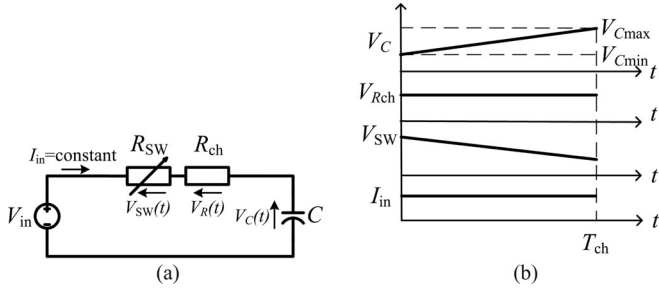


Fig. 8. (a) Equivalent charging circuit of a QSC converter and (b) its theoretical voltage and current waveforms.

III. CHARGING EFFICIENCY OF QSC CONVERTERS AND BASICS OF THEIR CONTROLS

A. Charging Efficiency Analysis

For QSC converters, the MOSFET switch in the charging path is operated in the active region such that the converter behaves like a constant current source [25], [26]. This is possible via the control of the gate voltage of the switch. Theoretically, the control of current flow through the switch is equivalent to the control of its internal resistance. Hence, to have a constant current I_{in} flowing through the RC circuit from a constant voltage source while the capacitor voltage is linearly increasing, the resistance of the switch R_{SW} should be time varying. Fig. 8(a) shows the equivalent charging circuit of the QSC converter. The theoretical voltage and current waveforms are given in Fig. 8(b). The instantaneous voltages and current, energy profile and the charging efficiency of QSC converters over a charging cycle can be expressed as

$$\begin{cases} V_C(t) = \frac{V_{C_{max}} - V_{C_{min}}}{T_{ch}}(t) + V_{C_{min}} \\ V_{R_{ch}}(t) = I_{in} \cdot R_{ch} \\ V_{SW}(t) = I_{in} \cdot R_{SW}(t) \\ I_{in}(t) = I_{in} \end{cases} \quad (6)$$

$$\begin{cases} \Delta E_C = \int_0^{T_{ch}} V_C(t) \cdot I_{in} dt = \frac{C}{2}(V_{C_{max}}^2 - V_{C_{min}}^2) \\ \Delta E_{(R_{ch}+R_{SW})} = \int_0^{T_{ch}} (V_{R_{ch}}(t) + V_{SW}(t)) \cdot I_{in} dt \\ = \frac{C}{2}[(V_{in} - V_{C_{min}})^2 - (V_{in} - V_{C_{max}})^2] \\ \Delta E_{in} = \int_0^{T_{ch}} V_{in} \cdot I_{in} dt = CV_{in}(V_{C_{max}} - V_{C_{min}}) \end{cases} \quad (7)$$

$$\eta_{ch(QSC)} = \frac{\Delta E_C}{\Delta E_{in}} = \frac{1}{2} \left(\frac{V_{C_{min}} + V_{C_{max}}}{V_{in}} \right) = \frac{\overline{V_C}}{V_{in}}. \quad (8)$$

From this analysis, several points can be concluded.

- 1) Even though the charging trajectories of SC converters (exponential) and QSC converters (linear) are different, their charging efficiencies are identical [see (5) and (8)]. This is because the charging efficiency is independent of R_{ch} and the use of MOSFET in the saturation region merely alters its internal resistance while as an ON-OFF switch, the MOSFET has a fixed $R_{DS(on)}$. Hence, the QSC converter is not more lossy than the conventional SC converter, which is consistent to the comments given in [28].

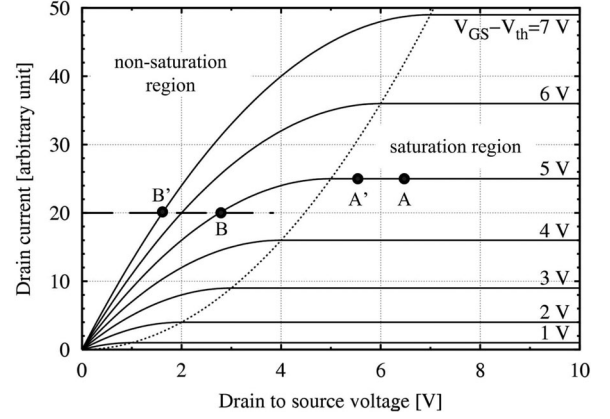


Fig. 9. Output characteristics (I_D and V_{DS}) of a typical N-channel power MOSFET.

- 2) The QSC converter has a flat and continuous input current flow, which means that it does not have an issue with electromagnetic radiation. However, the precise control of the current level may be difficult especially for a varying output power which requires the use of more than one unit of the SC converter connected in parallel.
- 3) Due to voltage-current crossing, nonideal “ON-OFF” switches of conventional SC converters can be regarded as a form of time-varying resistance R_{SW} [39]. Hence, switching loss does not affect the overall charging efficiency. Application of soft-switching in conventional SC converters will not improve the charging efficiency.

B. Control of QSC Converters

In QSC converters, the MOSFET is operated as a constant current source by application of the following control methods.

1) *Saturation Region*: The drain current of power MOSFETs operating in saturation region can be expressed as $I_D = K_n \cdot (V_{GS} - V_{TN})^2$. By applying a small-signal perturbation on I_D and V_{GS} , we have

$$I_D + \tilde{i}_d = K_n \cdot [(V_{GS} + \tilde{v}_{gs}) - V_{TN}]^2 \quad (9)$$

which gives the ac equation as

$$\tilde{i}_d = 2K_n \cdot (V_{GS} - V_{TN}) \cdot \tilde{v}_{gs}. \quad (10)$$

From (10), $\tilde{v}_{gs} = 0$ if $\tilde{i}_d = 0$. To keep I_D constant, the power MOSFET should operate in the saturation region over the entire charging cycle, i.e., V_{DS} should be kept constant within the saturation region, for example, from point A to A' in Fig. 9. Additionally, $V_{C_{max}}$ should be limited to keep the power MOSFET in the saturation region, i.e.,

$$V_{DS} = V_{in} - V_{R_{ch}} - V_{C_{max}} \geq V_{DS(sat)} = V_{GS} - V_{TN}. \quad (11)$$

2) *Nonsaturation Region*: For power MOSFETs operating in nonsaturation region, the expression of the drain current is $I_D = K_n \cdot [(V_{GS} - V_{TN}) \cdot V_{DS} - \frac{V_{DS}^2}{2}]$. By applying a

small-signal perturbation on I_D , V_{DS} , and V_{GS} , we have

$$I_D + \tilde{i}_d = K_n \cdot \left\{ \left[(V_{GS} + \tilde{v}_{gs}) - V_{TN} \right] \cdot (V_{DS} + \tilde{v}_{ds}) - \frac{(V_{DS} + \tilde{v}_{ds})^2}{2} \right\} \quad (12)$$

which gives the small-signal equation as

$$\tilde{i}_d = V_{DS} \cdot \tilde{v}_{gs} + (V_{GS} - V_{TN} - V_{DS}) \cdot \tilde{v}_{ds} \quad (13)$$

where \tilde{v}_{gs} and \tilde{v}_{ds} can be adjusted to keep $\tilde{i}_d = 0$. Thus, another operating point should be selected (by increasing V_{GS} and decreasing V_{DS} , or vice versa) to maintain I_D (for example, from point B to B' in Fig. 9). To ensure that the power MOSFET operates in the nonsaturation region, it is necessary to ensure $V_{DS} < V_{DS(sat)}$ over the entire charging cycle, i.e.,

$$V_{DS} = V_{in} - V_{Rch} - V_{Cmin} < V_{DS(sat)} = V_{GS} - V_{TN}. \quad (14)$$

While there are methods of operating the MOSFET as a constant current source in order to charge the capacitor linearly, the control of the power MOSFET in nonsaturation region requires higher precision due to the narrow operating range of V_{DS} .

IV. CHARGING LOSS DISTRIBUTION

Assume that R_{ch} is the total equivalent resistance in the charging path and it is made up of the ESR of the capacitor R_{ESR} , the $R_{DS(on)}$, and the resistance due to the switching loss R_{SW} . The total energy loss over a switching cycle is $\Delta E_{Total} = \Delta E_{RESR} + \Delta E_{RDS(on)} + \Delta E_{RSW}$. Since these resistive elements are connected in series, the total energy loss will be distributed according to the proportion of the individual resistance over the total equivalent resistance. Consider two charging circuits having the same V_{Cmin} and V_{Cmax} , i.e., same charging efficiencies, but a different R_{ch} [one is R_{ch1} and the other is $R_{ch2} = 10 R_{ch1}$ (by increasing only R_{SW})]. The energy loss in both circuits are the same, i.e., $\Delta E_{Total1} = \Delta E_{Total2}$ as the total energy loss in the charging process is independent of R_{ch} . However, with $R_{ch2} = 10 R_{ch1}$, the squaring of the average current flowing in each circuit will have a tenfold increase, i.e., $I_{in1}^2 = 10 I_{in2}^2$. The energy loss in the two suggested circuits can be found as (15) and (16), respectively

$$\begin{cases} \Delta E_{Total1} = \Delta E_{RESR1} + \Delta E_{RDS(on)1} + \Delta E_{RSW1} \\ \Delta E_{RESR1} = \int_0^{T_{ch}} I_{in1}^2(t) \cdot R_{ESR} dt \\ \Delta E_{RDS(on)1} = \int_0^{T_{ch}} I_{in1}^2(t) \cdot R_{DS(on)} dt \\ \Delta E_{RSW1} = \Delta E_{Total1} - \Delta E_{RESR1} - \Delta E_{RDS(on)1} \end{cases} \quad (15)$$

$$\begin{cases} \Delta E_{Total2} = \Delta E_{RESR2} + \Delta E_{RDS(on)2} + \Delta E_{RSW2} \\ \Delta E_{RESR2} = 0.1 \int_0^{T_{ch}} I_{in1}^2(t) \cdot R_{ESR} dt \\ \Delta E_{RDS(on)2} = 0.1 \int_0^{T_{ch}} I_{in1}^2(t) \cdot R_{DS(on)} dt \\ \Delta E_{RSW2} = \Delta E_{Total1} - 0.1(\Delta E_{RESR2} + \Delta E_{RDS(on)2}). \end{cases} \quad (16)$$

From the equations, it can be seen that the loss in both R_{ESR} (ΔE_{RESR}) and $R_{DS(on)}$ ($\Delta E_{RDS(on)}$) are proportionally decreased while that of R_{SW} (ΔE_{RSW}) is increased when R_{SW}

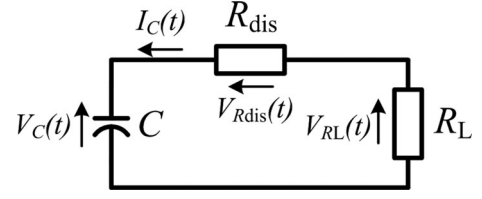


Fig. 10. Equivalent RC discharging circuit with a resistor load.

increases. This indicates that while the change of a resistance component in the charging path does not affect the total charging efficiency, the energy loss among the individual resistive components in the charging path will be changed by adjusting the charging duration, i.e., the switching frequency and the duty ratio, to keep the same desired value of V_{Cmax} . Therefore, by inserting an external resistor in the charging path, the energy loss in the electronic components (power switch and capacitor) will be diverted to the external resistor, thus improving the thermal condition of the components with no penalty on the overall efficiency of the converter.

V. EFFICIENCY OF RC DISCHARGING CIRCUITS

The equivalent discharging circuit of an SC converter can also be represented by an RC circuit. Three types of loading, namely, a resistor, a capacitor, and a parallel resistor–capacitor loads, are considered.

A. Discharging Efficiency With Resistor Load

Fig. 10 presents the equivalent discharging circuit with the resistor load. The simulated voltage and current waveforms are shown in Fig. 11. The instantaneous voltages and current, energy profile, and the discharging efficiency of this circuit over a discharging cycle are

$$\begin{cases} V_C(t) = V_{Cmax} \left[e^{\frac{-t}{(R_{dis} + R_L)C}} \right] \\ I_C(t) = -\frac{V_{Cmax}}{(R_{dis} + R_L)} \left[e^{\frac{-t}{(R_{dis} + R_L)C}} \right] \end{cases} \quad (17)$$

$$\begin{cases} \Delta E_C = \int_0^{T_{dis}} V_C(t) \cdot I_C(t) dt \\ = \frac{C}{2} (V_{Cmax}^2 - V_{Cmin}^2) \\ \Delta E_{RL} = \int_0^{T_{dis}} V_{RL}(t) \cdot I_C(t) dt \\ = \frac{C}{2} (V_{Cmax}^2 - V_{Cmin}^2) \left(\frac{R_L}{R_{dis} + R_L} \right) \\ \Delta E_{Rdis} = \int_0^{T_{dis}} V_{Rdis}(t) \cdot I_C(t) dt \\ = \frac{C}{2} (V_{Cmax}^2 - V_{Cmin}^2) \left(\frac{R_{dis}}{R_{dis} + R_L} \right) \end{cases} \quad (18)$$

$$\eta_{dis(Rload)} = \frac{\Delta E_{RL}}{\Delta E_C} = \frac{R_L}{R_{dis} + R_L} = \frac{\bar{V}_O}{V_C}. \quad (19)$$

From (19), the total equivalent resistance in the discharging path R_{dis} (sum of R_{ESR} , $R_{DS(on)}$, and R_{SW}) will degrade the discharging efficiency, irrespective of whether it is a full ($V_{Cmin} = 0$ V) or partial ($V_{Cmin} > 0$ V) discharging condition. This is consistent with what is reported in [30]. It is important to

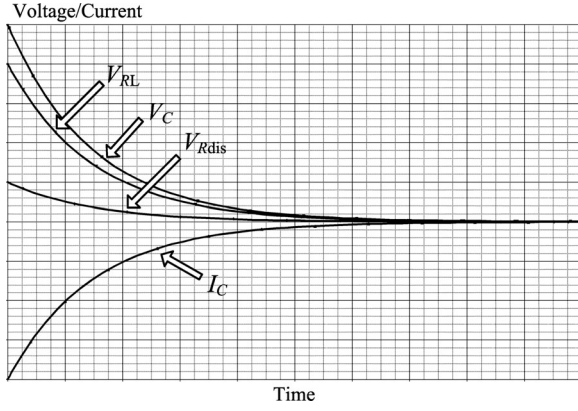


Fig. 11. Simulated current and voltage waveforms of a RC discharging circuit with a resistor load.

keep $R_{\text{dis}} \ll R_L$ (i.e., use of soft-switching) to maintain a high discharging efficiency.

B. Discharging Efficiency With Capacitor Load

The energy transfer from one capacitor to another is a very common process in SC converters. The equivalent circuit, simulated voltage, and current waveforms are given in Figs. 12 and 13, respectively. When two capacitors with different voltages are connected in parallel, charges will be redistributed and energy will be lost (called the charge redistribution loss) [40]. Two different final conditions, resulting from full discharging [see Fig. 14(a)] and partial discharging [see Fig. 14(b)], will be discussed. The instantaneous voltages, current, and energy profile in both the full and partial discharging processes over a discharging cycle are respectively given in (20) and (21)

$$\begin{cases}
 V_C(t) = V_{C\text{max}} - (V_{C\text{max}} - V_{O\text{min}}) \left(\frac{C_E}{C} \right) \left(1 - e^{-\frac{t}{R_{\text{dis}} C_E}} \right) \\
 V_O(t) = V_{O\text{min}} + (V_{C\text{max}} - V_{O\text{min}}) \left(\frac{C_E}{C_O} \right) \left(1 - e^{-\frac{t}{R_{\text{dis}} C_E}} \right) \\
 I_C(t) = -\frac{V_{C\text{max}} - V_{O\text{min}}}{R_{\text{dis}}} \left(e^{-\frac{t}{R_{\text{dis}} C_E}} \right) \\
 C_E = \frac{C \cdot C_O}{C + C_O}, C_O = mC
 \end{cases} \quad (20)$$

$$\begin{cases}
 \Delta E_C = \int_0^{T_{\text{dis}}} V_C(t) \cdot I_C(t) dt \\
 = \frac{C_E}{2} (V_{C\text{max}} - V_{O\text{min}}) \left(1 - e^{-\frac{T_{\text{dis}}}{R_{\text{dis}} C_E}} \right) \\
 \quad \times (V_{C\text{min}} + V_{C\text{max}}) \\
 \Delta E_{C_O} = \int_0^{T_{\text{dis}}} V_O(t) \cdot I_C(t) dt \\
 = \frac{C_E}{2} (V_{C\text{max}} - V_{O\text{min}}) \left(1 - e^{-\frac{T_{\text{dis}}}{R_{\text{dis}} C_E}} \right) \\
 \quad \times (V_{O\text{min}} + V_{O\text{max}}) \\
 \Delta E_{R_{\text{dis}}} = \int_0^{T_{\text{dis}}} V_{R_{\text{dis}}}(t) \cdot I_C(t) dt \\
 = \frac{C_E}{2} (V_{C\text{max}} - V_{O\text{min}})^2 \left(1 - e^{-\frac{2T_{\text{dis}}}{R_{\text{dis}} C_E}} \right). \quad (21)
 \end{cases}$$

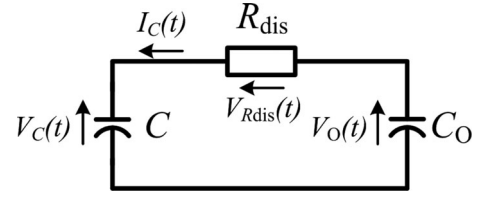


Fig. 12. Equivalent RC discharging circuit with a capacitor load.

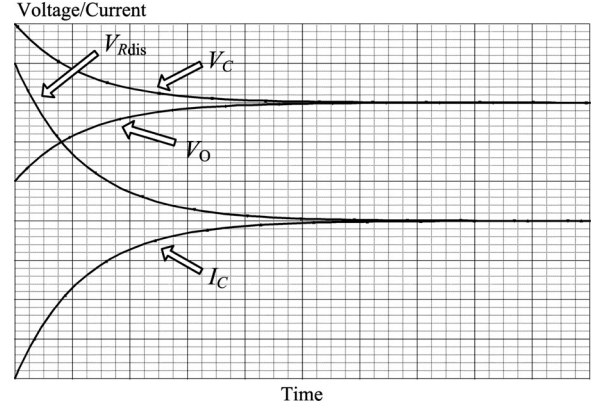


Fig. 13. Simulated current and voltage waveforms of a RC discharging circuit with a capacitor load.

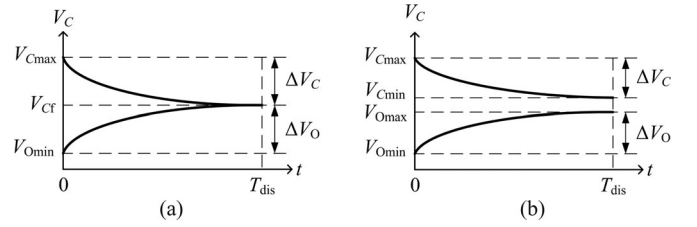


Fig. 14. Sketched capacitor voltage waveforms under two different discharging processes. (a) Full discharging. (b) Partial discharging.

The balanced voltage V_{Cf} can be found using the charge balance approach as

$$\begin{aligned}
 C(V_{C\text{max}} - V_{Cf}) &= C_O(V_{Cf} - V_{O\text{min}}) \\
 \Rightarrow V_{Cf} &= \frac{V_{C\text{max}} + mV_{O\text{min}}}{m + 1}. \quad (22)
 \end{aligned}$$

Differentiating V_{Cf} with respect to m , we have

$$\frac{dV_{Cf}}{dm} = -\frac{V_{C\text{max}} - V_{O\text{min}}}{(m + 1)^2} < 0. \quad (23)$$

From (23), the increase of m will lead to the decrease of V_{Cf} , where m is the ratio between C and C_O (with $C_O = mC$). Additionally, using (21), the efficiency in both discharging conditions can be calculated as

$$\begin{aligned}
 \eta_{\text{dis(Cload,full)}} &= \frac{\Delta E_{C_O}}{\Delta E_C} = \frac{V_{Cf} + V_{O\text{min}}}{V_{Cf} + V_{C\text{max}}} \\
 &= \frac{2V_{Cf} - \Delta V_{C_O}}{2V_{Cf} + \Delta V_C} \quad (24)
 \end{aligned}$$

$$\begin{aligned}
 \eta_{\text{dis(Cload,partial)}} &= \frac{\Delta E_{C_O}}{\Delta E_C} = \frac{V_{O\text{max}} + V_{O\text{min}}}{V_{C\text{max}} + V_{C\text{min}}} \\
 &= \frac{2V_{O\text{max}} - \Delta V_{C_O}}{2V_{C\text{min}} + \Delta V_C}. \quad (25)
 \end{aligned}$$

By substituting (22) into (24), and differentiating $\eta_{\text{dis(Cload,full)}}$ with respect to m , we have

$$\frac{d\eta_{\text{dis(Cload,full)}}}{dm} = -\frac{V_{C_{\text{max}}}^2 + V_{O_{\text{min}}}^2}{[(m+1)V_{C_{\text{max}}} + mV_{C_{\text{min}}}]^2} < 0. \quad (26)$$

If $C_O > C$, both V_{C_f} and $\eta_{\text{dis(Cload,full)}}$ will decrease when m increases. Equations (24) and (25) indicate that the discharging efficiency is independent of R_{dis} , but is dependent on ΔV_C . The difference between $V_{O_{\text{min}}}$ and $V_{C_{\text{max}}}$, therefore both $\Delta V_C (= V_{C_{\text{max}}} - V_{C_{\text{min}}})$ and $\Delta V_O (= V_{O_{\text{max}}} - V_{O_{\text{min}}})$, should be kept small for a higher discharging efficiency.

It is important to emphasize that in this case, the discharging efficiency on C is the same as the charging efficiency on C_O . However, the charging efficiency on a capacitor in an RC circuit is different when the capacitor is charged by a constant voltage source and by a precharged capacitor. Consider an RC circuit (see Fig. 1) with the following condition: $V_{\text{in}} = 1$ V and $V_{C_{\text{min}}} = 0$ V. After the capacitor C is fully charged ($V_{C_{\text{max}}} = V_{\text{in}}$), the charging efficiency is 50% [using (3)]. Consider another RC circuit (see Fig. 12) with the following parameters: $V_{C_{\text{max}}} = 2$ V, $V_{O_{\text{min}}} = 0$ V, and $C = C_O$. After the completion of the charge redistribution process, $V_{C_{\text{min}}} = V_{O_{\text{max}}} = 1$ V, $\Delta E_C = 1.5C$, and $\Delta E_{C_O} = 0.5C$, leading to the charging efficiency on C_O is only 33% [refer to (24)]. Although $\Delta V_C = 1$ V is the same in both cases (same amount of energy delivered), charging a capacitor by a voltage source is more efficient than by a precharged capacitor due to the smaller charging current peak and the shorter charging duration.

C. Discharging Efficiency With Parallel RC Load

For practical SC converters, an output capacitor is connected in parallel with the load resistor for minimizing the output voltage ripple. Precharged flying capacitors will deliver energy to both the output capacitor and load resistor. Fig. 15(a) gives the equivalent circuit of a capacitor C discharging to an RC load. The waveforms of V_C and V_O are shown in Fig. 15(b). Figs. 16 and 17 are, respectively, the simulated and experimental results of the RC discharging circuit with an RC parallel load. The voltage and current profile can be described as

$$\begin{cases} C \frac{dV_C(t)}{dt} = \frac{V_O(t) - V_C(t)}{R_{\text{dis}}} \\ \frac{V_O(t) - V_C(t)}{R_{\text{dis}}} + C_O \frac{dV_O(t)}{dt} + \frac{V_O(t)}{R_L} = 0. \end{cases} \quad (27)$$

By solving (27), the voltage and current profile can be found as

$$\begin{cases} V_C(t) = \left(\frac{1}{4CR_L\alpha^{1/2}} \right) (X_1 Z_1 e^{-Y_1 t} + X_2 Z_2 e^{-Y_2 t}) \\ V_O(t) = \frac{1}{2\alpha^{1/2}} (X_1 e^{-Y_1 t} + X_2 e^{-Y_2 t}) \\ I_C(t) = \left(\frac{1}{4R_L\alpha^{1/2}} \right) (X_1 Y_1 Z_1 e^{-Y_1 t} + X_2 Y_2 Z_2 e^{-Y_2 t}) \\ I_{C_O}(t) = \frac{-C_O}{2\alpha^{1/2}} (X_1 Y_1 e^{-Y_1 t} + X_2 Y_2 e^{-Y_2 t}) \end{cases} \quad (28)$$

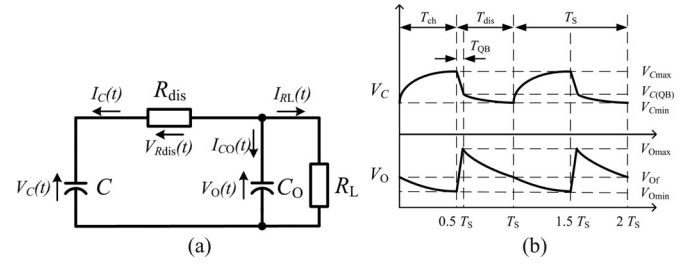


Fig. 15. (a) Equivalent RC discharging circuit with a parallel RC load and (b) the voltage waveforms of C and C_O .

where

$$\alpha = R_{\text{dis}}^2 C^2 + 2R_{\text{dis}}R_L C^2 - 2R_{\text{dis}}R_L C C_O + R_L^2 C^2 + 2C C_O R_L^2 + R_L^2 C_O^2$$

$$X_1 = -Z_2 V_{O_{\text{min}}} + 2R_L C V_{C_{\text{max}}}$$

$$X_2 = Z_1 V_{O_{\text{min}}} - 2R_L C V_{C_{\text{max}}}$$

$$Y_1 = \frac{1}{2R_{\text{dis}}R_L C C_O} (Z_2 - 2R_L C_O)$$

$$Y_2 = \frac{1}{2R_{\text{dis}}R_L C C_O} (Z_1 + 2R_L C_O)$$

$$Z_1 = R_{\text{dis}}C + C R_L - R_L C_O + \alpha^{1/2}$$

$$Z_2 = R_{\text{dis}}C + C R_L - R_L C_O - \alpha^{1/2}.$$

The operation of the circuit can be briefly described as follows: If $V_{C_{\text{max}}} > V_{O_{\text{min}}}$, the charge in C will be delivered to C_O and dissipated in R_L until C_O is fully charged ($I_{C_O} = 0$ A). When this happens, both capacitors will then transfer energy to the load resistor. A two-stage analysis based on the operation of C_O is given to elaborate the operation of the circuit (see Figs. 16 and 17).

1) *Stage One—Charge Redistribution Phase*: Due to the unbalanced initial voltages on C and C_O (with $V_{C_{\text{max}}} > V_{O_{\text{min}}}$), C delivers charge to both C_O and R_L until C_O is fully charged. By conservation of charge, we have

$$C(V_{C_{\text{max}}} - V_{C_{\text{(QB)}}}) = C_O(V_{O_{\text{max}}} - V_{O_{\text{min}}}) + I_{R_L} \cdot T_{\text{QB}} \quad (29)$$

where $V_{C_{\text{(QB)}}}$ and $V_{O_{\text{max}}}$ are, respectively, the voltages of C and C_O after the completion of the charge redistribution process, T_{QB} is the time duration of the process [see Fig. 15(b)]. As $V_{O_{\text{max}}} = V_{C_{\text{(QB)}}} \left(\frac{R_L}{R_L + R_{\text{dis}}} \right)$ and $I_{R_L} = \frac{V_{O_{\text{max}}} + V_{O_{\text{min}}}}{2R_L}$ (with the assumption that T_{QB} is much smaller than the time constant of the circuit, i.e., C_O charges up linearly), $V_{C_{\text{(QB)}}}$ and $V_{O_{\text{max}}}$ can be, respectively, expressed as

$$V_{C_{\text{(QB)}}} = \frac{C V_{C_{\text{max}}} + (C_O - \frac{T_{\text{QB}}}{2R_L}) V_{O_{\text{min}}}}{C + C_O \left(\frac{R_L}{R_L + R_{\text{dis}}} \right) + \frac{T_{\text{QB}}}{2(R_L + R_{\text{dis}})}} \quad (30)$$

$$V_{O_{\text{max}}} = \frac{C V_{C_{\text{max}}} + (C_O - \frac{T_{\text{QB}}}{2R_L}) V_{O_{\text{min}}}}{C \left(1 + \frac{R_{\text{dis}}}{R_L} \right) + C_O + \frac{T_{\text{QB}}}{2(R_L)}}. \quad (31)$$

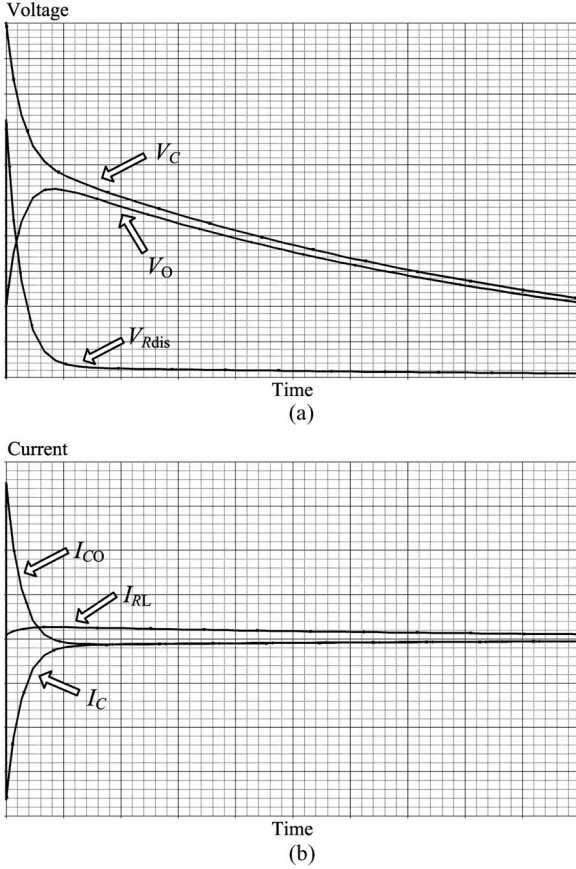


Fig. 16. Simulated (a) voltage and (b) current waveforms of the RC discharging circuit with an RC parallel load.

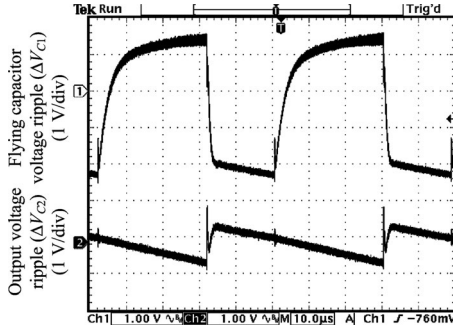


Fig. 17. Experimental results of the voltage waveforms of C and C_O in the RC discharging circuit in Fig. 15(a) with the following parameters: $V_{C_{\max}} = 11.7$ V, $V_{O_{\min}} = 7.4$ V, $C = 20$ μ F, $C_O = 94$ μ F, $R_{\text{dis}} = 0.07$ Ω , and $R_L = 8.4$ Ω .

The discharging efficiency in the first stage can be calculated as

$$\begin{aligned} \eta_{RC\text{load}1} &= \frac{\Delta E_{RC\text{load}}}{\Delta E_C} = \frac{\overline{V_{C_O}} \cdot I_C \cdot T_{Q_B}}{\frac{1}{2} C (V_{C_{\max}}^2 - V_{C(QB)}^2)} \\ &= \frac{V_{O_{\max}} + V_{O_{\min}}}{V_{C(QB)} + V_{C_{\max}}}. \end{aligned} \quad (32)$$

The expression in (32) is similar to (25), i.e., a charge sharing loss between the capacitors exists in this stage. Additionally, (30) and (31) reflect that the presence of R_{dis} increases $V_{C(QB)}$ but decreases $V_{O_{\max}}$, leading to a reduction in the discharging efficiency. The parasitics will lower the discharging efficiency since it is in series with the output resistor, thereby creating a voltage divider network between the two.

2) *Stage Two—Loading Phase*: Both C and C_O will deliver energy to the load resistor together. Applying the principle of charge balance, we have

$$C(V_{C(QB)} - V_{C_{\min}}) + C_O(V_{O_{\max}} - V_{O_f}) = I_{R_L}(T_{\text{dis}} - T_{Q_B}). \quad (33)$$

Using $V_{O_f} = V_{C_{\min}} \left(\frac{R_L}{R_L + R_{\text{dis}}} \right)$ and $I_{R_L} = \frac{V_{O_{\max}} + V_{O_f}}{2R_L}$, the final voltages of C and C_O can be found as

$$V_{C_{\min}} = V_{C(QB)} \left[\frac{C(R_L + R_{\text{dis}}) + R_L C_O - \frac{T_{\text{dis}} - T_{Q_B}}{2}}{C(R_L + R_{\text{dis}}) + R_L C_O + \frac{T_{\text{dis}} - T_{Q_B}}{2}} \right] \quad (34)$$

$$\begin{aligned} V_{O_f} &= V_{C(QB)} \left(\frac{R_L}{R_L + R_{\text{dis}}} \right) \\ &\times \left[\frac{C(R_L + R_{\text{dis}}) + R_L C_O - \frac{T_{\text{dis}} - T_{Q_B}}{2}}{C(R_L + R_{\text{dis}}) + R_L C_O + \frac{T_{\text{dis}} - T_{Q_B}}{2}} \right]. \end{aligned} \quad (35)$$

The discharging efficiency can then be derived as

$$\begin{aligned} \eta_{RC\text{load}2} &= \frac{\Delta E_{RC\text{load}}}{\Delta E_C} = \frac{\overline{V_{C_O}} \cdot I_C \cdot (T_{\text{dis}} - T_{Q_B})}{\frac{1}{2} C (V_{C(QB)}^2 - V_{C_{\min}}^2)} \\ &= \frac{R_L}{R_{\text{dis}} + R_L} \end{aligned} \quad (36)$$

which is the same expression as given in (19), i.e., only the voltage divider loss among the parasitics and the load will have an effect on the discharging efficiency. This can be explained by the lossless discharging process on an RC circuit. As the energy delivered by C_O will dissipate entirely on R_L (ignore the ESR of C_O), the discharging process under such a circumstance is regarded as lossless. Thus, the only loss encountered in this stage is the discharging loss of C on R_{dis} .

To conclude, the discharging efficiency of an RC circuit with an RC load is affected by two factors: the charge redistribution loss and the voltage-divider loss in the discharging path. To maximize the discharging efficiency of an SC converter with an parallel RC load, it is necessary to keep $R_{\text{dis}} \ll R_L$, $\Delta V_C (= V_{C_{\max}} - V_{C(QB)})$ and $\Delta V_O (= V_{O_{\max}} - V_{O_{\min}})$ small.

VI. SWITCHING FREQUENCY VERSUS EFFICIENCY

The effect of switching frequency on the overall efficiency will be presented in this section. Fig. 18(a) presents a simple SC converter with the corresponding timing diagram shown in Fig. 18(b). The flying capacitor is charged when S_1 is turned ON and S_2 is turned OFF. The output capacitor C_O is discharged to the load at the same time. Then, both S_1 and S_2 are turned OFF during T_{hold} . In the second half of the switching period, S_2 is turned ON and S_1 is turned OFF. The flying capacitor will be discharged to both the output capacitor and the output load (see

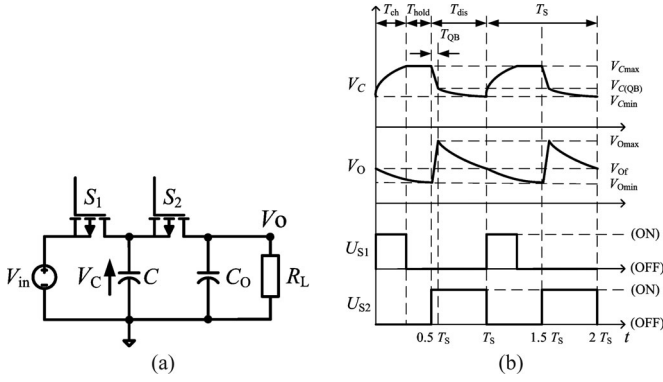


Fig. 18. (a) Complete SC converter circuit with (b) its timing diagram.

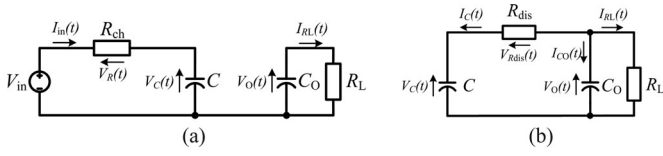


Fig. 19. Equivalent (a) charging and (b) discharging circuits for the SC converter in Fig. 18.

the equivalent charging and discharging circuits in Fig. 19(a) and (b), respectively).

Based on the critical values of V_C and V_O (refer to the detailed derivation in Appendix A), the overall efficiency can be given by

$$\eta_{SC} = \frac{\Delta E_{RL}}{\Delta E_{in}} = \left[\frac{1}{2V_{in}(V_{Cmax} - V_{Cmin})} \right] \times \left[V_{Cmax}(V_{Omin} + V_{Omax}) + V_{C(QB)}(V_{Of} + V_{Omin}) - V_{Cmin}(V_{Omax} + V_{Of}) \right]. \quad (37)$$

For detailed derivation, refer to Appendix B.

Substituting (45)–(48) into (37), the relationship between the switching frequency and the overall efficiency is derived and plotted in Fig. 20. As shown in the figure, the efficiency increases with the increment of frequency in the low-frequency region, and then reach a limit at around 200 kHz. Note that the effect of parasitic inductance (which is only significant at very high frequency) is neglected as this will convert the SC circuit into a resonant circuit, which is beyond the scope of this work.

VII. OVERALL EFFICIENCY OF SC CONVERTERS

Combining the analysis of the charging and discharging operations, the overall SC converter's efficiency can be analyzed at a system's level using a simple SC converter circuit in Fig. 18(a), with the corresponding timing diagram shown in Fig. 18(b).

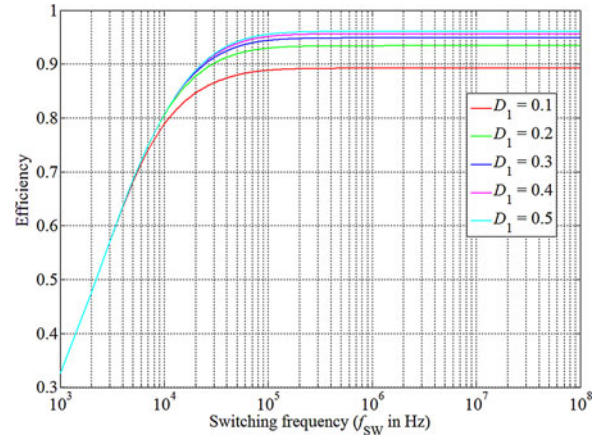


Fig. 20. Simulated results on the relationship between the switching frequency and the overall efficiency for an unregulated SC converter ($V_{in} = 12$ V, $C = C_O = 47$ μ F, $R_{ch} = R_{dis} = 0.1$ Ω , and $R_L = 10$ Ω).

Table I summarizes the major efficiency expressions in different aspects and conditions. Since at steady state, energy is balanced on the flying capacitor, i.e., $\Delta E_{C(ch)} = \Delta E_{C(dis)}$, the overall efficiency of the SC converter over a complete switching cycle is

$$\eta_{SC} = \frac{\Delta E_{RL}}{\Delta E_{in}} = \left(\frac{\Delta E_{C(ch)}}{\Delta E_{in}} \right) \left(\frac{\Delta E_{RL}}{\Delta E_{C(dis)}} \right) = \eta_{ch(partial)} \cdot \eta_{dis(Rload)}. \quad (38)$$

With the assumption of linear charging on the flying capacitor (the charging time is much smaller than the time constant in the charging circuit) and the relatively larger output capacitor compared to the flying capacitor (i.e., $C_O \gg C$), (39) can also be derived from (5) and the voltage divider property at the output in Fig. 10 to reach the same result given in [36] and [37]

$$\frac{\bar{V}_O}{V_{in}} = \left(\eta_{dis(Rload)} \cdot \bar{V}_C \right) \left(\frac{\eta_{ch(partial)}}{\bar{V}_C} \right) = \eta_{ch(partial)} \cdot \eta_{dis(Rload)}. \quad (39)$$

An experimental prototype has been constructed based on Fig. 18(a) with the following design specifications: $V_{in} = 12$ V, $\bar{V}_O = 9$ V, $C = 47$ μ F, $C_O = 94$ μ F, and $f_{SW} = 200$ kHz. $R_{DS(on)}$ of PMOS switches S_1 and S_2 is 0.06 Ω and the current sensing resistor inserted in both the charging and discharging paths is 0.1 Ω , i.e., $R_{ch} = 0.16$ Ω and $R_{dis} = 0.16$ Ω . The output voltage is regulated using a standard voltage mode controller IC TL494. A Type II compensator with transfer function $G_C(s) = \frac{s + 2.74 \times 10^3}{s(1.12 \times 10^{-5}s + 8.55 \times 10^{-2})}$ obtained through a trial-and-error tuning is used in the feedback control.

Fig. 21(a) shows the experimentally measured overall efficiency versus the load current of the SC converter based on the original design specifications, but with different values of charging resistance R_{ch} . Here, the input power and the output power of the SC converter are measured for three values of R_{ch} (0.16, 0.26, and 0.36 Ω) with the discharging side of the SC converter remains unchanged for the load current range of 1 to 2 A. In

TABLE I
MAJOR EFFICIENCY EQUATIONS OF SC CONVERTERS

Descriptions	Efficiency Equations
Charging efficiency (full)	$\eta_{\text{ch(full)}} = \frac{1}{2} \left(1 + \frac{V_{C\text{min}}}{V_{\text{in}}} \right)$
Charging efficiency (partial)	$\eta_{\text{ch(partial)}} = \frac{1}{2} \left(\frac{V_{C\text{min}} + V_{C\text{max}}}{V_{\text{in}}} \right) \approx \frac{\overline{V_C}}{V_{\text{in}}}$
Discharging efficiency (R load)	$\eta_{\text{dis(Rload)}} = \frac{R_L}{R_{\text{dis}} + R_L}$
Discharging efficiency (C load, full)	$\eta_{\text{dis(Cload,full)}} = \frac{V_{Cf} + V_{O\text{min}}}{V_{Cf} + V_{C\text{max}}}$
Discharging efficiency (C load, partial)	$\eta_{\text{dis(Cload,partial)}} = \frac{V_{O\text{max}} + V_{O\text{min}}}{V_{C\text{max}} + V_{C\text{min}}}$
Discharging efficiency (RC load, 1st stage)	$\eta_{RC\text{load1}} = \frac{V_{O\text{max}} + V_{O\text{min}}}{V_{C(QB)} + V_{C\text{max}}}$
Discharging efficiency (RC load, 2nd stage)	$\eta_{RC\text{load2}} = \frac{R_L}{R_{\text{dis}} + R_L}$

the experiment, the turn-on time of the charging circuit T_{ch} is adjusted such that for different values of R_{ch} , $\overline{V_C}$ is maintained constant under the same loading condition while the turn-on time of the discharging circuit T_{dis} remains unchanged and that the output voltage is regulated at 9 V. The so-called overall efficiency described here is obtained by dividing the measured output power by the measured input power. It can be seen from the plot that for a different value of R_{ch} , the same efficiency under the same input voltage, output voltage, and loading condition, is obtained. Since the same discharging circuit is used throughout the experiment, there is no change in the discharging efficiency under the same load condition even when R_{ch} is different. Therefore, Fig. 21(a) shows equivalently the trend of the charging efficiency of the SC converter, which conclusively proves that charging efficiency is independent of the charging resistance R_{ch} .

Fig. 21(b) shows the plots of experimentally measured overall efficiency against the input power of the SC converter for different values of discharging resistance R_{dis} . Here, the experiment is conducted for three values of R_{dis} (0.16, 0.26, and 0.36 Ω) while the charging side of the SC converter remains unchanged for the input power range of 10 to 25 W. In the experiment, both T_{ch} and T_{dis} are adjusted such that for different values of R_{dis} , $\overline{V_C}$ is maintained constant under the same loading condition. In this way, the charging efficiency is constant for different values of R_{dis} . Thus, the efficiency plot is equivalently illustrating the trend of the discharging efficiency of the SC converter for different values of R_{dis} . From the plots, a larger value R_{dis} results in a lower discharging efficiency under the same input power, which is consistent with our analysis that R_{dis} degrades the discharging efficiency of SC converters.

Fig. 22(a)–(c) shows the experimental and calculated efficiencies of the SC converter against the load current for different flying capacitance, output capacitance, and switching frequency. Here, the SC converter is based on the design specifications, but with different values of C , C_O , and f_{SW} , under feedback control which automatically regulates the output voltage at 9 V. There is no manual adjustment of T_{ch} and T_{dis} to regulate the value of $\overline{V_C}$. From the plots, it can be observed that a larger

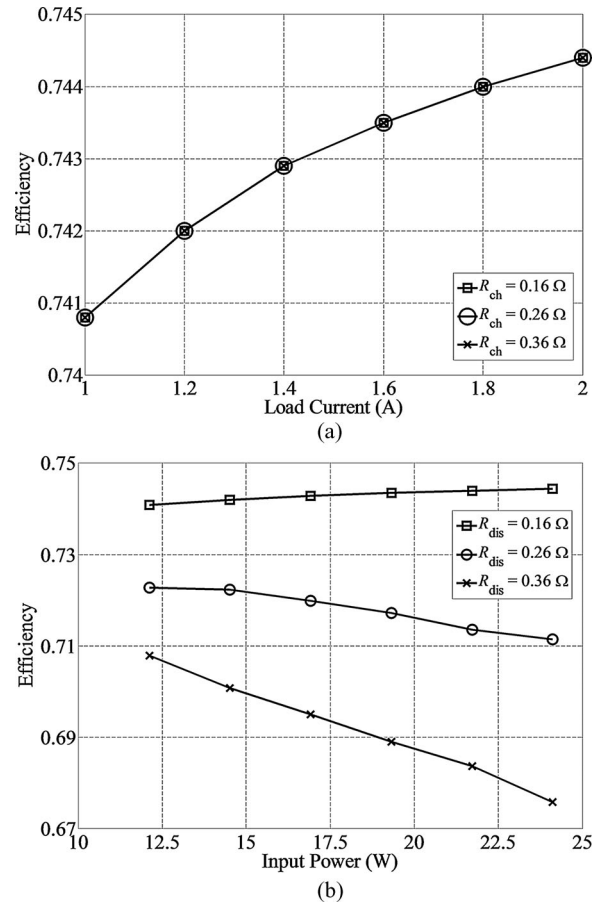


Fig. 21. Experimental results showing (a) the overall efficiency versus load current with different charging resistances R_{ch} and (b) the overall efficiency versus the input power with different discharging resistances R_{dis} under closed-loop control where $\overline{V_C}$ is maintained constant under the same load.

switching frequency, flying capacitance, and output capacitance can achieve a higher power efficiency, which is consistent to our analysis. Note that the experimental results include the power consumption of the control circuits, which is relatively small

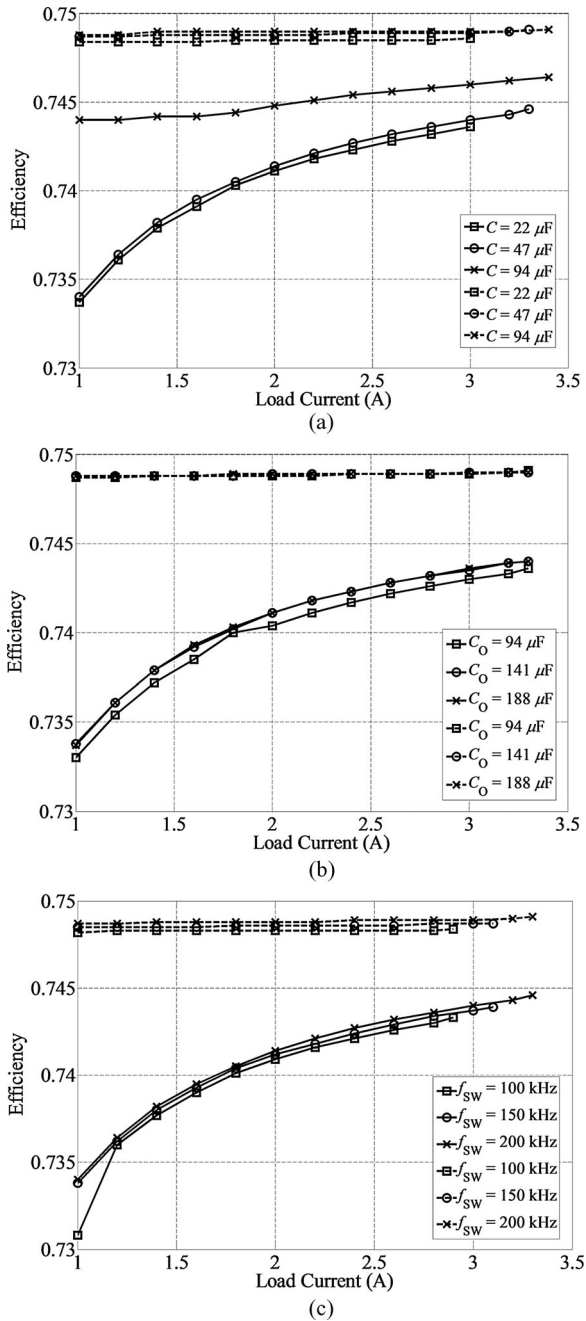


Fig. 22. Experimental (solid lines) and calculated (dotted lines) results showing the efficiency versus load current with (a) different flying capacitance, (b) different output capacitance, and (c) different switching frequency.

(less than 0.7 W) and only has a significant effect on the overall efficiency at light load condition.

Fig. 23 shows the plots of the measured and calculated efficiencies of the SC converter (based on the original design specifications) with different load values, of which both results are in close proximity with one another.

Additionally, with the converter operating as a system that toggles between the charging and discharging operations, the capacitor size and switching frequency are important factors that influence the energy efficiency. For an unregulated SC converter,

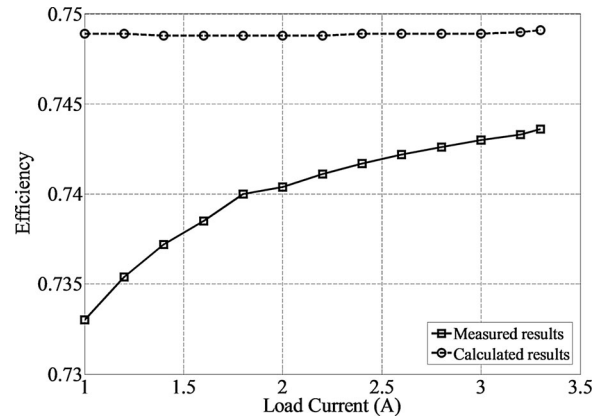


Fig. 23. Plots of experimental and calculated result of the efficiency of the SC converter (based on the original design specifications) versus different load currents.

a bigger capacitance and a higher switching frequency f_{sw} will increase the average voltage of the flying capacitor, and reduce the charging/discharging flying capacitor voltage ripple ΔV_C , leading to a higher efficiency. However, for a regulated SC converter, the efficiency can be found in (39).

VIII. CONCLUSION

A thorough discussion on the charging, discharging, and overall efficiencies of SC converters have been presented. The following are the major points of concern for the design of SC converters. The charging resistance R_{ch} does not affect the charging efficiency, but the discharging resistance R_{dis} in the discharging circuit does affect the discharging efficiency. Second, QSC converters have a similar loss to SC converters. Third, soft switching would not improve the charging efficiency, but would improve the discharging efficiency. Moreover, a change in resistance of one resistive component will redistribute the energy loss of other resistive components without affecting the overall efficiency. Furthermore, the discharging efficiency of an SC converter with an RC load is affected by both the voltage divider loss and the capacitors' charges redistribution. Last, since ΔV_C affects the overall energy efficiency, increasing f_{sw} or C can improve the efficiency of SC converters.

With this understanding, the rules of thumb toward designing a highly efficient SC converter are suggested. First, $\overline{V_C}$ should be near V_{in} in the charging process. Additionally, ΔV_C should be small in the charging/discharging processes during steady state. Soft switching should be applied only on the power switches in the discharging path to enhance the discharging efficiency. R in the discharging path should be kept as small as possible to maximize the discharging efficiency. For capacitors that share charges, ΔV_C on both capacitors should be small. This also implies that a high f_{sw} and a large C can be used to minimize ΔV_C .

It is important to emphasize that the maximum theoretical efficiency of SC converters is still a function of the voltage conversion ratio n , the input and output voltages of the converter [29]. Thus, the practical design rules should aim to ensure that

the efficiency of SC converters approach this theoretical limit. Additionally, although the charging efficiency is only 50% when a capacitor is fully charged from 0 V to V_{in} , SC converters can still achieve a very high efficiency since the flying capacitors are never charged from 0 V in the steady state. Furthermore, energy efficiency is the same as power efficiency during steady state since energy transfer is repeated periodically.

APPENDIX A

DERIVATION ON THE CRITICAL VOLTAGES ON C AND C_O

The instantaneous voltages on C and C_O can be expressed as

$$V_C(t) = \begin{cases} (V_{in} - V_{Cmin})(1 - e^{-\frac{t}{R_{ch}C}}) + V_{Cmin}, & 0 \leq t \leq T_{ch} \\ \left(\frac{1}{4CR_L\alpha^{1/2}}\right) \left(X_1 Z_1 e^{-Y_1(t-0.5T_S)} + X_2 Z_2 e^{-Y_2(t-0.5T_S)}\right), & 0.5T_S \leq t \leq T_S \end{cases} \quad (40)$$

$$V_O(t) = \begin{cases} \frac{1}{2\alpha^{1/2}} \left(X_1 e^{-Y_1 T_{dis}} + X_2 e^{-Y_2 T_{dis}}\right) \left(e^{-\frac{t}{R_L C_O}}\right), & 0 \leq t \leq 0.5T_S \\ \frac{1}{2\alpha^{1/2}} \left(X_1 e^{-Y_1(t-0.5T_S)} + X_2 e^{-Y_2(t-0.5T_S)}\right), & 0.5T_S \leq t \leq T_S \end{cases} \quad (41)$$

where

$$\alpha = R_{dis}^2 C^2 + 2R_{dis} R_L C^2 - 2R_{dis} R_L C C_O + R_L^2 C^2 + 2C C_O R_L^2 + R_L^2 C_O^2$$

$$X_1 = -Z_2 V_{Omin} + 2R_L C V_{Cmax}$$

$$X_2 = Z_1 V_{Omin} - 2R_L C V_{Cmax}$$

$$Y_1 = \frac{1}{2R_{dis} R_L C C_O} (Z_2 - 2R_L C_O)$$

$$Y_2 = \frac{1}{2R_{dis} R_L C C_O} (Z_1 + 2R_L C_O)$$

$$Z_1 = R_{dis} C + C R_L - R_L C_O + \alpha^{1/2}$$

$$Z_2 = R_{dis} C + C R_L - R_L C_O - \alpha^{1/2}$$

Using (40), (41), and $T_{dis} = 0.5T_S$, the initial voltages of both C and C_O on the discharging cycle can be expressed as

$$V_{Cmax} = V_C(T_{ch}) = V_{in} \left(1 - e^{-\frac{T_{ch}}{R_{ch}C}}\right) + V_{Cmin} \cdot e^{-\frac{T_{ch}}{R_{ch}C}} \quad (42)$$

$$V_{Omin} = V_O(0.5T_S) = \frac{V_{Cmax} \left[\left(\frac{R_L C_O}{\alpha^{0.5}}\right) \left(e^{-Y_1 \cdot 0.5T_S} - e^{-Y_2 \cdot 0.5T_S}\right) \left(e^{-\frac{0.5T_S}{R_L C_O}}\right)\right]}{1 + \frac{1}{2\alpha^{0.5}} \left(Z_2 e^{-Y_1 \cdot 0.5T_S} - Z_1 e^{-Y_2 \cdot 0.5T_S}\right) \left(e^{-\frac{0.5T_S}{R_L C_O}}\right)}$$

Additionally, the charge redistribution time T_{QB} can be computed by considering the time duration from the start of the discharging cycle until V_O is maximum [see Fig. 18(b)], i.e.,

$$\frac{dV_O(t)}{dt} = 0 \Rightarrow T_{QB} = \left(\frac{R_{dis} R_L C C_O}{\alpha^{0.5}}\right) \ln \left[\frac{(Z_1 V_{Omin} - 2R_L C V_{Cmax})(Z_1 + 2R_L C_O)}{(Z_2 V_{Omin} - 2R_L C V_{Cmax})(Z_2 + 2R_L C_O)}\right]. \quad (44)$$

Using (30) and (44), and by substituting (34) into (42) and (43), V_{Cmax} and V_{Omin} can be solved in terms of the circuit parameters and the operating conditions. Similarly, other critical design values, such as V_{Cmin} , $V_{C(QB)}$, V_{Omax} , and V_{Of} can be calculated using (30), (31), (34), (35), and the solution of V_{Cmax} and V_{Omin} . The derived solutions are

$$V_{Cmin} = V_{Cmax} \left[\left(\frac{1}{2\alpha^{0.5}}\right) \left(Z_1 e^{-Y_1 \cdot 0.5T_S} - Z_2 e^{-Y_2 \cdot 0.5T_S}\right)\right] - V_{Omin} \left[\left(\frac{Z_1 Z_2}{4C R_L \alpha^{0.5}}\right) \left(e^{-Y_1 \cdot 0.5T_S} - e^{-Y_2 \cdot 0.5T_S}\right)\right] \quad (45)$$

$$V_{C(QB)} = V_{Cmax} \left[\left(\frac{1}{2\alpha^{0.5}}\right) \left(Z_1 e^{-Y_1 \cdot T_{QB}} - Z_2 e^{-Y_2 \cdot T_{QB}}\right)\right] - V_{Omin} \left[\left(\frac{Z_1 Z_2}{4C R_L \alpha^{0.5}}\right) \left(e^{-Y_1 \cdot T_{QB}} - e^{-Y_2 \cdot T_{QB}}\right)\right] \quad (46)$$

$$V_{Omax} = V_{Cmax} \left[\left(\frac{R_L C}{\alpha^{0.5}}\right) \left(e^{-Y_1 \cdot T_{QB}} - e^{-Y_2 \cdot T_{QB}}\right)\right] \times \left(e^{-\frac{(T_S - 0.5T_S)}{R_L C_O}}\right) - V_{Omin} \left[\left(\frac{1}{2\alpha^{0.5}}\right)\right] \times \left(Z_2 e^{-Y_1 \cdot T_{QB}} - Z_1 e^{-Y_2 \cdot T_{QB}}\right) \left(e^{-\frac{(T_S - 0.5T_S)}{R_L C_O}}\right) \quad (47)$$

$$V_{Of} = V_{Cmax} \left[\left(\frac{R_L C}{\alpha^{0.5}}\right) \left(e^{-Y_1 \cdot 0.5T_S} - e^{-Y_2 \cdot 0.5T_S}\right)\right] \times \left(e^{-\frac{(T_S - 0.5T_S)}{R_L C_O}}\right) - V_{Omin} \left[\left(\frac{1}{2\alpha^{0.5}}\right)\right] \times \left(Z_2 e^{-Y_1 \cdot 0.5T_S} - Z_1 e^{-Y_2 \cdot 0.5T_S}\right) \left(e^{-\frac{(T_S - 0.5T_S)}{R_L C_O}}\right) \quad (48)$$

APPENDIX B

DERIVATION ON THE ENERGY PROFILE AND THE ENERGY EFFICIENCY

The energy profile for different circuit components over a switching period can be analyzed as follows:

- 1) *charging phase*: C will be charged by the voltage source and C_O will be discharged to R_L ($\Delta E_{in} = \Delta E_C + \Delta E_{Rch}$, $\Delta E_{CO} = \Delta E_{RL}$);
- 2) *redistribution phase*: C will be discharged to both C_O and R_L ($\Delta E_C = \Delta E_{CO} + \Delta E_{Rdis} + \Delta E_{RL}$);
- 3) *loading phase*: Both C and C_O will be discharged to R_L ($\Delta E_C + \Delta E_{CO} = \Delta E_{Rdis} + \Delta E_{RL}$).

TABLE II
ENERGY PROFILE ON DIFFERENT CIRCUIT COMPONENTS IN A SWITCHING PERIOD

Components	Charging phase	Charge redistribution phase	Loading phase
C (ΔE_C)	$\frac{C}{2}(V_{C\max}^2 - V_{C\min}^2)$	$\frac{C}{2}(V_{C\max}^2 - V_{C(QB)}^2)$	$\frac{C}{2}(V_{C(QB)}^2 - V_{C\min}^2)$
C_O (ΔE_{C_O})	$\frac{C_O}{2}(V_{Of}^2 - V_{O\min}^2)$	$\frac{C_O}{2}(V_{O\max}^2 - V_{O\min}^2)$	$\frac{C_O}{2}(V_{O\max}^2 - V_{Of}^2)$
R_{ch} ($\Delta E_{R_{ch}}$)	$\frac{C}{2}[(V_{in} - V_{C\min})^2 - (V_{in} - V_{C\max})^2]$	N/A	N/A
R_{dis} ($\Delta E_{R_{dis}}$)	N/A	$\frac{C}{2}(V_{C\max} - V_{C(QB)})[(V_{C\max} + V_{C(QB)}) - (V_{O\max} + V_{O\min})]$	$\frac{C}{2}(V_{C(QB)} - V_{C\min})[(V_{C(QB)} + V_{C\min}) - (V_{O\max} + V_{Of})]$
R_L (ΔE_{R_L})	$\frac{C_O}{2}(V_{Of}^2 - V_{O\min}^2)$	$\frac{1}{2}(V_{O\max} + V_{O\min})[C(V_{C\max} - V_{C(QB)}) - C_O(V_{O\max} - V_{O\min})]$	$\frac{1}{2}(V_{O\max} + V_{Of})[C(V_{C(QB)} - V_{C\min}) + C_O(V_{O\max} - V_{Of})]$
V_{in} (ΔE_{in})	$CV_{in}(V_{C\max} - V_{C\min})$	N/A	N/A

The detailed evaluation on the energy profile is summarized in Table II.

Therefore, the total amount of energy delivered to the load is the summation of the energy profile of R_L over all the three phases, i.e.,

$$\Delta E_{R_L} = \frac{C}{2}[V_{C\max}(V_{O\min} + V_{O\max}) + V_{C(QB)}(V_{Of} + V_{O\min}) - V_{C\min}(V_{O\max} + V_{Of})]. \quad (49)$$

The input energy is

$$\Delta E_{in} = CV_{in}(V_{C\max} - V_{C\min}). \quad (50)$$

Dividing (49) by (50), the overall efficiency can be given by

$$\eta_{SC} = \frac{\Delta E_{R_L}}{\Delta E_{in}} = \left[\frac{1}{2V_{in}(V_{C\max} - V_{C\min})} \right] [V_{C\max}(V_{O\min} + V_{O\max}) + V_{C(QB)}(V_{Of} + V_{O\min}) - V_{C\min}(V_{O\max} + V_{Of})]. \quad (51)$$

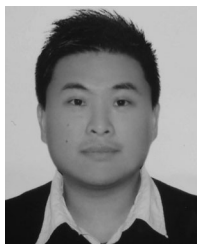
ACKNOWLEDGMENT

The authors would like to thank the anonymous reviewers for their useful comments and suggestions to enhance the content of this paper.

REFERENCES

- [1] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits Syst. Mag.*, vol. 1, no. 3, pp. 37–42, Sep. 2001.
- [2] S. V. Cheong, H. Chung, and A. Ioinovici, "Inductorless DC-to-DC converter with high power density," *IEEE Trans. Ind. Electron.*, vol. 41, no. 2, pp. 208–215, Apr. 1994.
- [3] O. C. Mak, Y. C. Wong, and A. Ioinovici, "Step-up DC power supply based on a switched-capacitor circuit," *IEEE Trans. Ind. Electron.*, vol. 42, no. 1, pp. 90–97, Feb. 1995.
- [4] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
- [5] F. H. Khan, L. M. Tolbert, and W. E. Webb, "Start-up and dynamic modeling of the multilevel modular capacitor-clamped converter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 519–531, Feb. 2010.
- [6] J. M. Henry and J. W. Kimball, "Practical performance analysis of complex switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 127–136, Jan. 2011.
- [7] S. C. Tan, S. Kiratipongvoot, S. Bronstein, A. Ioinovici, Y. M. Lai, and C. K. Tse, "Adaptive mixed on-time and switching frequency control of a system of interleaved switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 364–380, Feb. 2011.
- [8] J. Zhao, Y. Han, X. He, C. Tan, J. Cheng, and R. Zhao, "Multilevel circuit topologies based on the switched-capacitor converter and diode-clamped converter," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2127–2136, Aug. 2011.
- [9] C. P. Hsu and H. Lin, "Analytical models of output voltages and power efficiencies for multistage charge pumps," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1375–1385, Jun. 2010.
- [10] C. Govindaraju and K. Baskaran, "Efficient sequential switching hybrid-modulation techniques for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1639–1648, Jun. 2011.
- [11] A. Shukla, A. Ghosh, and A. Joshi, "Hysteresis modulation of multilevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1396–1409, May 2011.
- [12] Y. H. Liao and C. M. Lai, "Newly constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2836–2892, Sep. 2011.
- [13] J. M. Henry and J. W. Kimball, "Switched-capacitor converter state model generator," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2415–2425, May 2012.
- [14] S. Ben-Yaakov, "On the influence of switch resistances on switched-capacitor converter losses," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 638–640, Jan. 2012.
- [15] S. Ben-Yaakov, "Behavioral average modeling and equivalent circuit simulation of switched capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 632–636, Feb. 2012.
- [16] P. Midya, "Efficiency analysis of switched capacitor doubler," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Aug. 1996, vol. 3, pp. 1019–1022.
- [17] J. Chen and A. Ioinovici, "Switching-mode DC–DC converter with switched capacitor based resonant circuit," *IEEE Trans. Circuits Syst. I—Fundam. Theory Appl.*, vol. 43, no. 11, pp. 933–938, Nov. 1996.
- [18] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless DC–DC converters with a very high DC line-to-load voltage ratio," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2003, vol. 3, pp. 435–438.
- [19] C. K. Cheung, S. C. Tan, Y. M. Lai, and C. K. Tse, "A new visit to an old problem in switched-capacitor converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 3192–3195.
- [20] Y. H. Chang, "Design and analysis of power-CMOS-gate-based switched-capacitor boost DC–AC inverter," *IEEE Trans. Circuits Syst. I—Reg. Pap.*, vol. 51, no. 10, pp. 1998–2016, Oct. 2004.
- [21] S. Bin, Yujia, Y. Wang, and Z. Hong, "High efficiency, inductorless step-down DC/DC converter," in *Proc. Int. Conf. ASIC*, Oct. 2005, vol. 1, pp. 395–398.
- [22] D. Maksimovic and S. Dhar, "Switched-capacitor DC–DC converters for low-power on-chip applications," in *Proc. IEEE Power Electron. Spec. Conf.*, Jul. 1999, vol. 1, pp. 54–59.

- [23] P. Favrat, P. Deval, and M. J. Decleroq, "A high-efficiency CMOS voltage doubler," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 410–416, Mar. 1998.
- [24] O. Keiser, P. K. Steimer, and J. W. Kolar, "High power resonant switched-capacitor step-down converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 2772–2777.
- [25] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor DC–DC converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 30, no. 1, pp. 92–101, Jan. 1994.
- [26] H. Chung and A. Ioinovici, "Switched-capacitor-based DC-to-DC converter with improved input current waveform," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1996, pp. 541–544.
- [27] Y. S. Lee and Y. Y. Chiu, "Zero-current-switching switched-capacitor bidirectional DC–DC converter," *IEE Proc. Electr. Power Appl.*, vol. 152, no. 6, pp. 1525–1530, Nov. 2005.
- [28] A. Ioinovici, H. S. H. Chung, M. S. Makowski, and C. K. Tse, "Comments on 'unified analysis of switched-capacitor resonant converters,'" *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 684–685, Feb. 2007.
- [29] B. Arntzen and D. Maksimovic, "Switched-capacitor DC/DC converter with resonant gate drive," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 892–902, Sep. 1998.
- [30] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC–DC converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1995, vol. 2, pp. 1215–1221.
- [31] J. Liu, Z. Chen, and Z. Du, "A new design of power supplies for pocket computer systems," *IEEE Trans. Ind. Electron.*, vol. 45, no. 2, pp. 228–235, Apr. 1998.
- [32] Z. Pan, F. Zhang, and F. Z. Peng, "Power losses and efficiency analysis of multilevel DC–DC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2005, vol. 3, pp. 1393–1398.
- [33] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 4008–4015.
- [34] J. Han, A. v. Jouanne, and G. C. Temes, "A new approach to reducing output ripple in switched-capacitor-based step-down DC–DC converter," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1548–1555, Nov. 2006.
- [35] C. Wang and J. Wu, "Efficiency improvement in charge pump circuits," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 852–860, Jun. 1997.
- [36] G. Zhu and A. Ioinovici, "Switched-capacitor power supplies: DC voltage ratio, efficiency, ripple, regulation," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1996, pp. 553–556.
- [37] G. Zhu and A. Ioinovici, "Steady-state characteristics of switched-capacitor electronic converters," *J. Circuits Syst. Comput.*, vol. 7, no. 2, pp. 69–91, Jul. 1997.
- [38] C. K. Tse, S. C. Wong, and M. H. L. Chow, "On lossless switched-capacitor power converters," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 286–291, May 1995.
- [39] J. W. Kimball, P. T. Krein, and K. R. Cahill, "Modeling of capacitor impedance in switching converters," *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 136–140, Dec. 2005.
- [40] W. H. Ki, F. Su, and C. Y. Tsui, "Charge redistribution loss consideration in optimal charge pump design," *IEEE Int. Symp. Circuits Syst.*, vol. 2, pp. 1895–1898, May 2005.



Chun-Kit Cheung (S'09) received the B.Eng. (first class Hons.) degree in electronic and information engineering from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2008, where he is currently working toward the Ph.D. degree.

His current research interests include switched-capacitor converters and field-programmable gate array control applications.



Siew-Chong Tan (S'00–M'06–SM'11) received the B.Eng. (Hons.) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, Singapore, in 2000 and 2002, respectively, and the Ph.D. degree in electronic and information engineering from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2005.

From October 2005 to May 2012, he was a Research Associate, Postdoctoral Fellow, Lecturer, and an Assistant Professor in the Department of Electronic and Information Engineering, The Hong Kong

Polytechnic University. From January to October 2011, he was a Senior Scientist in Agency for Science, Technology and Research (A*Star), Singapore. He was a Visiting Scholar at Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, Champaign, from September to October 2009, and an Invited Academic Visitor of the Huazhong University of Science and Technology, Wuhan, China, in December 2011. He is currently an Associate Professor in the Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam, Hong Kong. He is a coauthor of the book *Sliding Mode Control of Switching Power Converters: Techniques and Implementation* (Boca Raton, FL: CRC Press, 2011). His research interests are focused in the areas of power electronics and control, LED lightings, smart grids, and clean energy technologies.

Dr. Tan serves extensively as a reviewer for various IEEE/IET transactions and journals on power, electronics, circuits, and control engineering.



Chi K. Tse (M'90–SM'97–F'06) received the B.Eng. (first class Hons.) degree in electrical engineering and the Ph.D. degree from the University of Melbourne, Melbourne, Vic., Australia, in 1987 and 1991, respectively.

He is currently a Chair Professor and the Head of the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong. He is the author of the books *Linear Circuit Analysis* (London, U.K.: Addison-Wesley, 1998) and *Complex Behavior of Switching*

Power Converters (Boca Raton, FL: CRC Press, 2003), coauthor of *Chaos-Based Digital Communication Systems* (Heidelberg, Germany: Springer-Verlag, 2003), *Digital Communications With Chaos* (London, U.K.: Elsevier, 2006), *Reconstruction of Chaotic Signals With Applications to Chaos-Based Communications* (Singapore: World Scientific, 2007), and *Sliding Mode Control of Switching Power Converters: Techniques and Implementation* (Boca Raton, FL: CRC Press, 2010), and coholder of four U.S. patents and two other pending patents. In 2011, he became the Honorary Professor at RMIT University, Melbourne, Vic., Australia. His research interests include complex network applications, power electronics, and chaos-based communications.

Dr. Tse received the L.R. East Prize from the Institution of Engineers, Australia, in 1987, the Best Paper Award from the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2001 and the Best Paper Award from the *International Journal of Circuit Theory and Applications* in 2003. In 2005 and 2011, he was selected and appointed as the IEEE Distinguished Lecturer. In 2007, he was awarded the Distinguished International Research Fellowship by the University of Calgary, Canada. In 2009, he and his coinventors won the Gold Medal with Jury's Commendation at the International Exhibition of Inventions of Geneva, Switzerland, for a novel driving technique for LEDs. In 2010, he was appointed the Chang Jiang Scholar Chair Professorship by the Ministry of Education of China and the appointment is hosted by the Huazhong University of Science and Technology, Wuhan, China. He serves as the Editor-in-Chief of the IEEE CIRCUITS AND SYSTEMS MAGAZINE and the Editor-in-Chief of the IEEE Circuits and Systems Society Newsletter. He was an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART I: FUNDAMENTAL THEORY AND APPLICATIONS from 1999 to 2001 and again from 2007 to 2009. He has also been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1999. He is an Associate Editor of the *International Journal of Systems Science*, and is also on the Editorial Board of the *International Journal of Circuit Theory and Applications* and *International Journal and Bifurcation and Chaos*. He also served as a Guest Editor and a Guest Associate Editor for a number of special issues in various journals. In 2008, he was the Chairman of the Technical Committee on Nonlinear Circuits and Systems of the IEEE Circuits and Systems Society.



Adrian Ioinovici (M'84–SM'85–F'04) received the B.Eng. degree in electrical engineering and the Doctor-Engineer degree from Polytechnic University, Iasi, Romania, in 1974 and 1981, respectively.

In 1982, he joined the Holon Institute of Technology, Holon, Israel. He served for several terms as the Head of the Department, and in 2007 as the Dean of the Faculty of Engineering. During 1990–1995, he was a reader and then a Professor in the Department of Electrical Engineering, The Hong Kong Polytechnic University. He is currently working in the National

Center for Power Electronics and Energy, Sun Yat-Sen University, Guangzhou, China. He is the author of the books *Computer-Aided Analysis of Active Circuits* (New York: Marcel Dekker, 1990), *Power Electronics and Energy Conversion Systems*, Volume 1: *Fundamentals and Hard-switching Converters* (New York: Wiley, Oct. 2012, to be published), and of the chapter *Power Electronics* in the *Encyclopedia of Physical Science and Technology* (San Francisco, CA: Academic, 2001). He has published more than 150 papers in circuit theory and power electronics. He is in great demand as a Lecturer and gave seminars at many universities in U.S., Canada, Brazil, Europe, Korea, China, and Japan. His research interests include the simulation of power electronics circuits, switched-capacitor-based converters and inverters, soft-switching dc power supplies, and three-level converters.

Dr. Ioinovici has served a few terms as the Chairman of the Technical Committee on Power Systems and Power Electronics of the IEEE Circuits and Systems Society (CAS–S). He served repetitive terms as an Associate Editor for power electronics of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I and as an Associate Editor for power electronics of the *Journal of Circuits,*

Systems, and Computers. He served as an IEEE CAS–S Distinguished Lecturer from 1999 to 2002. He has been an Overseas Advisor of the Institute of Electrical, Information and Communication Engineers Transactions, Japan. He was the Chairman of the Israeli chapter of the IEEE CAS–S between 1985 and 1990, and served as the General Chairman of the Israel Symposium on Circuits Systems and Control Conferences, Herzlyia, Israel (ISCSC'86 and ISCSC'88), SPEC'94 (Hong Kong), organized and chaired special sessions in power electronics at International Symposium on Circuits and Systems (ISCAS'91), ISCAS'92, ISCAS'95, ISCAS'2000, and was a member of the Technical Program Committee at the Conferences ISCAS'91–ISCAS'95, ISCAS'06, PESC'92–PESC'95, track Chairman at ISCAS'96, ISCAS'99–ISCAS'2005, Co-Chairman of the Special Session's Committee at ISCAS'97, chaired sessions at almost all ISCAS in the years 1991–2011, member of technical committee and session chair at Power Electronics Specialists Conference (PESC'06–PESC'08), international program committee member International Association of Science and Technology for Development (IASTED'04–IASTED'10), international advisory committee member IEEE Conference on Industrial Electronics and Applications (2006–2009), of International Power Electronics and Motion Control Conference (IPEMC'09), and of International Symposium on Power Electronics for Distributed Generation Systems 2010, Co-Chairman of the Tutorial Committee at ISCAS'06, and Co-Chair, Special Session Committee at ISCAS'10, Paris, France. He was a Guest Editor of special issues of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I (August 1997 and August 2003) and a special issue on *Power Electronics of Journal of Circuits, System and Computers* (August 2003). He was invited to give the keynote speech at the 19th China Power Supply Society Conference, Shanghai, China, November 2011, and IPEMC Energy Conversion Congress and Exposition Asia 2012, Harbin, China.